Funções e Portas Lógicas

prof. Michel Robert Veiga

Portas lógicas

- E ou AND
- OU ou OR
- NÃO ou NOT
- NÃO E, NE ou NAND
- NÃO OU, NOU ou NOR

Estados

- **0 e 1**
  - Verdadeiro e falso
  - Portão aberto e fechado
  - Aparelho ligado e desligado
  - Ausência e presença de tensão

  Obs: ausência de tensão não é o mesm o que circuito aberto, e sim ligado ao terra ou negativo do circuito.

Eletrônica
E ou AND

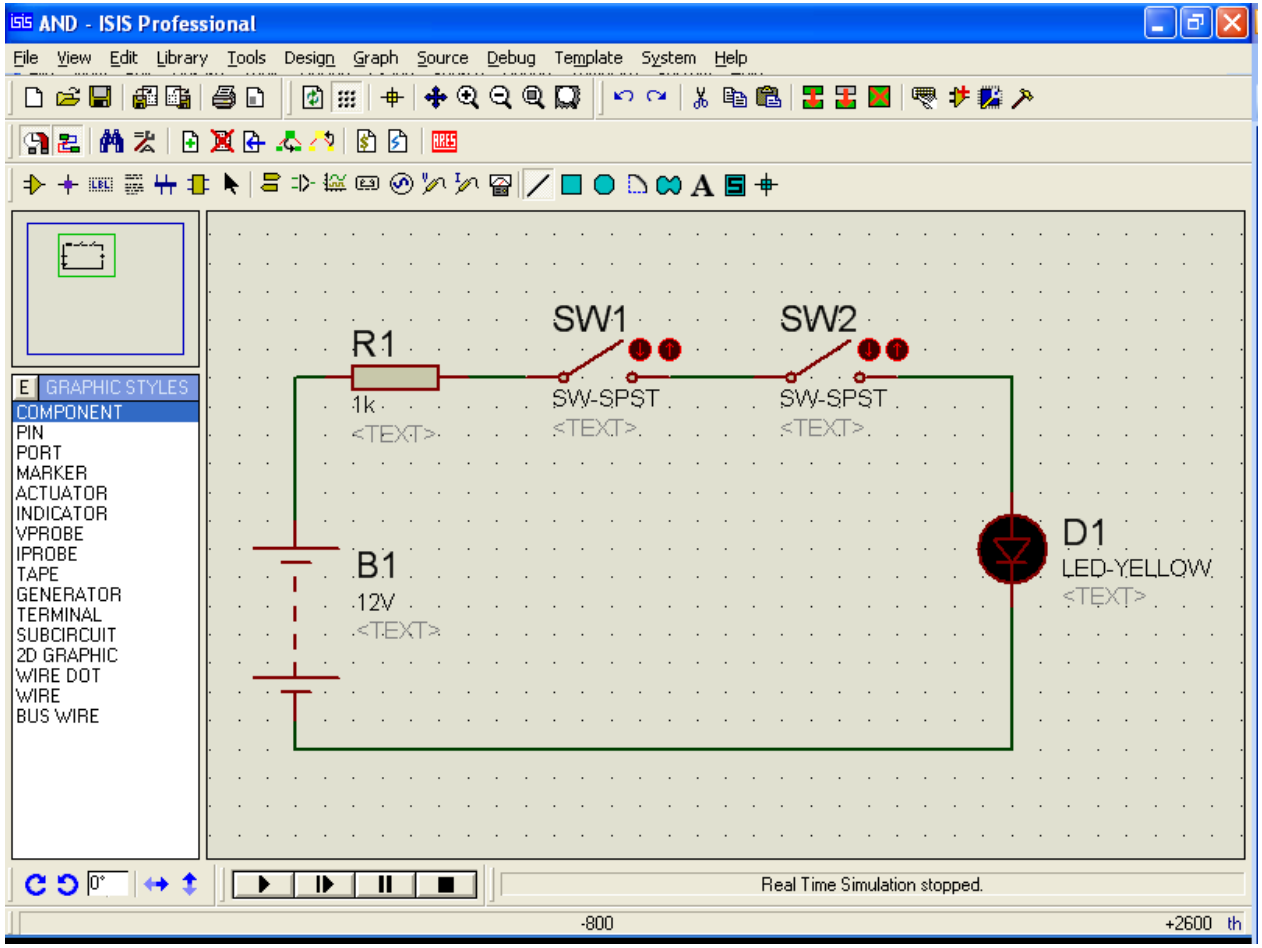


Tabela Verdade
E ou AND

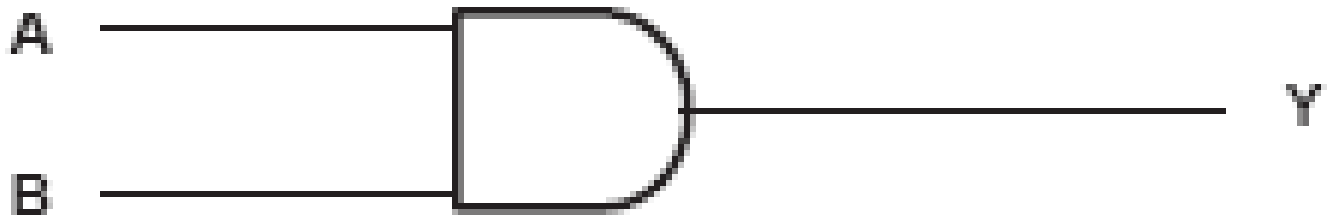
- 1 na saída sempre que todas entradas iguais a 1

A	B	S
0	0	0
0	1	0
1	0	0
1	1	1

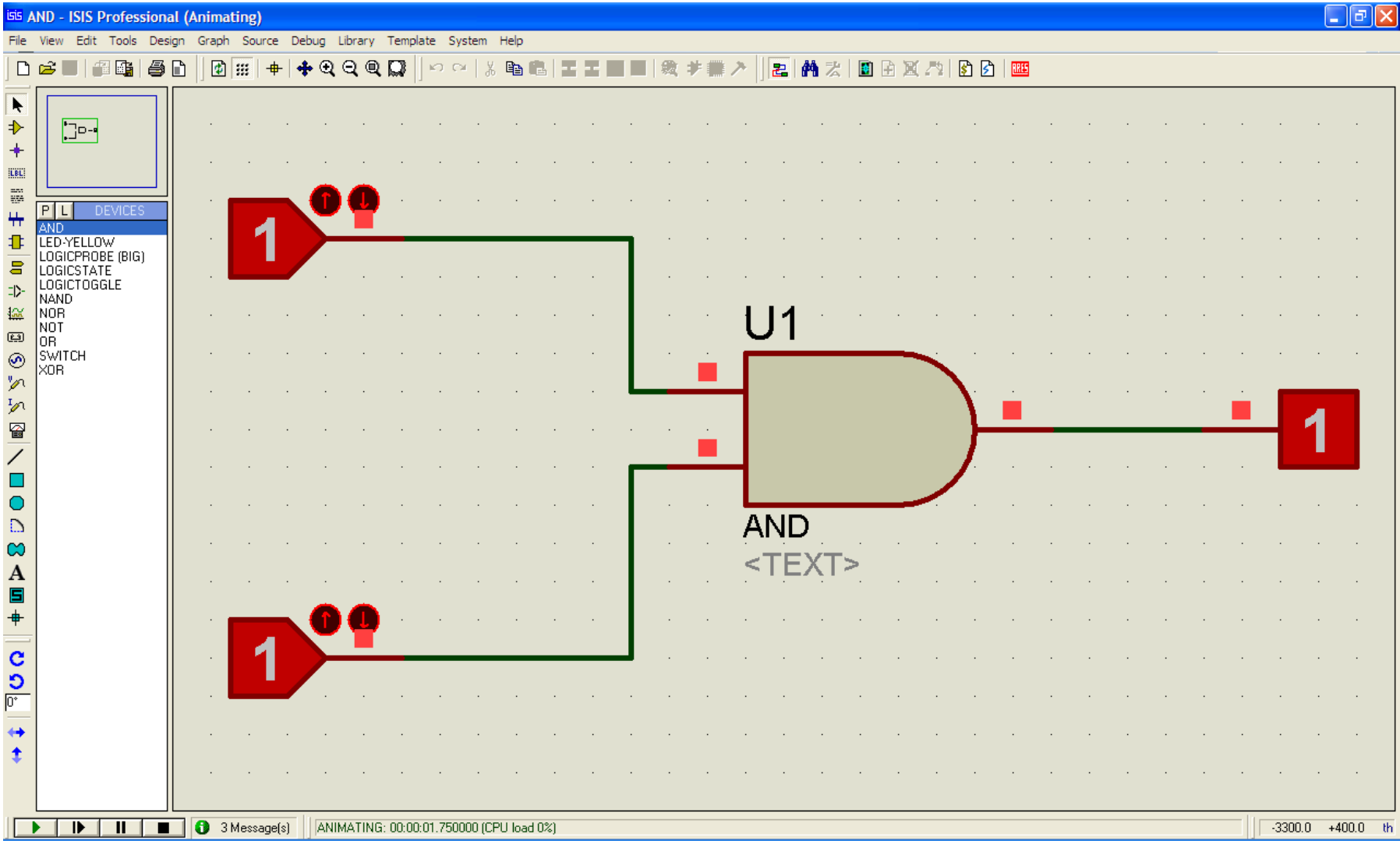
INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

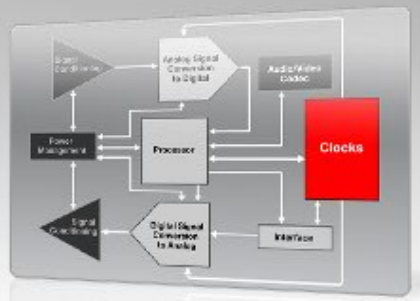
Simbologia
E ou AND

- Y = A.B



Simulação
E ou AND





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Industrial
Medical
Security
Space, Avionics, & Defense
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Logic

Cross Reference · Logic Design Support · Logic Packaging · Selection & Solution Guides · Application Notes

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Product Tree

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- Inverting Buffers and Drivers (211)
- Non-Inverting Buffers and Drivers (313)
- Parity Transceivers (10)
- Registered Transceivers (122)
- Standard Transceivers (194)

Flip-Flops, Latches and Registers (482)
- D-Type (3-State) Flip-Flops (141)
- D-Type Flip-Flops (97)
- D-Type Latches (132)
- J-K Flip-Flops (26)
- Other Latches (18)
- Shift Registers (69)

Gates (317)
- AND Gates (70)
- Configurable Gates (6)
- Exclusive NOR Gates (XNOR) (4)
- Exclusive OR Gates (XOR) (29)
- NAND Gates (110)
- NOR Gates (51)
- OR Gates (48)

Find a Device by Technology Family

- Select a Technology Family - Go

View all technology families

Logic Design Support

see all

Selection & Solution Guides

Logic Selection Guide 2007 (Rev. Z) (4462 KB)

Standard Linear & Logic 5-Minute Guide (786 KB)

more

Other Technical Documents

- Application Notes
- Models
- User Guides
- Block Diagrams

New Products

see all

SN74AVC2T245: Dual-Bit Dual-Supply Bus Transceiver With Configurable Voltage Translation and 3-State Outputs

SN74AVC4T774: 4-Bit Dual-Supply Bus Transceiver With Configurable Voltage Translation and 3-State Outputs

SN74AUP2G08: Low-Power Dual 2-Input Positive-AND Gate

SN74AUP2G126: Low-Power Dual Bus Buffer Gate With 3-State Outputs

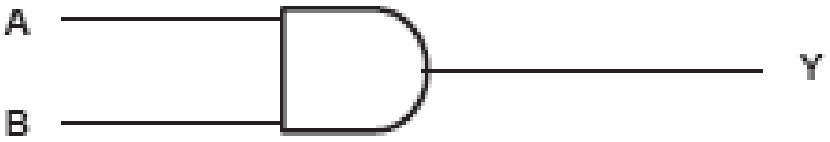
TXS0101: 1-Bit Bidirectional Voltage-Level Translator for Open-Drain Application

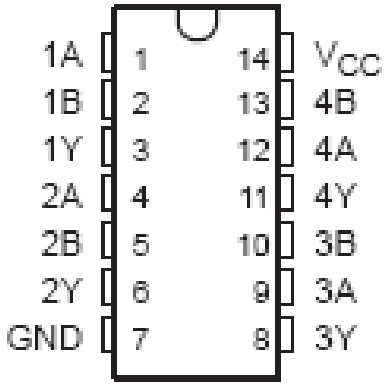
TXS0102: 2-Bit Bidirectional Voltage-Level Translator for Open-Drain Application

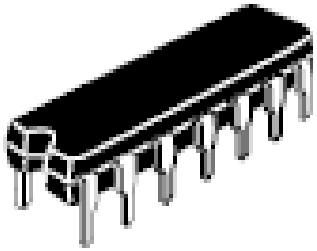
TXS0104E: 4-Bit Bidirectional Voltage-Level Translator for Open-Drain Applications

SN74AC08
Texas Instruments

- Quadruple 2-Input Positive AND Gates
- Ver data sheet – folha de dados - sn74ls08.pdf







OU ou OR

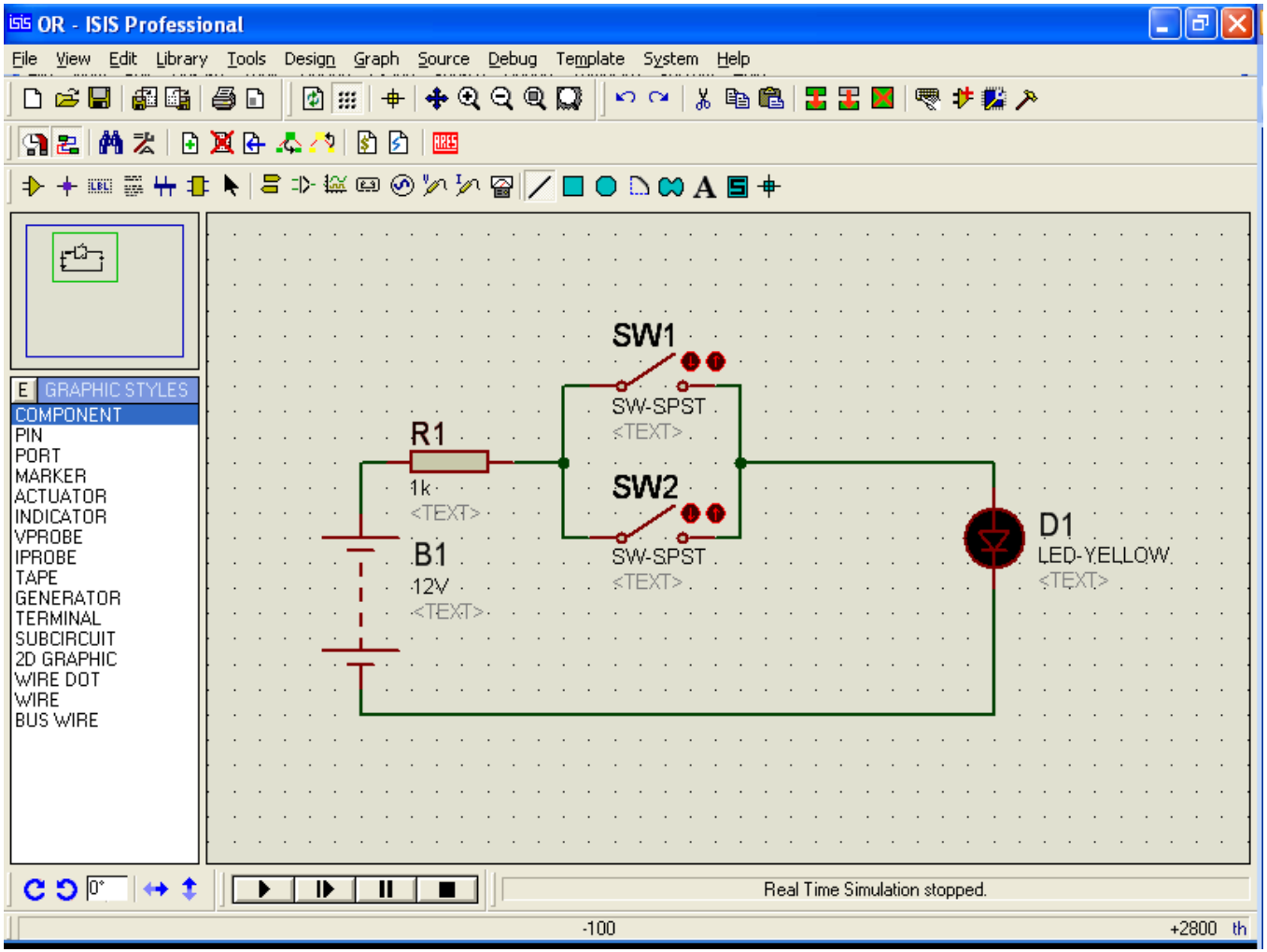

OR - ISIS Professional
File View Edit Library Tools Design Graph Source Debug Template System Help
SW1
SW-SPST
<TEXT>
R1
1k
<TEXT>
SW2
SW-SPST
<TEXT>
B1
12V
<TEXT>
D1
LED-YELLOW
<TEXT>
E GRAPHIC STYLES
COMPONENT
PIN
PORT
MARKER
ACTUATOR
INDICATOR
VPROBE
IPROBE
TAPE
GENERATOR
TERMINAL
SUBCIRCUIT
2D GRAPHIC
WIRE DOT
WIRE
BUS WIRE
Real Time Simulation stopped.
-100
+2800 th

Tabela Verdade
OU ou OR

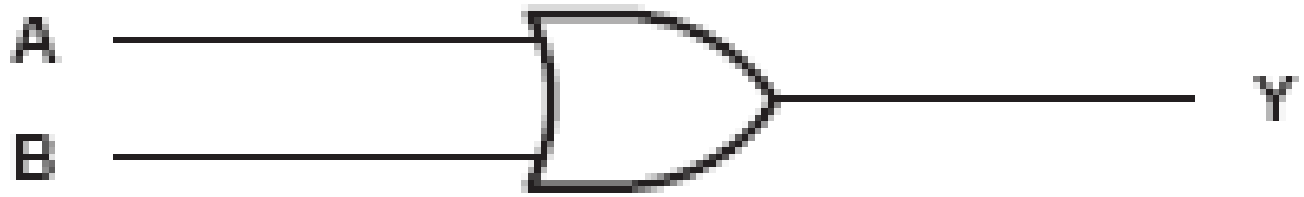
- 1 na saída sempre que pelo menos uma entrada igual a 1

A	B	S
0	0	0
0	1	1
1	0	1
1	1	1

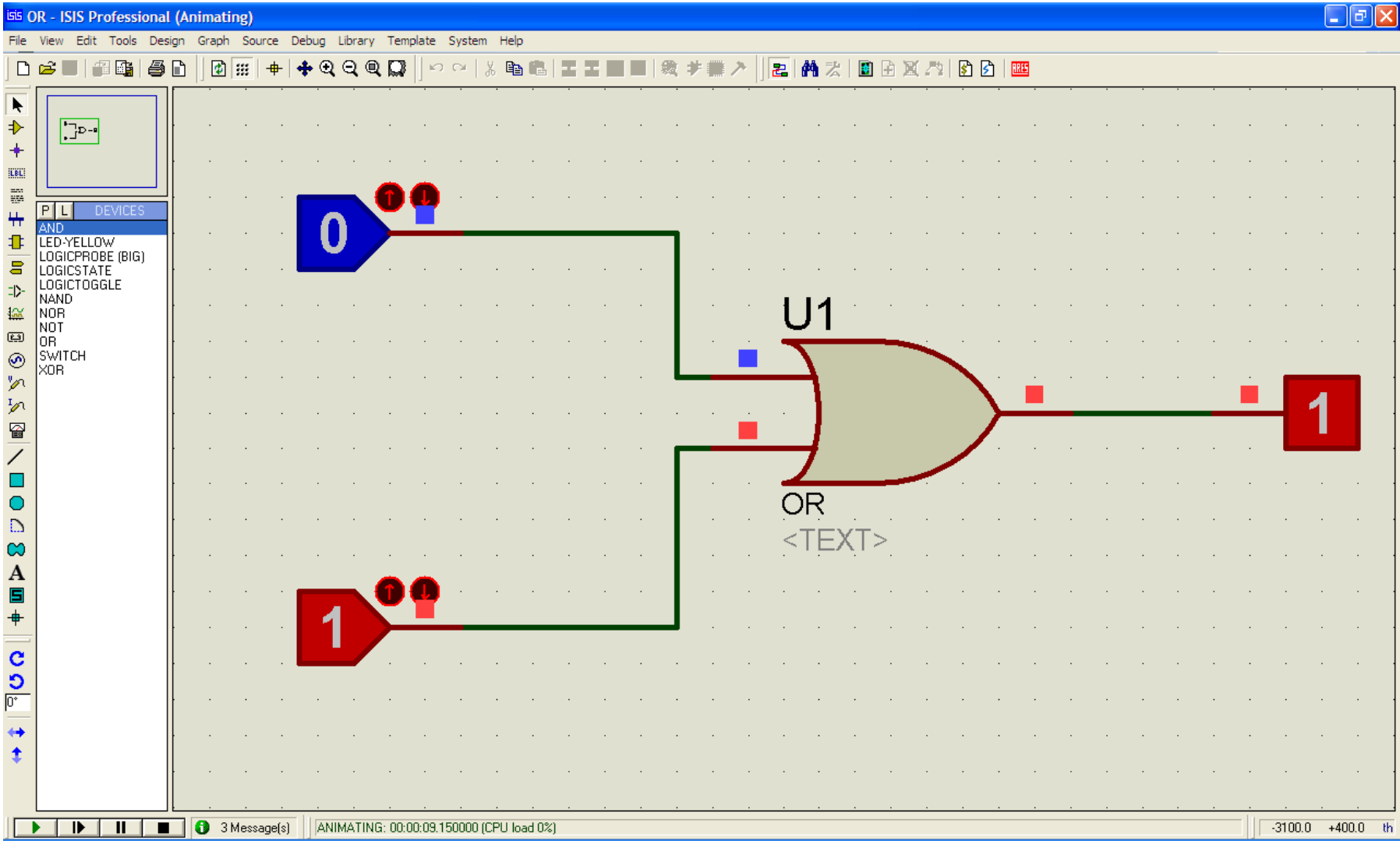
INPUTS		OUTPUT
A	B	Y
H	X	H
X	H	H
L	L	L

Simbologia
OU ou OR

- Y = A + B

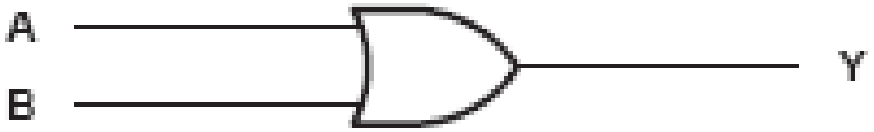


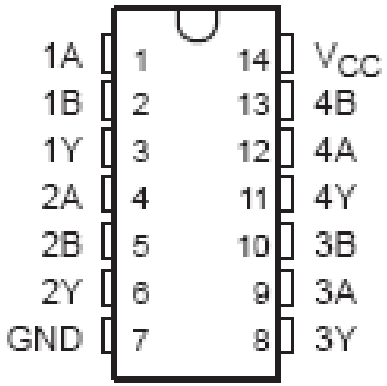
Simulação
OU ou OR

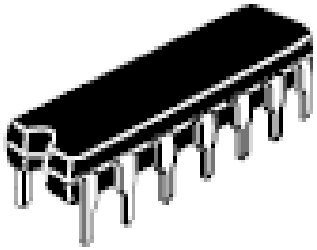


SN74AC32
Texas Instruments

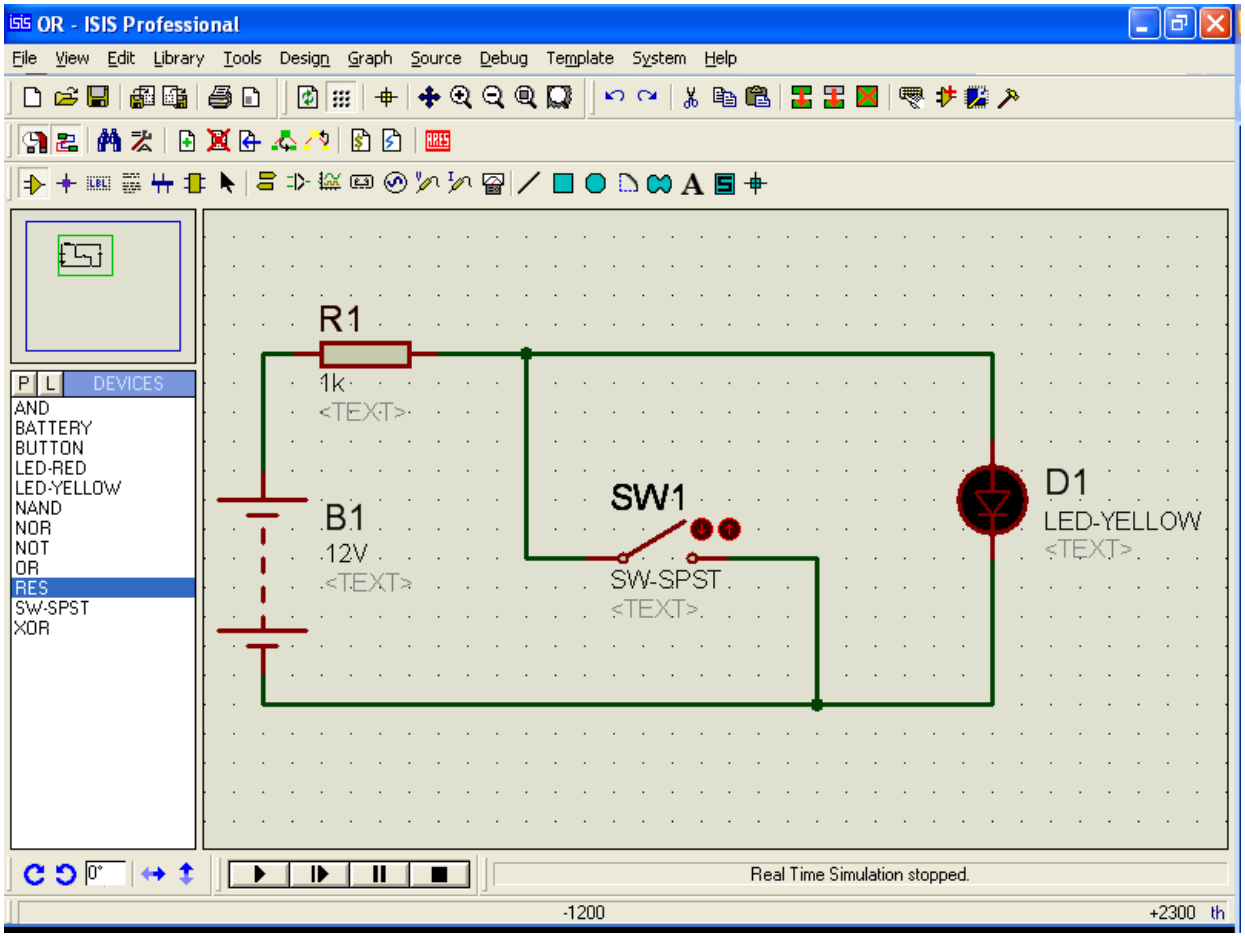
- Quadruple 2-Input Positive OR Gates
  - *sn74ac32 - OR.pdf*







Eletrônica
NÃO ou NOT



- *NOT.DSN*

Tabela Verdade
NÃO ou NOT

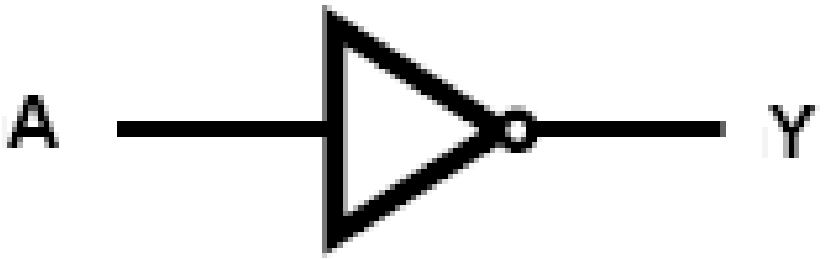
- Saída igual inverso da entrada

A	S
0	1
1	0

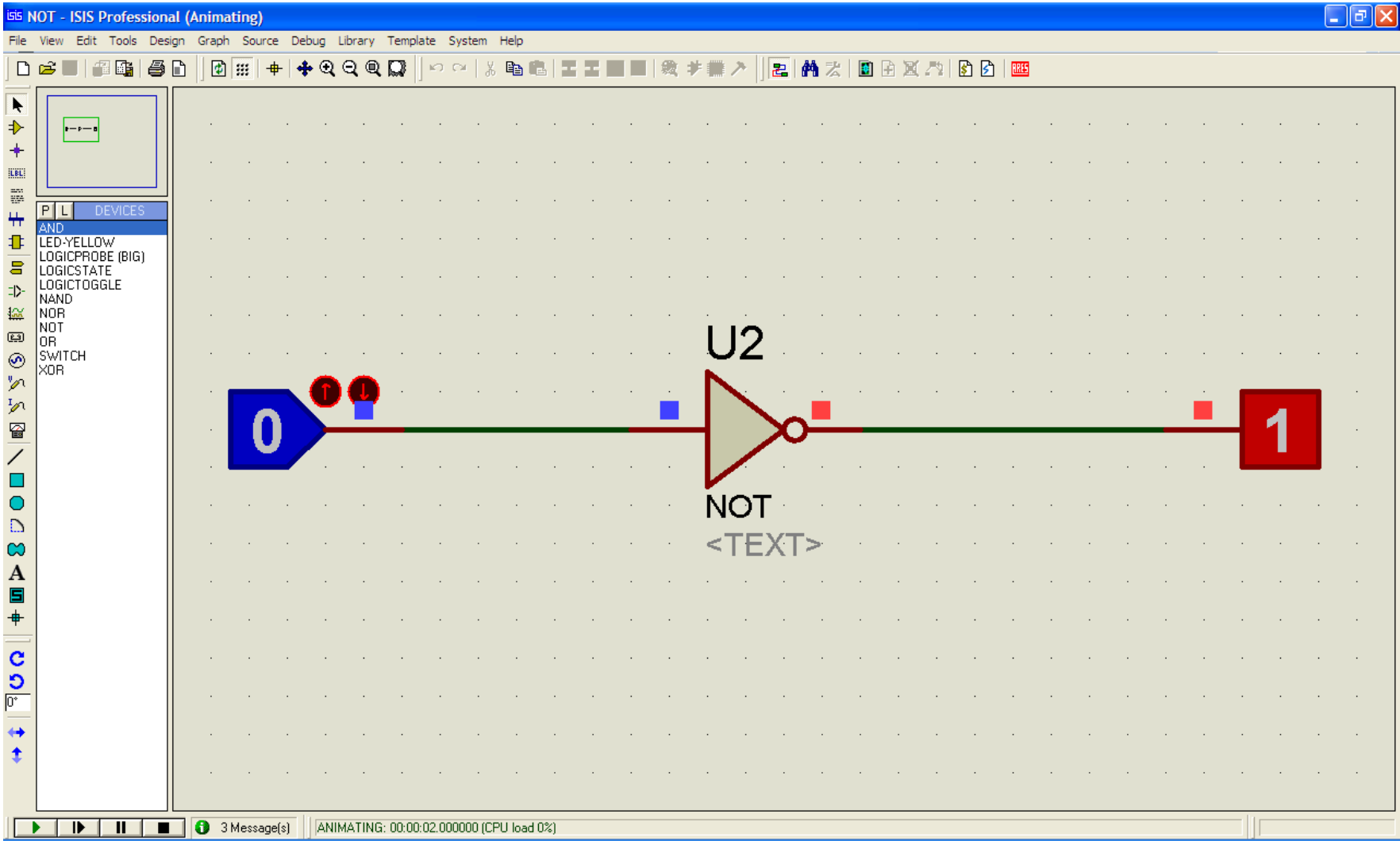
INPUT A	OUTPUT Y
H	L
L	H

Simbologia
NÃO ou NOT

- $Y = \overline{A}$
- Y = A`

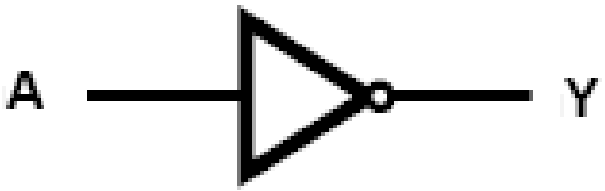


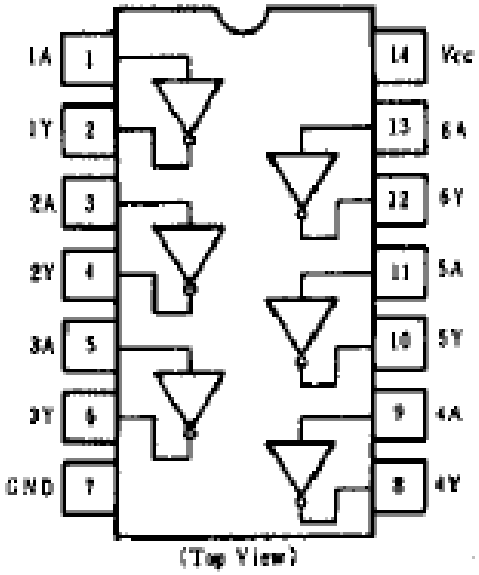
Simulação
NÃO ou NOT

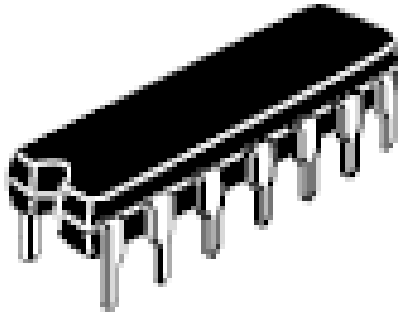


HD74LS04
Hitachi

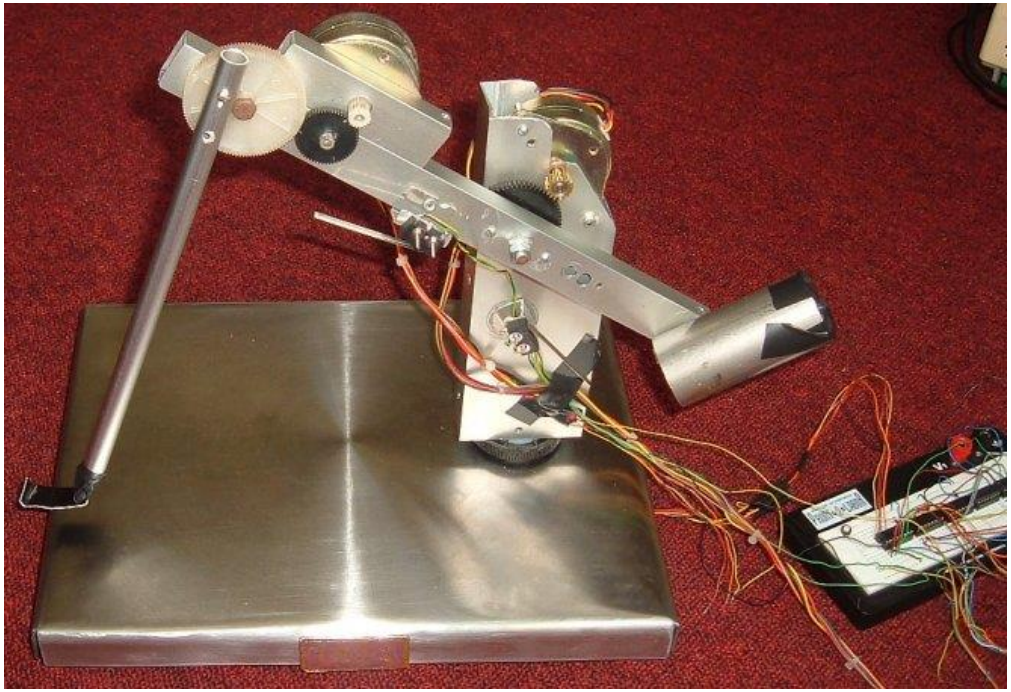
- NOT Gates
  - *HD74LS04.pdf*







Exemplo Prático



Problema do Motor de Passo

- Dados do problema:
  - Um motor de passo de 4 fios pode ser ativado de 3 formas diferentes
    - Passo completo 1
    - Passo completo 2
    - Meio Passo
  - Seu acionamento pode ser feito via porta paralela do computador que tem 8 bits de saída
  - Para acionar 2 motores com 4 bits cada utiliza-se todos os 8 bits da porta paralela
  - Pergunta-se, utilizando o conhecimento de portas NOT, como é possível ativar mais de 2 motores?

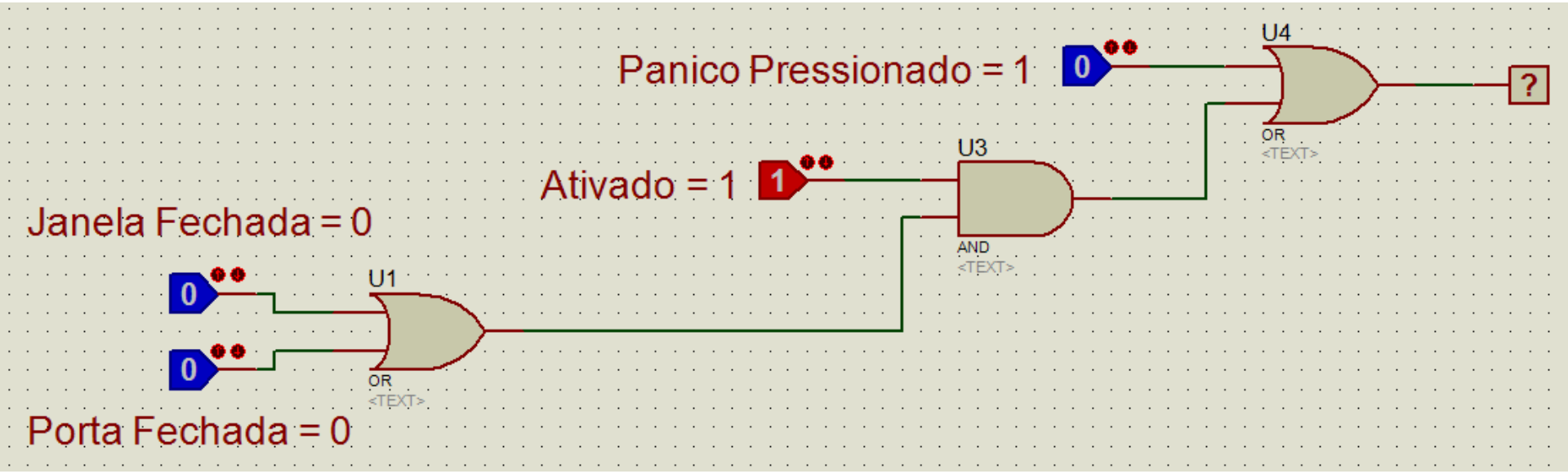
Problema do Motor de Passo

Passo completo 1				
tempo	b1	b2	b3	b4
t1	1	0	0	0
t2	0	1	0	0
t3	0	0	1	0
t4	0	0	0	1

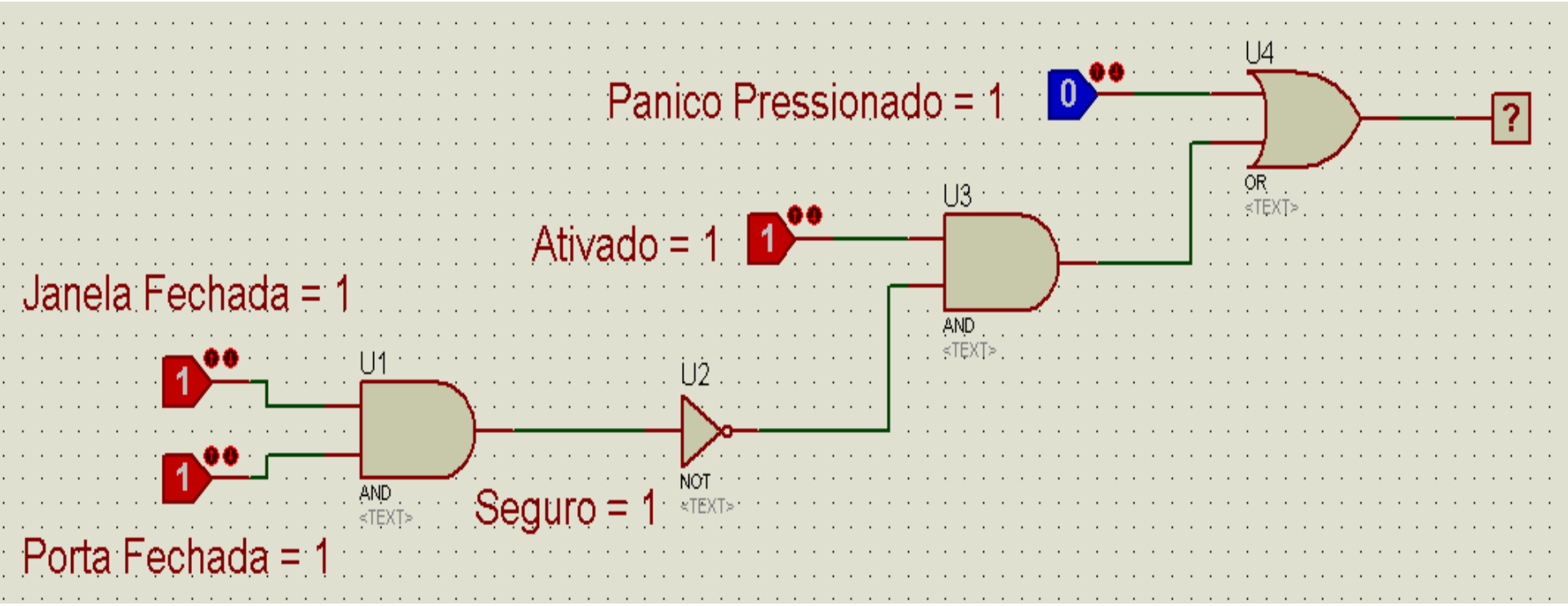
Passo completo 2				
tempo	b1	b2	b3	b4
t1	1	1	0	0
t2	0	1	1	0
t3	0	0	1	1
t4	1	0	0	1

Meio Passo				
tempo	b1	b2	b3	b4
t1	1	0	0	0
t2	1	1	0	0
t3	0	1	0	0
t4	0	1	1	0
t5	0	0	1	0
t6	0	0	1	1
t7	0	0	0	1
t8	1	0	0	1

Exercício


Panico Pressionado = 1
0
U4
OR
<TEXT>
?
Ativado = 1
1
U3
AND
<TEXT>
Janela Fechada = 0
0
0
U1
OR
<TEXT>
Porta Fechada = 0

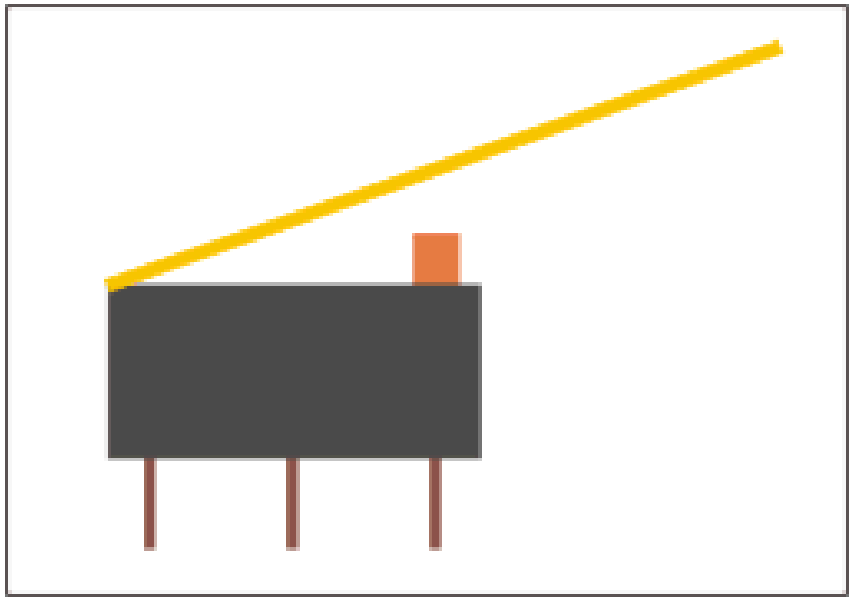
Exercício


Panico Pressionado = 1
0
U4
OR
<TEXT>
?
Ativado = 1
1
U3
AND
<TEXT>
Janela Fechada = 1
1
U1
AND
<TEXT>
U2
NOT
<TEXT>
Seguro = 1
1
Porta Fechada = 1

A	B	C	D	S
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	
0	0	0	0	

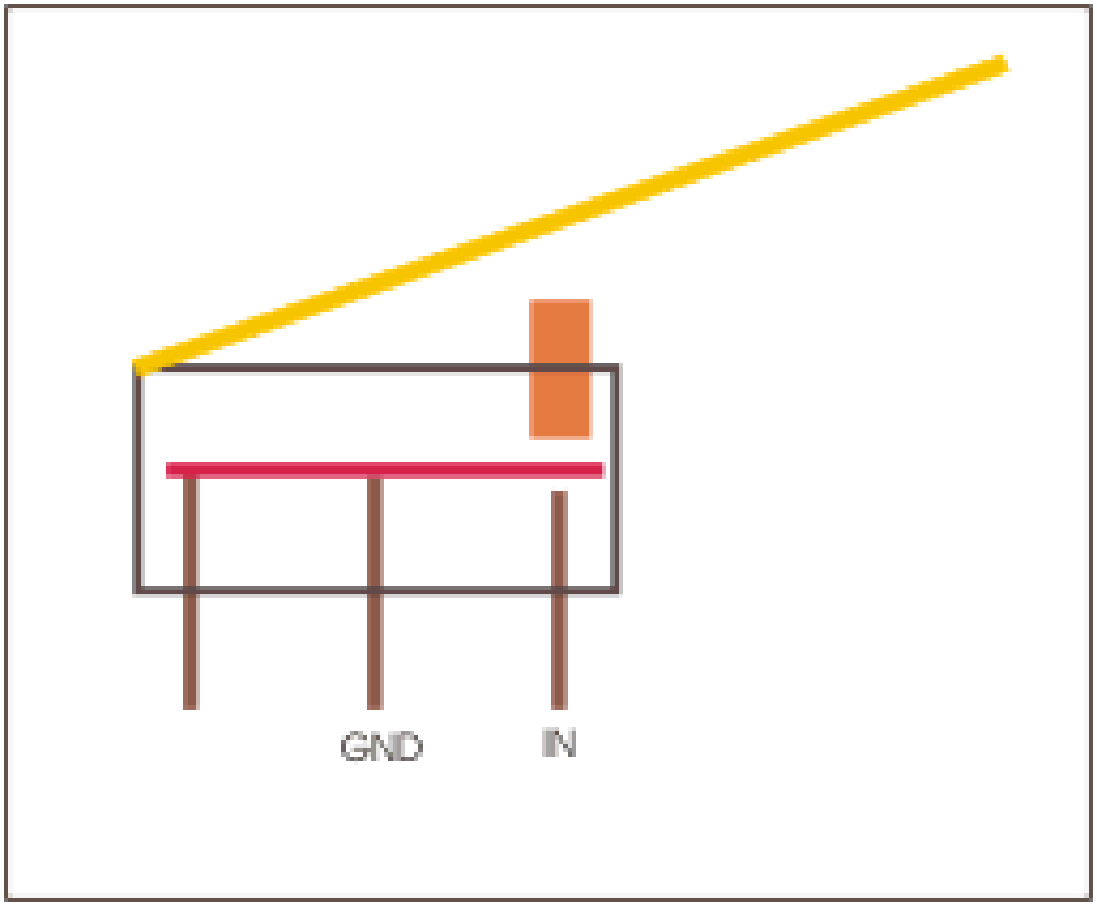
Sensor de fim de curso

- Sensor mecânico de toque
- Detectar final de curso
- Pode ser usado como referência 0 (zero)



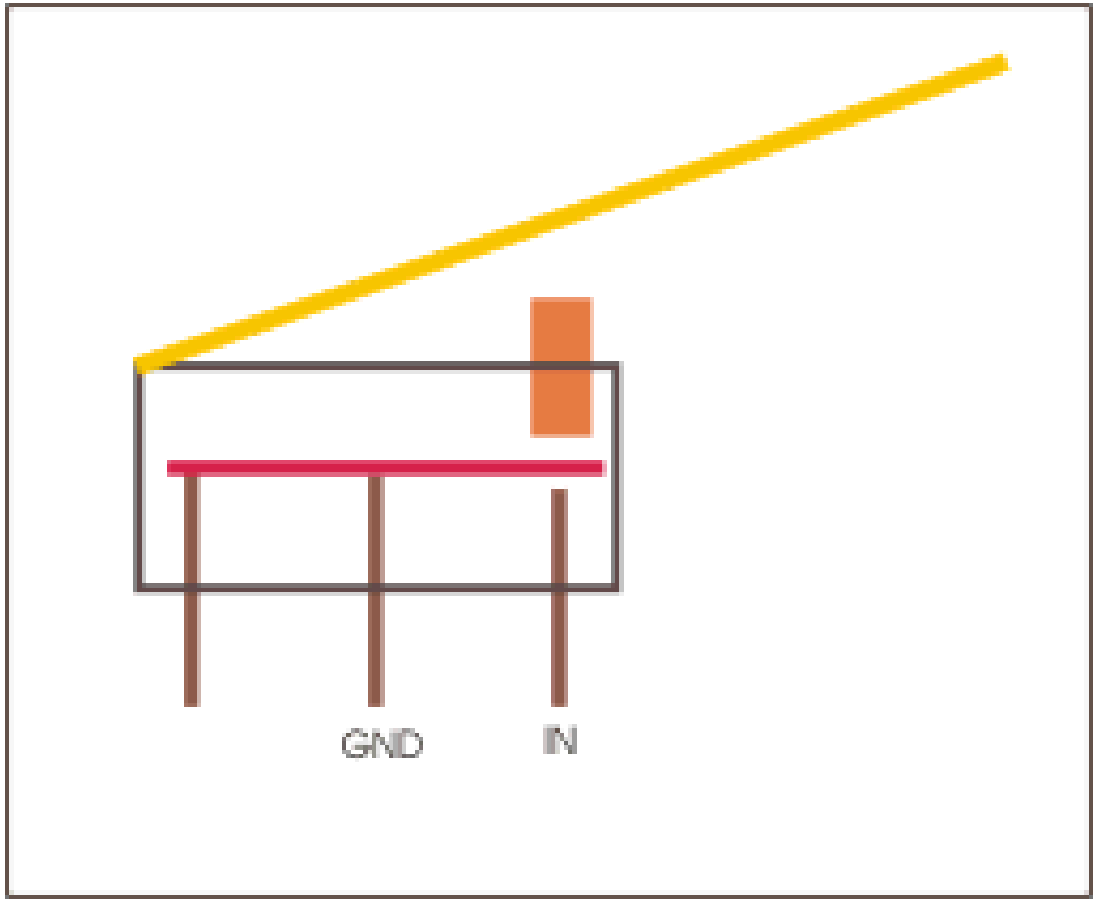
Sensor de fim de curso

NA – Normal Aberto



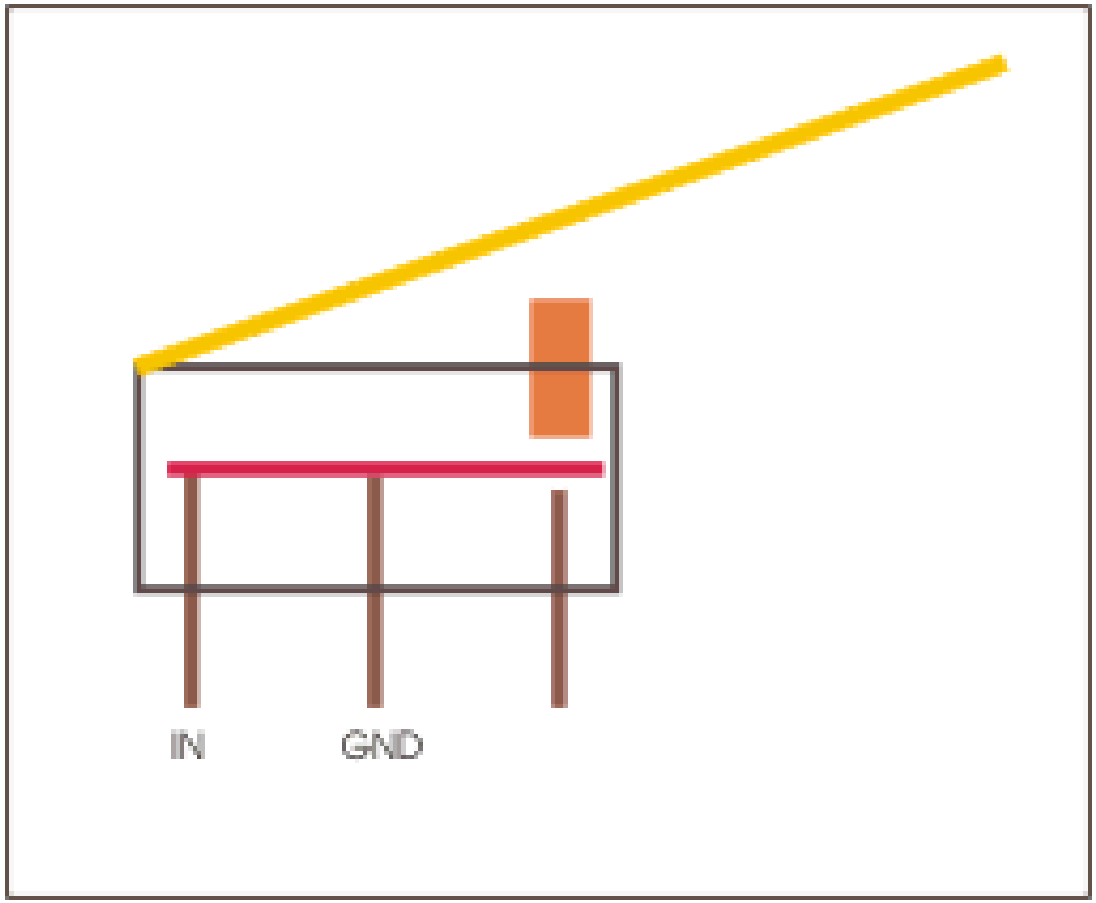
Sensor de fim de curso

NA – Normal Aberto



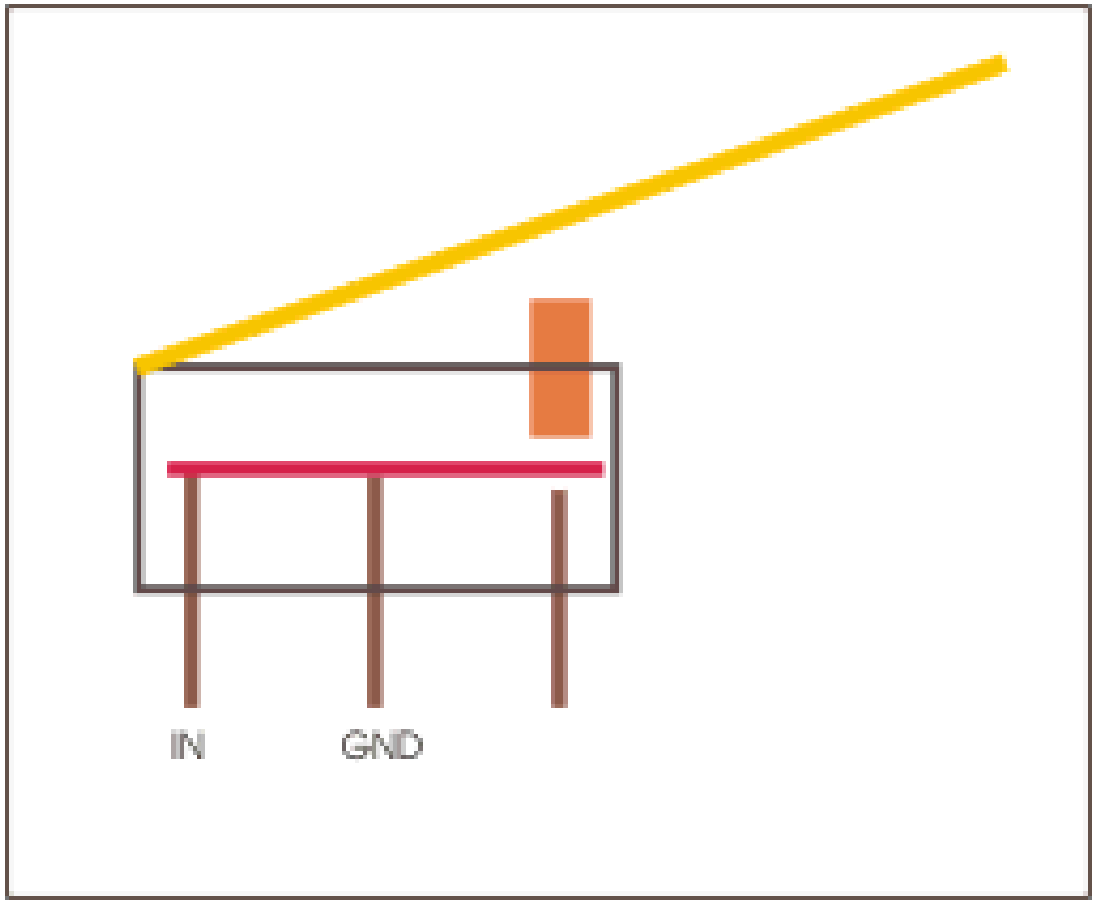
Sensor de fim de curso

NF – Normal Fechado

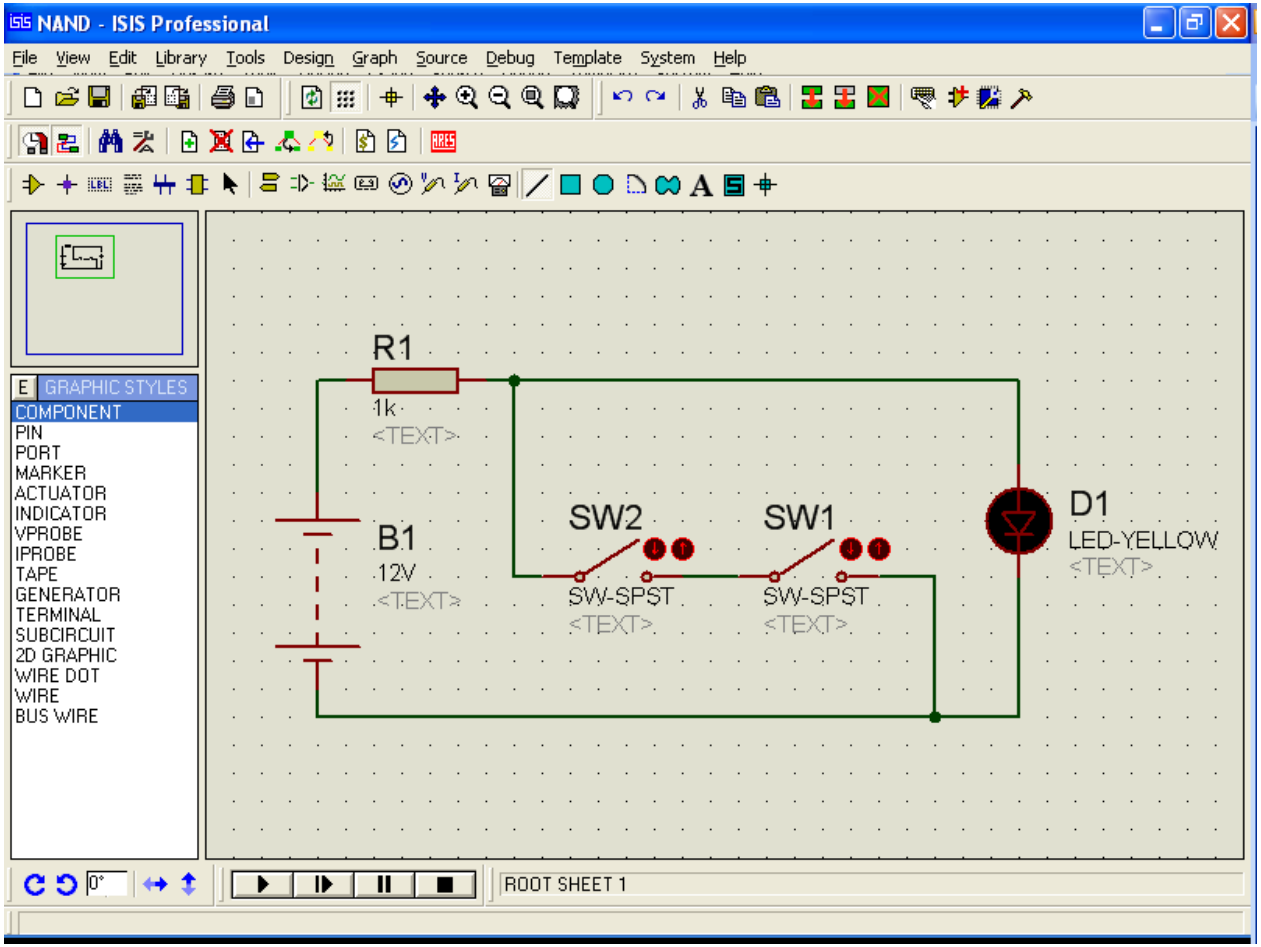


Sensor de fim de curso

NF – Normal Fechado



Eletrônica
NÃO E, NE ou NAND



- NAND.DSN

Tabela Verdade
NÃO E, NE ou NAND

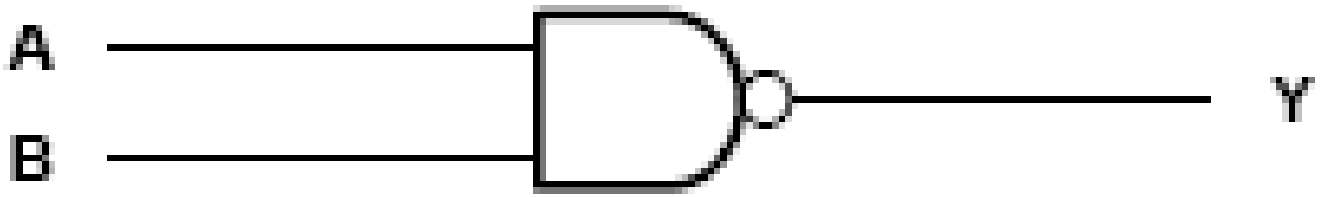
- Inverso da função AND

A	B	S
0	0	1
0	1	1
1	0	1
1	1	0

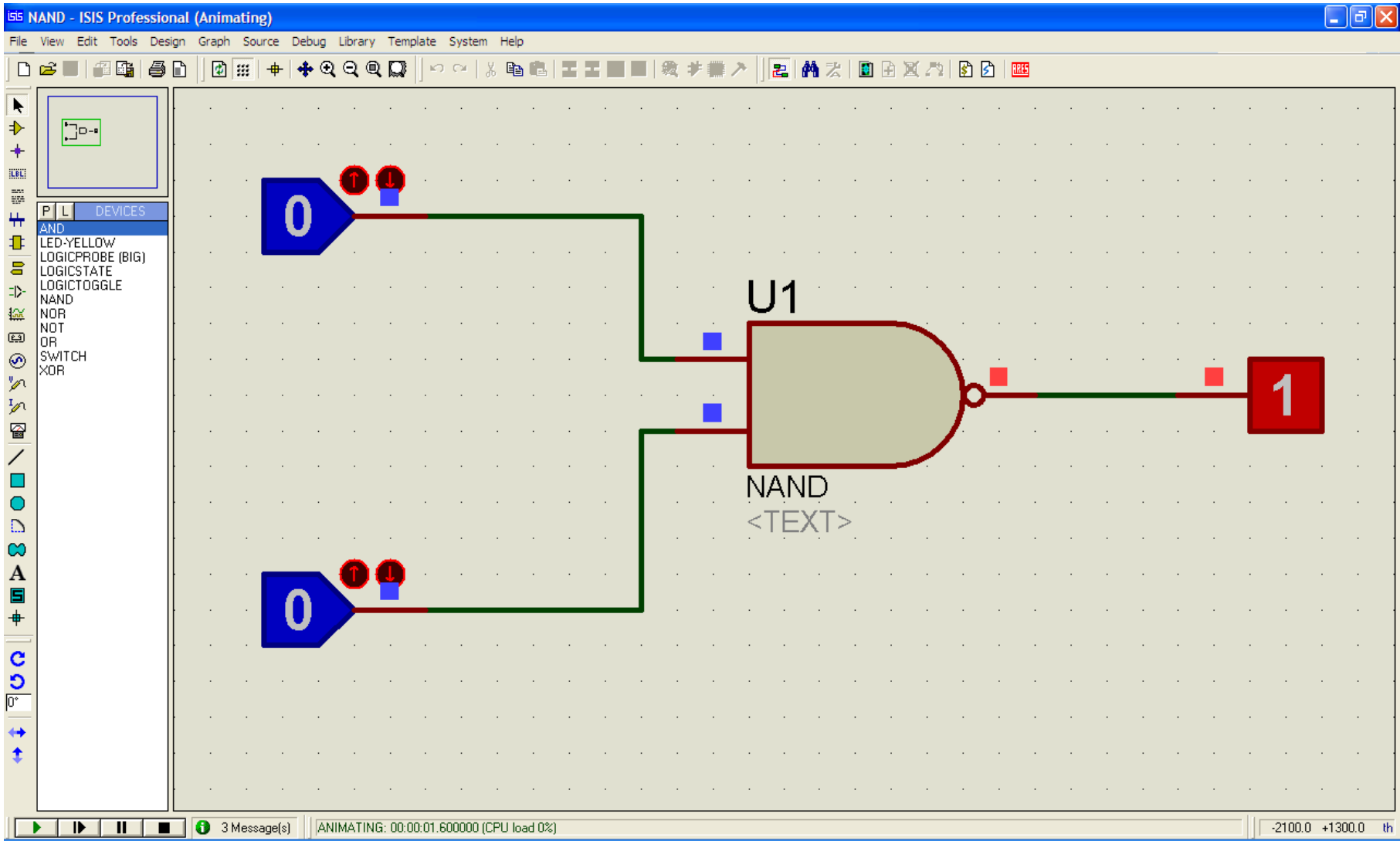
INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

Simbologia
NÃO E, NE ou NAND

- $Y = (\overline{A.B})$
- $Y = (A.B)'$

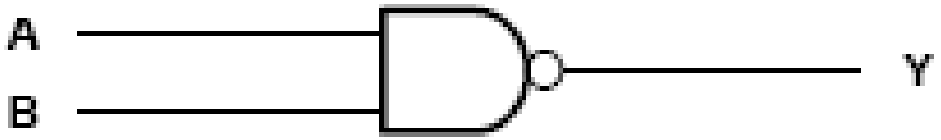


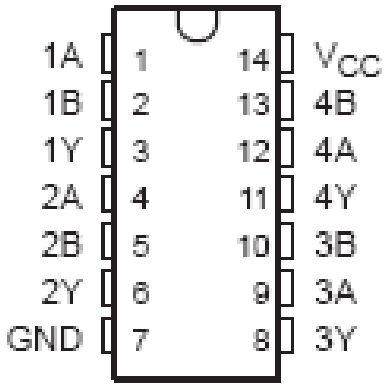
Simulação
NÃO E ou NAND

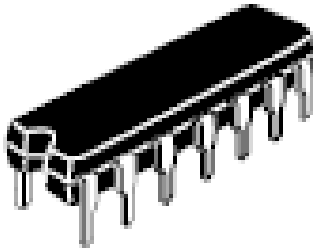


SN74LVC00
Texas Instruments

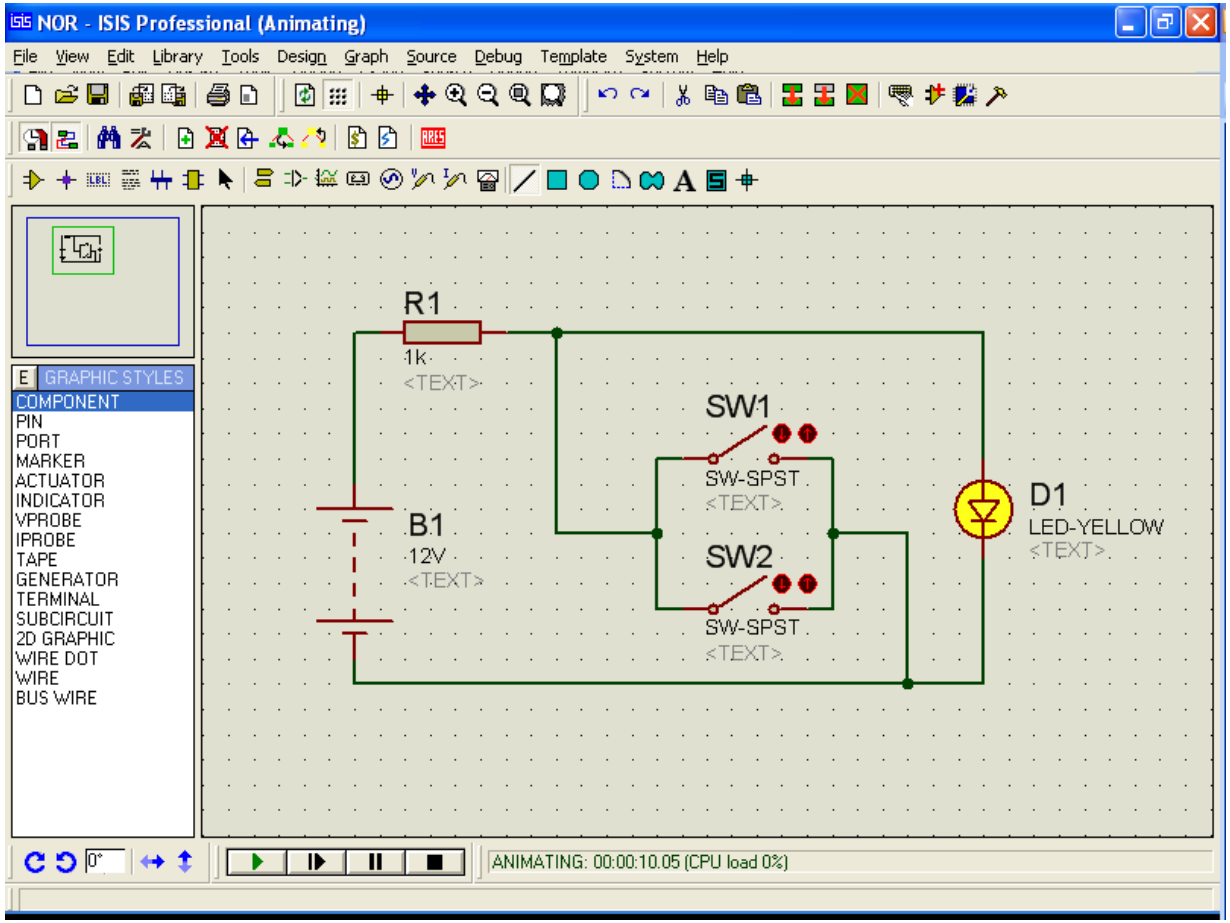
- Quadruple 2-Input Positive NAND Gates
  - *sn74lvc00a - NAND.pdf*







Eletrônica
NÃO OU, NOU ou NOR



- NOR.DSN

Tabela Verdade
NÃO OU, NOU ou NOR

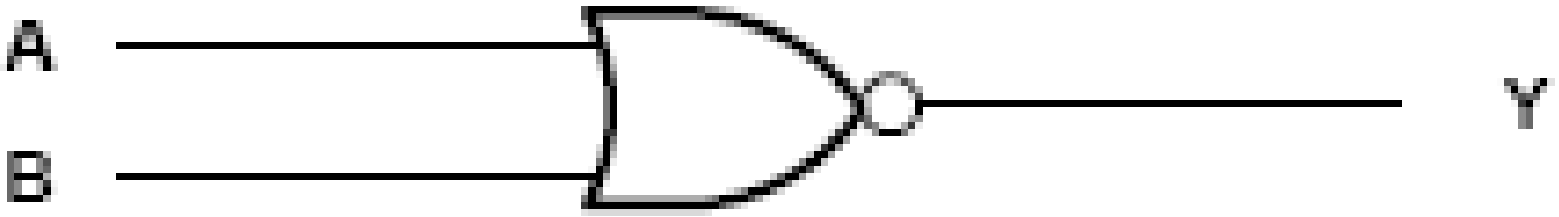
- Inverso da função OU

A	B	S
0	0	1
0	1	0
1	0	0
1	1	0

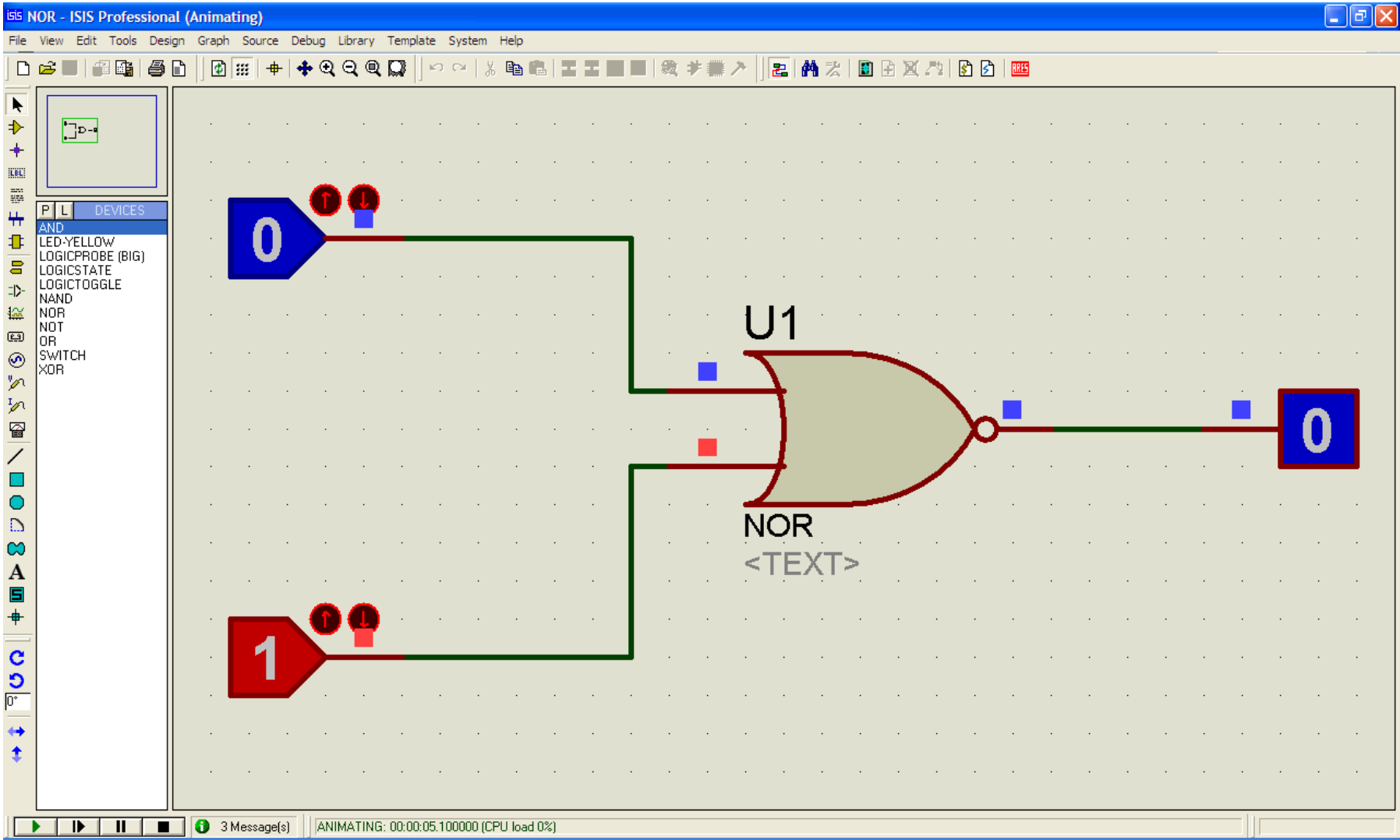
INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

Simbologia
NÃO OU, NOU ou NOR

- $Y = (\overline{A+B})$
- $Y = (A+B)'$

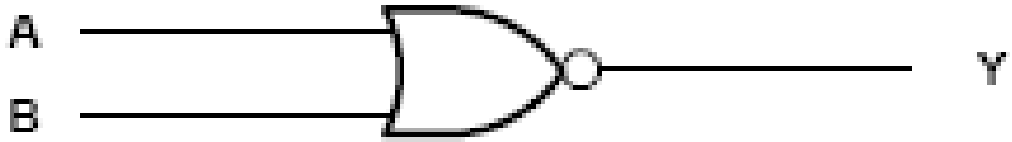


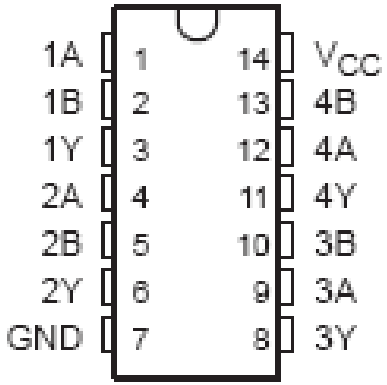
Simulação
NÃO OU ou NOR

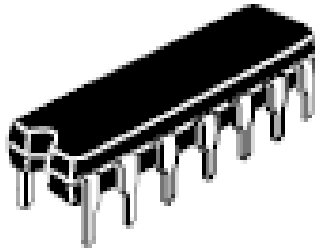


SN74AHC02
Texas Instruments

- Quadruple 2-Input Positive NOR Gates
  - *Capitulo 01 SI1\CIs Portas Logicas\sn74ahc02 - NOR.pdf*

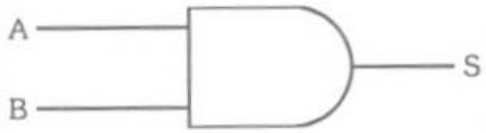






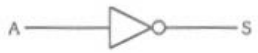
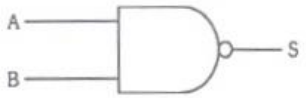
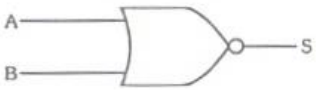
Quadro Resumo

BLOCOS LÓGICOS BÁSICOS

Porta	Símbolo Usual	Tabela da Verdade	Função Lógica	Expressão
E AND		A B S 0 0 0 0 1 0 1 0 0 1 1 1	**Função E:** assume 1 quando todas as variáveis forem 1 e 0 nos outros casos.	S = AB
OU OR		A B S 0 0 0 0 1 1 1 0 1 1 1 1	**Função OU:** assume 0 quando todas as variáveis forem 0 e 1 nos outros casos.	S = A + B

Quadro Resumo

BLOCOS LÓGICOS BÁSICOS

Porta	Símbolo Usual	Tabela da Verdade	Função Lógica	Expressão
NÃO NOT INVERSOR		A | S 0 | 1 1 | 0	**Função NÃO:** inverte a variável aplicada à sua entrada.	$S=\overline{A}$
NE NAND		A B | S 0 0 | 1 0 1 | 1 1 0 | 1 1 1 | 0	**Função NE:** inverso da função E.	$S=\overline{AB}$
NOU NOR		A B | S 0 0 | 1 0 1 | 0 1 0 | 0 1 1 | 0	**Função NOU:** inverso da função OU.	$S=\overline{A+B}$