Positive Sequence Tracking Phase Locked Loops: A Unified Graphical Explanation

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***Abstract*-- This paper presents a graphical analysis which explains several three-phase Phase-Locked Loop (PLL) algorithms based on the detection of the positive-sequence component of the power system. It is shown that, by employing vector algebra (dot, inner or scalar product) and space vectors concepts, several PLLs methods presented in literature may be represented by a unique theory.**

***Index Terms*-- Phased Locked Loop (PLL), three phase PLL, positive sequence tracking PLLs, Synchronization, Utility-Connected Systems.**

I. Introduction

Phase-Locked Loops (PLL) are methods to achieve synchronization of signals, usually employed in communication, control, automation and instrumentation systems. With the development of power electronic based devices connected to AC power systems, i.e. Dynamic Voltage Restorers [10], Converters connected to alternative energy systems [13], FACTS [10,13] or Active Filters [1], PLL algorithms have been widely used in power systems. In these applications, the PLL must assure frequency and phase angle synchronism with the positive sequence component, even with harmonic distortion and unbalance at the grid, since this is the component of interest for generation, transmission or power consumption. This paper compares and analyzes only positive sequence based three-phase PLL techniques.

Figure 1 shows the topology of a three-phase PLL applied to power systems, considering instantaneous voltages in *a,b,c* system [1],[2],[3]. Fig. 7 presents another consolidated strategy presented in literature in terms of $\alpha\beta$ components [4], known as p-PLL or q-PLL [6],[7],[8]. Fig. 8 shows the most common representation of positive sequence PLLs, which is based on *d,q* synchronous reference frame [9], [10], [11], [12], [13], [14], [15], [16].

This paper shows that the techniques of [1]-[16] are all the same and proposes an intuitive graphical explanation to these algorithms, based on Space Vectors. Moreover, comparison shows that main differences of these techniques are the coordinate system implementation and the topology of filtering functions. The stability analysis and locking conditions graphical explanations of the algorithms are also presented.

II. PLL Algorithm in *abc* frame

In this paper, the PLL is represented as a control system (Fig. 1), where the control objective in is to force the dot product y(t) between PLL instantaneous voltage vector $\vec{\mathbf{V}}_{PLL} = \vec{\mathbf{V}}_{PLL}(t) = [v_{PLLa}(t) \;\; v_{PLLb}(t) \;\; v_{PLLc}(t)]^T$ and the mains instantaneous voltage vector $\vec{\mathbf{V}} = \vec{\mathbf{V}}(t) = [v_a(t) \;\; v_b(t) \;\; v_c(t)]^T$ to be null, that is, to assure orthogonality between these vectors. The dot product error ε is the input of controller $G_C(s)$, usually a Proportional Integral (PI) type, whose output is in general added to the mains frequency ω_{MAINS} to minimize control effort. The output of the Controller Block $G_C(s)$ is the PLL angular frequency reference ω_{PLL}, i.e., the frequency to be synthesized by the three-phase Voltage Controlled

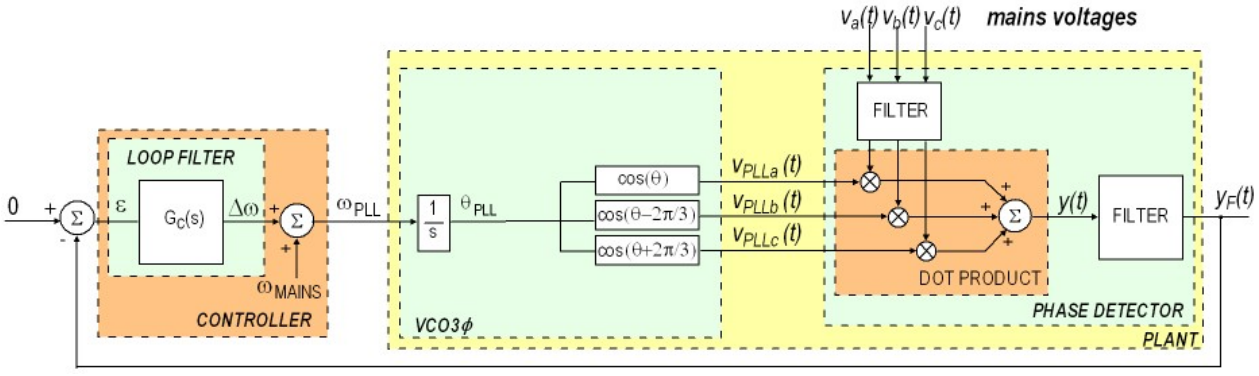

Fig.1 PLL representation in **abc** coordinate system.

Oscillator (VCO). The plant is composed by the VCO and by a dot product based phase detector. The phase detector may employ filtering actions on either the mains voltages [14],[15],[16], or on output of the Dot Product Block [1],[2],[6] to attenuate high order components (caused by harmonics and negative sequence).

A. Space vectors: Definitions and adopted notation

In Fig. 2, the instantaneous mains voltages $v_a(t)$, $v_b(t)$ and $v_c(t)$ and an orthonormal basis composed by the unitary vectors $\vec{\mathbf{a}}$, $\vec{\mathbf{b}}$ and $\vec{\mathbf{c}}$, define the mains voltage space vector [5]:

$$\vec{\mathbf{V}} = \vec{\mathbf{V}}(t) = v_a(t)\cdot\vec{\mathbf{a}} + v_b(t)\cdot\vec{\mathbf{b}} + v_c(t)\cdot\vec{\mathbf{c}} \quad (1)$$

The zero-sequence instantaneous voltage, from (3), is equal to:

$$v_0(t) = \left(v_a(t) + v_b(t) + v_c(t)\right)/\sqrt{3} \quad (2)$$

If $v_0(t) = 0$, $v_a(t) + v_b(t) + v_c(t) = 0$ defines the **αβ** plane of Fig. 2. In three-phase three-wire systems, the vector $\vec{\mathbf{V}}$ is in this plane. It is convenient to adopt the $\vec{\boldsymbol{\alpha}}, \vec{\boldsymbol{\beta}}, \vec{\mathbf{0}}$ basis, where the $\vec{\boldsymbol{\alpha}}, \vec{\boldsymbol{\beta}}$ vectors, which are perpendicular between each other, belong to the plane and $\vec{\mathbf{0}}$ is orthogonal to this plane. The $\vec{\boldsymbol{\alpha}}$ component is parallel to the projection of $\vec{\mathbf{a}}$ onto the $\vec{\boldsymbol{\alpha}}, \vec{\boldsymbol{\beta}}$ plane. The relationship between $\vec{\mathbf{V}}$ coordinates in **abc** and **αβ0** base is given by (3) [4].

$$\begin{bmatrix} v_0(t) \\ v_\alpha(t) \\ v_\beta(t) \end{bmatrix} = \sqrt{\frac{2}{3}} \cdot \begin{bmatrix} 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \\ 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \cdot \begin{bmatrix} v_a(t) \\ v_b(t) \\ v_c(t) \end{bmatrix} \quad (3)$$

$$\vec{V}_{0\alpha\beta} = \mathbf{M}\vec{V}_{abc}$$

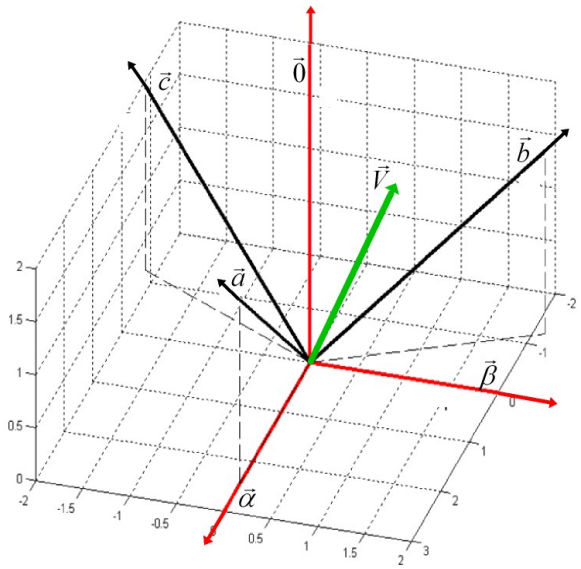

Fig. 2. Coordinate systems **abc** and **αβ0 and vector** $\vec{V}$ **.**

Equation (3) is an orthogonality transformation, i.e. $\mathbf{M}^{-1} = \mathbf{M}^T$, in which the amplitude and the relative position between the space vectors $\overrightarrow{\mathbf{V}_{abc}}$ and $\overrightarrow{\mathbf{V}_{\alpha\beta 0}}$ are unaltered when this transformation is applied. In this paper, the coordinate systems transformations from **abc** to **αβ0** are applied in order to present the algorithm in a more didactic way. However, it shall be noted that the implementation of the PLL may be done in any coordinate system (**abc** , **αβ0** or **dq0**).

In this way, a set of positive sequence *h*-order harmonic voltages, $v_{ha}^{+}(t), v_{hb}^{+}(t), v_{hc}^{+}(t)$, with a peak value of V_h^+, generates the vector $\overrightarrow{\mathbf{V}_h^+}$:

$$\overrightarrow{\mathbf{V}_h^+} = \overrightarrow{\mathbf{V}_h^+}(t) = \left[v_{ha}^{+}(t)\ v_{hb}^{+}(t)\, v_{hc}^{+}(t)\right]^T \quad (4)$$

The projection of the vector $\overrightarrow{\mathbf{V}_h^+}$ on the $(\boldsymbol{\alpha}, \boldsymbol{\beta})$ plane has the same amplitude V_h^+, and rotates with $h\omega$ angular frequency (speed) in the counterclockwise direction (Fig. 3a).

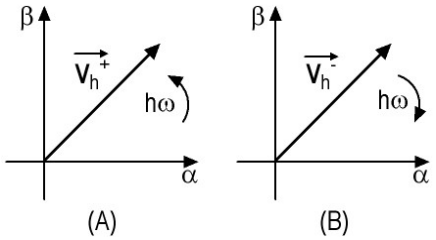

Fig. 3. Mains voltage harmonics space vector projection on αβ-plane. (a) Positive sequence harmonics. (b) Negative sequence harmonics.

A set of negative sequence *h*-order harmonic voltages defined as $v_{ha}^{-}(t), v_{hb}^{-}(t), v_{hc}^{-}(t)$ generates the vector $\overrightarrow{\mathbf{V}_h^-}$, with a peak value of V_h^-:

$$\overrightarrow{\mathbf{V}_h^-} = \overrightarrow{\mathbf{V}_h^-}(t) = \left[v_{ha}^{-}(t)\ v_{hb}^{-}(t)\, v_{hc}^{-}(t)\right]^T \quad (5)$$

The projection of the vector $\overrightarrow{\mathbf{V}_h^-}(t)$ on the $\boldsymbol{\alpha}, \boldsymbol{\beta}$ plane, has the same amplitude V_h^- and rotates with $h\omega$ angular frequency (speed) in the clockwise direction (Fig. 3b).

A set of zero sequence *h*-order harmonic voltages is defined as $v_{ha}^{0}(t), v_{hb}^{0}(t), v_{hc}^{0}(t)$ and generates the vector $\overrightarrow{\mathbf{V}_h^o}$:

$$\overrightarrow{\mathbf{V}_h^o} = \overrightarrow{\mathbf{V}_h^o}(t) = \left[v_{ha}^{o}(t)\ v_{hb}^{o}(t)\, v_{hc}^{o}(t)\right]^T \quad (6)$$

The vector $\overrightarrow{\mathbf{V}_h^o}$ with variable amplitude, is always perpendicular to the $\boldsymbol{\alpha}, \boldsymbol{\beta}$ plane and thus parallel to $\vec{\mathbf{0}}$ axis.

B. Dot Product Analysis

In Fig. 1, VCO block generates a set of three, positive sequence, sinusoidal voltages $v_{PLLa}(t), v_{PLLb}(t), v_{PLLc}(t)$ at the angular frequency ω_{PLL}, associated with the positive sequence vector $\vec{\mathbf{V}}_{\mathbf{PLL}}$:

$$\vec{\mathbf{V}}_{PLL} = \vec{\mathbf{V}}_{PLL}(t) = \left[v_{PLLa}(t) \quad v_{PLLb}(t) \quad v_{PLLc}(t)\right]^T \tag{7}$$

The superscript '+' was dropped in all signals and vectors related to the PLL, because they are always positive sequence ones. $\vec{\mathbf{V}}_{\mathbf{PLL}}$ will always be in the $\alpha\beta$ plane.

The dot product between $\vec{\mathbf{V}}_{\mathbf{PLL}}$ vector and the mains voltage vector $\vec{\mathbf{V}}$ (Fig. 4) is given by:

$$\overrightarrow{\mathbf{V}_{\mathbf{PLL}}}\cdot\vec{\mathbf{V}} = \overrightarrow{\mathbf{V}_{\mathbf{PLL}}}\cdot\left(\overrightarrow{\mathbf{V}_{\mathbf{1}}^{+}} + \overrightarrow{\mathbf{V}_{\mathbf{1}}^{-}} + \overrightarrow{\mathbf{V}_{\mathbf{1}}^{\mathbf{0}}} + \sum_{2}^{N}\overrightarrow{\mathbf{V}_{\mathbf{h}}^{+}} + \sum_{2}^{N}\overrightarrow{\mathbf{V}_{\mathbf{h}}^{-}} + \sum_{2}^{N}\overrightarrow{\mathbf{V}_{\mathbf{h}}^{\mathbf{0}}}\right) \tag{8}$$

Equation (8) is expanded as:

$$\overrightarrow{\mathbf{V}_{\mathbf{PLL}}}\cdot\vec{\mathbf{V}} = \underbrace{\overrightarrow{\mathbf{V}_{\mathbf{PLL}}}\cdot\overrightarrow{\mathbf{V}_{\mathbf{1}}^{+}}}_{I} + \underbrace{\overrightarrow{\mathbf{V}_{\mathbf{PLL}}}\cdot\overrightarrow{\mathbf{V}_{\mathbf{1}}^{-}}}_{II} + \underbrace{\overrightarrow{\mathbf{V}_{\mathbf{PLL}}}\cdot\overrightarrow{\mathbf{V}_{\mathbf{1}}^{\mathbf{0}}}}_{III} + \underbrace{\sum_{2}^{N}\overrightarrow{\mathbf{V}_{\mathbf{PLL}}}\cdot\overrightarrow{\mathbf{V}_{\mathbf{h}}^{+}}}_{IV} + \underbrace{\sum_{2}^{N}\overrightarrow{\mathbf{V}_{\mathbf{PLL}}}\cdot\overrightarrow{\mathbf{V}_{\mathbf{h}}^{-}}}_{V} + \underbrace{\sum_{2}^{N}\overrightarrow{\mathbf{V}_{\mathbf{PLL}}}\cdot\overrightarrow{\mathbf{V}_{\mathbf{h}}^{\mathbf{0}}}}_{VI} \tag{9}$$

In (9), the instantaneous values of terms III and VI, which include mains voltage zero sequence components, are null, since the $\overrightarrow{\mathbf{V}_{\mathbf{h}}^{\mathbf{0}}}$ (h=1…n) vectors are parallel to the $\vec{\mathbf{0}}$ axis and consequently are perpendicular to the $\boldsymbol{\alpha},\boldsymbol{\beta}$ plane and to $\vec{\mathbf{V}}_{\mathbf{PLL}}$ vector. Consequently, this PLL is not affected by zero sequence components in the mains voltages.

The term I of (9) corresponds to the dot product of synchronous vectors with phase displacement $\delta = \phi_1^+ - \theta_{PLL}$ (see Fig. 4):

$$\vec{\mathbf{V}}_{\mathbf{PLL}}\cdot\overrightarrow{\mathbf{V}_{\mathbf{1}}^{+}} = \left|\vec{\mathbf{V}}_{\mathbf{PLL}}\right|\cdot\left|\overrightarrow{\mathbf{V}_{\mathbf{1}}^{+}}\right|\cdot\cos(\delta) \tag{10}$$

The terms II, IV and V of (9) correspond to the dot product between vectors with non-zero relative angular frequency, resulting in a non-zero instantaneous voltage with null mean value. In particular, the relative angular frequency between vectors of term II is equal to 2ω, which is the lowest frequency that the filters in the plant of Fig. 1 must attenuate. The 2ω component will be feed-forwarded through $G_C(s)$, and appear in the ω_{PLL} signal, producing a frequency modulation in the VCO input. This results in distorted signals at the VCO output.

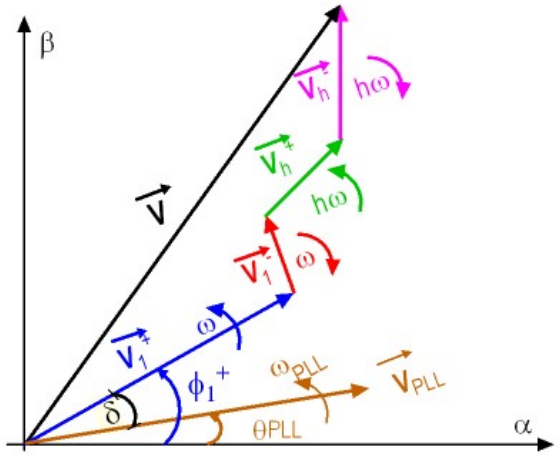

Fig. 4. Dot product between $\vec{\mathbf{V}}_{\mathbf{PLL}}$ and $\vec{\mathbf{V}}$ space vectors.

The filters of Fig. 1 may be implemented by means of a PI Controller [1],[2],[6], Double Synchronous Reference Frame [15], Sinusoidal Signal Integrator [14] or by the extraction of positive and negative sequence methods [16]. Some authors consider that the loop filter implementation is done by the PI Controller and the inherent filtering action of the plant, since the VCO is modeled as an integrator [9], [10], [11].

The dynamic response of the PLL is strictly related to its application and to the design of the controller and of the filter(s) of Fig. 1. For instance, in a Dynamic Voltage Restorer [10], in the occurrence of voltage sags and swells the PLL should not quickly track the mains voltage, since with such behavior the PLL output may exhibit phase jumps. Thus, the PLL closed loop system should be designed to have slow dynamic response in this application.

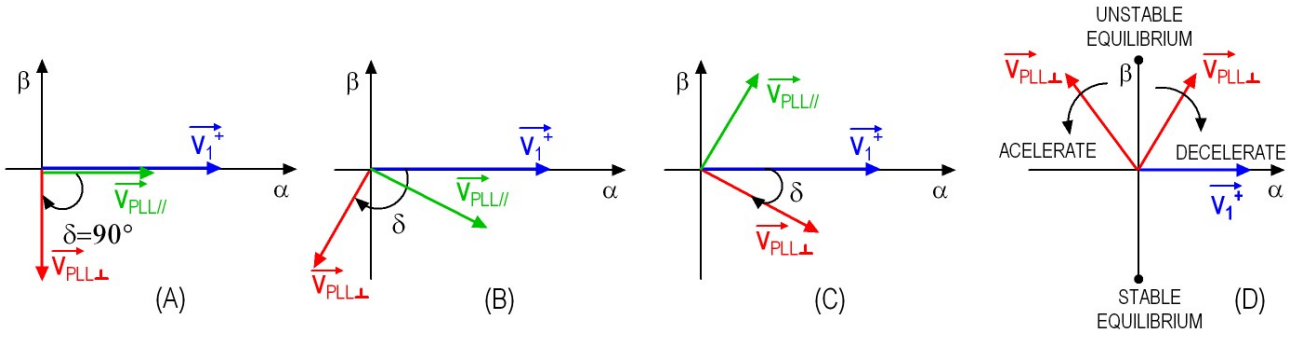

Fig.5. Locking Conditions in **αβ0** (a) Locked (b) Lag (c) Lead (d) Stability points.

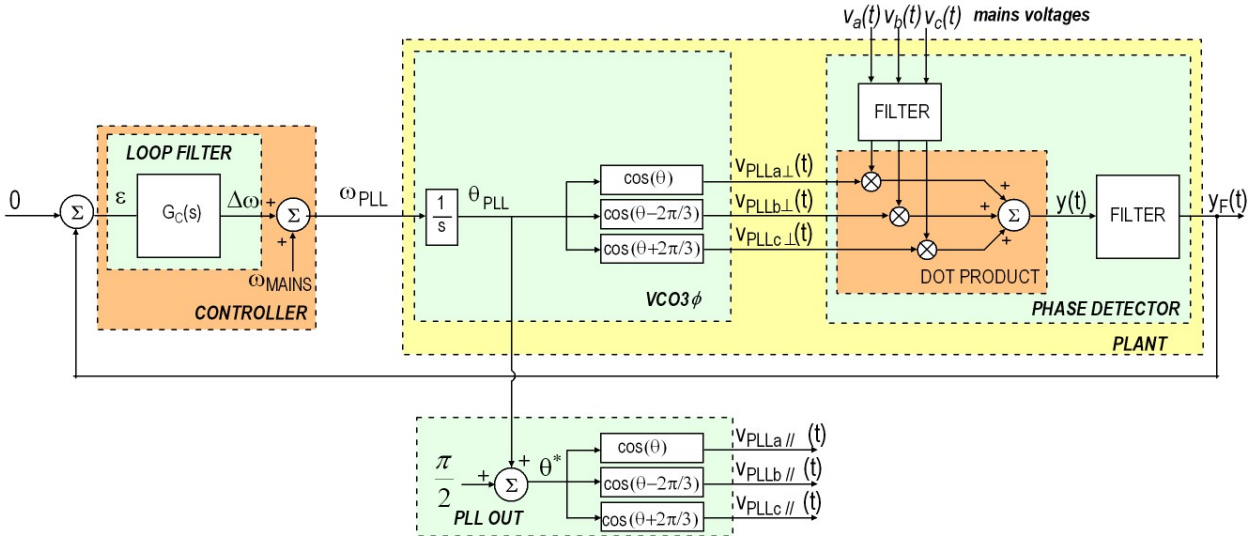

Fig. 6. Generating a PLL output vector $\overrightarrow{\mathbf{V}_{\mathbf{PLL//}}}$ parallel to $\overrightarrow{\mathbf{V}_1^+}$.

C. Locking Conditions

As stated before, the controller of Fig. 1 must force the filtered dot product $\overrightarrow{\mathbf{V}_{\mathbf{PLL}}} \cdot \vec{\mathbf{V}}$ to zero, resulting in $\overrightarrow{\mathbf{V}_{\mathbf{PLL}}} = \overrightarrow{\mathbf{V}_{\mathbf{PLL}\perp}}$, shown in figure 5a. $\overrightarrow{\mathbf{V}_{\mathbf{PLL}\perp}}$ vector lags $\overrightarrow{\mathbf{V}_1^+}$ by 90° (see Fig. 5a).

However, since the majority of PLL applications employs a PLL vector synchronized and in phase with the mains positive sequence voltage, the vector $\overrightarrow{\mathbf{V}_{\mathbf{PLL//}}}$ must be obtained leading $\overrightarrow{\mathbf{V}_{\mathbf{PLL}\perp}}$ by 90° (Fig. 5a). Fig. 6 introduces the 'PLL OUT' block to generate $\overrightarrow{\mathbf{V}_{\mathbf{PLL//}}}$.

If $\overrightarrow{\mathbf{V}_1^+}$ leads $\overrightarrow{\mathbf{V}_{\mathbf{PLL//}}}$ (Fig. 5b), $\delta > 90°$ and the mean value of the dot product $\overrightarrow{\mathbf{V}_{\mathbf{PLL}\perp}} \cdot \vec{\mathbf{V}}$ is negative. Consequently, the error $\boldsymbol{\varepsilon}(\mathbf{t})$ in Fig. 1 is positive, resulting in an increment of the VCO frequency, accelerating $\overrightarrow{\mathbf{V}_{\mathbf{PLL}\perp}^+}$. If $\overrightarrow{\mathbf{V}_1^+}$ lags $\overrightarrow{\mathbf{V}_{\mathbf{PLL//}}}$ (Fig. 5c), the same analysis is valid and $\overrightarrow{\mathbf{V}_{\mathbf{PLL}\perp}^+}$ will decelerate. Thus, it can be noted that $\delta = 90°$ is a point of stable equilibrium and $\delta = 270°$ or $\delta = -90°$ is an unstable equilibrium point (Fig. 5d).

III. PLL Algorithm in αβ0 Frame

The PLL in **αβ0** frame is directly obtained from the **abc** frame PLL presented in Fig. 1. Fig. 7 shows the control topology of the PLL in the **αβ0** coordinate system. The coordinate transformation (3) is applied to the **abc** mains voltages, resulting in the **αβ0 coordinates** $v_\alpha(t), v_\beta(t), v_0(t)$, of the mains vector $\overrightarrow{\mathbf{V}_{\alpha\beta 0}}$ (11):

$$\begin{aligned}\overrightarrow{\mathbf{V}_{\alpha\beta 0}}(t) &= v_\alpha(t)\vec{\boldsymbol{\alpha}} + v_\beta(t)\vec{\boldsymbol{\beta}} + v_0(t)\vec{\mathbf{0}} \\ &= \left[v_\alpha(t)\ v_\beta(t)\, v_0(t)\right]^T\end{aligned} \tag{11}$$

Applying the above procedure to the VCO

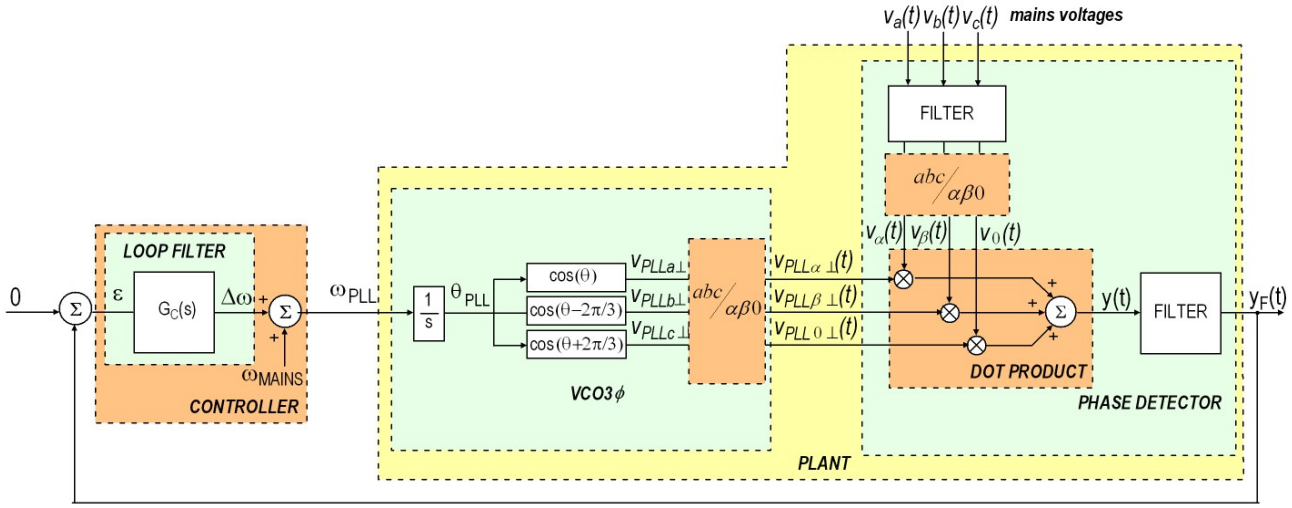

Fig..7. PLL representation in **αβ0** coordinate system.

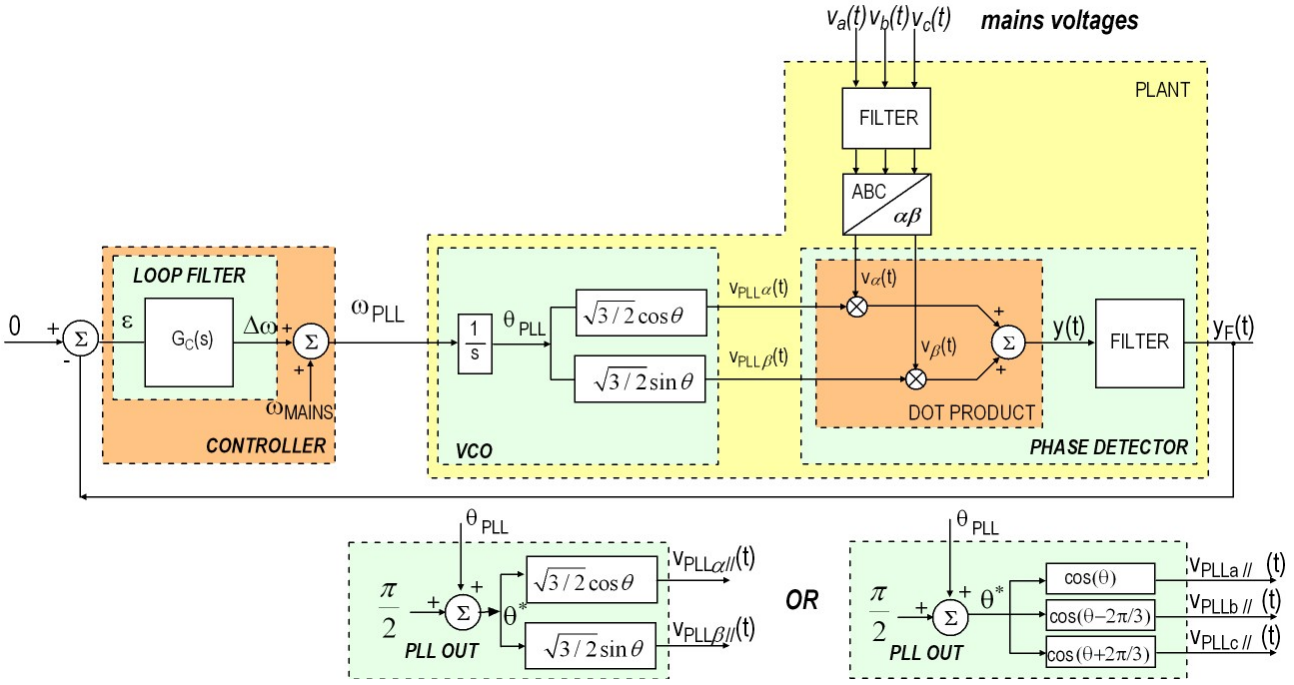

Fig.8. PLL representation in **αβ** coordinate system including two possible 'PLL OUT' blocks.

outputs $v_{PLLa}(t), v_{PLLb}(t), v_{PLLc}(t)$, results in the **αβ0 coordinates** $v_{PLL\alpha}(t), v_{PLL\beta}(t), v_{PLL0}(t)$ of the PLL vector $\overrightarrow{\mathbf{V}_{PLL\alpha\beta0}}$ (12):

$$\begin{aligned}\overrightarrow{\mathbf{V}_{PLL\alpha\beta0}}(t) &= v_{PLL\alpha}(t)\vec{\boldsymbol{\alpha}} + v_{PLL\beta}(t)\vec{\boldsymbol{\beta}} + v_{PLL0}(t)\vec{\mathbf{0}} \\ &= \left[v_{PLL\alpha}(t)\ v_{PLL\beta}(t) v_{PLL0}(t)\right]^T\end{aligned} \qquad (12)$$

Item IIA has shown that the **abc/αβ0** coordinate transformation (3) preserves amplitudes and relative position (i.e., angles) between space vectors, resulting in $\overrightarrow{\mathbf{V}_{PLL\ \alpha\beta0}} = \overrightarrow{\mathbf{V}_{PLL\ abc}} = \overrightarrow{\mathbf{V}_{PLL}}$, and $\overrightarrow{\mathbf{V}_{\alpha\beta0}} = \overrightarrow{\mathbf{V}_{abc}} = \overrightarrow{\mathbf{V}}$. The dot product $\overrightarrow{\mathbf{V}_{PLL\ \alpha\beta0}} . \overrightarrow{\mathbf{V}_{\alpha\beta0}}$ has exactly the same value of the dot product calculated in **abc** frame in Fig. 1, because of the orthogonality property of T matrix. Thus, the PLL in Fig. 7 has the same behavior of the one in Fig. 1.

Since, as proved by the Dot Product analysis of item IIB, the VCO has no zero sequence components, this PLL is not affect by zero sequence components of the mains voltages, and the PLL in Fig. 7 can be redrawn as shown in Fig. 8. The VCO directly generates the **αβ** components and the amplitude must be corrected by a factor $\sqrt{3/2}$ to respect (3) (the amplitude of $\overrightarrow{\mathbf{V}_{\mathbf{PLL}}}$ must be $\sqrt{3/2}$). Fig. 8 also includes the 'PLL OUT' block, which allows generation of an output vector $\overrightarrow{\mathbf{V}_{\mathbf{PLL}}}$ parallel to $\overrightarrow{\mathbf{V}_1^+}$ in **abc** or in **αβ** coordinates systems.

This PLL is often called p-PLL by some authors, because of the dot product similarity with the instantaneous active power *p(t)* [6],[7][8]. Reference [8] calculates *p(t)* using the **abc** coordinates system.

The signals $v_{PLL\alpha}(t), v_{PLL\beta}(t)$ are called as fictitious currents and the *y(t)* signal (Fig. 8) becomes a fictitious active power $p(t)$. The control objective is to achieve $p(t) = 0$, that is, to assure orthogonality between mains and PLL voltages vectors (null dot product). Thus, the explanation developed in Topics II and III is also valid for this technique.

Reference [7] discusses the possibility of using the fictitious reactive instantaneous power signal. In this case the PLL vector will be parallel to the mains vector. These vectors will have the same or opposite signals depending on the positive or negative feedback signal of Fig. 8, respectively.

The fictitious reactive power can be easily calculated by:

$$q(t) = v_\beta(t) v_{PLL\alpha}(t) - v_\alpha(t) v_{PLL\beta}(t) \qquad (13)$$

In (13), $q > 0$ for $\overrightarrow{\mathbf{V}_{PLL}}$ lagging $\overrightarrow{\mathbf{V}}$.

IV. PLL ALGORITHM IN **DQ0** FRAME

This method is extensively cited in the literature [9], [11], [12], [13], [14], [15], [16], and is known as Synchronous Reference Frame – SRF-PLL. Fig. 9 shows the control topology of the PLL in the **dq0** coordinate system. Two coordinate transformations are made: **abc** to **αβ0** (3) and then **αβ0** to the synchronous reference frame **dq0** (Park transform). The zero sequence components are

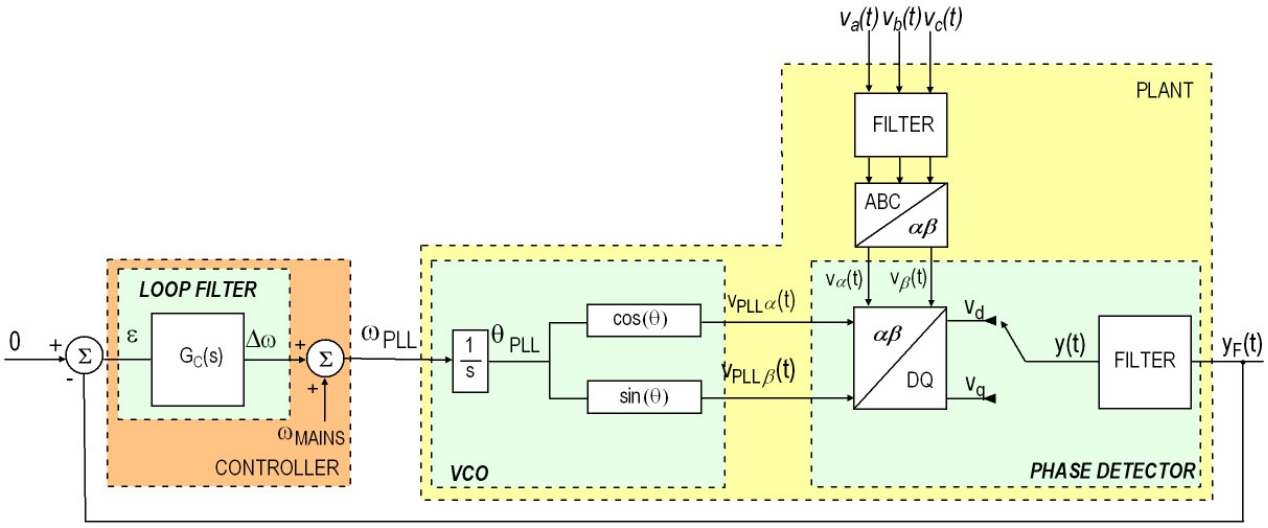

Fig.9 PLL representation in **dq** coordinate system.

not considered in the PLL implementation, according to previous discussions in items IIB and III. The **αβ/ dq** conversion of the mains voltages is carried out using the VCO signals. This results in $\overrightarrow{\mathbf{V}_{\mathbf{PLL}}}$ always parallel to the $\vec{\mathbf{d}}$ axis, as shown in figure 10. The **dq** rotates in the couterclockwise direction around $\vec{0}$ axis.

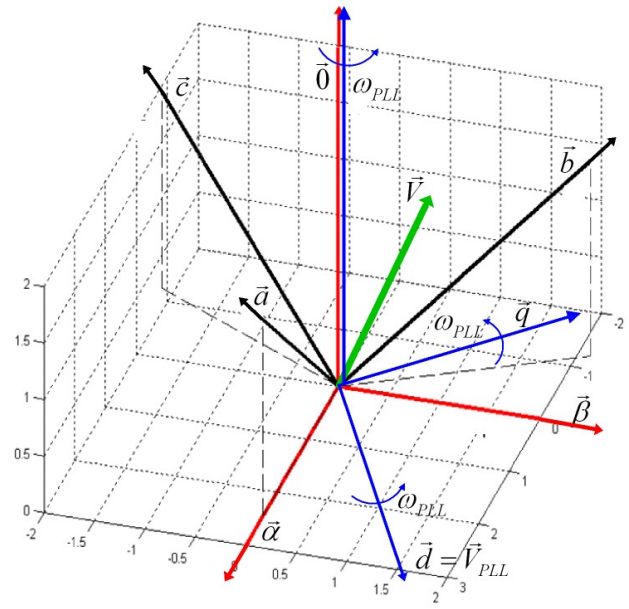

Fig. 10 relationship between **abc**, $\alpha\beta 0$ and **dq0** coordinate systems.

Figure 11a shows the mains voltage positive sequence vector $\vec{\mathbf{V}}_1^+$ projections v_d and v_q into $\vec{\mathbf{d}}$ and $\vec{\mathbf{q}}$ axes, respectively. Forcing $y(t) = v_d = 0$ (Fig. 9) is equivalent to force the dot product $v_d = \vec{\mathbf{V}}_1^+ \cdot \vec{\mathbf{d}}$ to zero, which is assured only if $\vec{\mathbf{V}}_1^+$ is perpendicular to $\vec{\mathbf{d}}$. This condition is shown in Fig. 11b and is achieved by rotating the **dq** reference frame with angular speed ω_{PLL}, until $\vec{\mathbf{V}}_1^+$ becomes orthogonal to $\vec{\mathbf{d}}$, which, according to the explanation of Topic II, is equivalent to set $\overrightarrow{\mathbf{V}_{\mathbf{PLL}//}} = \vec{\mathbf{d}}$ (and $\overrightarrow{\mathbf{V}_{\mathbf{PLL}\perp}} = -\vec{\mathbf{q}}$).

As a consequence, the same previous graphical explanation is valid to Synchronous Reference Frame PLLs.

Some variations of this strategy include forcing $\mathbf{v_q = 0}$ [14] (Fig. 11c) or the use of positive feedback of $y_F(t)$ in the control loop [15][10](Fig. 11d). This last case is very convenient because the mains positive sequence vector $\vec{\mathbf{V}}_1^+$ will be parallel to the axis $\vec{\mathbf{d}}$.

The problems related to the operation with the presence of harmonics and negative sequence components, discussed in item IIB, are minimized by implementing filters.

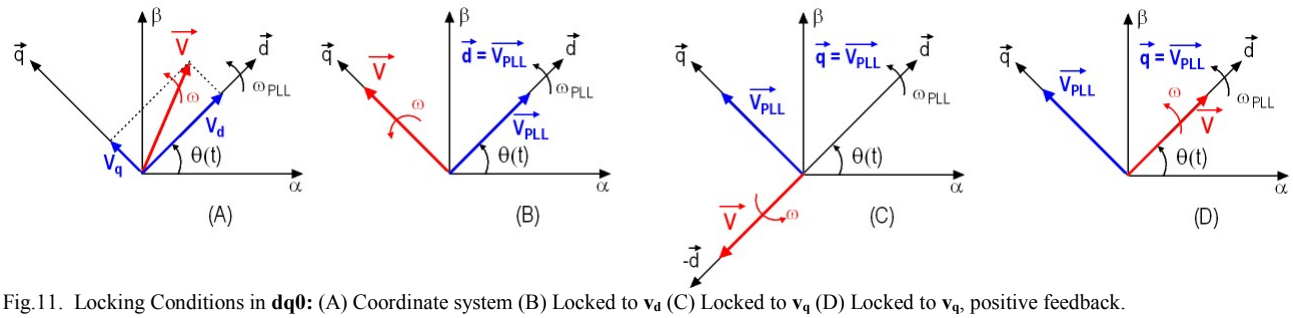

Fig.11. Locking Conditions in **dq0:** (A) Coordinate system (B) Locked to $\mathbf{v_d}$ (C) Locked to $\mathbf{v_q}$ (D) Locked to $\mathbf{v_q}$, positive feedback.

V. PLANT MODEL

Considering the plant and the control system approach of Fig. 1, a model of the plant (VCO + phase detector) will be necessary when designing the controller. A simple method to obtain this unified model is then developed.

The locally averaged value of $y(t)$ in Fig. 1 is:

$$y(t) = \left|\overrightarrow{\mathbf{V}_{PLL}}(t)\right| \cdot \left|\overrightarrow{\mathbf{V}_{1}^{+}}(t)\right| \cdot cos(\delta) \tag{14}$$

- Assuming that: the amplitudes of the VCO signals in Fig. 1 are unitary. This means that the amplitude of the vector $\overrightarrow{\mathbf{V}_{PLL}}$ is $\sqrt{3/2}$;
- the peak amplitude of the mains voltages positive sequence is $\mathbf{V}_1^+(t)$. This results in a mains voltage, positive sequence vector, with amplitude $\sqrt{3/2}\,\mathbf{V}_1^+(t)$.

If (14) is linearized around the operating point $\delta = +\pi/2$, $y(t)$ is rewritten as:

$$y(t) \cong \frac{3}{2}\mathbf{V}_1^+(t) \cdot \left(\frac{\pi}{2} - \delta\right) \tag{15}$$

From Fig. 4, $\delta = \phi_1^+ - \theta_{PLL}$, can be expanded to:

$$\delta = \left[\phi_1^+(t_0) - \theta_{PLL}(t_0)\right] + \int \left[\omega(t) - \omega_p(t)\right] \cdot dt \tag{16}$$

where $\phi_1^+(t_0)$, $\phi_{PLL}(t_0)$ are the initial values of the phase angles of the positive sequence of main voltages and of the PLL signals, respectively. From (15) and (16):

$$y(t) = \frac{3}{2}\mathbf{V}_1^+(t) \cdot \left\{ \underbrace{\left[\frac{\pi}{2} + \theta_{PLL}(t_0) - \varphi_1^+(t_0)\right]}_{I} + \underbrace{\int \left[\omega_{PLL}(t) - \omega(t)\right] \cdot dt}_{II} \right\} \tag{17}$$

If the *offset* described by term I of (17) is neglected, the plant can be represented by an integrator and a gain $\frac{3}{2}\mathbf{V}_1^+(t)$, as shown in Fig. 12. Voltage sags, swells and unbalances will affect the gain of the PLL plant, unless a normalization by the a gain and by the positive sequence amplitude is done.

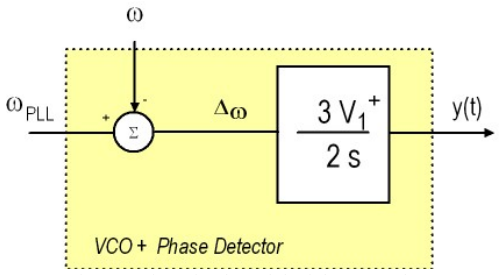

Fig. 12. Linearized model of the PLL plant.

For the $\alpha\beta$ PLL (or p-PLL), the model is exactly the same, if the VCO signals are multiplied by $\sqrt{3/2}$ as discussed in item III and shown in figure 8.

It is important to note that almost all referenced authors in this paper use the factor 2/3 instead of $\sqrt{2/3}$ in (3). This and other small variations found in the references only affect the plant gain, which can be easily calculated by the reasoning presented above.

For the **dq** PLL presented in figure 9, using the **αβ/ dq** conversion presented in figure 10, the $\vec{d}$ axis is equal to the PLL vector $\overrightarrow{\mathbf{V}_{PLL}}$, and has unitary amplitude. Unless the PLL voltages are corrected by a factor $\sqrt{3/2}$, the gain for the plant presented in figure 9 is $\sqrt{3/2}$ (instead of 3/2 as shown in figure 12.

VI. CONCLUSION

This paper has presented a graphical method which explains several three-phase PLL algorithms applied to power systems, aiming to unify these techniques. It has been shown that main differences rely on adopted coordinate system, choice of the feedback variable and on filtering techniques. It was also presented PLL filtering strategies and a unified plant model for the PLL circuits from [1] to [16]. Their plants linearized model only differs by a gain, which depends on the employed coordinate transformation formula, and on implementation details.

VII. REFERENCES

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