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VIENNA Rectifier & Beyond…

Johann W. Kolar et al.

Swiss Federal Institute of Technology (ETH) Zurich
Power Electronic Systems Laboratory
www.pes.ee.ethz.ch

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J. W. Kolar, L. Schrittwieser, F. Krismer, M. Antivachis, and D. Bortis

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Outline

- *History*
- *Vienna Rectifier*
- *Comparative Evaluation*
- *... and Beyond*
- *Future*

Source: Li-Core

Acknowledgement

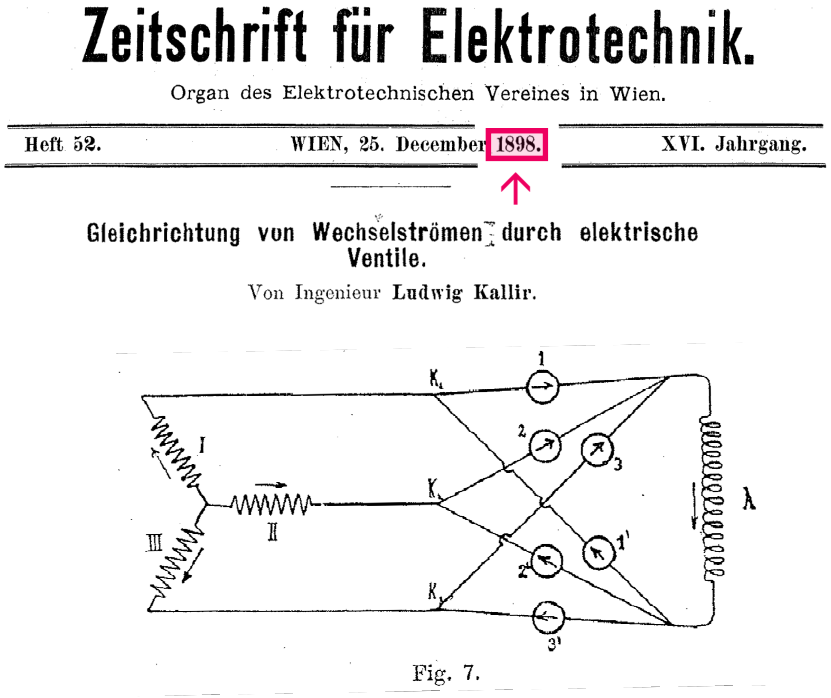
H. Ertl
T. Friedli
M. Hartmann
G. Laimer
M. Leibl
J. Miniböck

History

Passive 3-Φ Rectifier
Vienna Rectifier
APEC 1998

History of 3-Φ Rectifiers

- *L. Kallir @ Techn. Hochschule Wien (25. Dec. 1898)*
- Extension of 1-Φ Graetz/Pollak Rectifier



Zeitschrift für Elektrotechnik.

Organ des Elektrotechnischen Vereines in Wien.

Heft 52. WIEN, 25. December 1898. XVI. Jahrgang.

Gleichrichtung von Wechselströmen durch elektrische Ventile.

Von Ingenieur Ludwig Kallir.

Fig. 7.

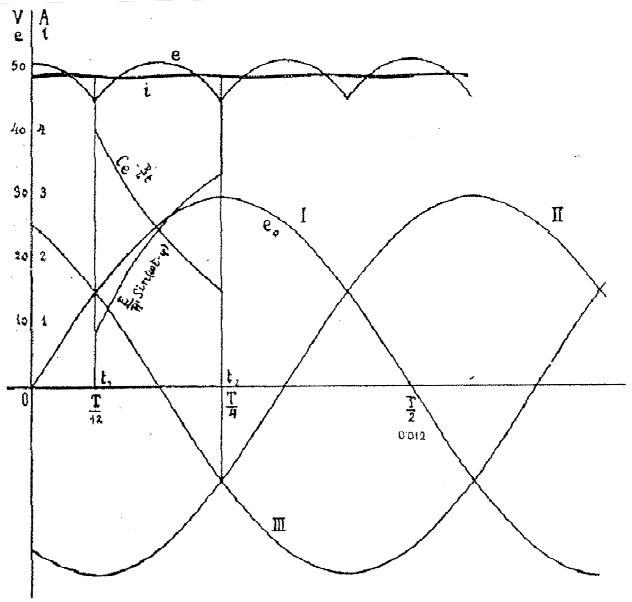


Fig. 8.

- Electrolytic Cells, Sparc Gaps, Discharge Tubes as „Valves“

Vienna Rectifier

- *Patent filed Dec. 23, 1993*
- Name Acknowledging

TECHNISCHE UNIVERSITÄT WIEN
Vienna University of Technology

Europäisches Patentamt
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(72) Erfinder: **Kolar, Johann W.**
Straussengasse 2-10/2/68
A-1050 Wien (AT)

EP 0 660 498 A2

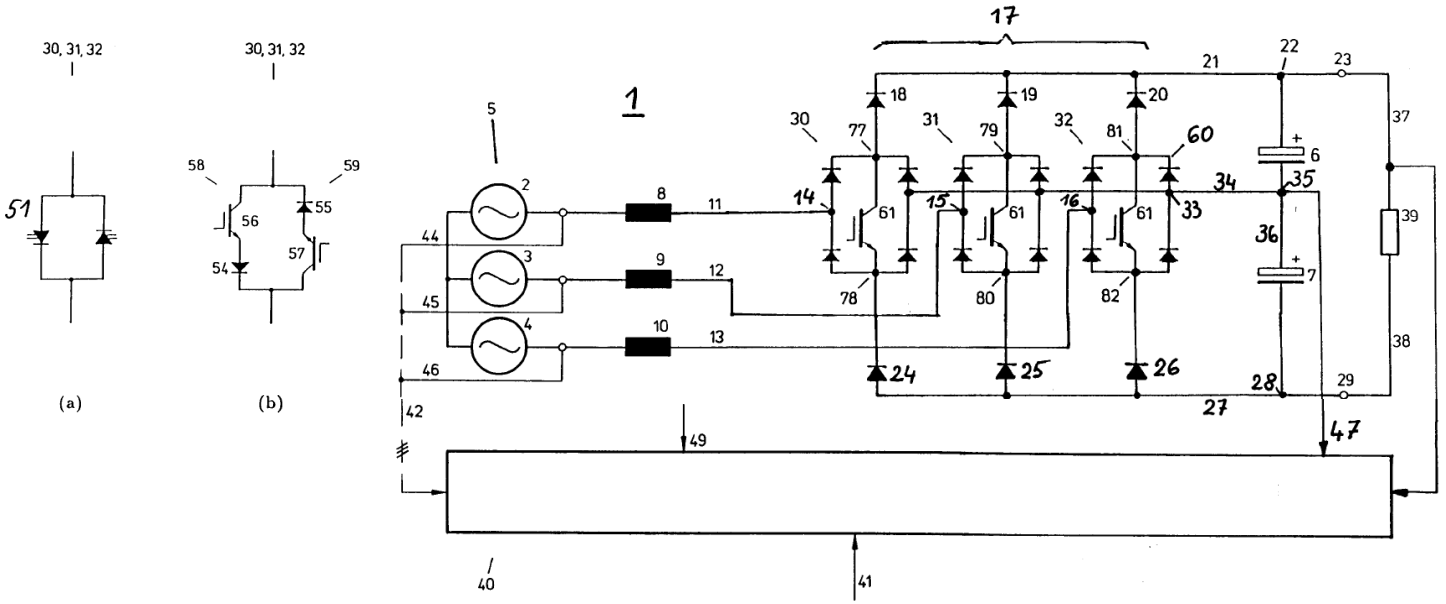
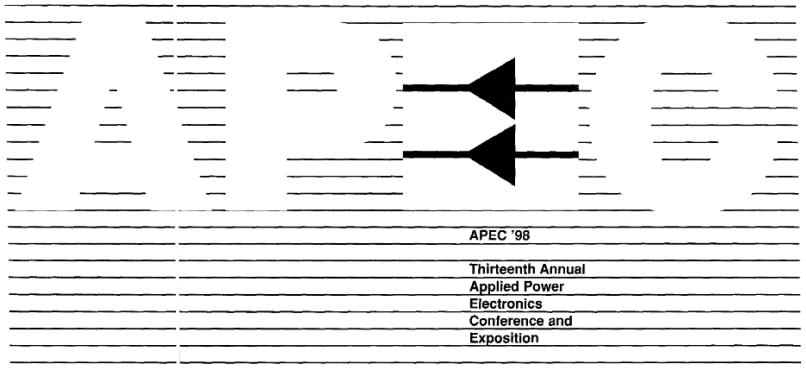
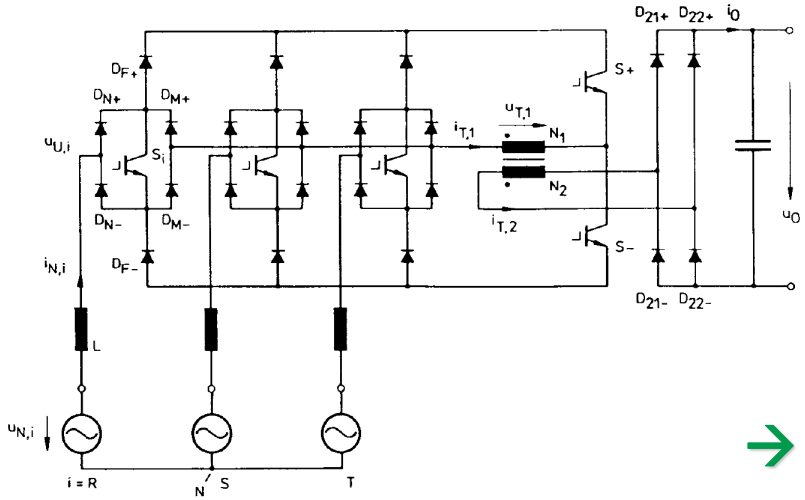


Fig. 1

- First Demonstrator for *High-Power Telecom Rectifier*

APEC ... 20 years ago





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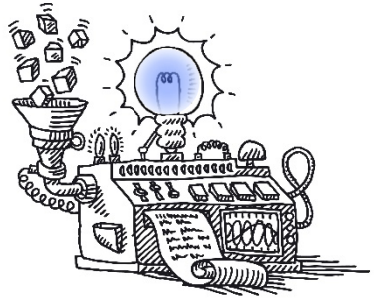
► Plenary Presentation @ APEC 1998

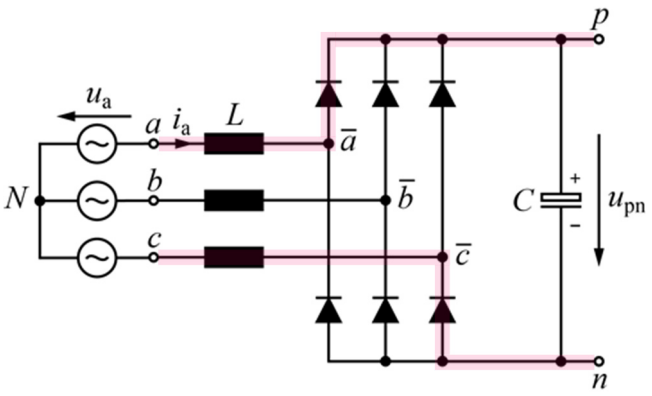
Vienna Rectifier

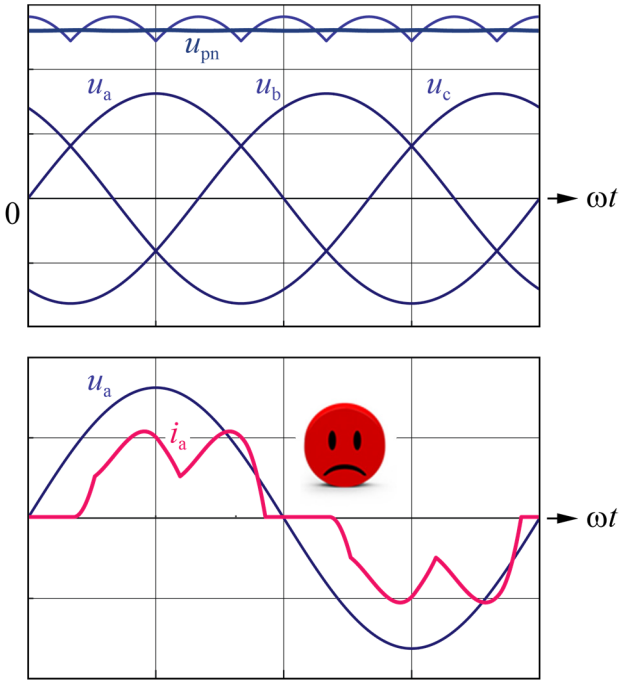
Topology Derivation
Basic Function
Hardware Demonstrator



3-Φ Diode Bridge Rectifier

- Conduction States Defined by *Line-to-Line* Mains Voltages
- Intervals with *Zero Current* / LF Harmonics
- No Output Voltage Control

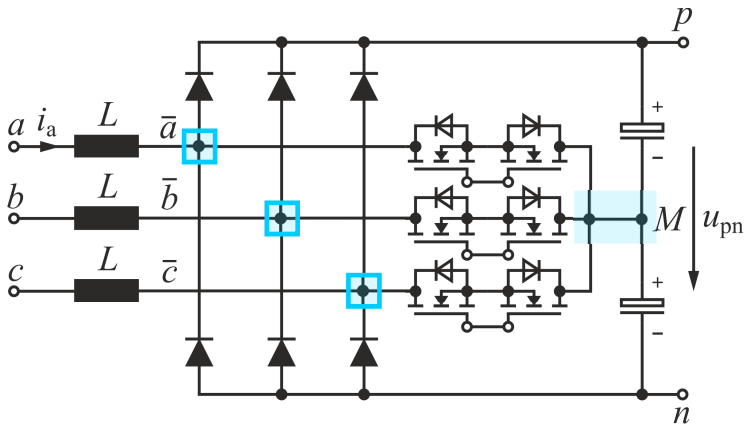


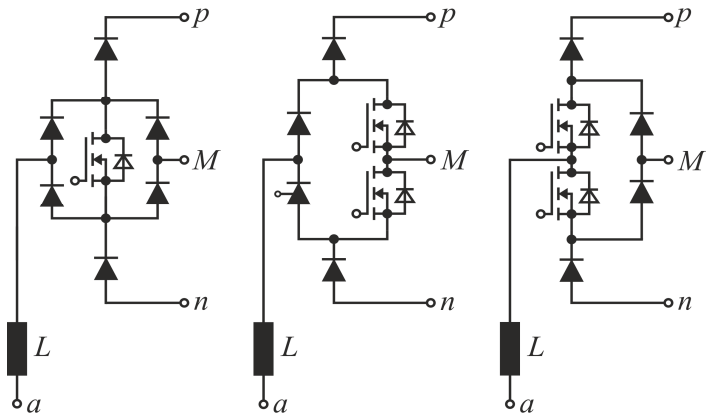


- Modulation of Diode Bridge Input Voltages

Vienna Rectifier (1)

- *Active Control of Diode Bridge Conduction State / Input Voltages*
- Bridge Leg Topologies with Different Voltage Stresses / Cond. Losses
- Phase & Bridge Symmetry !

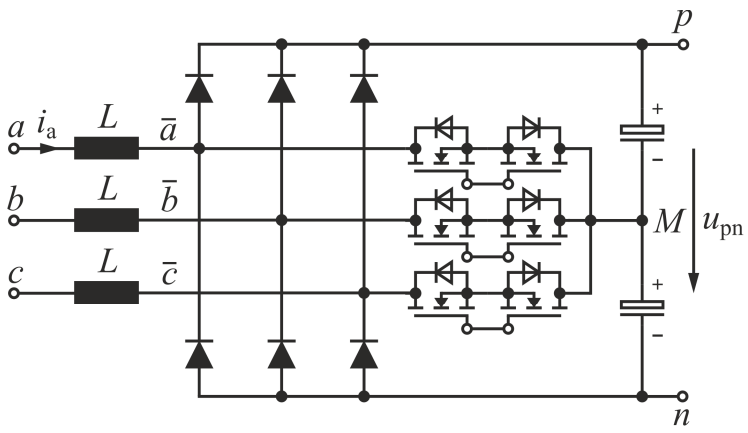


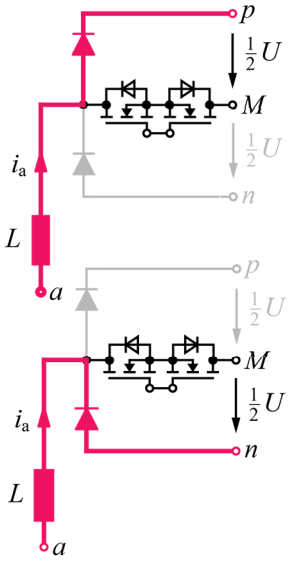


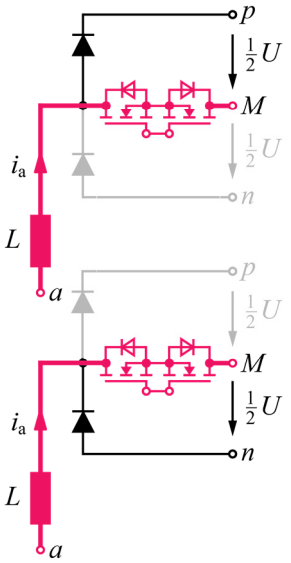
► Analysis of Input Voltage Formation

Vienna Rectifier (2)

- *Diode Bridge Input Voltage Formation Dependent on Current Direction*
- Min. Output Voltage Defined by Mains *Line-to-Line* Voltage Amplitude
- Boost-Type



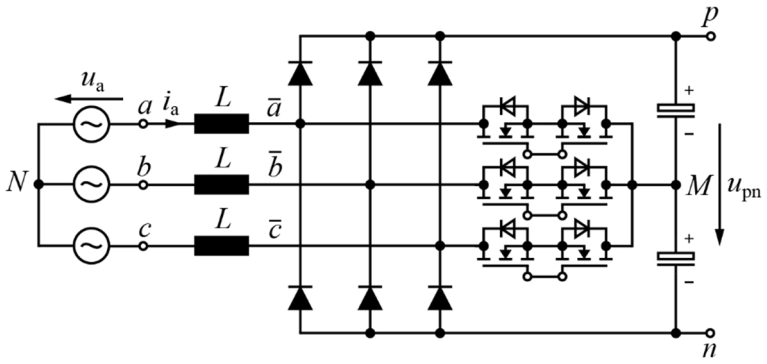


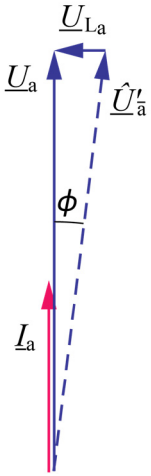


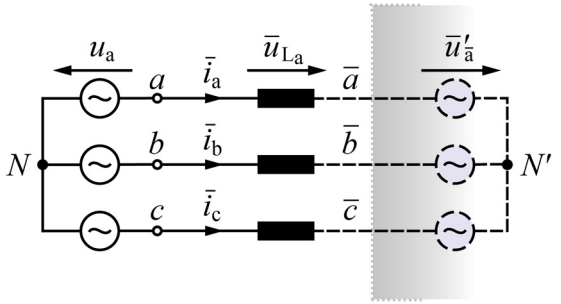
- ▶ Sinusoidal Input Current Shaping

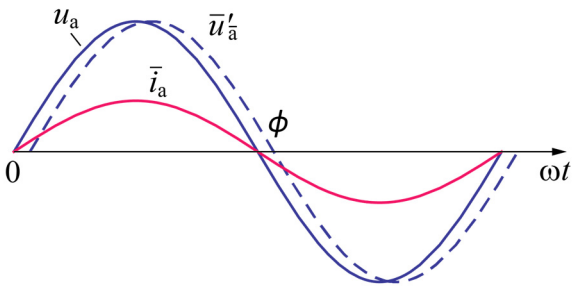
Vienna Rectifier (3)

- *Input Current Impressed by Difference of Mains & Diode Bridge Input Voltage*
- Φ = (-30°,+30°) *Limit* Due to Current Dependent Voltage Formation





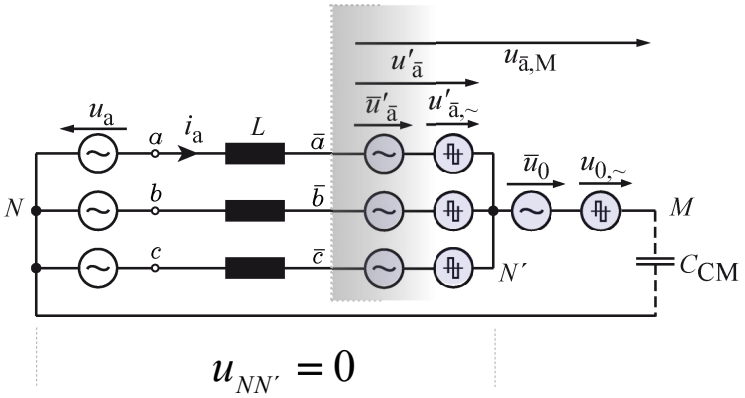


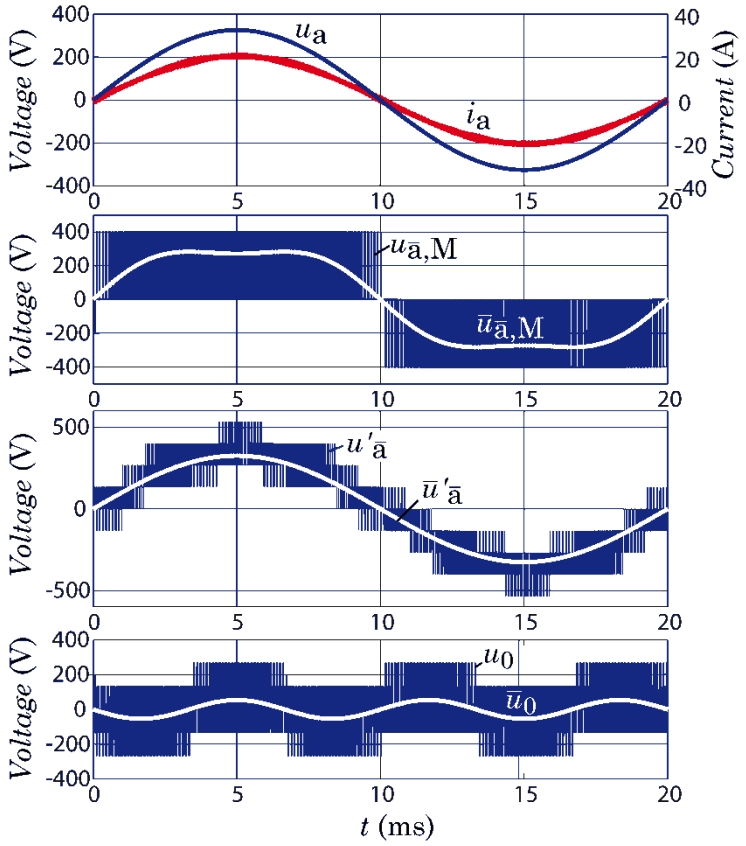


► Time Behavior of PWM Voltages

Vienna Rectifier (4)

- *3-Level Bridge Leg Characteristic / 9-Level Phase Voltage*
- Low Input Current Ripple / *Low Inductance L*
- Switching Frequency CM Output Voltage

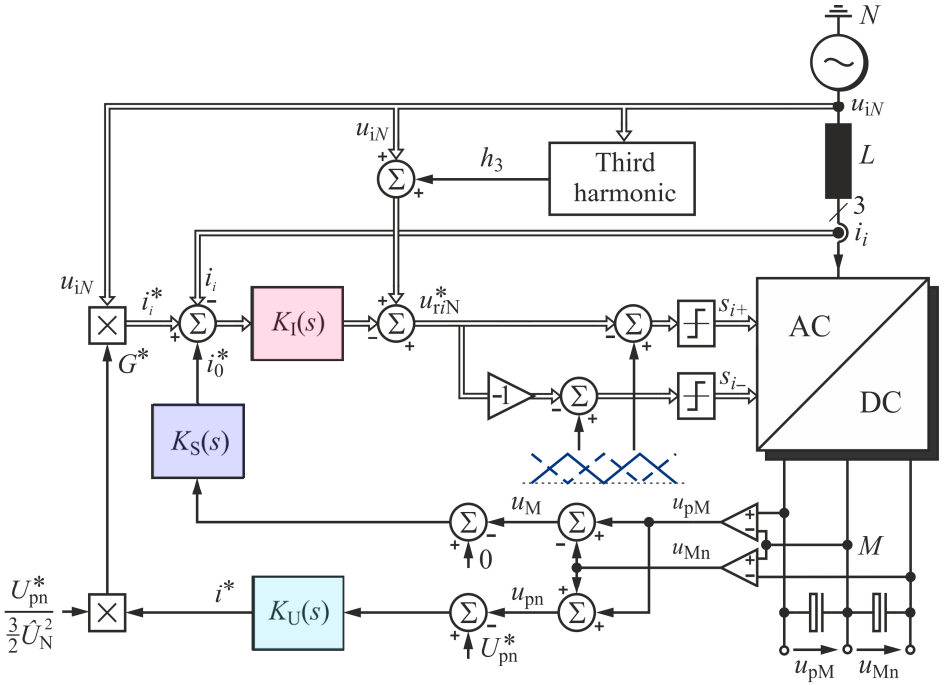


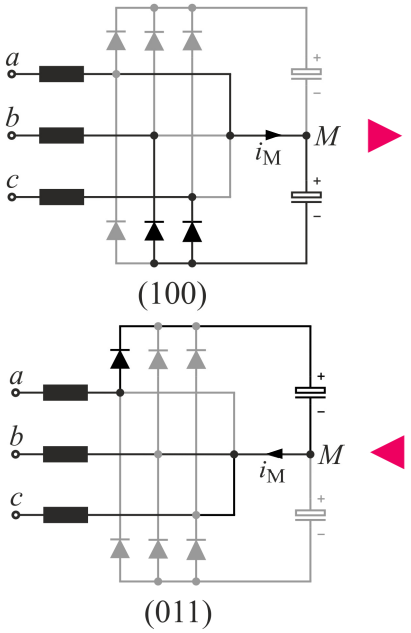


- **Multi-Loop Control Structure**

Vienna Rectifier (5)

- *Output Voltage Control / Inner Mains Current Control*
- Add. Control Loop for DC Midpoint Balancing
- Redundant Sw. States Utilized for DC Midpoint Balancing

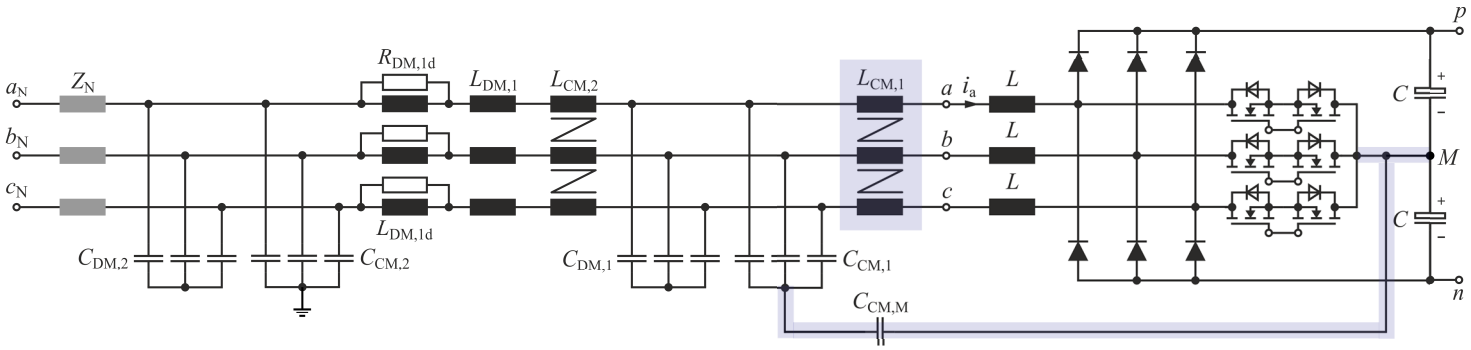




- Multi-Stage Diff. Mode & Common Mode *EMI Filter*

Vienna Rectifier (6)

- *CM EMI Filtering Utilizing Internal Cap. Connection to Virtual Star Point*
- No Limit of CM Capacitance by Max. Leakage Current
- CM Filter Stage(s) on DC-Side as Alternative



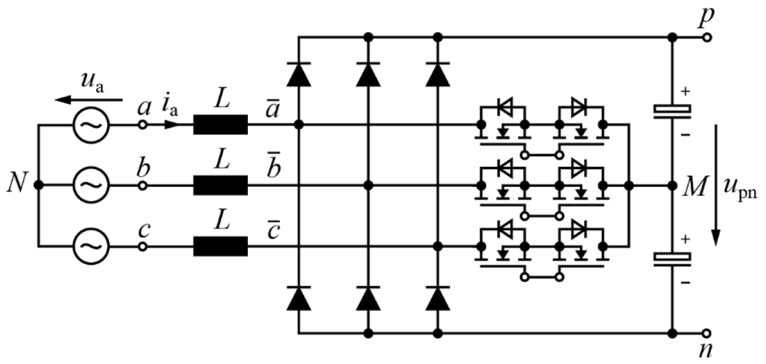
► Number of Filter Stages Dependent on Sw. Frequency

Vienna Rectifier (7)

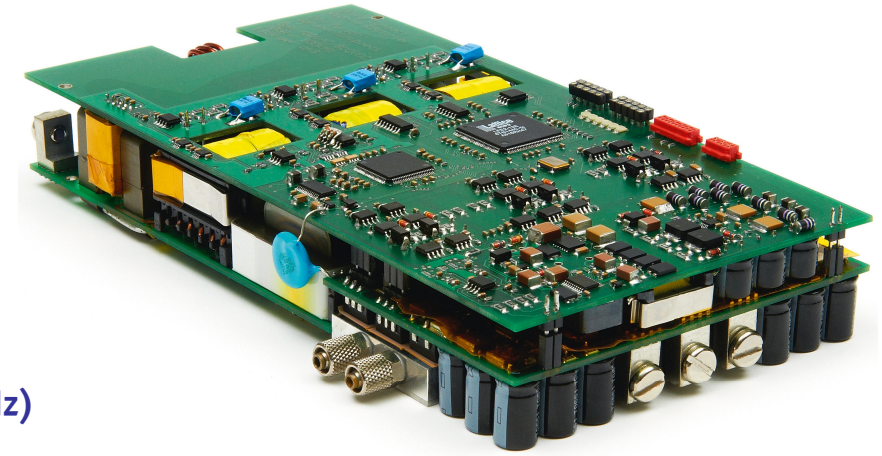
- Highly-Compact Demonstrator System
- CoolMOS & SiC Diodes
- Coldplate Cooling

P_O= 10 kW
U_N= 400V_{AC}±10%
f_N = 50Hz or 360…800Hz
U_O= 800V_{DC}

η =96.8%



★ ρ =10 kW/dm³



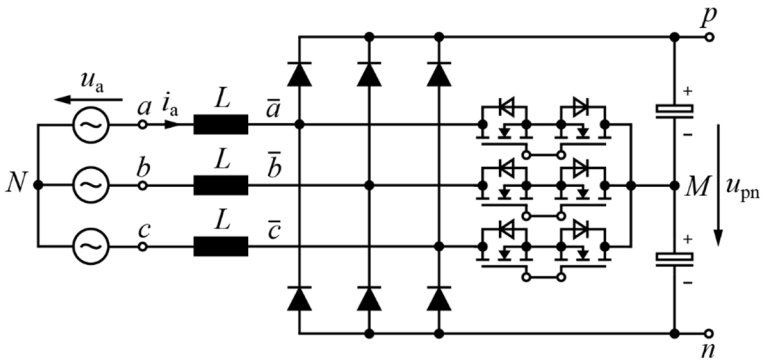
► THD_i = 1.6% @ f_N = 800Hz (f_P= 250kHz)

Vienna Rectifier (8)

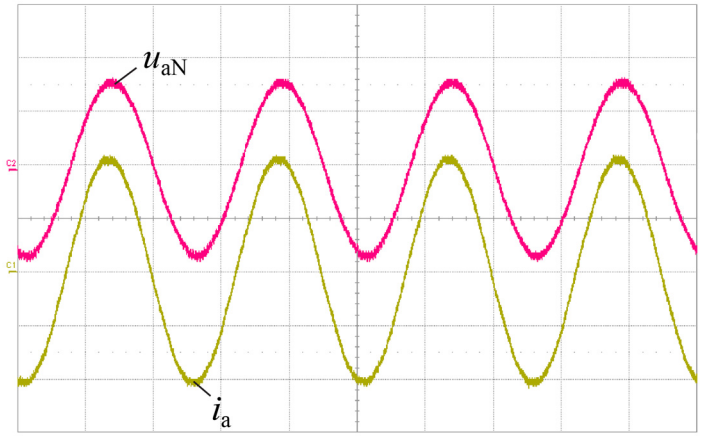
- Highly-Compact Demonstrator System
- CoolMOS & SiC Diodes
- Coldplate Cooling

P_O= 10 kW
U_N= 400V_{AC}±10%
f_N = 50Hz or 360…800Hz
U_O= 800V_{DC}

η =96.8%
ρ =10 kW/dm^3
f_P= 250kHz



10A/Div
200V/Div
0.5ms/Div

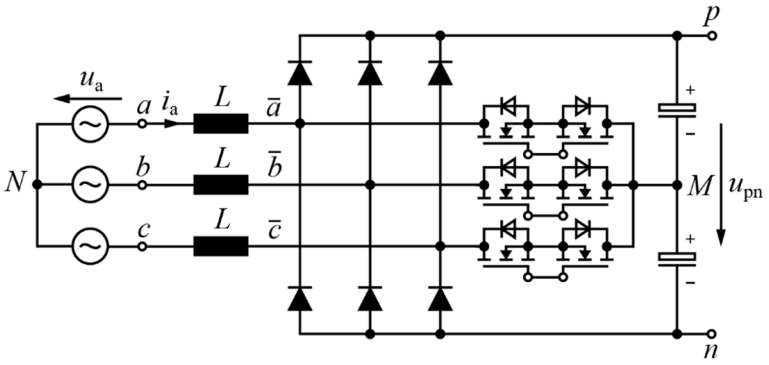


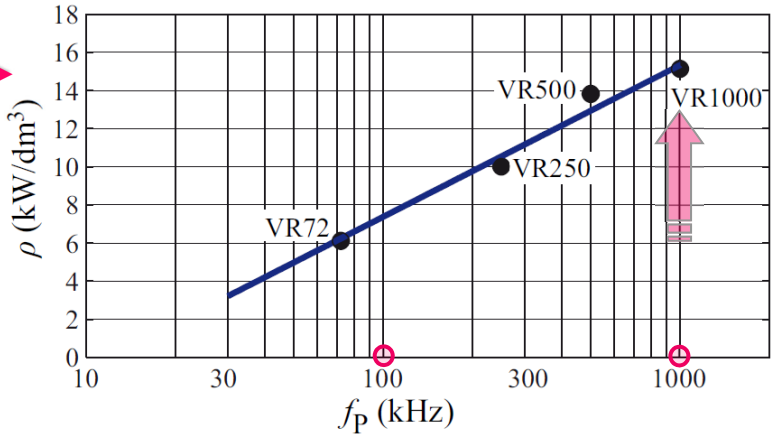
- THD_i = 1.6% @ f_N = 800Hz
- System Allows 2-Φ Operation

Vienna Rectifier (9)

- Dependency of Power Density on Sw. Frequency f_P
- CoolMOS & SiC Diodes
- Coldplate Cooling

P_O= 10 kW
U_N= 230V_{AC}±10%
f_N = 50Hz or 360…800Hz
U_O= 800V_{DC}





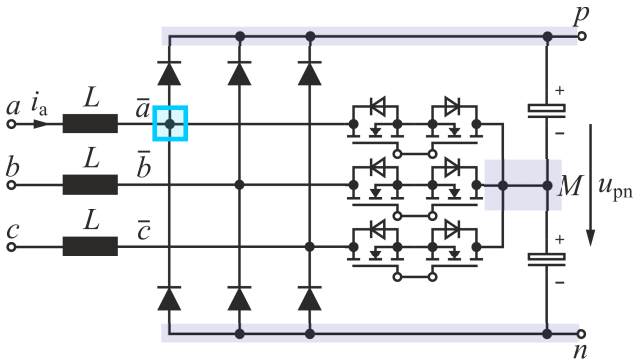
- Factor 10 in f_P → Factor 2 in Power Density
- Systems with f_P= 72/250/500/1000kHz

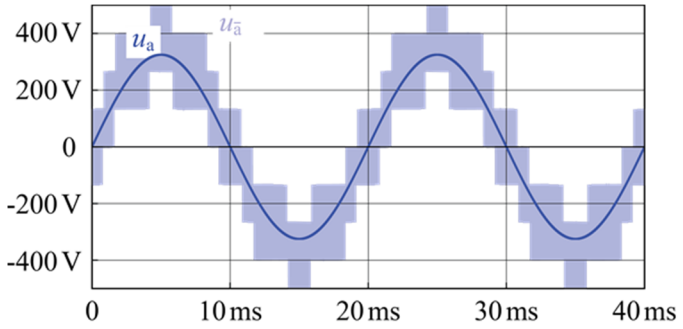
Comparative Evaluation

3L-Topology vs. 2L-Topology

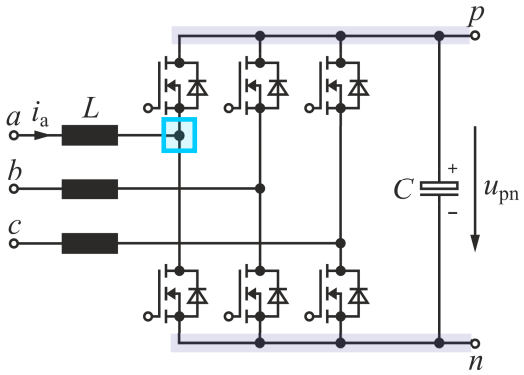
Comparative Evaluation (1)

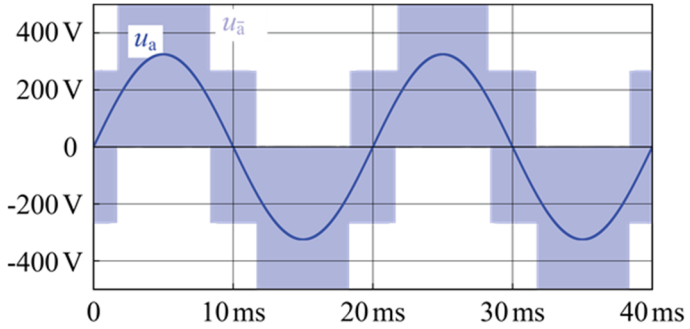
- Comparison to Standard *2-Level* PWM Rectifier
- *9 vs. 5 Volt. Levels & Factor 2...3 Lower Sw. Losses → Factor 4...6 (!) Lower L*





- Vienna Rectifier

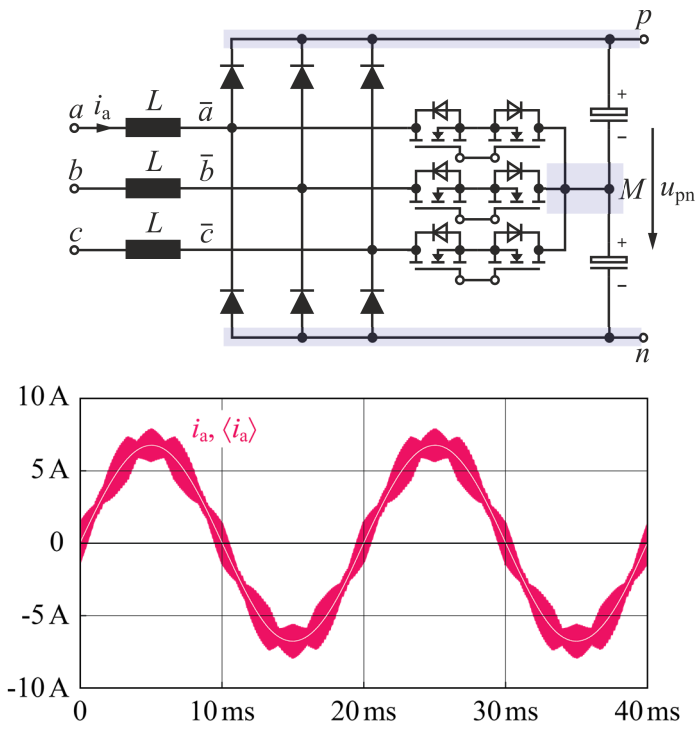




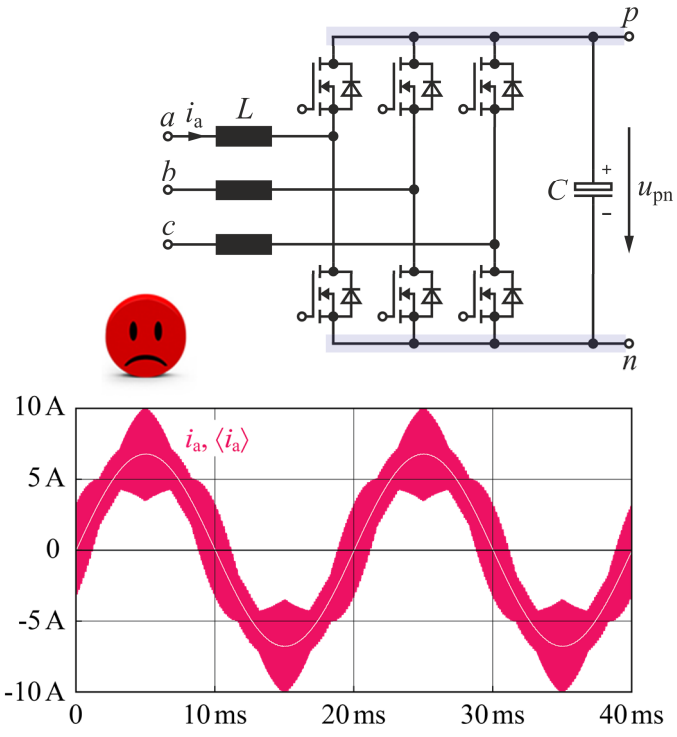
- Standard PWM Rectifier

Comparative Evaluation (2)

- Comparison to Standard *2-Level* PWM Rectifier
- *9 vs. 5 Volt. Levels & Factor 2..3 Lower Sw. Losses → 12 kW/dm³ vs. 8 kW/dm³ @ 22kW*

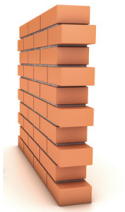


- Vienna Rectifier

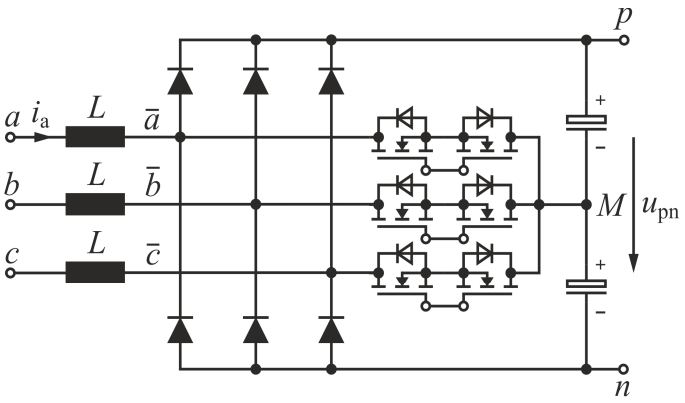


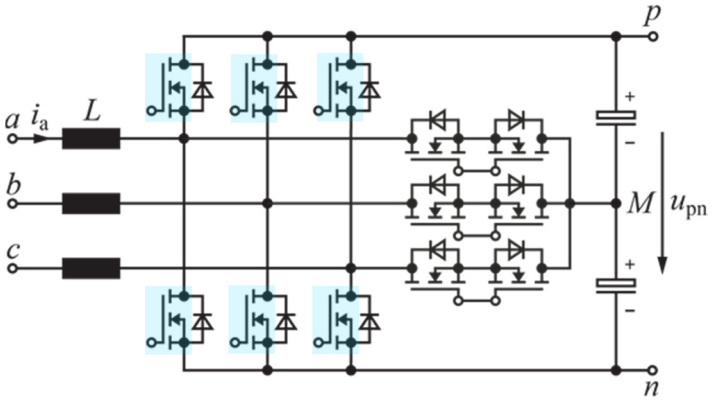
- Standard PWM Rectifier

Conceptual Limits



- *Boost-Type*
- *No Isolation*
- Unidirectional (in Basic Form)



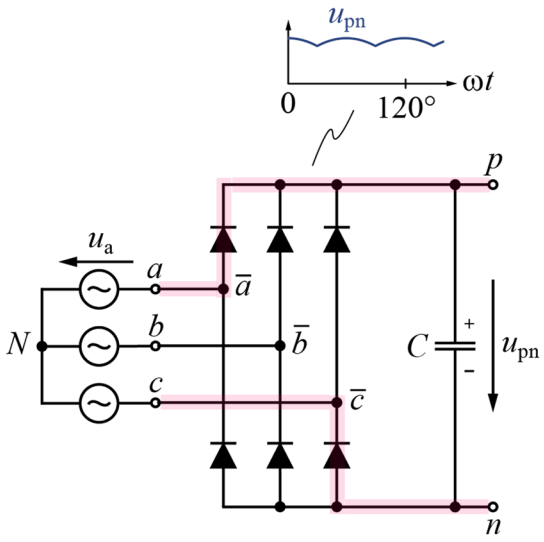


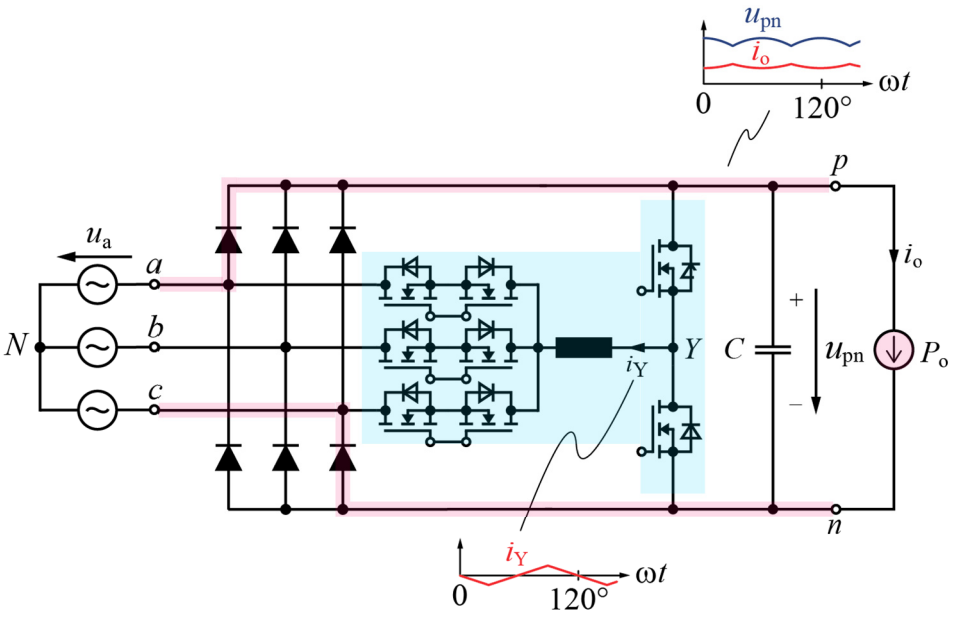
► Buck-Type & Buck-Boost Topologies / Single-Stage Isolated Systems

Buck-Type

Integr. Active Filter PFC Rectifier
1-of-3 PWM Rectifier
SWISS Rectifier

Integr. Active Filter (*IAF*) PFC Rectifier



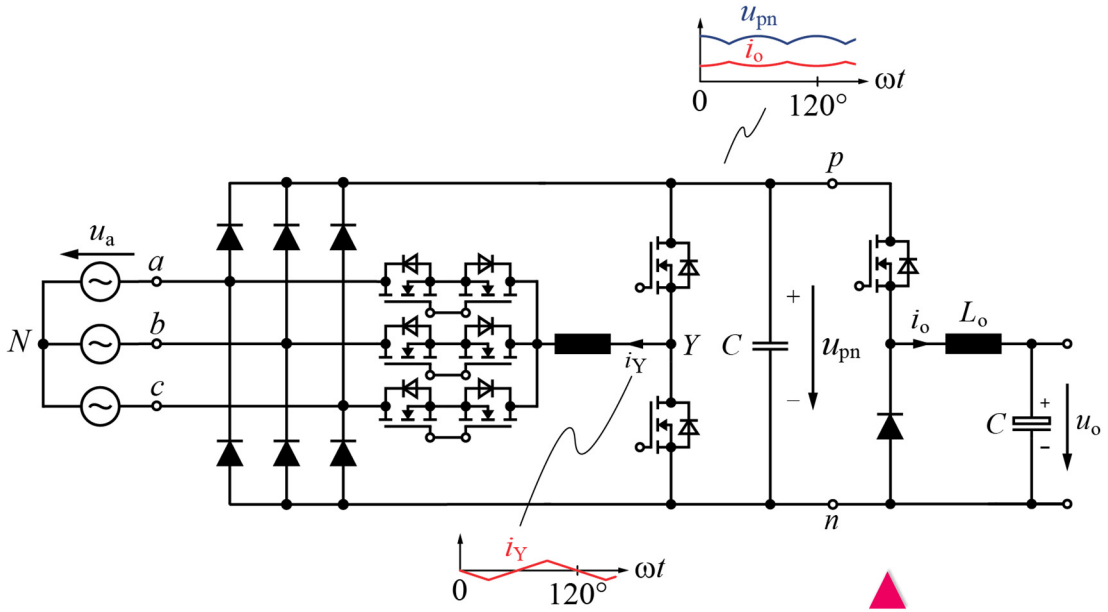


- Non-Sinusoidal Mains Current

→ P_0= const. Required
→ *NO (!) Output Voltage Control*
→ *Basic Idea: M. Jantsch, 1997 (for PV Inv.)*

IAF Rectifier

- 3rd Harm. Injection into "Middle" Phase
- *Buck-Output Stage* for P_0= const. & *Outp. Voltage Control*
- Sinusoidal Current in All Phases

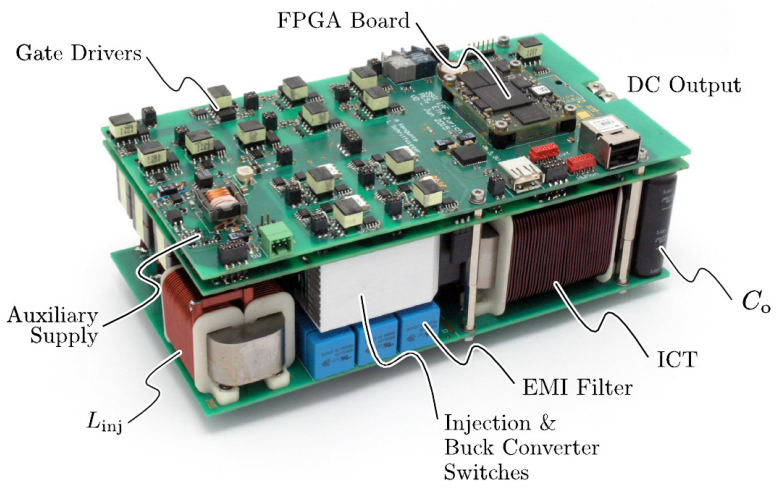


► Buck-Stage Could be Replaced by *Isol. DC/DC Conv.* or Inverter

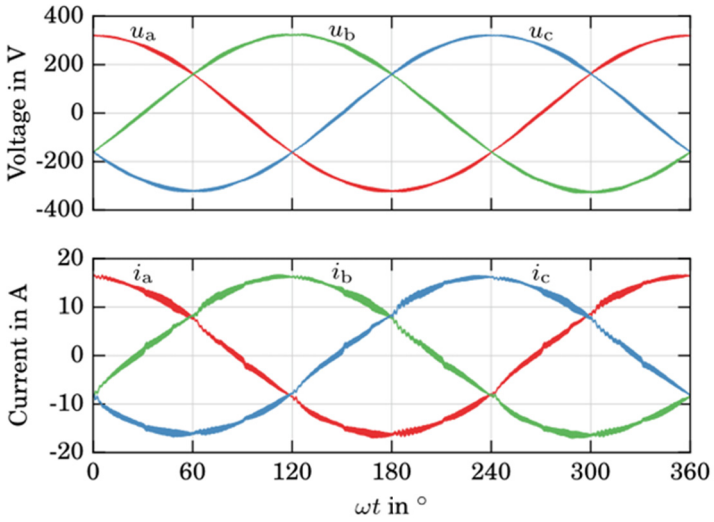
IAF Rectifier Demonstrator

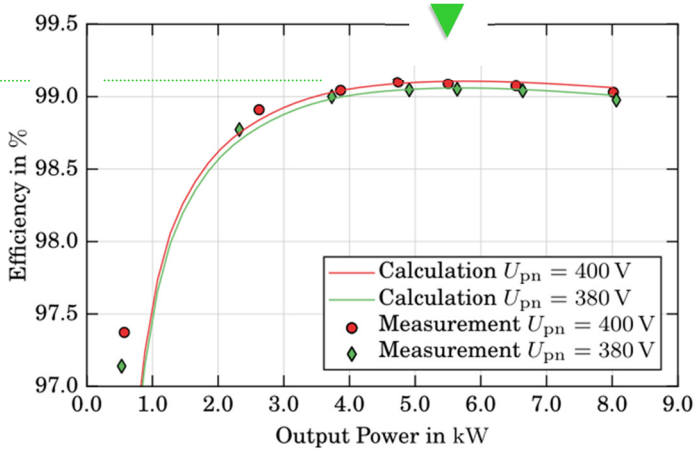
- Efficiency η > 99.1% @ 60% Rated Load
- Mains Current $THD_I \approx 2\%$ @ Rated Load
- Power Density $\rho \approx 4 kW/dm^3$

P_O= 8 kW
U_N= 400V_{AC} → U_O= 400V_{DC}
f_S = 27kHz



- SiC Power MOSFETs & Diodes
- 2 Interleaved Buck Output Stages

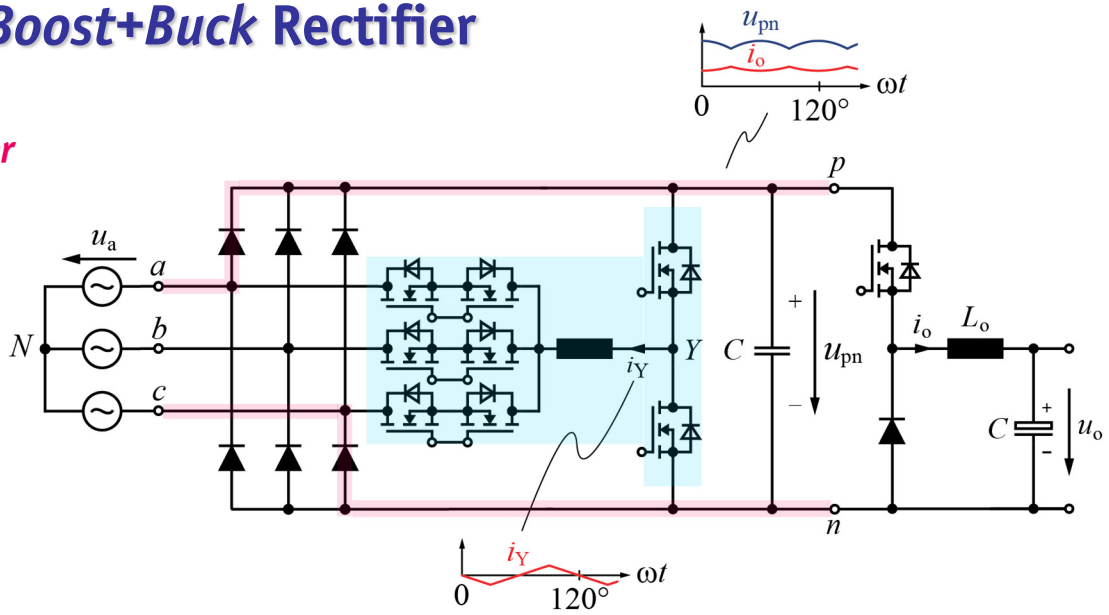




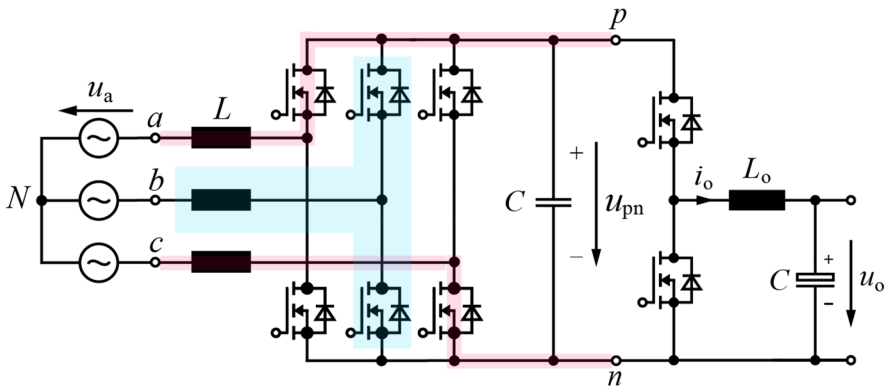
1-out-of-3 Rectifier

1-out-of-3 PWM *Boost+Buck* Rectifier

- *IAF Buck-Type Rectifier*
- Unidirectional

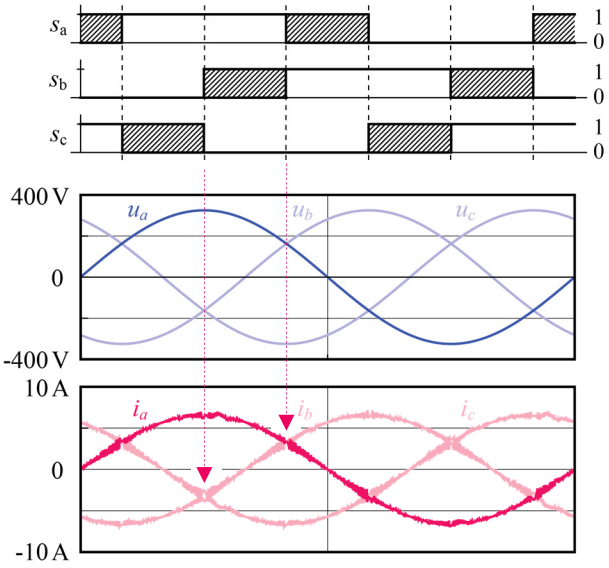


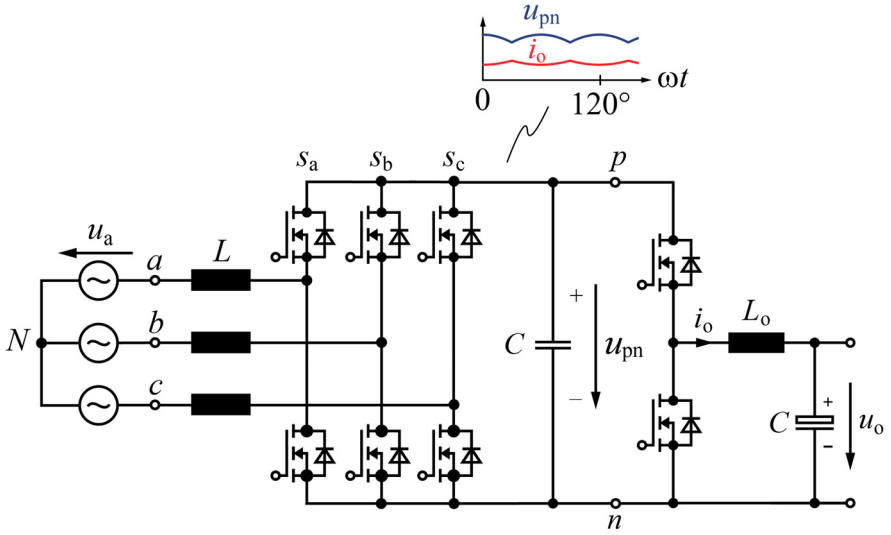
- *Buck-* or *Boost+Buck-Type*
- Bidirectional / Inv. Operation
- *Similar Concept: D. Neacsu, 2012*



1/3 PWM Boost+Buck Rectifier

- *Buck-Stage Utilized for DC Link Voltage Shaping / Control of 2 Mains Phase Currents*
- *Low Switching Losses* / High Efficiency
- Cont. Input & Output Currents



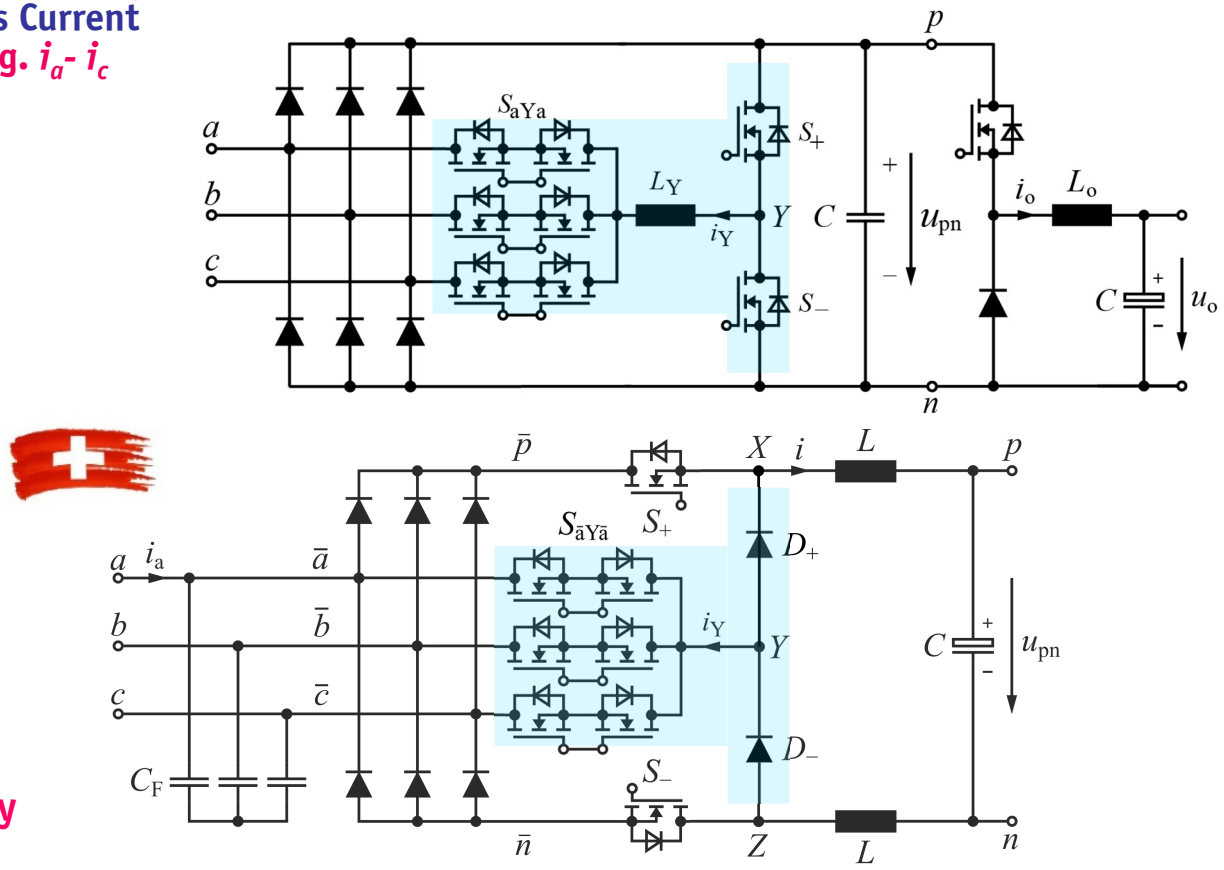


▶ Option → Operation as *Conv. Boost-Type Const. DC-Link Voltage* PWM Rectifier

SWISS Rectifier

Swiss Rectifier

- Controlled Output Voltage
- Sinusoidal Mains Current
- i_y Def. by KCL: E.g. i_a- i_c

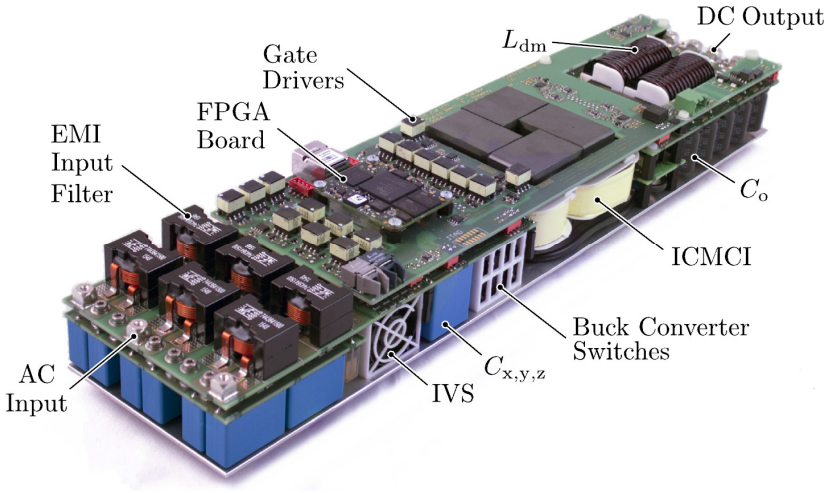


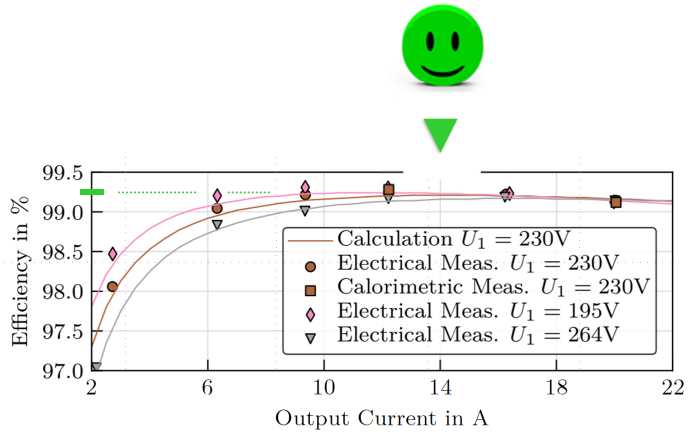
- Low Complexity

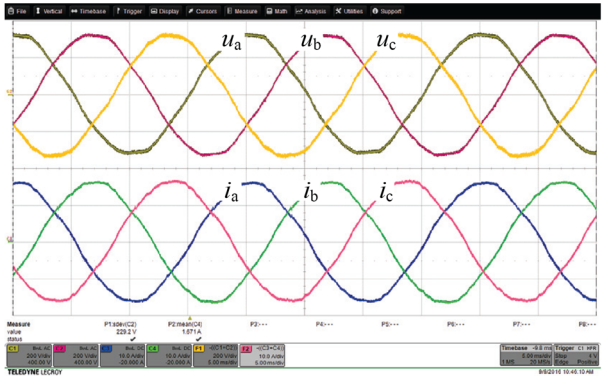
Swiss Rectifier Demonstrator

- Efficiency η = 99.26% @ 60% Rated Load
- Mains Current $THD_I \approx$ 0.5% @ Rated Load
- Power Density $\rho \approx 4\text{kW/dm}^3$

P_O= 8 kW
U_N= 400V_{AC} → U_O= 400V_{DC}
f_S = 27kHz







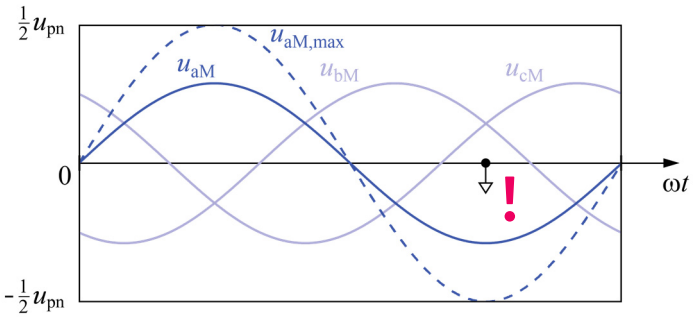
- SiC Power MOSFETs & Diodes
- Integr. CM Coupled Output Inductors (ICMCI)

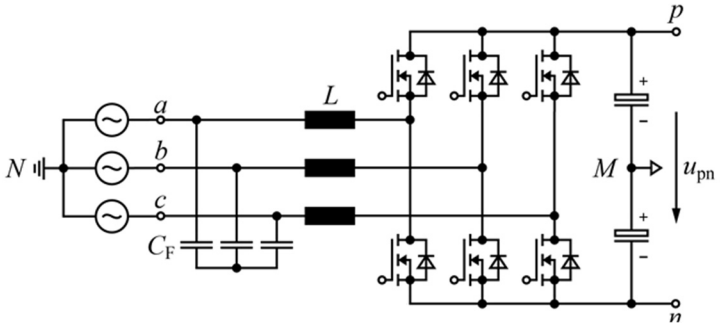
Buck+Boost-Type

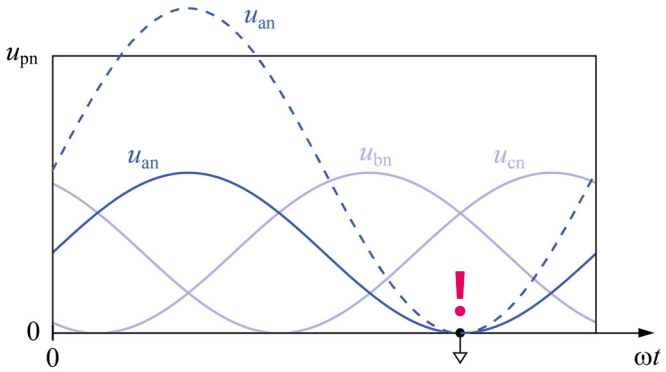
Y_3-Rectifier

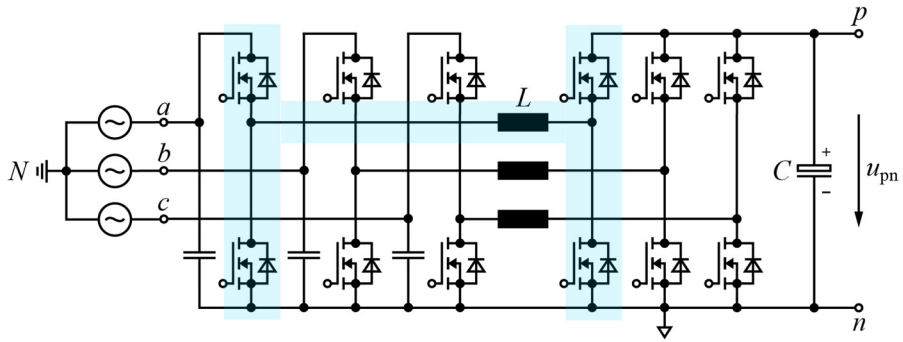
Buck+Boost PWM Y_3-Rectifier

- *Voltage Reference Potential Shifted from DC-Midpoint to Neg. DC-Link Rail*
- *Front-End Buck-Stage / Phase → Buck+Boost Operation*







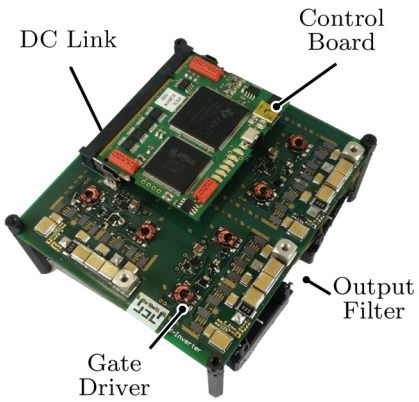


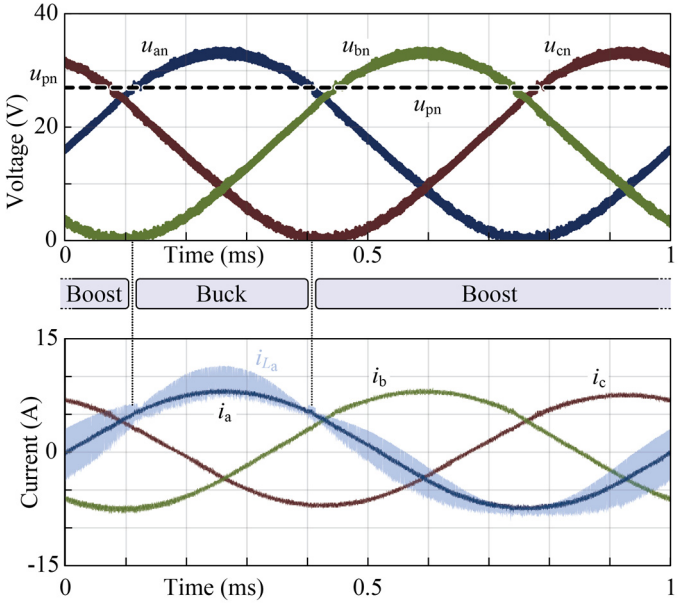
▶ *Bidirectional* & Wide Input and Output Voltage Range

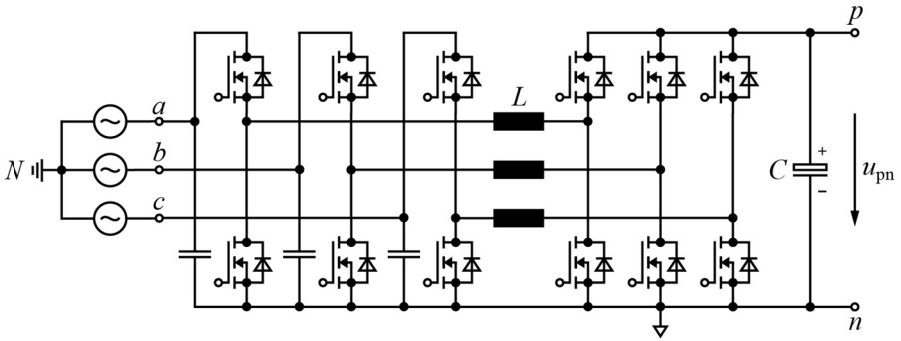
Basic Idea: S. Cuk, 1982

Y_3-Rectifier

- *Rectifier Operation with Fully Controlled Input Filter*
- *Inverter Operation with Continuous Output Voltage (!)*
- All-GaN Demonstrator





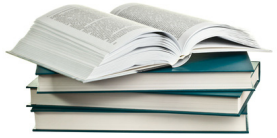


→ Session T32 ← "Grid Applications", ROOM 217-D, Thursday, 8:30 a.m. – 11:20 a.m.

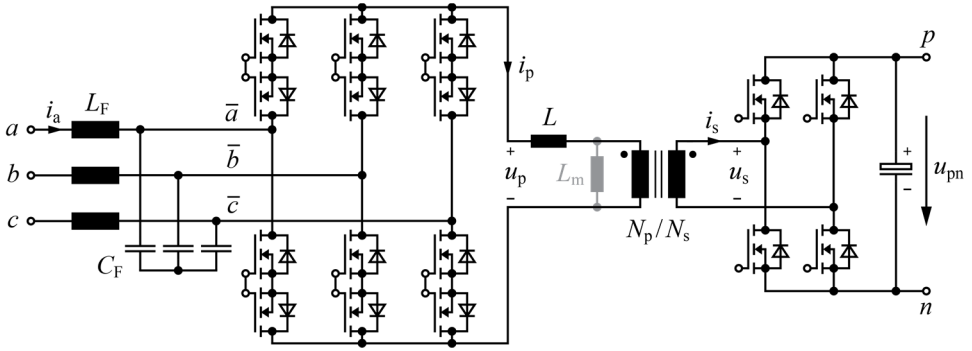
Isolated Single-Stage

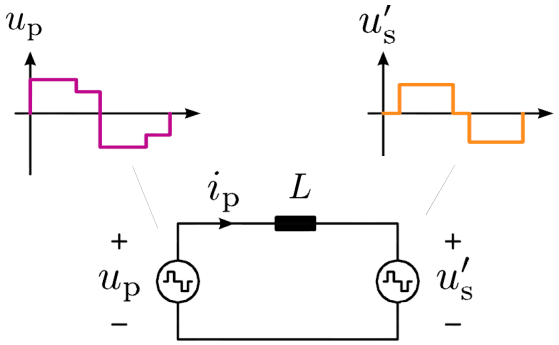
Matrix-Type Rectifier
D3AB-Rectifier

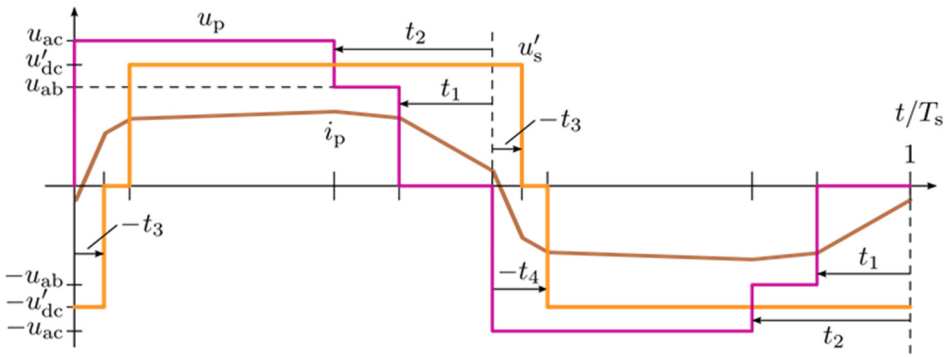
Isolated *Matrix-Type* PFC Rectifier



- *Based on Dual Active Bridge* (DAB) Concept
- Opt. Modulation ($t_1 \ldots t_4$) for Min. Transformer RMS Curr. & ZVS or ZCS
- Allows Buck-Boost Operation







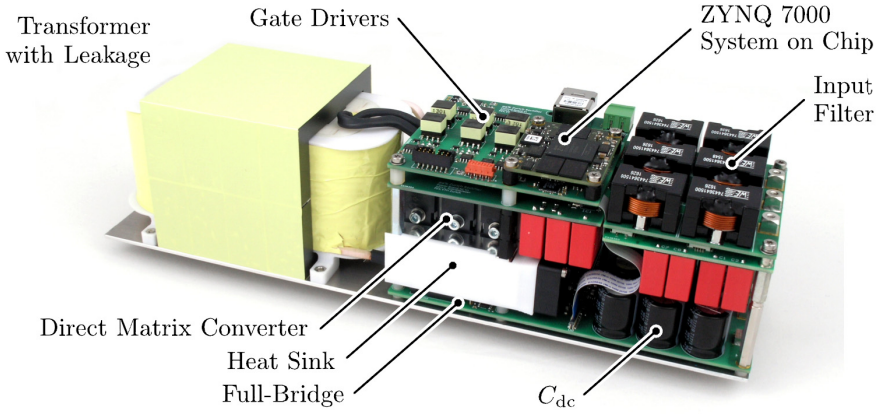
▶ Equivalent Circuit

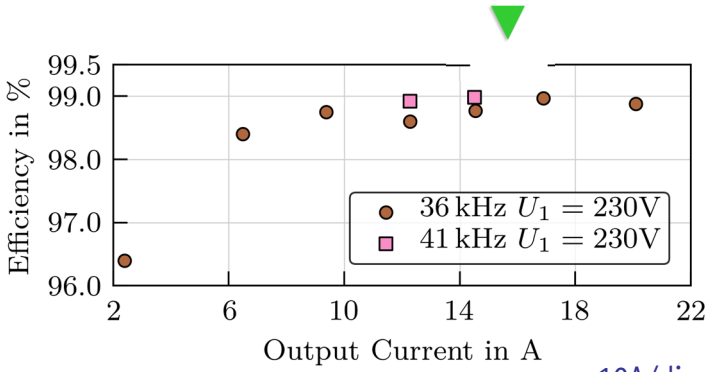
▶ Transformer Voltages / Currents

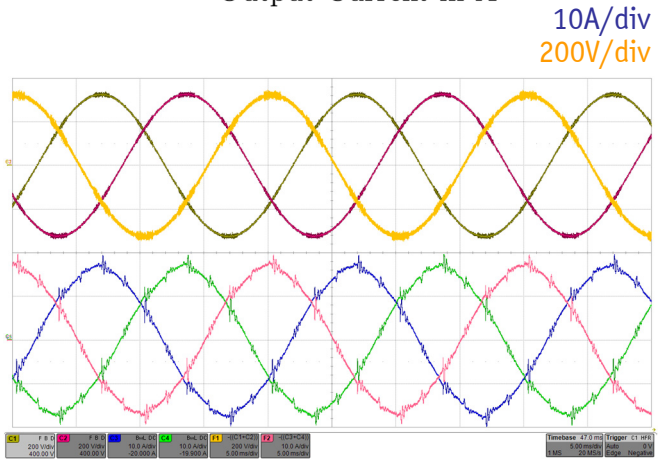
Isolated *Matrix-Type* PFC Rectifier

- Efficiency η = 98.9% @ 60% Rated Load (ZVS)
- Mains Current $THD_I \approx 4\%$ @ Rated Load
- Power Density $\rho \approx 4\text{kW/dm}^3$

P_0= 8 kW
U_N= 400V_{AC} → U_0= 400V_{DC}
f_S = 36kHz





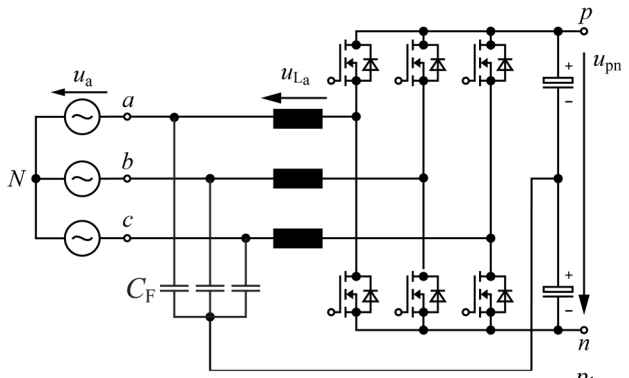


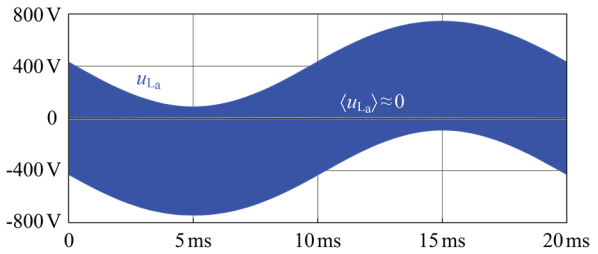
- 900V / 10mΩ SiC Power MOSFETs
- Opt. Modulation Based on 3D Look-Up Table

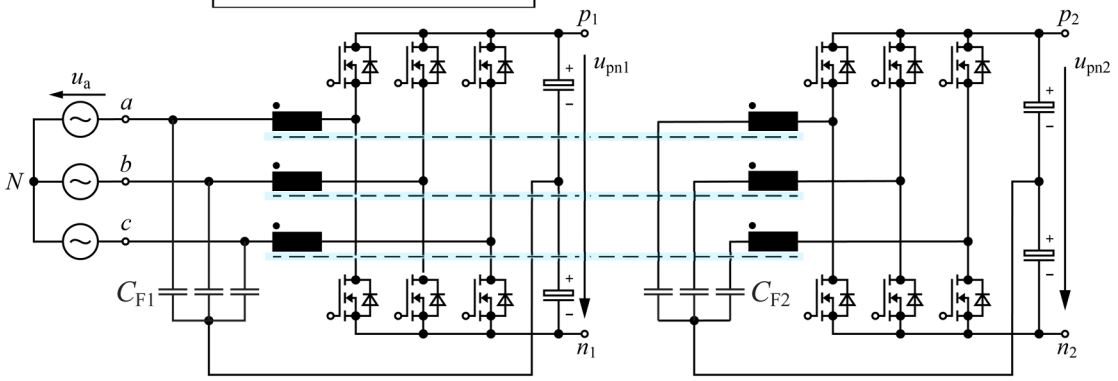
Isolated Dual 3-Φ Active Bridge Rectifier

Dual 3-Φ Active Bridge PFC Rectifier

- *HF-Components of Boost Ind. Voltages Utilized for Power Transfer*
- *Dual Active Bridge Concept*
- *ZVS*



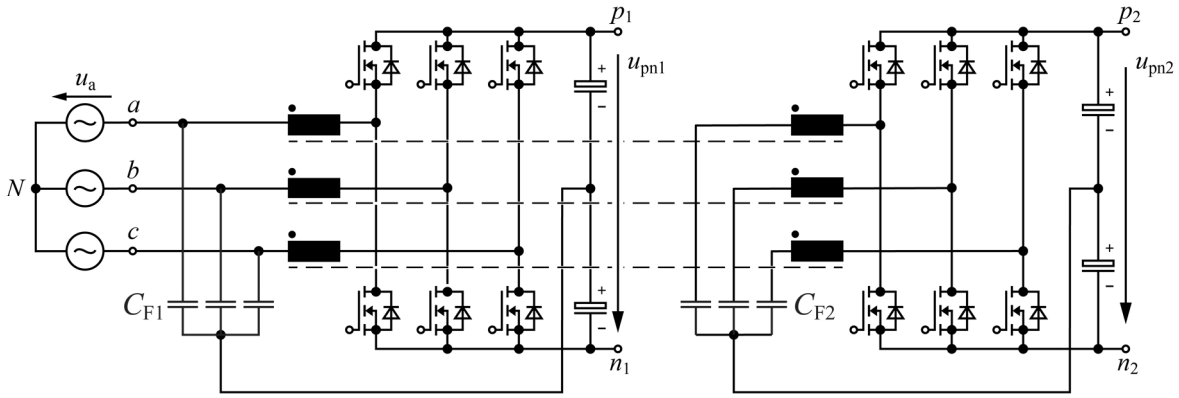


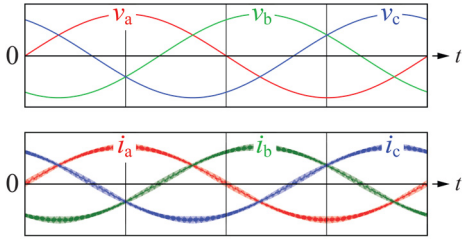


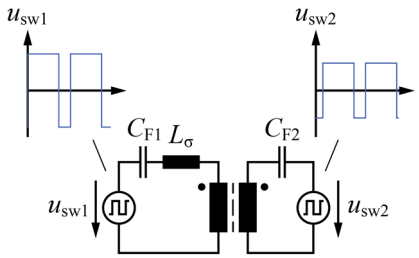
▶ *Three-Port System* - AC Input / Isol. DC Output / Non-Isol. DC Output

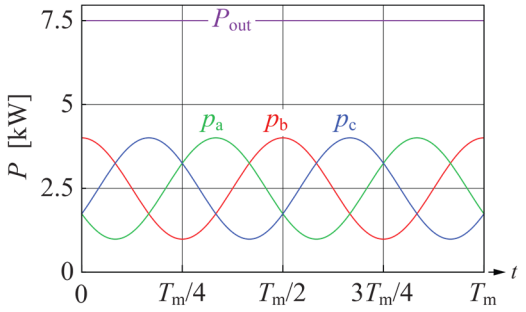
Dual 3-Φ Active Bridge PFC Rectifier

- *HF-Components of Boost Ind. Voltages Utilized for Power Transfer*
- *Dual Active Bridge Concept*
- *ZVS*

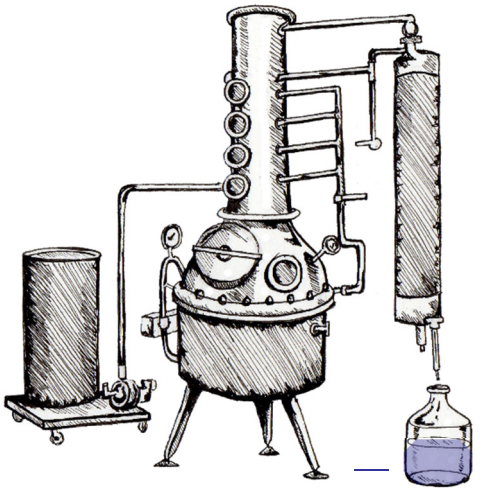








► *Three-Port System* - AC Input / Isol. DC Output / Non-Isol. DC Output



Source: whiskeybehavior.info

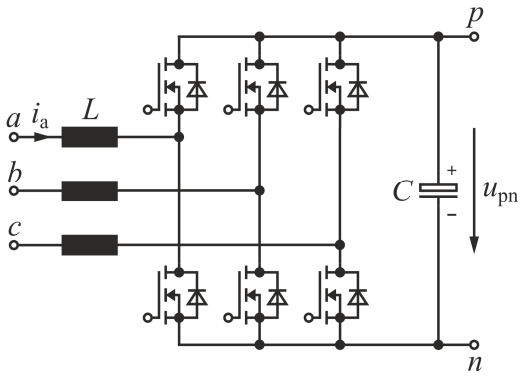
Overall Summary

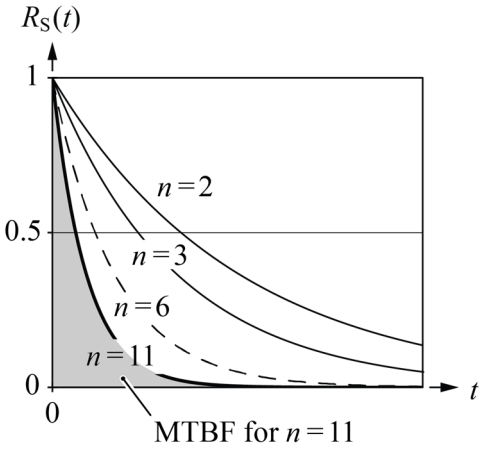
Conclusions

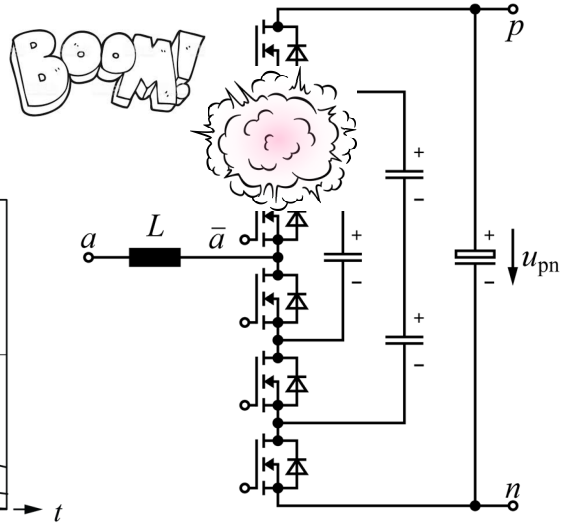
- Several *"Black-Belt"* PFC Rectifier Topologies
- Highly-Efficiency → 99.5% / 99% Non-Isolated/Isolated
- High Compactness → 10...12kW/dm³

Further Improvements

- Higher Number of Levels (?)





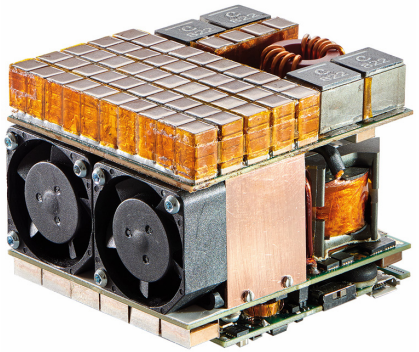


- Higher Number of Levels → Lower Reliability → Only Fault-Tolerant Topologies Survive!

Further Improvements (cont.)

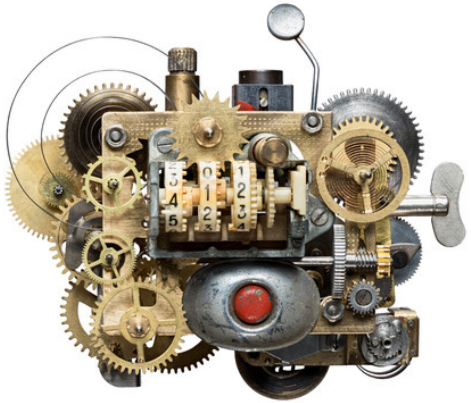
- Faster Switching (?)

Google
Little-Box 2.0
240 W/in³



- 140W/in³ @ f_S=250...1000kHz
- 240W/in³ @ f_S=140kHz
- Mapping of Comp. Technologies into Syst. Performance Largely Unclear

- Faster Design & Development (!)

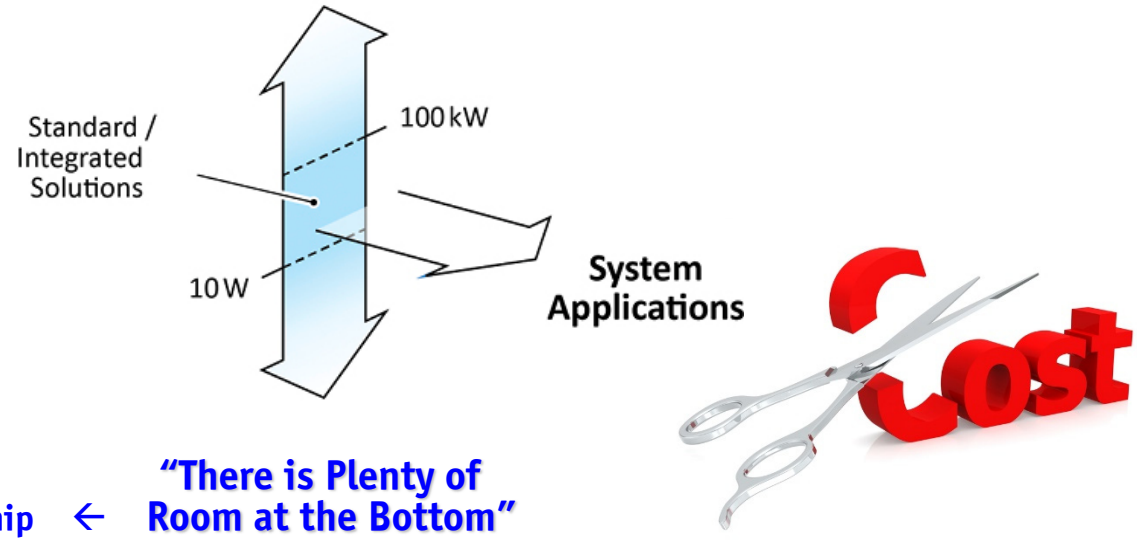


- Mutual Coupling of Performance Indices
- Simulation Tools for Optimal Design / Trade-Offs
- Design for Manufacturing & Measurement
- "Digital Twin"– Measurement & Simulation

Future Development 1/2

- Commoditization / Standardization
- Extreme Cost Pressure (!)

"There is Plenty of Room at the Top" → Medium Voltage/Frequency Solid-State Transformers

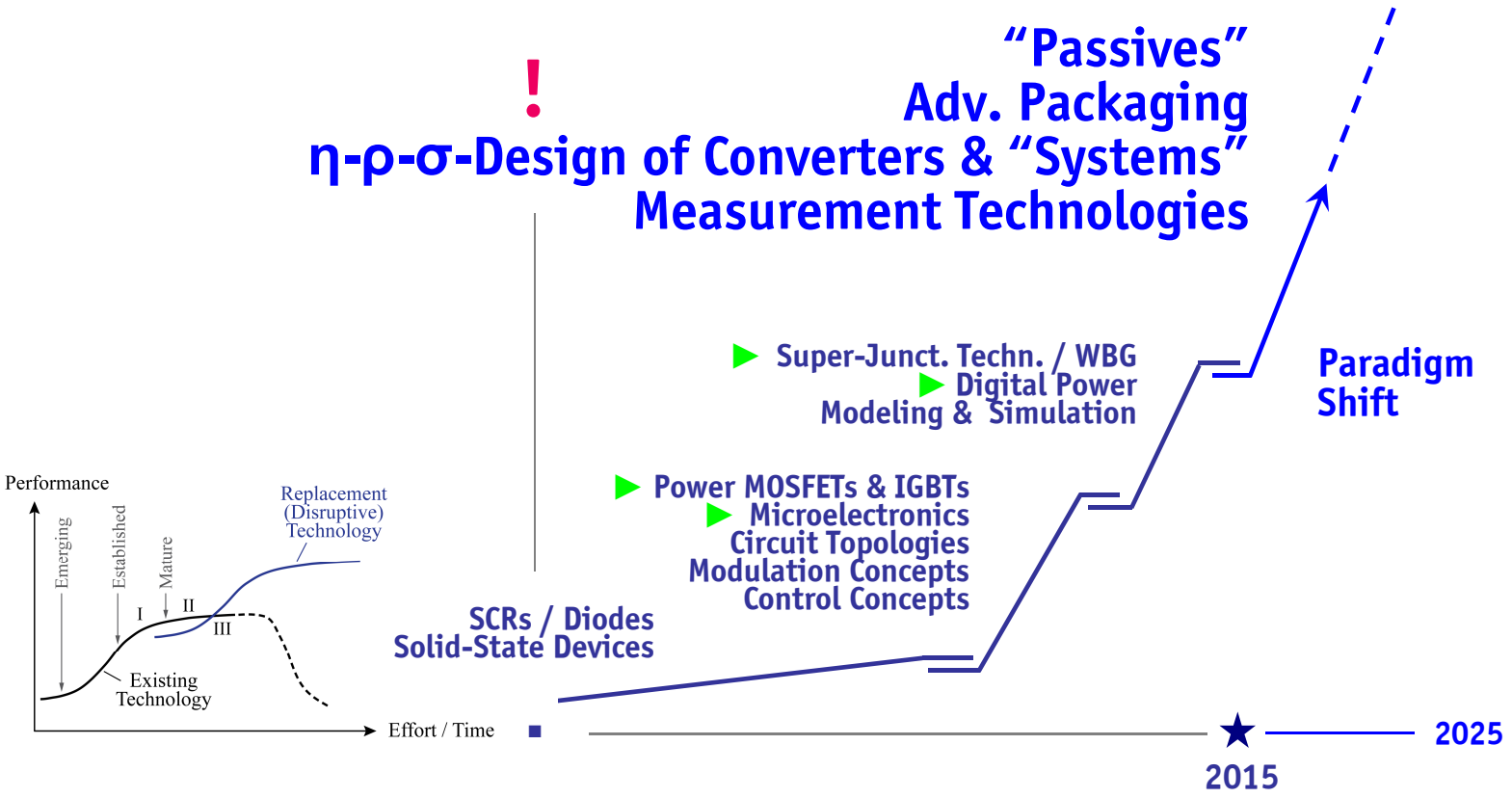


Power-Supplies on Chip ← "There is Plenty of Room at the Bottom"

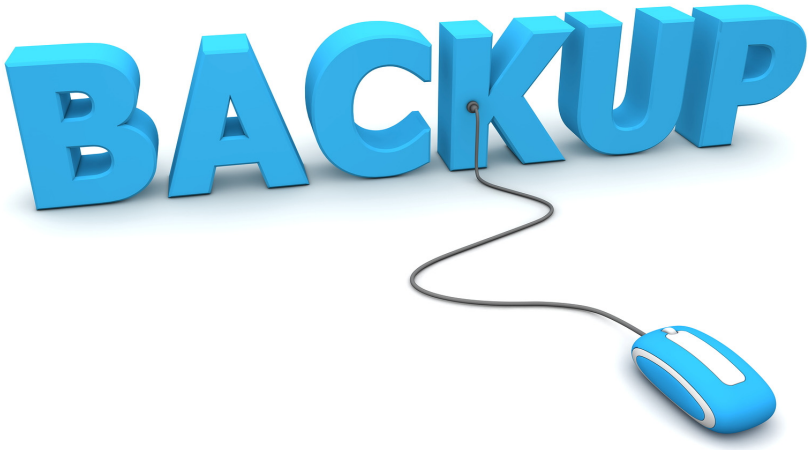
► Key Importance of Technology Partnerships of Academia & Industry

Future Development 2/2

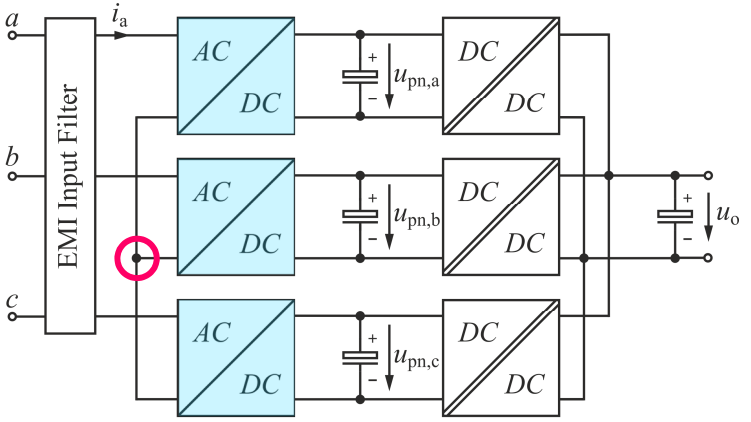
- Extrapolation of Technology S-Curve



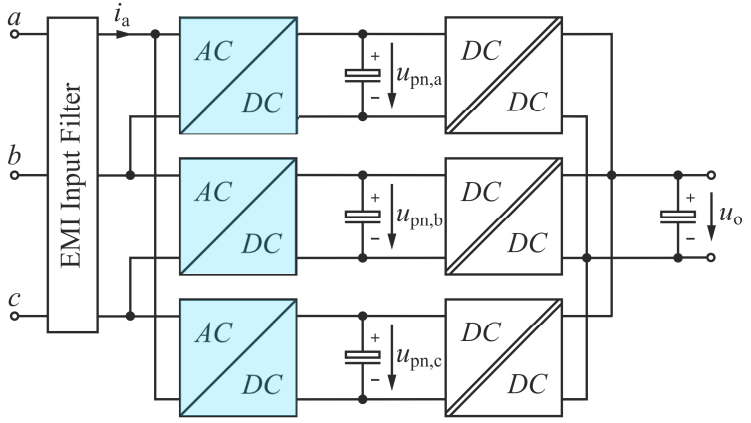
Thank You !


BACKUP

Y -Rectifier
Δ-Rectifier

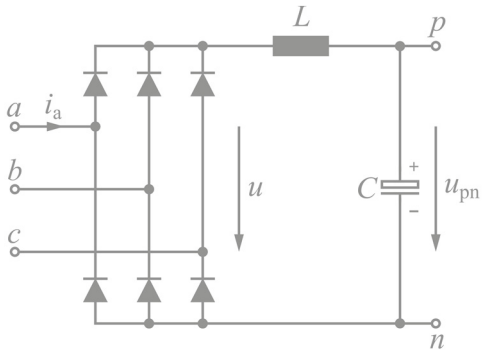


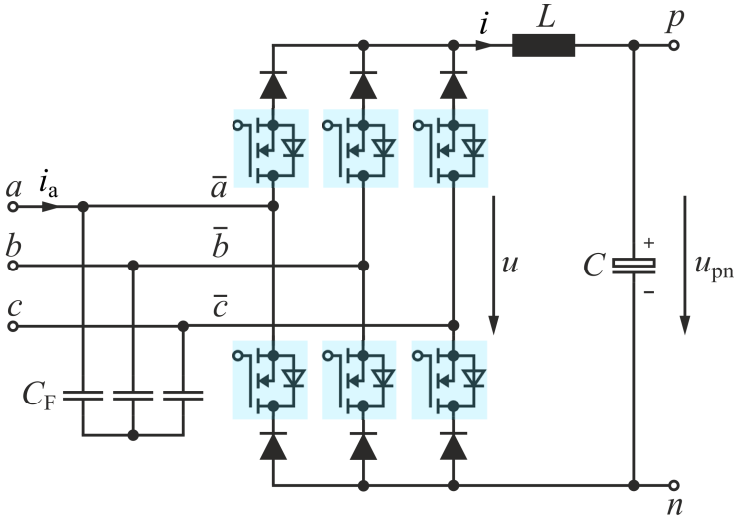
- Balancing of Phase Modules
- High Semiconductor Voltage Stress



■ Δ-Rectifier Clearly Preferable

Six-Switch *Buck-Type* PFC Rectifier



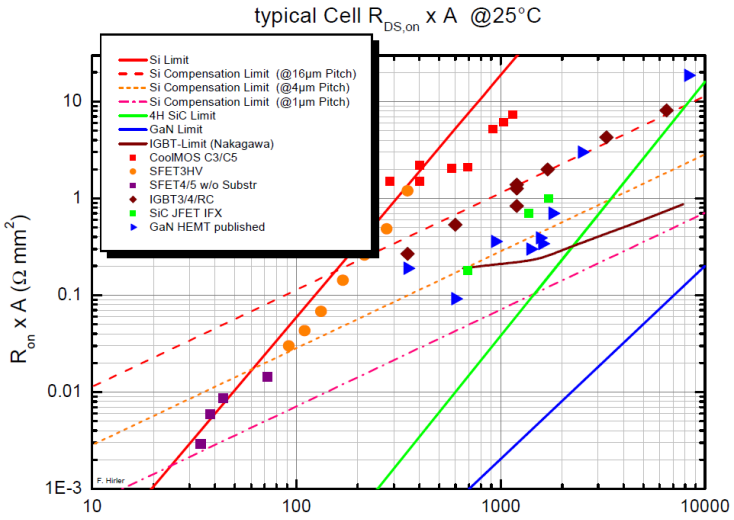


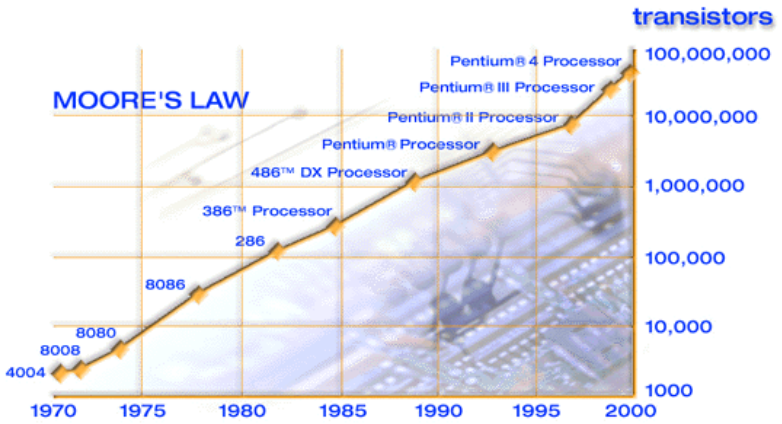
- **Derivation of Rectifier Topology**

→ **Controllability of Conduction State**
→ **Phase-Symmetry / Bridge-Symmetry**

Technology Progress – *Technology Push*

- WBG Semiconductor Technology → Higher Efficiency, Lower Complexity
- Microelectronics → More Computing Power



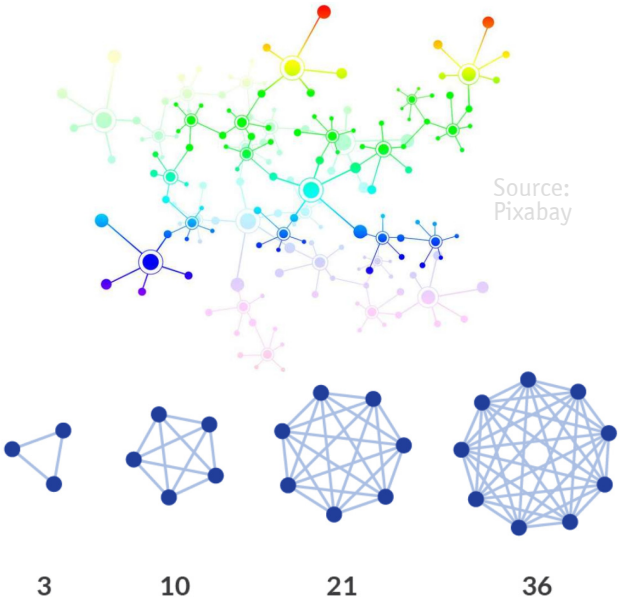


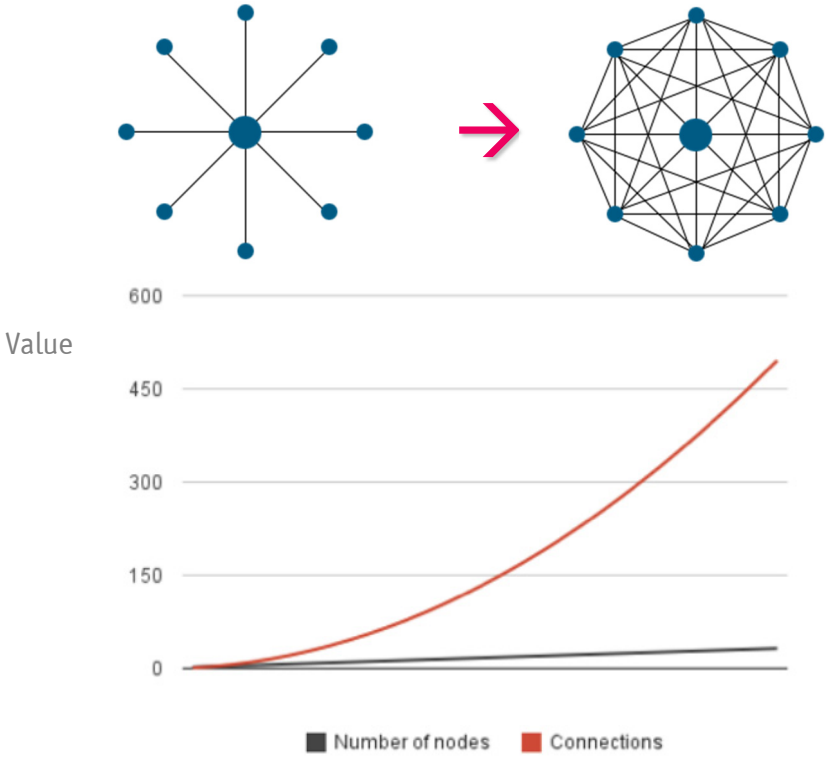
→ + Advanced Packaging (!)

→ Moore's Law

System / Smart Grid Drivers

- **Metcalfe's Law**
  - **Moving form Hub-Based Concept to Community Concept Increases Potential Network Value Exponentially (~n(n-1) or ~n log(n))**





Future Development

"Devices"
- Minimize / Avoid Packages → (PCB) Embedding
- Integrate Driver Stage
- Integrate Sensors / Monitoring
- Multiple Use of Isolated Gate Drive Communication Channel
- Offer Test Devices with Integrated Measurement Function
- Facilitate (Double Sided) Heat Extraction

Converters
- Standardized Very Low Cost Building Blocks
- "Application Specific" = Wide Operating Range Standardized Blocks
- Self-Parametrization
- Bidirectional Converters

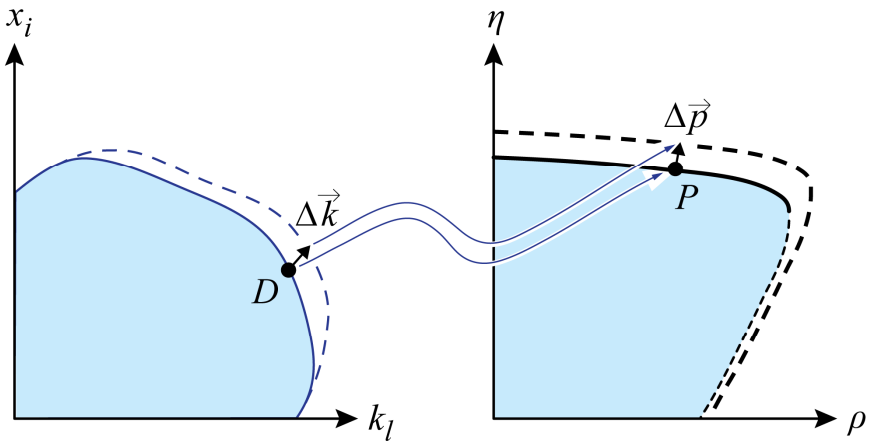
Systems
- AC and DC Distribution
- Single Converter vs. Combination of Modules / Cells
- Initial Costs / Life Cylce Cost Trade-off
- Grid 4.0

Design
- Minimize Design Time / Fully Computerized
- Maximize Design Flexibility for Appl. Specific Solution (PCB)
- Maximize Design Insight for Trade-off Analysis
- Design for Manufacturing (Planar / PCB Based)

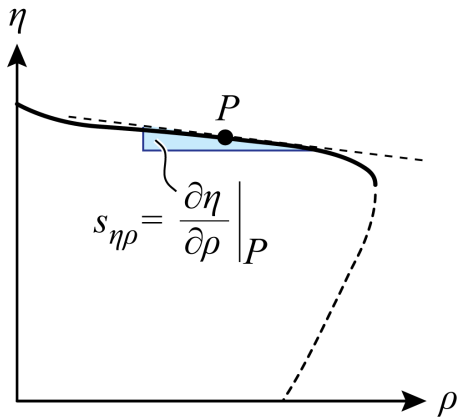
Literature
- More & More "White Noise"

Technology Sensitivity Analysis Based on η-ρ-Pareto Front

- Sensitivity to Technology Advancements
- Trade-off Analysis

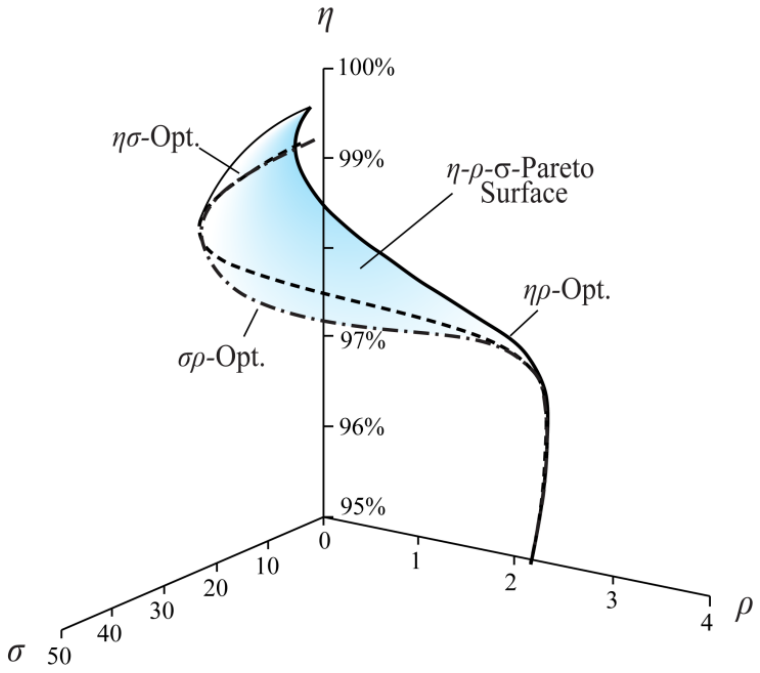


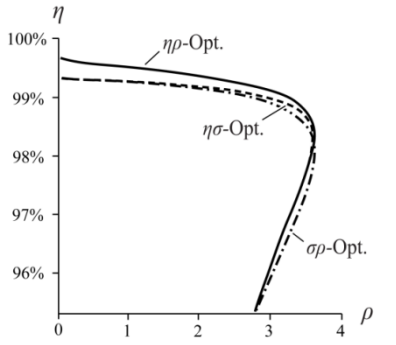
Design Space Performance Space

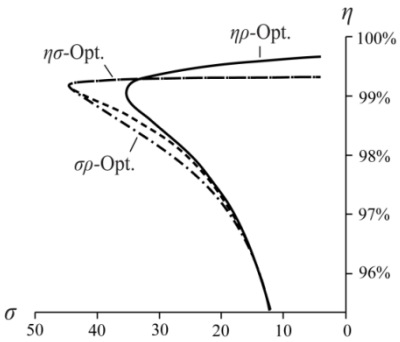


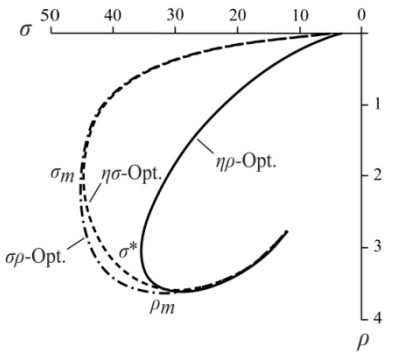
Converter Performance Evaluation Based on η-ρ-σ-Pareto Surface

- σ: kW/$



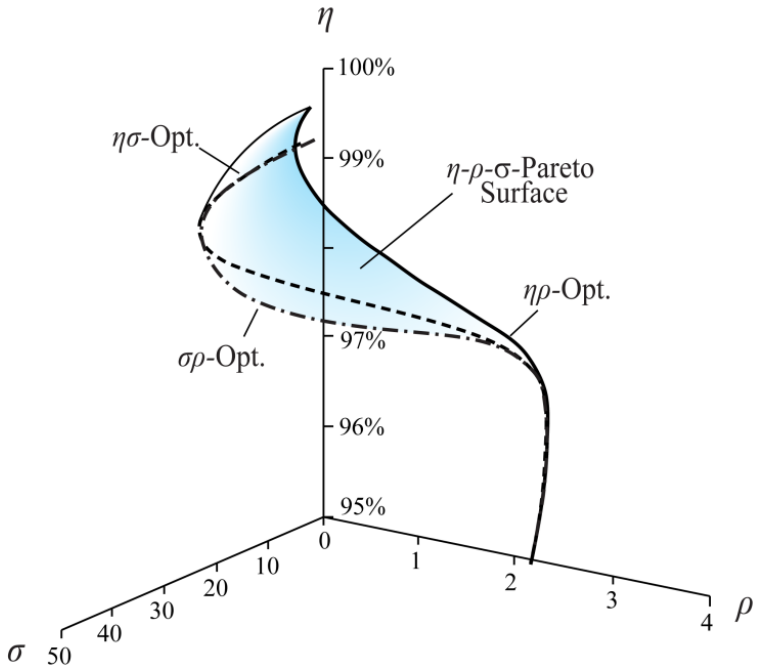


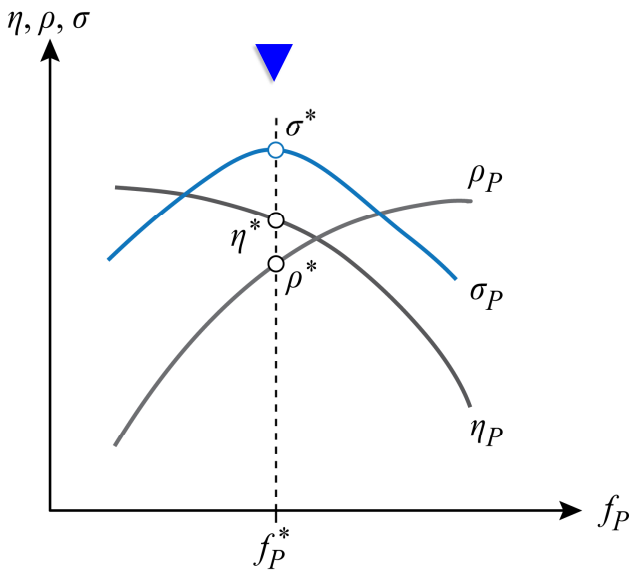




Converter Performance Evaluation Based on η-ρ-σ-Pareto Surface

- *´Technology Node´*





Technology Node: $(\sigma^*, \eta^*, \rho^*, f_P^*)$