PSI3441 – Arquitetura de Sistemas Embarcados

- Portas de Entrada e Saída GPIO

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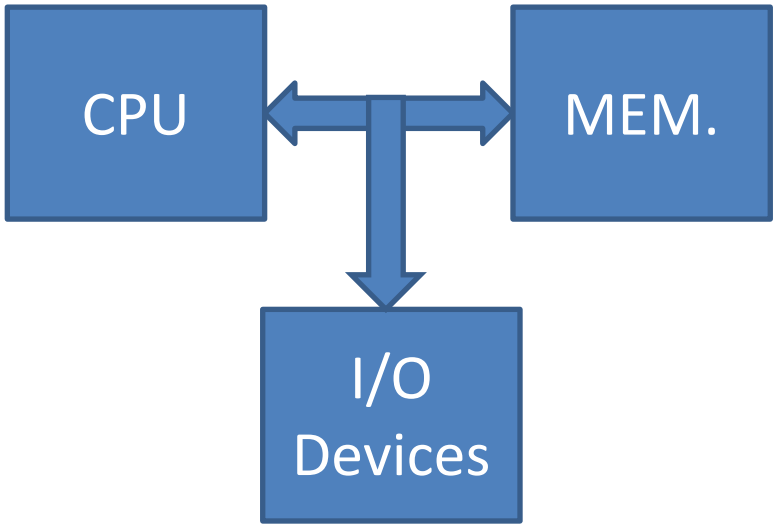
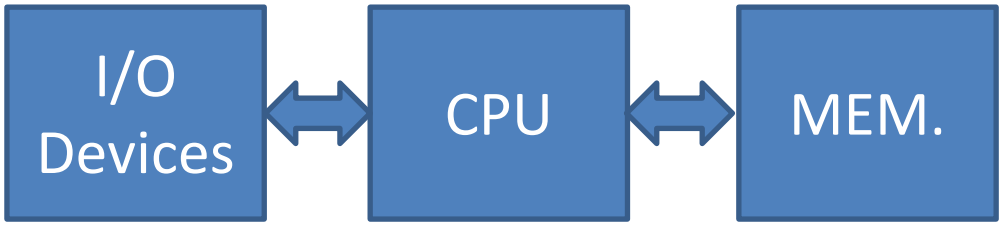
Memory-Mapped I/O vs. Port-Mapped I/O





Memory-mapped I/O	Port-mapped I/O
Mesmo Bus para Memoria e I/O Devices	Buses e conjuntos de endereço diferentes para acessar memória e I/O devices
Dispositivos de I/O são acessados por instruções regulares	Utiliza instruções especiais para acessar os dispositivos de I/O
Método mais utilizado	Processadores x86 Intel – instruções IN e OUT

Mapa da Memória do Cortex M0+

Memória do ARM é mapeada em 4 Gb
KL25Z

	Allocated size	Allocated address
Flash	128KB	0x00000000 to 0x0001FFFF
SRAM	16KB	0x1FFFF000 to 0x20002FFF
I/O	All the peripherals	0x400FF000 to 0x400FFFFF

Table 2-1: Memory Map in KL25Z128VLK4

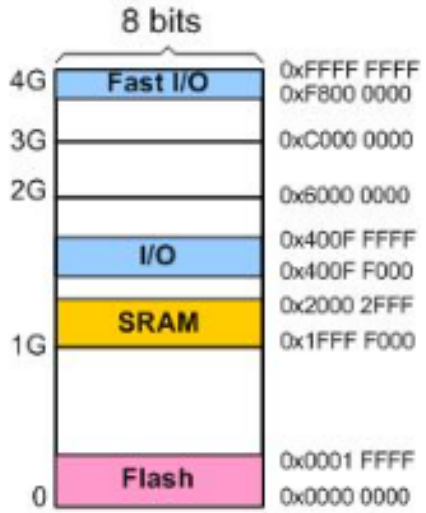


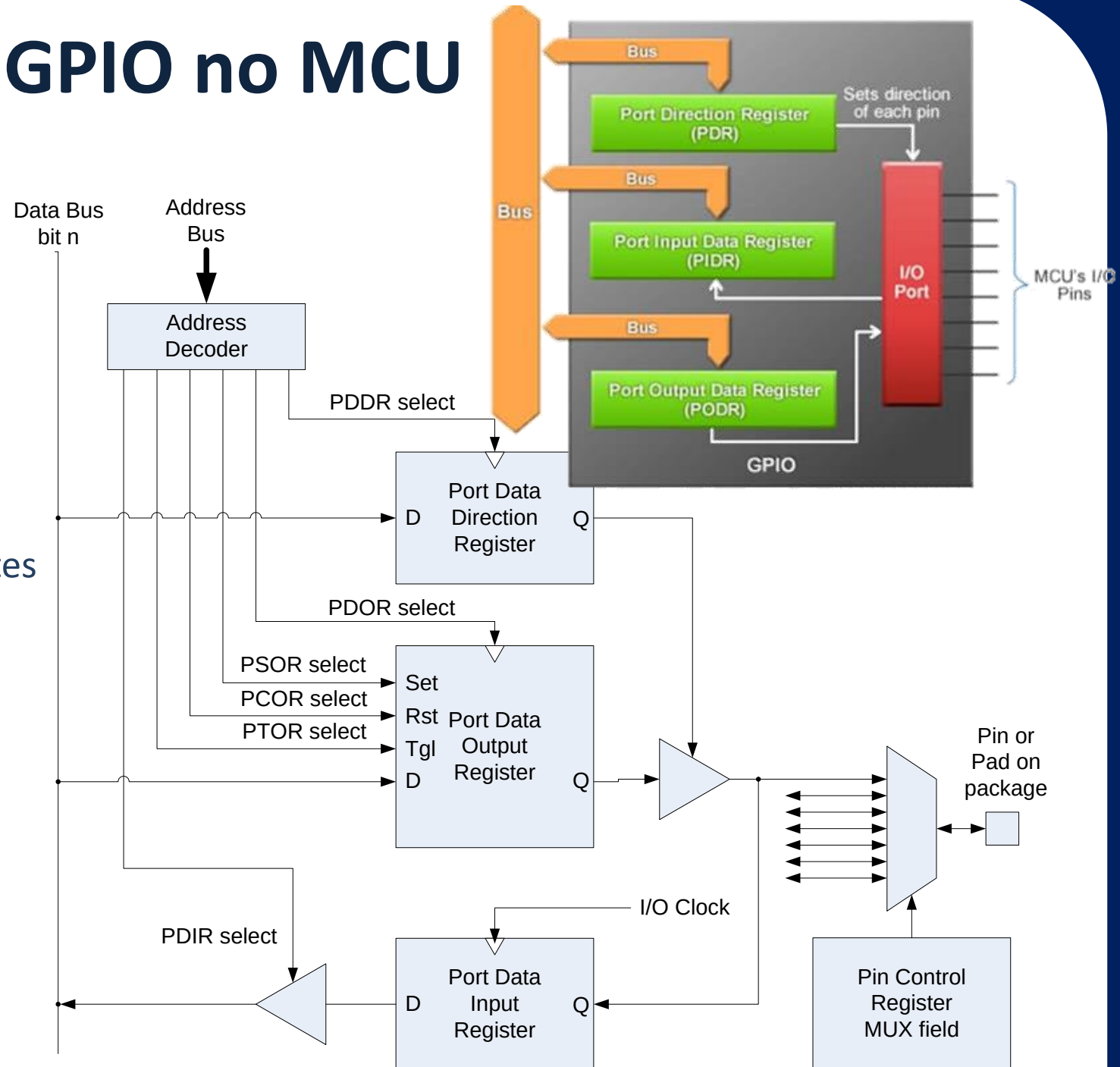
Figure 2-3: Memory Map

- Flash – Código do Programa e dados fixos como tabelas no ROM
- SRAM – variáveis
- Periféricos - endereços para registradores associados a I/Os, Timers, ADCs etc.

Olhar página 177 do KL25 Sub-Family Refernce Manual para definições do registrador

Circuito do GPIO no MCU

- Configuração
  - Direção
  - MUX
  - …
- Data
  - Output (diferentes possibilidades)
  - Input



General Purpose I/O (GPIO)

- 5 portas (A, B, C, D e E);
- 32 pinos por porta (PTA0 .. PTA31; PTB0 .. PTB21 etc.);
- Nem todos pinos são implementados;
- Chips da ARM têm dois barramentos: APB (Advanced Peripheral Bus) e o AHB (Advanced High-Performance Bus);
- AHB muito mais rápido que o APB.

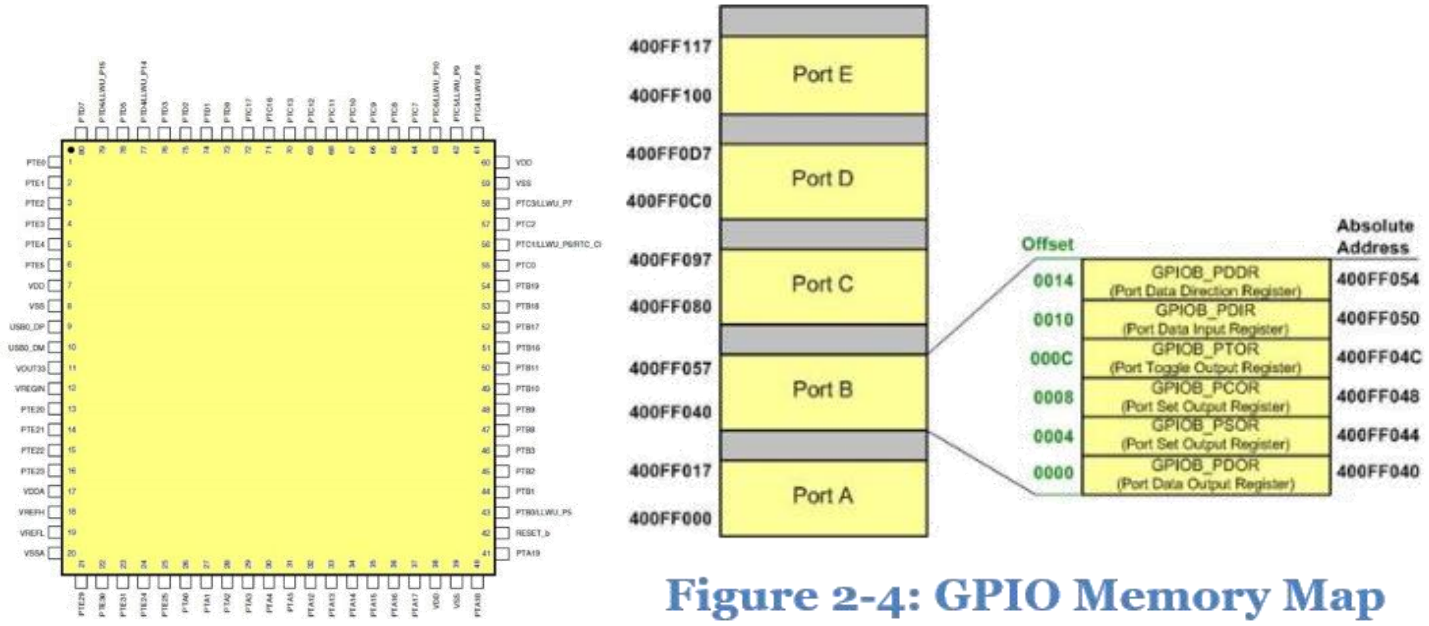


Figure 2-4: GPIO Memory Map

Endereçamento

- GPIO Port A (APB): 0x400F F000
- GPIO Port B (APB): 0x400F F040
- GPIO Port C (APB): 0x400F F080
- GPIO Port D (APB): 0x400F F0C0
- GPIO Port E (APB): 0x400F F100

- GPIO Port A (AHB): 0xF80F F000
- GPIO Port B (AHB): 0xF80F F040
- GPIO Port C (AHB): 0xF80F F080
- GPIO Port D (AHB): 0xF80F F0C0
- GPIO Port E (AHB): 0xF80F F100

Exemplo

- Configurar Pinos PTB18 e PTB19 para output:
  - GPIOB_PDDR=0x000C 0000 → 0b0000 0000 0000 1100 0000 0000 0000 0000

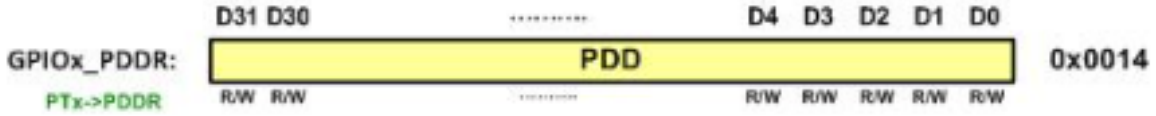


Figure 2-9: GPIOx_PDDR (Port Data Direction Register)

- Endereço do registrador GPIOB_PDDR:
  - Para Porta B = 0x4000 F040
  - Offset de 0x0014
  - Enderço do 0x4000 F054

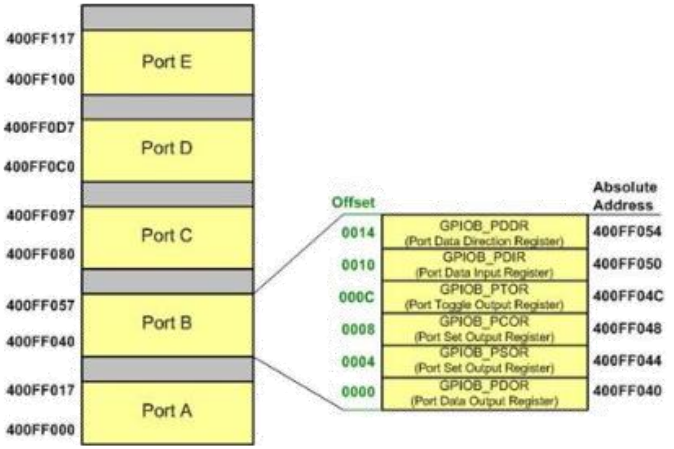


Figure 2-4: GPIO Memory Map

Registradores das Portas

- Direction Register (PDDR) – define se o pino é uma entrada ou saída;
- Data Registers – escreve (PDOR, PSOR, PCOR, PTOR) ou lê (PDIR).

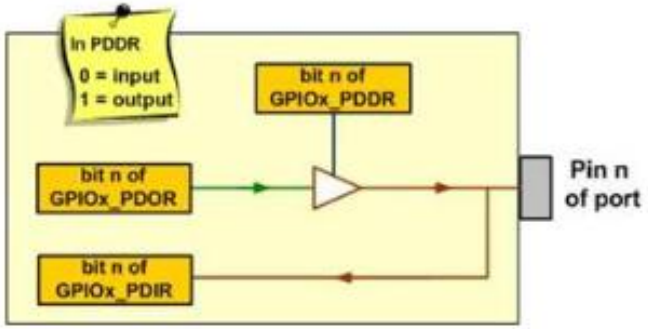


Figure 2-7: The Data and Direction Registers and a Simplified View of an I/O pin

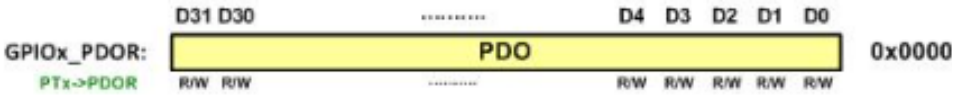


Figure 2-8: GPIOx_PDOR (Port Data Output Register)

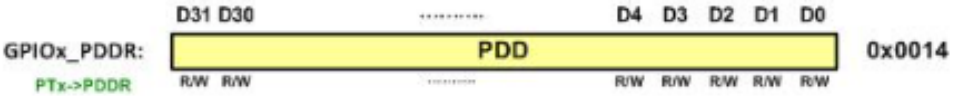


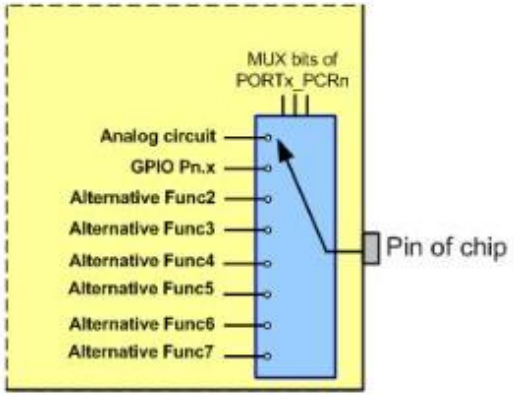
Figure 2-9: GPIOx_PDDR (Port Data Direction Register)

Address	Name	Description	Type	Reset Value
0x400FF000	GPIOA_PDOR	Port Data Output Register	R/W	0x00000000
0x400FF004	GPIOA_PSOR	Port Set Output register	W (always reads 0)	0x00000000
0x400FF008	GPIOA_PCOR	Port Clear Output Register	W (always reads 0)	0x00000000
0x400FF00C	GPIOA_PTOR	Port Toggle Output Register	W (always reads 0)	0x00000000
0x400FF010	GPIOA_PDIR	Port Data Input Register	R	0x00000000
0x400FF014	GPIOA_PDDR	Port Data Direction Register	R/W	0x00000000

Table 2-3: Some GPIO Registers for PORTA

Funções alternativas dos pinos

- Pin multiplexing
- Função controlado pelo PORTx_PCRn (Port x Pin n Control Register
- Bits mais importantes: D10-D8 (Mux Control)



Address: Base address + 0h offset + (4d × i), where i=0d to 31d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0							ISF	0				IRQC			
W								w1c								
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0					MUX			0	DSE	0	PFE	0	SRE	PE	PS
W																
Reset	0	0	0	0	0	x*	x*	x*	0	x*	0	x*	0	x*	x*	x*

* Notes:
- x = Undefined at reset.

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Figure 2-10: Alternative Functions of Pins

BIT	Field	Description
0	Pull Select (PS)	If the PE field is set, the field chooses between pull-up and pull-down resistors. 0: pull-down resistor, 1: pull-up resistor
1	Pull Enable (PE)	0: Disable the internal pull resistors 1: Enable the internal pull resistors
2	Slew Rate Enable (SRE)	0: Fast slew rate 1: Slow slew rate
4	Passive Filter Enable (PFE)	0: Passive input filter is disabled 1: Passive input filter is enabled
6	Drive Strength Enable (DSE)	0: Low drive strength 1: High drive strength
10-8	Pin Mux Control (MUX)	

Pin Mux Control

000	Pin disabled (analog).
001	Alternative 1 (GPIO).
010	Alternative 2 (chip-specific).
011	Alternative 3 (chip-specific).
100	Alternative 4 (chip-specific).
101	Alternative 5 (chip-specific).
110	Alternative 6 (chip-specific).
111	Alternative 7 (chip-specific).

Exemplo

- Configurar Pino PTB18 com slow slew rate, high drive e sem pull-up:
  - Registrado PORTB_PCR18:
  - 0b0000 0000 0000 0000 0000 0001 0100 0100
  - 0x0000 0144
- Endereço:
  - PORTB PCR18 = 4004 A048

BIT	Field	Description
0	Pull Select (PS)	If the PE field is set, the field chooses between pull-up and pull-down resistors. 0: pull-down resistor, 1: pull-up resistor
1	Pull Enable (PE)	0: Disable the internal pull resistors 1: Enable the internal pull resistors
2	Slew Rate Enable (SRE)	0: Fast slew rate 1: Slow slew rate
4	Passive Filter Enable (PFE)	0: Passive input filter is disabled 1: Passive input filter is enabled
6	Drive Strength Enable (DSE)	0: Low drive strength 1: High drive strength
10-8	Pin Mux Control (MUX)	

Address: Base address + 0h offset + (4d × i), where i=0d to 31d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0							ISF	0				IRQC			
W								w1c								
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0					MUX			0	DSE	0	PFE	0	SRE	PE	PS
W																
Reset	0	0	0	0	0	x*	x*	x*	0	x*	0	x*	0	x*	x*	x*

Notes:
x = Undefined at reset.

Olhar página 177do KL25 Sub-Family Refernce Manual para definições do registrador

Port Control - Sub-Family Refence Manual (p. 101)

Table 3-49. Ports Summary

Feature	Port A	Port B	Port C	Port D	Port E
Pull Select control	No	No	No	No	No
Pull Select at reset	PTA0=Pull down, Others=Pull up	Pull up	Pull up	Pull up	Pull up
Pull Enable control	Yes	Yes	Yes	Yes	Yes
Pull Enable at reset	PTA0/PTA3/PTA4/ RESET_b=Enabled ; Others=Disabled	Disabled	Disabled	Disabled	Disabled
Slew Rate Enable control	No	No	No	No	No
Slew Rate Enable at reset	PTA3/PTA14/ PTA15/PTA16/ PTA17=Disabled; Others=Enabled	PTB10/PTB11/ PTB16/PTB17 = Disabled; Others=Enabled	PTC3/PTC4/PTC5/ PTC6/ PTC7=Disabled; Others=Enabled	PTD4/PTD5/PTD6/ PTD7=Disabled; Others=Enabled	PTE16/PTE17/ PTE18/ PTE19=Disabled; Others=Enabled
Passive Filter Enable control	PTA4 and RESET_b only	No	No	No	No
Passive Filter Enable at reset	RESET_b=Enabled ; Others=Disabled	Disabled	Disabled	Disabled	Disabled
Open Drain Enable control[1]	No	No	No	No	No
Open Drain Enable at reset	Disabled	Disabled	Disabled	Disabled	Disabled
Drive Strength Enable control	No	PTB0/PTB1 only	No	PTD6/PTD7 only	No
Drive Strength Enable at reset	Disabled	Disabled	Disabled	Disabled	Disabled
Pin Mux control	Yes	Yes	Yes	Yes	Yes
Pin Mux at reset	PTA0/PTA3/ PTA4=ALT7; Others=ALT0	ALT0	ALT0	ALT0	ALT0
Lock Bit	No	No	No	No	No
Interrupt and DMA Request	Yes	No	No	Yes	No
Digital Glitch Filter	No	No	No	No	No

Clock para GPIO

- O clock deve ser habilitado antes de configurar a porta;
- Registrador SIM_SCGC5 habilita o clock para todas as portas;
- Para economizar energia o clock das portas que não são utilizadas não devem ser habilitado;
- Endereço do SIM_SCGC5:
  - 0x4004 7000 + 0x1038= 0x4004 8038

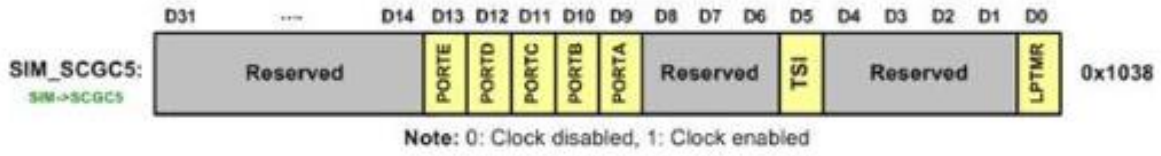

Figure 2-13: SIM_SCGC5 (System Clock Gating Control Register 5) Register

Exemplo

- Habilitar clock somente para porta B:
  - SIM_SCGC5 = 0b0000 0000 0000 0000 0000 0100 0000 0000
  - SIM_SCGC5 = 0x0000 0400
  - SIM_SCGC5 |= 0x0400 (OR binário - *bitwise*)
    - SIM_SCGC5 = SIM+SCGC5 | 0x0400 (seta somente o bit de interesse)

- Operações Booleanas Binárias:
  - OR | 0x04 | 0x68 = 0x6C
  - AND & 0x35 & 0x0F = 0x05
  - XOR ^ 0x54 | 0x78 = 0x2C
  - Invert ~ ~0x55 = 0xAA
  - Shift << ou >>

    0b0001 0000 >> 3 = 0b0000 0010

    1<< 3 = 0b0000 1000

Qualquer número | 1 = 1
Qualquer número | 0 = sem mudança

Qualquer número & 1 = sem mudança
Qualquer número & 0 = 0

Referência

- Freescale ARM Cortex-M Embedded - Muhammad Ali Mazidi
- Muhammad Ali Mazidi, Sarmad Naimi, Sepehr Naimi, Janice Mazidi-ARM Assembly Language_ Programming and Architecture (2013)