HARDWARE

PCS3100 – INTRODUÇÃO À ENGENHARIA DE COMPUTAÇÃO

PROF. DR. BRUNO DE CARVALHO ALBERTINI

ABR/2023

O QUE É HARDWARE?

O QUE É HARDWARE?

- O que é um SOFTWARE?
  - O SW existe sem um processador?
  - O que acontece se há um problema no SW?
- O que é um HARDWARE?
  - A parte física da computação: portas lógicas, circuitos integrados, processadores, etc.


Desligar
Você não tem permissão para desligar o computador.
OK
EU:

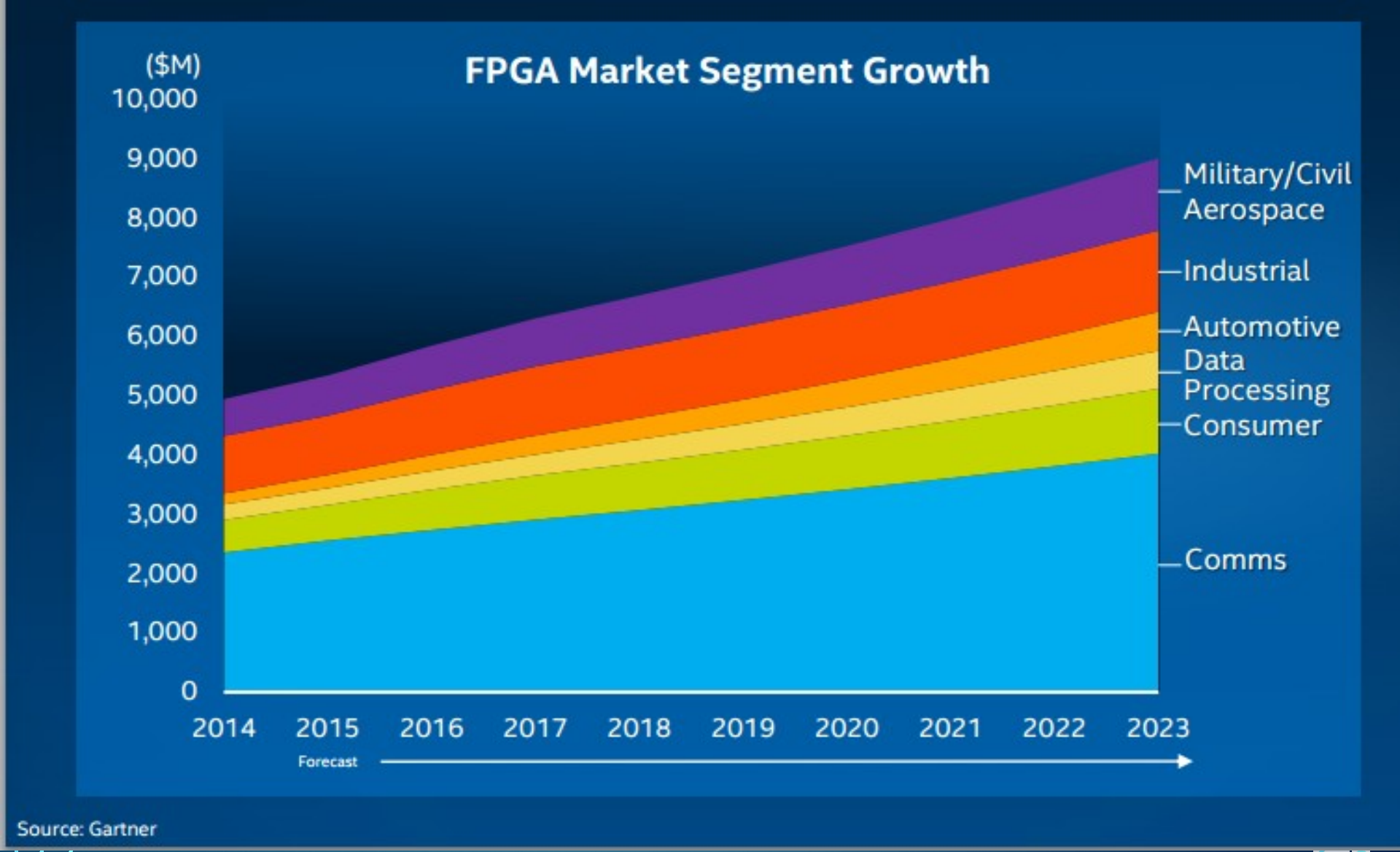
9/9

0800 Arctan started { 1.2700 9.037 847 025
1000 " stopped - arctan ✓ 9.037 846 995 correct
13" sc (032) MP - MC ~~1.9826447000~~ ~~2.13047647 15 (-3)~~ 4.615925059(-2)
(033) PRO 2 2.13047 6415
correct 2.13067 6415
Relays 6-2 in 033 failed special speed test
In relay " 10,000 test.
Relays changed
1100 Started Cosine Tape (Sine check)
1525 Started Mult + Adder Test.

1545

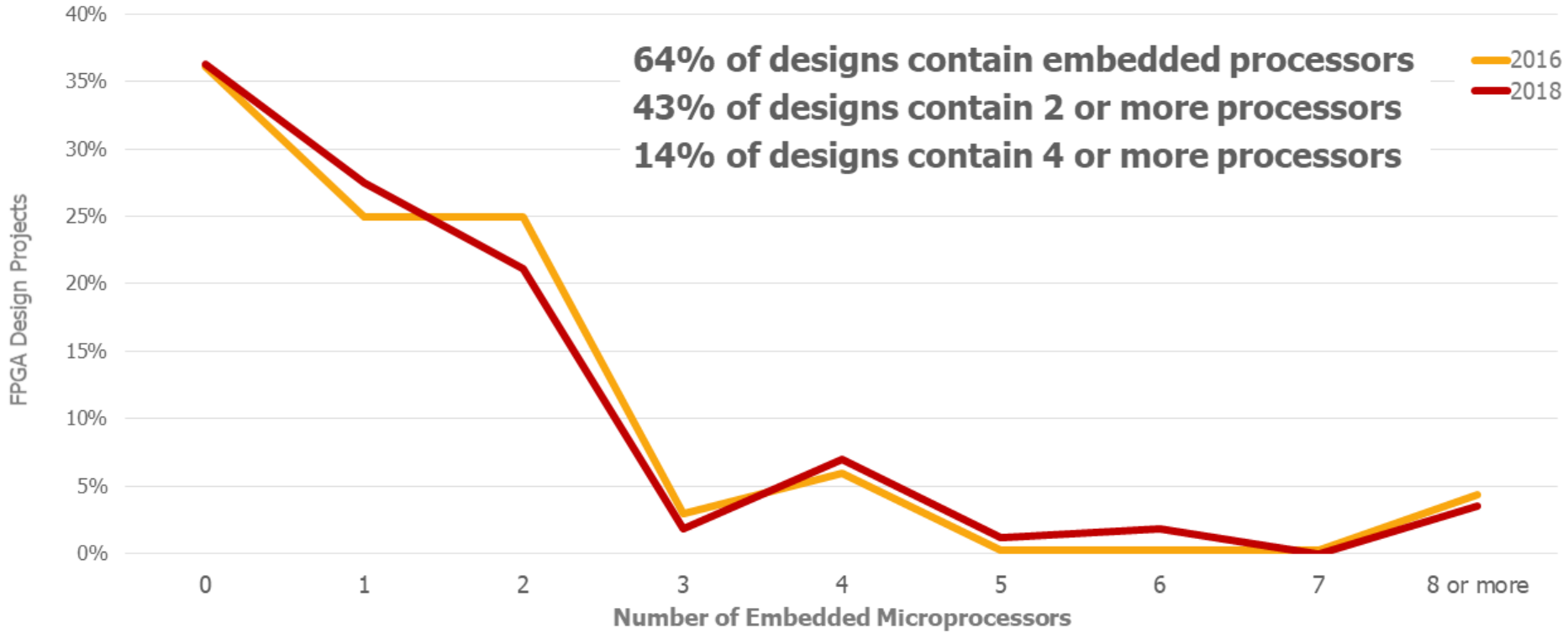
Relay #70 Panel F
(moth) in relay.
First actual case of bug being found.

~~1645~~ 1630 Arctangent started.
1700 closed down.



PROTÓTIPO COM FPGA?

FPGA: Number of Embedded Microprocessors



Source: Wilson Research Group and Mentor, A Siemens Business, 2018 Functional Verification Study

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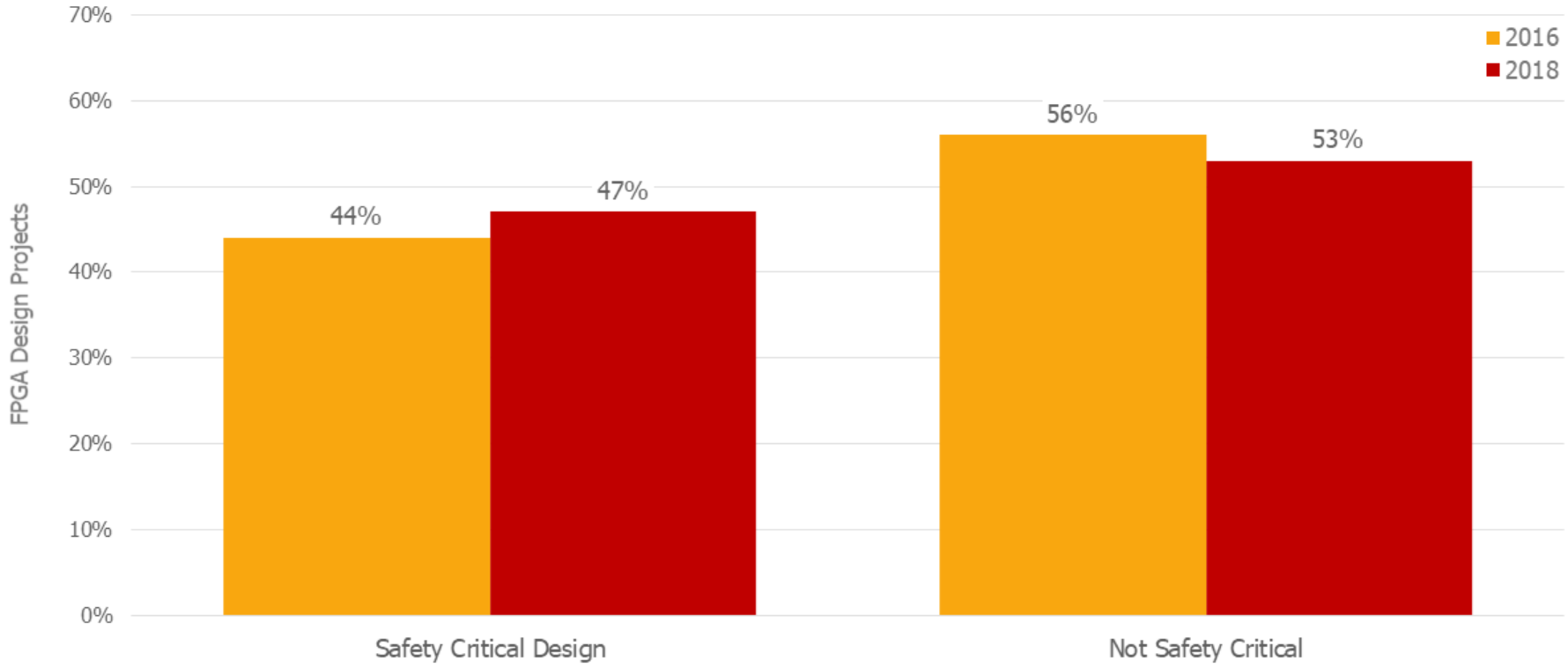
A Siemens Business

PROCESSADORES ESTÃO VIRANDO MODA!

FPGA: Projects Working on Safety Critical Design



Source: Wilson Research Group and Mentor, A Siemens Business, 2018 Functional Verification Study

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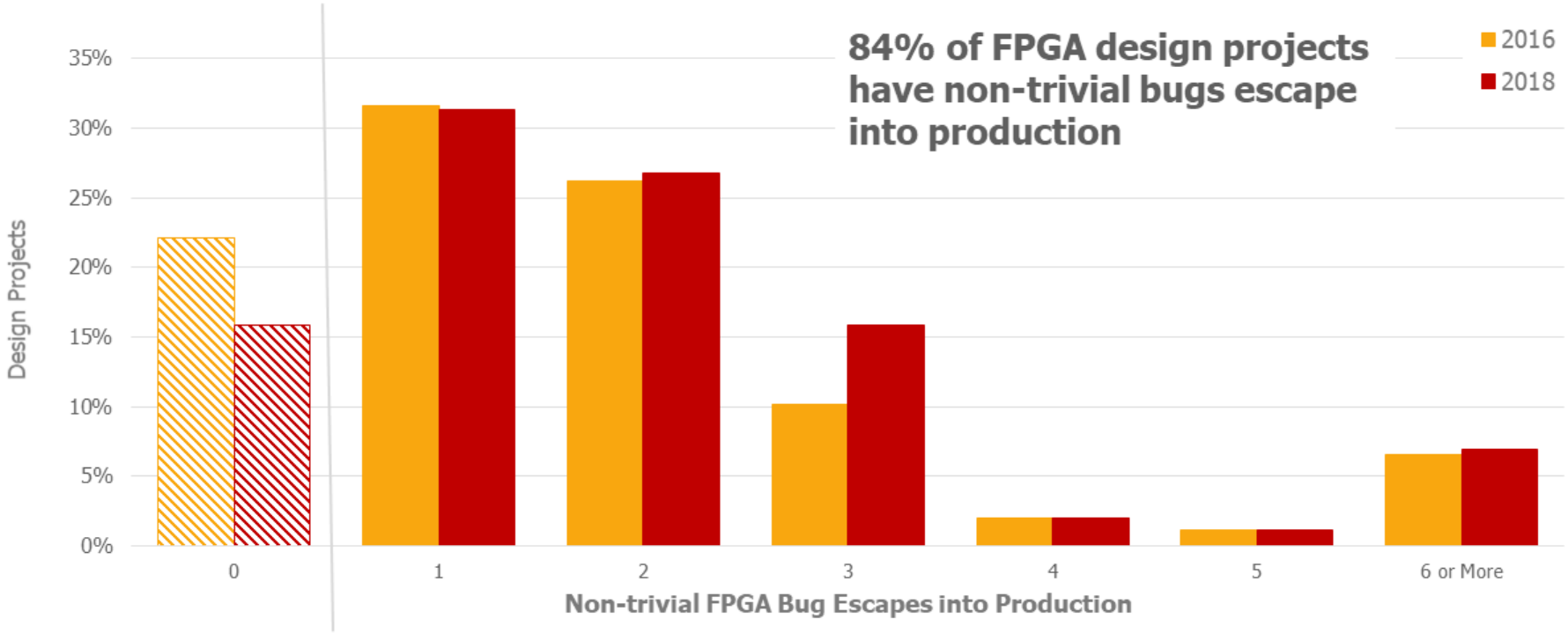
SISTEMAS CRÍTICOS ESTÃO CRESCENDO

FPGA: Non-trivial Bug Escapes into Production



Source: Wilson Research Group and Mentor, A Siemens Business, 2018 Functional Verification Study

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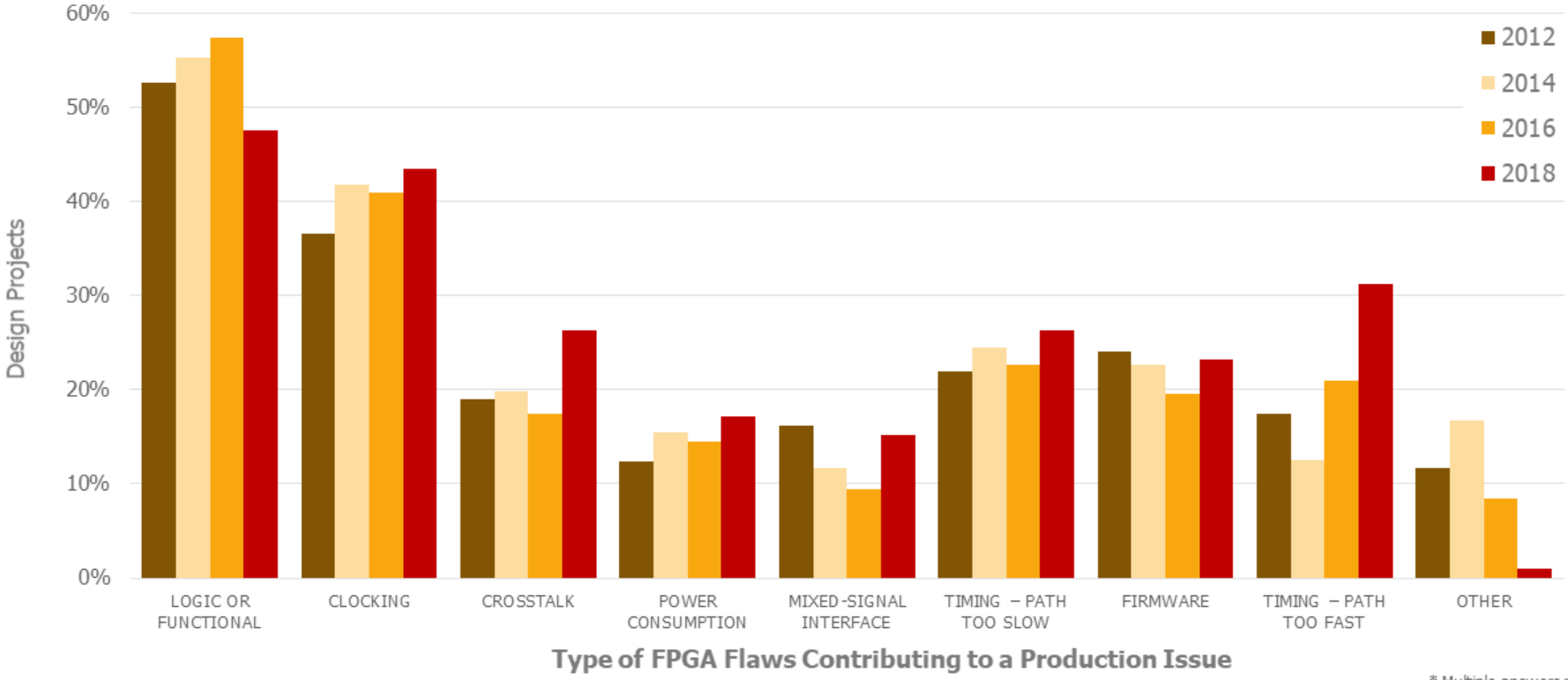
BUGS AINDA ESCAPAM (COMPARE COM SW :)

FPGA: Type of Flaws Contributing to a Production Issue



* Multiple answers possible

Source: Wilson Research Group and Mentor, A Siemens Business, 2018 Functional Verification Study

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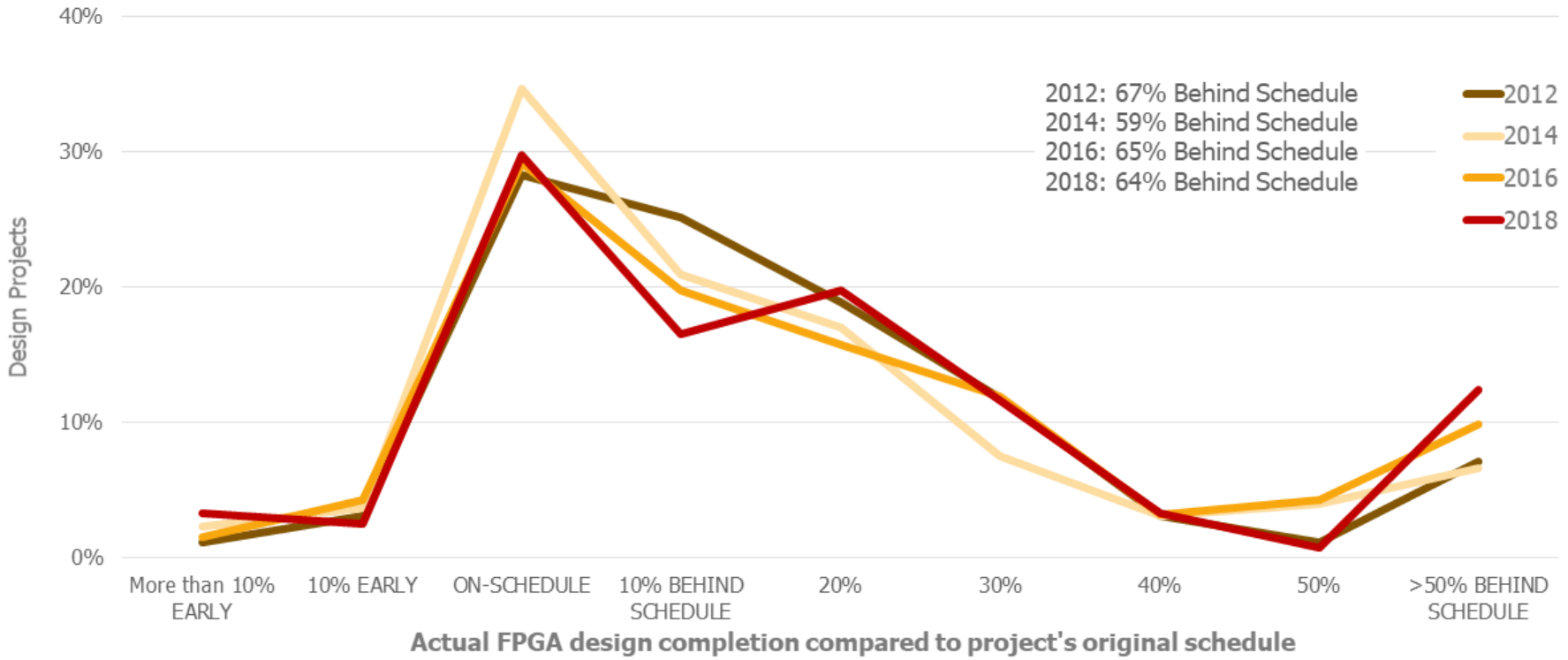
QUAIS BUGS ESCAPAM?

FPGA: Completion to Project's Original Schedule



Source: Wilson Research Group and Mentor, A Siemens Business, 2018 Functional Verification Study

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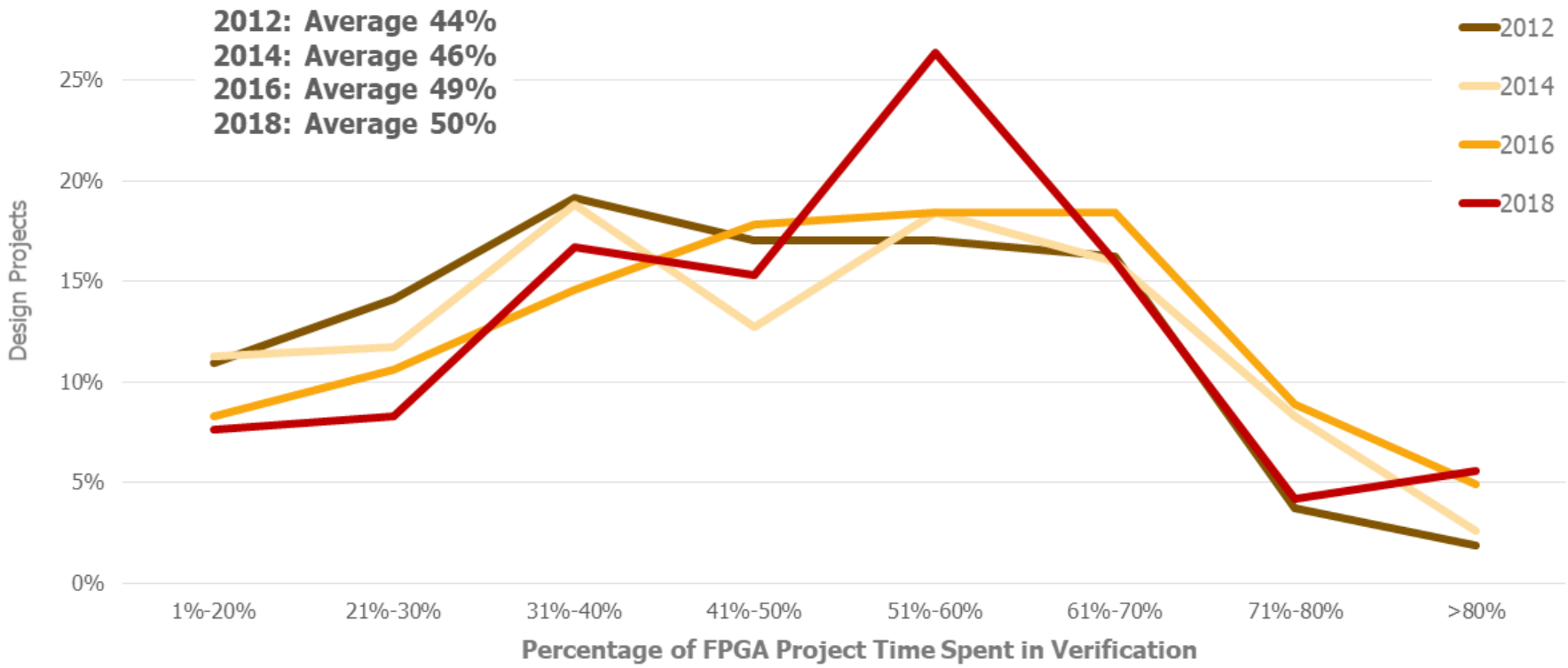
ISSO ATRASA O PROJETO?

FPGA: Percentage of Project Time Spent in Verification



Source: Wilson Research Group and Mentor, A Siemens Business, 2018 Functional Verification Study

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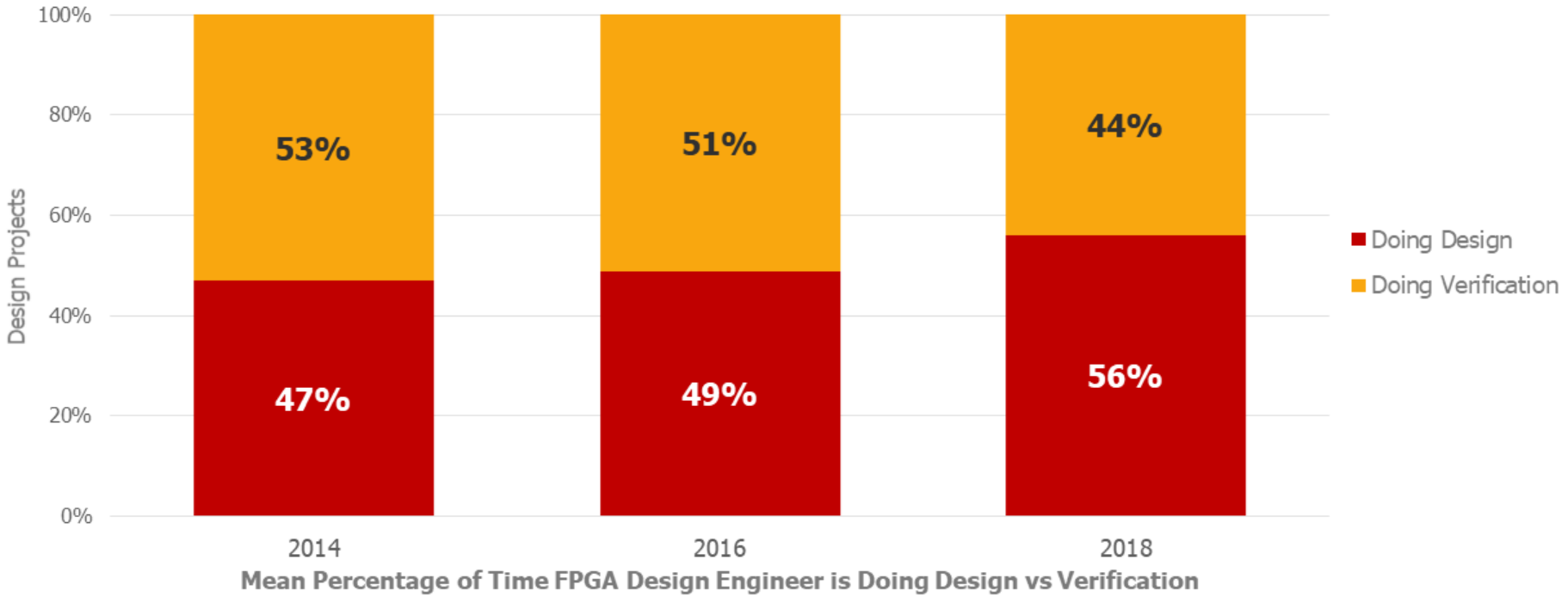
QUANTO TEMPO GASTAMOS TESTANDO?

FPGA: Mean % Time Design Engineer is Doing Design vs Verification



Source: Wilson Research Group and Mentor, A Siemens Business, 2018 Functional Verification Study

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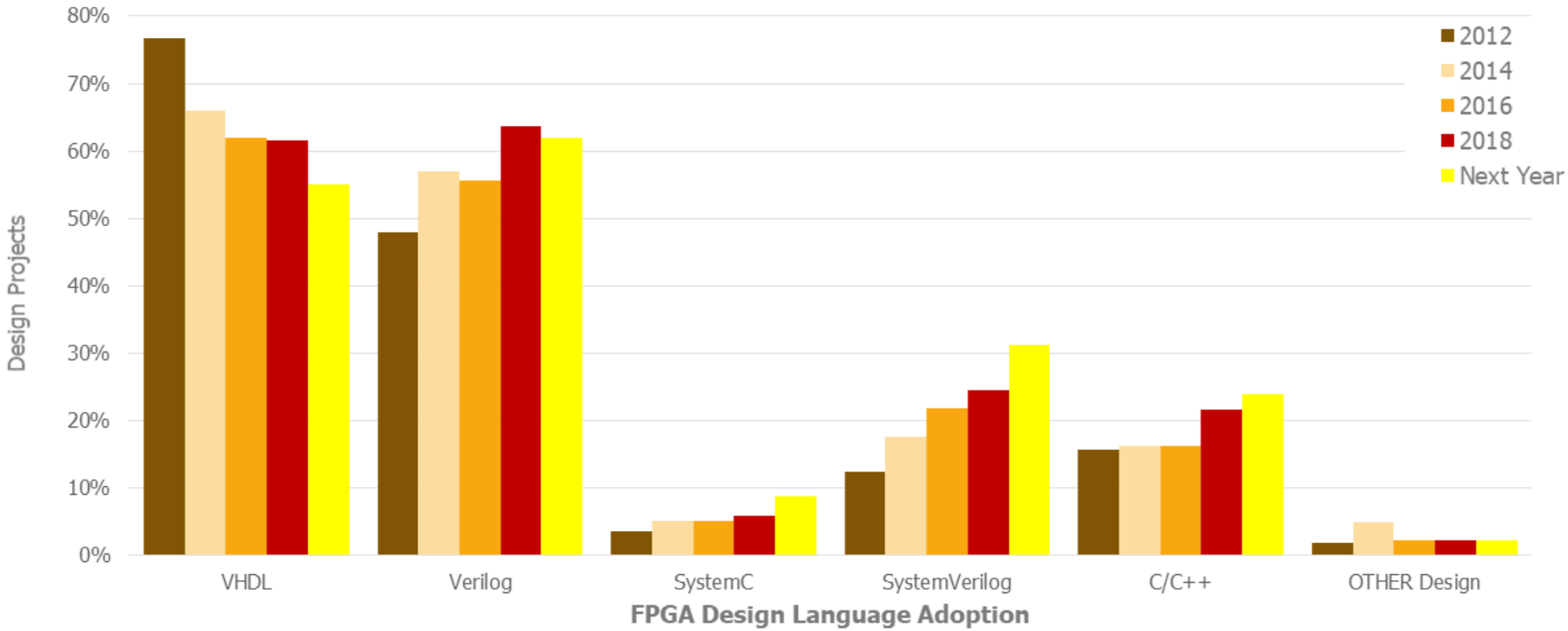
COMPARAÇÃO DEV-DEBUG

FPGA: Design Language Adoption Next Twelve Months



* Multiple answers possible

Source: Wilson Research Group and Mentor, A Siemens Business, 2018 Functional Verification Study

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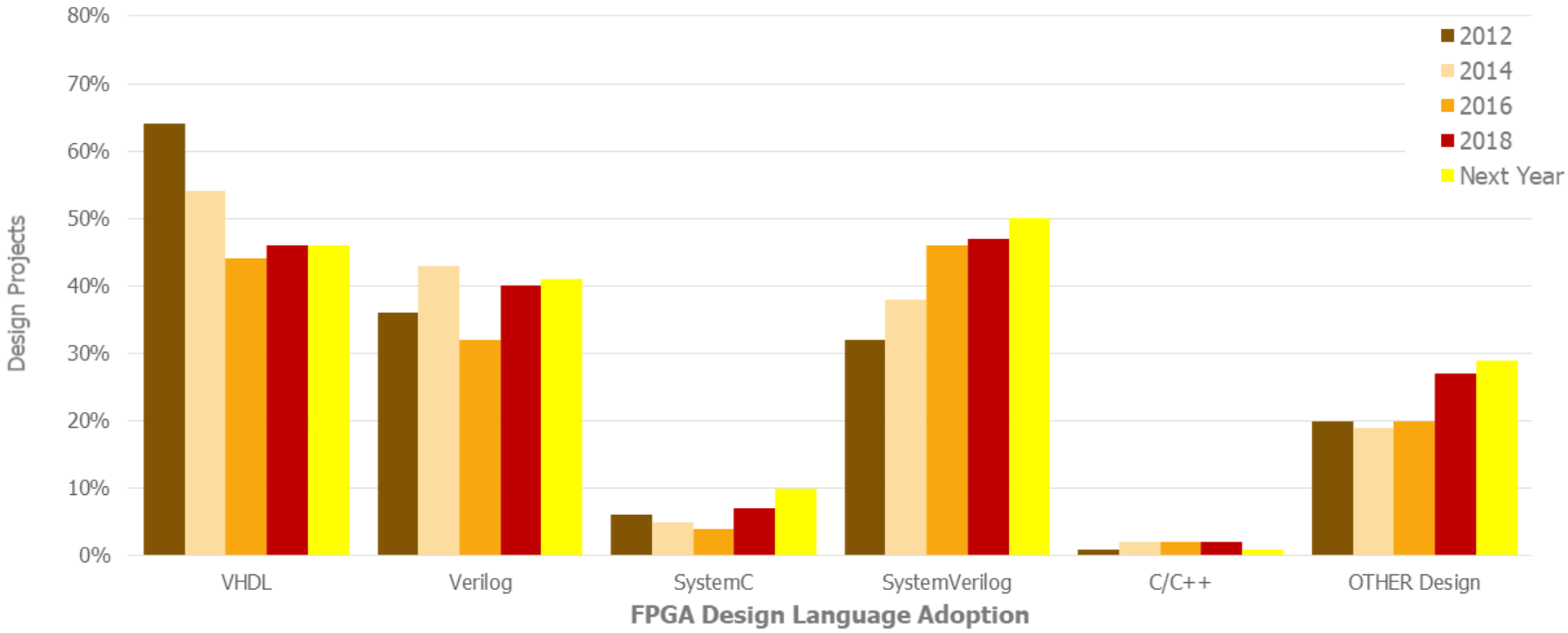
TENDÊNCIAS DE LINGUAGENS (DEV)

FPGA: Verification Language Adoption



* Multiple answers possible

Source: Wilson Research Group and Mentor, A Siemens Business, 2018 Functional Verification Study

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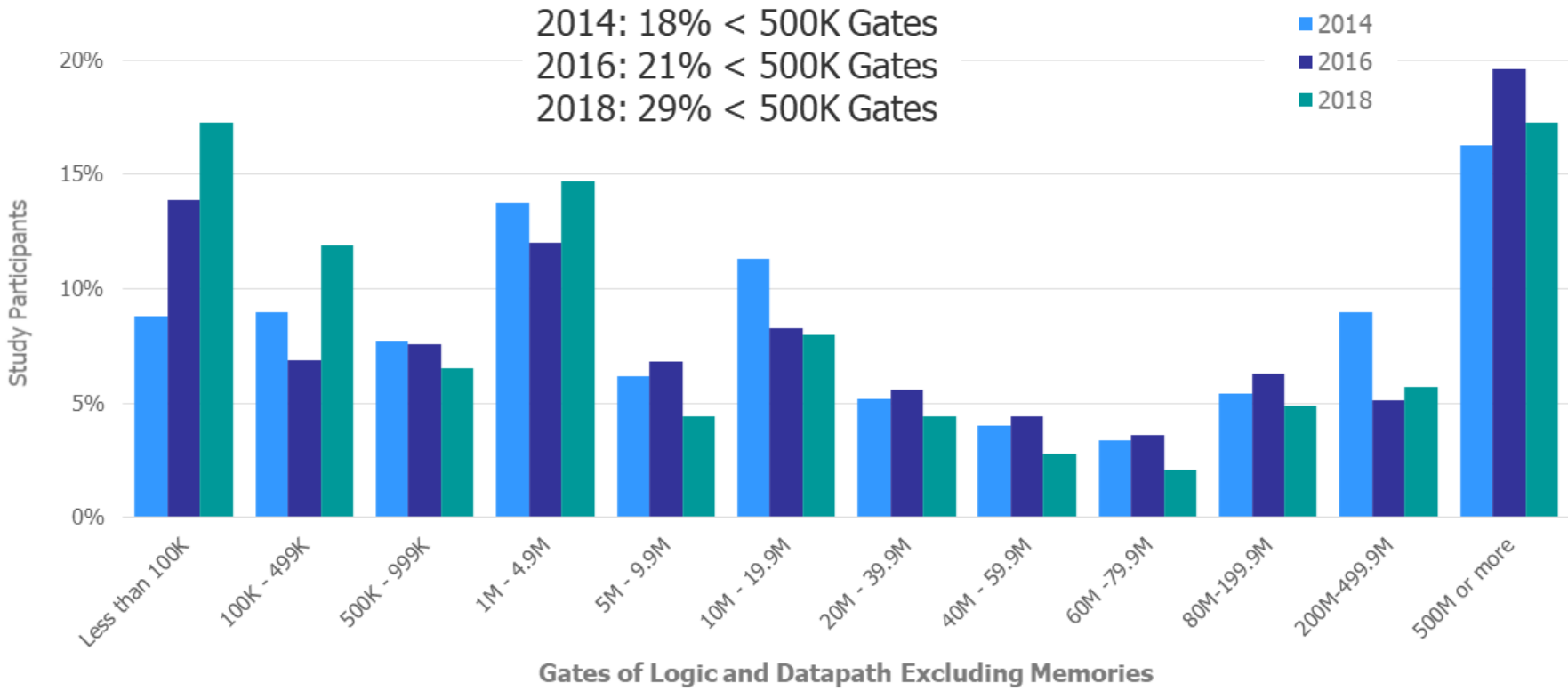
TENDÊNCIAS DE LINGUAGENS (DEBUG)

ASIC Study Participation by Gate Count (Design Size)



Source: Wilson Research Group and Mentor, A Siemens Business, 2018 Functional Verification Study

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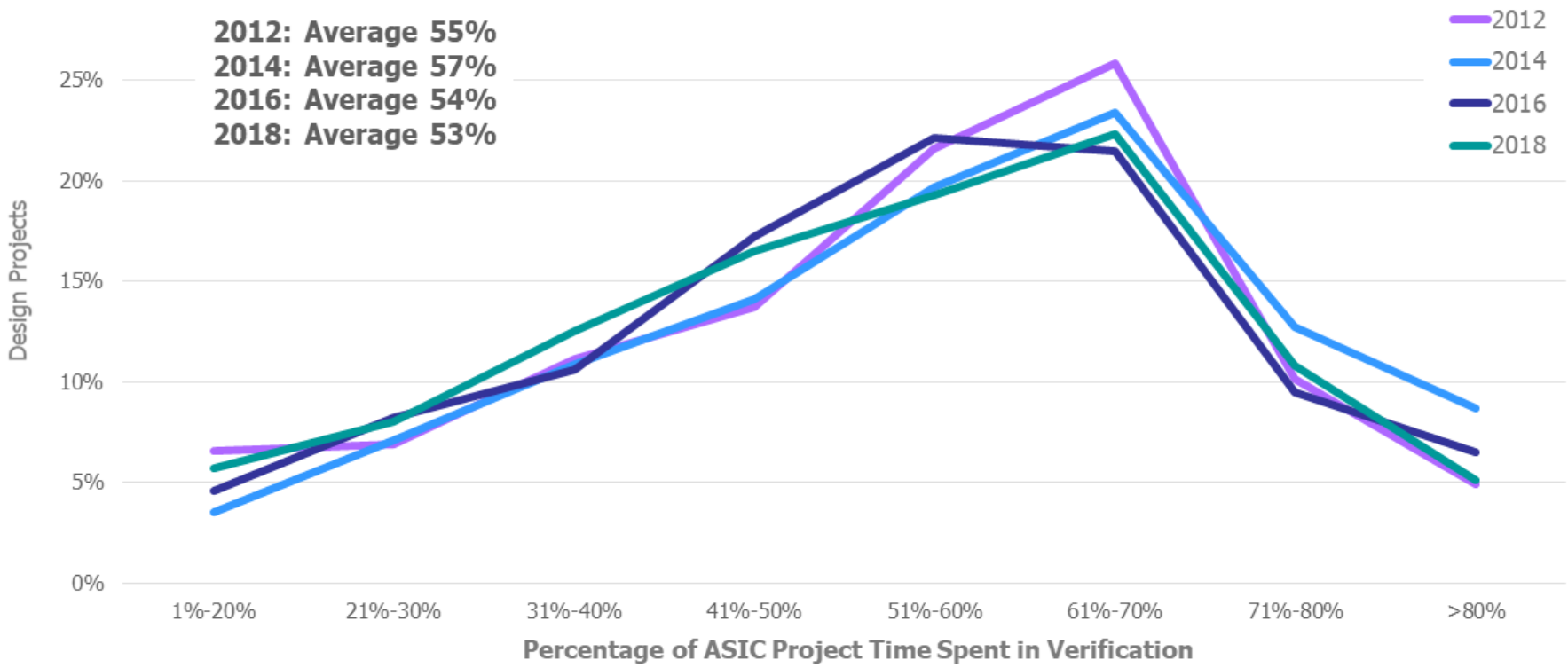
TAMANHO DOS ASICS

ASIC: Percentage of Project Time Spent in Verification



Source: Wilson Research Group and Mentor, A Siemens Business, 2018 Functional Verification Study

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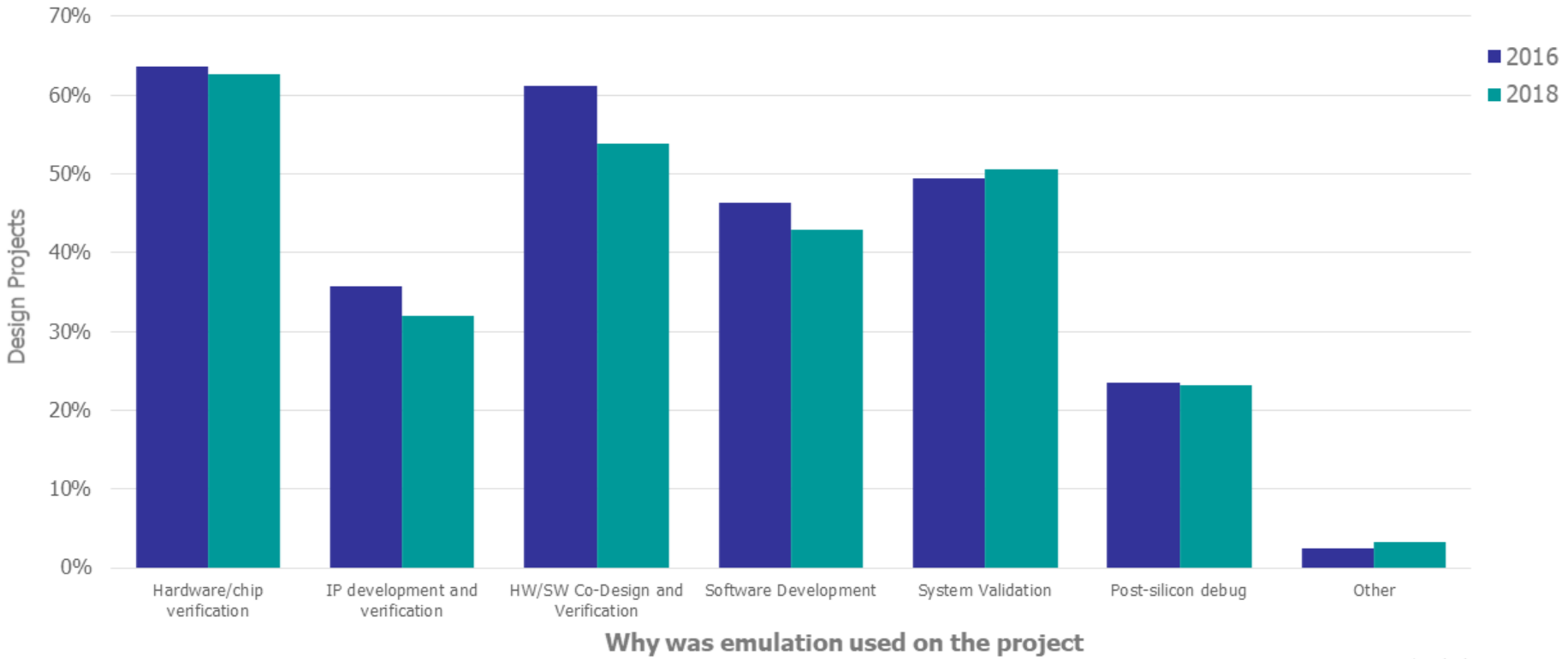
VERIFICAÇÃO NOS ASICS

Why was emulation used on the project



* Multiple answers possible

Source: Wilson Research Group and Mentor, A Siemens Business, 2018 Functional Verification Study

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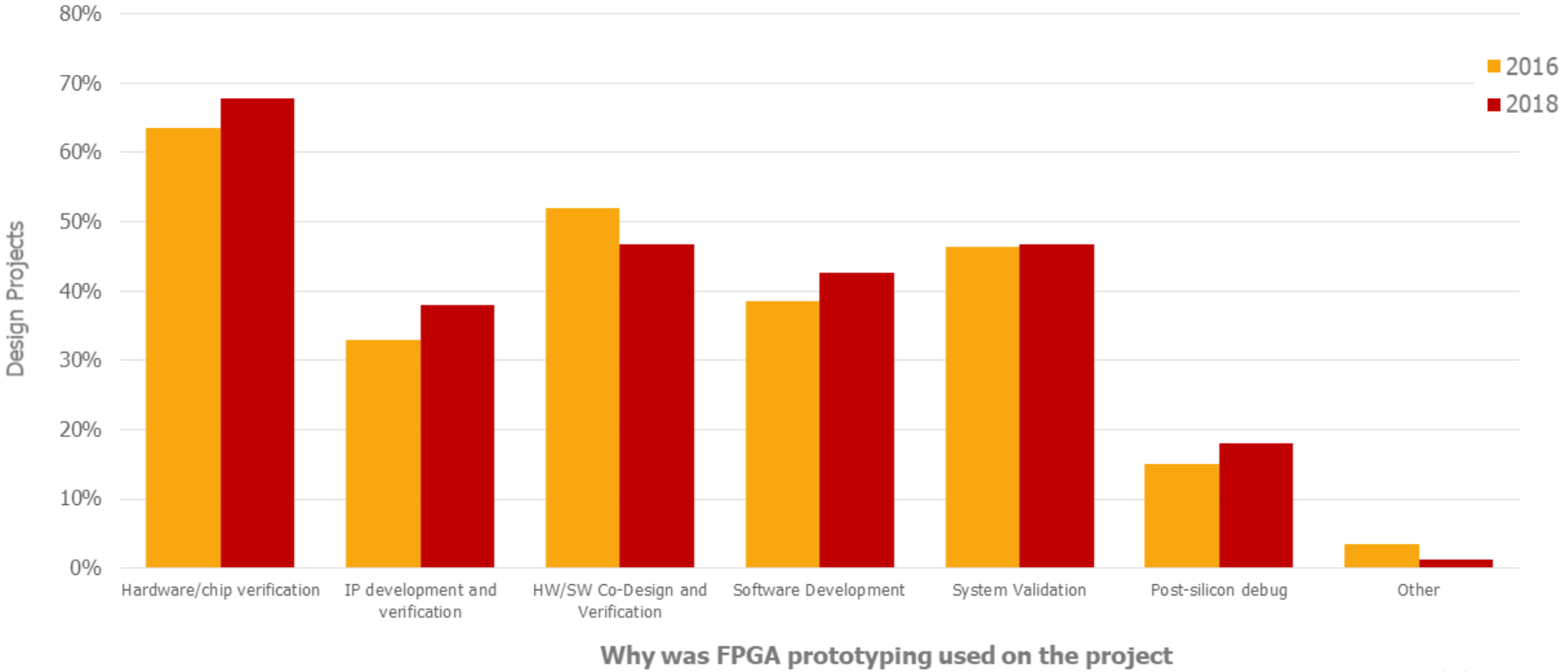
EMULAÇÃO

Why was FPGA prototyping used on the project



* Multiple answers possible

Source: Wilson Research Group and Mentor, A Siemens Business, 2018 Functional Verification Study

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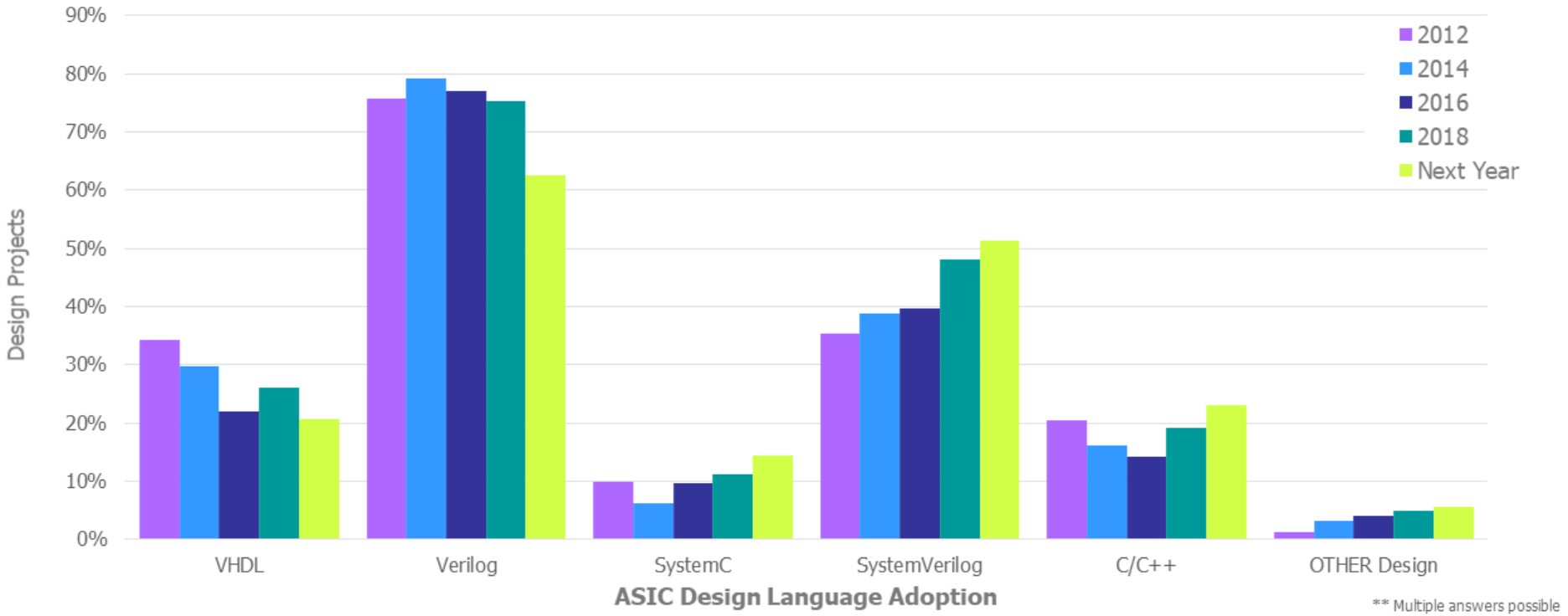
PROTÓTIPO EM FPGA

ASIC: Design Language Adoption Next Twelve Months



** Multiple answers possible

Source: Wilson Research Group and Mentor, A Siemens Business, 2018 Functional Verification Study

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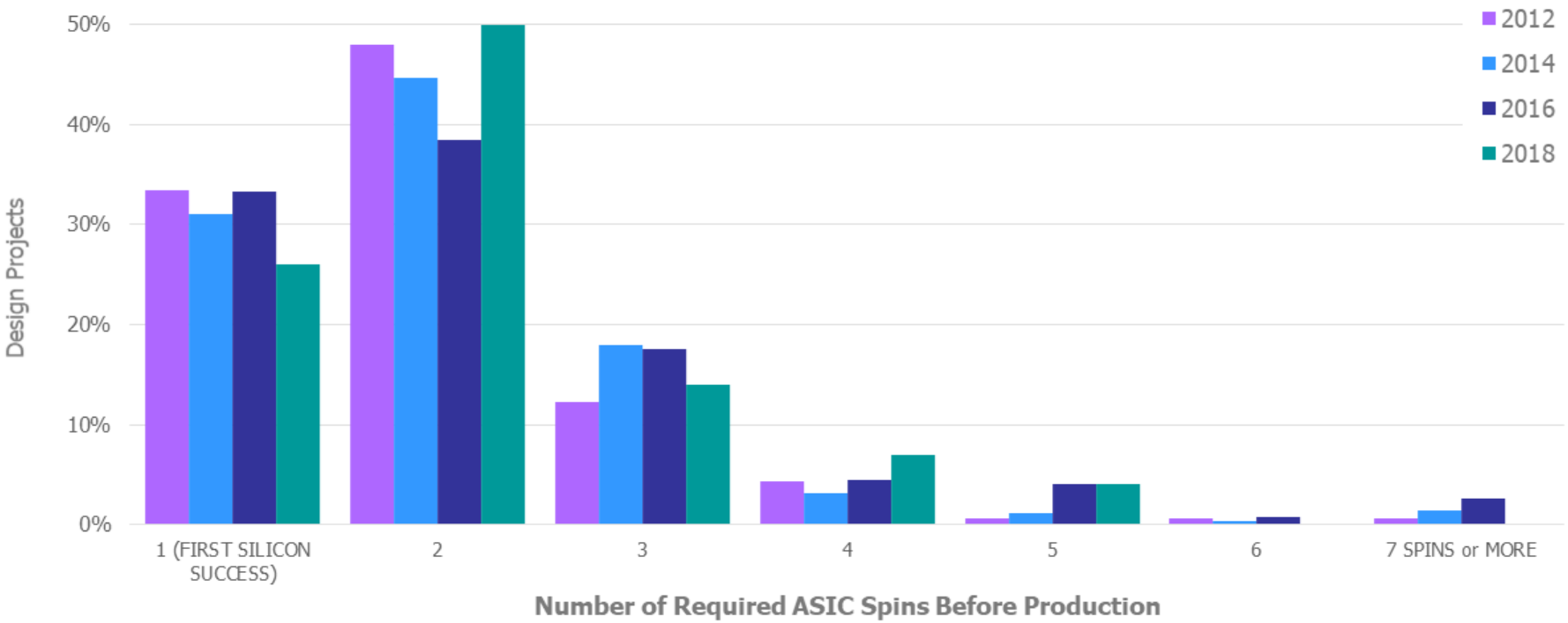
LINGUAGEM USADA EM ASICS

ASIC: Number of Required Spins Before Production



Source: Wilson Research Group and Mentor, A Siemens Business, 2018 Functional Verification Study

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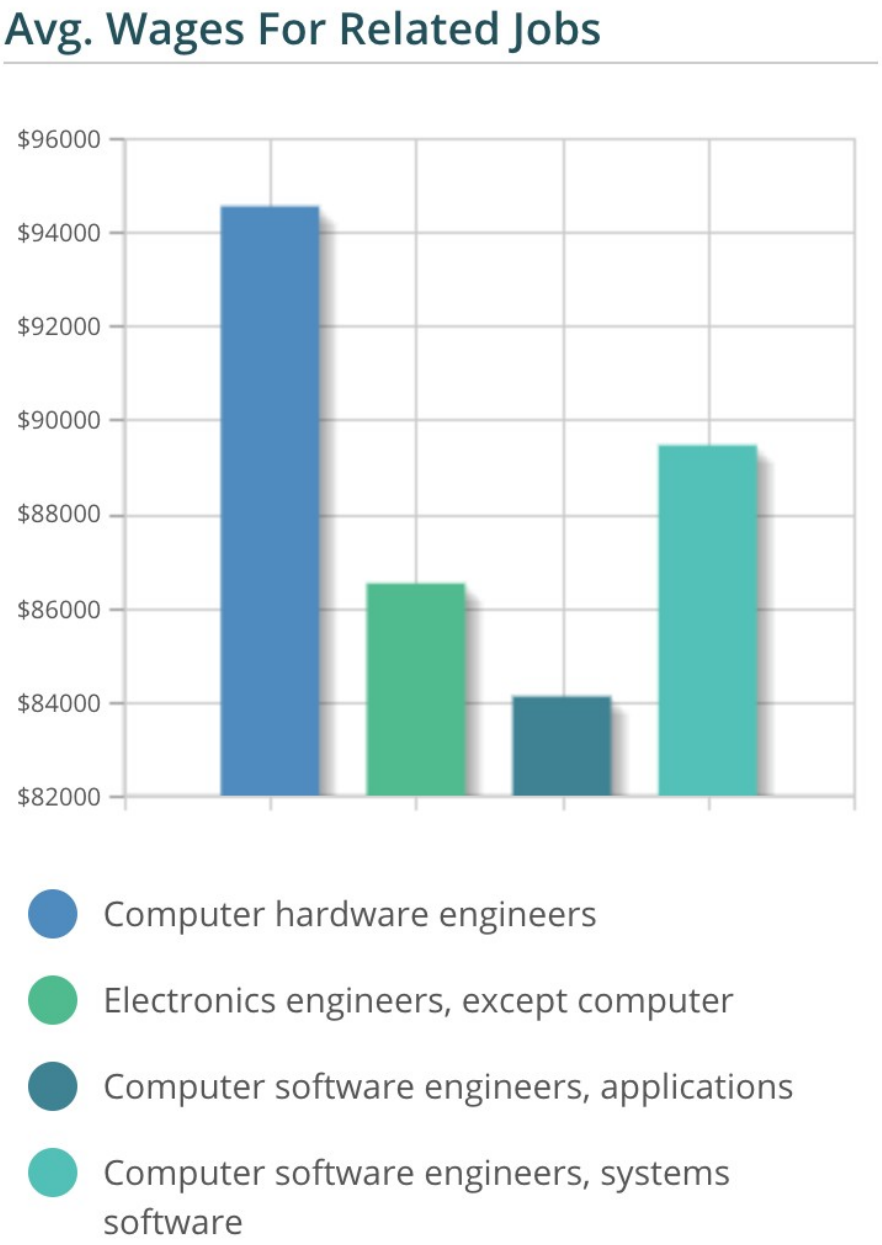
NÚMERO DE INTERAÇÕES

PORQUE SE TORNAR UM ENG. DE HARDWARE?

- HW está crescendo:
  - Low-power
  - Massive Computing
- HW é engenharia:
  - Problemas são físicos e não abstratos
  - Criatividade

CARREIRA EM HW

Dados de 2011/2022

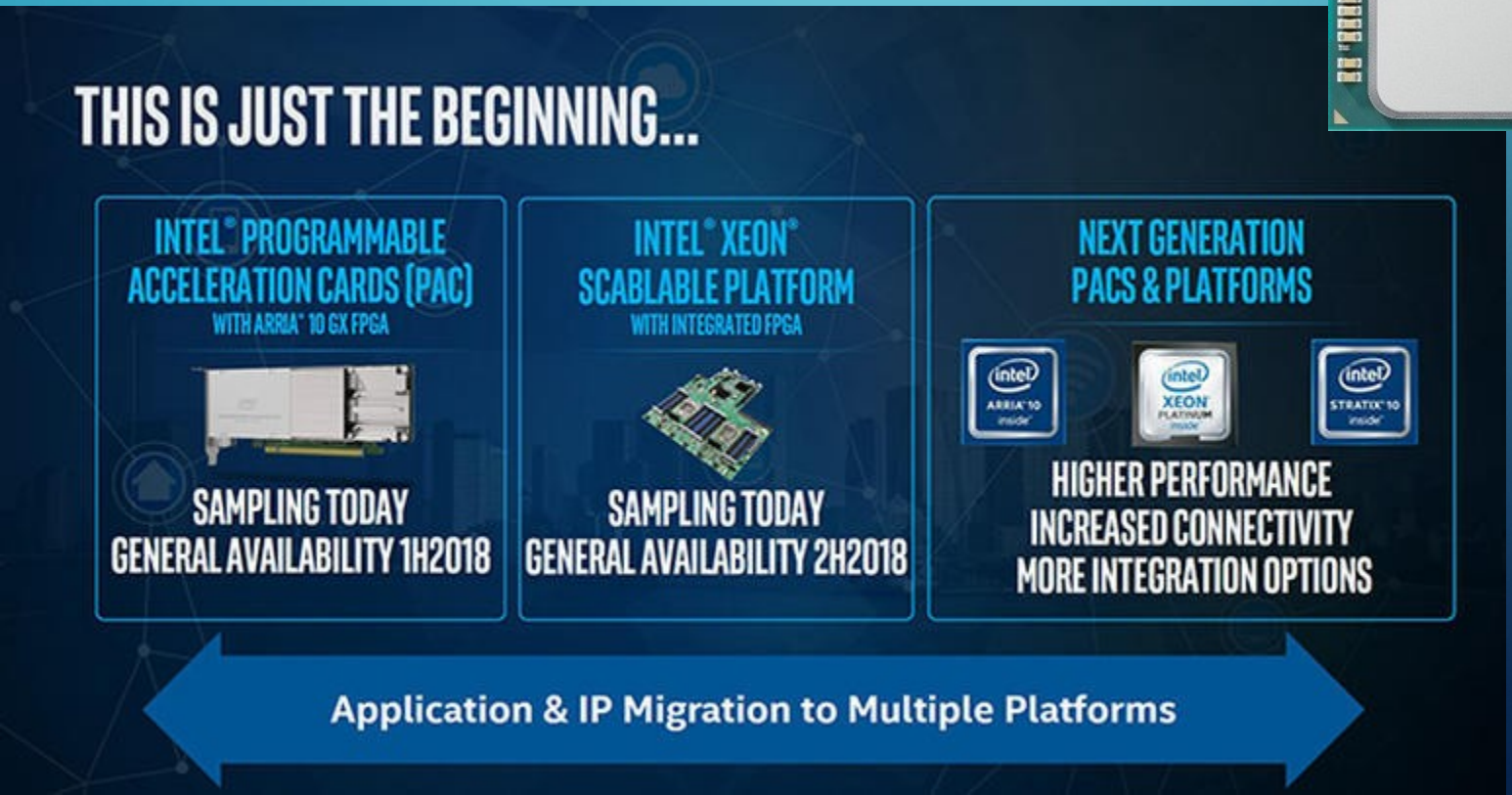


PORQUE SE TORNAR UM ENG. DE HARDWARE?

- Sistemas Embarcados
  - Onda “maker”
  - IoT
  - Conectividade (5G/smart-<coloqueaqui>)
- IA e Data Analytics
  - Até 2025, 50% dos datacenters terão algum tipo de FPGA (Intel)

PROCESSADOR DA INTEL

https://www.nextplatform.com/2018/05/24/a-peek-inside-that-intel-xeon-fpga-hybrid-chip/



COMO SE TORNAR UM ENG. DE HW?

- Engenharia Elétrica
  - Ir para PSI (silício) ou PCS (digitais)
- Engenharia de Computação
  - Sistemas Digitais
  - Arquiteturas de Computadores
  - Sistemas Embarcados

O QUE FAZ UM ENG. DE HW?

- Projetar HW computacional
  - Propósito específico, processadores, comunicação
- Testar HW
  - Ciclo teste > atualização > teste
- Suportar o SW
  - Drivers, SO, emuladores, etc.

COMPLICAÇÕES

- HW é intolerante a erros
- Criatividade e habilidade em solucionar problemas
- Capacidade analítica

TEXTO PARA LEITURA (IMEDIATA)

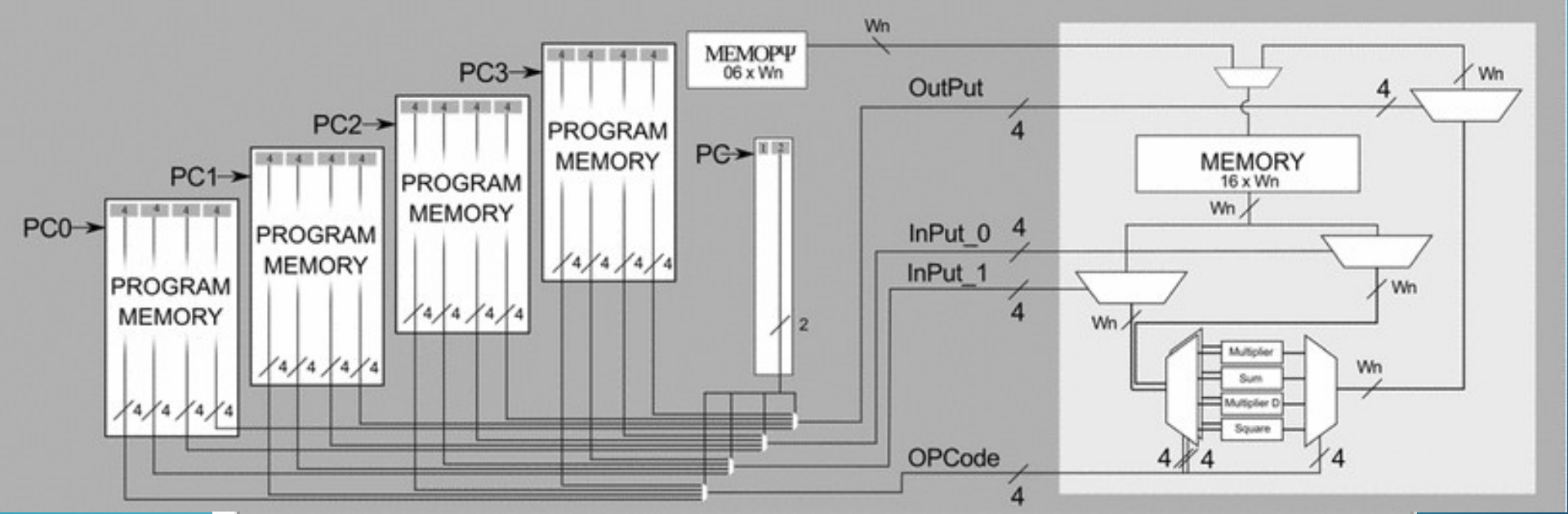
bit.ly/
2u8SlrI

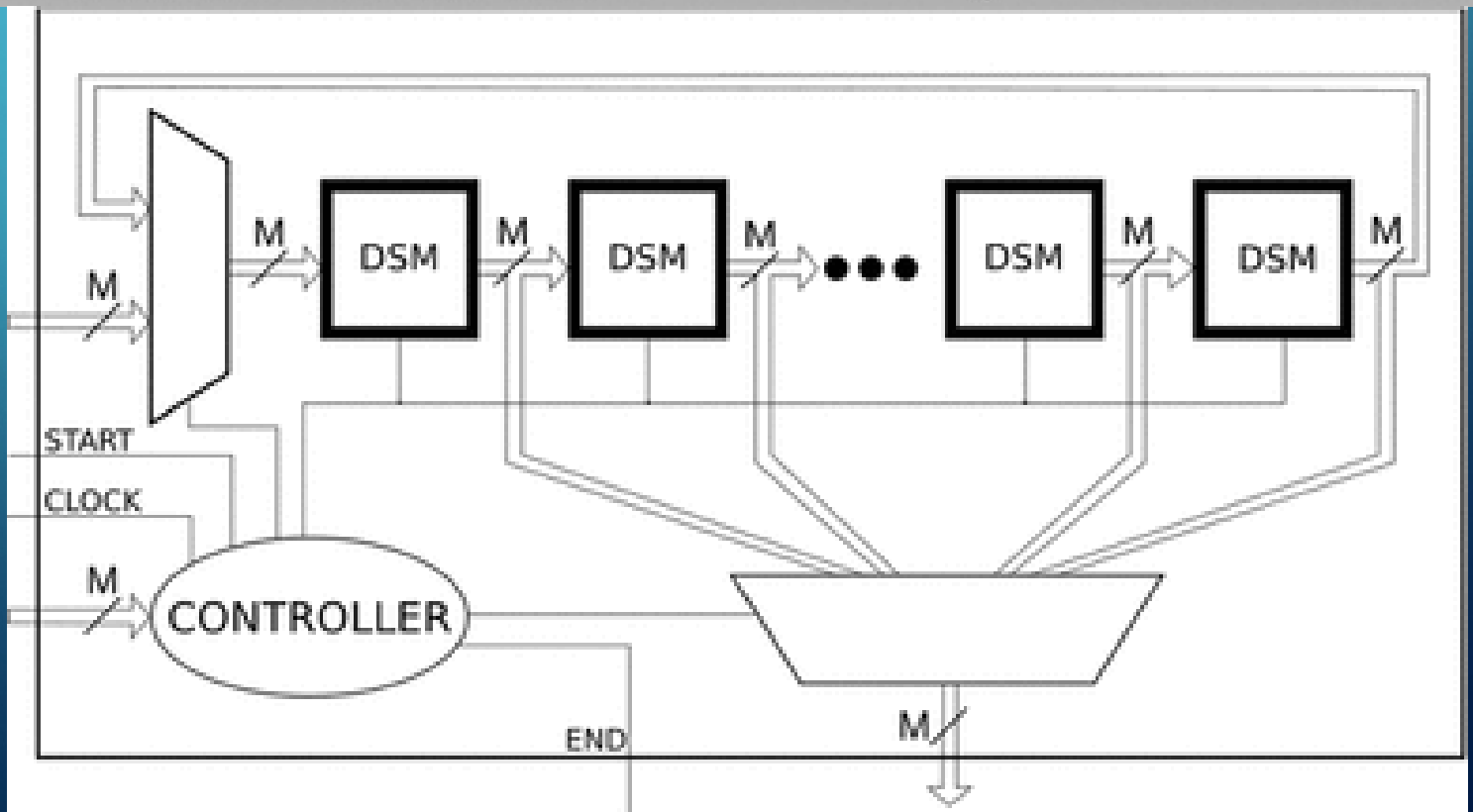
PESQUISA EM HARDWARE NO PCS

- Arquiteturas
- Hardware paralelo
- Sistemas Embarcados
- Aplicações

ARQUITETURAS

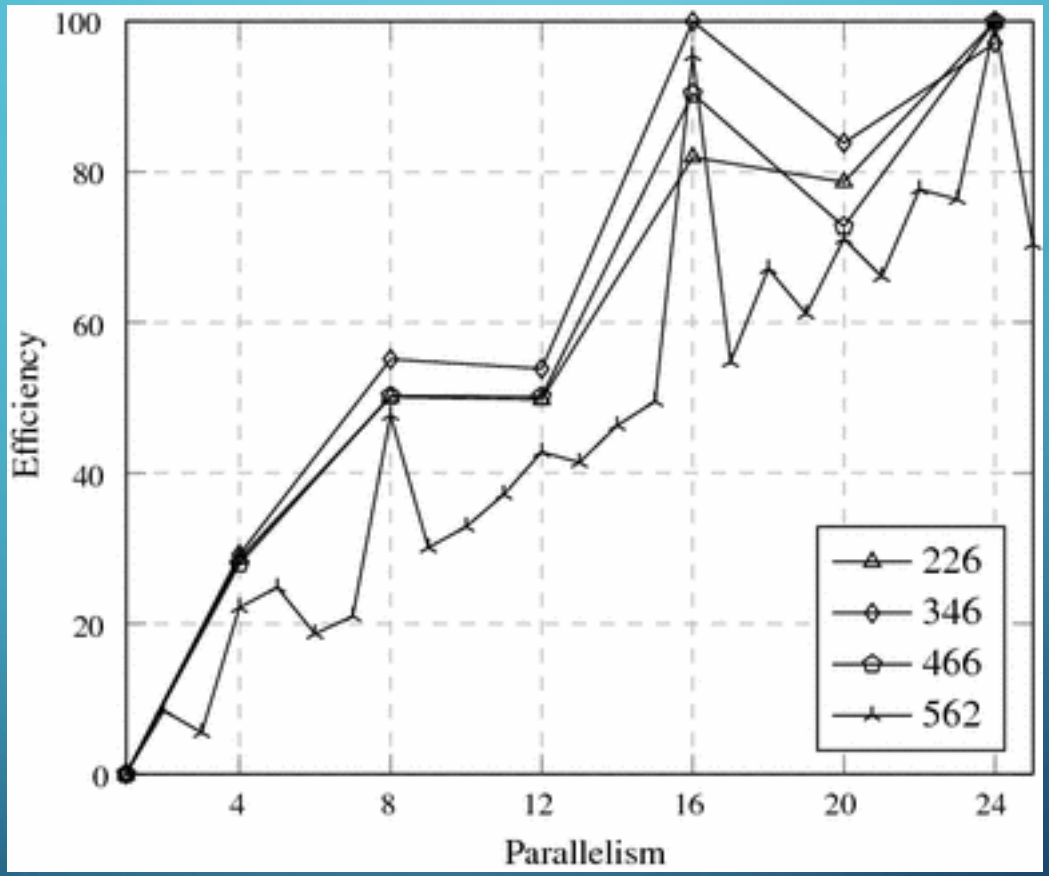
- Hardware de propósito específico
  - Criptohardware
  - Unidades voltadas para IA


PC0
PC1
PC2
PC3
PC
PROGRAM MEMORY
PROGRAM MEMORY
PROGRAM MEMORY
PROGRAM MEMORY
MEMORY
06 x Wn
Wn
OutPut
4
MEMORY
16 x Wn
Wn
InPut_0
InPut_1
Multiplier
Sum
Multiplier D
Square
OPCode
2


M
DSM
DSM
DSM
DSM
START
CLOCK
CONTROLLER
END

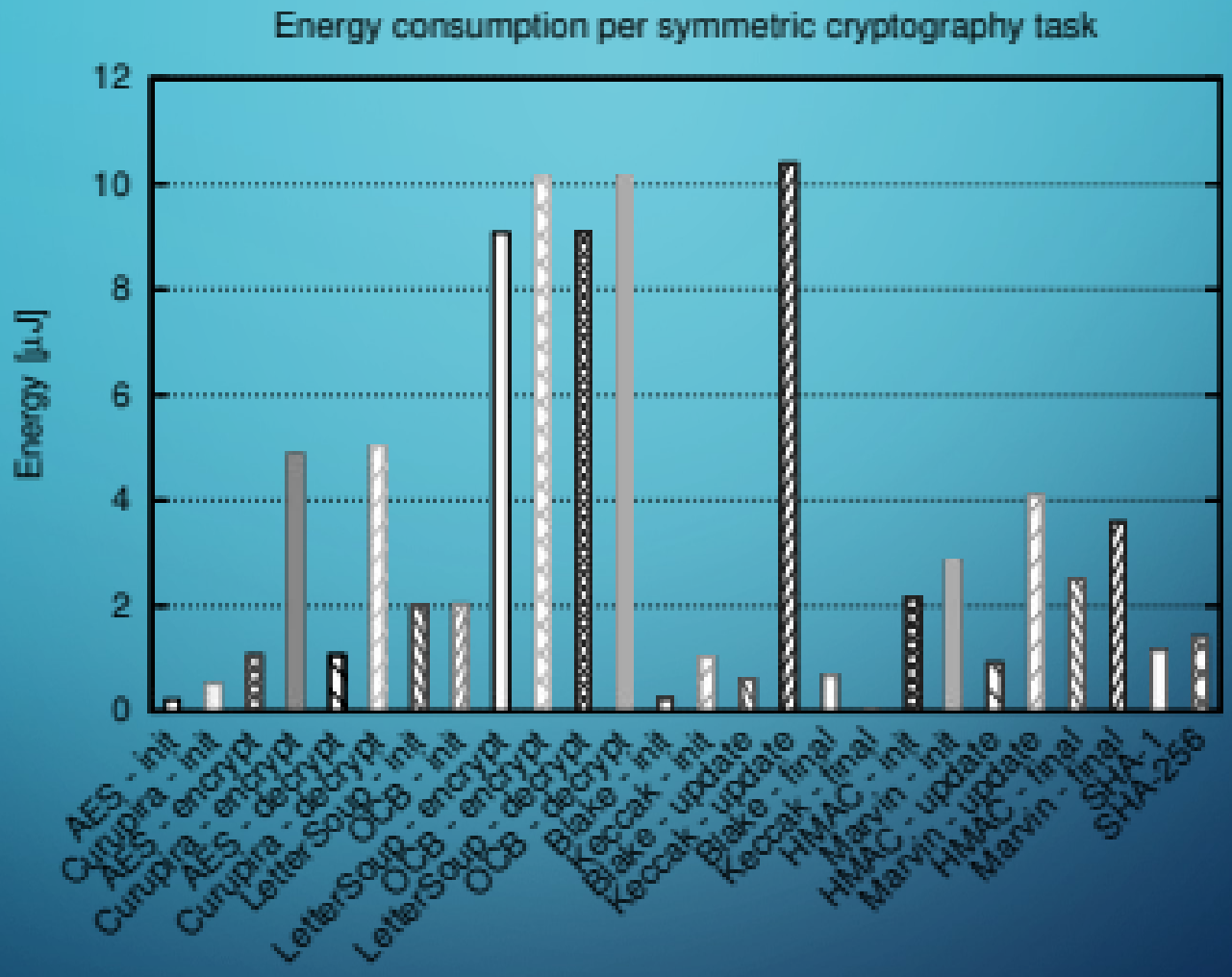
HARDWARE PARALELO

- Como fazer várias coisas ao mesmo tempo?
- Como aproveitar arquiteturas massivamente paralelas?


100
80
60
40
20
0
Efficiency
4
8
12
16
20
24
Parallelism
226
346
466
562

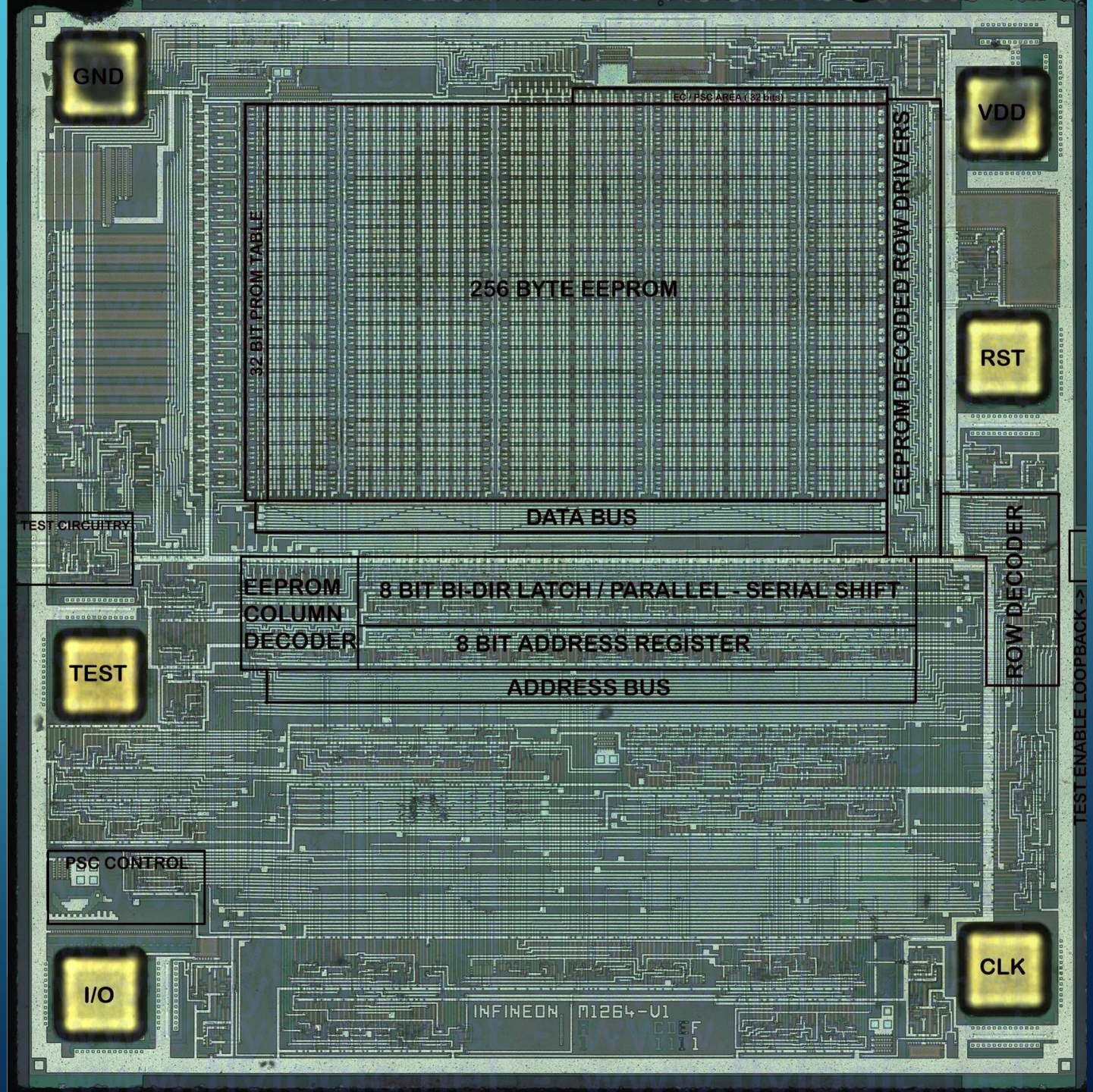
SISTEMAS EMBARCADOS

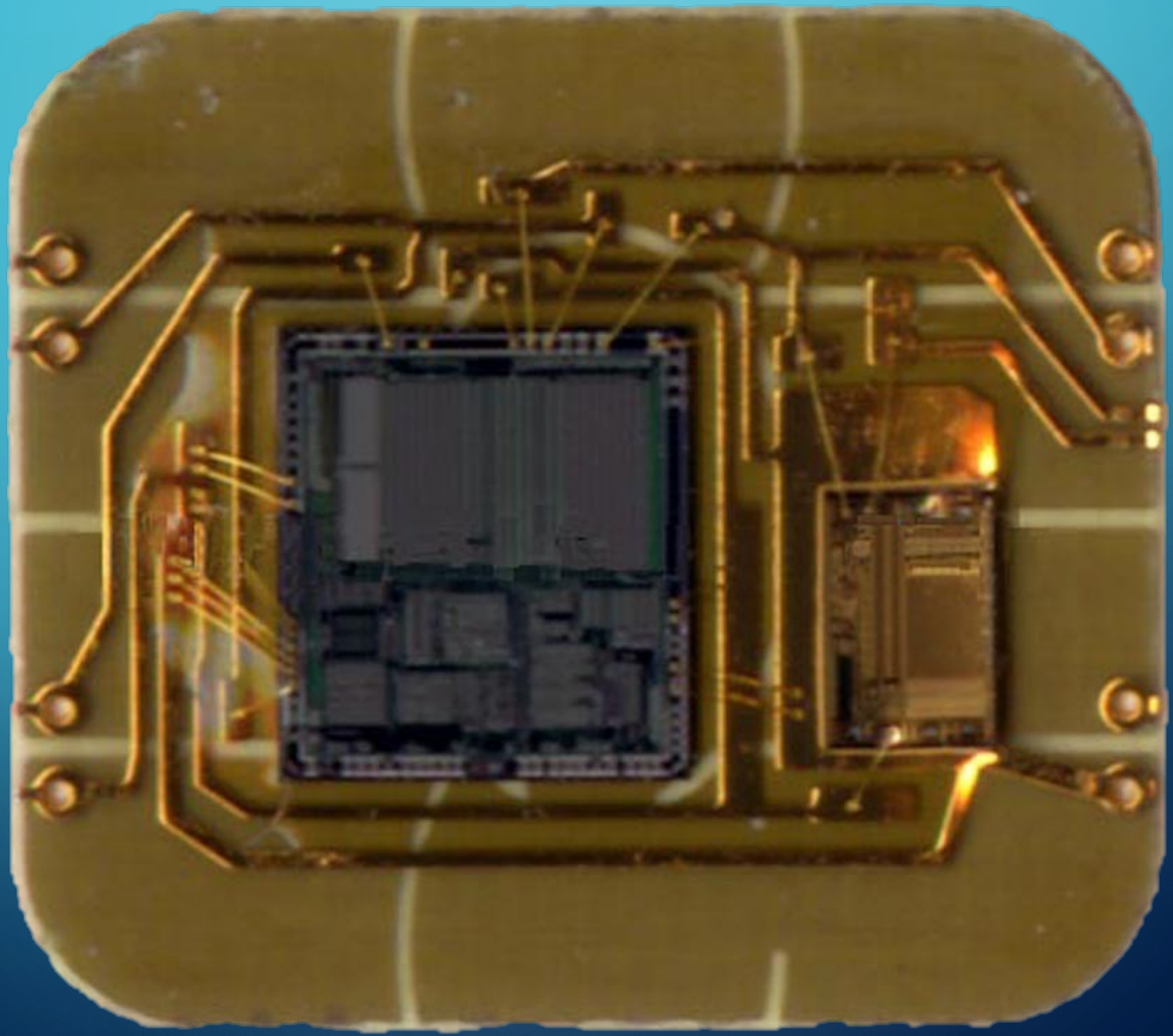
- Redes de sensores sem fio
  - Transmissão de dados ad-hoc
  - Protocolos
  - SDR (*Software Defined Radio*)
  - Segurança

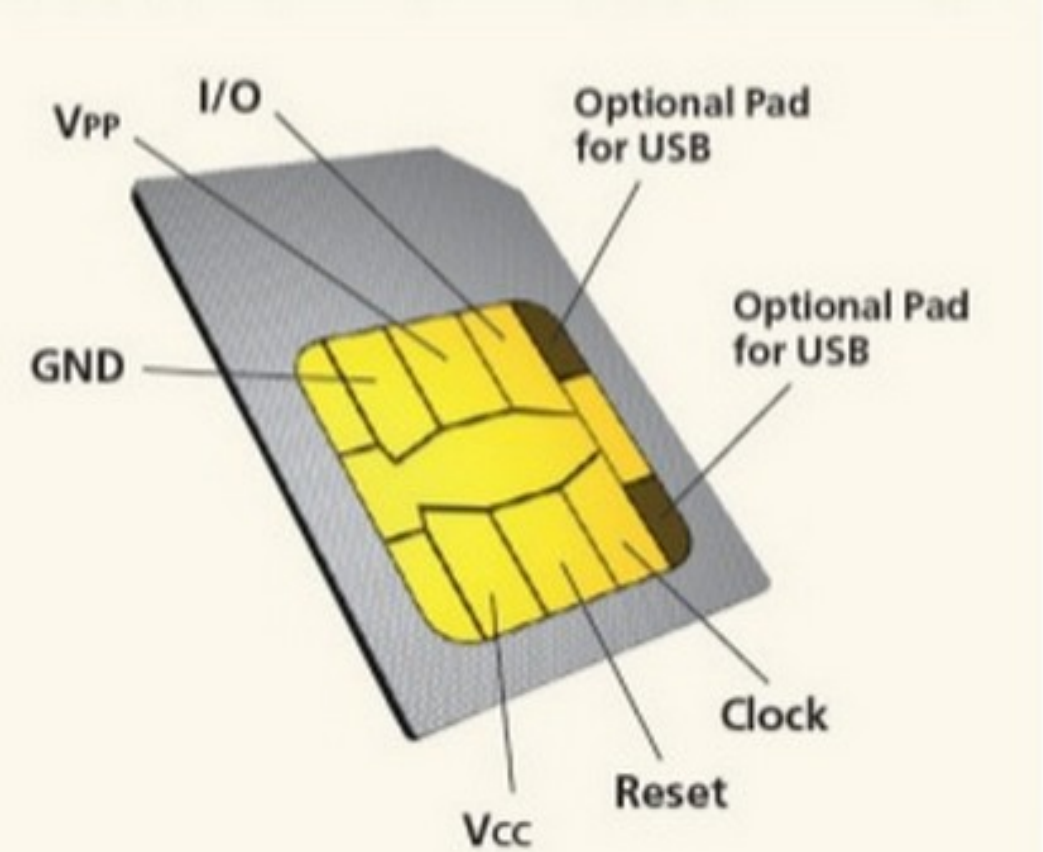

Energy consumption per symmetric cryptography task
Energy [µJ]
0
2
4
6
8
10
12
AES - init
Cunpira - init
AES - encryp
Cunpira - encryp
AES - decryp
Cunpira - decryp
LetterSoup - init
OCB - init
LetterSoup - encryp
OCB - encryp
LetterSoup - decryp
OCB - decryp
Blake - init
Keccak - init
Blake - update
Keccak - update
Blake - final
Keccak - final
HMAC - init
Marvin - init
HMAC - update
Marvin - update
HMAC - final
Marvin - final
SHA-1
SHA-256

SISTEMAS EMBARCADOS

- Consumo de energia
  - Hardware específico para economia de energia
  - Ambientes severamente limitados


GND
VDD
RST
TEST
I/O
CLK
EC / PSC AREA (32 bits)
32 BIT PROM TABLE
256 BYTE EEPROM
EEPROM DECODED ROW DRIVERS
DATA BUS
TEST CIRCUITRY
EEPROM COLUMN DECODER
8 BIT BI-DIR LATCH / PARALLEL - SERIAL SHIFT
8 BIT ADDRESS REGISTER
ADDRESS BUS
ROW DECODER
TEST ENABLE LOOPBACK ->
PSC CONTROL
INFINEON M1264-V1





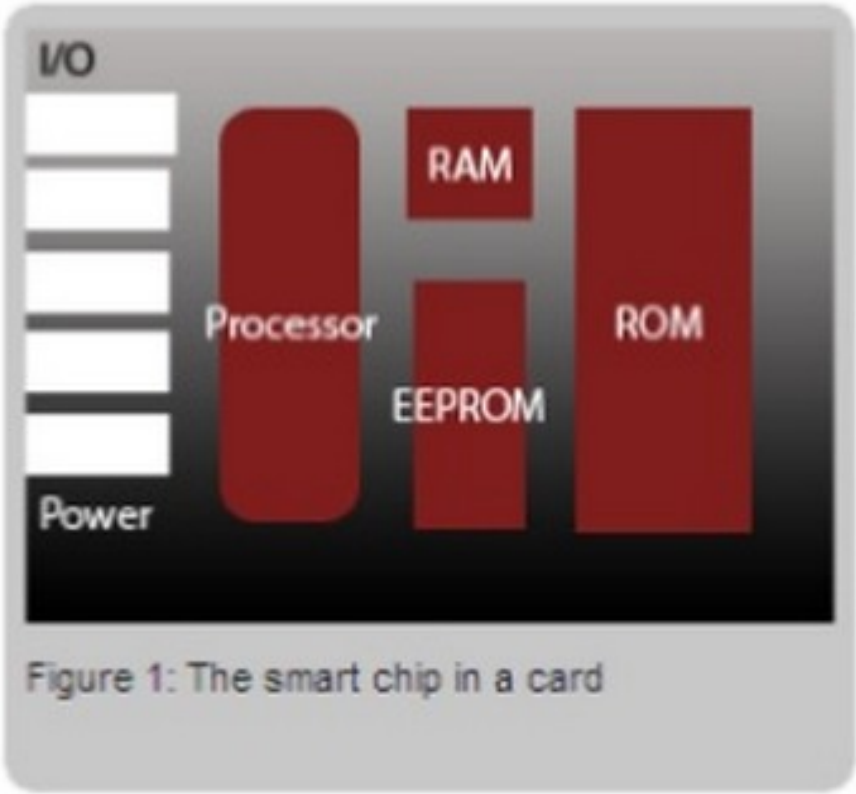
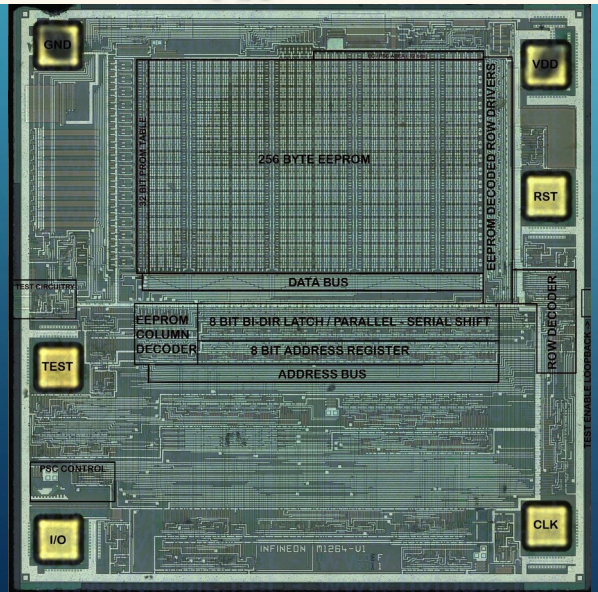
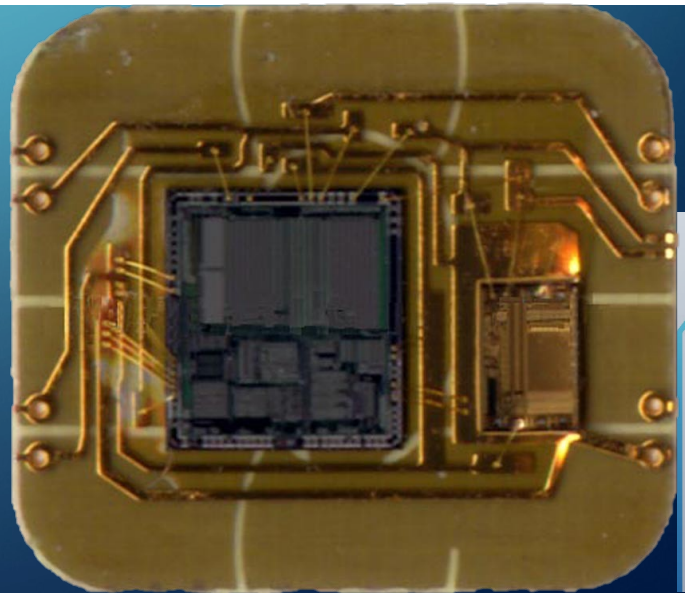


Figure 1: The smart chip in a card

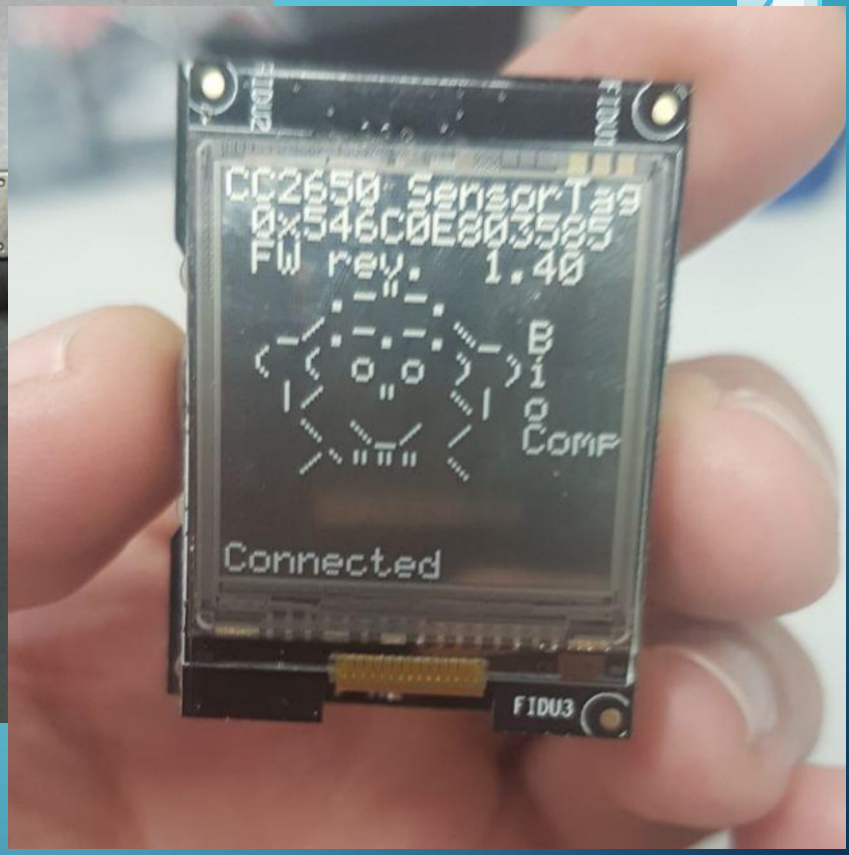




APLICAÇÕES

- A mágica da computação...
- Localização
- Coleta de Dados
  - *Citizen Science*
- Aceleração de desempenho

EXEMPLOS



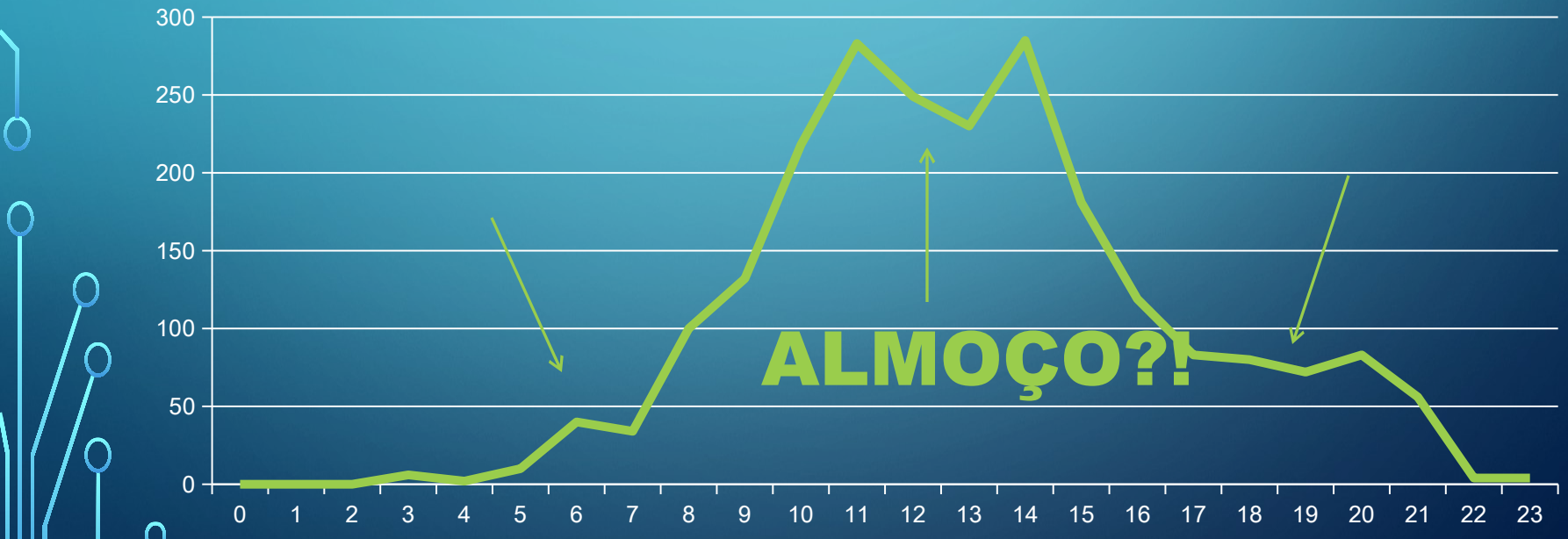
Bio Comp

INSTITUTO BUTANTAN

Museu IB INSTITUTO BUTANTAN

observatório de aves butantan


microSensys
Serien-Nr.: 0060212
microSensys
Serien-Nr.: 0060217


300
250
200
150
100
50
0
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23
ALMOÇO?!


eko Node 1
eKo Node 3
eKo Node 2
Base 0
eKo Node 5
eKo Node 6


Image © 2014 DigitalGlobe
© 2013 Google
Google earth
Guia de turismo
2005
Data das imagens: 8/23/2012 23°33'52.12"S 46°43'51.82"O elev 778 m altitude do ponto de visão 2.34 km

OUTROS PROJETOS

- Audio Fingerprint + CNN
- PCL motion detection
- Video colorizing
- Neuromorphic Processor

ONDA MAKER

- Dispositivo de prototipação
- Linguagens de descrição
- Laboratório Digital ☺

http://www.laa.pcs.usp.br

http://www.biocomp.org.br

balbertini@usp.br