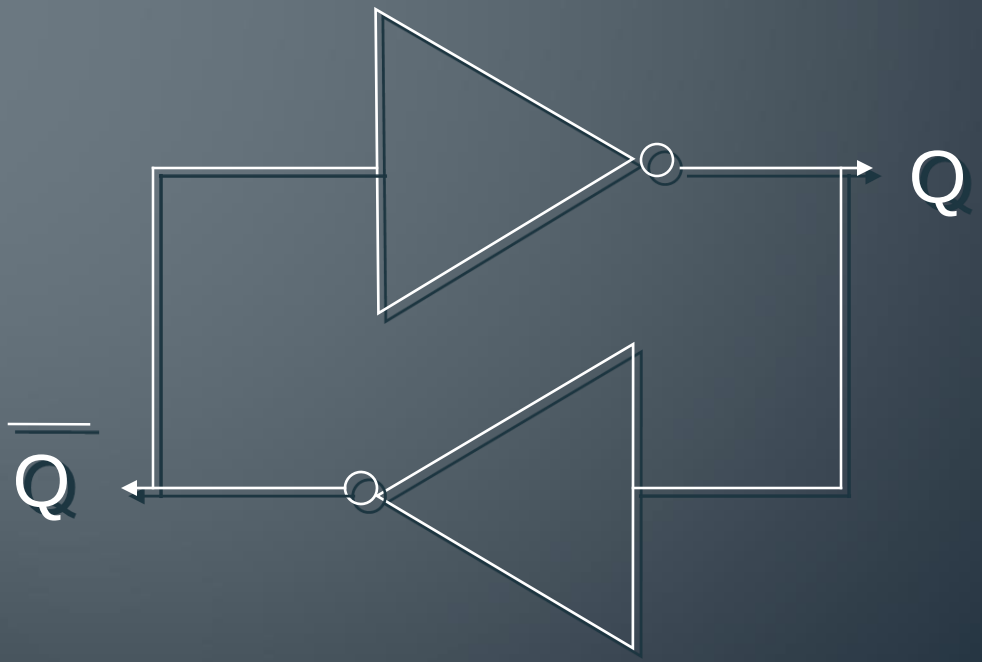
SEL 454

Introdução aos Sistemas Digitais

SISTEMAS SEQUENCIAIS BIESTÁVEIS

Prof. Homero Schiabel

LATCH RS



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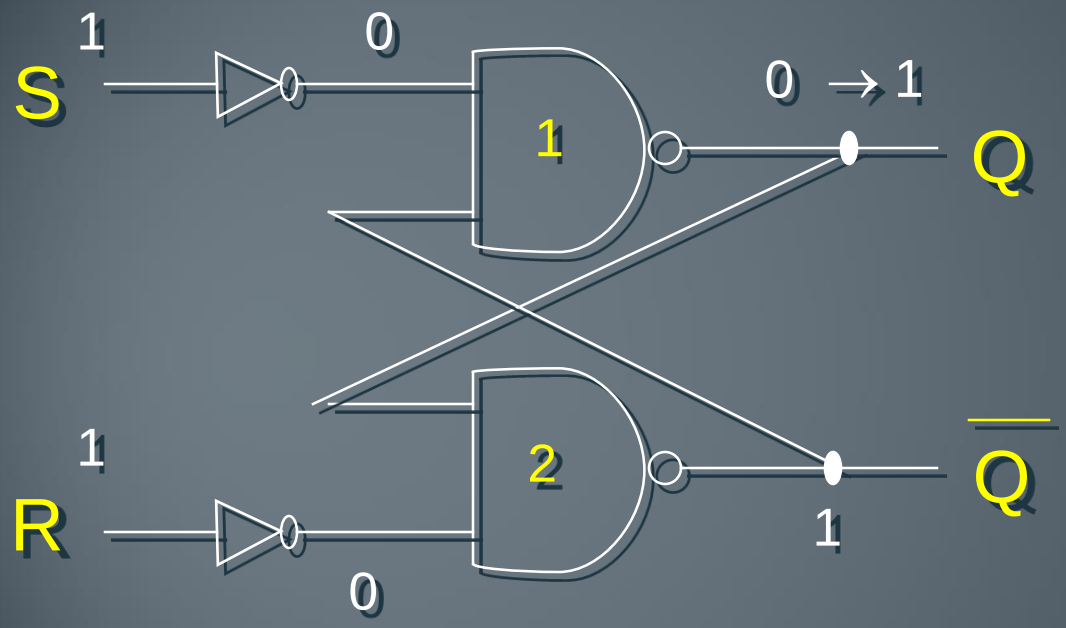

Condição Inicial ➔ Q = 0

S	R	1	2	Q	$\overline{Q}$	
0	0	1 1	0 1	0	1	
0	1	1 1	0 0	0	1	
1	0	0 1	0 1	1	1	*
		0 1	1 1	1	0	
1	1	0 1	0 0	1	1	
		0 1	1 0	1	1	**

* Estado instável

** "Incompatibilidade" (Est. "proibido")

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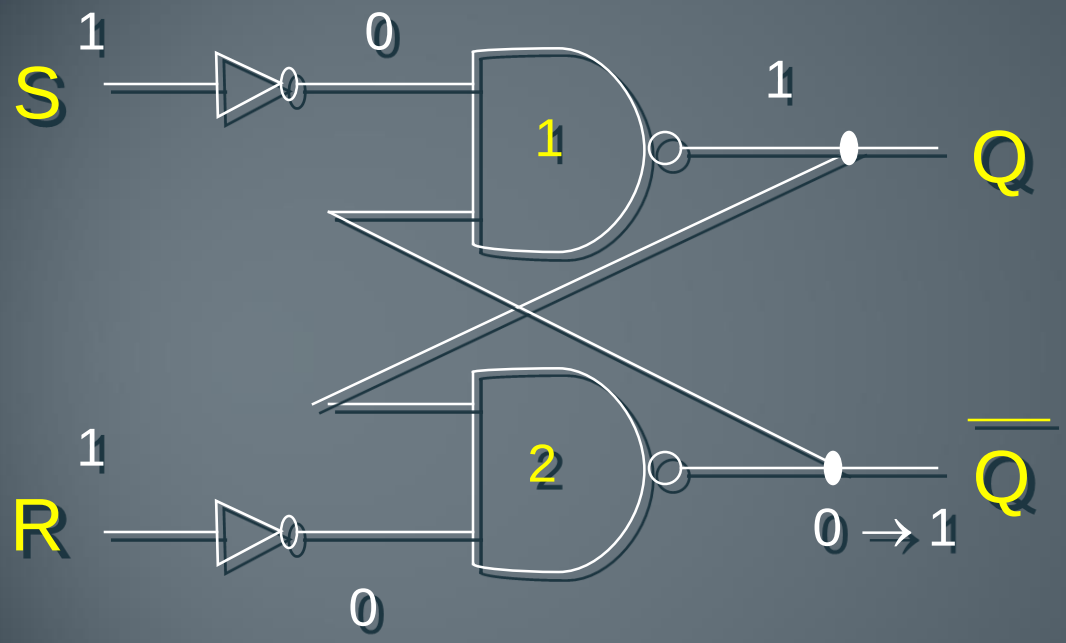

Condição Inicial ➔ Q = 1

S	R	1	2	Q	$\overline{Q}$
0	0	1 0	1 1	1	0
0	1	1 0	1 0	1	1 *
		1 1	1 0	0	1
1	0	0 0	1 1	1	0
1	1	0 0	1 0	1	1
		0 1	1 0	1	1**

* Estado instável

** "Incompatibilidade" (Est. "proibido")

Tabela da verdade:

Q = 0

S	R	Q	$\overline{Q}$
0	0	0	1
0	1	0	1
1	0	1	0
1	1	1	1**

Q = 1

S	R	Q	$\overline{Q}$
0	0	1	0
0	1	0	1
1	0	1	0
1	1	1	1**

Condição de memória!

S	R	Q*
0	0	Q
0	1	0
1	0	1
1	1	1 **

Reset

Set

** “Incompatibilidade”
(Est. “proibido”)

Mas... Por que "Estado proibido" (S=R=1)?

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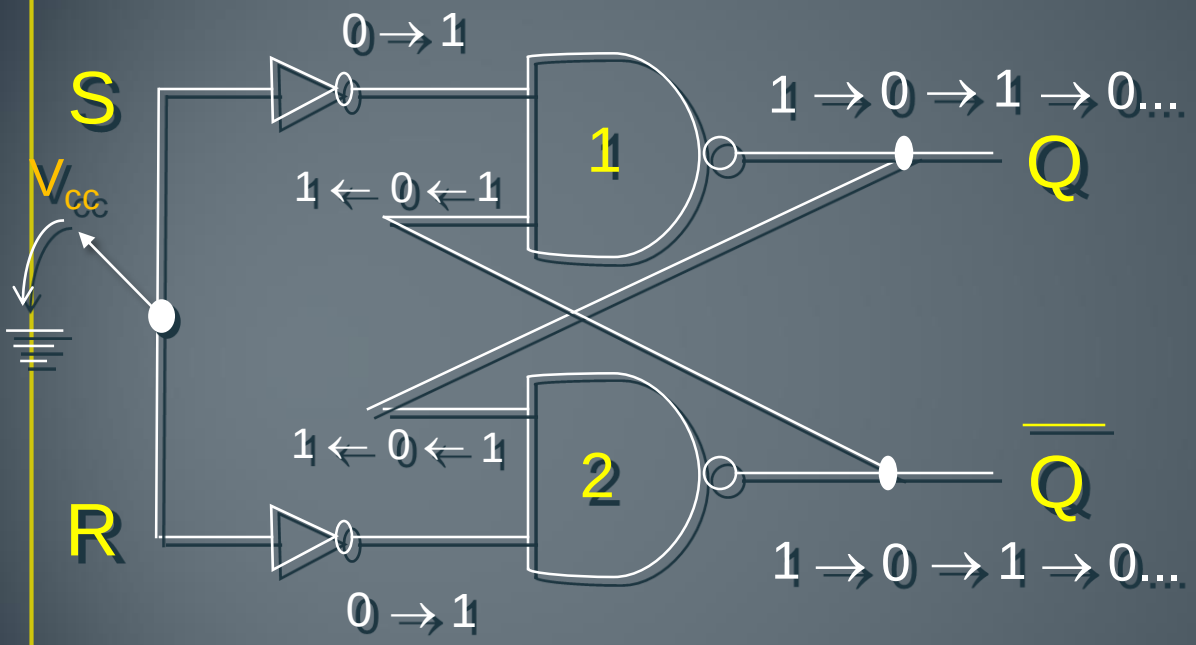
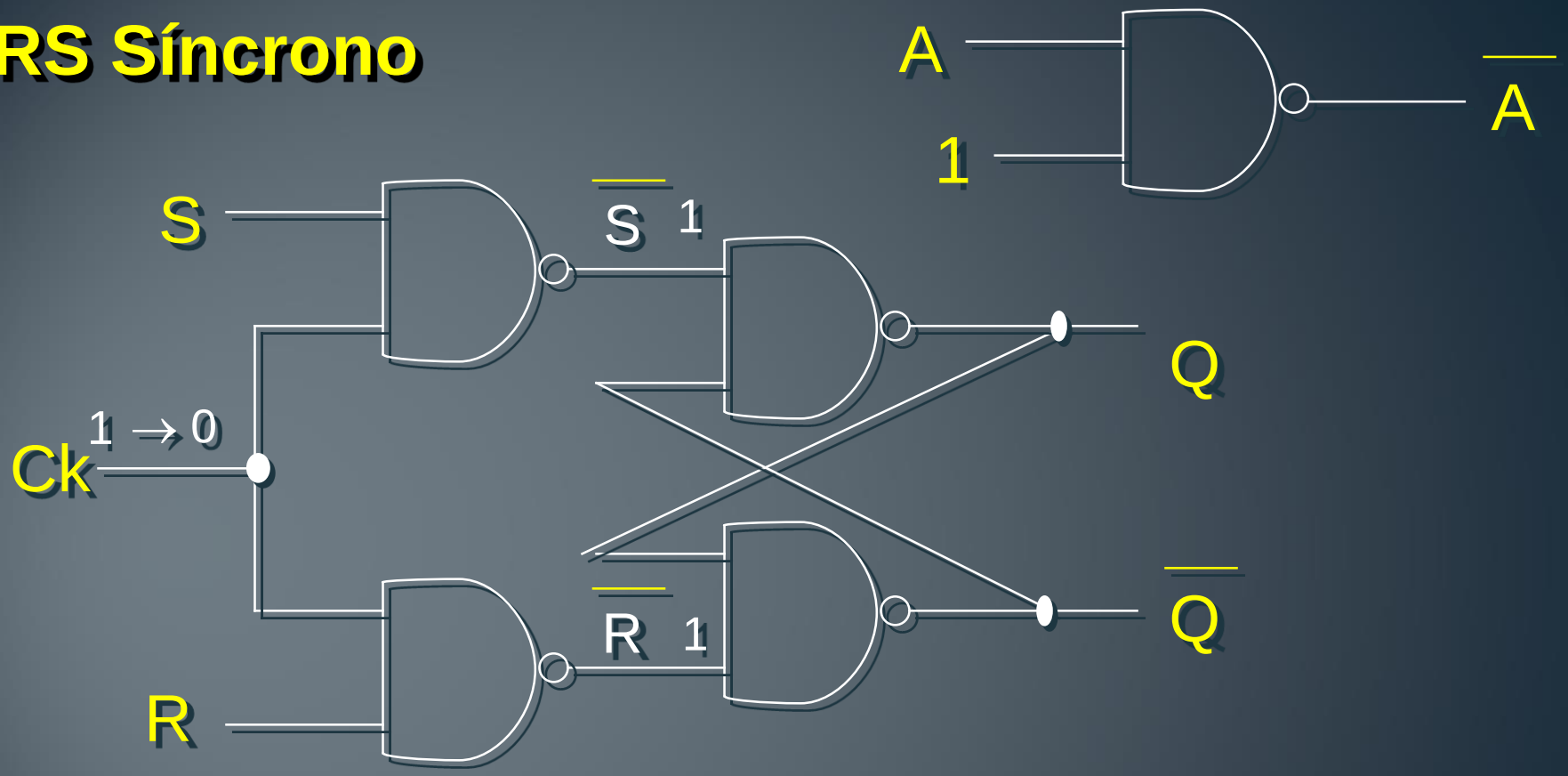


Condição de memória

S	R	Q*
0	0	Q
0	1	0
1	0	1
1	1	1 **

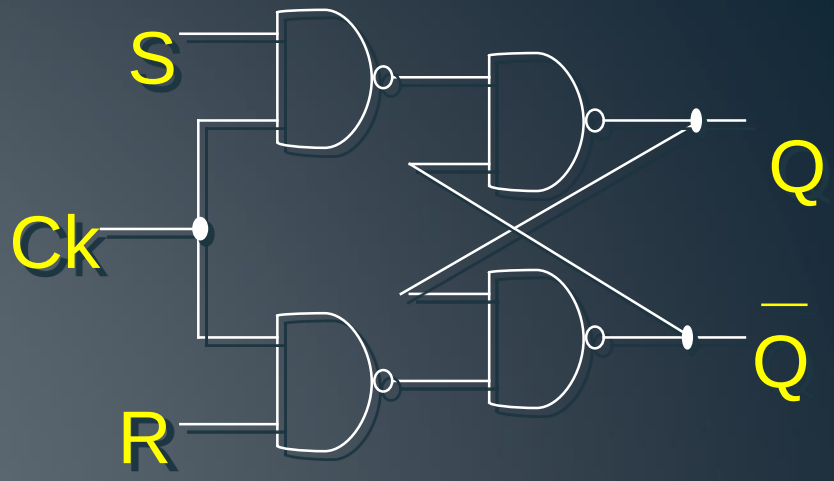
** “Incompatibilidade”
(Est. “proibido”)

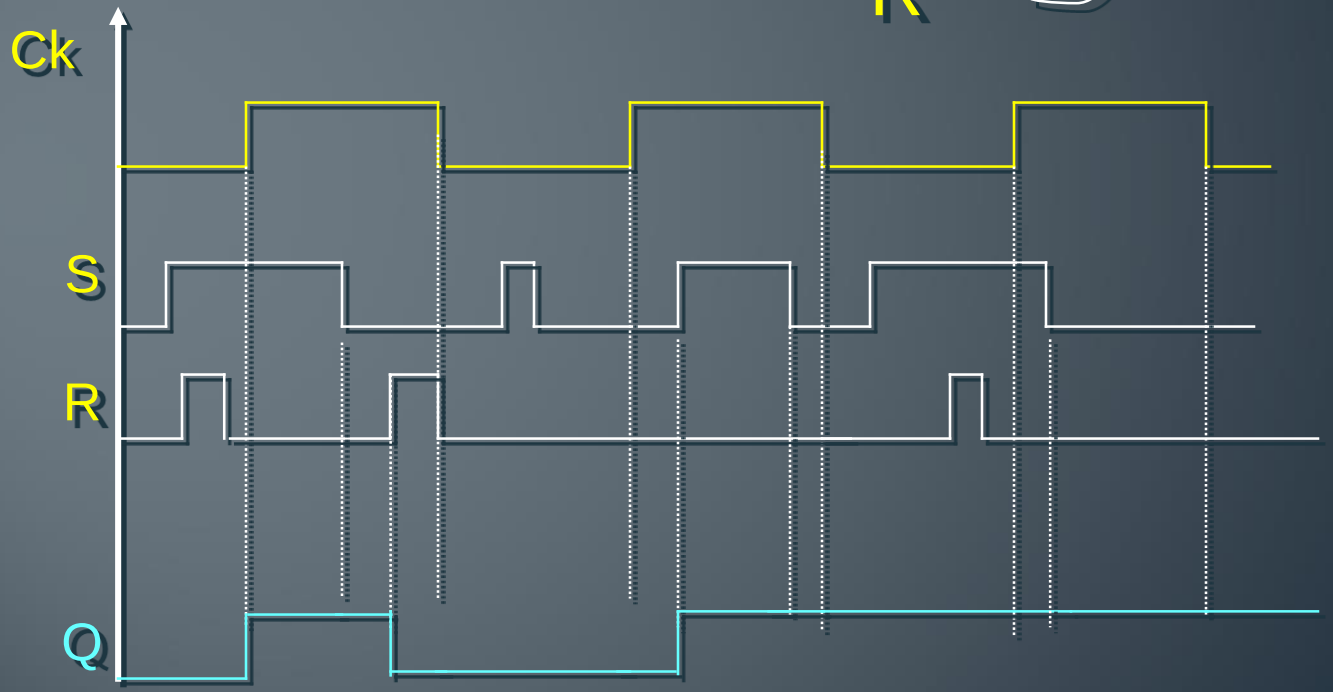
RS Síncrono



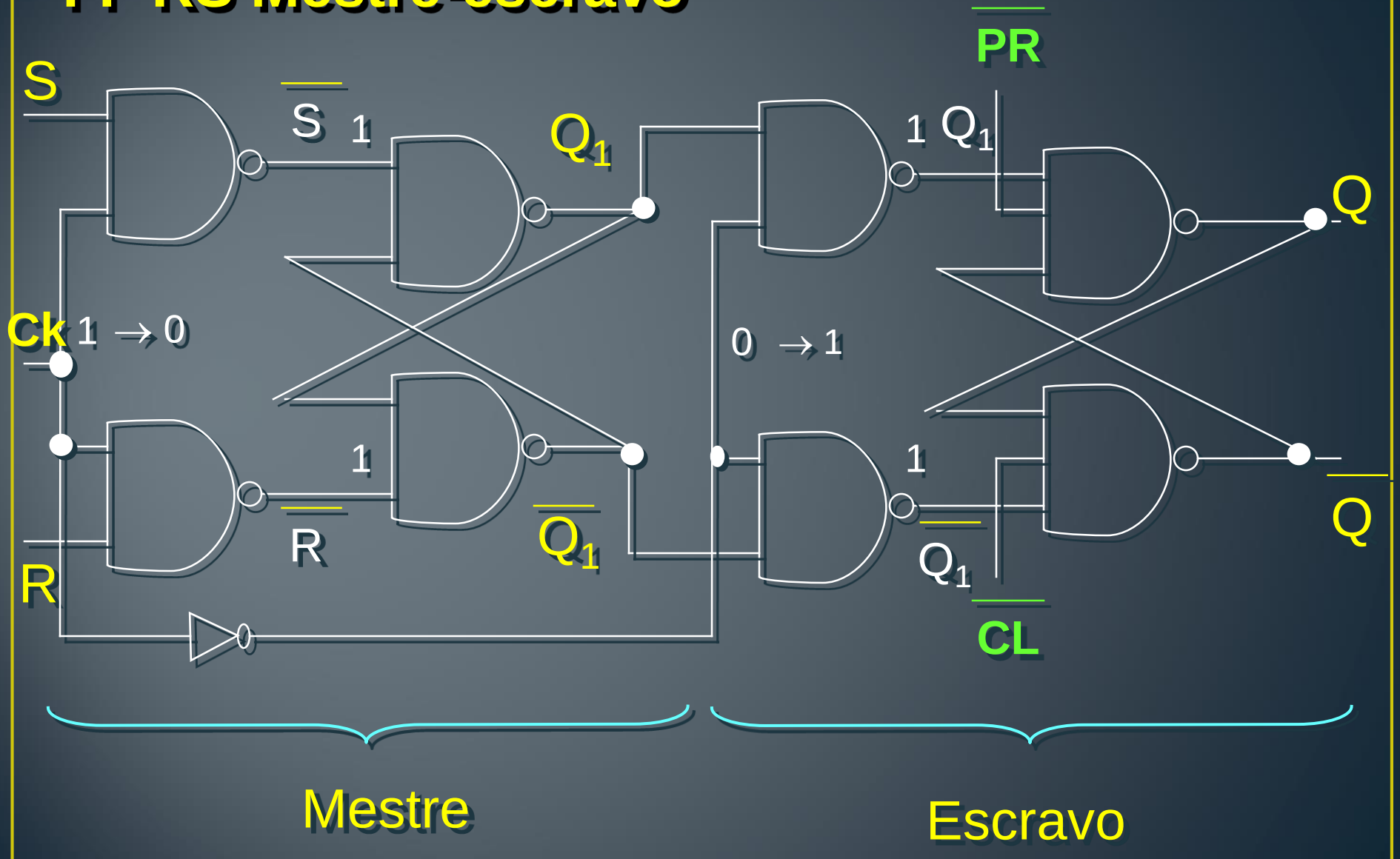
- Para Ck=0 ➔ Q e $\overline{Q}$ não "sentirão" eventuais variações nas entradas
- Para Ck=1 ➔ funcionamento normal (portas de entrada habilitadas)

RS Síncrono





FF RS Mestre-escravo



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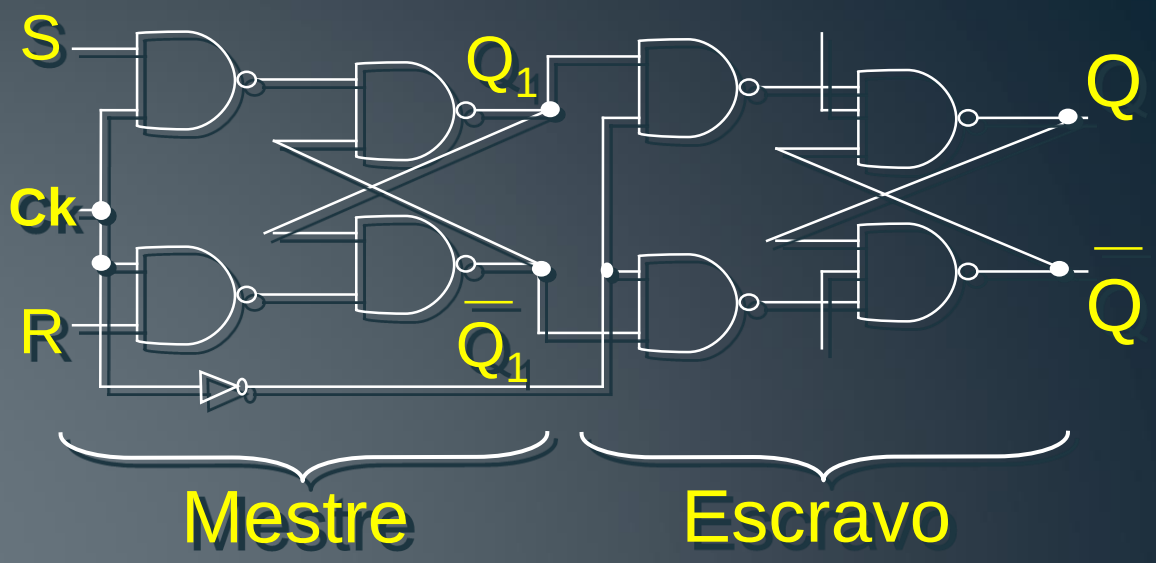

- Ck=1 ➔ Q_1 e $\overline{Q_1}$ respondem às variações de S e R (circuito Mestre habilitado) ➔ entradas do circuito Escravo: desabilitadas ➔ Q e $\overline{Q}$ = ctes)
- Ck=1→0 ➔ Q_1 e $\overline{Q_1}$ passam adiante (circuito Escravo habilitado) e podem afetar Q e $\overline{Q}$ ➔ entradas do circuito Mestre: desabilitadas
- Ck=0 ➔ Q_1 e $\overline{Q_1}$ = ctes ➔ Q e $\overline{Q}$ = ctes

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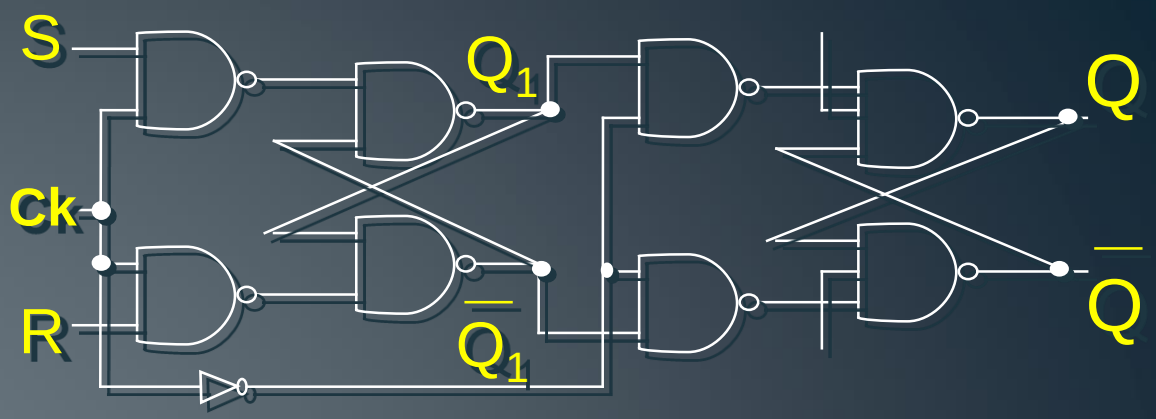
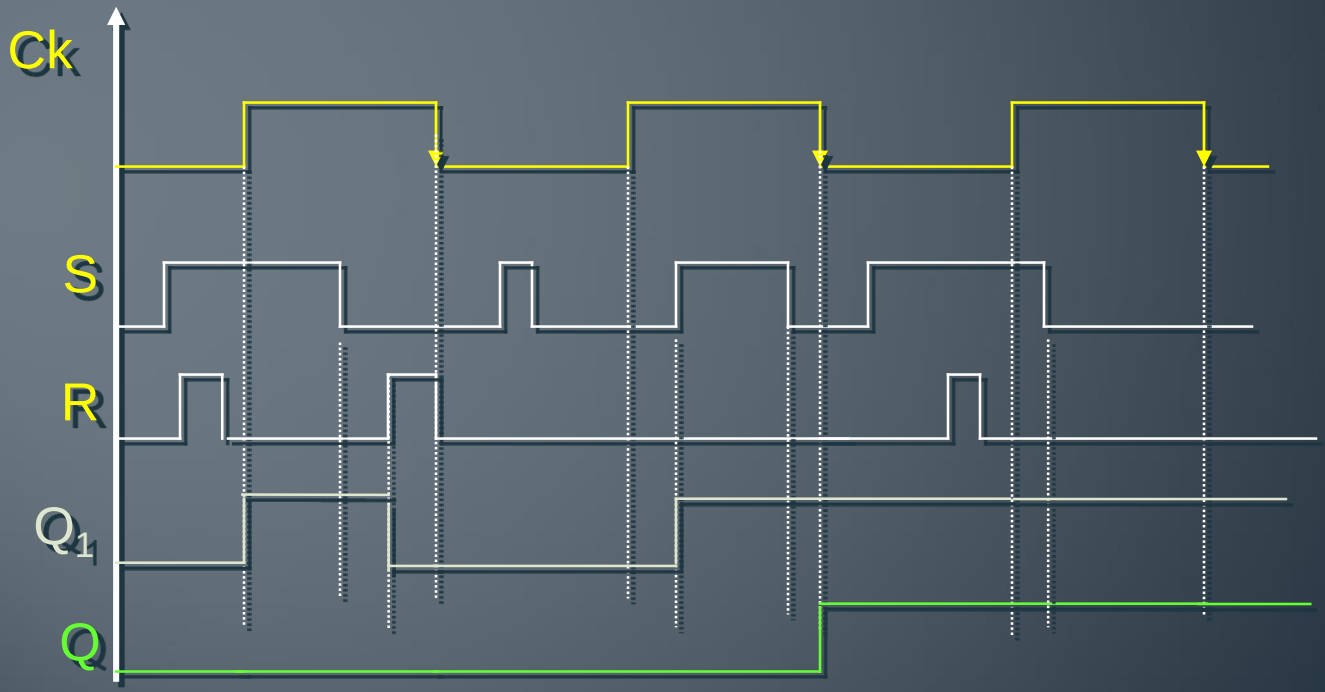
Controle ✓

Estabilidade ?

(S=R=1)





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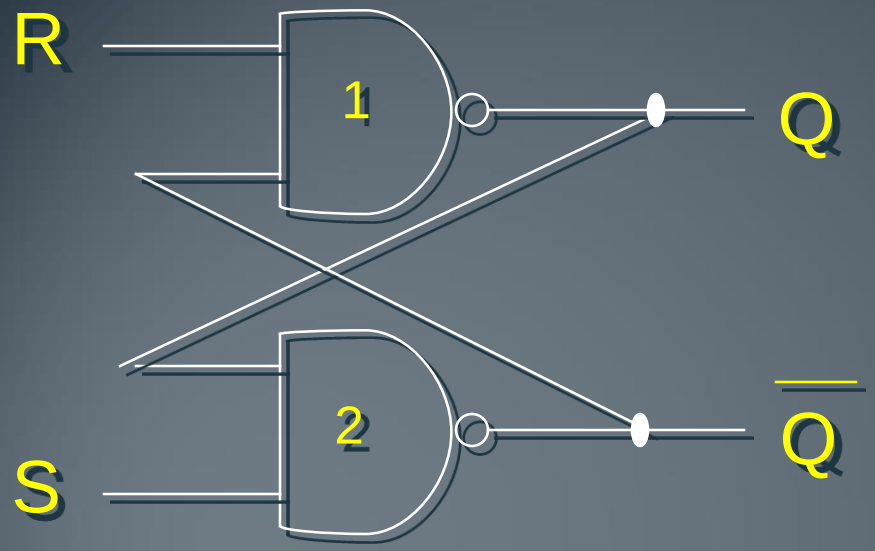
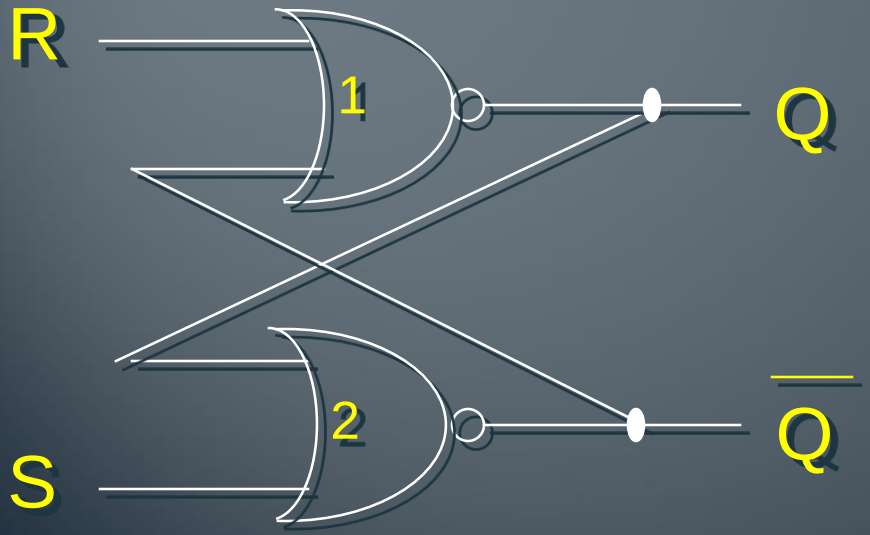


R	S	Q
0	0	1 **
0	1	1
1	0	0
1	1	Q_a



R	S	Q
0	0	Q_a
0	1	1
1	0	0
1	1	1 **