## 6.3 Digital implementation of analog controller design

This section introduces an indirect approach to digital controller design. The approach is based on designing an analog controller for the analog subsystem and then obtaining an equivalent digital controller and using it to digitally implement the desired control. The digital controller can be obtained using a number of recipes that are well known in the field of signal processing, where they are used in the design of digital filters. In fact, a controller can be viewed as a filter that attenuates some dynamics and accentuates others so as to obtain the desired time response. We limit our discussion of digital filters and the comparison of various recipes for obtaining them from analog filters to differencing methods, pole-zero matching, and bilinear transformation. The system configuration we consider is shown in Figure 6.12. The system includes (1) a $z$-transfer function model of a DAC, analog subsystem, and ADC and (2) a cascade controller. We begin with a general procedure to obtain a digital controller using analog design.

### PROCEDURE 6.1

1. Design a controller $C_a(s)$ for the analog subsystem to meet the desired design specifications.
2. Map the analog controller to a digital controller $C(z)$ using a suitable transformation.
3. Tune the gain of the transfer function $C(z)G_{ZAS}(z)$ using proportional $z$-domain design to meet the design specifications.
4. Check the sampled time response of the digital control system and repeat steps 1 to 3, if necessary, until the design specifications are met.

Step 2 of Procedure 6.1—that is, the transformation from an analog to a digital filter—must satisfy the following requirements:

1. A stable analog filter (poles in the left half plane (LHP)) must transform to a stable digital filter.
2. The frequency response of the digital filter must closely resemble the frequency response of the analog filter in the frequency range $0 \rightarrow \omega_s/2$ where $\omega_s$ is the sampling frequency.

Most filter transformations satisfy these two requirements to varying degrees. However, this is not true of all analog-to-digital transformations, as illustrated by the following section.

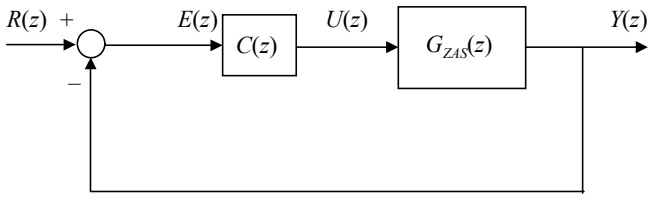


**FIGURE 6.12**

Block diagram of a single-loop digital control system.

### 6.3.1 Differencing methods

An analog filter can be represented by a transfer function or differential equation. Numerical analysis provides standard approximations of the derivative so as to obtain the solution to a differential equation. The approximations reduce a differential equation to a difference equation and could thus be used to obtain the difference equation of a digital filter from the differential equation of an analog filter. We examine two approximations of the derivative: forward differencing and backward differencing.

#### *Forward differencing*

The forward differencing approximation of the derivative is

$$\dot{y}(k) \cong \frac{1}{T}[y(k+1) - y(k)] \tag{6.13}$$

The approximation of the second derivative can be obtained by applying (6.13) twice—that is,

$$\begin{aligned} \ddot{y}(k) &\cong \frac{1}{T}[\dot{y}(k+1) - \dot{y}(k)] \\ &\cong \frac{1}{T}\left\{\frac{1}{T}[y(k+2) - y(k+1)] - \frac{1}{T}[y(k+1) - y(k)]\right\} \\ &= \frac{1}{T^2}\{y(k+2) - 2y(k+1) + y(k)\} \end{aligned} \tag{6.14}$$

Approximations of higher-order derivatives can be similarly obtained. Alternatively, one may consider the Laplace transform of the derivative and the $z$-transform of the difference in (6.13). This yields the mapping

$$sY(s) \rightarrow \frac{1}{T}[z-1]Y(z) \tag{6.15}$$

Therefore, the direct transformation of an $s$-transfer function to a $z$-transfer function is possible using the substitution

$$s \rightarrow \frac{z-1}{T} \tag{6.16}$$

---

**EXAMPLE 6.5: FORWARD DIFFERENCE**

Apply the forward difference approximation of the derivative to the second-order analog filter

$$C_a(s) = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

and examine the stability of the resulting digital filter for a stable analog filter.

**Solution**

The given filter is equivalent to the differential equation

$$\ddot{y}(t) + 2\zeta\omega_n\dot{y}(t) + \omega_n^2 y(t) = \omega_n^2 u(t)$$

where $y(t)$ is the filter output and $u(t)$ is the filter input. The approximation of the first derivative by (6.13) and the second derivative by (6.14) gives the difference equation

$$\frac{1}{T^2}\Big\{y(k+2) - 2y(k+1) + y(k)\} + 2\zeta\omega_n\frac{1}{T}[y(k+1) - y(k)] + \omega_n^2 y(k) = \omega_n^2 u(k)$$

Multiplying by $T^2$ and rearranging terms, we obtain the digital filter

$$y(k+2) + 2[\zeta\omega_n T - 1]y(k+1) + [(\omega_n T)^2 - 2\zeta\omega_n T + 1]y(k) = (\omega_n T)^2 u(k)$$

Equivalently, we obtain the transfer function of the filter using the simpler transformation (6.16)

$$C(z) = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}\bigg|_{s=\frac{z-1}{T}}$$
$$= \frac{(\omega_n T)^2}{z^2 + 2[\zeta\omega_n T - 1]z + [(\omega_n T)^2 - 2\zeta\omega_n T + 1]}$$

For a stable analog filter, we have $\zeta > 0$ and $\omega_n > 0$ (positive denominator coefficients are sufficient for a second-order polynomial). However, the digital filter is unstable if the magnitude of the constant term in its denominator polynomial is greater than unity. This gives the instability condition

$$(\omega_n T)^2 - 2\zeta\omega_n T + 1 > 1$$
$$\textbf{i.e.}, \quad \zeta < \omega_n T/2$$

For example, a sampling period of 0.2 s and an undamped natural frequency of 10 rad/s yield unstable filters for any underdamped analog filter.

## *Backward differencing*

The backward differencing approximation of the derivative is

$$\dot{y}(k) \cong \frac{1}{T}[y(k) - y(k-1)] \tag{6.17}$$

The approximation of the second derivative can be obtained by applying (6.17) twice—that is,

$$\begin{aligned}\ddot{y}(k) &\cong \frac{1}{T}[\dot{y}(k) - \dot{y}(k-1)] \\ &\cong \frac{1}{T}\left\{\frac{1}{T}[y(k) - y(k-1)] - \frac{1}{T}[y(k-1) - y(k-2)]\right\} \\ &= \frac{1}{T^2}\{y(k) - 2y(k-1) + y(k-2)\}\end{aligned} \tag{6.18}$$

Approximations of higher-order derivatives can be similarly obtained. One may also consider the Laplace transform of the derivative and the $z$-transform of the difference in (6.17). This yields the substitution

$$s \to \frac{z-1}{zT} \tag{6.19}$$

**EXAMPLE 6.6: BACKWARD DIFFERENCE**

Apply the backward difference approximation of the derivative to the second-order analog filter

$$C_a(s) = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

and examine the stability of the resulting digital filter for a stable analog filter.

**Solution**

We obtain the transfer function of the filter using (6.19)

$$C(z) = \left.\frac{\omega_n^2}{s^2+2\zeta\omega_n s+\omega_n^2}\right|_{s=\frac{z-1}{zT}}$$

$$= \frac{(\omega_n T z)^2}{[(\omega_n T)^2 + 2\zeta\omega_n T + 1]z^2 - 2[\zeta\omega_n T + 1]z + 1}$$

The stability conditions for the digital filter are (see Chapter 4)

$$[(\omega_n T)^2 + 2\zeta\omega_n T + 1] + 2[\zeta\omega_n T + 1] + 1 > 0$$
$$[(\omega_n T)^2 + 2\zeta\omega_n T + 1] - 1 > 0$$
$$[(\omega_n T)^2 + 2\zeta\omega_n T + 1] - 2[\zeta\omega_n T + 1] + 1 > 0$$

The conditions are all satisfied for $\zeta > 0$ and $\omega_n > 0$—that is, for all stable analog filters.

### 6.3.2 Pole-zero matching

We know from equation (6.3) that discretization maps an $s$-plane pole at $p_s$ to a $z$-plane pole at $e^{psT}$ but that no rule exists for mapping zeros. In pole-zero matching, a discrete approximation is obtained from an analog filter by mapping both poles and zeros using (6.3). If the analog filter has $n$ poles and $m$ zeros, then we say that the filter has $n - m$ zeros at infinity. For $n - m$ zeros at infinity, we add $n - m$ or $n - m - 1$ digital filter zeros at unity. If the zeros are not added, it can be shown that the resulting system will include a time delay (see Problem 6.5). The second choice gives a strictly proper filter where the computation of the output is easier, since it only requires values of the input at past sampling points. Finally, we adjust the gain of the digital filter so that it is equal to that of the analog filter at a critical frequency dependent on the filter. For a low-pass filter, $\alpha$ is selected so that the gains are equal at DC; for a bandpass filter, they are set equal at the center of the pass band.

For an analog filter with transfer function

$$G_a(s) = K\frac{\prod_{i=1}^{m}(s-a_i)}{\prod_{j=1}^{m}(s-b_j)} \tag{6.20}$$

we have the digital filter

$$G(z) = \alpha K\frac{(z+1)^{n-m-1}\prod_{i=1}^{m}(z-e^{a_iT})}{\prod_{j=1}^{m}(z-e^{b_jT})} \tag{6.21}$$

where $\alpha$ is a constant selected for equal filter gains at a critical frequency. For example, for a low-pass filter, $\alpha$ is selected to match the DC gains using $G_a(1) = G_a(0)$, while for a high-pass filter, it is selected to match the high-frequency gains using $G(-1) = G_a(\infty)$. Setting $z = e^{(j\omega T)} = -1$ (i.e., $\omega T = \pi$) is equivalent to selecting the folding frequency $\omega_s/2$, which is the highest frequency allowable without aliasing. Pole-zero matched digital filters can be obtained using the MATLAB command

**>> g = c2d(ga, *T*, 'matched')**

## EXAMPLE 6.7

Find a pole-zero matched digital filter approximation for the analog filter

$$G_a(s) = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

If the damping ratio is equal to 0.5 and the undamped natural frequency is 5 rad/s, determine the transfer function of the digital filter for a sampling period of 0.1 s. Check your answer using MATLAB and obtain the frequency response of the digital filter.

**Solution**

The filter has a zero at the origin and complex conjugate poles at $s_{1,2} = -\zeta\omega_n \pm j\omega_d$. We apply the pole-zero matching transformation to obtain

$$G(z) = \frac{\alpha(z+1)}{z^2 - 2e^{-\zeta\omega_n T}\cos(\omega_d T)z + e^{-2\zeta\omega_n T}}$$

The analog filter has two zeros at infinity, and we choose to add one digital filter zeros at $-1$ for a strictly proper filter. The difference equation for the filter is

$$\begin{aligned} y(k+2) = {} & 2e^{-\zeta\omega_n T}\cos(\omega_d T)y(k+1) - e^{-2\zeta\omega_n T}y(k) \\ & + \alpha(u(k+1) - u(k)) \end{aligned}$$

Thus, the computation of the output only requires values of the input at earlier sampling points, and the filter is easily implementable. The gain $\alpha$ is selected in order for the digital filter to have the same DC gain of the analog filter, which is equal to unity.

For the given numerical values, we have the damping ratio $\omega_d = 5\sqrt{1-0.5^2} = 4.33\ \text{rad}/s$ and the filter transfer function

$$G(z) = \frac{0.09634(z+1)}{z^2 - 1.414z + 0.6065}$$

The following MATLAB commands give the transfer function:

```
>> wn = 5;zeta = 0.5; % Undamped natural frequency, damping ratio
>> ga = tf([wn^2],[1,2*zeta*wn,wn^2]) % Analog transfer function
Transfer function:
25
- - - - - - - - - -
s^2 + 5 s + 25
>> g = c2d(ga,.1,'matched') % Transformation with a sampling period 0.1
Transfer function:
0.09634 z + 0.09634
- - - - - - - - - - - -
z^2 - 1.414 z + 0.6065
Sampling time: 0.1
```

The frequency responses of the analog and digital filters obtained using MATLAB are shown in Figure 6.13. Note that the frequency responses are almost identical in the low frequency range but become different at high frequencies.

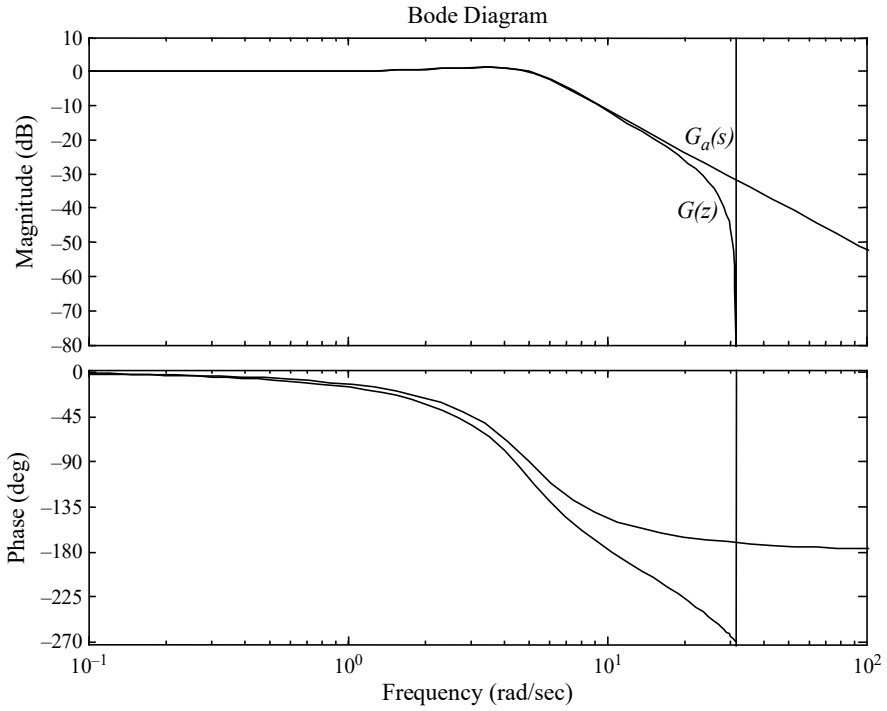


**FIGURE 6.13**

Frequency response of digital filter for Example 6.7.

### 6.3.3 Bilinear transformation

The relationship

$$s = c\frac{z-1}{z+1} \tag{6.22}$$

with a linear numerator and a linear denominator and a constant scale factor $c$ is known as a bilinear transformation. The relationship can be obtained from the equality $z = e^{sT}$ using the first-order approximation

$$s = \frac{1}{T}\ln(z) \cong \frac{2}{T}\left[\frac{z-1}{z+1}\right] \tag{6.23}$$

where the constant $c = 2/T$. A digital filter $C(z)$ is obtained from an analog filter $C_a(s)$ by the substitution

$$C(z) = C_a(s)\Big|_{s=c\left[\frac{z-1}{z+1}\right]} \tag{6.24}$$

The resulting digital filter has the frequency response

$$\begin{aligned} C(e^{j\omega T}) &= C_a(s)\Big|_{s=c\left[\frac{e^{j\omega T}-1}{e^{j\omega T}+1}\right]} \\ &= C_a\left(c\left[\frac{e^{j\omega T/2}-e^{-j\omega T/2}}{e^{j\omega T/2}+e^{-j\omega T/2}}\right]\right) \end{aligned}$$

Thus, the frequency responses of the digital and analog filters are related by

$$C(e^{j\omega T}) = C_a\left(jc\tan\left[\frac{\omega T}{2}\right]\right) \tag{6.25}$$

Evaluating the frequency response at the folding frequency $\omega_s/2$ gives

$$\begin{aligned} C(e^{j\omega_s T/2}) &= C_a\left(jc\tan\left[\frac{\omega_s T}{4}\right]\right) \\ &= C_a\left(jc\tan\left[\frac{2\pi}{4}\right]\right) = C_a(j\infty) \end{aligned}$$

We observe that bilinear mapping squeezes the entire frequency response of the analog filter for a frequency range $0 \to \infty$ into the frequency range $0 \to \omega_s/2$. This implies the absence of aliasing (which makes the bilinear transformation a popular method for digital filter design) but also results in distortion or warping of the

frequency response. The relationship between the frequency $\omega_a$ of the analog filter and the associated frequency $\omega$ of the digital filter for the case $c = 2/T$—namely,

$$\omega_a = \frac{2}{T}\tan\left(\frac{\omega T}{2}\right)$$

is plotted in Figure 6.14 for $T = 1$. Note that, in general, if the sampling period is sufficiently small so that $\omega \ll \pi/T$, then

$$\tan\left(\frac{\omega T}{2}\right) \cong \frac{\omega T}{2}$$

and therefore $\omega_a \approx \omega$, so that the effect of the warping is negligible.

In any case, the distortion of the frequency response can be corrected at a single frequency $\omega_0$ using the *prewarping* equality

$$C(e^{j\omega_0 T}) = C_a\left(jc\tan\left[\frac{\omega_0 T}{2}\right]\right) = C_a(j\omega_0) \tag{6.26}$$

The equality holds provided that the constant $c$ is chosen as

$$c = \frac{\omega_0}{\tan\left(\frac{\omega_0 T}{2}\right)} \tag{6.27}$$

The choice of the prewarping frequency $\omega_0$ depends on the mapped filter. In control applications, a suitable choice of $\omega_0$ is the 3-dB frequency for a PI or PD controller and the upper 3-dB frequency for a PID controller. This is explored further in design examples.

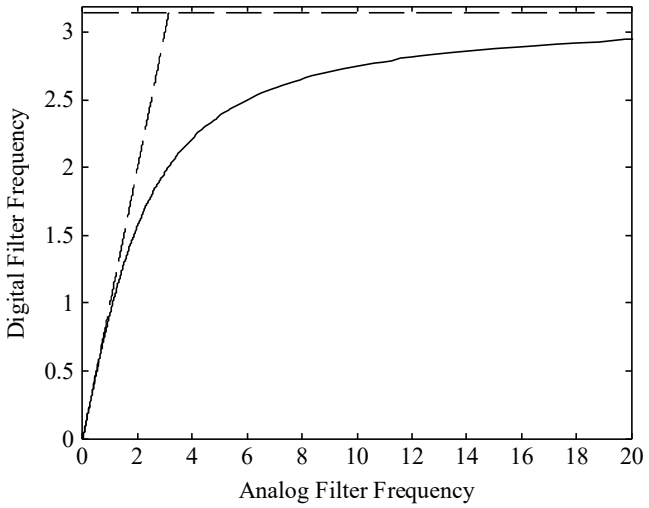


**FIGURE 6.14**

Relationship between analog filter frequencies $\omega_a$ and the associated digital filter frequencies with bilinear transformation.

In MATLAB, the bilinear transformation is accomplished using the following command:

$$\textbf{>> gd = c2d(g, tc, 'tustin')}$$

where **g** is the analog system and **tc** is the sampling period. If prewarping is requested at a frequency **w**, then the command is

$$\textbf{>> gd = c2d(g, tc, 'prewarp', w)}$$

## EXAMPLE 6.8

Design a digital filter by applying the bilinear transformation to the analog filter

$$C_a(s) = \frac{1}{0.1s + 1} \tag{6.28}$$

with $T = 0.1$ s. Examine the warping effect and then apply prewarping at the 3-dB frequency.

**Solution**

By applying the bilinear transformation (6.22) to (6.28), we obtain

$$C(z) = \frac{1}{0.1\frac{2}{0.1}\frac{z-1}{z+1} + 1} = \frac{z+1}{3z-1}$$

The Bode plots of $C_a(s)$ (solid line) and $C(z)$ (dash-dot line) are shown in Figure 6.15, where the warping effect can be evaluated. We select the 3-dB frequency $\omega_0 = 10$ as a prewarping frequency and apply (6.27) to obtain

$$C(z) = \frac{1}{0.1\frac{10}{\tan\left(\frac{10\cdot 0.1}{2}\right)}\frac{z-1}{z+1} + 1} \cong \frac{0.35z + 0.35}{z - 0.29}$$

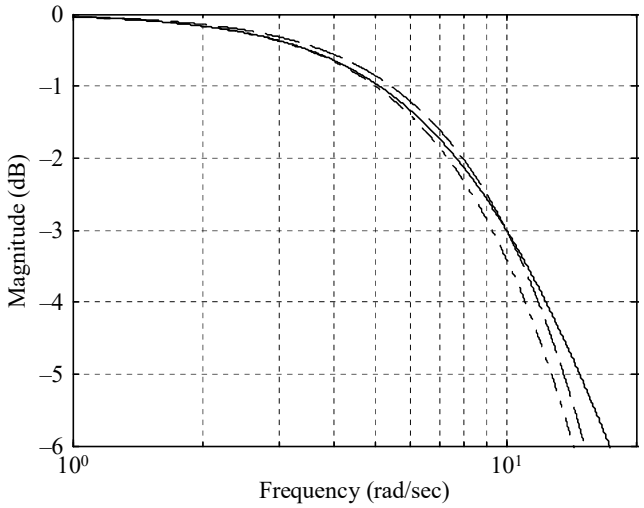


**FIGURE 6.15**

Bode plots of the analog filter (*solid*) and the digital filter obtained with (*dashed*) and without prewarping (*dash-dot*).

The corresponding Bode plot is shown again in Figure 6.15 (dashed line). It coincides with the Bode plot of $C(s)$ at $\omega_0 = 10$. Note that for lower values of the sampling period, the three Bode plots tend to coincide.

Another advantage of bilinear transformation is that it maps points in the LHP to points inside the unit circle and thus guarantees the stability of a digital filter for a stable analog filter. This property was discussed in Section 4.42 and is clearly demonstrated in Figure 4.4.

Bilinear transformation of the analog PI controller gives the following digital PI controller:

$$\begin{aligned} C(z) &= K\frac{(s+a)}{s}\bigg|_{s=c\left[\frac{z-1}{z+1}\right]} \\ &= K\left(\frac{a+c}{c}\right)\frac{z+\left(\frac{a-c}{a+c}\right)}{z-1} \end{aligned} \tag{6.29}$$

The digital PI controller increases the type of the system by one and can therefore be used to improve steady-state error. As in the analog case, it has a zero that reduces the deterioration of the transient response due to the increase in system type. The PI controller of (6.29) has a numerator order equal to its denominator order. Hence, the calculation of its output from its difference equation requires knowledge of the input at the current time. Assuming negligible computational time, the controller is approximately realizable.

Bilinear transformation of the analog PD controller gives the digital PD controller

$$\begin{aligned} C(z) &= K(s+a)\bigg|_{s=c\left[\frac{z-1}{z+1}\right]} \\ &= K(a+c)\frac{z+\left(\frac{a-c}{a+c}\right)}{z+1} \end{aligned} \tag{6.30}$$

This includes a zero that can be used to improve the transient response and a pole at $z = -1$ that occurs because the continuous time system is not proper (see Problem 6.8). A pole at $z = -1$ corresponds to an unbounded frequency response at the folding frequency, as $e^{j\omega_s T/2} = e^{j\pi} = -1$, and must therefore be eliminated. However, eliminating the undesirable pole would result in an unrealizable controller. An approximately realizable PD controller is obtained by replacing the pole at $z = -1$ with a pole at the origin to obtain

$$C(z) = K(a+c)\frac{z+\left(\frac{a-c}{a+c}\right)}{z} \tag{6.31}$$

A pole at the origin is associated with a term that decays as rapidly as possible so as to have the least effect on the controller dynamics. However, this variation from direct transformation results in additional distortion of the analog filter and complication of the digital controller design and doubles the DC gain of the controller. To provide the best approximation of the continuous-time controller, disregarding subsequent gain tuning, the gain $K$ can be halved.

Bilinear transformation of the analog PID controller gives the digital PD controller

$$C(z) = K\frac{(s+a)(s+b)}{s}\bigg|_{s=c\left[\frac{z-1}{z+1}\right]}$$

$$= K\frac{(a+c)(b+c)}{c}\frac{\left[z+\left(\frac{a-c}{a+c}\right)\right]\left[z+\left(\frac{b-c}{b+c}\right)\right]}{(z+1)(z-1)}$$

The controller has two zeros that can be used to improve the transient response and a pole at $z = 1$ to improve the steady-state error. As with PD control, transforming an improper transfer function yields a pole at $z = -1$, which must be replaced by a pole at the origin to yield a transfer function with a bounded frequency response at the folding frequency. The resulting transfer function is approximately realizable and is given by

$$C(z) = K\frac{(a+c)(b+c)}{c}\frac{\left[z+\left(\frac{a-c}{a+c}\right)\right]\left[z+\left(\frac{b-c}{b+c}\right)\right]}{z(z-1)} \tag{6.32}$$

As in the case of PD control, the modification of the bilinearly transformed transfer function results in distortion that can be reduced by halving the gain $K$.

Using Procedure 6.1 and equations (6.29), (6.31), and (6.32), respectively, digital PI, PD, and PID controllers can be designed to yield satisfactory transient and steady-state performance.

## EXAMPLE 6.9

Design a digital controller for a DC motor speed control system (see Example 3.6) where the (type 0) analog plant has the transfer function

$$G(s) = \frac{1}{(s+1)(s+10)}$$

to obtain zero steady-state error due to a unit step, a damping ratio of 0.7, and a settling time of about 1 s.

### Solution

The design is completed following Procedure 6.1. First, an analog controller is designed for the given plant. For zero steady-state error due to unit step, the system type must be increased by one. A PI controller affects this increase, but the location of its zero must be

chosen so as to obtain an acceptable transient response. The simplest possible design is obtained by pole-zero cancellation and is of the form

$$C_a(s) = K\frac{s+1}{s}$$

The corresponding loop gain is

$$C_a(s)G(s) = \frac{K}{s(s+10)}$$

Hence, the closed-loop characteristic equation of the system is

$$s(s+10) + K = s^2 + 2\zeta\omega_n s + \omega_n^2$$

Equating coefficients gives $\zeta\omega_n = 5$ rad/s and the settling time

$$T_s = \frac{4}{\zeta\omega_n} = \frac{4}{5} = 0.8 \text{ s}$$

as required. The damping ratio of the analog system can be set equal to 0.7 by appropriate choice of the gain $K$. The gain selected at this stage must often be tuned after filter transformation to obtain the same damping ratio for the digital controller. We solve for the undamped natural frequency

$$\omega_n = 10/(2\zeta) = 10/(2\times 0.7) = 7.142 \text{ rad/s}$$

The corresponding analog gain is

$$K = \omega_n^2 = 51.02$$

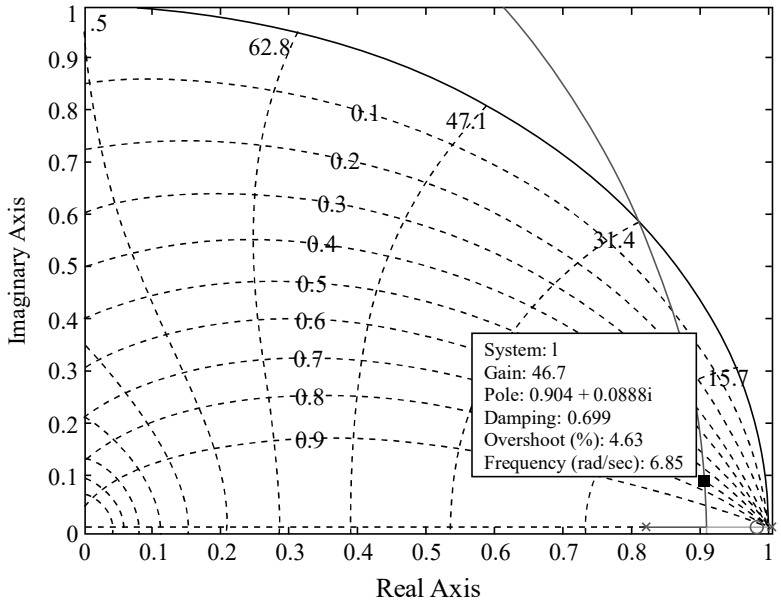


**FIGURE 6.16**

Root locus for PI design.

We therefore have the analog filter

$$C_a(s) = 51.02\frac{s+1}{s}$$

Next, we select a suitable sampling period for an undamped natural frequency of about 7.14 rad/s. We select $T = 0.02\text{ s} < 2\pi/(40\omega_d)$, which corresponds to a sampling frequency higher than 40 times the damped natural frequency (see Chapter 2). The model of the analog plant together with an ADC and sampler is

$$\begin{aligned} G_{ZAS}(z) &= (1-z^{-1})\mathcal{Z}\left\{\frac{G(s)}{s}\right\} \\ &= 1.8604\times 10^{-4}\frac{z+0.9293}{(z-0.8187)(z-0.9802)} \end{aligned}$$

Bilinear transformation of the PI controller, with gain $K$ included as a free parameter, gives

$$C(z) = 1.01K\frac{z-0.9802}{z-1}$$

Because the analog controller was obtained using pole-zero cancellation, near pole-zero cancellation occurs when the digital controller $C(z)$ is multiplied by $G_{ZAS}(z)$. The gain can now be tuned for a damping ratio of 0.7 using a CAD package with the root locus of the loop gain $C(z)G_{ZAS}(z)$. From the root locus, shown in Figure 6.16, at $\zeta = 0.7$, the gain $K$ is about 46.7, excluding the 1.01 gain of $C(z)$ (i.e., a net gain of 47.2). The undamped natural frequency is $\omega_n = 6.85$ rad/s. This yields the approximate settling time

$$\begin{aligned} T_s &= \frac{4}{\zeta\omega_n} = \frac{4}{6.85\times 0.7} \\ &= 0.83\text{ s} \end{aligned}$$

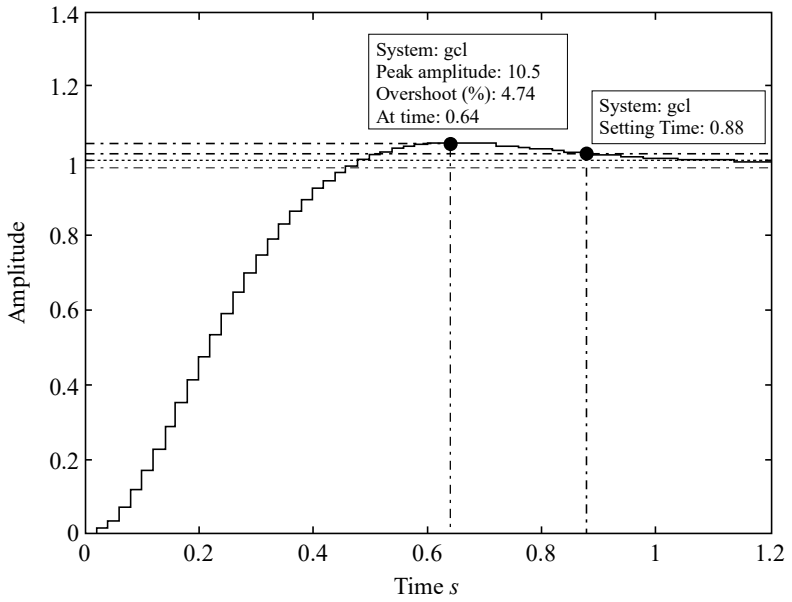


**FIGURE 6.17**

Step response for PI design with $K = 47.2$.

The settling time is acceptable but is slightly worse than the settling time for the analog controller. The step response of the closed-loop digital control system shown in Figure 6.17 is also acceptable and confirms the estimated settling time. The net gain value of 47.2, which meets the design specifications, is significantly less than the gain value of 51.02 for the analog design. This demonstrates the need for tuning the controller gain after mapping the analog controller to a digital controller.

## EXAMPLE 6.10

Design a digital controller for the DC motor position control system of Example 3.6, where the (type 1) analog plant has the transfer function

$$G(s) = \frac{1}{s(s+1)(s+10)}$$

to obtain a settling time of about 1 second and a damping ratio of 0.7.

**Solution**

Using Procedure 6.1, we first observe that an analog PD controller is needed to improve the system transient response. Pole-zero cancellation yields the simple design

$$C_a(s) = K(s+1)$$

We can solve for the undamped natural frequency analytically, or we can use a CAD package to obtain the values $K = 51.02$ and $\omega_n = 7.143$ rad/s for $\zeta = 0.7$.

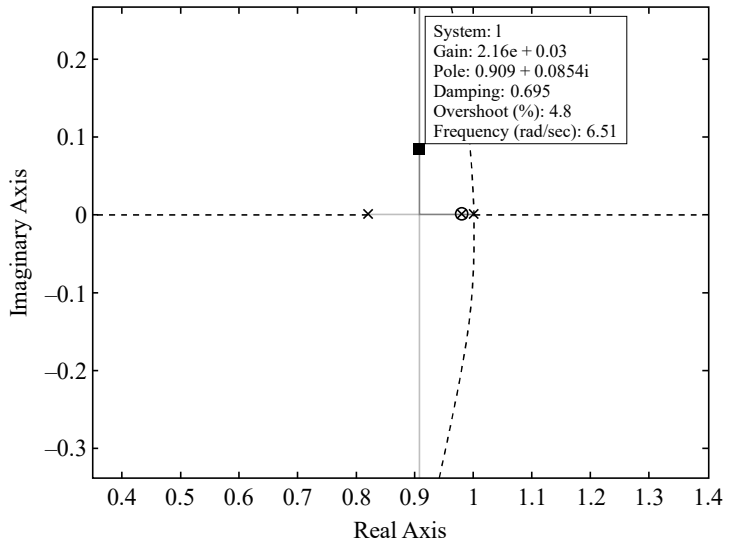


**FIGURE 6.18**

Root locus for PD design.

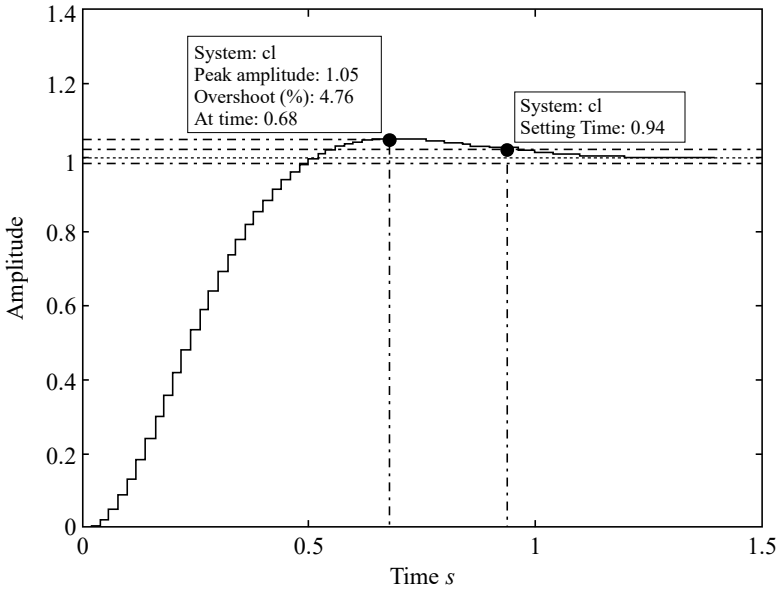


**FIGURE 6.19**

Time step response for PD design with $K = 2{,}160$.

A sampling period of 0.02 s is appropriate because it is less than $2\pi/(40\omega_d)$. The plant with the ADC and DAC has the $z$-transfer function

$$G_{ZAS}(z) = (1 - z^{-1})\mathcal{Z}\left\{\frac{G(s)}{s}\right\} = 1.2629 \times 10^{-6}\frac{(z + 0.2534)(z + 3.535)}{(z - 1)(z - 0.8187)(z - 0.9802)}$$

Bilinear transformation of the PD controller gives

$$C(z) = K\frac{z - 0.9802}{z} = K(1 - 0.9802z^{-1})$$

The root locus of the system with PD control (Figure 6.18) gives a gain $K$ of 2,160 and an undamped natural frequency of 6.51 rad/s at a damping ratio $\zeta = 0.7$. The settling time for this design is about

$$T_s = \frac{4}{\zeta\omega_n} = \frac{4}{0.7 \times 6.51} = 0.88\ s$$

which meets the design specifications.

Checking the step response with MATLAB gives Figure 6.19 with a settling time of 0.94 s, a peak time of 0.68 s, and a 5% overshoot. The time response shows a slight deterioration from the characteristics of the analog system but meets all the design specifications. In some cases, the deterioration may necessitate repeatedly modifying the digital design or modifying the analog design and then mapping it to the $z$-domain until the resulting digital filter meets the desired specifications.

Note that for a prewarping frequency $\omega_0 = 1$ rad/s, the 3-dB frequency of the PD controller, $\omega_0 T = 0.02$ rad and $\tan(\omega_0 T/2) = \tan(0.01) \cong 0.01$. Hence, equation (6.25) is approximately valid without prewarping, and prewarping has a negligible effect on the design.

## EXAMPLE 6.11

Design a digital controller for a speed control system, where the analog plant has transfer function

$$G(s) = \frac{1}{(s+1)(s+3)}$$

to obtain a time constant of less than 0.3 second, a dominant pole damping ratio of at least 0.7, and zero steady-state error due to a step input.

**Solution**

The root locus of the analog system is shown in Figure 6.20. To obtain zero steady-state error due to a step input, the system type must be increased to one by adding an integrator in the forward path. However, adding an integrator results in significant deterioration of the time response or in instability. If the pole at $-1$ is canceled, the resulting system is stable but has $\zeta\omega_n = 1.5$—that is, a time constant of 2/3 s and not less than 0.3 s as specified. Using a PID controller provides an additional zero that can be used to stabilize the system and satisfy the remaining design requirements.

For a time constant $\tau$ of 0.3 s, we have $\zeta\omega_n = 1/\tau \geq 3.33$ rad/s. A choice of $\zeta = 0.7$ and $\omega_n$ of about 6 rad/s meets the design specifications. The design appears conservative, but we choose a larger undamped natural frequency than the minimum needed in anticipation of the deterioration due to adding PI control. We first design a PD controller to meet these specifications using MATLAB. We obtain the controller angle of about 52.4° using the angle condition. The corresponding zero location is

$$a = \frac{6\sqrt{1-(0.7)^2}}{\tan(52.4^\circ)} + (0.7)(6) \cong 7.5$$

The root locus for the system with PD control (Figure 6.21) shows that the system with $\zeta = 0.7$ has $\omega_n$ of about 6 rad/s and meets the transient response specifications with a gain

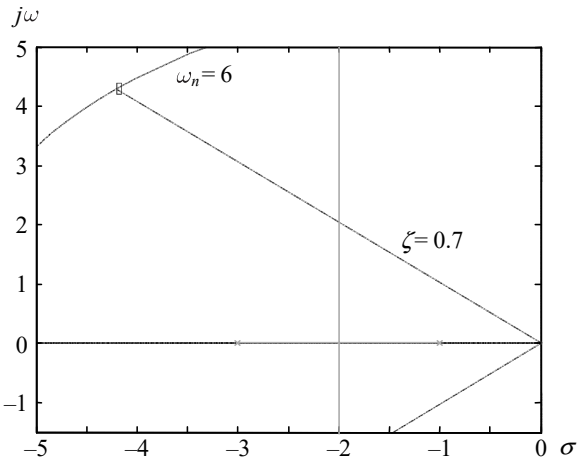


**FIGURE 6.20**

Root locus for the analog speed control system.

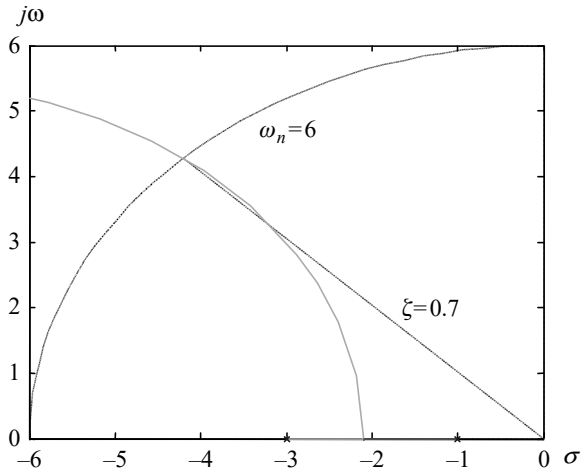


**FIGURE 6.21**

Root locus of a PD-controlled system.

of 4.4 and $\zeta\omega_n = 4.2$. Following the PI-design procedure, we place the second zero of the PID controller at one-tenth this distance from the $j\omega$ axis to obtain

$$C_a(s) = K\frac{(s+0.4)(s+7.5)}{s}$$

To complete the analog PID design, the gain must be tuned to ensure that $\zeta = 0.7$. Although this step is not needed, we determine the gain $K \approx 5.8$, and $\omega_n = 6.7$ rad/s (Figure 6.22) for later comparison to the actual gain value used in the digital design. The analog design meets the transient response specification with $\zeta\omega_n = 4.69 > 3.33$, and the dynamics allow us to choose a sampling period of 0.025 s ($\omega_s > 50\omega_d$).

The model of the analog plant with DAC and ADC is

$$G_{ZAS}(z) = (1-z^{-1})\mathcal{Z}\left\{\frac{G(s)}{s}\right\}$$
$$= 1.170\times 10^{-3}\frac{z+0.936}{(z-0.861)(z-0.951)}$$

Bilinear transformation and elimination of the pole at $-1$ yields the digital PID controller

$$C(z) = 47.975K\frac{(z-0.684)(z-0.980)}{z(z-1)}$$

The root locus for the system with digital PID control is shown in Figure 6.23, and the system is seen to be **minimum phase** (i.e., its zeros are inside the unit circle).

For design purposes, we zoom in on the most significant portion of the root locus and obtain the plot of Figure 6.24. With $K = 9.62, 13.2$, the system has $\zeta = 0.7, 0.5$, and $\omega_n = 43.2, 46.2$ rad/s, respectively. Both designs have a sufficiently fast time constant, but the second damping ratio is less than the specified value of 0.7. The time response of the two digital systems and for analog control with $K = 100$ are shown in Figure 6.25. Lower gains give an unacceptably slow analog design. The time response for the high-gain digital design is very fast. However, it has an overshoot of over 4% but has a settling time of 5.63 s. The digital design for $\zeta = 0.7$ has a much slower time response than its analog counterpart.

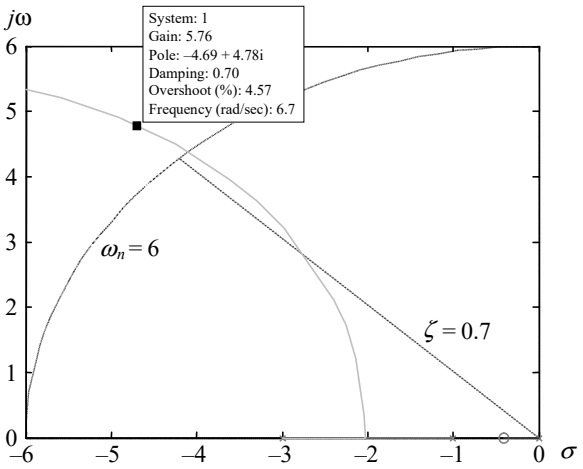


**FIGURE 6.22**

Root locus of an analog system with PID control.

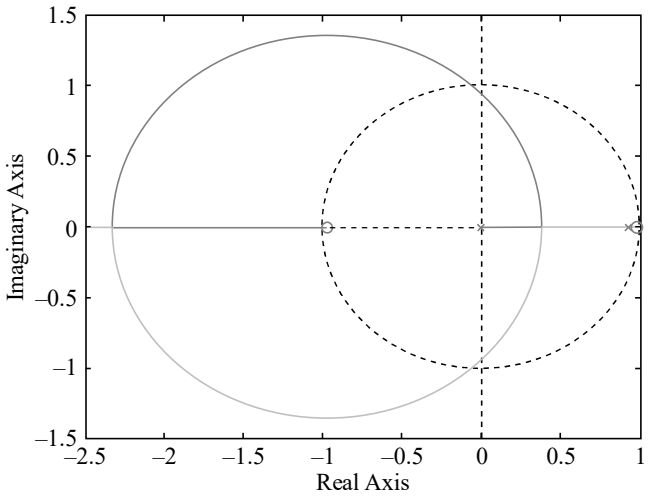


**FIGURE 6.23**

Root locus of a system with digital PID control.

It is possible to improve the design by trial and error, including redesign of the analog controller, but the design with $\zeta = 0.5$ may be acceptable. One must weigh the cost of redesign against that of relaxing the design specifications for the particular application at hand. The final design must be a compromise between speed of response and relative stability.

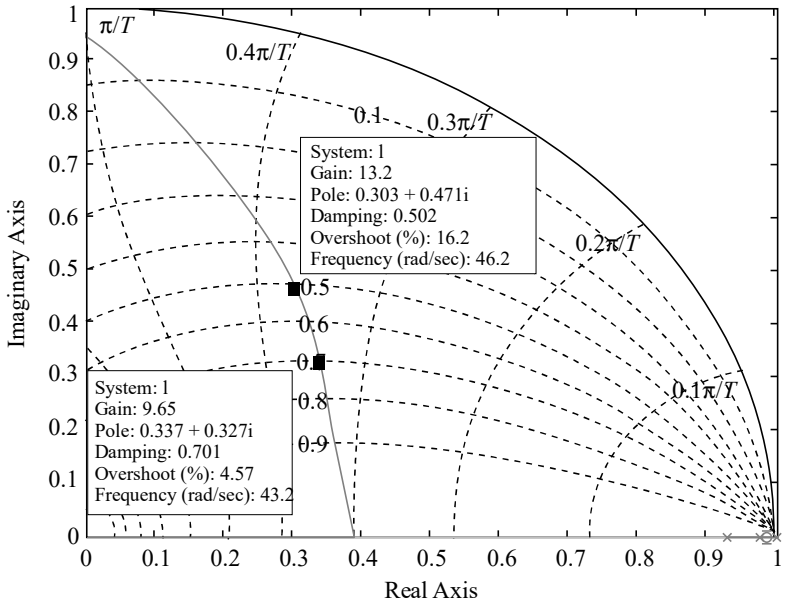


**FIGURE 6.24**

Detail of the root locus of a system with digital PID control.

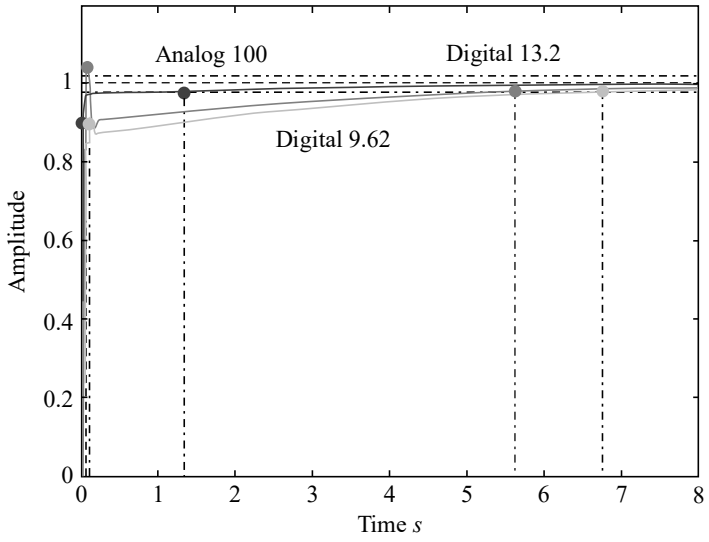


**FIGURE 6.25**

Time step response for the digital PID design with $K = 9.62$ (*light gray*), $K = 13.2$ (*dark gray*), and for analog design (*black*).

### 6.3.4 Empirical digital PID controller tuning

As explained in Section 5.5, the parameters of a PID controller are often selected by means of tuning rules. This concept can also be exploited to design a digital PID controller. The reader can show (Problem 6.7) that bilinear transformation of the PID controller expression (5.20) yields

$$C(z) = K_p\left(1 + \frac{1}{T_i}\frac{T}{2}\frac{z+1}{z-1} + T_d\frac{2}{T}\frac{z-1}{z+1}\right) \tag{6.33}$$

Bilinear transformation of the PID controller results in a pole at $z = -1$ because the derivative part is not proper (see Section 12.4.1). As in Section 6.3.3, we avoid an unbounded frequency response at the folding frequency by replacing the pole at $z = -1$ with a pole at $z = 0$ and dividing the gain by two. The resulting transfer function is

$$C(z) = \frac{K_p}{2}\left(1 + \frac{T}{2T_i}\frac{z+1}{z-1} + \frac{2T_d}{T}\frac{z-1}{z}\right)$$

If parameters $K_p$, $T_i$, and $T_d$ are obtained by means of a tuning rule as in the analog case, then the expression of the digital controller is obtained by substituting in the previous expression. The transfer function of a zero-order hold can be approximated by truncating the series expansions as

$$G_{ZOH}(s) = \frac{1 - e^{-sT}}{s} \cong \frac{1 - 1 + Ts - (Ts)^2/2 + \cdots}{Ts} = 1 - \frac{Ts}{2} + \cdots \cong e^{-\frac{T}{2}s}$$

Thus, the presence of the *ZOH* can be considered as an additional time delay equal to half of the sampling period. The tuning rules of Table 5.1 can then be applied to a system with a delay equal to the sum of the process time delay and a delay of $T/2$ due to the zero-order hold.

---

**EXAMPLE 6.12**

Design a digital PID controller with sampling period $T = 0.1$ for the analog plant of Example 5.9

$$G(s) = \frac{1}{(s+1)^4}e^{-0.2s}$$

by applying the Ziegler-Nichols tuning rules of Table 5.1.

**Solution**

A first-order-plus-dead-time model of the plant was obtained in Example 5.9 using the tangent method with gain c$K = 1$, a dominant time constant $t = 3$, and an apparent time delay $L = 1.55$. The apparent time delay for digital control is obtained by adding half of the value of the sampling period (0.05). This gives $L = 1.55 + 0.05 = 1.6$. The application of the tuning rules of Table 5.1 yields

$$K_p = 1.2\frac{\tau}{KL} = 2.25$$
$$T_i = 2L = 3.2$$
$$T_d = 0.5L = 0.8$$

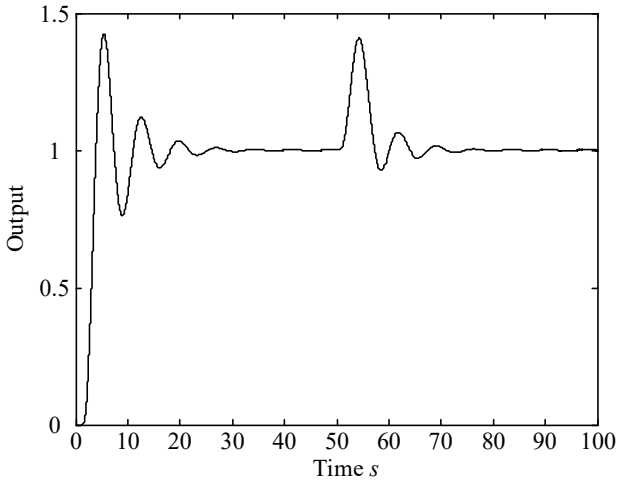


**FIGURE 6.26**

Process output with the digital PID controller tuned with the Ziegler-Nichols method.

Thus, the digital PID controller has the transfer function

$$C(z) = \frac{19.145z^2 - 35.965z + 16.895}{z(z-1)}$$

The response of the digital control system due to a unit step reference input applied at time $t = 0$ and to a unit step change in the control variable at time $t = 50$ is shown in Figure 6.26. The response is similar to the result obtained with the analog PID controller in Example 5.9.

## 6.4 Direct *z*-domain digital controller design

Obtaining digital controllers from analog designs involves approximation that may result in significant controller distortion. In addition, the locations of the controller poles and zeros are often restricted to subsets of the unit circle. For example, bilinear transformation of the term $(s + a)$ gives $[z - (c - a)/(c + a)]$, as seen from (6.29) through (6.32). This yields only RHP zeros because $a$ is almost always smaller than $c$. The plant poles are governed by $p_z = e^{p_s T}$, where $p_s$ and $p_z$ are the $s$-domain and $z$-domain poles, respectively, and can be canceled with RHP zeros. Nevertheless, the restrictions on the poles and zeros in (6.29) through (6.32) limit the designer's ability to reshape the system root locus.

Another complication in digital approximation of analog filters is the need to have a pole at 0 in place of the pole at $-1$, as obtained by direct digital transformation, to avoid an unbounded frequency response at the folding frequency. This may result in a significant difference between the digital and analog controllers and may complicate the design process considerably.