PSI2662 – Projeto em Sistemas Eletrônicos Embarcados: Sensores e Atuadores

Timers

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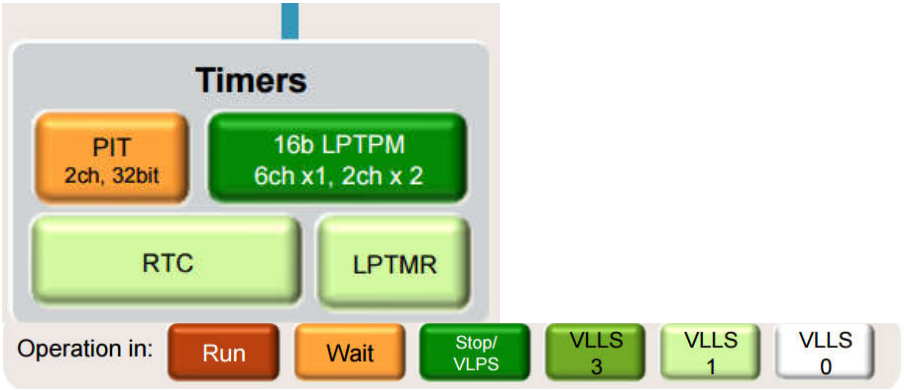
Timers no KL25Z



- PIT - Periodic Interrupt Timer
  - Gera interrupções periódicas.
- TPM - Timer/PWM Module
  - Conectado a portas de I/O; possui input capture, output compare, pode gerar sinais de PWM; pode gerar interrupções.
- LPTMR - Low-Power Timer
  - Pode operar como timer ou contador in todos os modos de potência; pode "acordar" o sistema com interrupções; pode sincronizar o hardware.
- Real-Time Clock
  - Alimentado por um cristal externo de 32.768 kHz; rastreia tempo em segudos utilizando um registrador de 32 bits; pode gerar um alarme; pode gerar um sinal de 1 Hz e/ou uma interrupção; pode "acordar o sistema com interrupção.
- SYSTICK
  - Parte do Cortex M0+ Core; contador que pode gerar interrupções

Timer/PWM Module

- 3 módulos (TPMx = TPM0, TPM1 e TPM2)
  - 1 com 6 canais e 2 com 2 canais
  - Contador de 16 bits (up ou down)
  - Modos: Output Compare, Input Capture e PWM

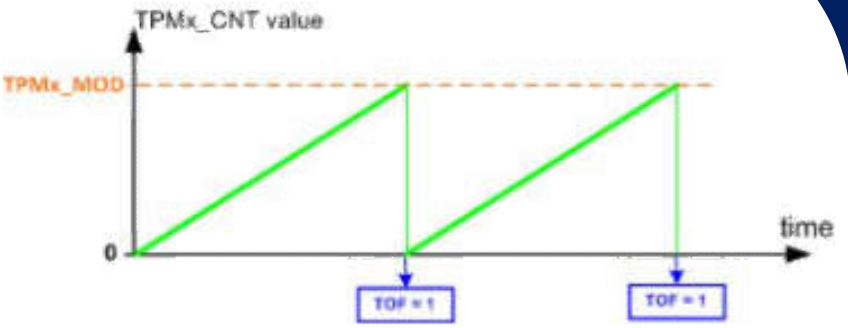


Figure 5-16: The role of TPMx_MOD

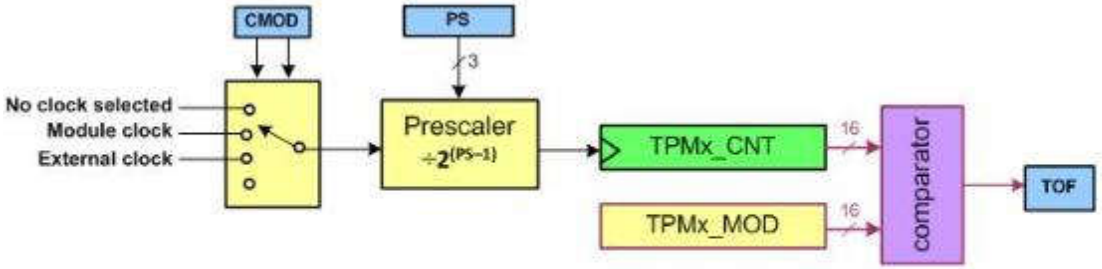
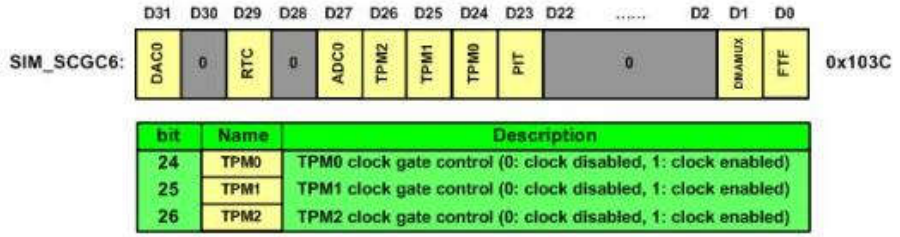


Figure 5-17: CMOD and PS (Prescaler) bits



bit	Name	Description
24	TPM0	TPM0 clock gate control (0: clock disabled, 1: clock enabled)
25	TPM1	TPM1 clock gate control (0: clock disabled, 1: clock enabled)
26	TPM2	TPM2 clock gate control (0: clock disabled, 1: clock enabled)

Figure 5-11: SIM_SCGC6 (SIM Clock Gating Control Register 6)

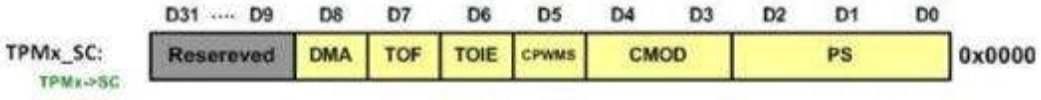
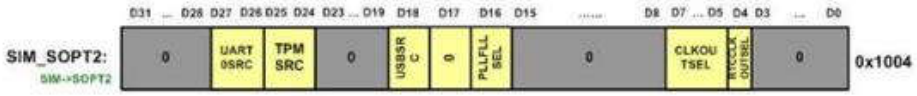


Figure 5-18: Timer Status and Control (TPMx_SC) Register



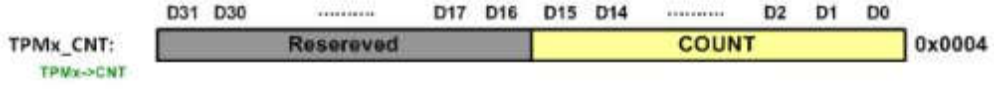


Figure 5-13: TPMx_CNT Register

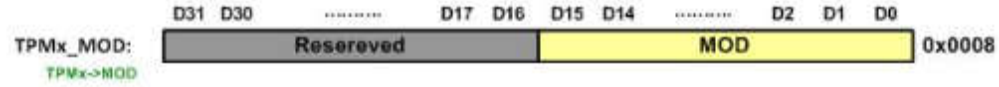


Figure 5-14: TPMx_CNT and TPMX_MOD registers

TPM clock source select selects the clock source for the TPM counter clock

TPMSRC	Selected Clock
00	Clock disabled
01	MCGFLLCLK clock or MCGFLLCLK/2
10	OSCERCLK clock
11	MCGIRCLK clock

Figure 5-12: SIM_SOPT2 (System Options 2)

TPM Output Compare

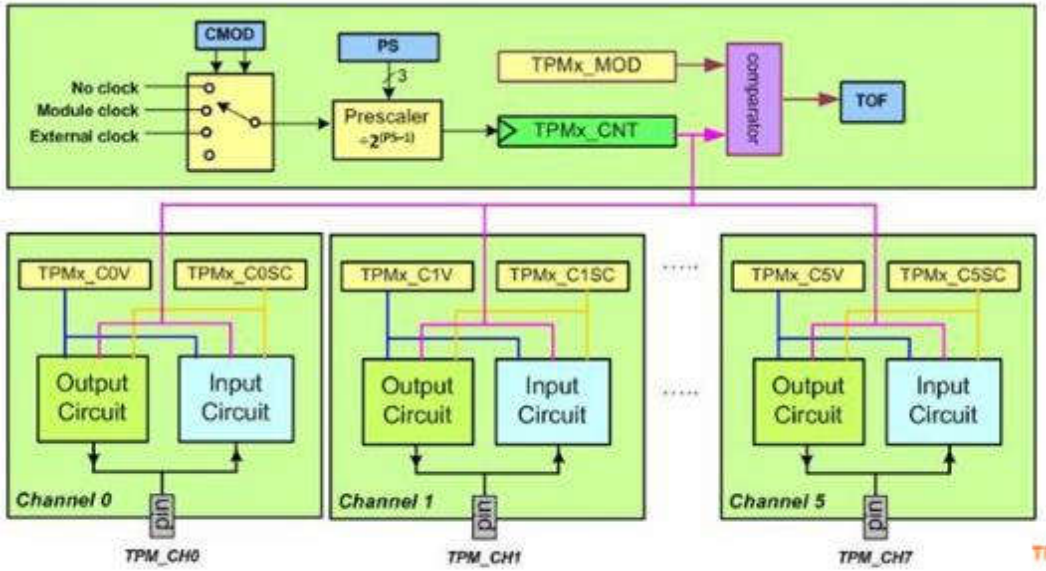


Figure 5-19: The Channels of TPMx

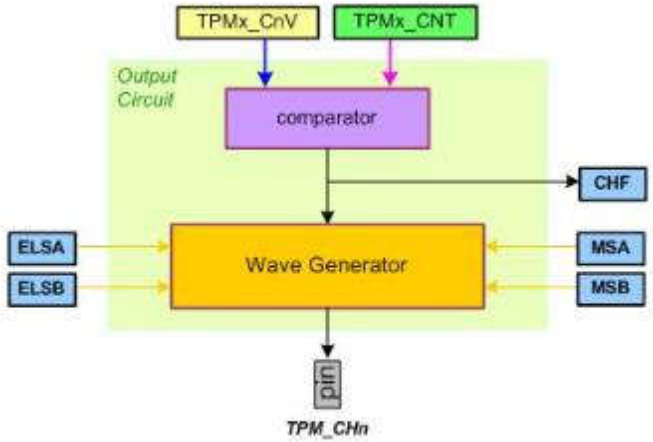


Figure 5-21: Output Circuit

Figure 5-20: TPMx_CnV (TPMx Channel Value) Register

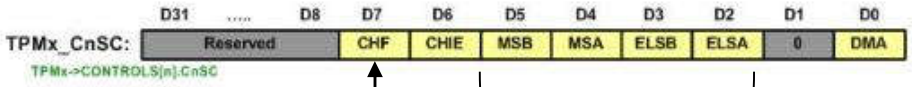


Figure 5-22: TPMxCnSC (TPMx Channel Status and Control)

Flag

Configuração da Saída

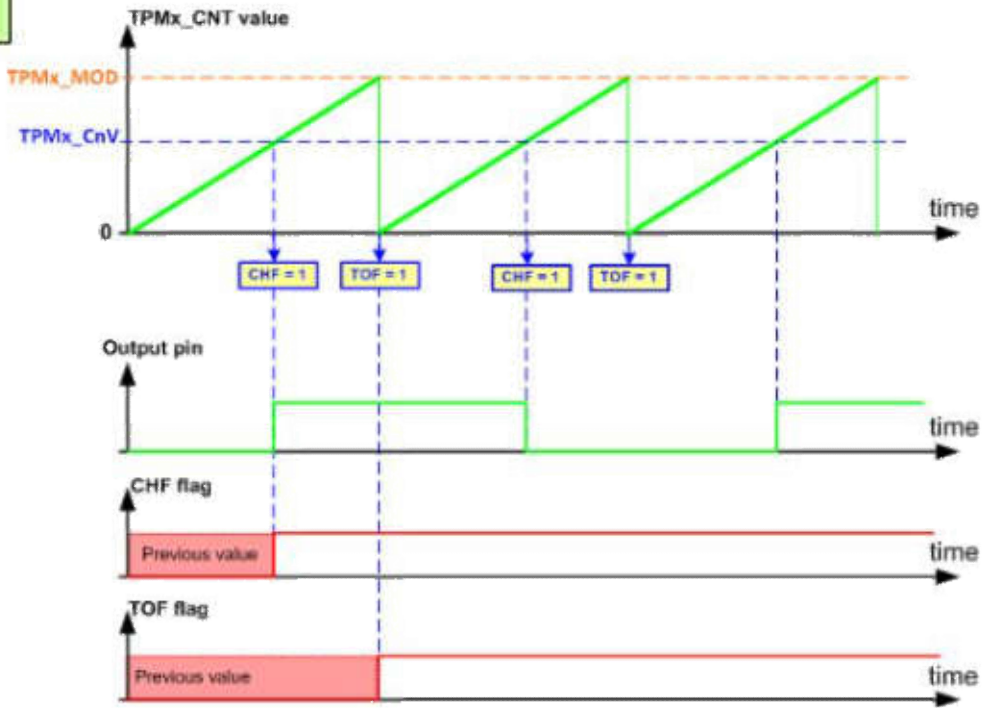


Figure 5-23: In Toggle Mode

Input Capture

Frequência e Largura de Pulso

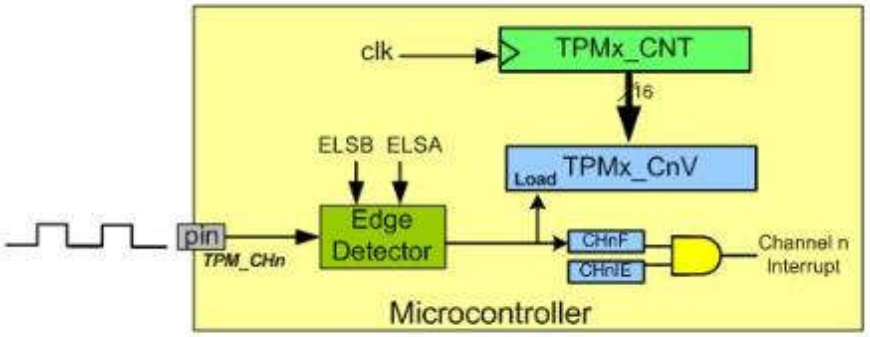
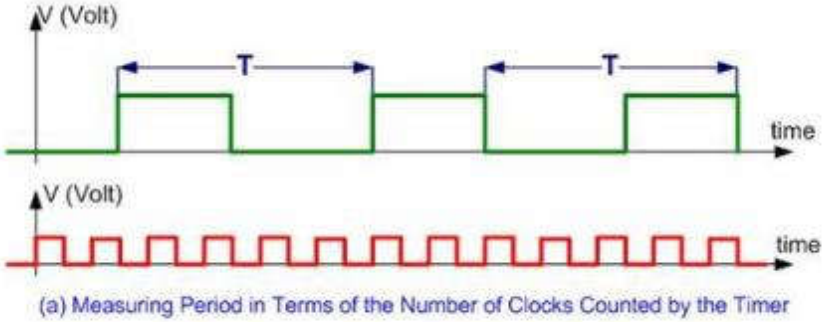
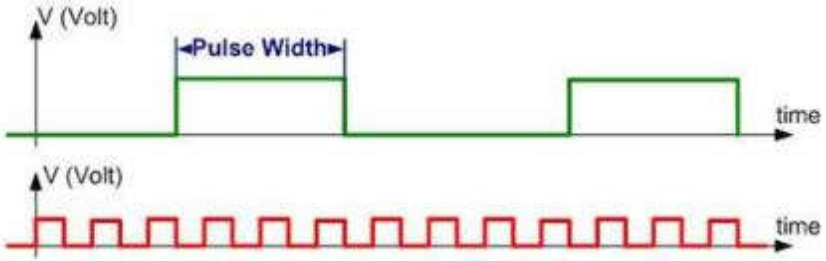


Figure 5-27: Input Edge Time Capturing



(a) Measuring Period in Terms of the Number of Clocks Counted by the Timer



(b) Measuring Pulse Width in Terms of the Number of Clocks Counted by the Timer

Figure 5-28: Measuring Period and Pulse Width

Eventos

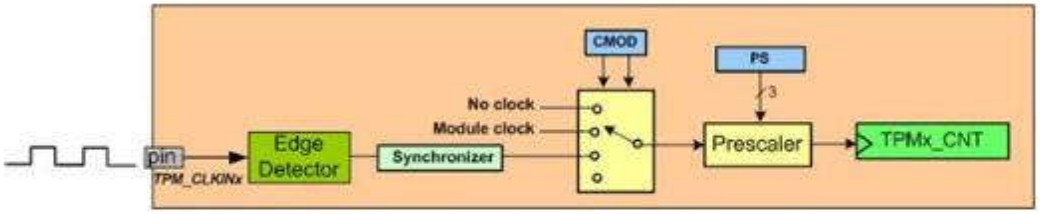


Figure 5-29: Counter Diagram

→ Interrupção