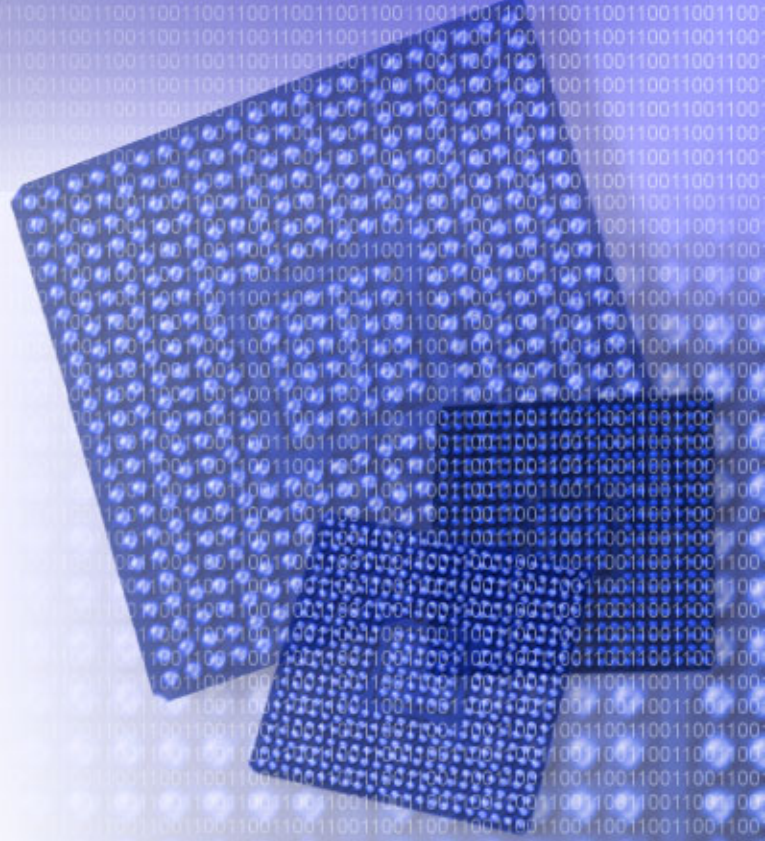
SEL–0629

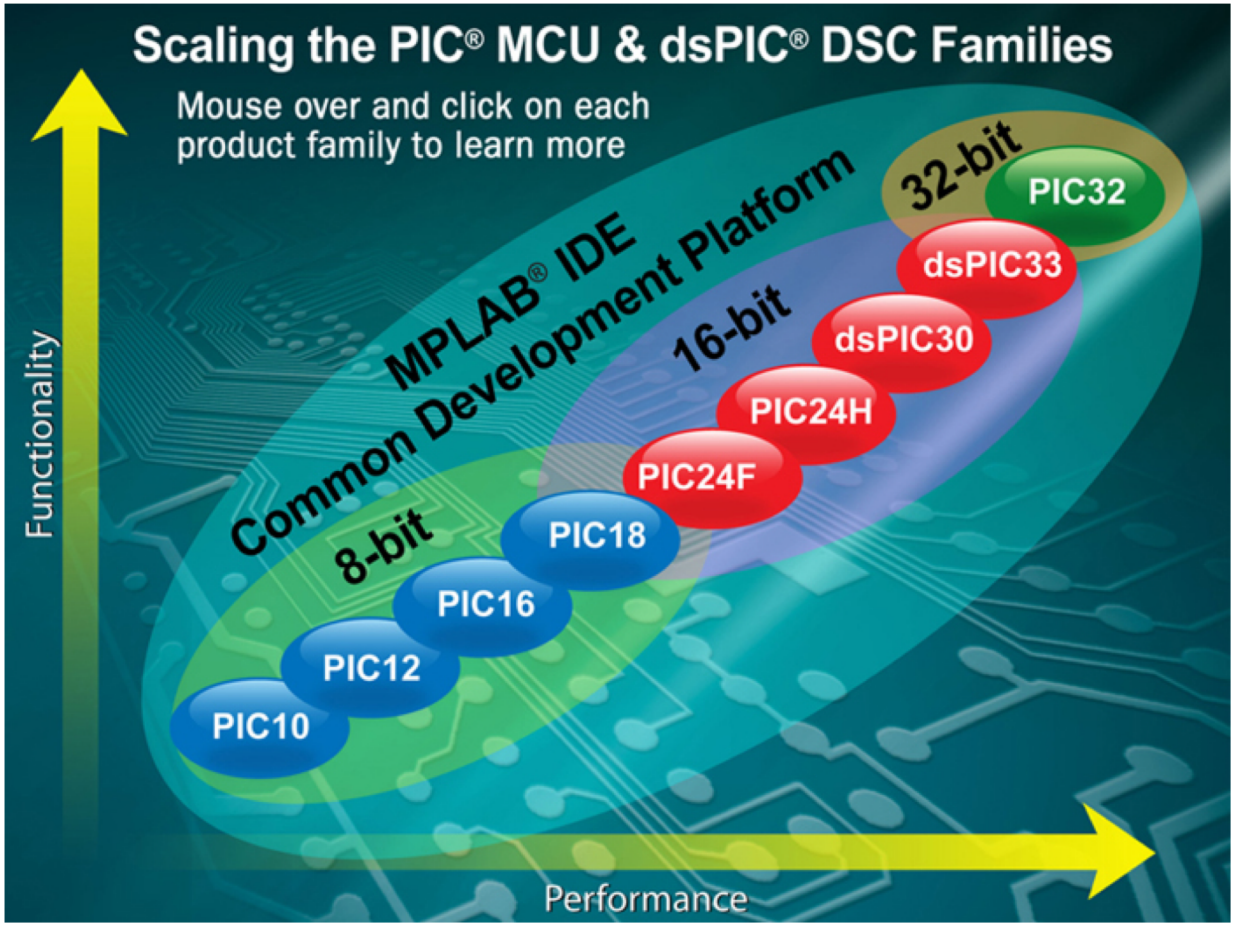
Aplicação de Microprocessadores I

Aula 2b
PIC 18F4550

Marcelo Andrade da Costa Vieira



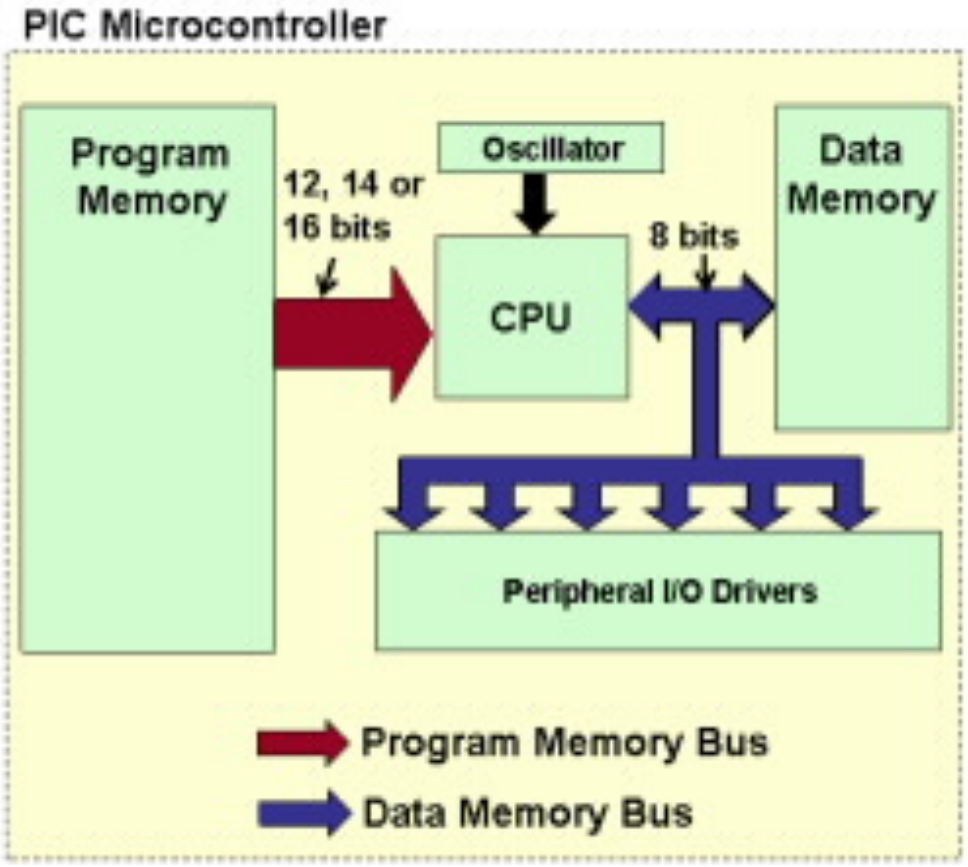
Família de Microcontroladores PIC



- Microprocessadores de 8-bit, 16-bit e 32-bit;
- A linha de 32-bit possui ULA de 32-bit, clock de até 200 MHZ e Pipeline de 5 estágios

Família PIC de 8-bits

Classificados de acordo com o tamanho do barramento de instruções. Isso define o tamanho da palavra de instruções, o número de instruções e a sua velocidade



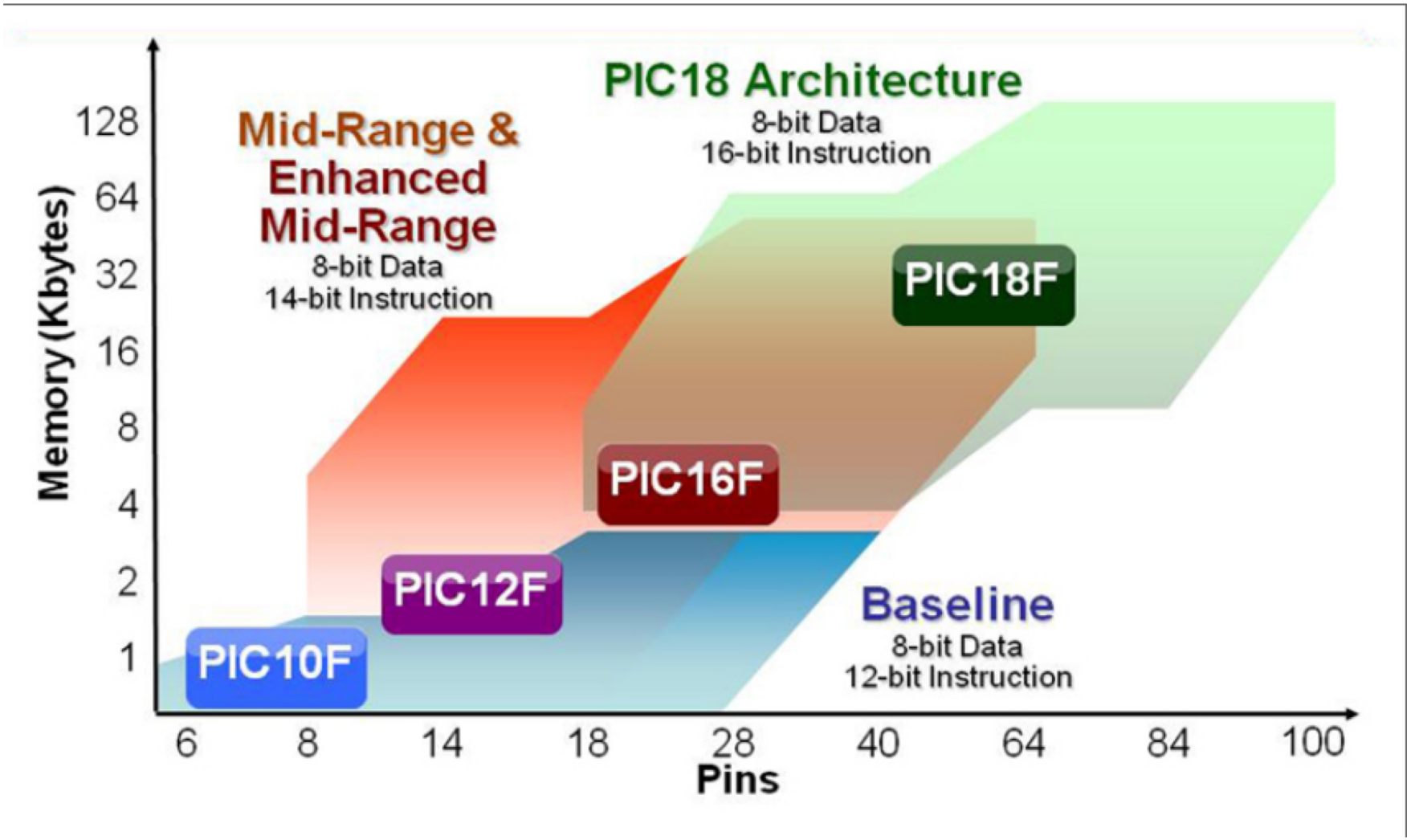
1. Baseline: 12-bits
2. Mid-range: 14-bits
1. Enhanced Mid-range: 14-bits
2. High-performance: 16-bits

Família PIC de 8-bits

Compare 8-bit PIC® MCU Architectures

	Baseline Architecture	Mid-Range Architecture	Enhanced Mid-Range Architecture	PIC18 Architecture
Pin Count	6-40	8-64	8-64	18-100
Interrupts	No	Single interrupt capability	Single interrupt capability with hardware context save	Multiple interrupt capability with hardware context save
Performance	5 MIPS	5 MIPS	8 MIPS	Up to 16 MIPS
Instructions	33, 12-bit	35, 14-bit	49, 14-bit	83, 16-bit
Program Memory	Up to 3 KB	Up to 14 KB	Up to 28 KB	Up to 128 KB
Data Memory	Up to 138 Bytes	Up to 368 Bytes	Up to 1,5 KB	Up to 4 KB
Hardware Stack	2 level	8 level	16 level	32 level
Features	▪ Comparator ▪ 8-bit ADC ▪ Data Memory ▪ Internal Oscillator	In addition to Baseline: ▪ SPI/I²C™ ▪ UART ▪ PWMs ▪ LCD ▪ 10-bit ADC ▪ Op Amp	In addition to Mid-Range: ▪ Multiple Communication Peripherals ▪ Linear Programming Space ▪ PWMs with Independent Time Base	In addition to Enhanced Mid-Range: ▪ 8x8 Hardware Multiplier ▪ CAN ▪ CTMU ▪ USB ▪ Ethernet ▪ 12-bit ADC
Highlights	Lowest cost in the smallest form factor	Optimal cost to performance ratio	Cost effective with more performance and memory	High performance, optimized for C programming, advanced peripherals
Total Number of Devices	16	58	29	193
Families	PIC10, PIC12, PIC16	PIC12, PIC16	PIC12FXXX, PIC16F1XX	PIC18

Família PIC de 8 Bits

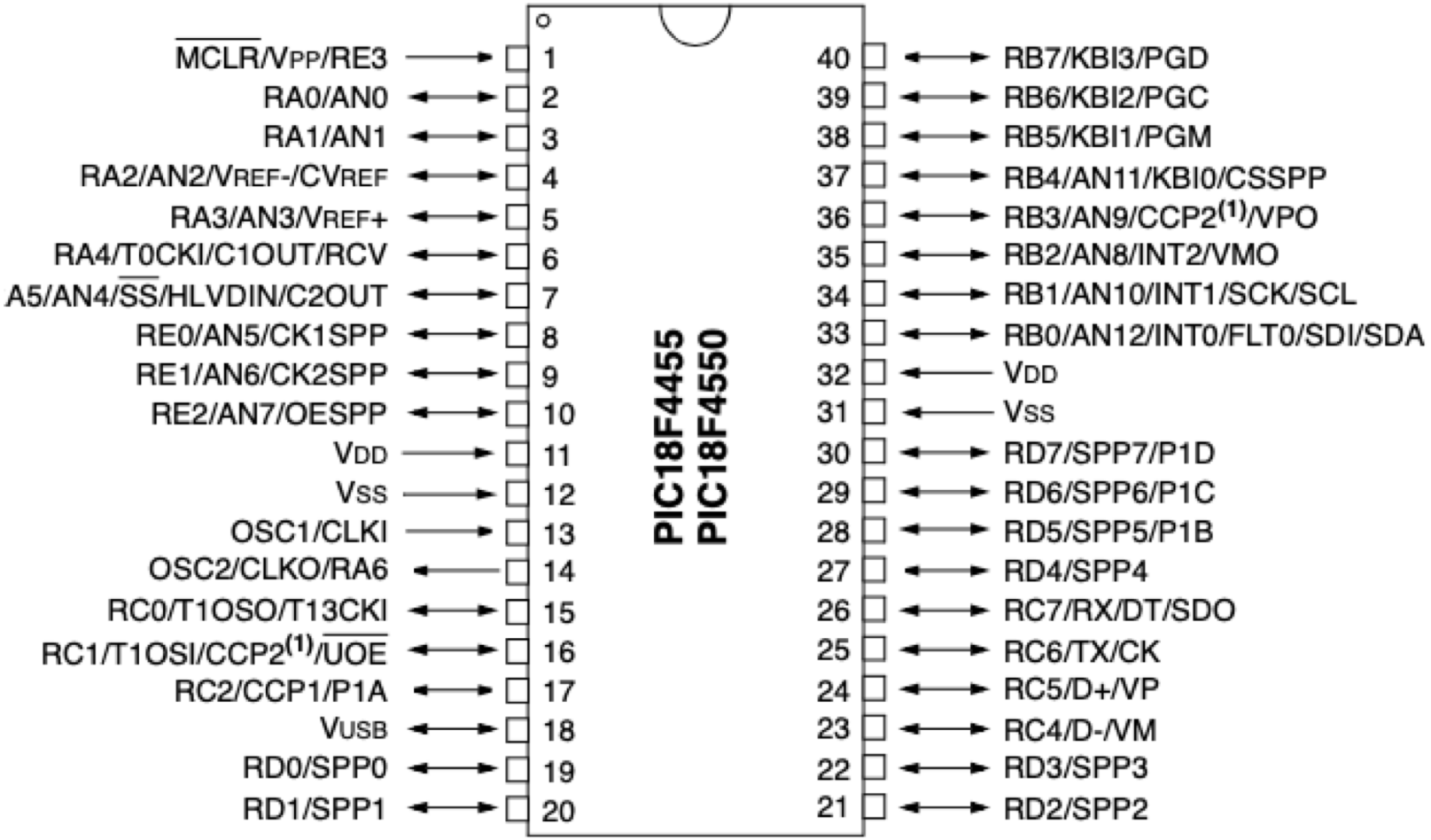


PIC 18F4550

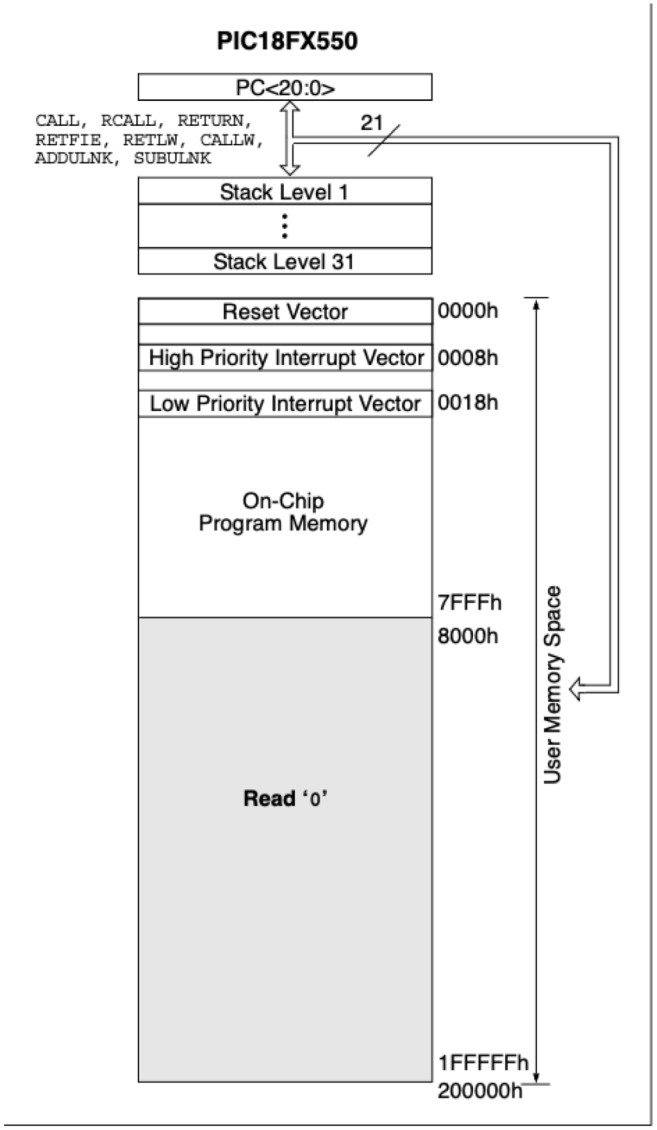
PIC 18F4550

- Memória de Instruções de 16K x **16 bits** (High-Performance) – FLASH – 32KB
- Memória de dados (SRAM) com 2 *Kbytes* de uso geral – endereçamento de 12 bits (4096 bytes) divididos em 16 bancos de 256 bytes cada;
- 40 pinos – 35 portas de I/O configuráveis como entrada ou saída;
- Memória adicional interna do tipo EEPROM não volátil de 256*bytes*;
- 20 fontes de interrupções diferentes com 2 níveis de prioridade;
- Programação com 75 instruções (otimizadas para C)
- Frequência máxima de operação de até 48 MHz (12 MIPS)
- Pilha (*Stack*) de 31 posições;
- Periféricos: 4 Timers, PWM, Conversor A/D, USB, etc...
- Multiplicador 8 x 8 de um ciclo de máquina.

PIC 18F4550

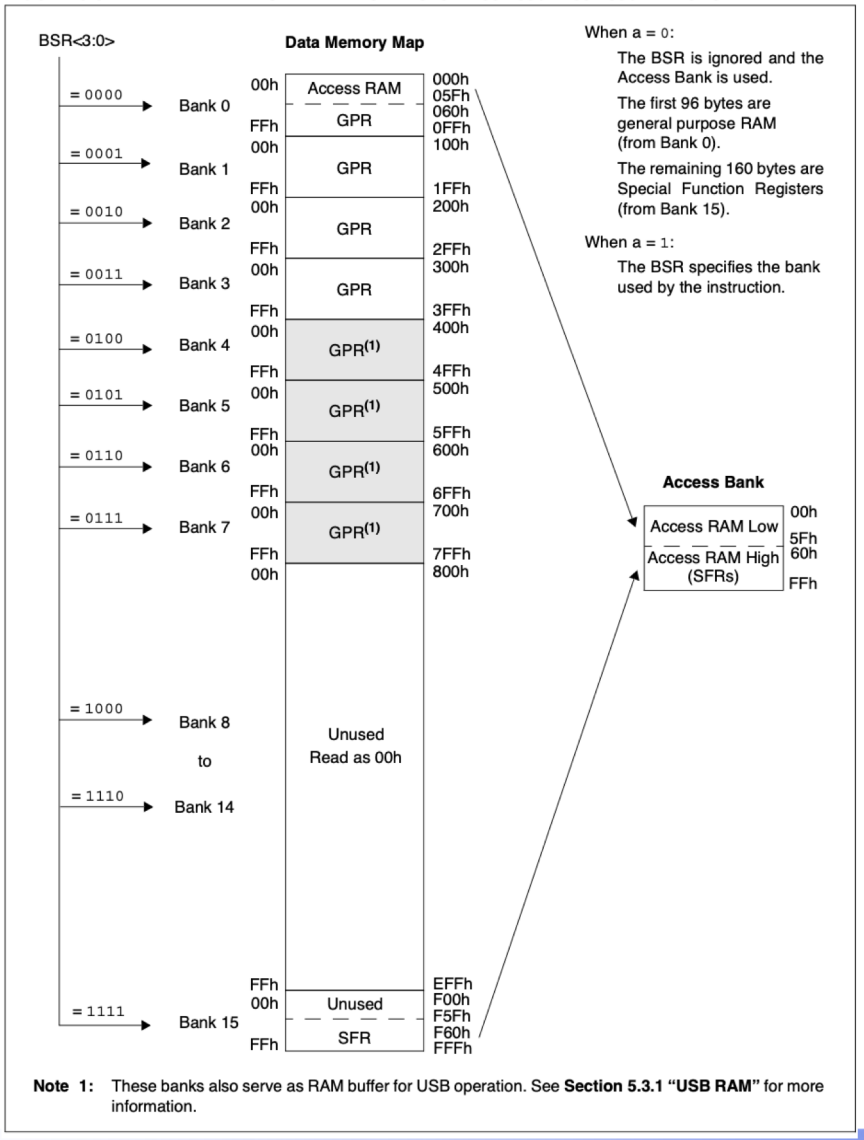

PIC18F4455
PIC18F4550
MCLR/VPP/RE3 1
RA0/AN0 2
RA1/AN1 3
RA2/AN2/VREF-/CVREF 4
RA3/AN3/VREF+ 5
RA4/T0CKI/C1OUT/RCV 6
A5/AN4/SS/HLVDIN/C2OUT 7
RE0/AN5/CK1SPP 8
RE1/AN6/CK2SPP 9
RE2/AN7/OESPP 10
VDD 11
VSS 12
OSC1/CLKI 13
OSC2/CLKO/RA6 14
RC0/T1OSO/T13CKI 15
RC1/T1OSI/CCP2(1)/UOE 16
RC2/CCP1/P1A 17
VUSB 18
RD0/SPP0 19
RD1/SPP1 20
40 RB7/KBI3/PGD
39 RB6/KBI2/PGC
38 RB5/KBI1/PGM
37 RB4/AN11/KBI0/CSSPP
36 RB3/AN9/CCP2(1)/VPO
35 RB2/AN8/INT2/VMO
34 RB1/AN10/INT1/SCK/SCL
33 RB0/AN12/INT0/FLT0/SDI/SDA
32 VDD
31 VSS
30 RD7/SPP7/P1D
29 RD6/SPP6/P1C
28 RD5/SPP5/P1B
27 RD4/SPP4
26 RC7/RX/DT/SDO
25 RC6/TX/CK
24 RC5/D+/VP
23 RC4/D-/VM
22 RD3/SPP3
21 RD2/SPP2

Memória de Programa



Memória RAM

FIGURE 5-5: DATA MEMORY MAP FOR PIC18F2455/2550/4455/4550 DEVICES



Note 1: These banks also serve as RAM buffer for USB operation. See **Section 5.3.1 "USB RAM"** for more information.

- Memória de dados de 2K x **8 bits;**
- Endereçado por duto de 12 bits (4096 bytes);
- 16 bancos de 256 bytes cada;
- Registrador BSR para seleção do banco:
  - 4 bits do BSR (MSB)
  - 8 bits da instrução (LSB)
- 256 bytes de acesso direto (0 e 15)
  - (GPR + SFR)
- Seleção na instrução se o acesso é direto (a = 0) ou via banco (a = 1).

SFR

TABLE 5-1: SPECIAL FUNCTION REGISTER MAP FOR PIC18F2455/2550/4455/4550 DEVICES

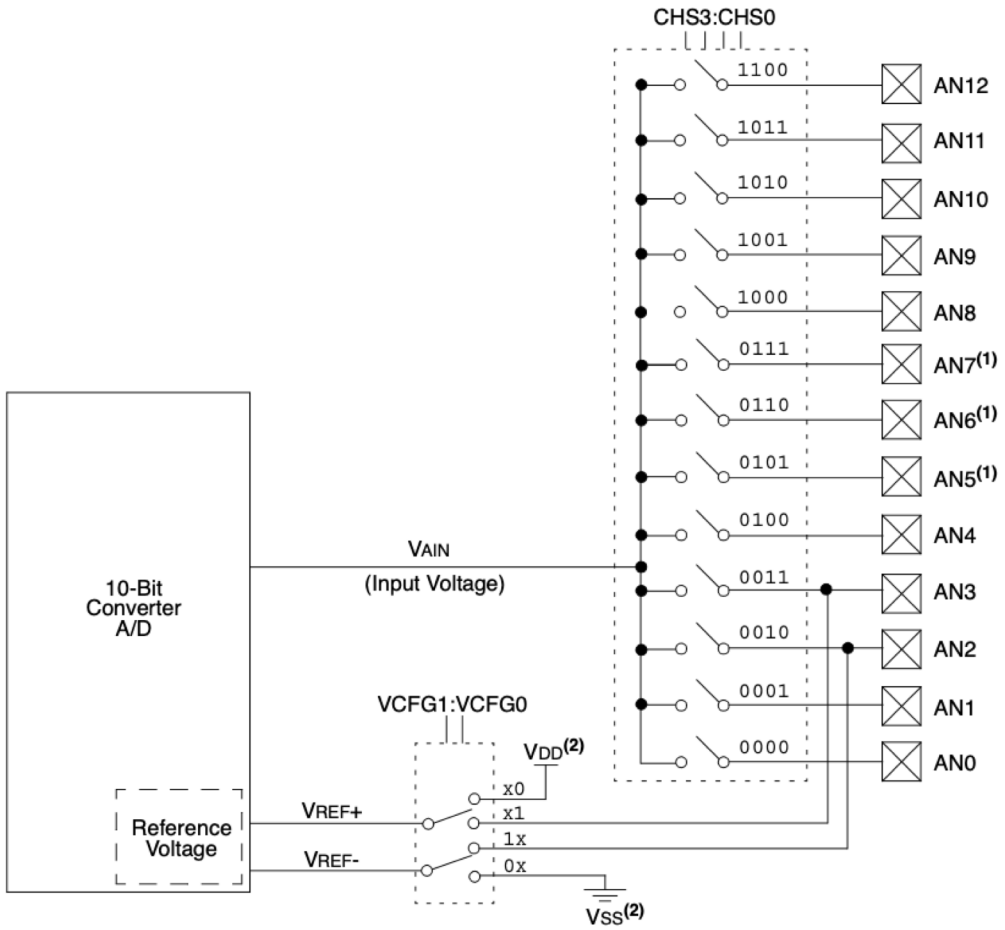
Address	Name	Address	Name	Address	Name	Address	Name	Address	Name
FFFh	TOSU	FDFh	INDF2(1)	FBFh	CCPR1H	F9Fh	IPR1	F7Fh	UEP15
FFEh	TOSH	FDEh	POSTINC2(1)	FBEh	CCPR1L	F9Eh	PIR1	F7Eh	UEP14
FFDh	TOSL	FDDh	POSTDEC2(1)	FBDh	CCP1CON	F9Dh	PIE1	F7Dh	UEP13
FFCh	STKPTR	FDCh	PREINC2(1)	FBCh	CCPR2H	F9Ch	—(2)	F7Ch	UEP12
FFBh	PCLATU	FDBh	PLUSW2(1)	FBBh	CCPR2L	F9Bh	OSCTUNE	F7Bh	UEP11
FFAh	PCLATH	FDAh	FSR2H	FBAh	CCP2CON	F9Ah	—(2)	F7Ah	UEP10
FF9h	PCL	FD9h	FSR2L	FB9h	—(2)	F99h	—(2)	F79h	UEP9
FF8h	TBLPTRU	FD8h	STATUS	FB8h	BAUDCON	F98h	—(2)	F78h	UEP8
FF7h	TBLPTRH	FD7h	TMR0H	FB7h	ECCP1DEL	F97h	—(2)	F77h	UEP7
FF6h	TBLPTRL	FD6h	TMR0L	FB6h	ECCP1AS	F96h	TRISE(3)	F76h	UEP6
FF5h	TABLAT	FD5h	T0CON	FB5h	CVRCON	F95h	TRISD(3)	F75h	UEP5
FF4h	PRODH	FD4h	—(2)	FB4h	CMCON	F94h	TRISC	F74h	UEP4
FF3h	PRODL	FD3h	OSCCON	FB3h	TMR3H	F93h	TRISB	F73h	UEP3
FF2h	INTCON	FD2h	HLVDCON	FB2h	TMR3L	F92h	TRISA	F72h	UEP2
FF1h	INTCON2	FD1h	WDTCON	FB1h	T3CON	F91h	—(2)	F71h	UEP1
FF0h	INTCON3	FD0h	RCON	FB0h	SPBRGH	F90h	—(2)	F70h	UEP0
FEFh	INDF0(1)	FCFh	TMR1H	FAFh	SPBRG	F8Fh	—(2)	F6Fh	UCFG
FEEh	POSTINC0(1)	FCEh	TMR1L	FAEh	RCREG	F8Eh	—(2)	F6Eh	UADDR
FEDh	POSTDEC0(1)	FCDh	T1CON	FADh	TXREG	F8Dh	LATE(3)	F6Dh	UCON
FECh	PREINC0(1)	FCCh	TMR2	FACh	TXSTA	F8Ch	LATD(3)	F6Ch	USTAT
FEBh	PLUSW0(1)	FCBh	PR2	FABh	RCSTA	F8Bh	LATC	F6Bh	UEIE
FEAh	FSR0H	FCAh	T2CON	FAAh	—(2)	F8Ah	LATB	F6Ah	UEIR
FE9h	FSR0L	FC9h	SSPBUF	FA9h	EEADR	F89h	LATA	F69h	UIE
FE8h	WREG	FC8h	SSPADD	FA8h	EEDATA	F88h	—(2)	F68h	UIR
FE7h	INDF1(1)	FC7h	SSPSTAT	FA7h	EECON2(1)	F87h	—(2)	F67h	UFRMH
FE6h	POSTINC1(1)	FC6h	SSPCON1	FA6h	EECON1	F86h	—(2)	F66h	UFRML
FE5h	POSTDEC1(1)	FC5h	SSPCON2	FA5h	—(2)	F85h	—(2)	F65h	SPPCON(3)
FE4h	PREINC1(1)	FC4h	ADRESH	FA4h	—(2)	F84h	PORTE	F64h	SPPEPS(3)
FE3h	PLUSW1(1)	FC3h	ADRESL	FA3h	—(2)	F83h	PORTD(3)	F63h	SPPCFG(3)
FE2h	FSR1H	FC2h	ADCON0	FA2h	IPR2	F82h	PORTC	F62h	SPPDATA(3)
FE1h	FSR1L	FC1h	ADCON1	FA1h	PIR2	F81h	PORTB	F61h	—(2)
FE0h	BSR	FC0h	ADCON2	FA0h	PIE2	F80h	PORTA	F60h	—(2)

Note 1: Not a physical register.
2: Unimplemented registers are read as '0'.
3: These registers are implemented only on 40/44-pin devices.

Conversor A/D

10 bits - 13 canais multiplexados

FIGURE 21-1: A/D BLOCK DIAGRAM



Note 1: Channels AN5 through AN7 are not available on 28-pin devices.

2: I/O pins have diode protection to VDD and VSS.

Equações

$$Resolução = \frac{Vref_+ - Vref_-}{2^n - 1}$$

$$V_{Analógica} = \frac{Valor\ binário \cdot (Vref_+ - Vref_-) + Vref_- \cdot (2^n - 1)}{2^n - 1}$$

$$V_{Analógica_{(Vref_- = 0)}} = \frac{Valor\ binário \cdot Vref}{2^n - 1}$$

Portas I/0

Portas de I/0

- Definir se é entrada ou saída (TRISA, TRISB, etc.);
- Quando for escrever na porta (saída), usar os registradores LATA, LATB, etc.
- Quando for ler o estado de um pino (entrada), usar os registradores PORTA, PORTB, etc.
- Definir se a porta é analógica ou digital, devido ao conversor A/D: (ADCON1);
- Não existe registrador ANSEL_ nesse microcontrolador!

ADCON1

REGISTER 21-2: ADCON1: A/D CONTROL REGISTER 1

U-0	U-0	R/W-0	R/W-0	R/W-0(1)	R/W(1)	R/W(1)	R/W(1)
—	—	VCFG0	VCFG0	PCFG3	PCFG2	PCFG1	PCFG0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented:** Read as '0'

bit 5 **VCFG0:** Voltage Reference Configuration bit (V_{REF-} source)
1 = V_{REF-} (AN2)
0 = V_{SS}

bit 4 **VCFG0:** Voltage Reference Configuration bit (V_{REF+} source)
1 = V_{REF+} (AN3)
0 = V_{DD}

bit 3-0 **PCFG3:PCFG0:** A/D Port Configuration Control bits:

PCFG3: PCFG0	AN12	AN11	AN10	AN9	AN8	AN7(2)	AN6(2)	AN5(2)	AN4	AN3	AN2	AN1	AN0
0000(1)	A	A	A	A	A	A	A	A	A	A	A	A	A
0001	A	A	A	A	A	A	A	A	A	A	A	A	A
0010	A	A	A	A	A	A	A	A	A	A	A	A	A
0011	D	A	A	A	A	A	A	A	A	A	A	A	A
0100	D	D	A	A	A	A	A	A	A	A	A	A	A
0101	D	D	D	A	A	A	A	A	A	A	A	A	A
0110	D	D	D	D	A	A	A	A	A	A	A	A	A
0111(1)	D	D	D	D	D	A	A	A	A	A	A	A	A
1000	D	D	D	D	D	D	A	A	A	A	A	A	A
1001	D	D	D	D	D	D	D	A	A	A	A	A	A
1010	D	D	D	D	D	D	D	D	A	A	A	A	A
1011	D	D	D	D	D	D	D	D	D	A	A	A	A
1100	D	D	D	D	D	D	D	D	D	D	A	A	A
1101	D	D	D	D	D	D	D	D	D	D	D	A	A
1110	D	D	D	D	D	D	D	D	D	D	D	D	A
1111	D	D	D	D	D	D	D	D	D	D	D	D	D

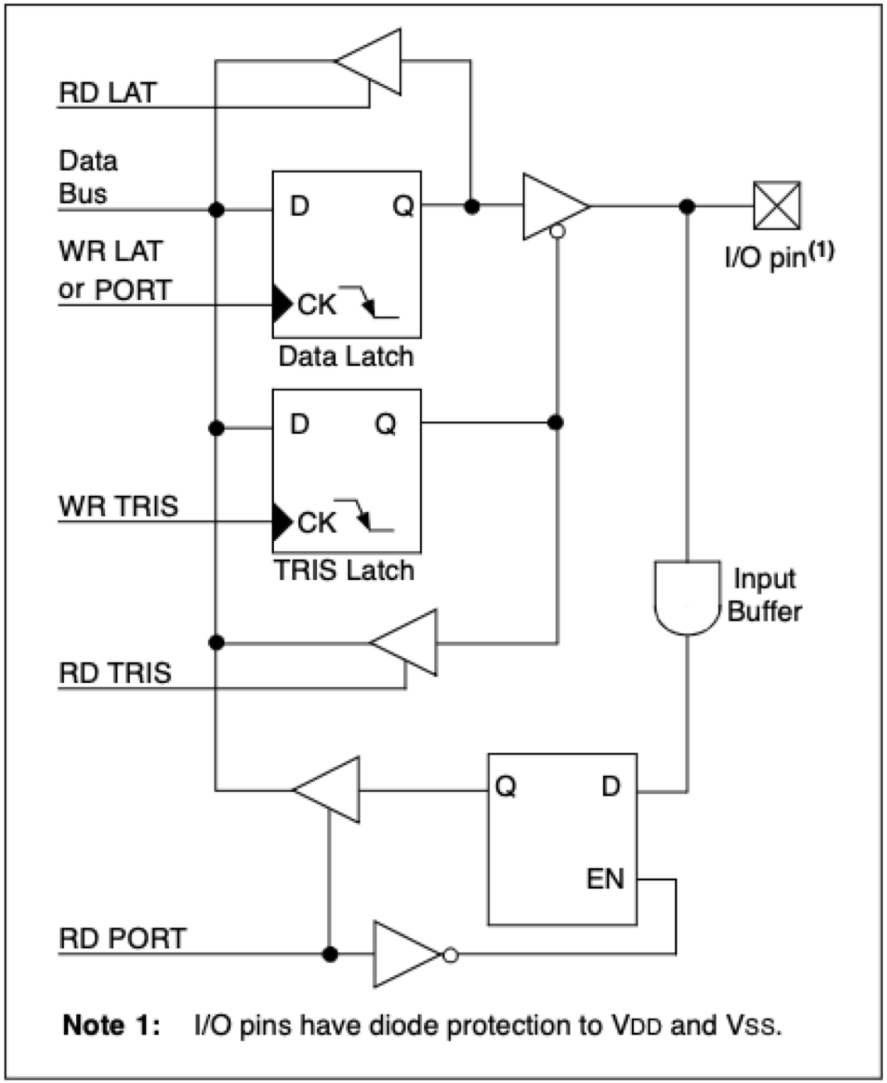
A = Analog input D = Digital I/O

Note 1: The POR value of the PCFG bits depends on the value of the PBADEN Configuration bit. When PBADEN = 1, PCFG<3:0> = 0000; when PBADEN = 0, PCFG<3:0> = 0111.

2: AN5 through AN7 are available only on 40/44-pin devices.

Portas de I/0

FIGURE 10-1: GENERIC I/O PORT OPERATION



Note 1: I/O pins have diode protection to VDD and VSS.

Módulo CCP

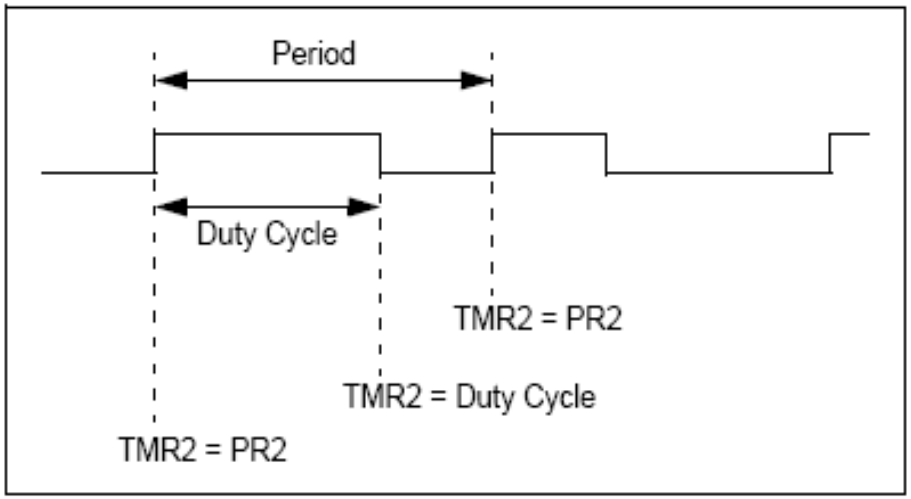
Módulo CCP

- CCP = Capture, Compare, PWM;
- Periférico presente em alguns microcontroladores PIC
- Modo Capture: contagem de tempo entre dois eventos ocorridos no pino do PIC (borda de descida ou subida)
- Modo Compare: contagem de tempo entre dois eventos ocorridos no pino do PIC e comparação com um valor pré determinado
- Modo PWM: geração de um pulso PWM no pino do PIC
- Pode gerar interrupção
- Utiliza os temporizadores do PIC para geração da base de tempo:

CCP/ECCP Mode	Timer Resource
Capture	Timer1 or Timer3
Compare	Timer1 or Timer3
PWM	Timer2

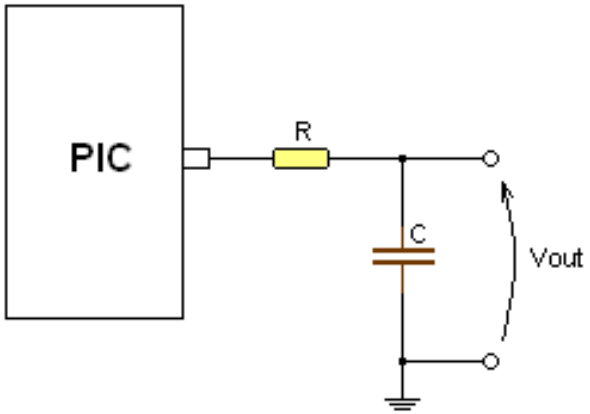
PWM

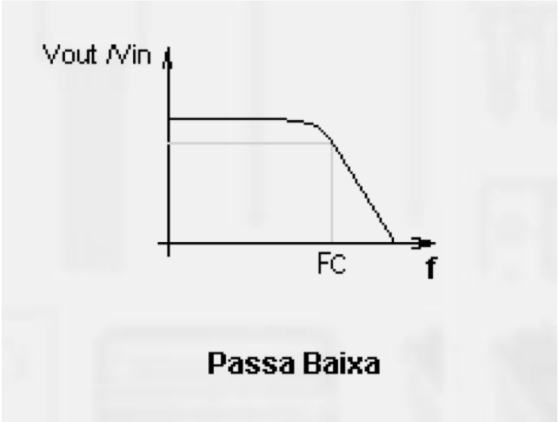
- *Pulse Width Modulation* = Modulação por largura de pulso
- Onda de frequência constante mas com largura de pulso variável (ciclo de trabalho ou *duty cycle*)
- Obtenção de uma tensão analógica a partir de um sinal digital (conversor D/A)



PWM

- Uso um filtro passa baixa com frequência de corte menor do que a frequênca do PWM





$$f_c = \frac{1}{2\pi RC}$$

FIM