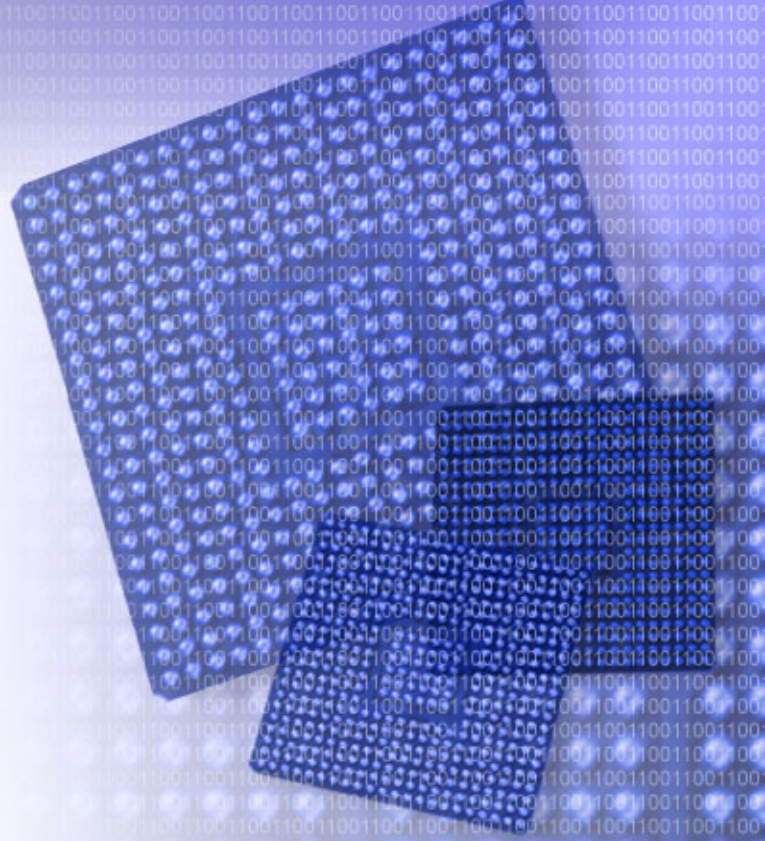
SEL–0629

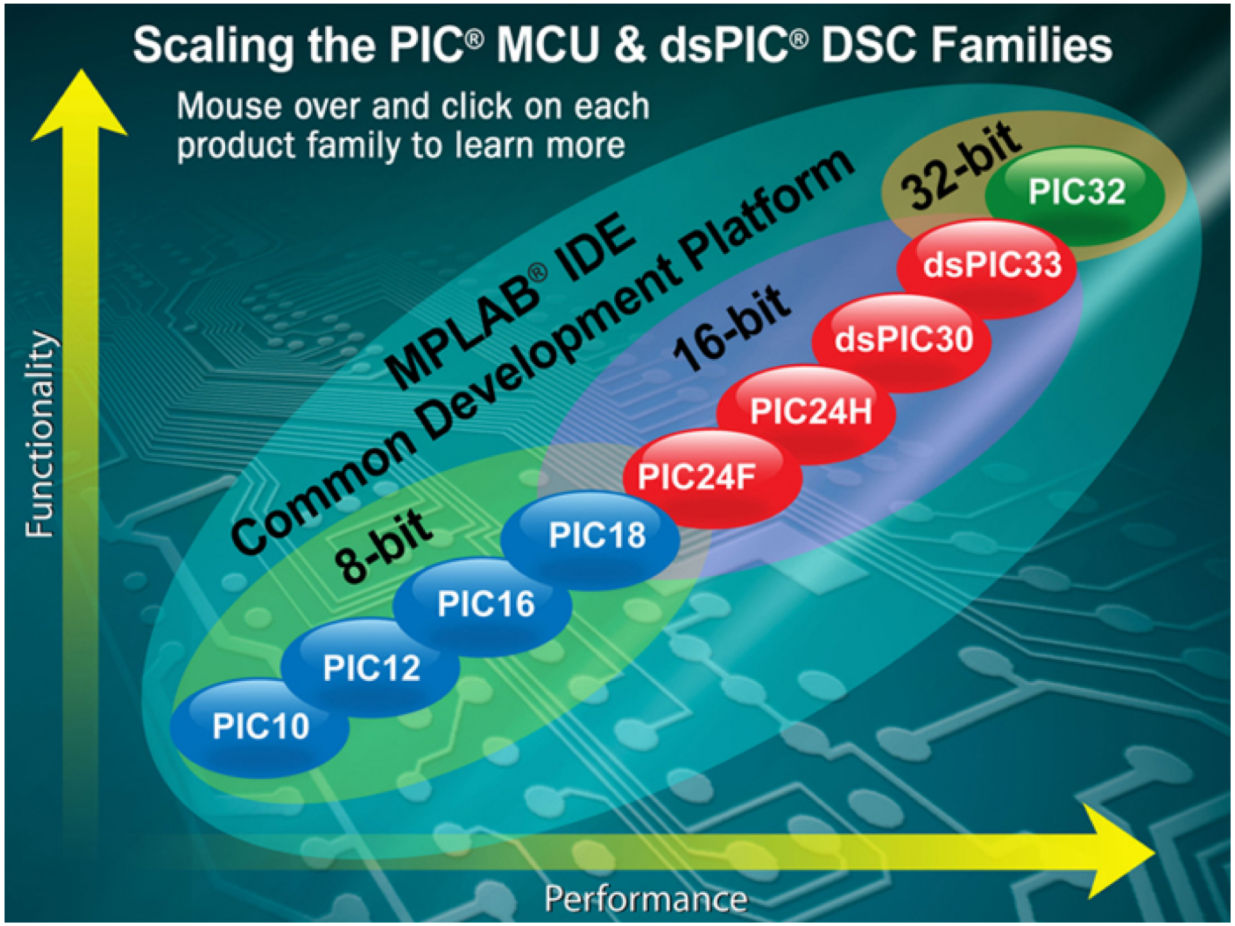
Aplicação de Microprocessadores I

Aula 2
PIC 18F45k22

Marcelo Andrade da Costa Vieira



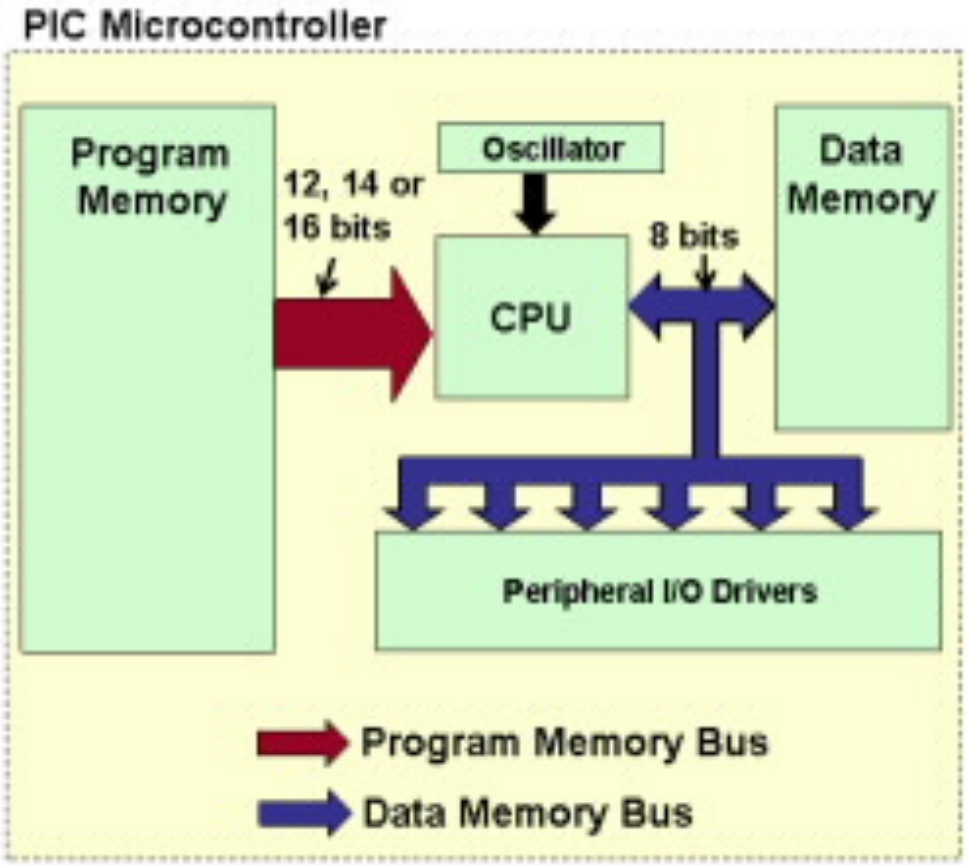
Família de Microcontroladores PIC



- Microprocessadores de 8-bit, 16-bit e 32-bit;
- A linha de 32-bit possui ULA de 32-bit, clock de até 200 MHZ e Pipeline de 5 estágios

Família PIC de 8-bits

Classificados de acordo com o tamanho do barramento de instruções. Isso define o tamanho da palavra de instruções, o número de instruções e a sua velocidade



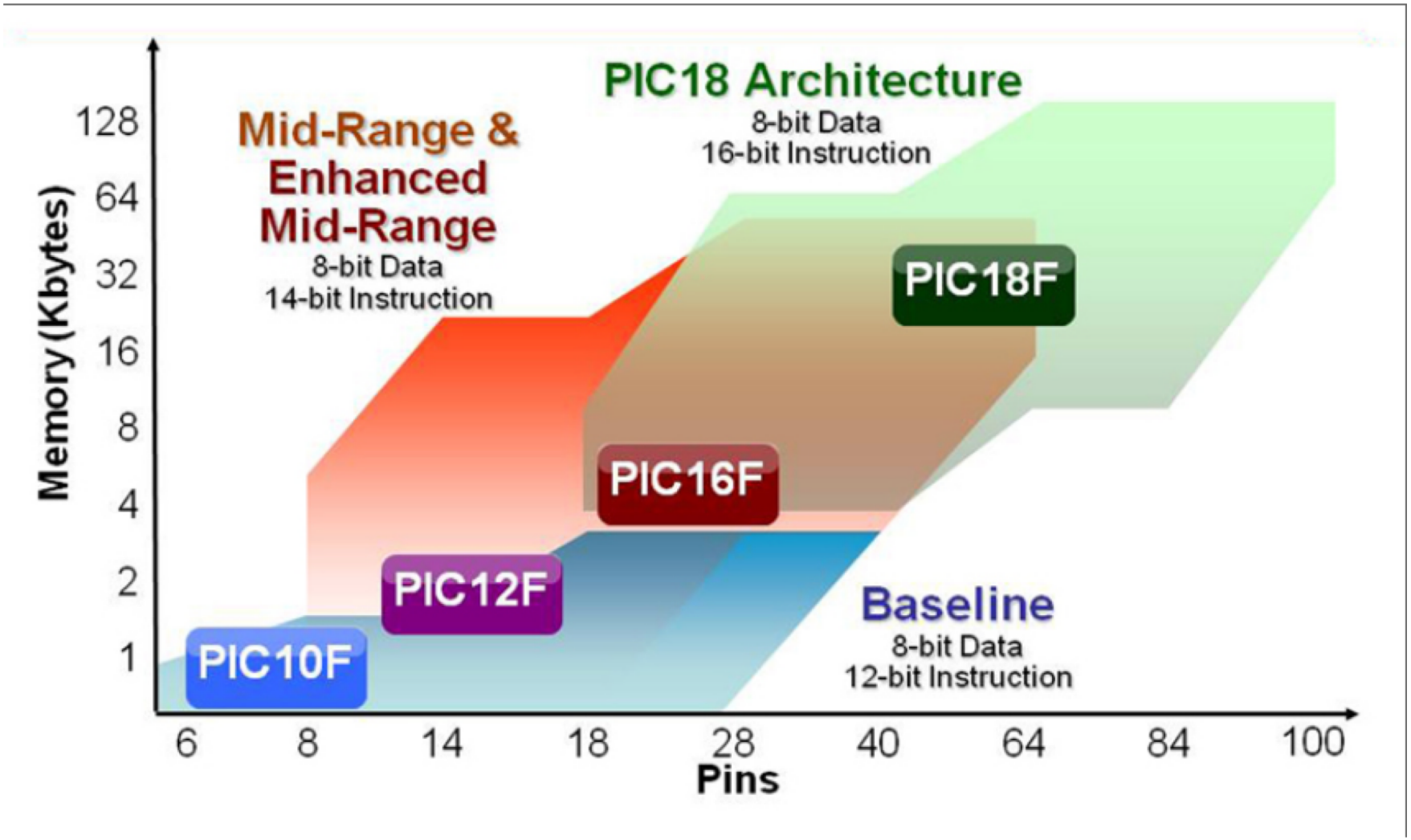
1. Baseline: 12-bits
2. Mid-range: 14-bits
1. Enhanced Mid-range: 14-bits
2. High-performance: 16-bits

Família PIC de 8-bits

Compare 8-bit PIC® MCU Architectures

	Baseline Architecture	Mid-Range Architecture	Enhanced Mid-Range Architecture	PIC18 Architecture
Pin Count	6-40	8-64	8-64	18-100
Interrupts	No	Single interrupt capability	Single interrupt capability with hardware context save	Multiple interrupt capability with hardware context save
Performance	5 MIPS	5 MIPS	8 MIPS	Up to 16 MIPS
Instructions	33, 12-bit	35, 14-bit	49, 14-bit	83, 16-bit
Program Memory	Up to 3 KB	Up to 14 KB	Up to 28 KB	Up to 128 KB
Data Memory	Up to 138 Bytes	Up to 368 Bytes	Up to 1,5 KB	Up to 4 KB
Hardware Stack	2 level	8 level	16 level	32 level
Features	▪ Comparator ▪ 8-bit ADC ▪ Data Memory ▪ Internal Oscillator	In addition to Baseline: ▪ SPI/I²C™ ▪ UART ▪ PWMs ▪ LCD ▪ 10-bit ADC ▪ Op Amp	In addition to Mid-Range: ▪ Multiple Communication Peripherals ▪ Linear Programming Space ▪ PWMs with Independent Time Base	In addition to Enhanced Mid-Range: ▪ 8x8 Hardware Multiplier ▪ CAN ▪ CTMU ▪ USB ▪ Ethernet ▪ 12-bit ADC
Highlights	Lowest cost in the smallest form factor	Optimal cost to performance ratio	Cost effective with more performance and memory	High performance, optimized for C programming, advanced peripherals
Total Number of Devices	16	58	29	193
Families	PIC10, PIC12, PIC16	PIC12, PIC16	PIC12FXXX, PIC16F1XX	PIC18

Família PIC de 8 Bits

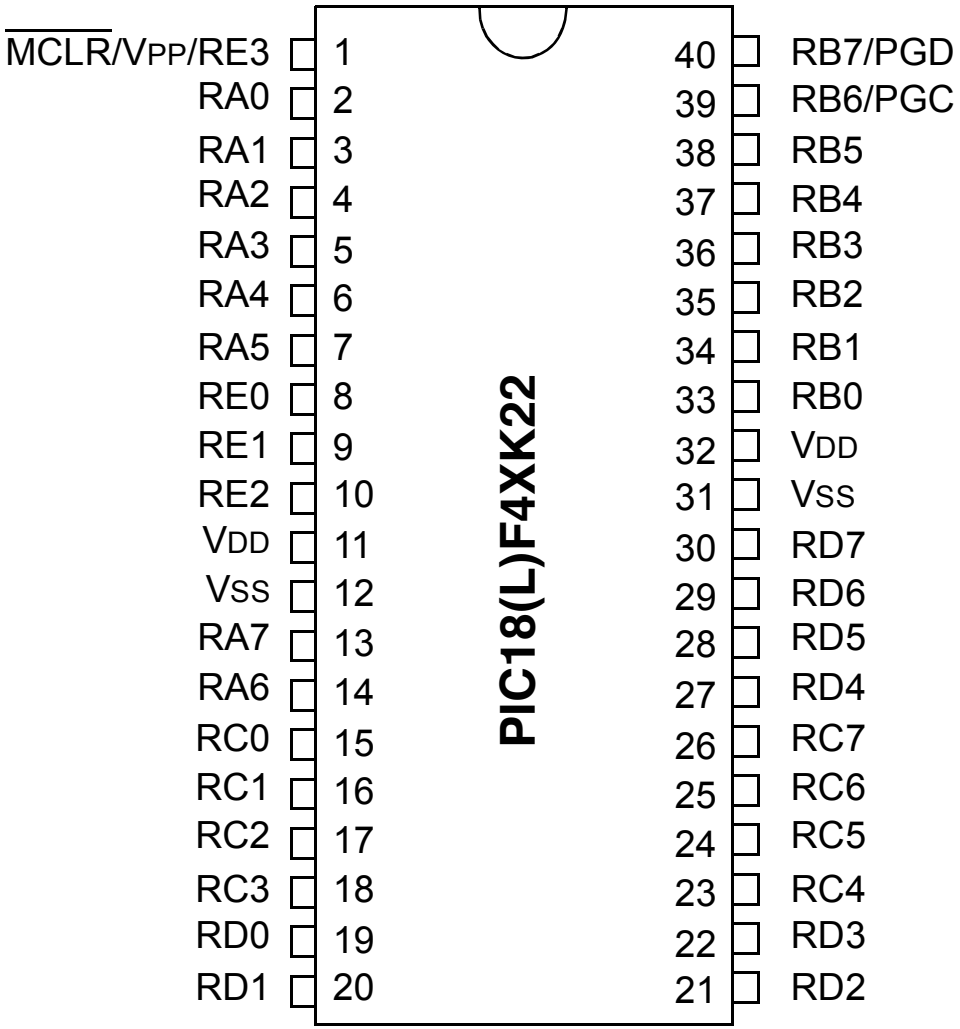


PIC 18F45K22

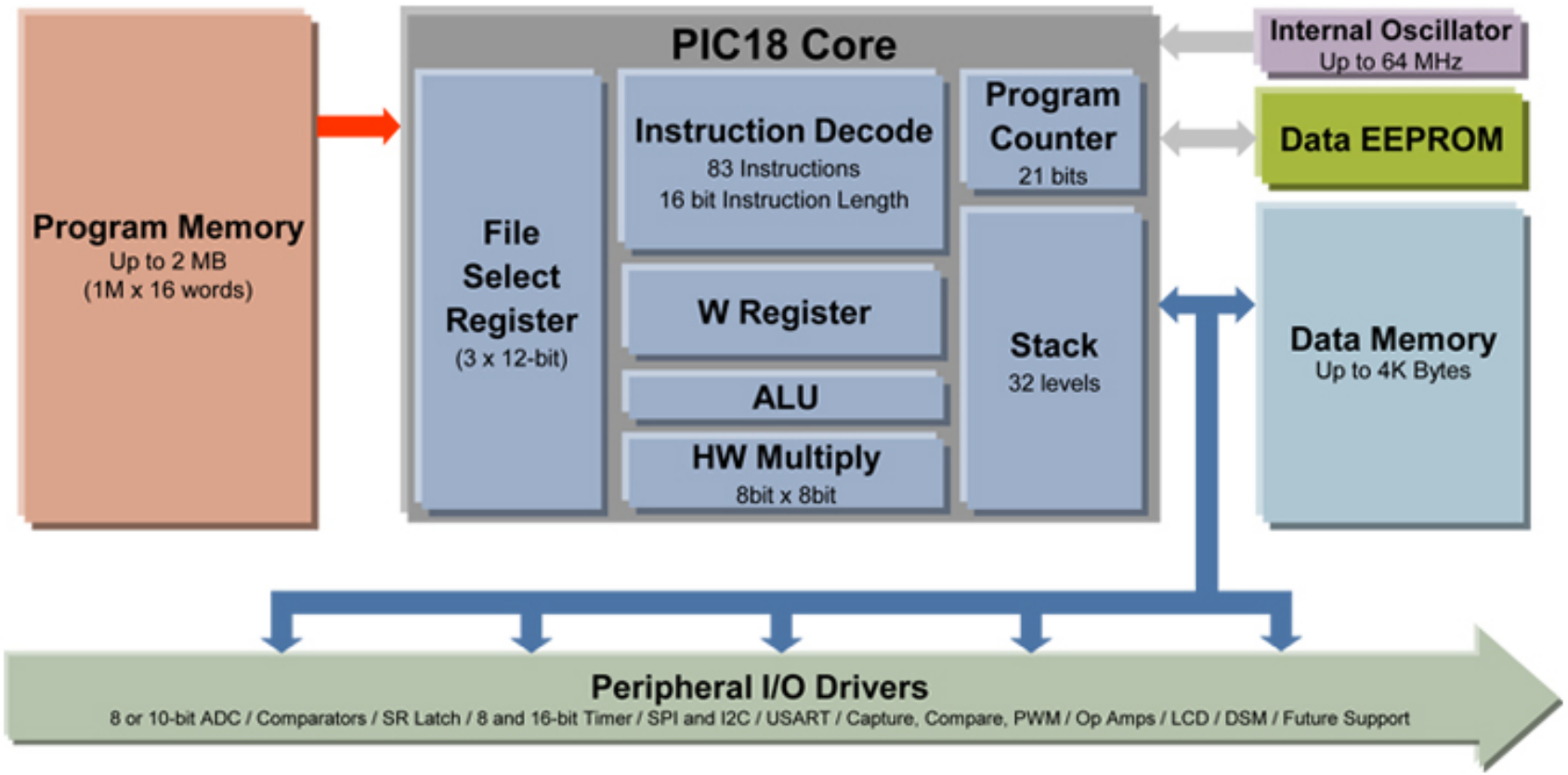
PIC 18F45K22

- Memória de Instruções de 16K x **16 bits** (High-Performance) – FLASH – 32KB
- Memória de dados (SRAM) com 1,5 *Kbytes* de uso geral – endereçamento de 12 bits (4096 bytes) divididos em 16 bancos de 256 bytes cada;
- 40 pinos – 35 portas de I/O configuráveis como entrada ou saída;
- Memória adicional interna do tipo EEPROM não volátil de 256*bytes*;
- 34 fontes de interrupções diferentes com 2 níveis de prioridade;
- Programação com 75 instruções (otimizadas para C)
- Frequência máxima de operação de até 40 MHz (10 MIPS)
- Pilha (*Stack*) de 31 posições;
- Periféricos: 7 Timers, PWM, Conversor A/D e D/A, USART, etc...
- Multiplicador 8 x 8 de um ciclo de máquina.

PIC 18F45K22

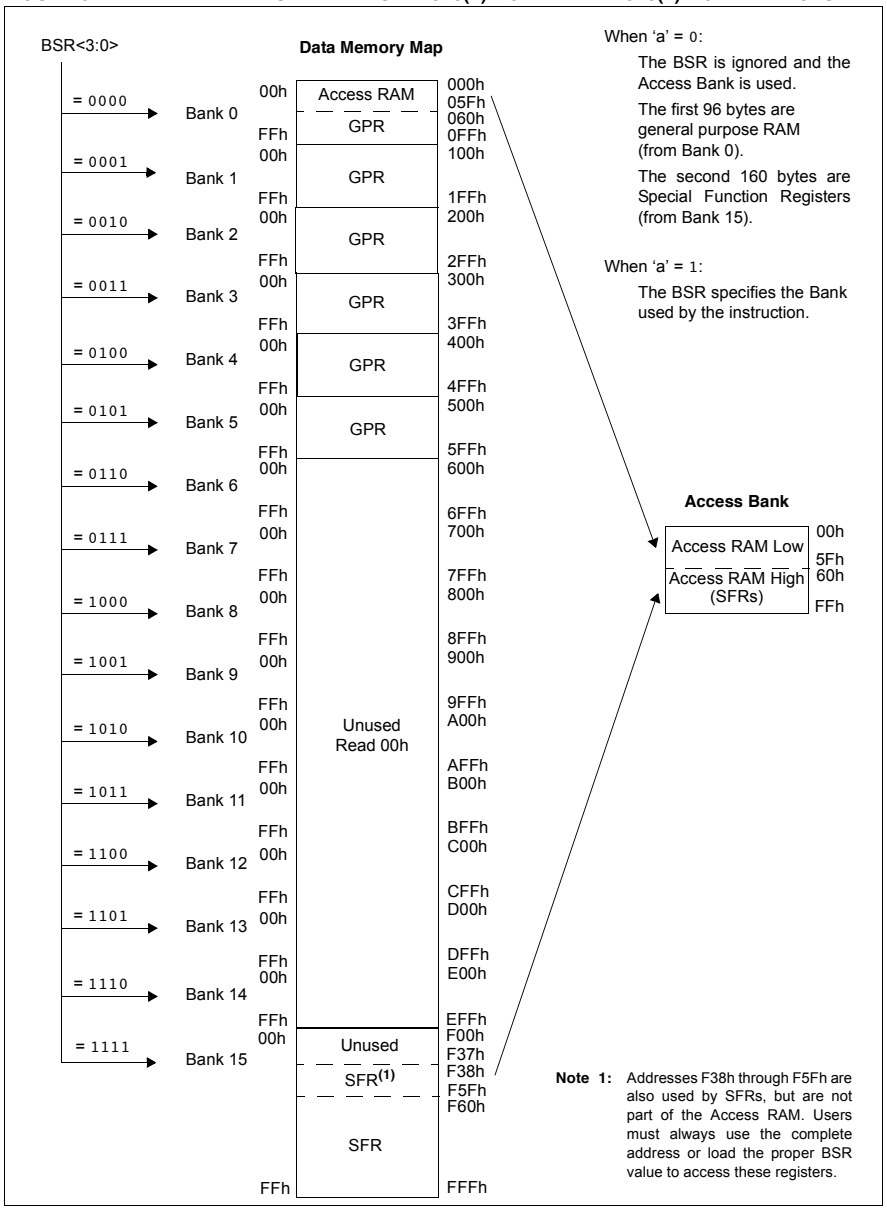


Memória de Programa



Memória RAM

FIGURE 5-7: DATA MEMORY MAP FOR PIC18(L)F25K22 AND PIC18(L)F45K22 DEVICES



- Memória de dados de 2K x **8 bits;**
- Endereçado por duto de 12 bits (4096 bytes);
- 16 bancos de 256 bytes cada;
- Registrador BSR para seleção do banco:
  - 4 bits do BSR (MSB)
  - 8 bits da instrução (LSB)
- 256 bytes de acesso direto (0 e 15)
  - (GPR + SFR)
- Seleção na instrução se o acesso é direto (a = 0) ou via banco (a = 1).

SFR

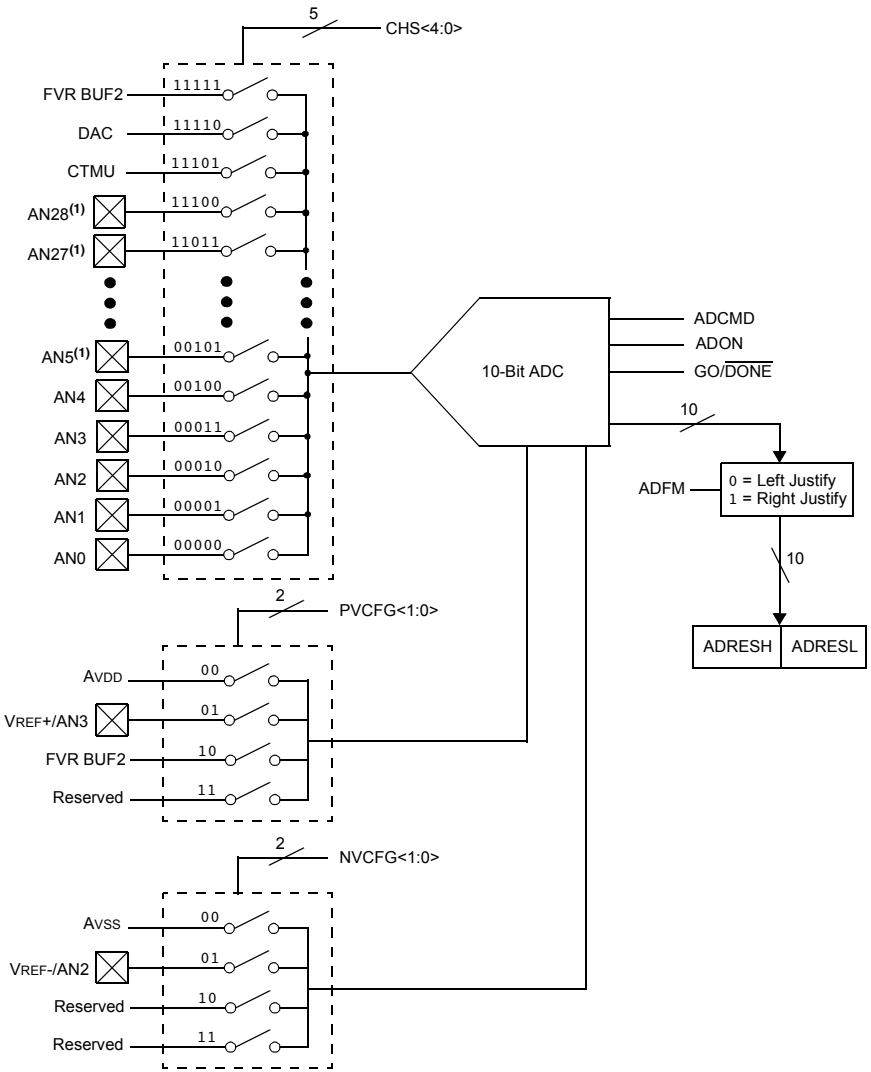
Address	Name	Address	Name	Address	Name	Address	Name	Address	Name
FFFh	TOSU	FD7h	TMR0H	FAFh	SPBRG1	F87h	—(2)	F5Fh	CCPR3H
FFEh	TOSH	FD6h	TMR0L	FAEh	RCREG1	F86h	—(2)	F5Eh	CCPR3L
FFDh	TOSL	FD5h	T0CON	FADh	TXREG1	F85h	—(2)	F5Dh	CCP3CON
FFCh	STKPTR	FD4h	—(2)	FACh	TXSTA1	F84h	PORTE	F5Ch	PWM3CON
FFBh	PCLATU	FD3h	OSCCON	FABh	RCSTA1	F83h	PORTD(3)	F5Bh	ECCP3AS
FFAh	PCLATH	FD2h	OSCCON2	FAAh	EEADRH(4)	F82h	PORTC	F5Ah	PSTR3CON
FF9h	PCL	FD1h	WDTCON	FA9h	EEADR	F81h	PORTB	F59h	CCPR4H
FF8h	TBLPTRU	FD0h	RCON	FA8h	EEDATA	F80h	PORTA	F58h	CCPR4L
FF7h	TBLPTRH	FCFh	TMR1H	FA7h	EECON2(1)	F7Fh	IPR5	F57h	CCP4CON
FF6h	TBLPTRL	FCEh	TMR1L	FA6h	EECON1	F7Eh	PIR5	F56h	CCPR5H
FF5h	TABLAT	FCDh	T1CON	FA5h	IPR3	F7Dh	PIE5	F55h	CCPR5L
FF4h	PRODH	FCCh	T1GCON	FA4h	PIR3	F7Ch	IPR4	F54h	CCP5CON
FF3h	PRODL	FCBh	SSP1CON3	FA3h	PIE3	F7Bh	PIR4	F53h	TMR4
FF2h	INTCON	FCAh	SSP1MSK	FA2h	IPR2	F7Ah	PIE4	F52h	PR4
FF1h	INTCON2	FC9h	SSP1BUF	FA1h	PIR2	F79h	CM1CON0	F51h	T4CON
FF0h	INTCON3	FC8h	SSP1ADD	FA0h	PIE2	F78h	CM2CON0	F50h	TMR5H
FEFh	INDF0(1)	FC7h	SSP1STAT	F9Fh	IPR1	F77h	CM2CON1	F4Fh	TMR5L
FEEh	POSTINC0(1)	FC6h	SSP1CON1	F9Eh	PIR1	F76h	SPBRGH2	F4Eh	T5CON
FEDh	POSTDEC0(1)	FC5h	SSP1CON2	F9Dh	PIE1	F75h	SPBRG2	F4Dh	T5GCON
FECh	PREINC0(1)	FC4h	ADRESH	F9Ch	HLVDCON	F74h	RCREG2	F4Ch	TMR6
FEBh	PLUSW0(1)	FC3h	ADRESL	F9Bh	OSCTUNE	F73h	TXREG2	F4Bh	PR6
FEAh	FSR0H	FC2h	ADCON0	F9Ah	—(2)	F72h	TXSTA2	F4Ah	T6CON
FE9h	FSR0L	FC1h	ADCON1	F99h	—(2)	F71h	RCSTA2	F49h	CCPTMRS0
FE8h	WREG	FC0h	ADCON2	F98h	—(2)	F70h	BAUDCON2	F48h	CCPTMRS1
FE7h	INDF1(1)	FBFh	CCPR1H	F97h	—(2)	F6Fh	SSP2BUF	F47h	SRCON0
FE6h	POSTINC1(1)	FBEh	CCPR1L	F96h	TRISE	F6Eh	SSP2ADD	F46h	SRCON1
FE5h	POSTDEC1(1)	FBDh	CCP1CON	F95h	TRISD(3)	F6Dh	SSP2STAT	F45h	CTMUCONH
FE4h	PREINC1(1)	FBCh	TMR2	F94h	TRISC	F6Ch	SSP2CON1	F44h	CTMUCONL
FE3h	PLUSW1(1)	FBBh	PR2	F93h	TRISB	F6Bh	SSP2CON2	F43h	CTMUICON
FE2h	FSR1H	FBAh	T2CON	F92h	TRISA	F6Ah	SSP2MSK	F42h	VREFCON0
FE1h	FSR1L	FB9h	PSTR1CON	F91h	—(2)	F69h	SSP2CON3	F41h	VREFCON1
FE0h	BSR	FB8h	BAUDCON1	F90h	—(2)	F68h	CCPR2H	F40h	VREFCON2
FDFh	INDF2(1)	FB7h	PWM1CON	F8Fh	—(2)	F67h	CCPR2L	F3Fh	PMD0
FDEh	POSTINC2(1)	FB6h	ECCP1AS	F8Eh	—(2)	F66h	CCP2CON	F3Eh	PMD1
FDDh	POSTDEC2(1)	FB5h	—(2)	F8Dh	LATE(3)	F65h	PWM2CON	F3Dh	PMD2
FDCh	PREINC2(1)	FB4h	T3GCON	F8Ch	LATD(3)	F64h	ECCP2AS	F3Ch	ANSELE
FDBh	PLUSW2(1)	FB3h	TMR3H	F8Bh	LATC	F63h	PSTR2CON	F3Bh	ANSELD
FDAh	FSR2H	FB2h	TMR3L	F8Ah	LATB	F62h	IOCB	F3Ah	ANSELC
FD9h	FSR2L	FB1h	T3CON	F89h	LATA	F61h	WPUB	F39h	ANSELB
FD8h	STATUS	FB0h	SPBRGH1	F88h	—(2)	F60h	SLRCON	F38h	ANSELA

Note 1: This is not a physical register.
2: Unimplemented registers are read as '0'.
3: PIC18(L)F4XK22 devices only.
4: PIC18(L)F26K22 and PIC18(L)F46K22 devices only.

Conversor A/D

10 bits - 30 canais multiplexados

FIGURE 17-1: ADC BLOCK DIAGRAM



Note: Additional ADC channels AN5-AN7 and AN20-AN27 are only available on PIC18(L)F4XK22 devices.

Equações

$$Resolução = \frac{Vref_+ - Vref_-}{2^n - 1}$$

$$V_{Analógica} = \frac{Valor\ binário \cdot (Vref_+ - Vref_-) + Vref_- \cdot (2^n - 1)}{2^n - 1}$$

$$V_{Analógica_{(Vref_- = 0)}} = \frac{Valor\ binário \cdot Vref}{2^n - 1}$$

Portas I/0

Portas de I/0

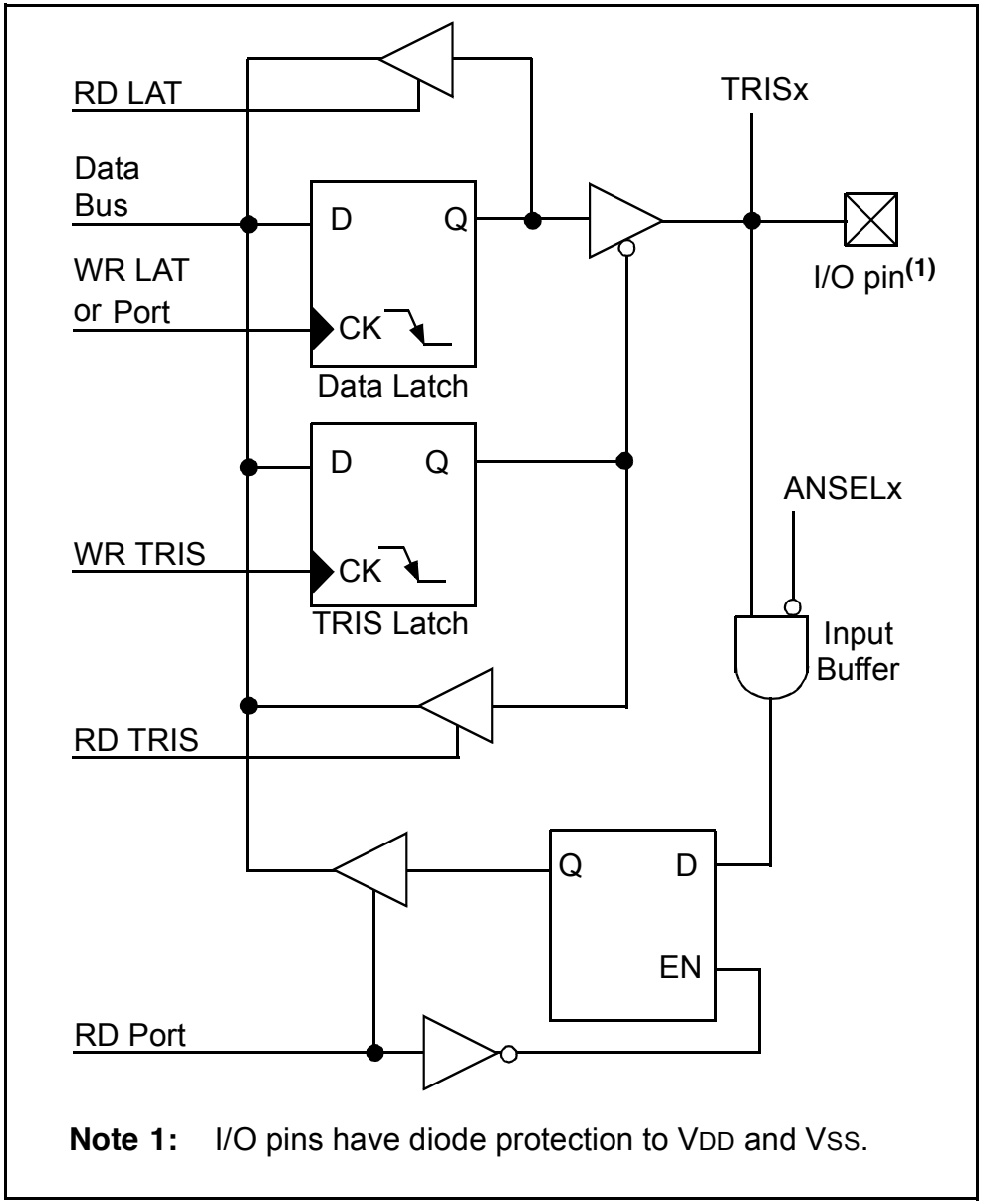
Definir se é entrada ou saída (TRISA, TRISB, etc.);

Quando for escrever na porta (saída), usar os registradores LATA, LATB, etc.

Quando for ler o estado de um pino (entrada), usar os registradores PORTA, PORTB, etc.

Definir se a porta é analógica ou digital, devido ao conversor A/D (ANSELA, ANSELB, etc..)

Portas de I/0



Note 1: I/O pins have diode protection to VDD and VSS.

Módulo CCP

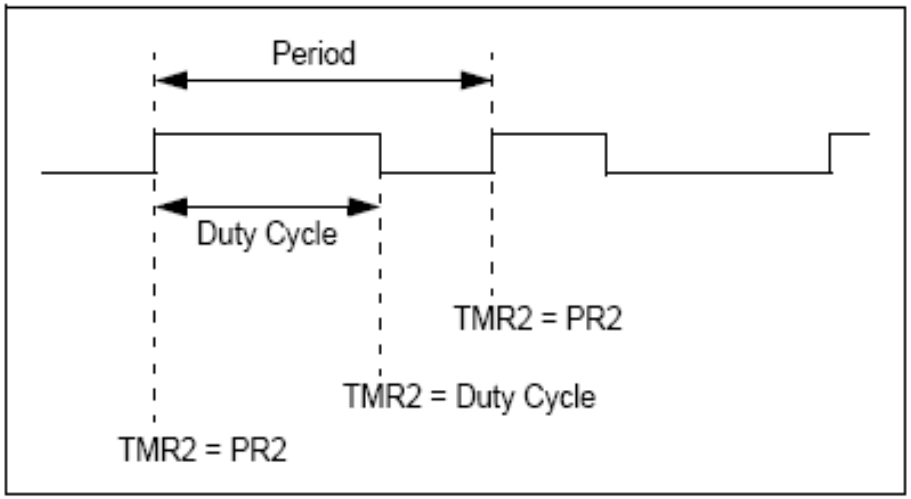
Módulo CCP

- CCP = Capture, Compare, PWM;
- Periférico presente em alguns microcontroladores PIC
- Modo Capture: contagem de tempo entre dois eventos ocorridos no pino do PIC (borda de descida ou subida)
- Modo Compare: contagem de tempo entre dois eventos ocorridos no pino do PIC e comparação com um valor pré determinado
- Modo PWM: geração de um pulso PWM no pino do PIC
- Pode gerar interrupção
- Utiliza os temporizadores do PIC para geração da base de tempo:

CCP/ECCP Mode	Timer Resource
Capture	Timer1 or Timer3
Compare	Timer1 or Timer3
PWM	Timer2

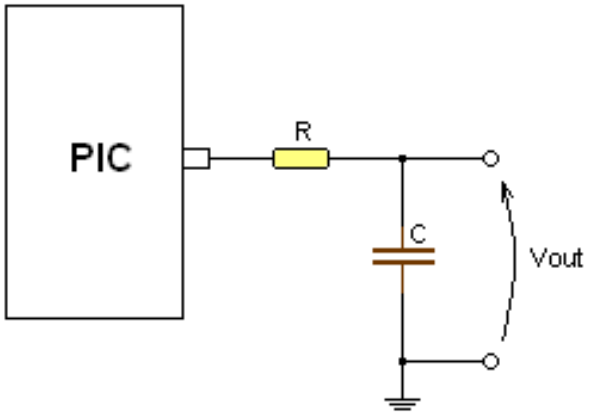
PWM

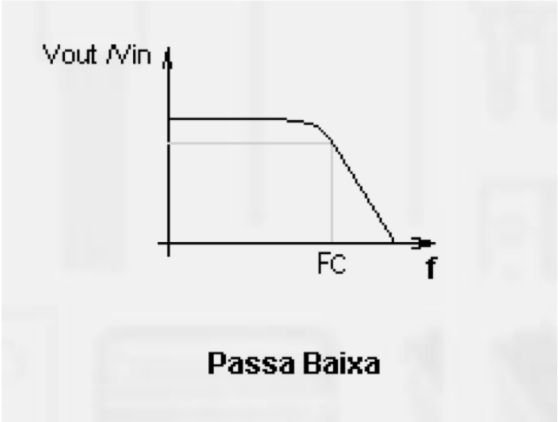
- *Pulse Width Modulation* = Modulação por largura de pulso
- Onda de frequência constante mas com largura de pulso variável (ciclo de trabalho ou *duty cycle*)
- Obtenção de uma tensão analógica a partir de um sinal digital (conversor D/A)



PWM

- Uso um filtro passa baixa com frequência de corte menor do que a frequênca do PWM





$$f_c = \frac{1}{2\pi RC}$$

FIM