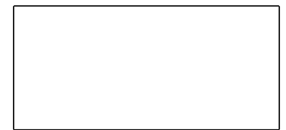

TSMC 0.18 μm Mixed Signal Salicide (1P6M+, 1.8V/3.3V) Brief Process Flow

Process Sequence	Process Stage	Description	Remark
1	WF1 SAR		
1-1	DNW1 PH	119	For Triple Well(DNW) Option
1-2	DNW1 IM	DEEP N-WELL IMPLANT	For Triple Well(DNW) Option
1-3	IM1 AN1	POST ANNEAL	For Triple Well(DNW) Option
2	PAD1 OX	110A	
3	SN1 DP	1625A	
4	OD1 PH	120	
5	OD1 ET	STI ETCH	
6	TRCH1 OX		
7	TRCH1 PH	121	
8	TRCH1 ET	RVERSE TONE ETCH	
9	TRCH1 CMP		
10	SN1 RM		
11	SAC1 OX	110A	
12	PWL1 PH	191	
13	PWL1 IM	P-WELL	
14	VTN1 IM	VTN IMP	
15	VTN1 PH2	118	For Medium NMOS option
16	NAPT1 IM1	N-CHANNEL APT IMP	
17	NWL1 PH2	192	
18	NWL1 IM1	N-WELL	
19	N-FLD1-IM1	P-CHANNEL APT IMP	
20	VTP1 PH	117	For Medium PMOS option
21	VTP1 IM1	VTP IMP	
22	GATE1 OX	SAC OX REMOVE	
23	GATE1 OX	GATE OX-1, 50A	
24	VT1 PH	132	
25	GATE 1 ET	SAC OXIDE REMOVE	
26	GATE2 OX	GATE OX, 32A	
27	PO1 DP	2000 A	

Process Sequence	Process Stage	Description	Remark
28	PO1 PH	130	
29	PO1 ET		
30	N-LDD1 PH	114	
31	N-LDD1 IM	1.8V N-POCKET IMP	
32	N-LDD1 IM	1.8V N-LDD1 IMP	
33	P-LDD1 PH	113	
34	P-LDD1 IM	1.8V P-POCKET IMP	
35	P-LDD1 IM	1.8V P-LDD IMP	
36	P-LDD2 PH	115	
37	P-LDD2 IM	P-LDD IMP	
38	N-LDD2 PH1	116	
39	NLDD2 IP1	NLDD2-1 IMP	
40	SW1 DP	SPACER DEP	
41	SW1 ET	SPACER ETCH	
42	N+S/D1 PH	198	
43	N+S/D1 IM		
44	N+S/D1 DI	N+ RTA	
45	P+S/D1 PH	197	
46	P+S/D1 IM		
47	HP-PHO	133	
48	HP-IMP	HIGH RESISTOR IMP	
49	ESD1 PH	110	Optional
50	ESD1 IM		Optional
51	RPO DP	RPO DEP	
52	S/D1 DI	S/D RTA ANNEAL	
53	RPO1 PH	155	
54	RPO1 ET		
55	SALII DP		
56	SALI1FORM	1ST RTA	
57	SALI1FORM	SALI1FORM	
58	SALI1FORM	2ND RTA	
59	ILDBPTS1 1	ILD	
60	ILD CMP	7.5K REMAINING	

Process Sequence	Process Stage	Description	Remark
61	CO1 PH	156	
62	CO1 ET		
63	WPL1 BAR		
64	WPL1 DP	W DEP	
65	WPL1 CMP		
66	ME1 SPU		
67	ME1 PH	160	
68	ME1 ET		
69	VA1OX1 DP		
70	VA1 CP	6.5KA REMAINING	
71	VA1 PH	178	
72	VA1 ET		
73	WPL2 BAR		
74	WPL2 DP	W DEP	
75	WPL2 CMP		
76	ME2 SPU		
77	ME2 PH	180	
78	ME2 ET		
79	VA2OX1 DP		
80	VA2 CMP	6.5K REMAINING	
81	VA2 PH	179	
82	VA2 ET		
83	WPL3 BAR		
84	WPL3 DP	W	
85	WPL3 CMP		
86	ME3 SPU		
87	ME3 PH	181	
88	ME3 ET		
89	VA3OX1 DP	HDP FSG	
90	VA3 CMP		
91	VA3 PH	173	
92	VA3 ET		
93	WPL4 BAR		
94	WPL4 DP	W DEP	

Process Sequence	Process Stage	Description	Remark
95	WPL4_CMP		
96	ME4 SPU		
97	ME4 PH	184	
98	ME4 ET		
99	VA4OX1 DP	HDP FSG DEP	
100	VA4 CMP		
101	VA4 PH	174	
102	VA4 ET		
103	WPL5 BAR		
104	WPL5 DP	W DEP	
105	WPL5 CP		
106	ME5 SPU		
107	CTM1 DP	MiM dielectric p.	For MiM capacitor(1P6M+
108	CTM1_SPU	CTM sputter	For MiM capacitor(1P6M+
109	CTM1_PH	182	For MiM capacitor(1P6M+
110	CTM1_ET		For MiM capacitor(1P6M+
111	ME5 PH	185	
112	ME5 ET		
113	VA5OX1 DP	HDP FSG DEP	
114	VA5 CMP		
115	VA5 PH	175	
116	VA5 ET		
117	WPL6 BAR		
118	WPL6 DP	W	
119	WPL6 CMP		
120	TME SPU	TOP METAL OPTION 1	NORMAL METAL
120-1	TME SPU	TOP METAL OPTION 2	THICK METAL
121	TME PH	186	
122	TME ET		
123	PA1OX1 DP	11.5 KA	
124	PA1SN1 DP	6KA	
125	PA1 PH	107	
126	PA1 ET		
127	ALLOY1 1		
128	WAT2 1		

PH: Photoresist + Mask

DP: deposição

SN: nitreto de Silicio

ET: etch

CMP: chemical mechanical polishing

SAC: sacrificio

GATE1: oxido mais espresso para gate

GATE 2: óxido de gate

PO: polisilicio

HP-PHO: High resistency Poly

RPO: resistence protection oxide (protege resistores do siliceto)

SAL: siliceto

CO: contact

WPL1 Bar: barreira para o W

Spu: sputtering

CTM1: dieletrico para capacitors metal metal

PA1OX: óxido final de passivacao

RTA: Rapid Thermal Annealing

ILD: Inter-Layer Dielectric