REVIEW SUMMARY

DEVICE TECHNOLOGY

Nanomaterials in transistors: From high-performance to thin-film applications

Aaron D. Franklin

BACKGROUND: Transistors are one of the most enabling "hidden" technologies of all time and have facilitated the development of computers, the Internet, thin mobile displays, and much more. Silicon, which has been the material of choice for transistors in nearly every application for decades, is now reaching the fundamental limits to what it can offer for future transistor technologies. The newest display technologies are already turning to metal oxide materials, such as indium gallium zinc oxide (IGZO), for the improvements needed to drive organic light-emitting diodes. Ranging from applications such as display backplanes to high-performance microprocessors for servers, nanomaterials offer lasting advantages for the coming decades of transistor technologies. In this Review, the advantages of nanomaterials are discussed in the context of different transistor applications, along with the breakthroughs needed for nanomaterial transistors to enable the next generation of technological advancement.

ON OUR WEB SITE

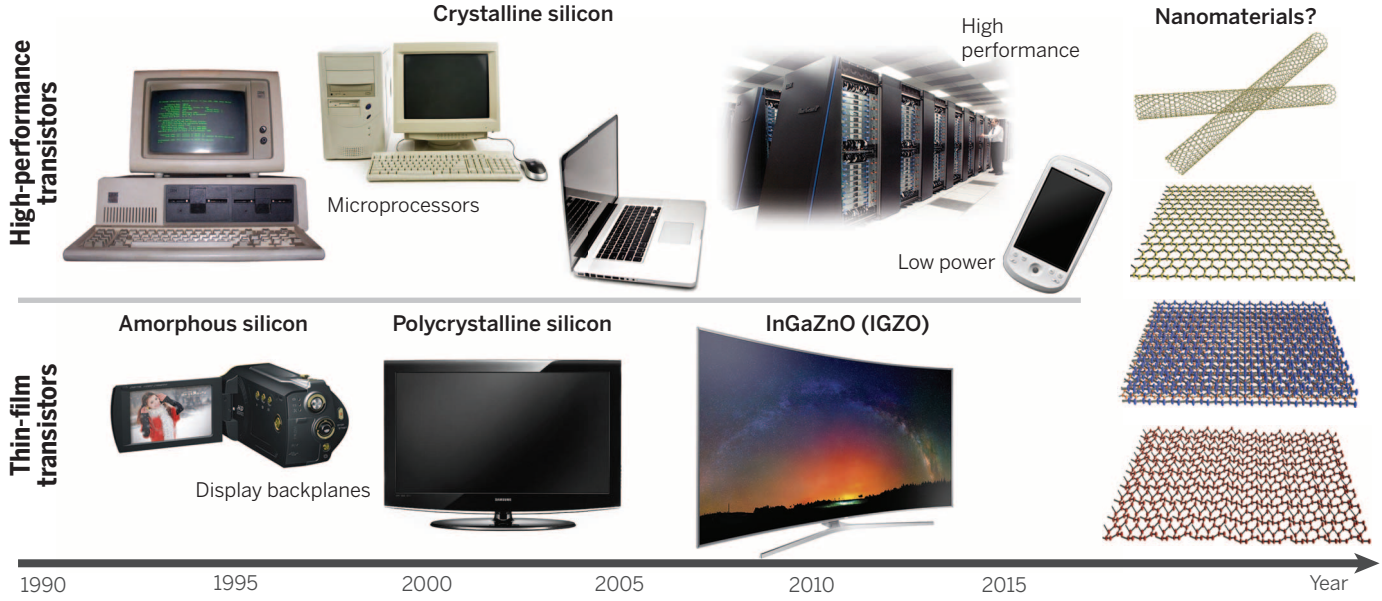
Read the full article at http://dx.doi.org/10.1126/science.aab2750

ADVANCES: About 15 years ago, nanomaterials began receiving focused attention for transistors. Carbon nanotubes—molecules consisting of a cylindrical single layer of carbon atoms arranged in a hexagonal lattice—were the first to be given serious consideration, and their benefits quickly became widely acclaimed. Given their ability to transport electrical current with near-zero resistance, even at room temperature, the explosion of interest in nanotubes for electronics was understandable. Graphene, a related allotrope of carbon, benefited from the expansive interest carbon nanotubes had created for nanomaterial electronics. Although graphene transistors eventually proved less viable for digital applications, owing to the absence of an energy band gap, the excitement over graphene ushered in a complete revolution of interest in similar two-dimensional materials. Now, transition metal dichalcogenides and the so-called X-ene family of nanomaterials (e.g., silicence, phosphorene) dominate the attention of the nanoelectronics community. Hardly a day goes by without a paper being published on some advancement related to the use of nanomaterials in transistors. Hence, this Review focuses on how to keep such progress in the proper context with respect to the target transistor application, as well as the consideration of nanomaterials for completely new application spaces.

OUTLOOK: The benefits and practicality differ for each nanomaterial, and varied amounts of progress have been made in considering each of them for transistors. In just a few short years, thousands of papers have been published on improving synthesis or demonstrating simple functions of the newer nanomaterials. However, reflection on whether their newness translates to actual superiority over other options is warranted. Clearly, all of the nanomaterial possibilities offer certain advantages for future transistor technologies, but some do so with fewer caveats than others. Future research will benefit from keeping scientific advancement of nanomaterial transistors in line with end-goal deliverables. Overall, considering that only 15 years have elapsed since the study of nanomaterials for transistors began in earnest, the toolbox of available options and the developments toward overcoming challenges are promising. ■

Department of Electrical and Computer Engineering and Department of Chemistry, Duke University, Durham, NC 27708, USA. E-mail: aaron.franklin@duke.edu

Cite this article as A. D. Franklin, *Science* 349, aab2750 (2015). DOI: 10.1126/science.aab2750



Technologies enabled by high-performance and thin-film transistors over the past 25 years. (**Top**) Silicon transistors have driven the microprocessors used in computational devices ranging from low-power gadgets to large servers. (**Bottom**) Various forms of cheaper silicon enabled the display revolution, now being shared by IGZO. (**Right**) Nanomaterials may be the next transistor material for enabling a new generation of technologies.

REVIEW

DEVICE TECHNOLOGY

Nanomaterials in transistors: From high-performance to thin-film applications

Aaron D. Franklin

For more than 50 years, silicon transistors have been continuously shrunk to meet the projections of Moore's law but are now reaching fundamental limits on speed and power use. With these limits at hand, nanomaterials offer great promise for improving transistor performance and adding new applications through the coming decades. With different transistors needed in everything from high-performance servers to thin-film display backplanes, it is important to understand the targeted application needs when considering new material options. Here the distinction between high-performance and thin-film transistors is reviewed, along with the benefits and challenges to using nanomaterials in such transistors. In particular, progress on carbon nanotubes, as well as graphene and related materials (including transition metal dichalcogenides and X-enes), outlines the advances and further research needed to enable their use in transistors for high-performance computing, thin films, or completely new technologies such as flexible and transparent devices.

Fifty years ago, Gordon Moore published his seminal paper that included a projection that the semiconductor industry would double the number of components on a chip (integrated circuit) roughly every couple of years (*1*). Although slightly modified over time, this projection from one of Intel's founders has served as the marching orders for what is now a >$330 billion global industry (*2*) and has been given the moniker "Moore's law." Notable innovations have allowed the silicon metal oxide semiconductor field-effect transistor (MOSFET) to be made smaller, the latest being from strained-silicon channel materials to three-dimensional (3D) fin gate structures, as depicted in Fig. 1C. Despite these advances, fundamental physical limits for the minimum size of silicon MOSFETs are now being approached, and the question of "what's next" for transistors has become inescapable.

The microprocessor, now driven by billions of MOSFETs on a single chip, is the most prominent transistor application, as it is the computational "brain" to every electronic system. Yet there are other needs for the transistor that do not necessarily require the high performance (and high cost) of MOSFETs—for example, chemical and biological sensors, optical detectors, and the pixel-driving circuits for displays. Aside from the microprocessor, the most prominent use of transistors is in the backplane electronics of flat-panel displays. Departure from the cathode ray tube was made possible, in part, by the use of low-cost amorphous silicon (a-Si) thin-film transistors (TFTs) in liquid-crystal displays.

Department of Electrical and Computer Engineering and Department of Chemistry, Duke University, Durham, NC 27708, USA. **E-mail: aaron.franklin@duke.edu**

That a-Si TFTs were made from silicon is one of very few attributes TFTs have in common with silicon MOSFETs. MOSFETs are generally high-performance and high-cost transistors used for computational devices (e.g., smartphones, computers, servers), whereas TFTs are less cost intensive and are used in applications with much lower performance requirements. Consider the different perspectives on Moore's law shown in Fig. 1 for these two types of transistors. The traditional Moore's law in Fig. 1A is obeyed by high-performance transistors, wherein the density of devices doubles approximately every 2 years (*3*). For TFTs, the integration density has changed relatively little, with the focus being more on improving stability and driving down cost. The Moore's law perspective in Fig. 1B focuses on the component substrate size (*4*); here, the trend for TFTs is based on the display market, where the ability to fabricate large areas of transistors is crucial (*5*). Meanwhile, the die size of the MOSFET—the area of a single chip on a much larger production wafer—has been capped at ~300 mm^2 to minimize production costs by yielding more chips per wafer. Overall, these two perspective plots highlight the importance of recognizing the differences in applications and deliverables between high-performance transistors and TFTs.

Nanomaterials are of great interest for use in transistors of all types, as they offer many electrical and mechanical advantages. Unlike silicon-based transistors, the general structure of a nanomaterial transistor changes very little between the high-performance and thin-film varieties, except in size (see Fig. 1C). This similarity has led to much confusion in the research community as to whether certain reported nanomaterial transistor advancements are useful for high-performance or thin-film applications. Such confusion occurs only for nanomaterials, as the silicon community developed different materials expressly for TFTs. Consider the substantial difference in target performance metrics—often orders of magnitude—between high-performance transistors and TFTs (from any material), as shown in Table 1. In this Review, in addition to considering the great progress and promise in the field of nanomaterial transistors, clarification of this important distinction between the intended application spaces will be provided. Guided by an understanding of the relevant dimensional and performance targets (see Table 1), it is hoped that future research on nanomaterial transistors can more accurately address the scientific challenges limiting their ultimate realization.

Nanomaterials

The term "nanomaterial" can refer to any material with dimensions at the nanoscale (<100 nm), but for transistor applications, the materials that naturally exhibit quantum confinement and occur without the need for thinning or patterning are of greatest interest. Hence, the focus of this Review will be on such naturally quantum-confined nanomaterials, including single-walled carbon nanotubes (CNTs), graphene, transition metal dichalcogenides (TMDs), and X-enes (the newest and least naturally occurring variant of 2D crystals, typically consisting of a buckled hexagonal structure to mimic graphene—hence the name "X-ene"; examples include phosphorene for phosphorous and silicene for silicon). There certainly are benefits in transistors from other types of nanomaterials, such as nanowires (*6*, *7*), which are nanoscale versions of bulk materials. However, it is typically best to avoid quantum confinement in such materials rather than embrace it as a key aspect of their electronic structure because it would introduce considerable variation in the resulting device performance and degrade carrier transport properties. Most of the nanomaterials discussed herein are often classified as van der Waals materials, as they do not covalently or ionically bond to other materials but exist as 1D or 2D constituents that are either isolated or assembled in some fashion via van der Waals weak attraction forces.

Extensive articles reviewing the distinctive properties of each of these nanomaterials have been published (*8*–*15*); as the focus of this Review is on the use of the nanomaterials in transistors, only a brief summary of their key attributes is given. Of note is that single-walled CNTs and graphene share the sp^2-bonded, hexagonal carbon lattice and thus exhibit similar carrier transport properties, including high Fermi velocity (v_F), which can lead to higher switching speeds. Low effective mass and correspondingly high carrier velocity make CNTs and graphene the most ideal electron transport systems available. Consequently, CNTs are favorable options for very small transistors that can operate at low voltages, thus conserving power, because silicon-based transistors suffer degradation in

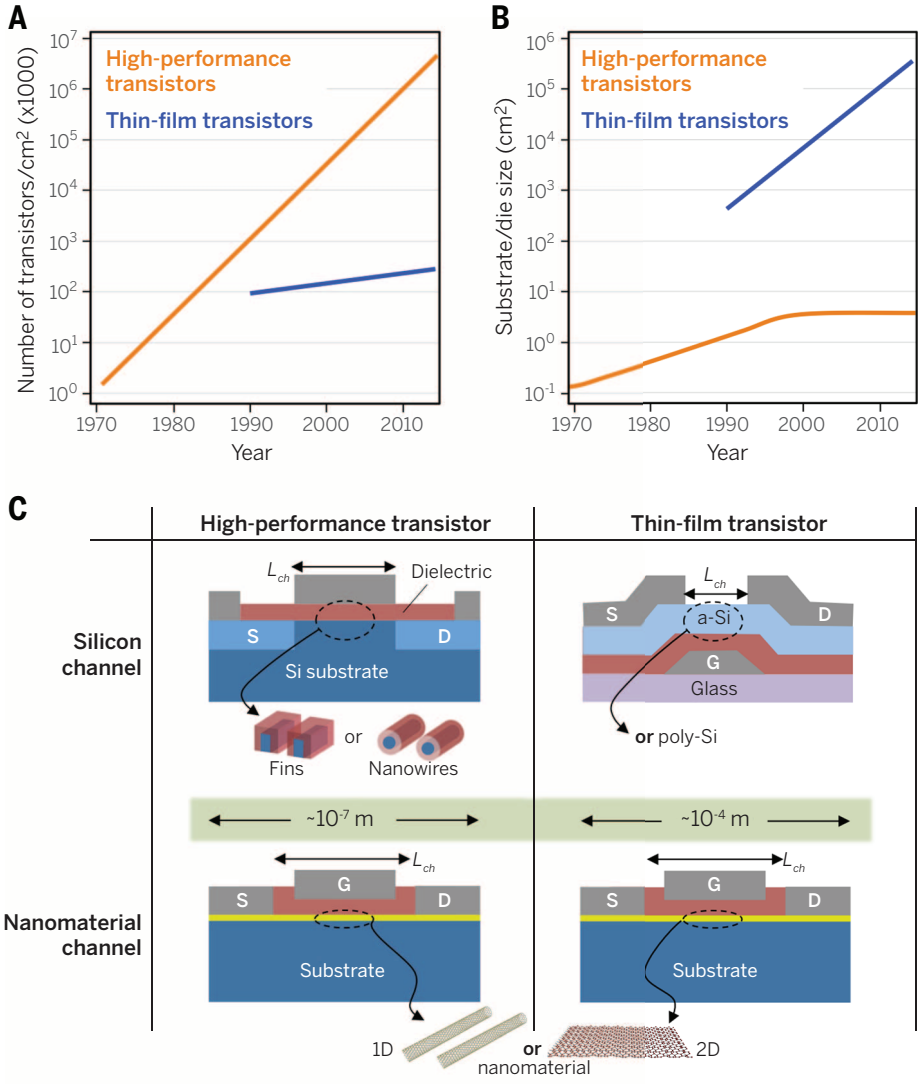


Fig. 1. High-performance transistors versus TFTs: Moore's law and device comparison. (**A**) Approximate plot of Moore's law, showing increasing density of integrated transistors (reduction of transistor size). High-performance transistors exhibit the traditional trend, with a density that doubles approximately every 2 years, whereas there has been little change in the approximate density of TFTs. (**B**) A different view of Moore's law, showing the approximate substrate or die size for the two transistor technologies over time (TFT substrate size is based on display applications and has doubled every ~2.5 years). For (A) and (B), lines are approximate fits to actual data, as in (*3*, *4*). (**C**) Cross-sectional schematics comparing the general structure of high-performance transistors and TFTs with silicon versus nanomaterial channels. Note that the latest high-performance silicon device could consist of fins (3D) or nanowire channels, as shown. Also indicated is the channel length L_{ch} for each device. In the nanomaterial channel transistors, where the channel is made up of 1D or 2D nanomaterials, there is little difference in structure between high-performance transistors and TFTs, yet size differs by orders of magnitude—a key source of confusion in the field. S, source; G, gate; D, drain.

performance (e.g., leakage currents) when operated below ~1 V. The nanotubes, which can be conceptualized as rolled up sheets of graphene, are circumferentially quantum-confined, which makes them true 1D electronic systems with reasonable energy band gaps that allow them to turn off with little leakage current. The lack of an energy band gap in graphene is the nanomaterial's greatest pitfall for transistors, rendering the devices unable to block current flow and be switched to the off state (digital "0"). Great efforts have been made to induce a band gap in graphene (*16*, *17*), but to date, they lack practicality. Even thinning graphene to create quasi-1D nanoribbons (*18*, *19*) to create a band gap still has disadvantages, such as edge states, compared with the naturally 1D nanotubes. The most likely use of graphene in digital transistors arises from its ability to enable distinct 2D heterostructures, which will be discussed below. A summary of some of the most relevant intrinsic properties of these nanomaterials for electronics applications is given in Fig. 2. Note that the focus in Fig. 2 is not given to mobility or extrinsic device metrics, such as contact resistance, as these are only relevant in certain devices or are highly variable, depending on specific interfacial materials. Further discussion of such other metrics is given below.

The interest in studying graphene for transistors spurred reconsideration of a very well-known class of van der Waals nanomaterials that had not been studied for electronics in many years: TMDs. Many combinations of transition metals (e.g., Mo, W, Hf) and chalcogens (e.g., S, Se, Te) can yield the three-atom-thick arrangement of a monolayer TMD (*9*). For transistors, the greatest interest has been in the Mo and W families, especially MoS_2. Electron transport in TMDs is slower by a factor of 20 compared with carbon nanomaterials, but TMDs offer sizable energy band gaps for switching and maintain the attractive 2D confinement of graphene. If more than one monolayer is stacked to form a many-layer TMD, the band gap changes markedly, typically saturating to approximately the bulk value at ~15 layers with a gap that is barely two-thirds that of the monolayer.

Most recent to join the options of nanomaterials for transistors is the so-called X-ene family (*20*–*26*). Exploration began a few years ago, motivated by the electronic structure of graphene, including a linear dispersion relation of Dirac cones, for other group IV and V nonmetals arranged in a similar fashion to the graphene hexagonal lattice. Thus far, demonstrations of silicene (silicon) (*21*), germanene (germanium) (*24*), phosphorene (black phosphorus) (*23*, *25*, *26*), stanene (tin) (*20*), and arsenene (arsenic) (*22*) have been made. Their lattice structures are not as perfectly planar hexagonal as that of graphene but tend to be some variation in a buckled hexagonal form (*20*). Phosphorene exhibits van der Waals stacking, but the other X-enes are synthesized as adlayer structures on certain substrates. Limited experimental work has been performed on X-enes, but theoretical projections indicate potentially attractive electronic properties, including the presence of a reasonable band gap and transport behavior about half as favorable as that of graphene (Fig. 2). One of the biggest challenges for X-enes compared with other nanomaterials is that X-enes tend to be highly reactive in air, making even simple device structures extremely difficult to realize (*21*).

To consider the progress that has been made in demonstrated nanomaterial transistors, a summary of a few key device metrics is given in Fig. 3A. For high-performance transistors, there is a need to scale the channel length L_{ch} and contact length L_c while operating at low voltage V_{DD}. Note that the approximate progress shown for each metric in Fig. 3A is from diverse reports; in other words, there has yet to be a solution that shows the scaling of all relevant dimensions along with low-voltage operation. As will be discussed below, the focus for TFTs is on mobility μ and on-state current I_{on}, where nanomaterials have already shown substantial improvements over silicon-based options. Based on the Fig. 3A comparisons, CNTs show the most consistent promise thus far,

which is partly an artifact of their being studied the longest but also undoubtedly related to their superior carrier transport properties compared with the TMDs or X-enes. These metrics are certainly not comprehensive, but when considering any of these nanomaterials for the indicated applications, such target deliverables must be kept in mind.

Benefits of nanomaterials

Despite the substantial differences in intrinsic properties among the nanomaterial options, they have common advantages for transistors, as summarized in Fig. 3B. Foremost, nanomaterials are all atomically thin. For high-performance transistors, there is a need to scale the channel length to sub–10-nm dimensions because this will be required for technologies targeted for the early 2020s, and silicon is unable to operate at such length scales. Such scaling requires the transistor gate to maintain electrostatic control over the channel—a difficult feat when the channel thickness (d_{body}) is greater than L_{ch}. The atomic thinness of nanomaterials, especially in their monolayer form for 2D nanomaterials, offers ideal electrostatic control. Often the ultimate scalability of a transistor with an undoped (intrinsic) channel—such as all nanomaterials shown in Fig. 2—is determined by the screening or natural length λ being proportional to d_{body}. The rule-of-thumb is that a $L_{ch} \geq 3\lambda$ will ensure that the gate maintains electrostatic control and that deleterious short-channel effects are avoided (*27*).

Another benefit shared by most nanomaterials is their substrate independence. CNTs can be synthesized in a reactor chamber, dispersed in solution to isolate a certain diameter or energy band gap (*28*–*38*), and then deposited onto any substrate of choice, all while keeping their crystal structure and transport properties intact. The same is true for graphene and TMDs, with the exception of X-enes, as they are generally substrate-bound (except for phosphorene). Although synthesis conditions are extreme in most cases, the ability to transfer nanomaterials to virtually any substrate and fabricate transistors from them is one of their greatest strengths.

Heterostructures of the nanomaterials in Fig. 2 are becoming an attractive possibility for transistors, including the use of all 2D nanomaterials for fabricating transistors (e.g., graphene contacts, TMD channel, and hexagonal boron nitride gate dielectric) (*39*–*41*), as well as the stacking of diverse TMDs in a fashion similar to epitaxial III-V materials (*42*–*49*). Work continues on understanding what governs transport at these nanomaterial heterostructure junctions. Several devices that make explicit use of such heterostructures in their operation have been demonstrated, and it will be exciting to see the types of new transistors this approach will enable.

Other strengths that nanomaterials offer for transistors typically depend on device structure or type. For instance, the presence of a small quantum capacitance (dependent on the density of states), especially in CNTs, has been shown to enable more extensive modulation of the surface potential in the on state of a transistor (*50*). Operation in this quantum capacitance limit is of great value for tunneling transistors, for which the thinning of tunnel barriers to achieve higher current is crucial. Other nanomaterial properties that are useful for specific devices include spin transport, Coulomb blockade, charge density

Table 1. Comparison of key target metrics for high-performance transistors and TFTs. Channel length is defined in Fig. 1 and is critical for the packing density of transistors. I_{on} indicates the on-state performance, including transistor speed. V_{DD} reflects the off-state performance, with lower V_{DD} needed for densely integrated high-performance applications. Mobility is discussed below and has become relevant only for TFTs. Process complexity is given in terms of the number of mask layers or levels used to fabricate the transistors. Although this number will vary for high-performance transistors, depending on the application (digital logic versus memory, server chip versus low-power system-on-chip, etc.), the approximate average is given and clearly shows the advantage for TFTs with <20% the process complexity. Cost for fabrication line or facility (fab) is based on the most recent facilities reported—and the numbers for TFTs are for fabs that produce full OLED displays (not just the TFT backplane)—yet it is still considerably cheaper than a high-performance transistor fab. The dash indicates no ability to numerically compare.

Metric	High-performance transistors	Thin-film transistors	Difference
Channel length (L_{ch})	<20 nm	5 to 10 μm	250×
Drive current (I_{on})	>1 mA/μm	>10 μA/μm	100×
Operating voltage (V_{DD})	<1 V	3 to 5 V	3× to 5×
Mobility (μ)	see Fig. 4	0.1 to 100 cm^2/Vs	–
Process complexity	>40 mask layers	<7 mask layers	5.7×
Cost for fab	$4 billion to $10 billion	$1 billion to $3 billion	3× to 4×

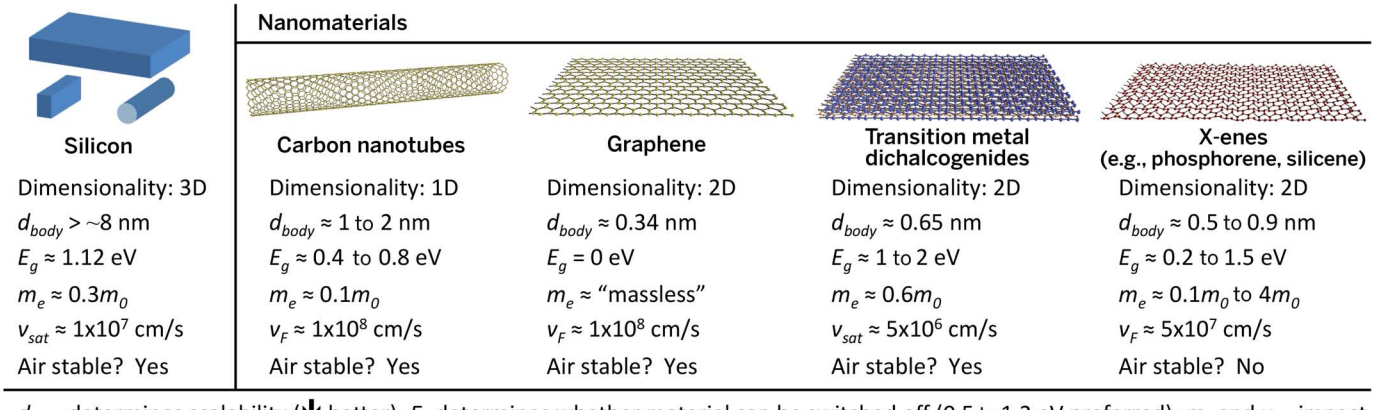


Fig. 2. Nanomaterial options for transistors. A comparison of key intrinsic attributes of the four most prominent nanomaterials (or families of nanomaterials) is shown contrasted with the related attributes of silicon. Carbon nanotubes and graphene share the sp^2 bond structure and thus many electrical transport properties, with the exception that the nanotubes are circumferentially quantum confined to form 1D cylinders with band gaps. The TMDs that are most amenable for transistors are the Mo and W families (e.g., MoS_2, WSe_2). X-enes, typically consisting of a buckled hexagonal structure and lacking stability in air, are the newest and least naturally occurring variant of 2D crystals. The channel or body thickness (d_{body}) limit for silicon is based on the onset of quantization effects that must be avoided for a bulk material. E_g, band gap; m_0, electron rest mass; v_{sat}, saturation velocity; v_F, Fermi velocity.

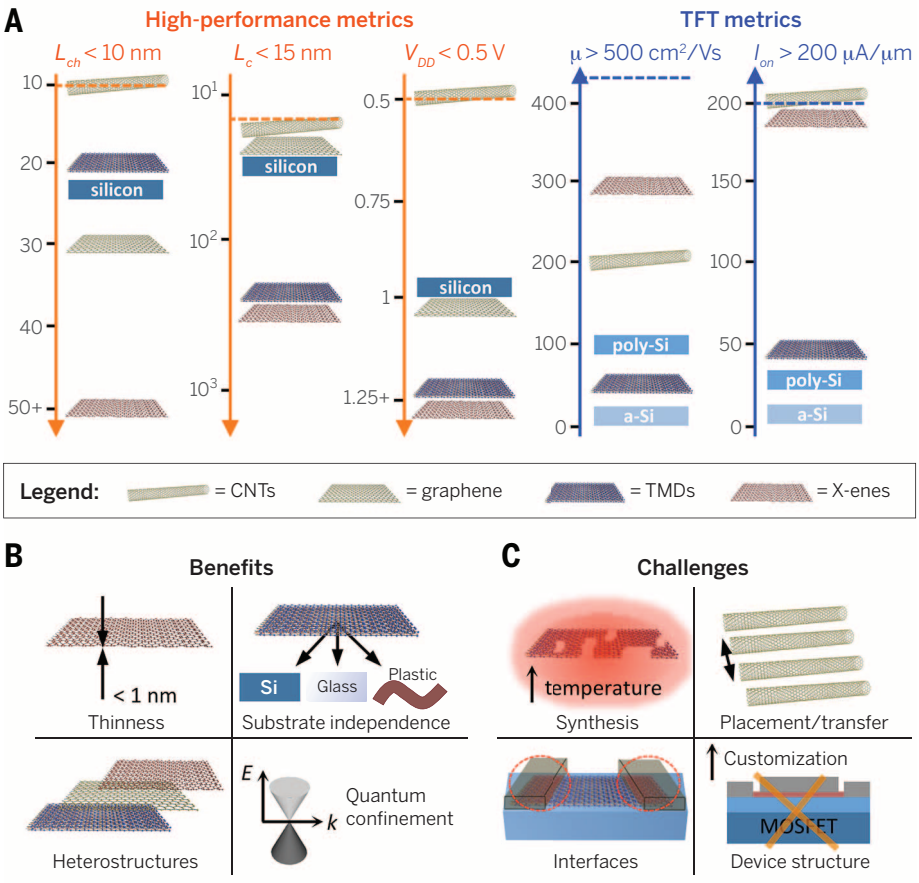


Fig. 3. Performance comparison, benefits, and challenges for nanomaterials in transistors. (**A**) Approximate comparison of demonstrated performance or device metrics, where L_{ch} is channel length and L_c is contact length (length over which the metal contact covers the nanomaterial). Note that the approximate values for the nanomaterials are from reports involving transistors with relevant dimensions and structure, and the metrics would need to be simultaneously met (along with others not included) for the targeted transistor technology. Also shown are the approximate values for the most advanced transistors from silicon-based materials. (**B**) Overview of transistor benefits offered by all nanomaterials, including atomic thinness, substrate independence, potential for heterostructures, and distinctive electronic properties. *E*, energy; *k*, wave number. (**C**) Overview of challenges shared in some fashion by all nanomaterials for transistors, including high-quality synthesis, controlled placement, improved interfaces (contact and dielectric), and devices that more fully utilize nanomaterial advantages.

waves, and plasmons, but the focus of this Review will be on more conventional digital transistors.

Challenges for nanomaterials

Just as the nanomaterials in Fig. 2 share many advantages for transistors, they also have challenges in common, as summarized in Fig. 3C. Without question, the biggest challenges relate to the controlled synthesis and placement of the nanomaterials. Although there has been widely varied progress on addressing the synthesis and placement challenges among the different nanomaterials, they all require substantial improvement to be viable for a transistor technology. Synthesis of nanomaterials takes place at high temperatures (typically >800°C). In most cases, the nanomaterials are synthesized on a sacrificial substrate and then transferred in some fashion to the substrate for fabricating transistors. Whether or not they are kept on their synthesis substrate, the distribution in d_{body} (diameters for CNTs and number of layers for 2D nanomaterials) must also be controlled. Tremendous progress has been made in separating CNTs of certain electronic type (band gap in CNTs is dependent on d_{body}) (*28*–*38*), which indicates promise for reaching technology targets so long as scientific investment continues (current highest verified purity is 99.99% with a target of 99.9999%) (*51*). Progress has also been made in synthesizing TMDs (*52*–*60*), although there has yet to emerge a process capable of growing a TMD with complete coverage, high quality (low defect and grain boundary density), and a uniform number of layers. Being the newest explored nanomaterial and not exhibiting van der Waals stacking behavior, X-enes have the farthest to go for improved synthesis.

If the nanomaterial is synthesized on one substrate and then transferred to another for transistor fabrication, then precision placement is important. For CNTs, this problem is especially pronounced, as they require accurate positioning into arrays. The target pitch for CNTs in high-performance transistors is 5 to 8 nm (125 to 200 CNTs per micrometer) (*13*), and promising advancements continue to be made to this end (*61*–*68*), including the use of selective deposition to predefined regions of a substrate (50-nm pitch achieved). It is less favorable to have tightly packed (~0-nm pitch) arrays of CNTs for high-performance transistors (*62*), as they will result in deleterious charge screening effects and challenges for establishing good electrical contacts. Requirements for TFTs are much more relaxed, where even tangled films of CNTs with no alignment can be used (*69*–*71*). The 2D nanomaterials do offer planar coverage, but it is difficult to transfer the films without inducing defects that are detrimental to transistor performance. An additional complication for X-enes is their pronounced dependence of carrier transport on crystallographic direction (*23*); orientation of the X-ene film will change the effective mass of the carriers by up to one order of magnitude.

Interfaces to nanomaterials are another challenge. Without having available surface states in the way that bulk materials do, the formation of covalent bonds to nanomaterials can be difficult. For instance, nucleating the growth of high-quality dielectrics (insulating barriers) with atomic layer deposition (ALD) is problematic for nanomaterials, as they do not offer typical end groups for reacting with the ALD precursors. Creative solutions have been presented for potentially addressing the creation of high-quality dielectric interfaces (*72*–*75*), but there has been much less progress on improving the contact metal interfaces. Regardless of whether a nanomaterial transistor is for high-performance or thin-film applications, the device will depend heavily on the quality of transport at the source and drain metal contact interfaces. Studies have been performed on the impact of different metals on the contact resistance for CNTs (*76*–*78*), TMDs (*79*–*81*), and even X-enes (*82*), most of which consider the metal-nanomaterial interface as a traditional Schottky barrier structure. However, with no covalent bonding between the metal and nanomaterial, the reality of what determines transport at the interface remains elusive, and the Schottky barrier picture has been shown to break down under certain conditions (*78*).

In all cases, the metal-nanomaterial contact interface requires further scientific study and engineering improvement to yield the necessary performance and consistency for a transistor technology. Many have interpreted this to simply mean the achievement of low contact resistance (R_c), but depending on the transistor application, realizing a low R_c may not address all of the relevant contact issues, including scalability and reproducibility. For example, for high-performance transistors with contact lengths <15 nm (see Fig. 3A), the target R_c must be <150 ohm·μm (measured contact resistance multiplied by device width) per contact (*78*)—a

substantial challenge even at very long (>200-nm) contact lengths.

A final point regarding challenges for nanomaterials in transistors is the need for further discovery and innovation of the transistor structures. Thus far, nanomaterials are integrated into transistors that essentially mimic the silicon MOSFET, especially for high-performance applications (Fig. 1). Considering their substrate independence, there are undoubtedly much more favorable transistor structures that have yet to be discovered for nanomaterials. Such structures would take more specific advantage of the electrical and mechanical properties of nanomaterials for boosting performance, lending new functionality, or both for certain applications. Additionally, regardless of the transistor structure into which nanomaterials are integrated, a need remains for studying the reliability of resultant devices and circuits to ensure their utility under certain application requirements, such as high clock speeds.

High-performance transistors

High-performance transistors are those that enable the primary computing electronics that we rely on daily. Servers that fill warehouses (server farms) are the lifeblood of the Internet and rely on the highest-performing scaled transistors. Semiconductor companies such as Intel and Taiwan Semiconductor Manufacturing Company will develop the transistor technology—for example, "14 nm" (*83*)—for the highest-performance applications and then use mostly the same transistor for other less-demanding applications. An example is the low-power chips that are used for mobile electronics (e.g., smartphones, tablets, laptops), where the chip will still make use of transistors with the latest technology (14 nm) but will be integrated less densely and run at lower voltages. In this case, the term "high-performance transistor" refers to the transistor technology itself that is applied to all such peripheral applications—from servers to smartphones.

A closer look at Moore's law for high-performance transistors, given in Fig. 4, helps to highlight why nanomaterials are so advantageous. In the early 2000s, the performance (as measured by chip clock frequency) was necessarily capped to address the runaway power density problem (*84*): Smaller transistors could leak power even in the off state, leading to power-consumption and heat-generation issues. Anything beyond ~100 W/cm^2 is detrimental to the chip and surrounding components; heating a semiconductor causes performance fluctuations, and the ability for cooling technologies to dissipate the heat is limited to ~100 W/cm^2. Active power (P_A) depends on clock frequency (f), operating voltage (V_{DD}), and the number of transistors per square centimeter (N) as $P_A \propto N^* f^* (V_{DD})^2$. With Moore's law demanding that N continue to increase, the most logical solution would be to reduce V_{DD} because of the squared dependence. However, the cost in terms of performance was too great, and V_{DD} has remained pegged for more than a decade at ~1 V for high-performance transistors. Reducing f would also seriously compromise performance, leading to the need for multicore architectures. The advantage of multicore chips in terms of the power problem is that the architecture ensures that, at any given time, a much smaller fraction of the transistors will be turned to the on state than for a single core chip—a phenomenon known as dark silicon (*85*). However, the multiplication of the number of cores will hit a level of maximized benefit at ~16 cores, leaving reduction of V_{DD} the only hope for further progress.

Nanomaterials offer several ways of reducing the operating voltage in high-performance transistors. First, their atomic thinness enables highly effective gate control over the channel potential through the reduced screening length discussed above. Improved gate control means that even at aggressively scaled channel lengths (needed for driving an increase in N), nanomaterial transistors can switch to the on state at the lowest possible voltages (i.e., small subthreshold swing, which is an indicator of how many volts are required to switch the current in a transistor by one order of magnitude). The subthreshold swing is referred to as the performance metric in the off state, indicating the ability of a transistor to switch at low voltages. Beyond improved gate control, nanomaterials also enable advanced transistor structures that may offer solutions for scaling V_{DD}. One such option is the tunneling transistor, where the small effective mass (m_e) in CNTs (as well as some 2D options) would offer dramatic improvement (increase) in the tunneling current to boost the on state, which limits the realization of these transistors (*86*, *87*).

Exceptional electron transport in most nanomaterials is another attractive feature for high-performance transistors. In the case of CNTs, nearly ballistic (zero resistance) transport has been observed at room temperature at lengths up to 40 nm (*88*, *89*). Such favorable transport has experimentally been shown to enable sub–10-nm CNT transistors that outperform any similarly scaled silicon-based transistor at low voltages ($V_{DD} \leq 0.5$ V) (*90*). Transport in TMDs is actually worse than in most bulk semiconductors, including silicon; yet at sufficiently scaled channel lengths, TMDs could still offer advantages, as performance in the transistor will become dominated by contacts rather than transport through the channel. For the required dimensions of a high-performance transistor, the performance of every device will be determined more by the contacts than by the channel, regardless of whether it is a nanomaterial or silicon or any other semiconductor. For this reason, the use of the prevalent transport metric, mobility, must be reevaluated.

Mobility

One of the most widely used metrics for describing the quality of carrier transport through a semiconductor is mobility (μ). Initially defined as the constant of proportionality between carrier velocity and the electric field across a material, μ has often been considered an intrinsic indicator of semiconductor quality and even quoted in textbook tables. Though it is understood that μ depends on other factors such as doping density and temperature, it has nevertheless been taken as the most important parameter for semiconductor consideration. In fact, consideration of channel materials other than silicon (which suffers from a relatively low μ compared with other bulk semiconductors) for high-performance transistors has largely focused on semiconductors with higher mobility, eventually leading to the classification "high-mobility semiconductors" (usually germanium or III-V compound semiconductors, such as GaAs, which despite higher mobility have other issues in achieving high levels of integration).

For the first 50 years of Moore's law, using mobility as a key parameter to indicate the quality of a semiconductor for transistors made sense. Channel lengths were long enough to yield an average transport length between scattering events (mean free path) or time between scattering events (mean free time τ) and, thus, a certain mobility: $\mu = q\tau/m_e$ (here, q is elementary charge of an electron). What happens if the channel length falls below the average length between scattering events, or, in the most extreme case, what happens if the channel is ballistic? As shown in Fig. 5, the use of mobility in such a short-channel transistor is misleading, as it no longer accurately indicates the quality of carrier transport through the semiconducting channel.

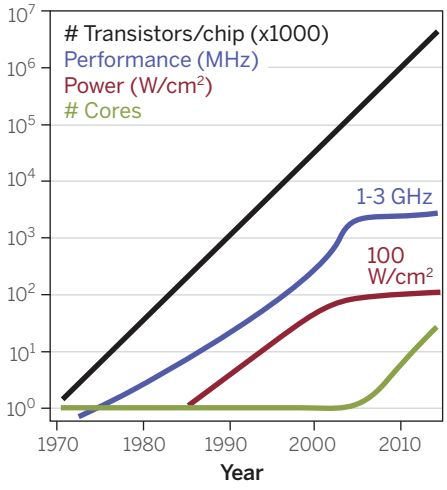


Fig. 4. Detailed look at Moore's law for high-performance transistors. Approximate plot of various metrics in high-performance microprocessors over the past >40 years [lines are approximate fits to actual data, see (*3*)]. The oft-quoted version of Moore's law is the number of transistors per chip (black line), but key trade-offs in chip performance (clock frequency, blue curve) have been made since the early 2000s because of the power density (red curve) reaching a physical limit of ~100 W/cm^2. Continued Moore's law scaling of high-performance transistors has been sustainable only by multicore architectures (green curve)—and the associated "dark silicon"—for the past decade.

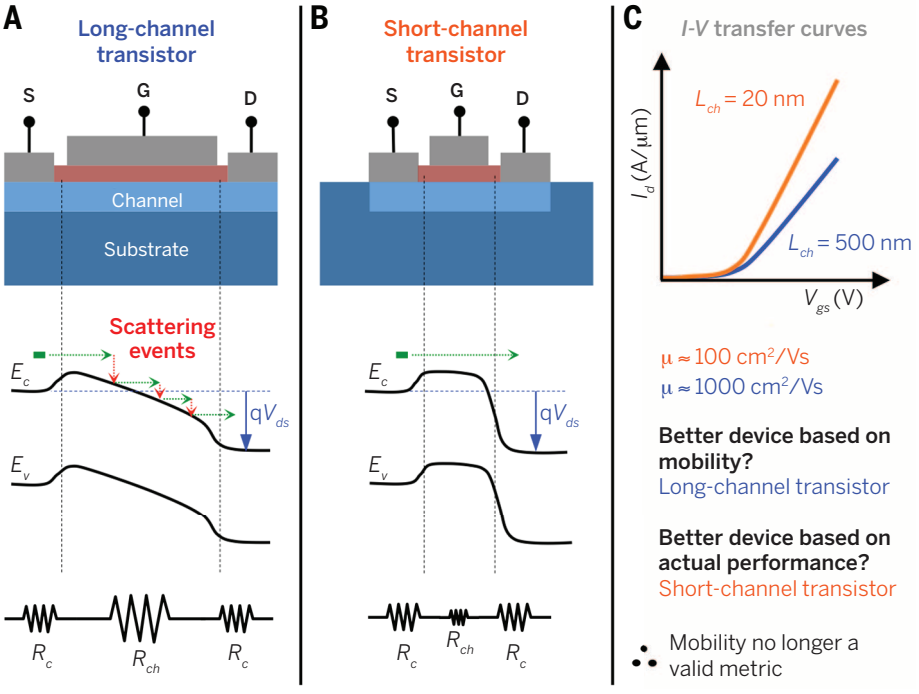


Fig. 5. Is mobility meaningful for all transistors? (**A**) Generic schematic of a long-channel transistor with a corresponding energy band diagram illustrating how the scattering events (red) of electrons (green) moving across the channel lead to a potential drop (sloped bands) of the applied drain-source field (qV_{ds}) and, hence, a substantial resistance in the channel (R_{ch}) compared with resistance at the contacts (R_c). E_c, conduction band edge; E_v, valence band edge. (**B**) Same as (A), but for a short-channel transistor where there are very few scattering events in the channel (quasi-ballistic) and hence the potential is dropped at, and the device is limited by, the contacts. (**C**) Conceptual transfer curves for the two devices, showing how mobility (μ) mistakenly suggests better performance in the long channel. This diagram illustrates why mobility is no longer a meaningful metric for short-channel (high-performance) transistors but is still valid in long-channel (thin-film) transistors. *I*, current; *V*, voltage; I_d, drain current.

With performance in short-channel transistors being determined almost exclusively by the injection of carriers at the source-drain contacts, extraction of mobility from device data defies the actual meaning of the parameter. The example in Fig. 5 illustrates how the band structure and relevant resistances change between long- and short-channel transistors. Extraction of mobility from two such transistors could yield μ that is an order of magnitude smaller for the short-channel devices, even though the performance is much better. This is a fallout of the widely used field-effect mobility expression, wherein $\mu = g_m L_{ch}/(WCV_{ds})$ (here, W is the device width, C is the capacitance, and V_{ds} is the drain-source voltage), where the transconductance (g_m) goes up but not nearly as much as L_{ch} goes down when scaling from long to short channels (all other terms remain the same). The contacts, including R_c, are identical in the two devices, as is the applied voltage, but the extraction of mobility from the device data relies on the assumption that transport is limited by the scattering in the channel, as in the long-channel case.

In reality, mobility is no longer meaningful for high-performance transistors (all of which are of the short-channel variety), regardless of whether they have silicon, III-V materials, or nanomaterial channels. The saturation velocity of carriers will matter, as will the effective mass, for determining how well carriers move through the channel. Consider the difference in common expressions for current in a long-channel (traditional) MOSFET (*91*)

$$I \approx \mu \frac{W}{L_{ch}} C_{ox}(V_{gs} - V_t)V_{ds}$$

versus a 1D short-channel nanomaterial transistor (*92*)

$$I \approx q\int f(E,T) \cdot v(E) \cdot T_p(E) \cdot D(E) \cdot dE$$

In addition to voltage dependencies [gate-source voltage (V_{gs}), threshold voltage (V_t), and V_{ds}], current in the long-channel transistor depends on mobility, gate capacitance (C_{ox}), and spatial parameters (W and L_{ch}). In contrast, the short-channel nanomaterial transistor shares none of these dependencies. Rather, the current for the 1D nanomaterial transistor relies on the Fermi function [f (indicates electron distribution)]; carrier velocity (v); transmission probability (T_p), including the probability that carriers will make it through the metal-nanomaterial contact without scattering; and density of energy states (D), with respect to energy (E) and temperature (T). The only material consideration in the long-channel expression is μ, whereas the short-channel transistor accounts for D, v, and f, as these are the material-related parameters that become relevant when scattering in the channel is minimal. Hence, at this point of development, relying on mobility as a metric when discussing options for high-performance transistors causes confusion and distraction from the parameters that matter most. This is especially true for nanomaterials, for which reports of mediocre mobilities extracted from short-channel transistors undercut the actual potential of the material. Mobility remains a useful parameter for comparing TFTs, as they are long-channel devices.

Thin-film transistors

There are many applications for which a digital transistor switch is needed without the extreme performance requirements of computational devices. This became especially clear in the 1980s, when a revolution was beginning to stir in display technology with the need for a more compact, mobile display for laptops. Liquid crystal displays were favored but needed transistors for the backplane to drive the pixels. In 1981, researchers showed that a-Si provided the answer—it could be deposited onto glass substrates, was mostly stable, and had sufficient mobility (0.1 to 1 $cm^2\ V^{-1}\ s^{-1}$) to yield the necessary level of drive current (I_{on}). The size of the a-Si TFTs did not have to be small, as the typical pixel is on the order of 100 μm by 100 μm, and the TFTs needed to be large to provide the required I_{on}. Perhaps most importantly, the a-Si TFTs could be fabricated on large substrates at relatively low cost.

With a-Si TFTs, the display revolution began. Shortcomings, including bias-stress instability (change in the voltage needed to turn the TFT on after prolonged operation) and low mobility, led to development of other TFT options, including polysilicon (μ ~ 100 $cm^2\ V^{-1}\ s^{-1}$) (*4*). Although too costly for replacing a-Si in the backplane, polysilicon has become important for display driver circuits in mobile applications, as it is still considerably cheaper than using high-performance MOSFETs. Much effort was devoted to using polysilicon to drive organic light-emitting diode (OLED) displays, which require much higher drive currents than a-Si TFTs could ever deliver, but the nonuniformity in threshold voltage in the polysilicon TFTs gave concern for causing nonuniformity in display brightness (*5*). The latest advancement has been the use of metal oxide materials—in particular, InGaZnO (IGZO), which offers manufacturing costs on par with a-Si, mobility near that of polysilicon, and better stability. IGZO TFTs now drive the latest OLED displays on the market, yet they have their own limits based on processing temperature and mobility pegged at ~100 $cm^2\ V^{-1}\ s^{-1}$ for reasonable synthesis temperatures.

Nanomaterials hold much promise for TFTs. Even though being formed into an inhomogeneous thin film seems to belie the advantages of the nanomaterials, they still are shown to deliver superb performance and processing benefits. For example, CNTs that are simply drop cast from

solution onto a substrate to form a thin film (the cheapest fabrication approach possible, as it is amenable for printing processes) consistently deliver mobilities of 10 to 100 $cm^2 V^{-1} s^{-1}$ (*69*–*71*, *93*–*95*). Further efforts to induce alignment in the CNT thin films could boost mobility much higher than 100 $cm^2 V^{-1} s^{-1}$ (*68*), which would be revolutionary performance improvement for TFTs processed in solution phase. TMDs have also shown encouraging performance in thin films, with mobilities of 1 to 40 $cm^2 V^{-1} s^{-1}$ (*96*–*100*), but they remain limited by insufficient synthesis to fabricate large numbers of transistors on a single substrate and the required use of high-temperature synthesis (not processed in solution). With cost being one of the most important driving factors for TFT applications, the most promising nanomaterial options are those that help break the cost barrier of current technologies. The most attractive way for this to happen is for a TFT to be printed rather processed in a vacuum or at a high temperature. This strength is beginning to receive attention for nanomaterial TFTs (*101*–*106*).

There are many other applications that benefit from current and future TFT technologies. Displays are presently the largest, and thus the most emphasized, but gas and biological sensors, optical detectors, radio-frequency identification tags, and Internet-of-Things applications also abound. Advancements in TFTs that allow for performance improvement and cost reduction are needed to open the way for a myriad of such exciting applications. Nanomaterials are poised to provide such solutions, requiring further improvement in synthesis and thin-film formation; discovery of better contact interfaces; and realization of stable, consistent TFT operation.

New generation of transistors

Thus far, the focus of this Review has been how nanomaterial transistors have the potential to provide transformative solutions in high-performance and thin-film applications. Yet there are other, completely new and distinct application spaces for which nanomaterial transistors are particularly suited. Just as TFT research is focused more on cost than performance, studies of these new generations of transistors focus on other opportunities, such as optical transparency or biocompatibility. A subset of new-generation transistor applications— including printed electronics (*103*), flexible electronics (*93*), transparent electronics (*40*), and biomedical electronics (*107*)—is depicted in Fig. 6. In addition to these areas (though not specifically highlighted here), nanomaterial transistors are beneficial in harsh environments [high temperature or radiation (*108*, *109*)] such as space or medical imaging applications, where the thinness and small cross-sectional area are among several nanomaterial advantages enabling greater protection from device damage.

The field of printed electronics has grown dramatically over the past 20 years. Relying almost exclusively on organic polymer materials, applications of printed electronics have been quite limited. Nanomaterials have the potential to offer conducting, semiconducting, and insulating printable inks that are compatible, stable, and able to be modulated for specific application needs. Such a toolkit of inks would be groundbreaking for this field that has potential to revolutionize on-the-fly electronics in an analogous fashion to how 3D printing of mechanical structures has transformed prototyping.

Nanomaterials offer some of the most promising possibilities for electronics that are flexible, transparent, or both. In addition to their substrate independence (discussed above), the atomic thinness of the nanomaterials also renders them nearly 100% transparent to visible light and has been exploited in some demonstrated all-2D transistors (*40*, *43*), motivated by the ability to create completely transparent circuits. Furthermore, the electronic properties of nanomaterials have proven to be robust to mechanical deformation for flexible substrate applications.

Finally, biomedical applications that have requirements of biocompatibility could also benefit from nanomaterials (*107*). For in vivo applications, small quantities of nanomaterials could be sufficiently safe to enable diagnostic circuits. Electronics applied directly to the skin are another possibility, where nanomaterials would mostly provide the types of benefits outlined in the flexible electronics discussion above.

Outlook

Transistors have completely transformed our daily lives, in areas ranging from communication to computation to comfort. As the limits of silicon transistors are unavoidably upon us, an intensified consideration of other transistor options is imperative. It is also important to keep clear the relevant deliverables for certain transistor applications spaces: namely, high performance and thin film. High-performance transistors are used in all computational devices, from servers to smartphones, whereas TFTs primarily provide the backplane circuitry for displays. The meaningfulness of parameters such as mobility must be kept in context for the different transistor applications so that scientific advances can be kept in proper perspective.

Nanomaterials, including carbon nanotubes and TMDs, show great promise for both high-performance transistors and TFTs. Not every scientific discovery or advancement benefits both nanomaterial high-performance transistors and TFTs, yet many reports confuse this fact. What is clear from the thousands of demonstrated nanomaterial transistors is that they offer considerable advantages, promoting transformative advancement in high-performance, thin-film, and completely new application spaces. Comparison of the distinctive aspects of the different nanomaterial options, or the transistors

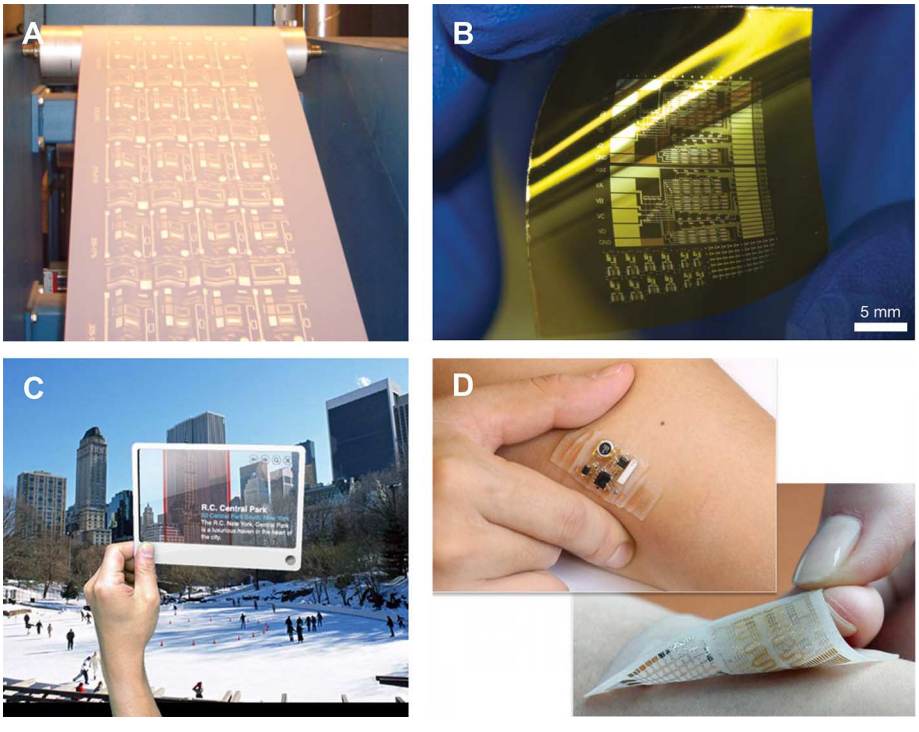


Fig. 6. New application spaces for nanomaterial transistors. (**A**) Printed electronics, where nanomaterials offer air-stable metallic, semiconducting, and even insulating options for the low-cost fabrication of multifunctional electronics. [From (*110*)] (**B**) Flexible electronics. Many demonstrations of nanomaterial transistors on flexible substrates have shown their robustness to mechanical deformation. [Modified from (*93*), with permission] (**C**) Transparent electronics can benefit greatly from the near complete optical transparency of nanomaterials. [From (*111*)] (**D**) Biomedical electronics require materials that can be safely dissolved on skin or even in vivo, and nanomaterials show promise for yielding the necessary function at quantities small enough to be safe. [Modified from (*107*), with permission]

assembled from them, suggests greater suitability of certain nanomaterials for particular applications (e.g., the instability of most X-enes in air largely precludes their use in low-cost, thin-film processing).

Going forward, much work remains in terms of improving the synthesis and resultant uniformity of nanomaterials, positioning them onto target device substrates, understanding and optimizing key interfaces (contacts and gate), and exploring re-invented transistor structures that make more direct use of the nanomaterial benefits. Varied levels of progress have been achieved in addressing these challenges for each nanomaterial, but each requires further attention to be suitable for a transistor technology. The most accessible area in the near term is the use of nanomaterials for printed (low-cost) TFTs, where they are already beginning to show consistent advantages over existing technologies.

Perhaps the greatest challenge to this unprecedentedly large research field of nanomaterial transistors is to make appropriate use of the deluge of scientific and engineering advancements. Hopefully, in the years to come, more collaborative and comprehensive advancements will be published that not only demonstrate a singular breakthrough on one of the challenges for nanomaterials but also give thorough evidence of the impacts of their solution on other key deliverables for a certain nanomaterial transistor application. With sufficient continued research investment into exploring nanomaterial transistors, there is little doubt that 50 years from now the next generation of scientists will be reflecting on a full century of Moore's law, in one form or another.

REFERENCES

1. G. E. Moore, Cramming more components onto integrated circuits. *Electronics* **38**, 114–117 (1965).
2. D. Rosso, "Global semiconductor industry posts record sales in 2014," Semiconductor Industry Association, press release (2 February 2015); www.semiconductors.org/news/2015/02/02/global_sales_report_2014/global_semiconductor_industry_posts_record_sales_in_2014/.
3. J. Hruska, "Stop obsessing over transistor counts: It's a terrible way of comparing chips," *ExtremeTech* (2014); www.extremetech.com/computing/190946-stop-obsessing-over-transistor-counts-theyre-a-terrible-way-of-comparing-chips.
4. R. A. Street, Thin-film transistors. *Adv. Mater.* **21**, 2007–2022 (2009). doi: 10.1002/adma.200803211; pmid: 21161982
5. Y. Kuo, Thin film transistor technology—Past, present, and future. *Interface* **22**, 55–61 (2013).
6. S. Bangsaruntip *et al*., "High performance and highly uniform gate-all-around silicon nanowire MOSFETs with wire size dependent scaling," in *2009 IEEE International Electron Devices Meeting Technical Digest*, Baltimore, MD, 7 to 9 December 2009 (IEEE, 2009), pp. 297–300.
7. D. K. Ferry, Nanowires in nanoelectronics. *Science* **319**, 579–580 (2008). doi: 10.1126/science.1154446; pmid: 18239115
8. R. Ganatra, Q. Zhang, Few-layer MoS_2: A promising layered semiconductor. *ACS Nano* **8**, 4074–4099 (2014). doi: 10.1021/nn405938z; pmid: 24660756
9. A. B. Kaul, Two-dimensional layered materials: Structure, properties, and prospects for device applications. *J. Mater. Res.* **29**, 348–361 (2014). doi: 10.1557/jmr.2014.6
10. S. Z. Butler *et al*., Progress, challenges, and opportunities in two-dimensional materials beyond graphene. *ACS Nano* **7**, 2898–2926 (2013). doi: 10.1021/nn400280c; pmid: 23464873
11. M. C. Lemme, L.-J. Li, T. Palacios, F. Schwierz, Two-dimensional materials for electronic applications. *MRS Bull.* **39**, 711–718 (2014). doi: 10.1557/mrs.2014.138
12. M. Naguib, V. N. Mochalin, M. W. Barsoum, Y. Gogotsi, 25th anniversary article: MXenes: A new family of two-dimensional materials. *Adv. Mater.* **26**, 992–1005 (2014). doi: 10.1002/adma.201304138; pmid: 24357390
13. G. S. Tulevski *et al*., Toward high-performance digital logic technology with carbon nanotubes. *ACS Nano* **8**, 8730–8745 (2014). doi: 10.1021/nn503627h; pmid: 25144443
14. F. Schwierz, Graphene transistors. *Nat. Nanotechnol.* **5**, 487–496 (2010). doi: 10.1038/nnano.2010.89; pmid: 20512128
15. D. Reddy, L. F. Register, G. D. Carpenter, S. K. Banerjee, Graphene field-effect transistors. *J. Phys. D Appl. Phys.* **44**, 313001 (2011). doi: 10.1088/0022-3727/44/31/313001
16. Y. Zhang *et al*., Direct observation of a widely tunable bandgap in bilayer graphene. *Nature* **459**, 820–823 (2009). doi: 10.1038/nature08105; pmid: 19516337
17. F. Xia, D. B. Farmer, Y. M. Lin, P. Avouris, Graphene field-effect transistors with high on/off current ratio and large transport band gap at room temperature. *Nano Lett.* **10**, 715–718 (2010). doi: 10.1021/nl9039636; pmid: 20092332
18. X. Wang *et al*., Room-temperature all-semiconducting sub-10-nm graphene nanoribbon field-effect transistors. *Phys. Rev. Lett.* **100**, 206803 (2008). doi: 10.1103/PhysRevLett.100.206803; pmid: 18518566
19. X. Liang, S. Wi, Transport characteristics of multichannel transistors made from densely aligned sub-10 nm half-pitch graphene nanoribbons. *ACS Nano* **6**, 9700–9710 (2012). doi: 10.1021/nn303127y; pmid: 23078122
20. S. Balendhran, S. Walia, H. Nili, S. Sriram, M. Bhaskaran, Elemental analogues of graphene: Silicene, germanene, stanene, and phosphorene. *Small* **11**, 640–652 (2015). doi: 10.1002/smll.201402041; pmid: 25380184
21. L. Tao *et al*., Silicene field-effect transistors operating at room temperature. *Nat. Nanotechnol.* **10**, 227–231 (2015). doi: 10.1038/nnano.2014.325; pmid: 25643256
22. C. Kamal, M. Ezawa, Arsenene: Two-dimensional buckled and puckered honeycomb arsenic systems. *Phys. Rev. B* **91**, 085423 (2015). doi: 10.1103/PhysRevB.91.085423
23. H. Liu *et al*., Phosphorene: An unexplored 2D semiconductor with a high hole mobility. *ACS Nano* **8**, 4033–4041 (2014). doi: 10.1021/nn501226z; pmid: 24655084
24. M. Derivaz *et al*., Continuous germanene layer on Al(111). *Nano Lett.* **15**, 2510–2516 (2015). doi: 10.1021/acs.nanolett.5b00085; pmid: 25802988
25. K. Lam, Z. Dong, J. Guo, Performance limits projection of black phosphorous field-effect transistors. *IEEE Electron Device Lett.* **35**, 963–965 (2014). doi: 10.1109/LED.2014.2333368
26. H. Liu, A. T. Neal, M. Si, Y. Du, P. D. Ye, The effect of dielectric capping on few-layer phosphorene transistors: Tuning the Schottky barrier heights. *IEEE Trans. Electron. Dev.* **35**, 795–797 (2014). doi: 10.1109/LED.2014.2323951
27. C. P. Auth, J. D. Plummer, Scaling theory for cylindrical, fully-depleted, surrounding-gate MOSFET's. *IEEE Electron Device Lett.* **18**, 74–76 (1997). doi: 10.1109/55.553049
28. B. S. Flavel, K. E. Moore, M. Pfohl, M. M. Kappes, F. Hennrich, Separation of single-walled carbon nanotubes with a gel permeation chromatography system. *ACS Nano* **8**, 1817–1826 (2014). doi: 10.1021/nn4062116; pmid: 24460395
29. M. S. Arnold, A. A. Green, J. F. Hulvat, S. I. Stupp, M. C. Hersam, Sorting carbon nanotubes by electronic structure using density differentiation. *Nat. Nanotechnol.* **1**, 60–65 (2006). doi: 10.1038/nnano.2006.52; pmid: 18654143
30. X. Tu, S. Manohar, A. Jagota, M. Zheng, DNA sequence motifs for structure-specific recognition and separation of carbon nanotubes. *Nature* **460**, 250–253 (2009). doi: 10.1038/nature08116; pmid: 19587767
31. J. Liu, M. Hersam, Recent developments in carbon nanotube sorting and selective growth. *MRS Bull.* **35**, 315–321 (2010). doi: 10.1557/mrs2010.554
32. C. Y. Khripin, J. A. Fagan, M. Zheng, Spontaneous partition of carbon nanotubes in polymer-modified aqueous phases. *J. Am. Chem. Soc.* **135**, 6822–6825 (2013). doi: 10.1021/ja402762e; pmid: 23611526
33. G. S. Tulevski, A. D. Franklin, A. Afzali, High purity isolation and quantification of semiconducting carbon nanotubes via column chromatography. *ACS Nano* **7**, 2971–2976 (2013). doi: 10.1021/nn400053k; pmid: 23484490
34. C. Homenick *et al*., High-yield, single-step separation of metallic and semiconducting SWCNTs using block copolymers at low temperatures. *J. Phys. Chem. C* **118**, 16156–16164 (2014). doi: 10.1021/jp5030476
35. J. Park, P. Deria, J.-H. Olivier, M. J. Therien, Fluence-dependent singlet exciton dynamics in length-sorted chirality-enriched single-walled carbon nanotubes. *Nano Lett.* **14**, 504–511 (2014). doi: 10.1021/nl403511s; pmid: 24329134
36. K. S. Mistry, B. A. Larsen, J. L. Blackburn, High-yield dispersions of large-diameter semiconducting single-walled carbon nanotubes with tunable narrow chirality distributions. *ACS Nano* **7**, 2231–2239 (2013). doi: 10.1021/nn305336x; pmid: 23379962
37. S. Fogden, C. A. Howard, R. K. Heenan, N. T. Skipper, M. S. P. Shaffer, Scalable method for the reductive dissolution, purification, and separation of single-walled carbon nanotubes. *ACS Nano* **6**, 54–62 (2012). doi: 10.1021/nn2041494; pmid: 22206484
38. T. Tanaka, Y. Urabe, D. Nishide, H. Kataura, Discovery of surfactants for metal/semiconductor separation of single-wall carbon nanotubes via high-throughput screening. *J. Am. Chem. Soc.* **133**, 17610–17613 (2011). doi: 10.1021/ja208221g; pmid: 21980975
39. T. Roy *et al*., Field-effect transistors built from all two-dimensional material components. *ACS Nano* **8**, 6259–6264 (2014). doi: 10.1021/nn501723y; pmid: 24779528
40. S. Das, R. Gulotty, A. V. Sumant, A. Roelofs, All two-dimensional, flexible, transparent, and thinnest thin film transistor. *Nano Lett.* **14**, 2861–2866 (2014). doi: 10.1021/nl5009037; pmid: 24754722
41. A. Avsar *et al*., Air-stable transport in graphene-contacted, fully encapsulated ultrathin black phosphorus-based field-effect transistors. *ACS Nano* **9**, 4138–4145 (2015). doi: 10.1021/acsnano.5b00289; pmid: 25769342
42. K. G. Zhou *et al*., Raman modes of MoS_2 used as fingerprint of van der Waals interactions in 2-D crystal-based heterostructures. *ACS Nano* **8**, 9914–9924 (2014). doi: 10.1021/nn5042703; pmid: 25198732
43. G. H. Lee *et al*., Flexible and transparent MoS_2 field-effect transistors on hexagonal boron nitride-graphene heterostructures. *ACS Nano* **7**, 7931–7936 (2013). doi: 10.1021/nn402954e; pmid: 23924287
44. C. J. Shih *et al*., Tuning on-off current ratio and field-effect mobility in a MoS_2-graphene heterostructure via Schottky barrier modulation. *ACS Nano* **8**, 5790–5798 (2014). doi: 10.1021/nn500676t; pmid: 24824139
45. C. Huang *et al*., Lateral heterojunctions within monolayer $MoSe_2$-WSe_2 semiconductors. *Nat. Mater.* **13**, 1096–1101 (2014). doi: 10.1038/nmat4064; pmid: 25150560
46. H. Wang *et al*., Two-dimensional heterostructures: Fabrication, characterization, and application. *Nanoscale* **6**, 12250–12272 (2014). doi: 10.1039/C4NR03435J; pmid: 25219598
47. L. Yu *et al*., Graphene/MoS_2 hybrid technology for large-scale two-dimensional electronics. *Nano Lett.* **14**, 3055–3063 (2014). doi: 10.1021/nl404795z; pmid: 24810658
48. X. Hong *et al*., Ultrafast charge transfer in atomically thin MoS_2/WS_2 heterostructures. *Nat. Nanotechnol.* **9**, 682–686 (2014). doi: 10.1038/nnano.2014.167; pmid: 25150718
49. J. H. Yu *et al*., Vertical heterostructure of two-dimensional MoS_2 and WSe_2 with vertically aligned layers. *Nano Lett.* **15**, 1031–1035 (2015). doi: 10.1021/nl503897h; pmid: 25590995
50. J. Knoch, J. Appenzeller, Tunneling phenomena in carbon nanotube field-effect transistors. *Phys. Status Solidi A* **205**, 679–694 (2008). doi: 10.1002/pssa.200723528
51. A. D. Franklin, Electronics: The road to carbon nanotube transistors. *Nature* **498**, 443–444 (2013). doi: 10.1038/498443a; pmid: 23803839
52. J. Jeon *et al*., Controlling grain size and continuous layer growth in two-dimensional MoS_2 films for nanoelectronic device application. *IEEE Trans. NanoTechnol.* **14**, 238–242 (2015). doi: 10.1109/TNANO.2014.2381667
53. D. Dumcenco *et al*., Large-area epitaxial monolayer MoS_2. *ACS Nano* **9**, 4611–4620 (2015). doi: 10.1021/acsnano.5b01281; pmid: 25843548
54. C.-C. Huang *et al*., Scalable high-mobility MoS_2 thin films fabricated by an atmospheric pressure chemical vapor deposition process at ambient temperature. *Nanoscale* **6**, 12792–12797 (2014). doi: 10.1039/C4NR04228J; pmid: 25226424
55. Z. Jin, S. Shin, H. Kwon, S.-J. Han, Y.-S. Min, Novel chemical route for atomic layer deposition of MoS_2 thin film on SiO_2/Si substrate. *Nanoscale* **6**, 14453–14458 (2014). doi: 10.1039/C4NR04816D; pmid: 25340905
56. A. Tarasov *et al*., Highly uniform trilayer molybdenum disulfide for wafer-scale device fabrication. *Adv. Funct. Mater.* **24**, 6389–6400 (2014). doi: 10.1002/adfm.201401389

57. H. Schmidt *et al*., Transport properties of monolayer MoS_2 grown by chemical vapor deposition. *Nano Lett.* **14**, 1909–1913 (2014). doi: 10.1021/nl4046922; pmid: 24640984
58. M. Okada *et al*., Direct chemical vapor deposition growth of WS2 atomic layers on hexagonal boron nitride. *ACS Nano* **8**, 8273–8277 (2014). doi: 10.1021/nn503093k; pmid: 25093606
59. A. S. George *et al*., wafer scale synthesis and high resolution structural characterization of atomically thin MoS_2 layers. *Adv. Funct. Mater.* **24**, 7461–7466 (2014). doi: 10.1002/adfm.201402519
60. Y. Yu *et al*., Controlled scalable synthesis of uniform, high-quality monolayer and few-layer MoS_2 films. *Sci. Rep.* **3**, 1866 (2013). doi: 10.1038/srep01866; pmid: 23689610
61. S. Park *et al*., Large-area assembly of densely aligned single-walled carbon nanotubes using solution shearing and their application to field-effect transistors. *Adv. Mater.* **27**, 2656–2662 (2015). doi: 10.1002/adma.201405289; pmid: 25788393
62. Q. Cao *et al*., Arrays of single-walled carbon nanotubes with full surface coverage for high-performance electronics. *Nat. Nanotechnol.* **8**, 180–186 (2013). doi: 10.1038/nnano.2012.257; pmid: 23353673
63. J. M. Lobez, S.-J. Han, A. Afzali, J. B. Hannon, Surface selective one-step fabrication of carbon nanotube thin films with high density. *ACS Nano* **8**, 4954–4960 (2014). doi: 10.1021/nn5009935; pmid: 24684374
64. T. A. Shastry *et al*., Large-area, electronically monodisperse, aligned single-walled carbon nanotube thin films fabricated by evaporation-driven self-assembly. *Small* **9**, 45–51 (2013). doi: 10.1002/smll.201201398; pmid: 22987547
65. S.-P. Han, H. T. Maune, R. D. Barish, M. Bockrath, W. A. Goddard III, DNA-linker-induced surface assembly of ultra dense parallel single walled carbon nanotube arrays. *Nano Lett.* **12**, 1129–1135 (2012). doi: 10.1021/nl201818u; pmid: 22320204
66. S. Shekhar, P. Stokes, S. I. Khondaker, Ultrahigh density alignment of carbon nanotube arrays by dielectrophoresis. *ACS Nano* **5**, 1739–1746 (2011). doi: 10.1021/nn102305z; pmid: 21323326
67. H. Park *et al*., High-density integration of carbon nanotubes via chemical self-assembly. *Nat. Nanotechnol.* **7**, 787–791 (2012). doi: 10.1038/nnano.2012.189; pmid: 23103933
68. G. J. Brady *et al*., Polyfluorene-sorted, carbon nanotube array field-effect transistors with increased current density and high on/off ratio. *ACS Nano* **8**, 11614–11621 (2014). doi: 10.1021/nn5048734; pmid: 25383880
69. M. Shimizu, S. Fujii, T. Tanaka, H. Kataura, Effects of surfactants on the electronic transport properties of thin-film transistors of single-wall carbon nanotubes. *J. Phys. Chem. C* **117**, 11744–11749 (2013). doi: 10.1021/jp3113254
70. V. K. Sangwan *et al*., Fundamental performance limits of carbon nanotube thin-film transistors achieved using hybrid molecular dielectrics. *ACS Nano* **6**, 7480–7488 (2012). doi: 10.1021/nn302768h; pmid: 22783918
71. S.-J. Choi *et al*., Comparative study of solution-processed carbon nanotube network transistors. *Appl. Phys. Lett.* **101**, 112104 (2012). doi: 10.1063/1.4752006
72. D. B. Farmer, R. G. Gordon, Atomic layer deposition on suspended single-walled carbon nanotubes via gas-phase noncovalent functionalization. *Nano Lett.* **6**, 699–703 (2006). doi: 10.1021/nl052453d; pmid: 16608267
73. A. D. Franklin *et al*., Carbon nanotube complementary wrap-gate transistors. *Nano Lett.* **13**, 2490–2495 (2013). doi: 10.1021/nl400544q; pmid: 23638708
74. S. Jandhyala *et al*., Atomic layer deposition of dielectrics on graphene using reversibly physisorbed ozone. *ACS Nano* **6**, 2722–2730 (2012). doi: 10.1021/nn300167t; pmid: 22352388
75. A. Azcatl *et al*., MoS_2 functionalization for ultra-thin atomic layer deposited dielectrics. *Appl. Phys. Lett.* **104**, 111601 (2014). doi: 10.1063/1.4869149
76. Z. Chen, J. Appenzeller, J. Knoch, Y. M. Lin, P. Avouris, The role of metal-nanotube contact in the performance of carbon nanotube field-effect transistors. *Nano Lett.* **5**, 1497–1502 (2005). doi: 10.1021/nl0508624; pmid: 16178264
77. Y. Chai *et al*., Low-resistance electrical contact to carbon nanotubes with graphitic interfacial layer. *IEEE Trans. Electron. Dev.* **59**, 12–19 (2012). doi: 10.1109/TED.2011.2170216
78. A. D. Franklin, D. B. Farmer, W. Haensch, Defining and overcoming the contact resistance challenge in scaled carbon nanotube transistors. *ACS Nano* **8**, 7333–7339 (2014). doi: 10.1021/nn5024363; pmid: 24999536
79. W. Liu *et al*., Role of metal contacts in designing high-performance monolayer n-type WSe2 field effect transistors. *Nano Lett.* **13**, 1983–1990 (2013). doi: 10.1021/nl304777e; pmid: 23527483
80. S. Das, H.-Y. Chen, A. V. Penumatcha, J. Appenzeller, High performance multilayer MoS_2 transistors with scandium contacts. *Nano Lett.* **13**, 100–105 (2013). doi: 10.1021/nl303583v; pmid: 23240655
81. C. D. English, G. Shine, V. E. Dorgan, K. C. Saraswat, E. Pop, Improving contact resistance in MoS_2 field effect transistors. *Device Res. Conf. Dig.* **2014**, 193–194 (2014).
82. A. Chanana, S. Mahapatra, First principles study of metal contacts to monolayer black phosphorous. *J. Appl. Phys.* **116**, 204302 (2014). doi: 10.1063/1.4901998
83. There is no longer much meaning behind this dimensional indicator for a certain technology node, as discussed in http://spectrum.ieee.org/semiconductors/devices/the-status-of-moores-law-its-complicated, where it is noted that the 14-nm node has 35-nm-long channel lengths with 8-nm-wide silicon fins.
84. E. Pop, Energy dissipation and transport in nanoscale devices. *Nano Res.* **3**, 147–169 (2010). doi: 10.1007/s12274-010-1019-z
85. H. Esmaeilzadeh, E. Blem, R. St. Amant, K. Sankaralingam, D. Burger, "Dark silicon and the end of multicore scaling," in *ISCA '11 Proceedings of the 38th Annual International Symposium on Computer Architecture*, San Jose, CA, 4 to 8 June 2011 (Association for Computing Machinery, New York, 2011), pp. 365–376.
86. J. Appenzeller, Y. Lin, J. Knoch, Z. Chen, P. Avouris, comparing carbon nanotube transistors - the ideal choice: A novel tunneling device design. *IEEE Trans. Electron. Dev.* **52**, 2568–2576 (2005). doi: 10.1109/TED.2005.859654
87. D. Jena, Tunneling transistors based on graphene and 2-D crystals. *Proc. IEEE* **101**, 1585–1602 (2013). doi: 10.1109/JPROC.2013.2253435
88. A. Javey, J. Guo, Q. Wang, M. Lundstrom, H. Dai, Ballistic carbon nanotube field-effect transistors. *Nature* **424**, 654–657 (2003). doi: 10.1038/nature01797; pmid: 12904787
89. A. D. Franklin, Z. Chen, Length scaling of carbon nanotube transistors. *Nat. Nanotechnol.* **5**, 858–862 (2010). doi: 10.1038/nnano.2010.220; pmid: 21102468
90. A. D. Franklin *et al*., Sub-10 nm carbon nanotube transistor. *Nano Lett.* **12**, 758–762 (2012). doi: 10.1021/nl203701g; pmid: 22260387
91. S. M. Sze, *Physics of Semiconductor Devices* (Wiley, Hoboken, NJ, ed. 2, 1981).
92. S. Datta, *Quantum Transport: Atom to Transistor* (Cambridge Univ. Press, New York, 2005).
93. Q. Cao *et al*., Medium-scale carbon nanotube thin-film integrated circuits on flexible plastic substrates. *Nature* **454**, 495–500 (2008). doi: 10.1038/nature07110; pmid: 18650920
94. B. Chandra, H. Park, A. Maarouf, G. J. Martyna, G. S. Tulevski, Carbon nanotube thin film transistors on flexible substrates. *Appl. Phys. Lett.* **99**, 072110 (2011). doi: 10.1063/1.3622767
95. D. Lee *et al*., High-performance thin-film transistors produced from highly separated solution-processed carbon nanotubes. *Appl. Phys. Lett.* **104**, 143508 (2014). doi: 10.1063/1.4871100
96. G. A. Salvatore *et al*., Fabrication and transfer of flexible few-layers MoS_2 thin film transistors to any arbitrary substrate. *ACS Nano* **7**, 8809–8815 (2013). doi: 10.1021/nn403248y; pmid: 23991756
97. H.-Y. Chang *et al*., High-performance, highly bendable MoS_2 transistors with high-k dielectrics for flexible low-power systems. *ACS Nano* **7**, 5446–5452 (2013). doi: 10.1021/nn401429w; pmid: 23668386
98. R. Yang, Z. Wang, P. X.-L. Feng, Electrical breakdown of multilayer MoS_2 field-effect transistors with thickness-dependent mobility. *Nanoscale* **6**, 12383–12390 (2014). doi: 10.1039/C4NR03472D; pmid: 25219778
99. N. R. Pradhan *et al*., Field-effect transistors based on few-layered α-$MoTe_2$. *ACS Nano* **8**, 5911–5920 (2014). doi: 10.1021/nn501013c; pmid: 24878323
100. J. Kumar, M. A. Kuroda, M. Z. Bellus, S.-J. Han, H.-Y. Chiu, Full-range electrical characteristics of WS_2 transistors. *Appl. Phys. Lett.* **106**, 123508 (2015). doi: 10.1063/1.4916403
101. B. Kim *et al*., High-speed, inkjet-printed carbon nanotube/zinc tin oxide hybrid complementary ring oscillators. *Nano Lett.* **14**, 3683–3687 (2014). doi: 10.1021/nl5016014; pmid: 24849313
102. M. Ha *et al*., Aerosol jet printed, low voltage, electrolyte gated carbon nanotube ring oscillators with sub-5 μs stage delays. *Nano Lett.* **13**, 954–960 (2013). doi: 10.1021/nl3038773; pmid: 23394463
103. P. Chen *et al*., Fully printed separated carbon nanotube thin film transistor circuits and its application in organic light emitting diode control. *Nano Lett.* **11**, 5301–5308 (2011). doi: 10.1021/nl202765b; pmid: 22050730
104. N. Rouhi, D. Jain, P. J. Burke, High-performance semiconducting nanotube inks: Progress and prospects. *ACS Nano* **5**, 8471–8487 (2011). doi: 10.1021/nn201828y; pmid: 21970293
105. F. Torrisi, J. N. Coleman, Electrifying inks with 2D materials. *Nat. Nanotechnol.* **9**, 738–739 (2014). doi: 10.1038/nnano.2014.218; pmid: 25286261
106. F. Torrisi *et al*., Inkjet-printed graphene electronics. *ACS Nano* **6**, 2992–3006 (2012). doi: 10.1021/nn2044609; pmid: 22449258
107. D. Son *et al*., Multifunctional wearable devices for diagnosis and therapy of movement disorders. *Nat. Nanotechnol.* **9**, 397–404 (2014). doi: 10.1038/nnano.2014.38; pmid: 24681776
108. C. D. Cress *et al*., Radiation effects in carbon nanoelectronics. *Electronics* **1**, 23–31 (2012). doi: 10.3390/electronics1010023
109. O. Ochedowski *et al*., Radiation hardness of graphene and MoS_2 field effect devices against swift heavy ion irradiation. *J. Appl. Phys.* **113**, 214306 (2013). doi: 10.1063/1.4808460
110. IDTechEx, "End user needs and case studies aired at IDTechEx's Printed Electronics Europe," *Print. Electron. News*, press release (28 March 2011).
111. M. Wilson, "Researchers develop transparent memory, see-through electronics next," (2008); http://gizmodo.com/5111411/researchers-develop-transparent-memory-see-through-electronics-next.

10.1126/science.aab2750

Nanomaterials in transistors: From high-performance to thin-film applications

Aaron D. Franklin

Science **349** (6249), aab2750.
DOI: 10.1126/science.aab2750

Improving transistors with nanomaterials

High-performance silicon transistors and thin-film transistors used in display technologies are fundamentally limited to miniaturization. Incorporating nanomaterials—such as carbon nanotubes, graphene, and related two-dimensional materials like molybdenum disulfide—into these devices as gate materials may circumvent some of these limitations. Franklin reviews the opportunities and challenges for incorporating nanomaterials into transistors to improve performance. Because high-performance transistors are distinct from thin-film transistors, incorporating them into flexible or transparent platforms raises new challenges.

Science, this issue 10.1126/science.aab2750