Revisão de TTL

Jun Okamoto Jr.

Níveis de tensão em TTL

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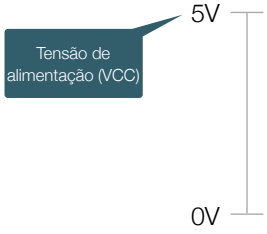

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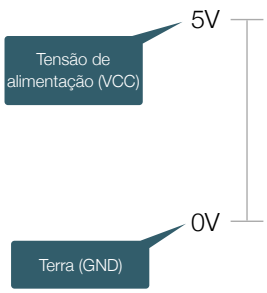

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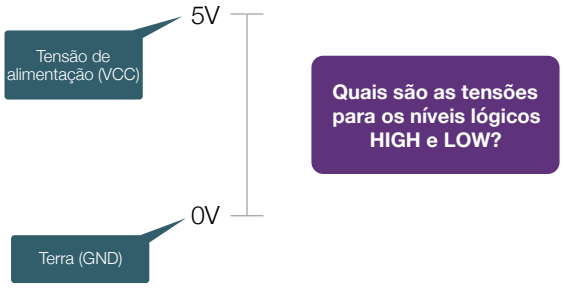

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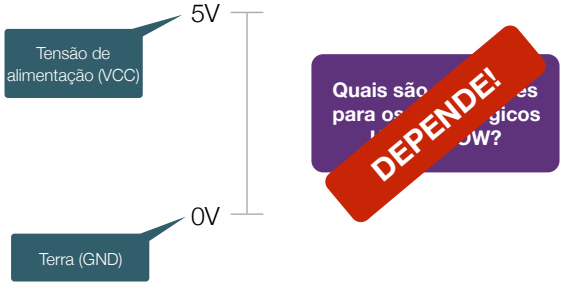

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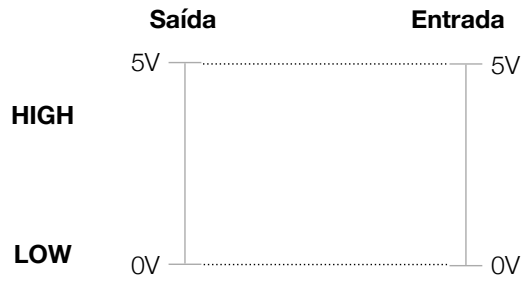

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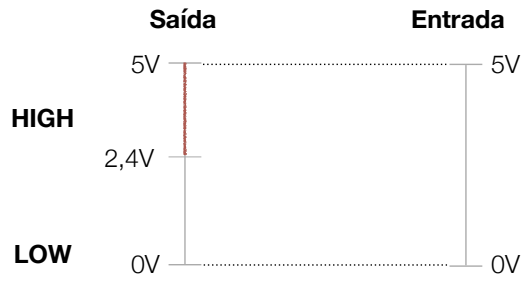

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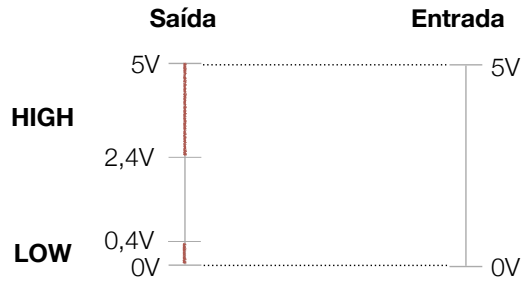

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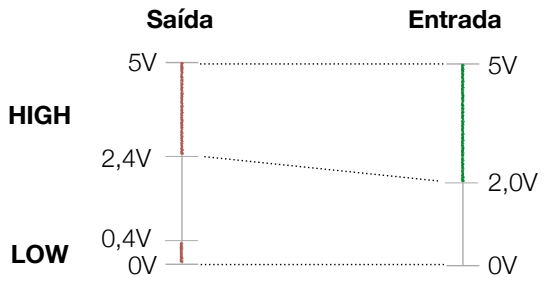

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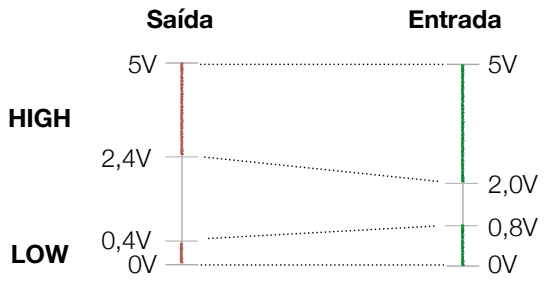
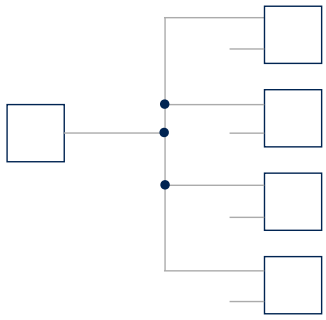


Correntes em TTL

Qual é a direção da corrente numa saída TTL?
E numa entrada TTL?

Correntes em TTL

Correntes em TTL



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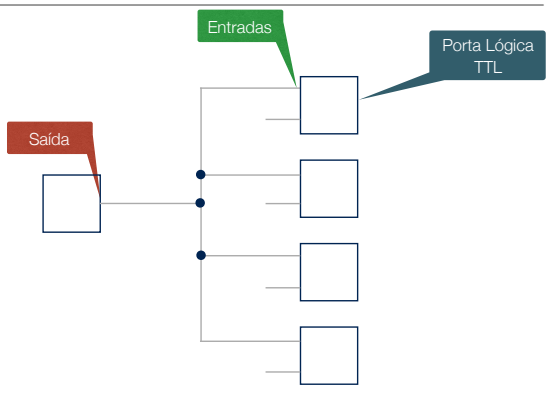

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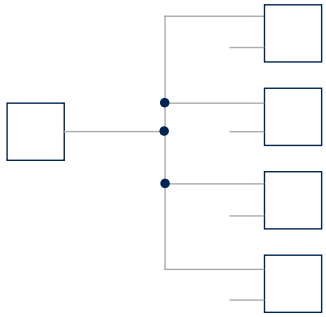

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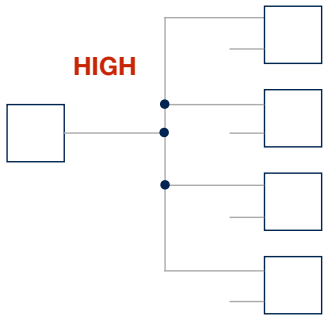

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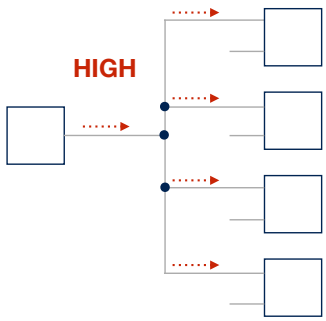

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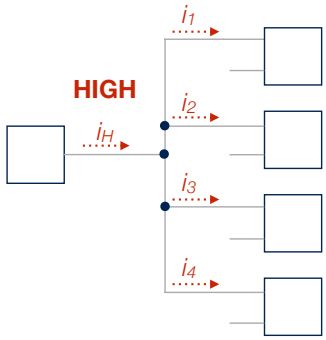

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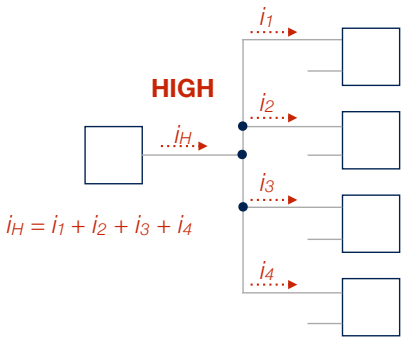

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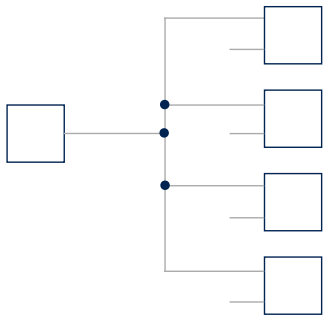

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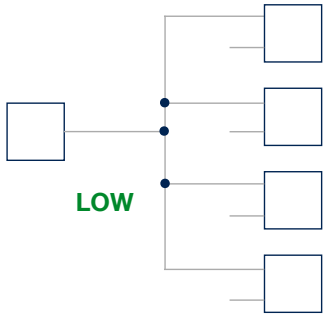

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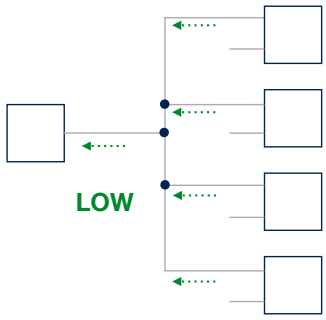

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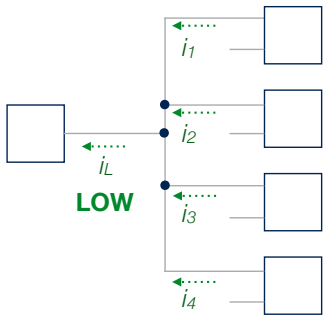

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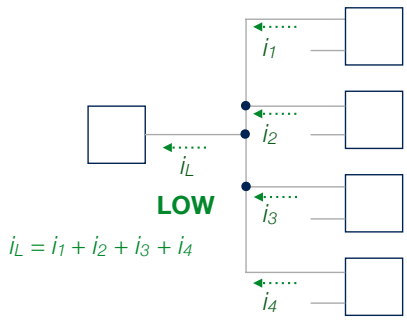

Correntes x Tecnologia

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- A tecnologia de fabricação determina a corrente e a velocidade e as tensões variam um pouco

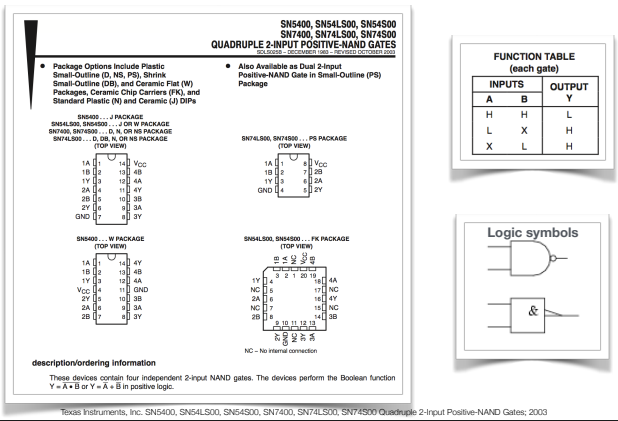
Correntes x Tecnologia

- A tecnologia de fabricação determina a corrente e a velocidade e as tensões variam um pouco
- Código do componente

SN74xx00A

- Versão
- Função lógica
- Tecnologia de fabricação
- Família
- Fabricante

Exemplo de TTL



SN5400, SN54LS00, SN54S00
SN7400, SN74LS00, SN74S00
QUADRUPLE 2-INPUT POSITIVE-NAND GATES

SDLS029 – DECEMBER 1983 – REVISED OCTOBER 2003

- Package Options Include Plastic Small-Outline (D, NS, PS), Shrink Small-Outline (DB), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) DIPs
- Also Available as Dual 2-Input Positive-NAND Gate in Small-Outline (PS) Package

SN5400 . . . J PACKAGE
SN54LS00, SN54S00 . . . J OR W PACKAGE
SN7400, SN74S00 . . . D, N, OR NS PACKAGE
SN74LS00 . . . D, DB, N, OR NS PACKAGE
(TOP VIEW)

1A	1	14	V_{CC}
1B	2	13	4B
1Y	3	12	4A
2A	4	11	4Y
2B	5	10	3B
2Y	6	9	3A
GND	7	8	3Y

SN74LS00, SN74S00 . . . PS PACKAGE
(TOP VIEW)

1A	1	8	V_{CC}
1B	2	7	2B
1Y	3	6	2A
GND	4	5	2Y

SN5400 . . . W PACKAGE
(TOP VIEW)

1A	1	14	4Y
1B	2	13	4B
1Y	3	12	4A
V_{CC}	4	11	GND
2Y	5	10	3B
2A	6	9	3A
2B	7	8	3Y

SN54LS00, SN54S00 . . . FK PACKAGE
(TOP VIEW)

1Y	4	18	4A
NC	5	17	NC
2A	6	16	4Y
NC	7	15	NC
2B	8	14	3B

NC – No internal connection

description/ordering information

These devices contain four independent 2-input NAND gates. The devices perform the Boolean function $Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

FUNCTION TABLE
(each gate)

INPUTS A	INPUTS B	OUTPUT Y
H	H	L
L	X	H
X	L	H

Logic symbols

Texas Instruments, Inc. SN5400, SN54LS00, SN54S00, SN7400, SN74LS00, SN74S00 Quadruple 2-Input Positive-NAND Gates; 2003

Tecnologia Standard

		SN5400			SN7400			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			–0.4			–0.4	mA
I_{OL}	Low-level output current			16			16	mA
T_A	Operating free-air temperature	–55		125	0		70	°C

Texas Instruments, Inc. SN5400, SN54LS00, SN54S00, SN7400, SN74LS00, SN74S00 Quadruple 2-Input Positive-NAND Gates; 2003

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Notação: I_{OH} - Corrente de saída para nível lógico High

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Tecnologia Standard

PARAMETER	TEST CONDITIONS‡			SN5400			SN7400			UNIT
				MIN	TYP§	MAX	MIN	TYP§	MAX	
V_{IK}	V_{CC} = MIN,	I_I = −12 mA				−1.5			−1.5	V
V_{OH}	V_{CC} = MIN,	V_{IL} = 0.8 V,	I_{OH} = −0.4 mA	2.4	3.4		2.4	3.4		V
V_{OL}	V_{CC} = MIN,	V_{IH} = 2 V,	I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I_I	V_{CC} = MAX,	V_I = 5.5 V				1			1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.4 V				40			40	µA
I_{IL}	V_{CC} = MAX,	V_I = 0.4 V				−1.6			−1.6	mA
I_{OS}¶	V_{CC} = MAX			−20		−55	−18		−55	mA
I_{CCH}	V_{CC} = MAX,	V_I = 0 V			4	8		4	8	mA
I_{CCL}	V_{CC} = MAX,	V_I = 4.5 V			12	22		12	22	mA

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				MIN	TYP§	MAX	MIN	TYP§	MAX	
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V_{OH}	V_{CC} = MIN,	V_{IL} = 0.8 V,	I_{OH} = −0.4 mA	2.4	3.4		2.4	3.4		V
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I_I	V_{CC} = MAX,	V_I = 5.5 V				1			1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.4 V				40			40	µA
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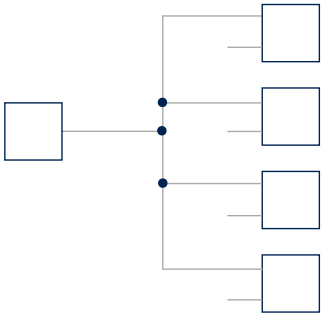
Fan-out

Saída
I_{OH} = 0,4 mA (saindo)
I_{OL} = 16 mA (entrando)

Entrada
I_{IH} = 40 µA (entrando)
I_{IL} = 1,6 mA (saindo)



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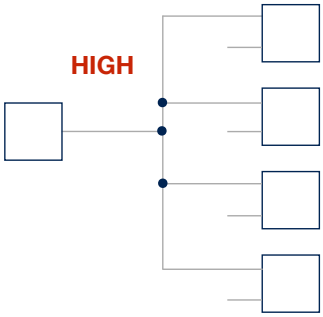

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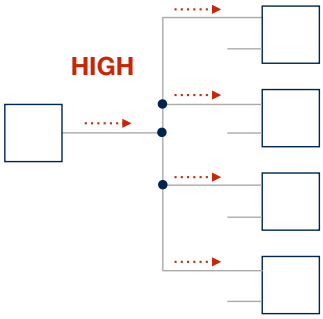

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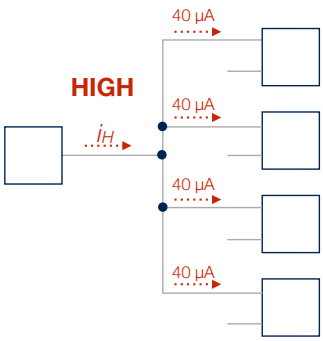

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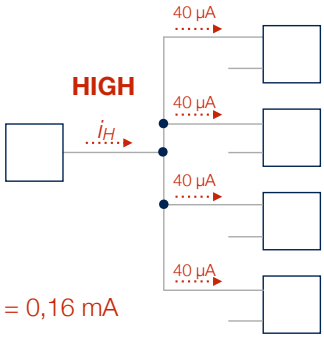

$i_H = 4 \times 40\ \mu A = 160\ \mu A = 0{,}16\ mA$

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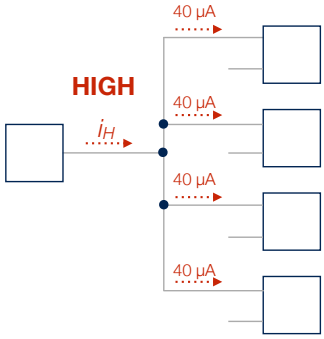

$i_H^{MAX} = n \times I_{IH} \leq I_{OH}$

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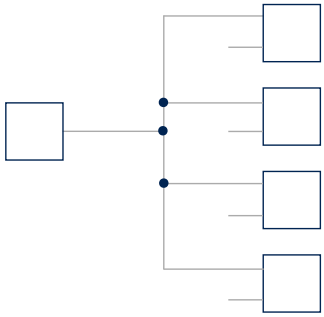

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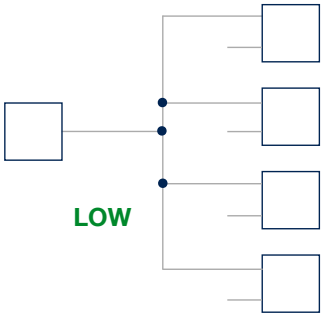

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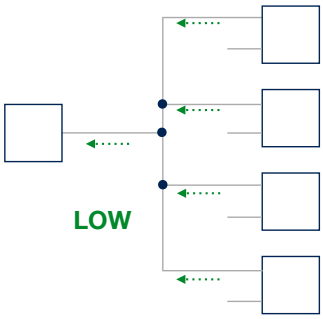

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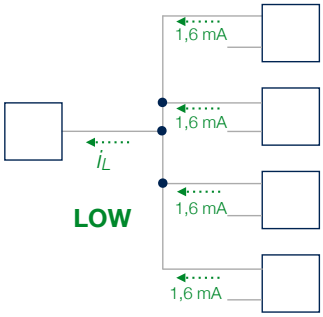

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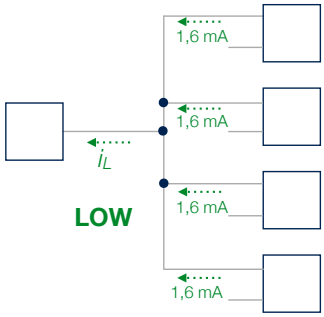

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$i_L = 4 \times 1{,}6\ mA = 6{,}4\ mA$

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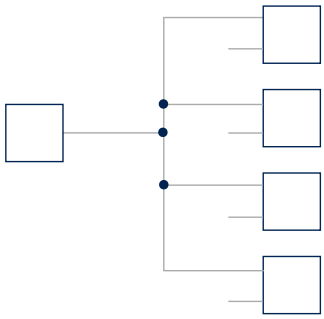
I_{IH} = 40 µA (entrando)
I_{IL} = 1,6 mA (saindo)



$i_H^{MAX} = n \times I_{IH} \leq I_{OH}$

$i_L^{MAX} = n \times I_{IL} \leq I_{OL}$

Tecnologia LS

- Low Power Schotky

		SN54LS00			SN74LS00			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

Texas Instruments, Inc. SN5400, SN54LS00, SN54S00, SN7400, SN74LS00, SN74S00 Quadruple 2-Input Positive-NAND Gates; 2003

Tecnologia LS

- Low Power Schotky

		SN54LS00			SN74LS00			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

Tecnologia LS

PARAMETER	TEST CONDITIONS†			SN54LS00			SN74LS00			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN,	I_I = −18 mA				−1.5			−1.5	V
V_{OH}	V_{CC} = MIN,	V_{IL} = MAX,	I_{OH} = −0.4 mA	2.5	3.4		2.7	3.4		V
V_{OL}	V_{CC} = MIN,	V_{IH} = 2 V	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 8mA					0.35	0.5	
I_I	V_{CC} = MAX,	V_I = 7 V				0.1			0.1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.7V				20			20	µA
I_{IL}	V_{CC} = MAX,	V_I = 0.4 V				−0.4			−0.4	mA
I_{OS}§	V_{CC} = MAX			−20		−100	−20		−100	mA
I_{CCH}	V_{CC} = MAX,	V_I = 0 V			0.8	1.6		0.8	1.6	mA
I_{CCL}	V_{CC} = MAX,	V_I = 4.5 V			2.4	4.4		2.4	4.4	mA

Texas Instruments, Inc. SN5400, SN54LS00, SN54S00, SN7400, SN74LS00, SN74S00 Quadruple 2-Input Positive-NAND Gates; 2003

Tecnologia LS

PARAMETER	TEST CONDITIONS†			SN54LS00			SN74LS00			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN,	I_I = −18 mA				−1.5			−1.5	V
V_{OH}	V_{CC} = MIN,	V_{IL} = MAX,	I_{OH} = −0.4 mA	2.5	3.4		2.7	3.4		V
V_{OL}	V_{CC} = MIN,	V_{IH} = 2 V	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 8mA					0.35	0.5	
I_I	V_{CC} = MAX,	V_I = 7 V				0.1			0.1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.7V				20			20	µA
I_{IL}	V_{CC} = MAX,	V_I = 0.4 V				−0.4			−0.4	mA
I_{OS}§	V_{CC} = MAX			−20		−100	−20		−100	mA
I_{CCH}	V_{CC} = MAX,	V_I = 0 V			0.8	1.6		0.8	1.6	mA
I_{CCL}	V_{CC} = MAX,	V_I = 4.5 V			2.4	4.4		2.4	4.4	mA

Texas Instruments, Inc. SN5400, SN54LS00, SN54S00, SN7400, SN74LS00, SN74S00 Quadruple 2-Input Positive-NAND Gates; 2003

Tecnologia S

- High Speed Schotky

		SN54S00			SN74S00			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−1			−1	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

Tecnologia S

- High Speed Schotky

		SN54S00			SN74S00			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−1			−1	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

Texas Instruments, Inc. SN5400, SN54LS00, SN54S00, SN7400, SN74LS00, SN74S00 Quadruple 2-Input Positive-NAND Gates; 2003

Tecnologia S

PARAMETER	TEST CONDITIONS†			SN54S00			SN74S00			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN,	I_I = −18 mA				−1.2			−1.2	V
V_{OH}	V_{CC} = MIN,	V_{IL} = 0.8 V,	I_{OH} = −1 mA	2.5	3.4		2.7	3.4		V
V_{OL}	V_{CC} = MIN,	V_{IH} = 2 V,	I_{OL} = 20 mA			0.5			0.5	V
I_I	V_{CC} = MAX,	V_I = 5.5 V				1			1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.7 V				50			50	µA
I_{IL}	V_{CC} = MAX,	V_I = 0.5V				−2			−2	mA
I_{OS}§	V_{CC} = MAX			−40		−100	−40		−100	mA
I_{CCH}	V_{CC} = MAX,	V_I = 0 V			10	16		10	16	mA
I_{CCL}	V_{CC} = MAX,	V_I = 4.5 V			20	36		20	36	mA

Texas Instruments, Inc. SN5400, SN54LS00, SN54S00, SN7400, SN74LS00, SN74S00 Quadruple 2-Input Positive-NAND Gates; 2003

Tecnologia S

PARAMETER	TEST CONDITIONS†			SN54S00			SN74S00			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN,	I_I = −18 mA				−1.2			−1.2	V
V_{OH}	V_{CC} = MIN,	V_{IL} = 0.8 V,	I_{OH} = −1 mA	2.5	3.4		2.7	3.4		V
V_{OL}	V_{CC} = MIN,	V_{IH} = 2 V,	I_{OL} = 20 mA			0.5			0.5	V
I_I	V_{CC} = MAX,	V_I = 5.5 V				1			1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.7 V				50			50	µA
I_{IL}	V_{CC} = MAX,	V_I = 0.5V				−2			−2	mA
I_{OS}§	V_{CC} = MAX			−40		−100	−40		−100	mA
I_{CCH}	V_{CC} = MAX,	V_I = 0 V			10	16		10	16	mA
I_{CCL}	V_{CC} = MAX,	V_I = 4.5 V			20	36		20	36	mA

Texas Instruments, Inc. SN5400, SN54LS00, SN54S00, SN7400, SN74LS00, SN74S00 Quadruple 2-Input Positive-NAND Gates; 2003

Exercício sobre Fan-out

TTL Standard	TTL LS	TTL S
Saída I_{OH} = 0,4 mA (saindo) I_{OL} = 16 mA (entrando)	**Saída** I_{OH} = 0,4 mA (saindo) I_{OL} = 8 mA (entrando)	**Saída** I_{OH} = 1 mA (saindo) I_{OL} = 20 mA (entrando)
Entrada I_{IH} = 40 µA (entrando) I_{IL} = 1,6 mA (saindo)	**Entrada** I_{IH} = 20 µA (entrando) I_{IL} = 0,4 mA (saindo)	**Entrada** I_{IH} = 50 µA (entrando) I_{IL} = 2 mA (saindo)

Out\In	STD	LS	S
STD	10(H)/10(L)		
LS			
S			

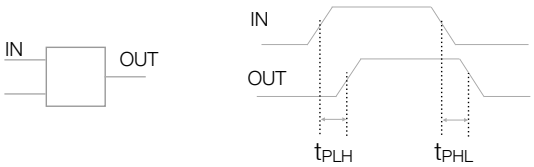
Exercício sobre Fan-out

TTL Standard	TTL LS	TTL S
Saída I_{OH} = 0,4 mA (saindo) I_{OL} = 16 mA (entrando)	**Saída** I_{OH} = 0,4 mA (saindo) I_{OL} = 8 mA (entrando)	**Saída** I_{OH} = 1 mA (saindo) I_{OL} = 20 mA (entrando)
Entrada I_{IH} = 40 µA (entrando) I_{IL} = 1,6 mA (saindo)	**Entrada** I_{IH} = 20 µA (entrando) I_{IL} = 0,4 mA (saindo)	**Entrada** I_{IH} = 50 µA (entrando) I_{IL} = 2 mA (saindo)

Out\In	STD	LS	S
STD	10(H)/10(L)	20(H)/40(L)	8(H)/8(L)
LS	10(H)/5(L)	20(H)/20(L)	8(H)/4(L)
S	25(H)/12,5(L)	50(H)/50(L)	20(H)/10(L)

Velocidade de chaveamento

- Tempo de propagação entre um determinado nível da entrada para a saída mudar de LOW para HIGH (T_{PLH}) ou de HIGH para LOW (T_{PHL})



Velocidade de chaveamento

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN5400 SN7400 MIN	SN5400 SN7400 TYP	SN5400 SN7400 MAX	UNIT
t_{PLH}	A or B	Y	R_L = 400 Ω, C_L = 15 pF		11	22	ns
t_{PHL}					7	15	

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54LS00 SN74LS00 MIN	SN54LS00 SN74LS00 TYP	SN54LS00 SN74LS00 MAX	UNIT
t_{PLH}	A or B	Y	R_L = 2 kΩ, C_L = 15 pF		9	15	ns
t_{PHL}					10	15	

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54S00 SN74S00 MIN	SN54S00 SN74S00 TYP	SN54S00 SN74S00 MAX	UNIT
t_{PLH}	A or B	Y	R_L = 280 Ω, C_L = 15 pF		3	4.5	ns
t_{PHL}					3	5	
t_{PLH}	A or B	Y	R_L = 280 Ω, C_L = 50 pF		4.5		ns
t_{PHL}					5		

Velocidade de chaveamento

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN5400 SN7400 MIN	SN5400 SN7400 TYP	SN5400 SN7400 MAX	UNIT
t_{PLH}	A or B	Y	R_L = 400 Ω, C_L = 15 pF		11	22	ns
t_{PHL}					7	15	

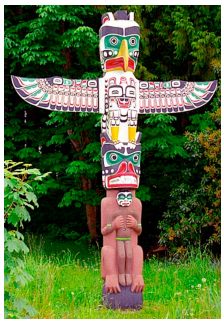
PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54LS00 SN74LS00 MIN	SN54LS00 SN74LS00 TYP	SN54LS00 SN74LS00 MAX	UNIT
t_{PLH}	A or B	Y	R_L = 2 kΩ, C_L = 15 pF		9	15	ns
t_{PHL}					10	15	

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54S00 SN74S00 MIN	SN54S00 SN74S00 TYP	SN54S00 SN74S00 MAX	UNIT
t_{PLH}	A or B	Y	R_L = 280 Ω, C_L = 15 pF		3	4.5	ns
t_{PHL}					3	5	
t_{PLH}	A or B	Y	R_L = 280 Ω, C_L = 50 pF		4.5		ns
t_{PHL}					5		

Tipos de saída de TTL

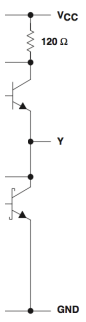
- Totem-pole
- Open-collector
- Tri-state

Totem-pole



Totem-pole

<=>

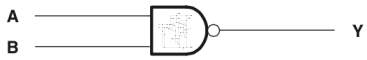


http://www.vivaboo.com/history-stands-tall-thanks-to-the-stanley-park-totem-poles/

Exemplo: Porta NAND (74LS00)

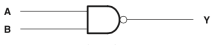
1/4 74LS00

Exemplo: Porta NAND (74LS00)

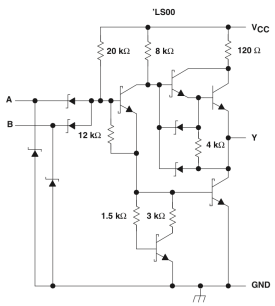


1/4 74LS00

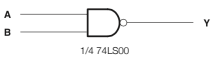
Exemplo: Porta NAND (74LS00)

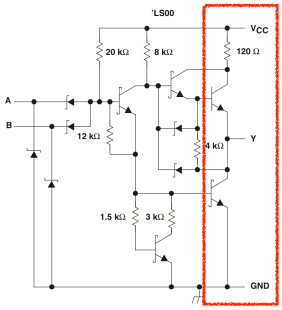


1/4 74LS00



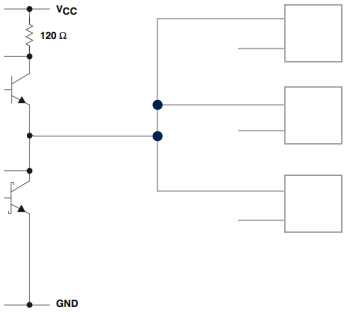
Exemplo: Porta NAND (74LS00)





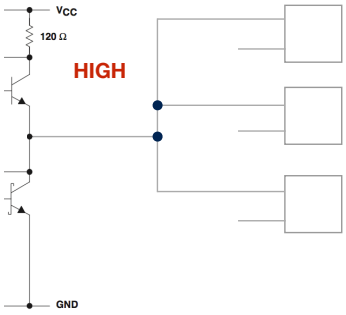
1/4 SN74LS00
(só estágio de saída)

Totem-pole



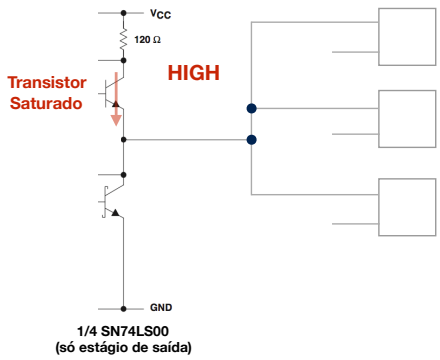
1/4 SN74LS00
(só estágio de saída)

Totem-pole



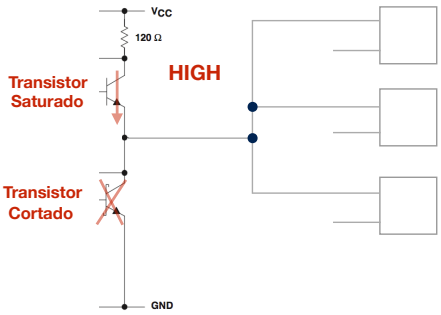
1/4 SN74LS00
(só estágio de saída)

Totem-pole



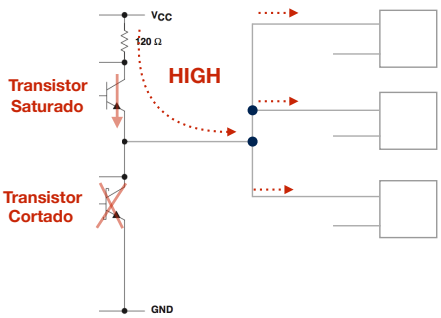
1/4 SN74LS00
(só estágio de saída)

Totem-pole



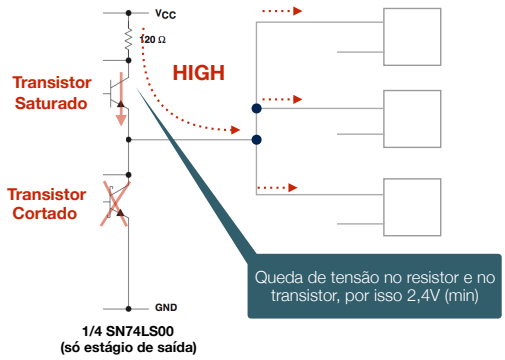
1/4 SN74LS00
(só estágio de saída)

Totem-pole



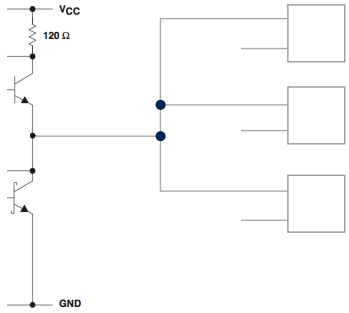
1/4 SN74LS00
(só estágio de saída)

Totem-pole



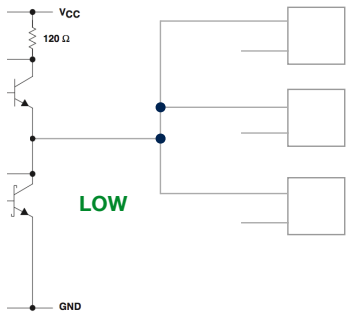
1/4 SN74LS00
(só estágio de saída)

Totem-pole



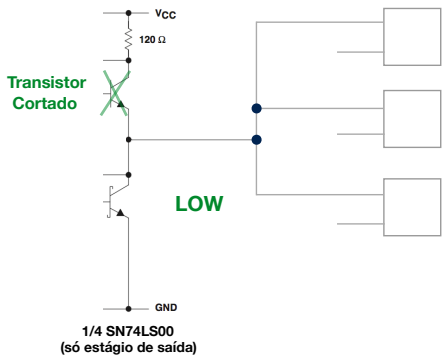
1/4 SN74LS00
(só estágio de saída)

Totem-pole



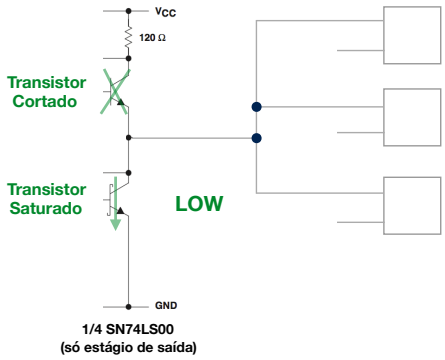
1/4 SN74LS00
(só estágio de saída)

Totem-pole



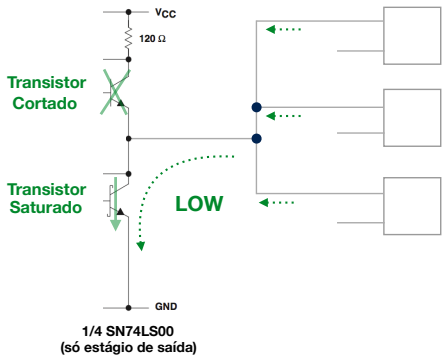
1/4 SN74LS00
(só estágio de saída)

Totem-pole



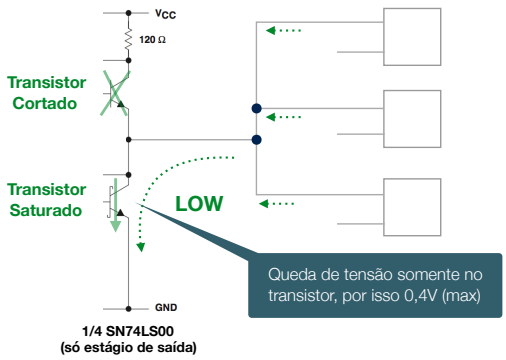
1/4 SN74LS00
(só estágio de saída)

Totem-pole

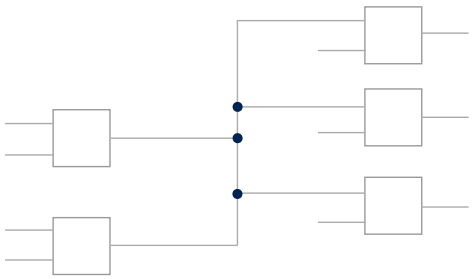


1/4 SN74LS00
(só estágio de saída)

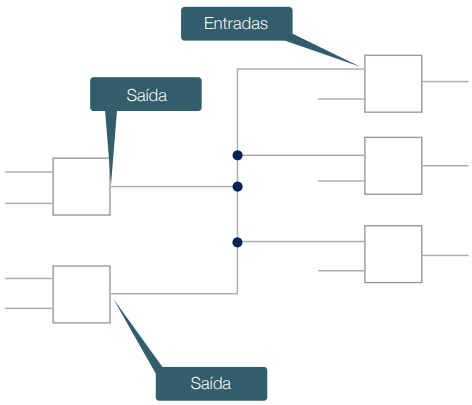
Totem-pole



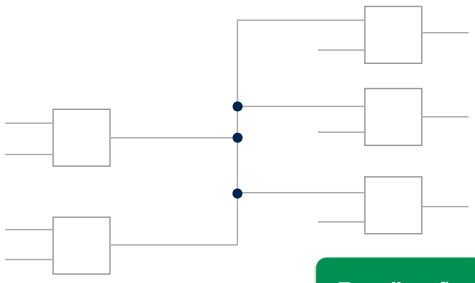
Totem-pole



Totem-pole



Totem-pole

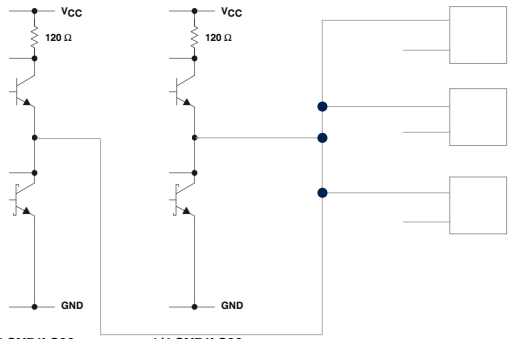


Essa ligação está OK?

Totem-pole

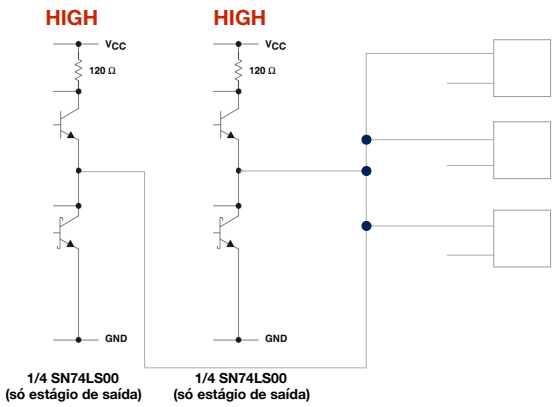
Essa ligação está OK?

Totem-pole

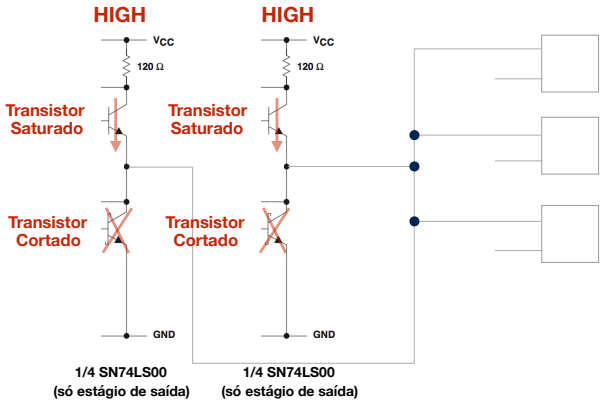


1/4 SN74LS00 (só estágio de saída) **1/4 SN74LS00 (só estágio de saída)**

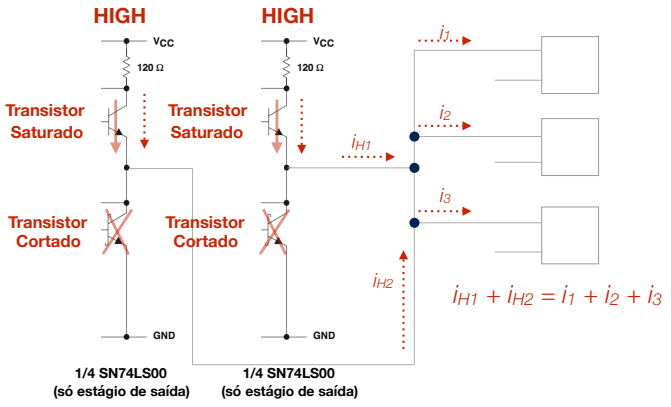
Totem-pole



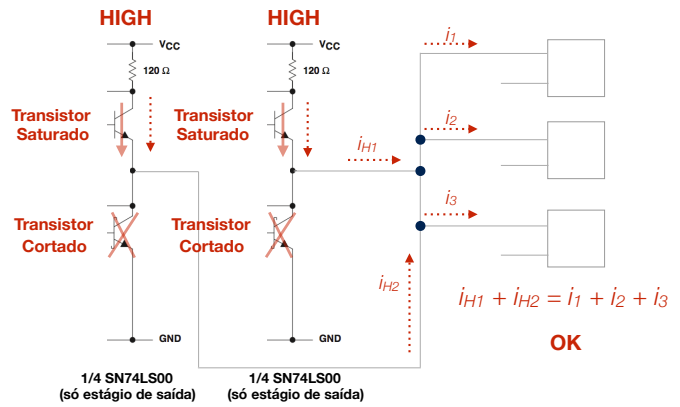
Totem-pole



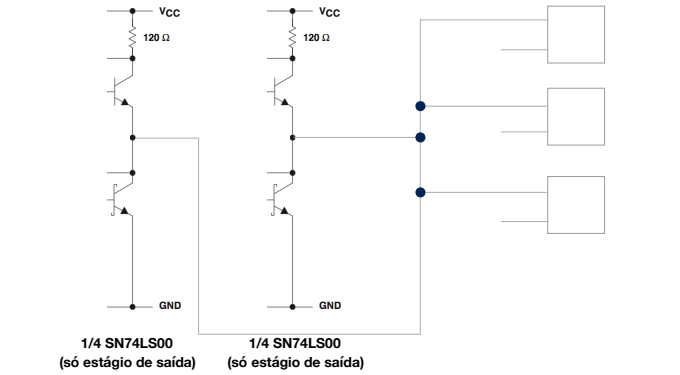
Totem-pole



Totem-pole



Totem-pole



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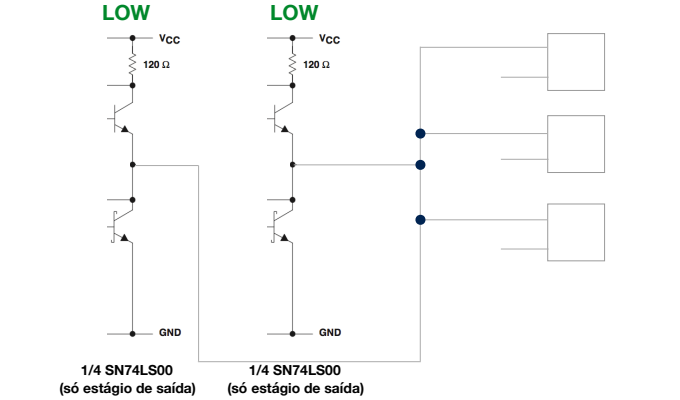

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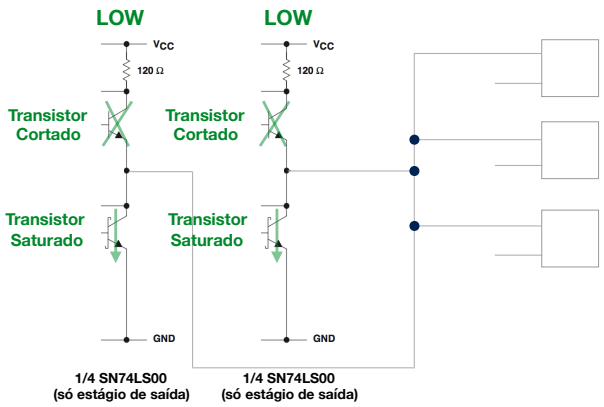

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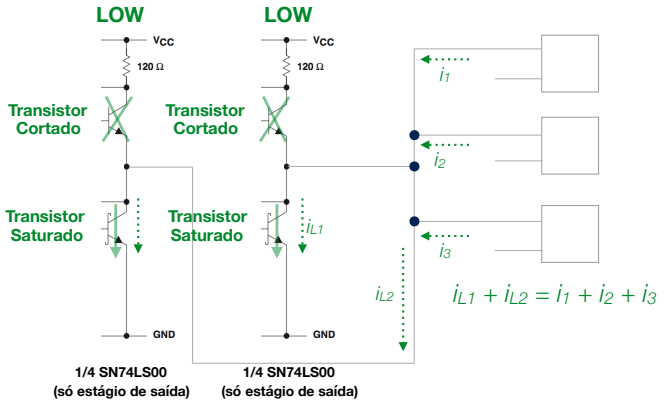
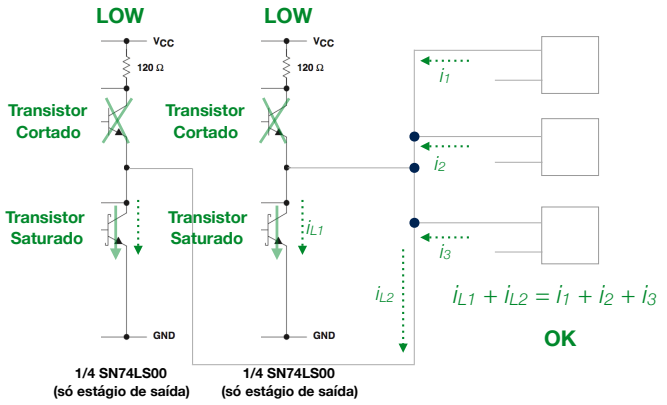
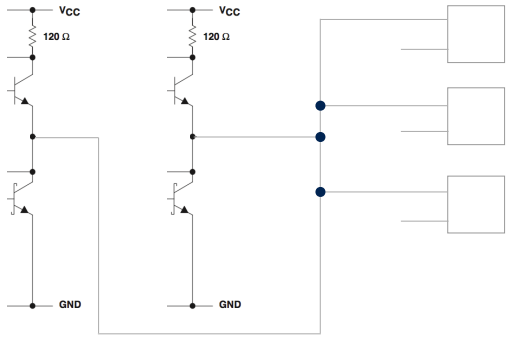


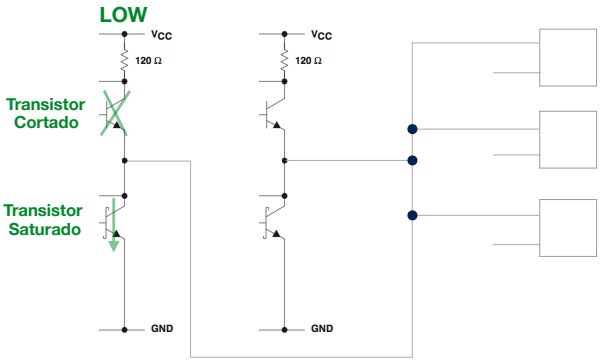
Totem-pole



Totem-pole



Totem-pole



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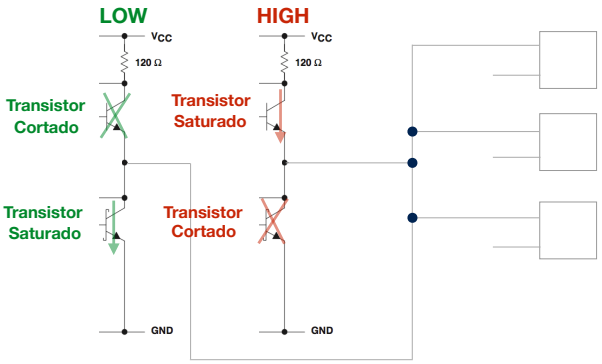
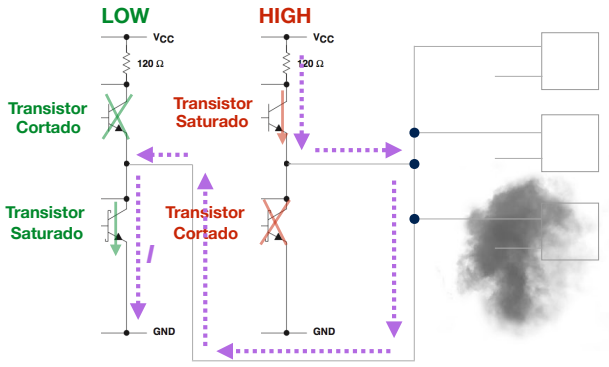
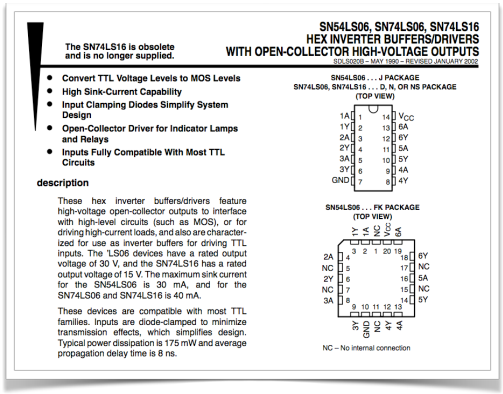


Totem-pole



Open-collector



The SN74LS16 is obsolete and is no longer supplied.

SN54LS06, SN74LS06, SN74LS16
HEX INVERTER BUFFERS/DRIVERS
WITH OPEN-COLLECTOR HIGH-VOLTAGE OUTPUTS

SDLS020B – MAY 1980 – REVISED JANUARY 2002

- Convert TTL Voltage Levels to MOS Levels
- High Sink-Current Capability
- Input Clamping Diodes Simplify System Design
- Open-Collector Driver for Indicator Lamps and Relays
- Inputs Fully Compatible With Most TTL Circuits

description

These hex inverter buffers/drivers feature high-voltage open-collector outputs to interface with high-level circuits (such as MOS), or for driving high-current loads, and also are characterized for use as inverter buffers for driving TTL inputs. The 'LS06 devices have a rated output voltage of 30 V, and the SN74LS16 has a rated output voltage of 15 V. The maximum sink current for the SN54LS06 is 30 mA, and for the SN74LS06 and SN74LS16 is 40 mA.

These devices are compatible with most TTL families. Inputs are diode-clamped to minimize transmission effects, which simplifies design. Typical power dissipation is 175 mW and average propagation delay time is 8 ns.

SN54LS06 . . . J PACKAGE
SN74LS06, SN74LS16 . . . D, N, OR NS PACKAGE
(TOP VIEW)

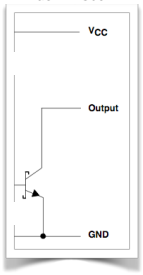
1A	1	14	VCC
1Y	2	13	6A
2A	3	12	6Y
2Y	4	11	5A
3A	5	10	5Y
3Y	6	9	4A
GND	7	8	4Y

SN54LS06 . . . FK PACKAGE
(TOP VIEW)

2A	4	18	6Y
NC	5	17	NC
2Y	6	16	5A
NC	7	15	NC
3A	8	14	5Y

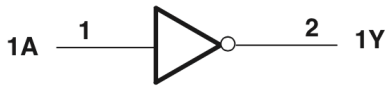
NC – No internal connection

Estágio de saída do 74LS06



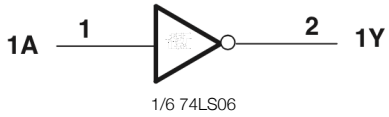
Texas Instruments, Inc. SN54LS06, SN74LS06, SN74LS16 Hex Inverter Buffer/Drivers with Open-collector High-Voltage Outputs; 2003

Exemplo: Inversora de alta tensão (74LS06)



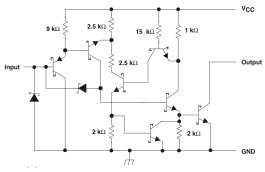
1/6 74LS06

Exemplo: Inversora de alta tensão (74LS06)

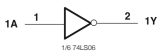


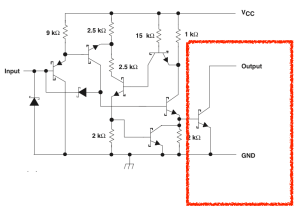
1/6 74LS06

Exemplo: Inversora de alta tensão (74LS06)



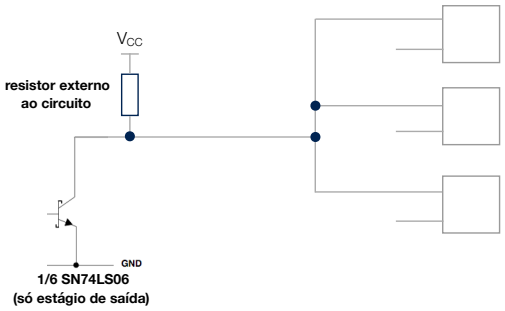
Exemplo: Inversora de alta tensão (74LS06)



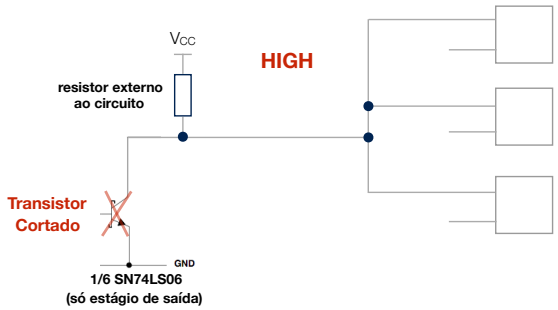


1/6 SN74LS06
(só estágio de saída)

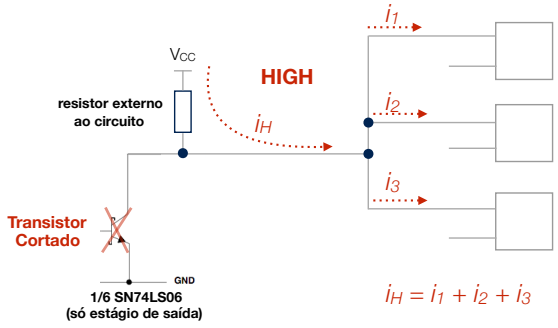
Open-collector



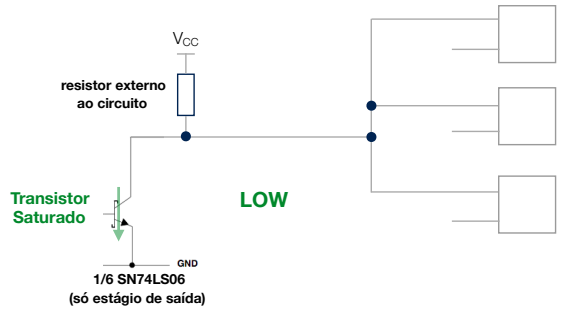
Open-collector



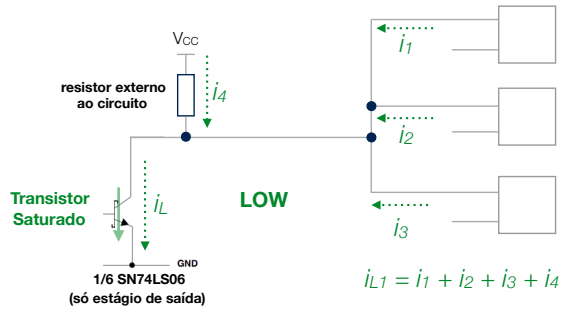
Open-collector



Open-collector



Open-collector



Open-collector

			SN54LS06			SN74LS06 SN74LS16			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_{OH}	High-level output voltage	'LS06			30			30	V
		SN74LS16						15	V
I_{OL}	Low-level output current				30			40	mA
T_A	Operating free-air temperature		−55		125	0		70	°C

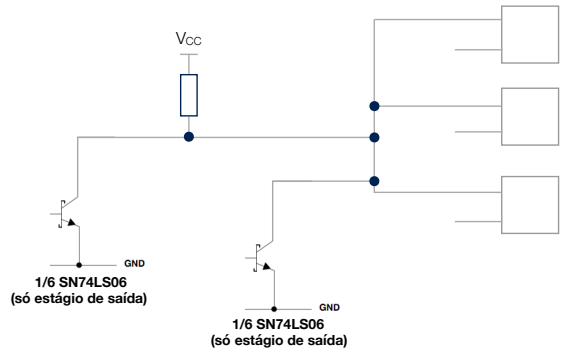
Texas Instruments, Inc. SN54LS06, SN74LS06, SN74LS16 Hex Inverter Buffer/Drivers with Open-collector High-Voltage Outputs; 2003

Open-collector

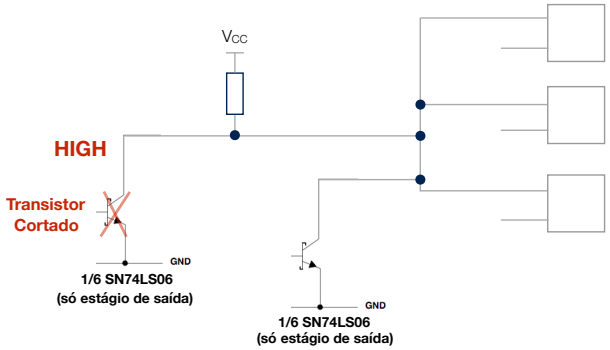
			SN54LS06			SN74LS06 SN74LS16			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_{OH}	High-level output voltage	'LS06			30			30	V
		SN74LS16						15	V
I_{OL}	Low-level output current				30			40	mA
T_A	Operating free-air temperature		−55		125	0		70	°C

Texas Instruments, Inc. SN54LS06, SN74LS06, SN74LS16 Hex Inverter Buffer/Drivers with Open-collector High-Voltage Outputs; 2003

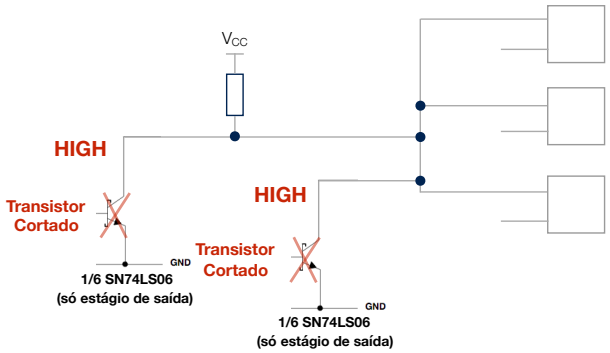
Open-collector



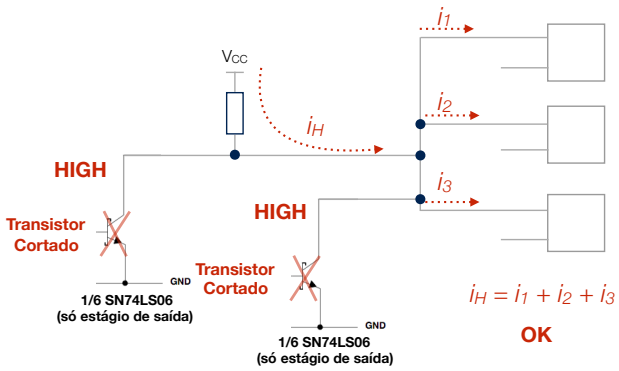
Open-collector



Open-collector



Open-collector



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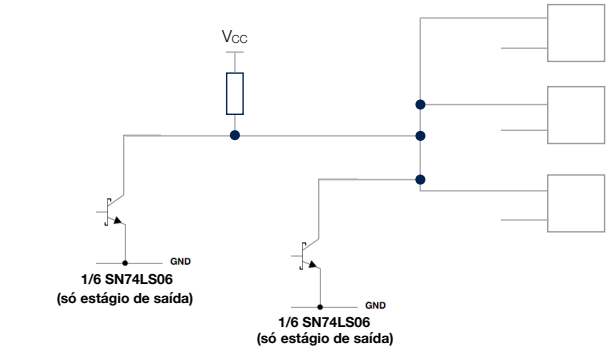

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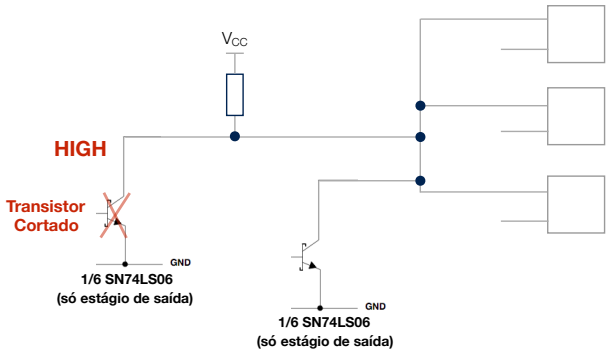

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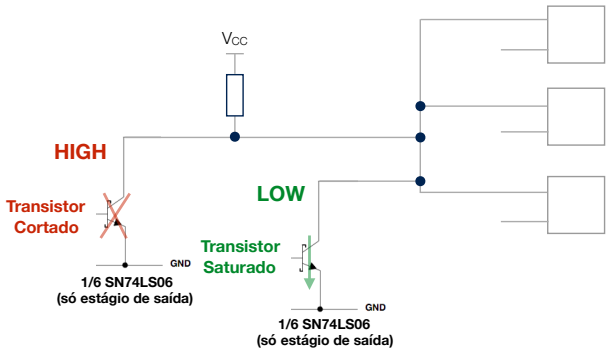

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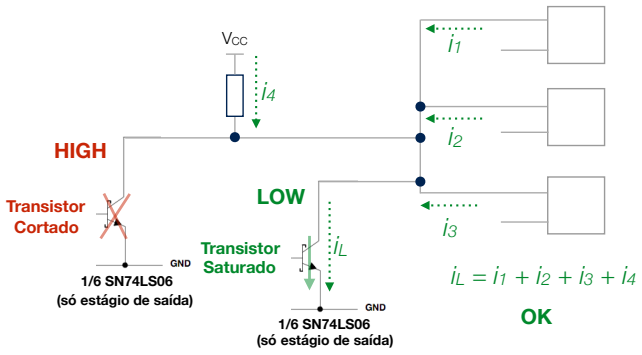

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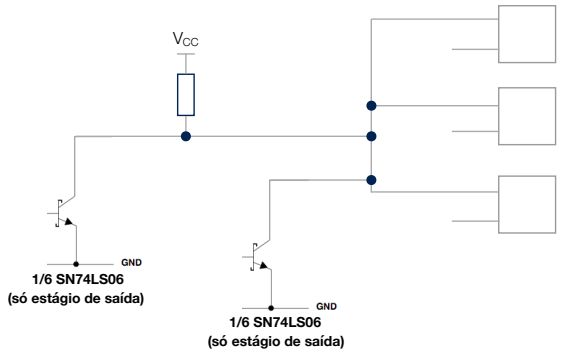

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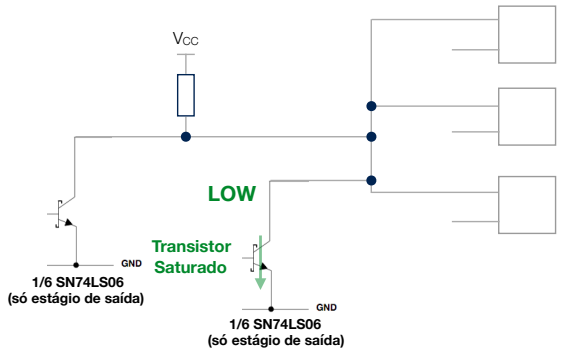

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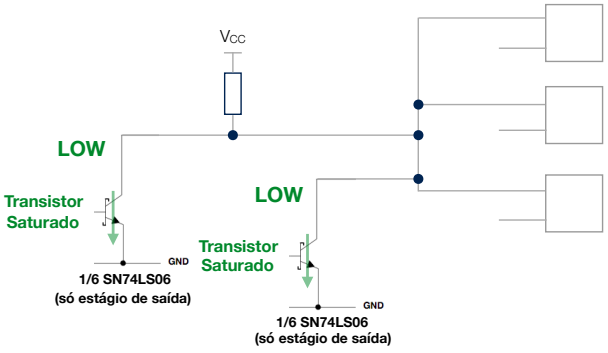
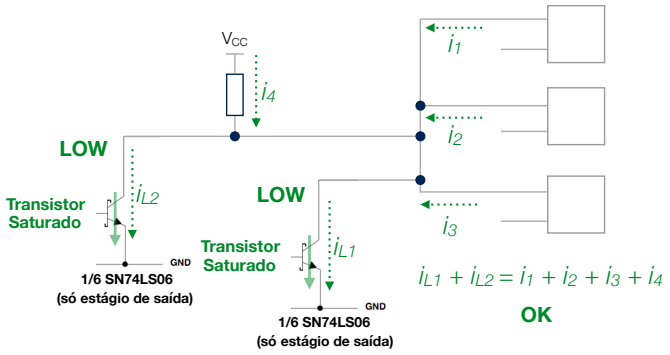


Open-collector



Open-collector

Saída Y1	Saída Y2	Entradas
HIGH	HIGH	HIGH
HIGH	LOW	LOW
LOW	HIGH	LOW
LOW	LOW	LOW

Open-collector

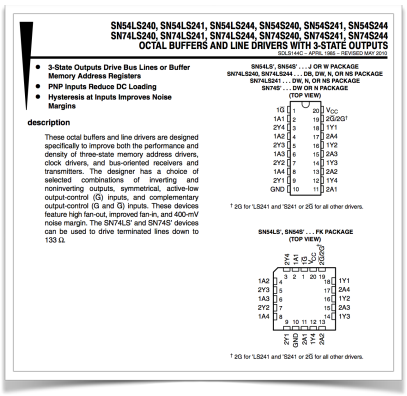
Saída Y1	Saída Y2	Entradas
1	1	1
1	0	0
0	1	0
0	0	0

Open-collector

Saída Y1	Saída Y2	Entradas
1	1	1
1	0	0
0	1	0
0	0	0

Wired AND

Tri-state

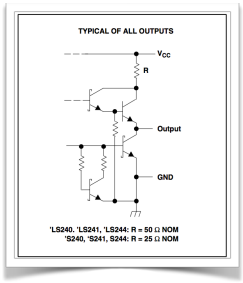


SN54LS240, SN54LS241, SN54LS244, SN54S240, SN54S241, SN54S244
SN74LS240, SN74LS241, SN74LS244, SN74S240, SN74S241, SN74S244
OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- PNP Inputs Reduce DC Loading
- Hysteresis at Inputs Improves Noise Margins

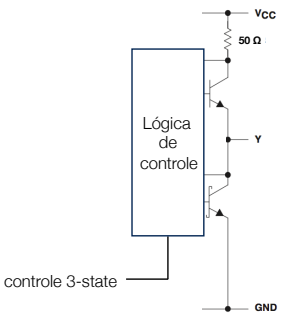
description

These octal buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The designer has a choice of selected combinations of inverting and noninverting outputs, symmetrical, active-low output-control (G) inputs, and complementary output-control (G and G) inputs. These devices feature high fan-out, improved fan-in, and 400-mV noise margin. The SN74LS' and SN74S' devices can be used to drive terminated lines down to 133 Ω.

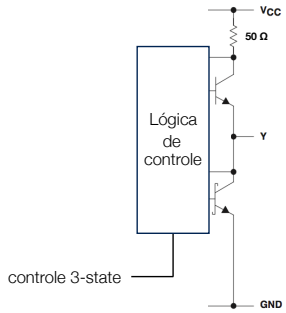


Texas Instruments, Inc. SN54LS240, SN54LS241, SN54LS244, ..., Octal Buffers and Line Drivers with 3-State Outputs; 2010

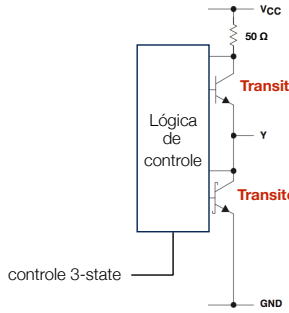
Tri-state



Tri-state

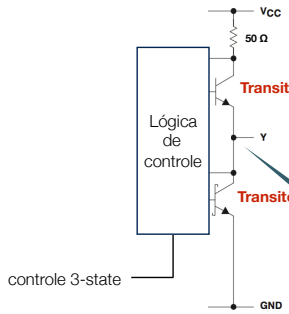


Tri-state



A	B	Estado
S	S	não ocorre
S	C	nível lógico HIGH
C	S	nível lógico LOW
C	C	3-state

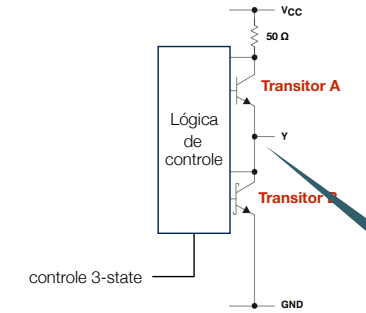
Tri-state



A	B	Estado
S	S	não ocorre
S	C	nível lógico HIGH
C	S	nível lógico LOW
C	C	3-state

Em 3-state a saída Y é desligada do circuito (saída em alta impedância)

Tri-state

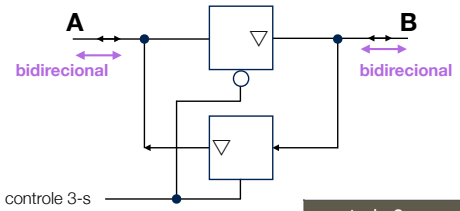


A	B	Estado
S	S	não ocorre
S	C	nível lógico HIGH
C	S	nível lógico LOW
C	C	3-state

Em 3-state a saída Y é desligada do circuito (saída em alta impedância)

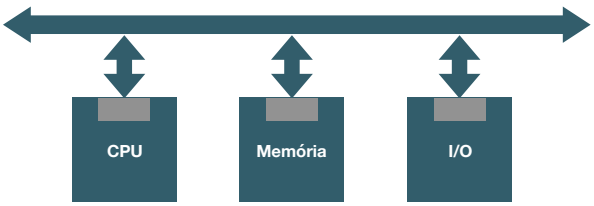
Controle 3-state	Estado da saída
0	níveis lógicos TTL
1	em alta impedância

Buffer Bidirecional

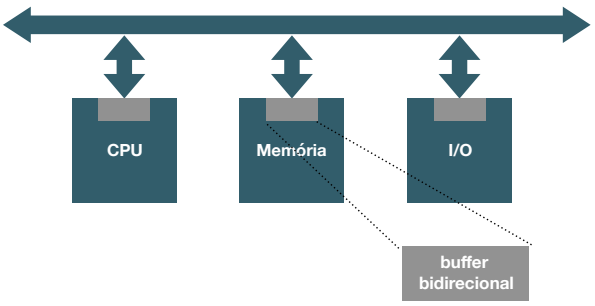


controle 3-s	direção
0	A → B
1	B → A

Barramento



Barramento



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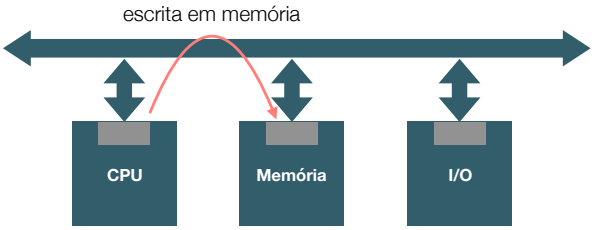

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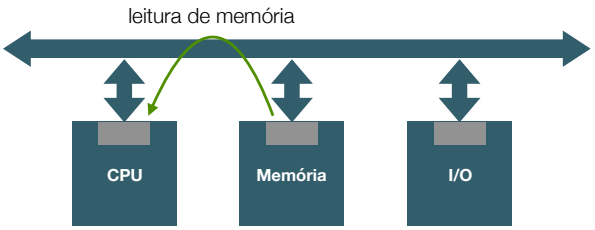

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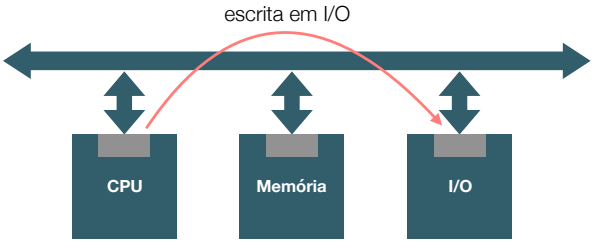
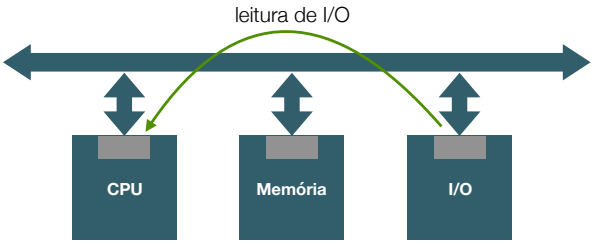


Barramento

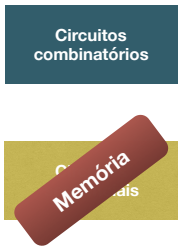


Memória

Circuitos combinatórios — Saída é função direta da entrada atual

Circuitos sequenciais — Saída depende da entrada e do estado anterior do circuito

Memória



Saída é função direta da entrada atual

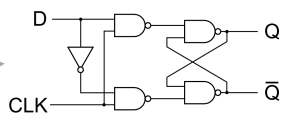
Saída depende da entrada e do estado anterior do circuito

Flip-flop

- Tipo R-S
- Tipo J-K
- Tipo D
- Tipo T

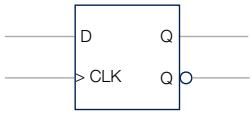
Flip-flop

- Tipo R-S
- Tipo J-K
- Tipo D
- Tipo T



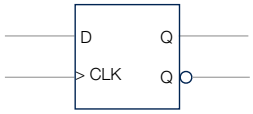
Flip-flop

- Tipo R-S
- Tipo J-K
- Tipo D
- Tipo T



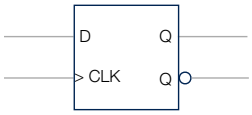
Flip-flop

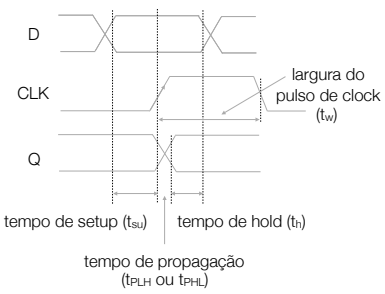
- Tipo R-S
- Tipo J-K
- Tipo D
- Tipo T



CLK	D	Q
↑	H	H
↑	L	L
L	x	Q^{ANT}

Flip-flop tipo D





Flip-flop tipo D

SN5474, SN54LS74A, SN54S74
SN7474, SN74LS74A, SN74S74
DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

SDLS119 – DECEMBER 1983 – REVISED MARCH 1988

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

These devices contain two independent D-type positive-edge-triggered flip-flops. A low level at the preset or clear inputs sets or resets the outputs regardless of the levels of the other inputs. When preset and clear are inactive (high), data at the D input meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the D input may be changed without affecting the levels at the outputs.

The SN54' family is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74' family is characterized for operation from 0°C to 70°C.

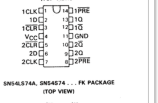
FUNCTION TABLE

INPUTS				OUTPUTS	
PRE	CLR	CLK	D	Q	Q̄
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H†	H†
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\bar{Q}_0$

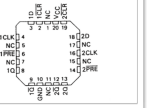
† The output levels in this configuration are not guaranteed to meet the minimum levels for V_{OH} if the lows at preset and clear are near V_{IL} maximum. Furthermore, this configuration is nonstable; that is, it will not persist when either preset or clear returns to its inactive (high) level.

SN5474 . . . J PACKAGE
SN54LS74A, SN54S74 . . . J OR W PACKAGE
SN7474 . . . N PACKAGE
SN74LS74A, SN74S74 . . . D OR N PACKAGE
(TOP VIEW)

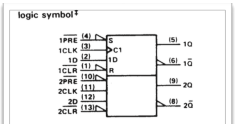
SN5474 . . . W PACKAGE
(TOP VIEW)



SN54LS74A, SN54S74 . . . FK PACKAGE
(TOP VIEW)

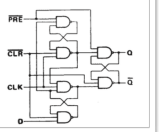


logic symbol‡



‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, N, and W packages.

logic diagram (positive logic)



Flip-flop tipo D

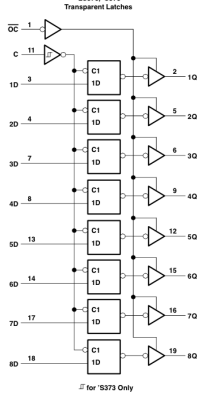
			SN54LS74A			SN74LS74A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current				−0.4			−0.4	mA
I_{OL}	Low-level output current				4			8	mA
f_{clock}	Clock frequency		0		25	0		25	MHz
t_w	Pulse duration	CLK high	25			25			ns
		$\overline{PRE}$ or $\overline{CLR}$ low	25			25			
t_{su}	Setup time-before CLK↑	High-level data	20			20			ns
		Low-level data	20			20			
t_h	Hold time-data after CLK↑		5			5			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			R_L = 400 Ω, C_L = 15 pF	15	25		MHz
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\bar{Q}$				25	ns
t_{PHL}						40	ns
t_{PLH}	CLK	Q or $\bar{Q}$			14	25	ns
t_{PHL}					20	40	ns

Texas Instruments, Inc. SN54LS74A, 74LS74A Dual D-Type Positive-Edge-Triggered Flip-Flops with Preset and Clear; 1988

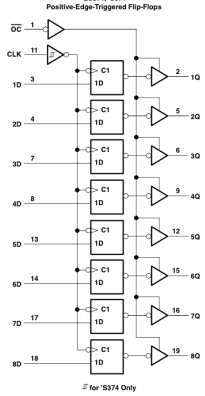
Registrador de 8-bits com saída 3-s

'LS373, 'S373
Transparent Latches



‡ for 'S373 Only

'LS374, 'S374
Positive-Edge-Triggered Flip-Flops



‡ for 'S374 Only

Function Tables

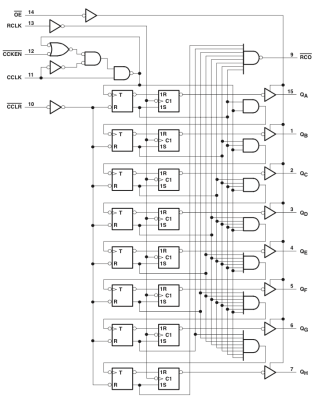
'LS373, 'S373
(each latch)

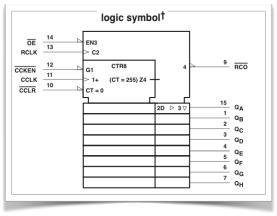
INPUTS			OUTPUT
$\overline{OC}$	C	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

'LS374, 'S374
(each latch)

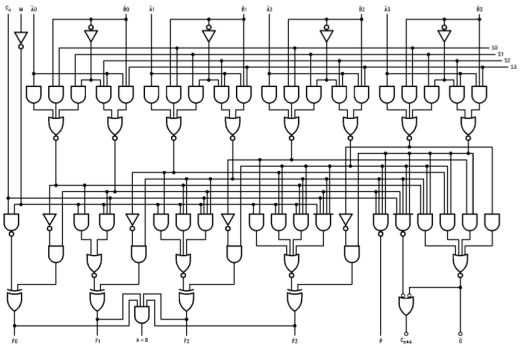
INPUTS			OUTPUT
$\overline{OC}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

Contador sincrono de 8-bits com saída 3-s

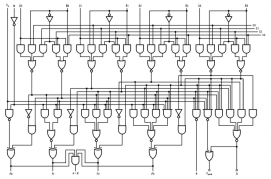


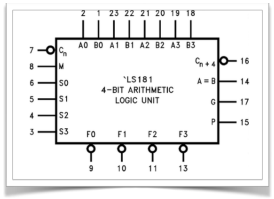


Unidade Lógico Aritmética



Unidade Lógico Aritmética





Mode Select Inputs				Active HIGH Operands & F_n Outputs	
				Logic	Arithmetic (Note 2)
S3	S2	S1	S0	(M = H)	(M = L) (C_n = H)
L	L	L	L	$\overline{A}$	A
L	L	L	H	$\overline{A + B}$	A + B
L	L	H	L	$\overline{A}$ B	A + $\overline{B}$
L	L	H	H	Logic 0	minus 1
L	H	L	L	$\overline{AB}$	A plus $\overline{AB}$
L	H	L	H	$\overline{B}$	(A + B) plus $\overline{AB}$
L	H	H	L	A ⊕ B	A minus B minus 1
L	H	H	H	$\overline{AB}$	AB minus 1
H	L	L	L	$\overline{A}$ + B	A plus AB
H	L	L	H	$\overline{A \oplus B}$	A plus B
H	L	H	L	B	(A + $\overline{B}$) plus AB
H	L	H	H	AB	AB minus 1
H	H	L	L	Logic 1	A plus A (Note 1)
H	H	L	H	A + $\overline{B}$	(A + B) plus A
H	H	H	L	A + B	(A + $\overline{B}$) plus A
H	H	H	H	A	A minus 1

Note 1: Each bit is shifted to the next most significar
Note 2: Arithmetic operations expressed in 2s comp