

PCS3515 – Sistemas Digitais

Blocos Básicos

Multiplicadores

Seções 6.11 – livro texto

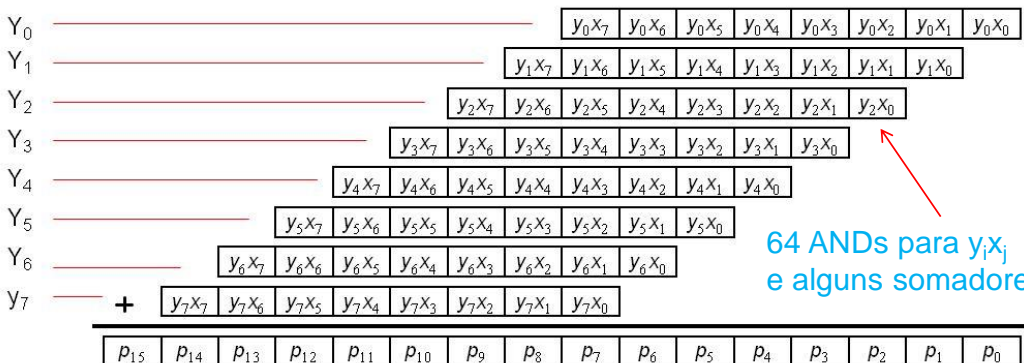
Com apoio do material dos demais professores

2018/1

From *Digital Design: Principles and Practices*, Fourth Edition, John F. Wakerly, ISBN 0-13-186389-4.
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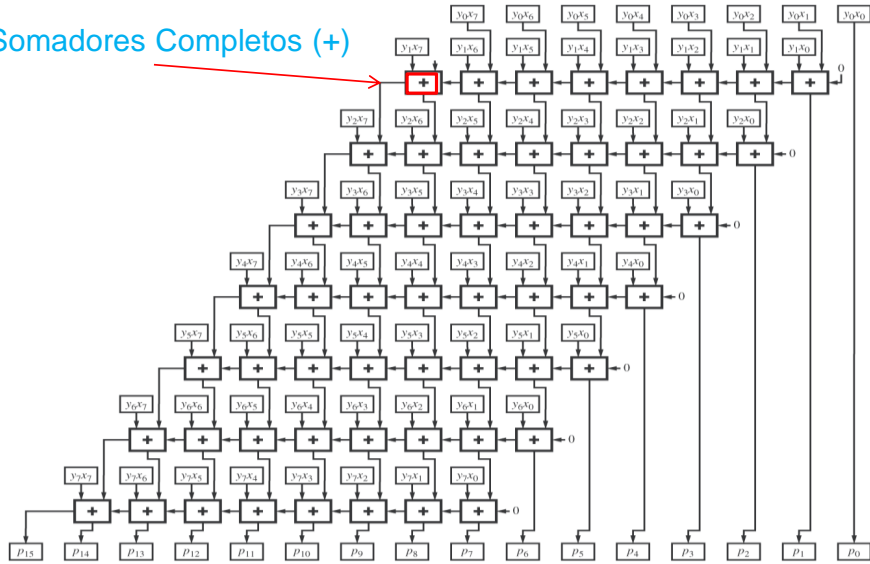
Multiplicador 8x8 dois inteiros sem sinal

Multiplicando $X = x_7x_6x_5x_4x_3x_2x_1x_0$
 Multiplicador $Y = y_7y_6y_5y_4y_3y_2y_1y_0$
 Produto $P = p_{15}p_{14}p_{13}p_{12}p_{11} \dots p_3p_2p_1p_0$



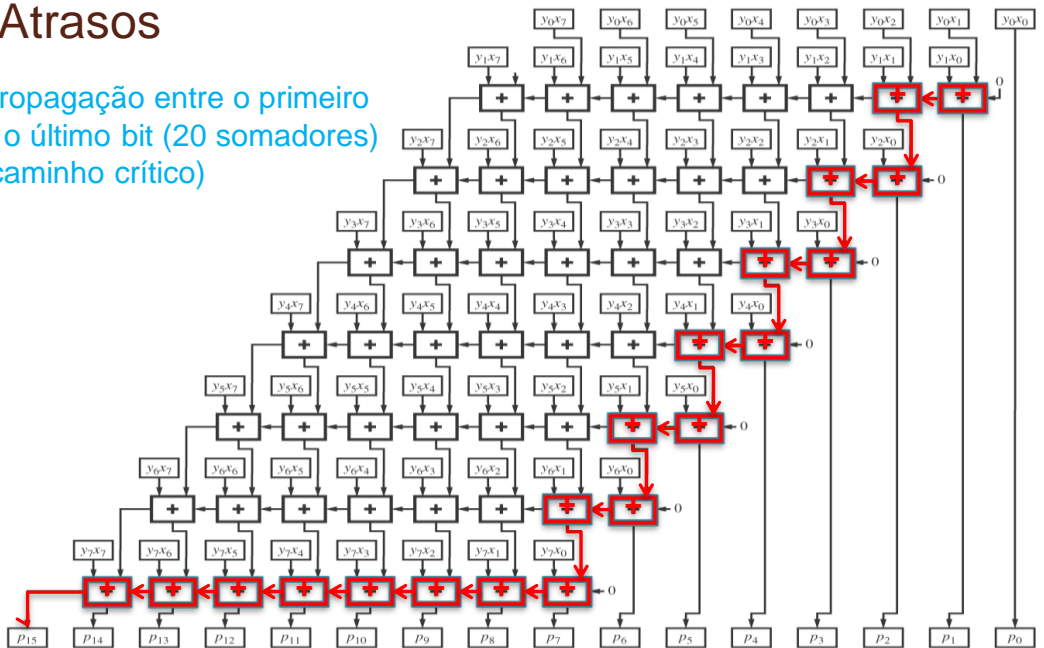
Multiplicador Combinatório

56 Somadores Completos (+)



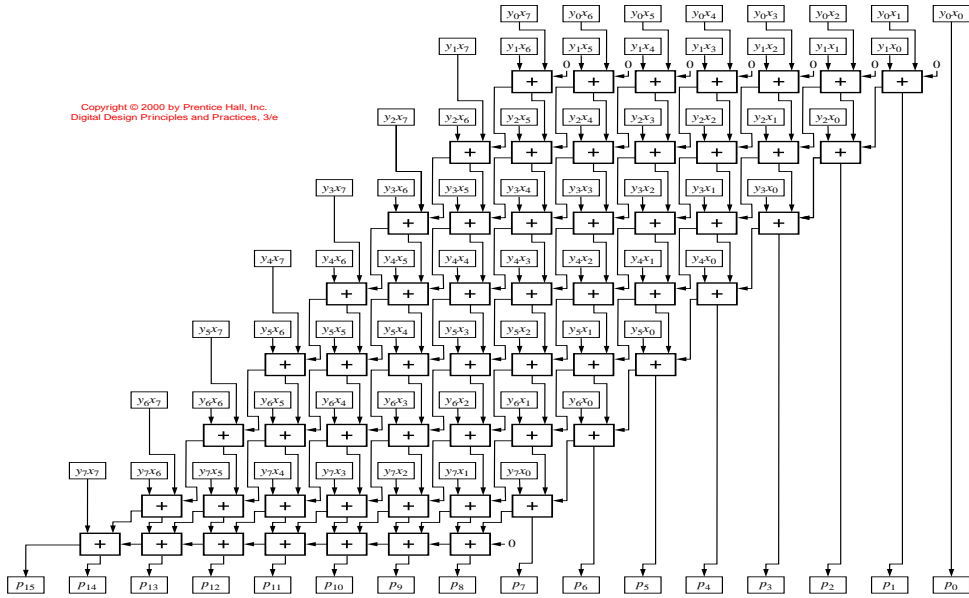
Atrasos

Propagação entre o primeiro e o último bit (20 somadores) (caminho crítico)



Faster 8x8 Multiplier

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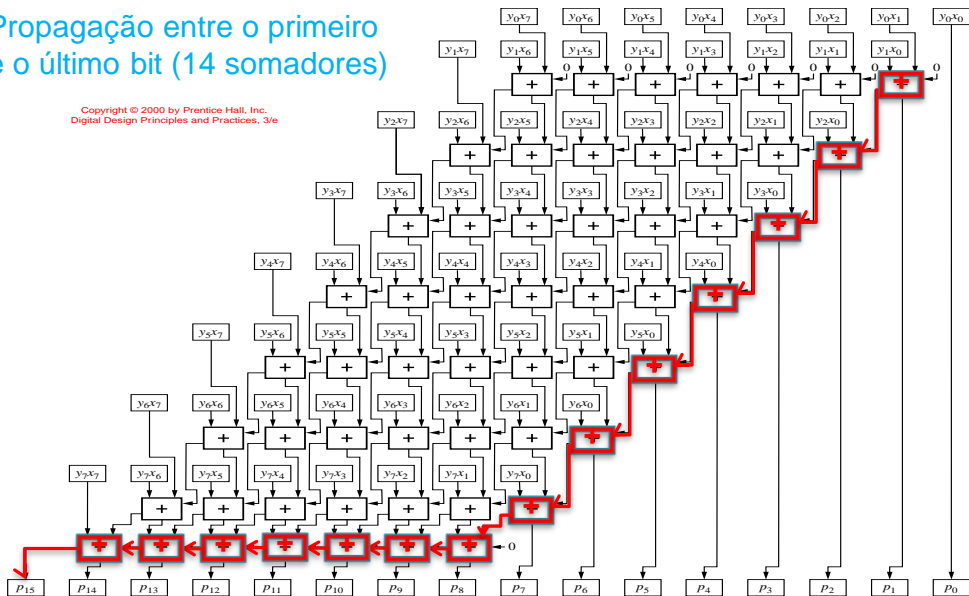


Spina

Faster 8x8 Multiplier

Propagação entre o primeiro e o último bit (14 somadores)

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Spina

Multiplicador 8x8 em VHDL (Comportamental)

```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_arith.all;

entity vmul8x8i is
    port (
        X: in UNSIGNED (7 downto 0);
        Y: in UNSIGNED (7 downto 0);
        P: out UNSIGNED (15 downto 0)
    );
end vmul8x8i;

architecture vmul8x8i_arch of vmul8x8i is
begin
    P <= X * Y;
end vmul8x8i_arch;
```
