Gain Limits for Current Loop Controllers of Single and Three-phase PWM Converters

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***Abstract*-- This paper analyzes Proportional (P) and Proportional-Integral (PI) techniques applied to current loop controllers of single and three phase Pulse Width Modulated (PWM) Power Converters. Gain limits are derived for both strategies based on intuitive per unit values of the grid and power converter parameters. Tracking response and disturbance rejection performances of each controller in continuous time domain are also evaluated. Simulation and experimental results for continuous time, as well as experimental results for discrete time are presented.**

***Index Terms*-- Controller design, Current loop control, PWM converters.**

I. Introduction

Multi loop control is a widely adopted control technique for Pulse Width Modulation power converters [1]. It consists of the concatenation of an inner current loop and an outer voltage loop, where the first and faster one is responsible for tracking the inductor current and also for providing overcurrent protection. The outer loop tracks the output voltage of the converter. This paper focuses only on the current loop control.

There are several control techniques applied to closed loop current control of PWM converters [1] and different arguments to decide which controller is best recommended to achieve current control satisfactory performance. Simpler strategies adopt Proportional (P) controllers [5], [6] combined with feedforward techniques. In [7] the integral part of the Proportional Integral controller of the current loop works as an anti-saturation control for the output transformer of an Uninterruptable Power Supply (UPS). The authors of [4] design a Proportional Integral Derivative (PID) current controller to achieve the same control objective. On the other hand, [2] states that PI controllers are not applicable to sinusoidal reference currents, and so Proportional-Integral-Sinusoidal (PIS) or Resonant Controllers shall be used. However, the design of current loop controller – gain selection, limits, performance criteria, etc - is one aspect that is poorly detailed in the literature.

This paper analyzes P and PI techniques by means of a novel approach, which consists in:

- Clarify why P and PI controllers are reasonable or not to be applied to current loops;

- Obtain minimum and maximum operation limits of proportional and integral gains. The operation constraints in continuous time presented in [3] are discussed, since a different result was obtained in this paper for the same control system. Moreover, the plant model and the derivation method to achieve gain limits in this paper are simpler and more intuitive than those previous presented in literature [3].

- Analyzing control system parameters in terms of per-unit values of the power converter and of the grid. This approach, which is more familiar to power system and power electronic engineers, allows the designer to clearly understand the influence of each inverter or grid parameter on the current control, independent of its power and voltage ratings.

This paper is organized as follows. Initially, the control system is modeled and per-unit parameters are presented. For each P and PI controller, the tracking and disturbance rejection responses are evaluated and gain limits are derived. Simulation and experimental results for a PWM converter with a second order output filter are then presented.

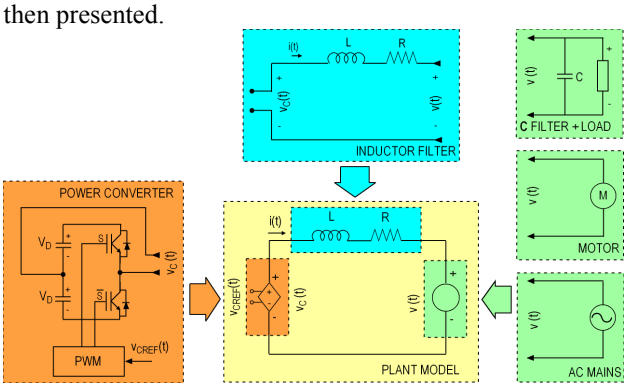

Fig. 1. Continuous time plant model (per phase model).

II. Plant Modeling

The per-phase circuit of the plant is shown in Fig. 1. Actually, the power converter may be single or three-phase, half or full-bridge topology - this last one can be switched with unipolar (3-level) or bipolar (2-level) PWM. The PWM block is initially considered to be an instantaneous PWM, implemented by a comparator of the reference voltage with a centered triangular carrier of frequency f_{TRI} whose amplitude varies between $-V_D$ and $+V_D$, where V_D is the DC-link voltage . The power converter plus the PWM block is represented by an averaged model of a voltage controlled source $v_C(t)$ with unitary gain. The converter is then series connected with a filter inductor of resistance R and inductance L, where $i(t)$ is the inductor current and $v(t)$ is the load side voltage. As can be seen in Fig. 1, this model may be used for a power inverter, where $v(t)$ will be the output voltage, or for grid-connected converters, where $v(t)$ will be the mains voltage, or for drives applications, where $v(t)$ will be the counter EMF of the motor.

All equations in this paper are developed in continuous

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time domain by considering a power inverter connected to $v(t)$. Besides that, in continuous time, it will be initially assumed that there are no actuation or computation time delays in the control system, which are inherent to discrete time setups.

The controlled system (Fig. 1), is described by (1) in the s-domain.

$$I(s)=\frac{V_C(s)-V(s)}{sL+R} \tag{1}$$

The main purpose of the current loop is to force the inductor current to follow a given reference current $i_{REF}(t)$, according to magnitude and phase tracking response performance criteria. Since the output voltage $v(t)$ represents a disturbance in the control loop, the controller must also reject it.

A. Per-unit variables definition

The following parameters are defined to express control variables in a per-unit system: $\overline{V}, \overline{I}$ (converter rated/base peak voltage and peak current), $\overline{Z}=\overline{V}/\overline{I}$ (converter base impedance), $\overline{\omega}$ (base angular frequency) and k_L (inductor per unit reactance). The inductor reactance and its quality factor are expressed, respectively, by (2) and (3):

$$\overline{\omega}L = k_L \cdot \overline{Z} \tag{2}$$

$$Q = \overline{\omega}L/R \tag{3}$$

In this work, it is considered that for a good inductor design Q > 10 and that $0.1 < k_L < 0.2$. Besides that, all gain limits are derived for the angular frequency $\overline{\omega}$ of the reference current.

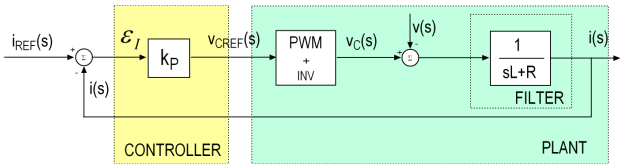

Fig. 2. Current loop proportional controller plus converter model.

III. Proportional Controller

Fig. 2 shows the simplest control strategy – Proportional (P) controller - with k_P gain applied to the current loop.

The tracking and disturbance transfer functions are given by (4) and (5), respectively:

$$\frac{I(s)}{I_{REF}(s)}=\frac{k_P}{sL+R+k_P} \tag{4}$$

$$\frac{I(s)}{V(s)}=\frac{-1}{sL+R+k_P} \tag{5}$$

Since the proportional gain k_P has impedance dimension, it can be described as a function of the filter reactance ωL, or of the base impedance $\overline{Z}$, and of the dimensionless parameter γ:

$$\gamma = k_P \,/\, (\overline{\omega}\cdot L) = k_P \,/\, (k_L \cdot \overline{Z}) \tag{6}$$

The tracking response and disturbance rejection performances depend on the choice of γ. It is assumed in this paper that $1/Q << \gamma$ (7).

A. Tracking transfer function evaluation

In (4), the tracking transfer function was obtained considering that there are no disturbances in the control loop. Moreover, initially, the effect of the modulator in Fig. 2 is neglected.

1) Magnitude

The magnitude of the tracking transfer function evaluated at the frequency ω is:

$$\left|\frac{I(\omega)}{I_{REF}(\omega)}\right|=\frac{k_P}{\sqrt{(\omega L)^2+(R+k_P)^2}} \tag{8}$$

Substituting (2), (3) and (6) into (8), considering $\omega=\overline{\omega}$ and (7):

$$\left|\frac{I(\overline{\omega})}{I_{REF}(\overline{\omega})}\right|=\frac{\gamma}{\sqrt{1+(1/Q+\gamma)^2}}\cong\frac{\gamma}{\sqrt{1+\gamma^2}} \tag{9}$$

2) Phase

The phase of the tracking transfer function evaluated at the frequency ω is:

$$\theta_{IT}(\omega)=-\tan^{-1}\left(\frac{\omega L}{R+k_P}\right) \tag{10}$$

Substituting (2), (3) and (6) into (10), for $\omega=\overline{\omega}$ and considering (7):

$$\theta_{IT}(\overline{\omega})=-tan^{-1}\left(\frac{1}{1/Q+\gamma}\right)\cong-tan^{-1}(1/\gamma) \tag{11}$$

Fig. 3 shows the magnitude and the phase of (4). An important result is that the proportional gain, for good tracking response, must be at least twice the converter base impedance if $k_L=0.2$ (worst case for k_L). For $\gamma>>10$, $|I(\overline{\omega})/I_{REF}(\overline{\omega})|\to 1$ and $\theta_{IT}\to 0$, i.e., P-controllers adopted in continuous time current loops provide small amplitude and phase error ($k_p>2\overline{Z}, k_L=0.2$), if the output voltage disturbance $v(t)$ is neglected. Chart of Fig. 3 may be useful for a estimative of the control parameters and of performance or for the design of P-controllers applied to current loops.

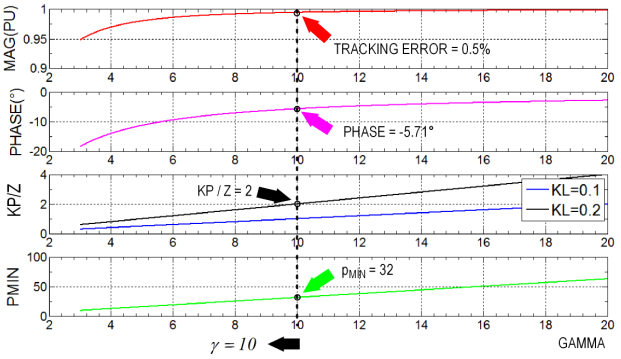

Fig. 3. Gamma selection, tracking response for γ = 10.

B. Maximum proportional gain for the triangular carrier PWM – Single phase converters

In Figure 1, consider now that the inverter is preceded by a PWM block and that the triangular carrier switching frequency f_{TRI} is much higher than the inverter reference voltage. The PWM converter reference voltage $v_{C\_REF}(t)$ may be divided in two components. The first term $\tilde{v}_{C\_REF}(t)$, which represents the ripple component is an alternating voltage with zero average value. The second component $\bar{v}_{C\_REF}(t)$ represents a low frequency term and dictates the inductor averaged current.

1) Slope condition

References [1] and [3] state that if the slope of PWM reference voltage is equal or greater than the slope of the triangular carrier, multiple crossing (switching) occurs. This result is the main assumption on the evaluation of gain limits in this paper and in [4]. In fact, as shown in this paper, the slope condition states that if the slope of the converter reference voltage is kept below the carrier slope, *multiple switching* in natural PWM and *instabilities* in natural or sampled PWM are avoided.

The slope of the converter reference voltage is the sum of a low-frequency behavior component $d\bar{v}_{C\_REF}(t)/dt$ and a ripple component $d\tilde{v}_{C\_REF}(t)/dt$. These components will be next determined. The inductor resistance may be neglected in this evaluation, because $L/R >>> f_{tri}^{-1}$, where f_{tri} is the triangular carrier frequency. For instance, supposing that $f_{TRI} = 10kHz \rightarrow T_{TRI} = 100\mu s$. A reasonable inductor design provides $Q = 10$, implying the time constant $\tau = L/R = 26.5ms >> 100\mu s$.

2) Low-frequency component of $v_{C\_REF}(t)$

The low frequency behavior of the reference voltage can be obtained by means of the control scheme of Fig. 2 and by the circuit analysis of Fig. 1. Applying the circuit analysis in Fig. 1, the locally averaged converter reference voltage $\bar{v}_{C\_REF}(t)$ that imposes the reference current $i_{REF}(t)$ is given by:

$$\bar{v}_{C\_REF}(t) = v(t) + L\frac{di_{REF}(t)}{dt} \tag{12}$$

Since sinusoidal reference voltages and currents of angular frequency ω are adopted, the maximum magnitude of the derivative of the low frequency converter reference voltage is given by:

$$\left|\frac{d\bar{v}_{C\_REF}(t)}{dt}\right| = \omega\cdot\sqrt{V_P^2 + \left(\omega LI_{REF\_P}\right)^2} = \omega\cdot V_{C\_P} \tag{13}$$

$$V_{C\_P} = \sqrt{V_P^2 + \left(\omega LI_{REF\_P}\right)^2} \tag{14}$$

where V_{C_P} , V_P and I_{REF_P} are the peak values of the converter output voltage $v_C(t)$, of the output voltage $v(t)$ and reference current $i_{REF}(t)$, respectively.

As stated in section IIA, the maximum filter inductor reactance in p.u. is $k_L = 0.2$. For 1 p.u. of the reference current, the amplitude of term ωLI_{REF_P} is equal to 0.2 p.u., which means that the amplitude of the converter reference voltage may vary between 0.8 and 1.2 p.u., depending on the phase angle of the inductor current. However, in practical implementation, the maximum peak value of the converter output voltage is $V_{C\_P} = V_D$, resulting in:

$$\left|\frac{d\bar{v}_{C\_ref}(t)}{dt}\right|_{MAX} = \omega\cdot V_D \tag{15}$$

The instant in which the maximum slope of locally averaged converter reference voltage $v_{C\_REF}(t)$ occurs is when the reference voltage is zero, that is t=0.

3) Ripple component of $v_{C\_REF}(t)$

In Fig. 2, the converter reference voltage is given by the product between the current error ε_I and the proportional gain. k_P The inductor voltage drop, considering only its ripple component is:

$$L\frac{d\varepsilon_I(t)}{dt} = v_C(t) - v_{C\_REF}(t) \tag{16}$$

If the full bridge topology and a 2-level PWM are assumed, the converter locally averaged output voltage varies between $\pm V_D$. The positive and negative inductor current slopes are respectively given by (17) and (18):

$$\frac{d\varepsilon_{I+}(t)}{dt} = \frac{V_D - v_{C\_REF}(t)}{L} \tag{17}$$

$$\frac{d\varepsilon_{I-}(t)}{dt} = \frac{-V_D - v_{C\_REF}(t)}{L} \tag{18}$$

The maximum positive inductor current slope occurs when $v_{C\_REF}(t) = -V_D$:

$$\frac{d\varepsilon_{I+}(t)}{dt} = \frac{2\cdot V_D}{L} \tag{19}$$

The maximum negative inductor current slope occurs when $v_{C\_REF}(t) = V_D$:

$$\frac{d\varepsilon_{I-}(t)}{dt} = -\frac{2\cdot V_D}{L} \tag{20}$$

Consequently the modulus of the maximum inductor current slope, considering a constant DC-link voltage is:

$$\left|\frac{d\varepsilon_I(t)}{dt}\right| = \frac{2\cdot V_D}{L} \tag{21}$$

The slope of ripple component of the converter voltage $\tilde{v}_{C\_REF}(t)$ is given by the multiplication of the current error ε_I by k_P (Fig. 2), which results:

$$\left|\frac{d\tilde{v}_{C\_REF}(t)}{dt}\right| = k_P\cdot\frac{d\varepsilon_I(t)}{dt} = k_P\cdot\frac{2\cdot V_D}{L} \tag{22}$$

The instant in which the maximum slope of the ripple

converter reference voltage $\tilde{v}_{C\_REF}(t)$ occurs is when the reference voltage is maximum, that is $t = n \cdot (\pi/2)$.

4) Slope of $v_{C\_REF}(t)$ and maximum proportional gain

The maximum slope of the converter reference voltage is the sum of (15) and (22), that is:

$$\left|\frac{dv_{C\_REF}(t)}{dt}\right| = \omega \cdot V_D + k_P \cdot \frac{2 \cdot V_D}{L} \tag{23}$$

The slope of a triangular carrier for a centered pulse PWM considering the DC-link voltage amplitude V_D is:

$$\left|\frac{dv_{TRI}}{dt}(t)\right| = \frac{2 \cdot V_D}{T_{TRI}/2} \tag{24}$$

where v_{TRI} is the carrier voltage and T_{TRI} is the carrier (switching) period. The slope condition states that:

$$\left|\frac{dv_{C\_REF}(t)}{dt}\right| < \left|\frac{dv_{TRI}}{dt}(t)\right| \tag{25}$$

Thus:

$$\omega + 2 \cdot k_P / L < 4 \cdot f_{TRI} \tag{26}$$

At this point, it must be noted that there is some mishandling on the development of gain limits of [3], which can be detected by a dimensional (units) check applied over the equations of [3], independently of the PWM pattern and of the number of phases of the converter. This mishandling can be avoided if the slope of the current error ε_I multiplied by k_P is kept below the carrier slope when deriving gain limits of current controllers and by checking the dimensions of (26).

Applying (6) and writing (26) as a function of the number of pulses per cycle p and of the fundamental frequency f:

$$\omega + 2 \cdot \gamma \cdot \omega L / L < 4 \cdot f \cdot p \tag{27}$$

$$1 + 2\gamma < 2p/\pi \tag{28}$$

$$\gamma_{MAX} = p/\pi - 1/2 \tag{29}$$

Since the number of pulses per cycle is in general high (p>10), (29) may be written as:

$$\gamma_{MAX} = p/\pi \tag{30}$$

Equation (30) shows that the predominant component of the slope condition is the ripple component of the reference voltage. Moreover, (30) defines *the maximum limit for the proportional gain of a current loop controller for a 2-level PWM single phase converter*, which can also be expressed as:

$$k_{PMAX} = 2 \cdot f_{TRI} \cdot L \tag{31}$$

For a given value of k_P (or γ), the minimum number of pulses per cycle, for sinusoidal reference, is:

$$p_{MIN} = \gamma \cdot \pi \tag{32}$$

Figure 3 shows that the values of γ, tracking error, phase error, k_p and minimum pulses per cycle (p_{MIN}) are related to each other. For example, for a 60Hz base frequency, if the switching frequency is defined as 1920Hz (p_{min} = 32), then γ_{max} = 10, the tracking error is 0.5%, the phase error is -5.71° and no instabilities or multiple switching will occur.

For a *single-phase full bridge converter with unipolar PWM, the maximum proportional gain is twice the result* of (31), since the maximum slope of the ripple component of the converter voltage is equal to $k_P \cdot V_D / L$.

C. Maximum proportional gain for the triangular carrier PWM – Three phase converters

For a three-phase three-leg PWM converter, it will be considered only the (predominant) ripple component of the converter reference voltage for the derivation of limit gains. The PWM converter (output) voltage has now five levels: $+4V_D/3 = V_{D\text{-}MAX}$, $+2V_D/3$, 0, $-2V_D/3$, $-4V_D/3 = -V_{D\text{-}MAX}$. In fact, if no zero sequence component is inserted at the reference voltage, the highest converter reference voltage amplitude which the converter can impose is $+V_D$.

There are three switching regions that are well defined when analyzing the PWM converter (output) voltage. The analysis of the maximum slope of the converter reference voltage will be done by means of the current slope, as done before, for each region. In the end, the current slope is multiplied by the proportional gain to obtain the converter reference voltage.

1) Region 1: $V_{C\text{-}REF}(t)$ from $4V_D/9$ to $4V_D/3$ ($V_{D\text{-}MAX}/3$ to $V_{D\text{-}MAX}$).

Figure 4 illustrates this region, where two cases are evaluated. The first case considers that the highest value of the converter reference voltage is $v_{C\_REF}(t) = V_D$. The maximum current slope occurs for the maximum variation of the PWM converter (output) voltage $v_C(t) = V_D - 0 = V_D$, and thus:

$$\left.\frac{d\varepsilon_I(t)}{dt}\right|_{MAX} = +\frac{V_D}{L} \tag{33}$$

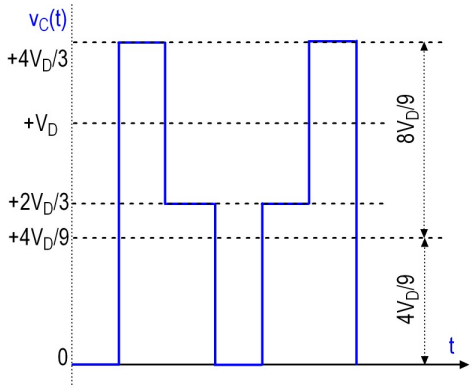

Fig. 4. Three phase converter gain limit derivation – Region 1.

In the second case, when a transition from Region 1 to region 2 occurs, the converter reference voltage is:

$$v_{C\_REF}(t) = V_{D\_MAX}/3 = (1/3) \cdot (4V_D/3) = (4V_D/9) \tag{34}$$

Consequently, the PWM voltage goes from $4V_D/3$ to $4V_D/9$, and thus the maximum current slope is:

$$\left.\frac{d\varepsilon_I(t)}{dt}\right|_{MAX} = \frac{1}{L}\left(\frac{4V_D}{3} - \frac{4V_D}{9}\right) = \frac{8V_D}{9L} \quad (35)$$

2) Region 2: $V_{C\text{-}REF}(t)$ from $-4V_D/9$ to $4V_D/9$ ($-V_{D\text{-}MAX}/3$ to $V_{D\text{-}MAX}/3$).

The maximum and minimum converter reference voltages are shown in Fig. 5 and are respectively $v_{C\_REF\_MAX}(t) = +4V_D/9$ and $v_{C\_REF\_MIN}(t) = -4V_D/9$. For this case, the PMW converter (output) voltage varies between $v_{C\_REF\_MAX}(t)$ and $v_{C\_REF\_MIN}(t)$ and thus the maximum current slope is:

$$\left.\frac{d\varepsilon_I(t)}{dt}\right|_{MAX} = \frac{1}{L}\left(\frac{4V_D}{9} + \frac{4V_D}{9}\right) = \frac{8V_D}{9L} \quad (36)$$

3) Region 3: $V_{C\text{-}REF}(t)$ from $-4V_D/9$ to $-4V_D/3$ ($-V_{D\text{-}MAX}/3$ to $V_{D\text{-}MAX}$).

Region 3 is symmetric to Region 1, and thus the maximum current slope is:

$$\left.\frac{d\varepsilon_I(t)}{dt}\right|_{MAX} = -\frac{V_D}{L} \quad (37)$$

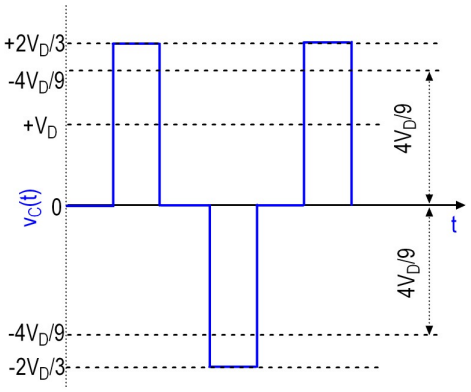

Fig. 5. Three phase converter gain limit derivation – Region 2.

4) Maximum Proportional Gain

The maximum slope of the converter reference voltage is obtained by multiplying (33) or (37) by the proportional gain $k_{P\_3\phi MAX}$ for the three-phase case. Considering only the predominant component of the converter voltage, (24) and the slope condition of (25):

$$k_{P\_3\phi} \cdot V_D / L < 2 \cdot V_D \cdot 2 \cdot f_{TRI} \quad (38)$$

$$k_{P\_3\phi MAX} = 4 \cdot f_{TRI} L = 2k_{PMAX} \quad (39)$$

It must be noted that the gain limit of (39) is different from result obtained in [3].

D. Harmonics in the reference current

The previous presented analysis is made for the fundamental frequency $\overline{\omega}$. If the reference current contains harmonics of angular frequency $h\overline{\omega}$, the inductor reactance k_L increases by a factor h. Since, for the same tracking performance achieved for the fundamental frequency, γ must be constant and thus the proportional gain k_P must also increase by a factor h according to (6).

However, the DC-link voltage limits the output of the converter and as a consequence, the converter reference voltage for $h\overline{\omega}$ may not be fully synthesized. As a consequence, if the same tracking performance is desired for frequencies above the fundamental frequency, the converter base (rated) voltage must be increased. In other words, if the converter is already defined, the gain limits for reference currents of $h\overline{\omega}$ is different of those obtained for $\overline{\omega}$.

E. Disturbance transfer function evaluation

1) Magnitude

The magnitude of the disturbance transfer function is:

$$\left|\frac{I(\omega)}{V(\omega)}\right| = \frac{1}{\sqrt{(\omega L)^2 + (R + k_P)^2}} \quad (40)$$

Substituting (2), (3) and (6) into (40), for $\omega = \overline{\omega}$ and considering (7):

$$\left|\frac{I(\overline{\omega})}{V(\overline{\omega})}\right| = \frac{1}{\overline{\omega}L\sqrt{1 + (1/Q + \gamma)^2}} \cong \frac{1}{k_L \cdot \overline{Z}\sqrt{1 + \gamma^2}} \quad (41)$$

2) Phase

The phase of the disturbance transfer function evaluated at the base frequency is:

$$\theta_{ID} = \pi - tan^{-1}\left(\frac{\omega L}{R + k_P}\right) \quad (42)$$

Substituting (2), (3) and (6) into (42) and considering (7):

$$\theta_{ID} = \pi - tan^{-1}\left(\gamma^{-1}\right) \quad (43)$$

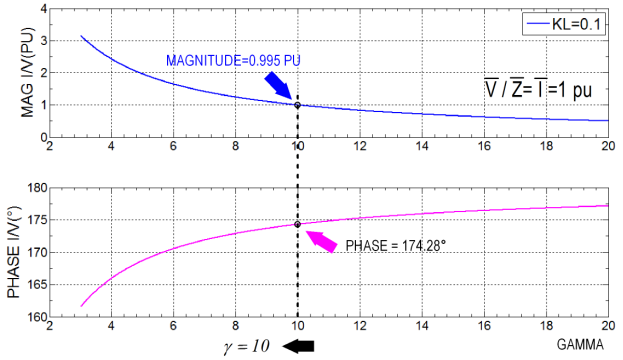

Fig. 6. Gamma selection, disturbance rejection response for $\gamma = 10$.

Figure 6 shows that the disturbance rejection of a P controller is poor for low values of γ. As an example, a 1 p.u. output voltage disturbance results in approximately 1 p.u. inductor current, for $\gamma = 10$. This result explains why a P-controller is not recommended to be applied to current closed loops. Next topic evaluates the tracking and disturbances performances of PI controller for the same plant of Fig.1.

IV. Proportional Integral Controller

The implementation of a Proportional Integral Controller for the current loop is shown in Fig. 7 where T_i is the integral time constant.

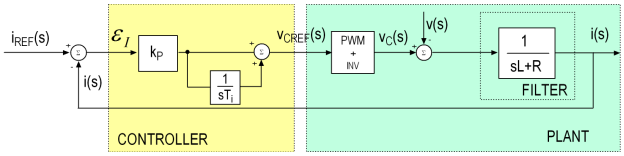

Fig. 7. Current loop proportional integral controller.

The tracking and disturbance transfer functions are given by (44) and (45), respectively:

$$\frac{I(s)}{I_{REF}(s)} = \frac{s\cdot(k_P/L)+(k_P/LT_i)}{s^2+s\cdot(R+k_P)/L+(k_P/LT_i)} \tag{44}$$

$$\frac{I(s)}{V(s)} = \frac{-s/L}{s^2+s\cdot(R+k_P)/L+(k_P/LT_i)} \tag{45}$$

The per-unit integral time constant is defined as function of the reference current period T:

$$\beta = T_i/T \tag{46}$$

A. Tracking transfer function evaluation

Substituting $s=j\omega$ into (44), considering $\omega=\overline{\omega}$ and (2), (3), (6) and (7), the magnitude and phase of the tracking transfer function evaluated at the base frequency are respectively given by (47) and (48):

$$\left|\frac{I(\overline{\omega})}{I_{REF}(\overline{\omega})}\right| = \frac{\gamma\sqrt{1+(2\pi\beta)^2}}{\sqrt{(\gamma-2\pi\beta)^2+(2\pi\beta\gamma)^2}} \tag{47}$$

$$\theta_{IT} = \tan^{-1}\left[-\frac{2\pi\beta\cdot(2\pi\beta+1/Q)}{(\gamma-2\pi\beta)+(2\pi\beta)^2\gamma}\right] \tag{48}$$

B. Design criteria

The closed loop tracking transfer function (44) has a zero at $1/T_i$ and two poles that can be expressed in the typical second order-system representation, where ξ is the damping factor and ω_d is the damped frequency:

$$\xi = \frac{R+k_P}{2}\sqrt{\frac{T_i}{L\cdot k_P}} = \sqrt{\frac{\gamma\cdot\pi\beta}{2}} \tag{49}$$

$$\omega_N = \sqrt{\frac{k_P}{L\cdot T_i}} = \omega\cdot\sqrt{\frac{\gamma}{2\pi\beta}} \tag{50}$$

If $\xi \geq \sqrt{2}/2$ is set as a design criterion to avoid under damped oscillations and high overshoots, then:

$$\beta \geq 1/\pi\gamma \tag{51}$$

If $\gamma_{MAX} = p/\pi$ (30) for a single phase 2-level PWM converter is applied to (51), (52) assures that no instabilities will occur if:

$$\beta_{MIN} = 1/p \tag{52}$$

Fig. 8 shows the operation region for tracking response of the PI controller. The magnitude will assume values slightly higher than 1, with tracking error higher than the P controller. As β increases, the controller will behave as a P controller, with the same responses of Fig. 3. The lower operation limit is given by β_{MIN} curve in fig. 8.

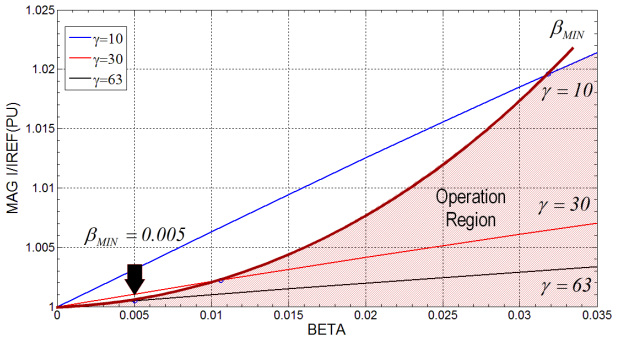

Fig. 8. Magnitude of tracking response for variation of β and γ.

The phase of the tracking transfer function (48) is lower than that obtained with a P controller, as can be seen in Fig. 9.

Optionally (but not derived in this paper), the damping factor can be calculated with respect to the disturbance transfer function and rejection performance criterion.

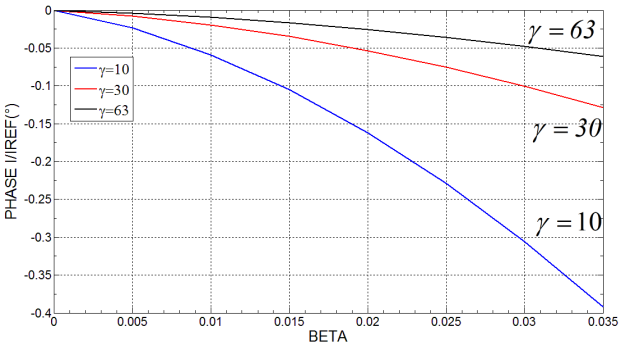

Fig. 9. Phase of tracking response for variation of β and γ.

C. Disturbance transfer function evaluation

In principle the PI controller presents no advantage over the P controller, if the disturbance $v(t)$ is not considered. Evaluating the disturbance transfer function by substituting $s=j\omega$ into (45) and by considering $\omega=\overline{\omega}$, (2), (3), (6) and (7), the magnitude and phase are respectively given by (53) and (54):

$$\left|\frac{I(\overline{\omega})}{V(\overline{\omega})}\right| = \frac{1}{k_L\cdot\overline{Z}\cdot\sqrt{(\gamma/2\pi\beta-1)^2+\gamma^2}} \tag{53}$$

$$\theta_{IV} = \tan^{-1}\left[\frac{1}{(2\pi\beta)}-\frac{1}{\gamma}\right] \tag{54}$$

Fig. 10 shows the magnitude of disturbance transfer function for $\beta<0.035$. It can be noted that it is worthless to operate with $\gamma<10$, since for $\gamma=10$ and $\beta=\beta_{MIN}\cong 0.03$, a 1 pu voltage at $v(t)$ produces a 0.2 pu current disturbance, which is high and thus inadequate. As a rule of thumb, $\gamma>20$ ($k_p>\overline{Z}, k_L=0.1$) and $\beta<0.016$ ($T_i<0.016T$) results in disturbance level lower than 5%. In spite of not providing zero tracking

error for the $\overline{\omega}$ frequency, and producing tracking errors slightly higher than the P controller without disturbances, the PI controller still produces reasonable tracking and disturbances performances. Charts of Figs. 8, 9 and 10 may be useful for a estimative of control parameters and performance or for the design of PI-controllers applied to current loops.

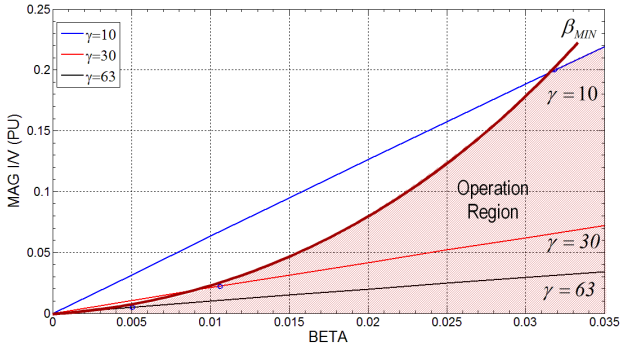

Fig. 10. Disturbance rejection for variation of β and γ.

V. Simulation and Experimental Results

A single-phase full bridge inverter with two-level PWM is simulated with PSIM 5.01 using the parameters of Table I ($\overline{Z} = 38\Omega$ and $k_L = 0.1$) for triangular carrier. Anti-windup strategies are not included.

TABLE I — Simulation Parameters

Parameter	Real value	PU value
Reference current	4.45 Apeak- 60Hz	0.9pu
DC link (base) voltage	187V	1 pu
Carrier/sampling frequency	12kHz	200 pu
Filter inductance/resistance	10mH/ 0.65 Ω	0.1pu/ 0.017pu
Filter capacitance/ R load	6.8μF / 34Ω	10 pu/0.9 pu

A. Proportional gain limit

In Fig. 11, the effect of gain above the limit of (31) is simulated for a P-controller and a zero-order-hold (ZOH) sampled 2-level PWM, and the output voltage disturbance is canceled by means of a positive feed forward of the output voltage. The proportional gain is set to $1.25 \cdot k_{PMAX}$, where $k_{PMAX} = 240\Omega$ (γ = 63 or k_P/Z = 6.3). Multiple switching is avoided, but instabilities take place. Converter reference and carrier voltages in Fig. 11 are divided by the DC-link voltage.

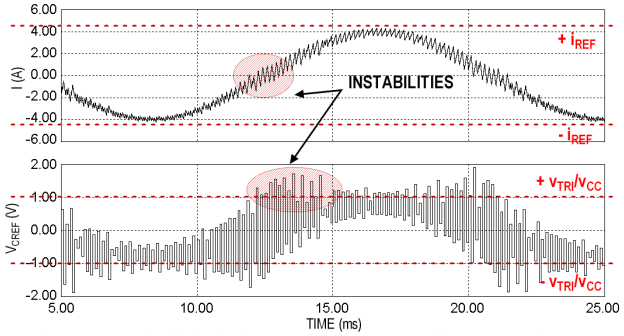

Fig. 11. P-gain limit, inductor current (top) and inverter reference voltage (bottom), k_P=1.25$k_{P\text{-}MAX}$ – simulation results for sampled PWM.

Fig. 12 shows experimental results for the same case of Fig. 11 and parameters of Table I. As can be seen, instabilities are present in the current, which shows that the derived gain limits are also valid for sampled PWM.

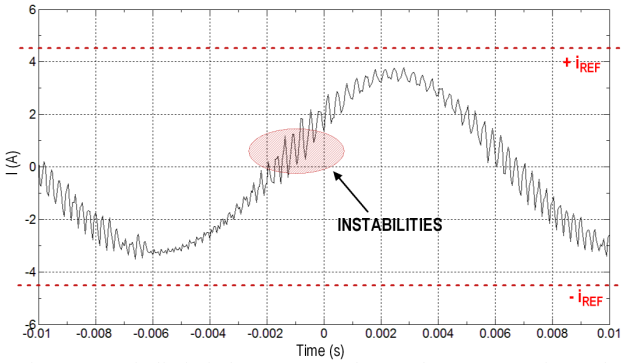

Fig. 12. P-gain limit, inductor current, k_P=1.25$k_{P\text{-}MAX}$ – experimental results.

Simulations results for an instantaneous PWM are shown in [4], where the proportional gain above the derived limit results in multiple switching.

B. Reference tracking and Disturbance rejection performances

The P and PI controllers were simulated with an instantaneous 2-level PWM for $k_{PMAX} = 240\Omega$ (γ_{MAX} = 63). As can be seen in Fig. 8, if γ_{MAX} = 63 then β_{MIN} = 0.005 ($T_{i\_MIN} = 83.33\mu s$). Figure 13 shows the tracking response of the P-controller with output voltage disturbance, where the tracking response is poor and the magnitude error is ≅12.5%. If the integral minimum gain is inserted, the response is improved (Fig. 14) and the magnitude tracking error diminishes ≅0.1%, as expected from Fig. 8. If the integral constant is decreased, instabilities will take place, since the parameter β is a minimum limit. The initial overshoot can be reduced by including an anti windup strategy.

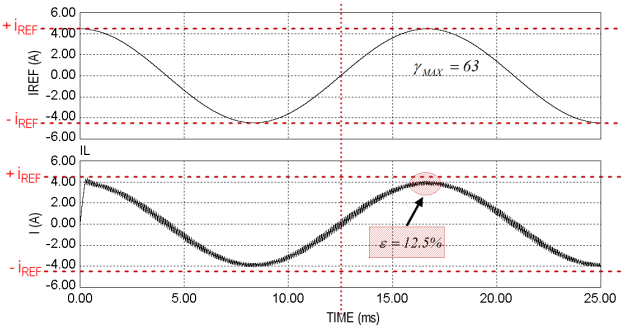

Fig. 13. P-Controller– simulation results. Reference current (top), inverter current (bottom)

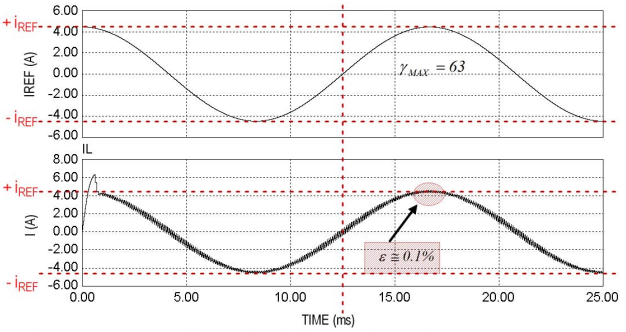

Fig. 14. PI- Controller – simulation results. Reference current (top), inverter current (bottom)

If the output voltage is summed up with the converter reference voltage [3],[4],[5],[6], i.e., if a feedforward

action is included, the disturbance at the current loop is canceled, tracking response is improved and magnitude and phase errors can be negligible. Despite PI-controller and feedforward techniques have great disturbance rejection performance, the feedforward technique is superior for transient conditions[4].

VI. Conclusion

This paper has presented operation ranges of proportional and integral gains and charts, useful for design of current controllers. Results are summarized in Table II. Moreover, these limits are expressed in terms of intuitive and well known converter or grid parameters, constituting a p.u. base for the design of controllers.

TABLE II – CONTINUOUS TIME P AND I GAINS LIMITS

Gain	Unit	Minimum	Maximum
P	PU	$k_{PMIN} = 2 \cdot \overline{Z}$	Single Phase, 2-level PWM: $\gamma_{MAX} = p/\pi$
			Single Phase, 3-level PWM and Three Phase-3wire: $\gamma_{MAX} = 2p/\pi$
I	PU	$\beta_{MIN} = 1/\pi\gamma$	-

It was also shown that P-controllers, with no feedforward technique, are not recommended to be employed in current loops, since the disturbance rejection performance is poor.

The same investigation is being developed to discrete time domain and some results are presented in Appendix I.

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Appendix I

Some Results for Discrete Time

Results of proportional controller in discrete time for single update (SU) and double update (DU) sampled PWM are presented in Table III. Admitting a ZOH discretization of the plant with one switching period delay, a P-controller at the current loop and a switching frequency much higher (e.g. 10 times) than the higher closed loop frequency, the closed loop damping factor and the damped angular frequency ω_D are respectively given by (55) and (56):

$$\xi = -\frac{\frac{1}{2}\cdot\ln\left(\frac{k_P T_A}{L}\right)}{\tan^{-1}\left(\sqrt{\frac{4k_P T_A L}{(L-RT_A)^2}-1}-\frac{1}{2}\cdot\ln\left(\frac{k_P T_A}{L}\right)\right)} \quad (55)$$

$$\omega_D = \omega_A \cdot \frac{1}{2\pi}\cdot\tan^{-1}\left(\sqrt{\frac{4k_P T_A L}{(L-RT_A)^2}-1}\right) \quad (56)$$

TABLE III – DISCRETE TIME PROPORTIONAL GAIN LIMITS

Gain		Damping Factor	Damped Frequency
Single update	$\gamma_D \cong \gamma_{MAX}/6$	$\xi = \sqrt{2}/2$	$\omega_D = 0.25\omega_A$
Double update	$\gamma_D \cong \gamma_{MAX}/3$		

Table III shows that limits are more restrict than those derived to continuous time and a 2-level PWM (e.g. six times lower than continuous time limit when ξ=0.707 for single update mode). The sampling frequency is equal to ω_A.

Figure 15 shows experimental results for a discrete time P-controller without disturbance compensation and a 2-level sampled PWM, in single update mode, with parameters of Table III. The amplitude of the damped is attenuated and no instabilities occur for this condition. As expected, the disturbance rejection of the controller is poor (simulated and experimental errors are approximately 55%), since no integral gain or feedforward technique is adopted in the control loop.

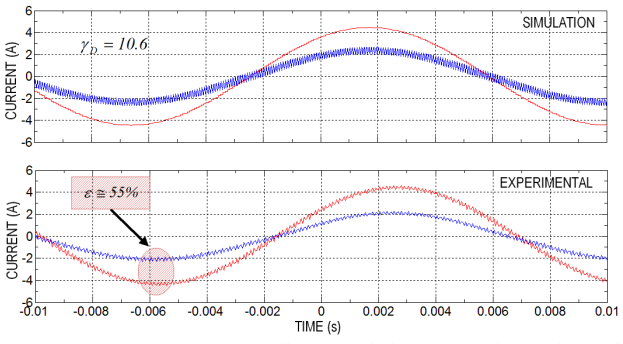

Fig. 15. Discrete time P-Controller– Simulation (top) and Experimental (bottom) results. Reference current (red), inverter current (blue)