USP - ICMC - SSC

SSC 0511 - Sist. Informação - 2o. Semestre 2014

Disciplina de Organização de Computadores Digitais

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Página Pessoal: http://www.icmc.usp.br/~fosorio/

Material on-line: Wiki ICMC:

http://wiki.icmc.usp.br/index.php/SSC-511-2014(fosorio)

IRM
Lab. de Robótica Móvel
CROB
Centro de Robótica da USP

Aula 02t

Tópicos da Aula

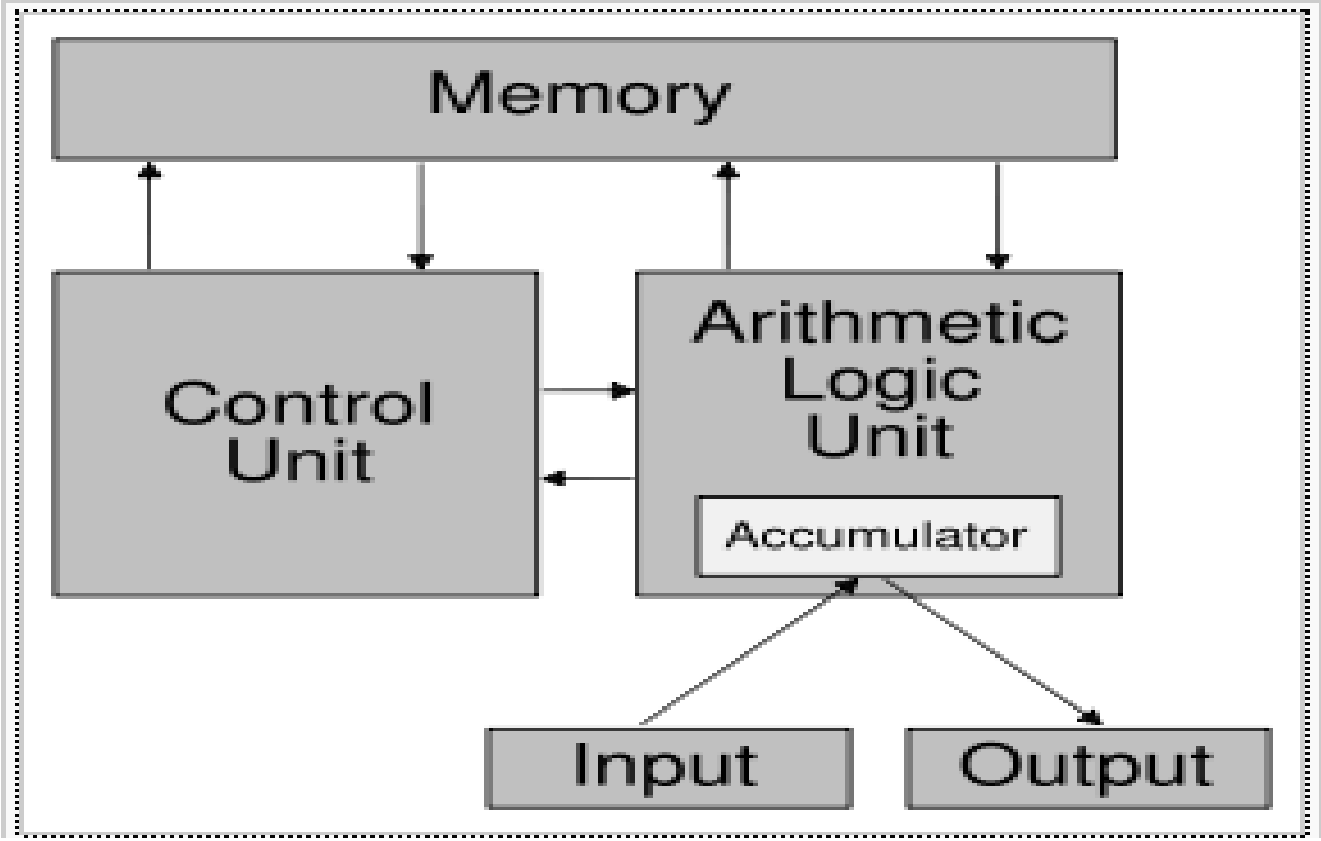
Agenda:

1. Arquitetura de Von Neumann:
   ULA, Memória, Registradores, UC e E/S
2. Memória – Conceitos Básicos
   - Flip-Flops, Registradores e Contadores
   - Registradores: Acumulador
   - Registradores: Registro de Instrução
   - Registradores: Contador de Programa
   - Registradores: Flags
   - Memória: Barramento e Acesso a Memória
3. Micro-Processadores...

1. Arquitetura de Von Neumann

Arquitetura - Modelo Inicial:

- Máquina de von Neumann



Refs: http://en.wikipedia.org/wiki/Von_Neumann_architecture

1. Arquitetura de Von Neumann

Arquitetura - Modelo Inicial:

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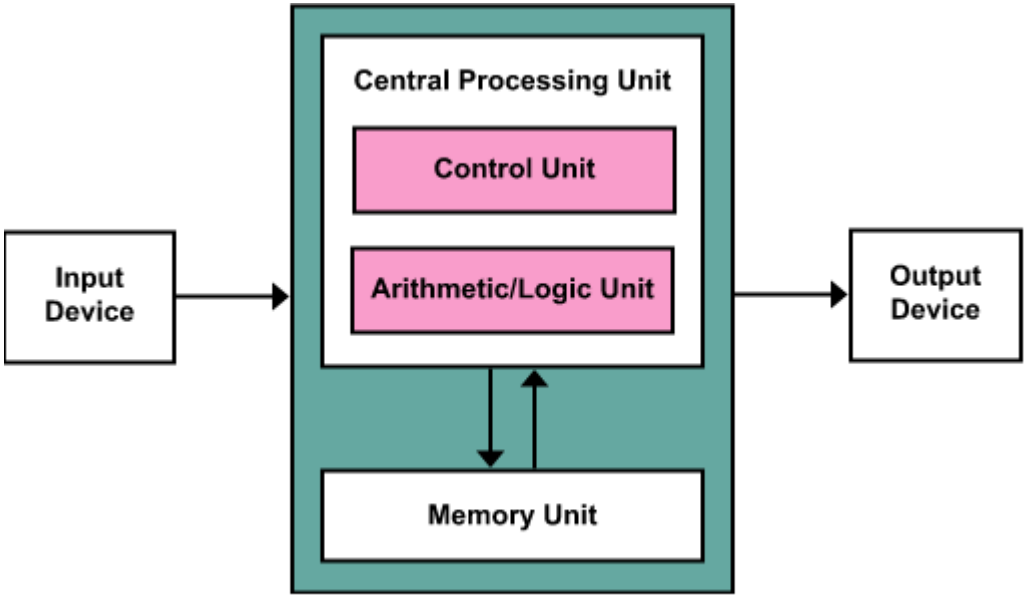

1. Arquitetura de Von Neumann

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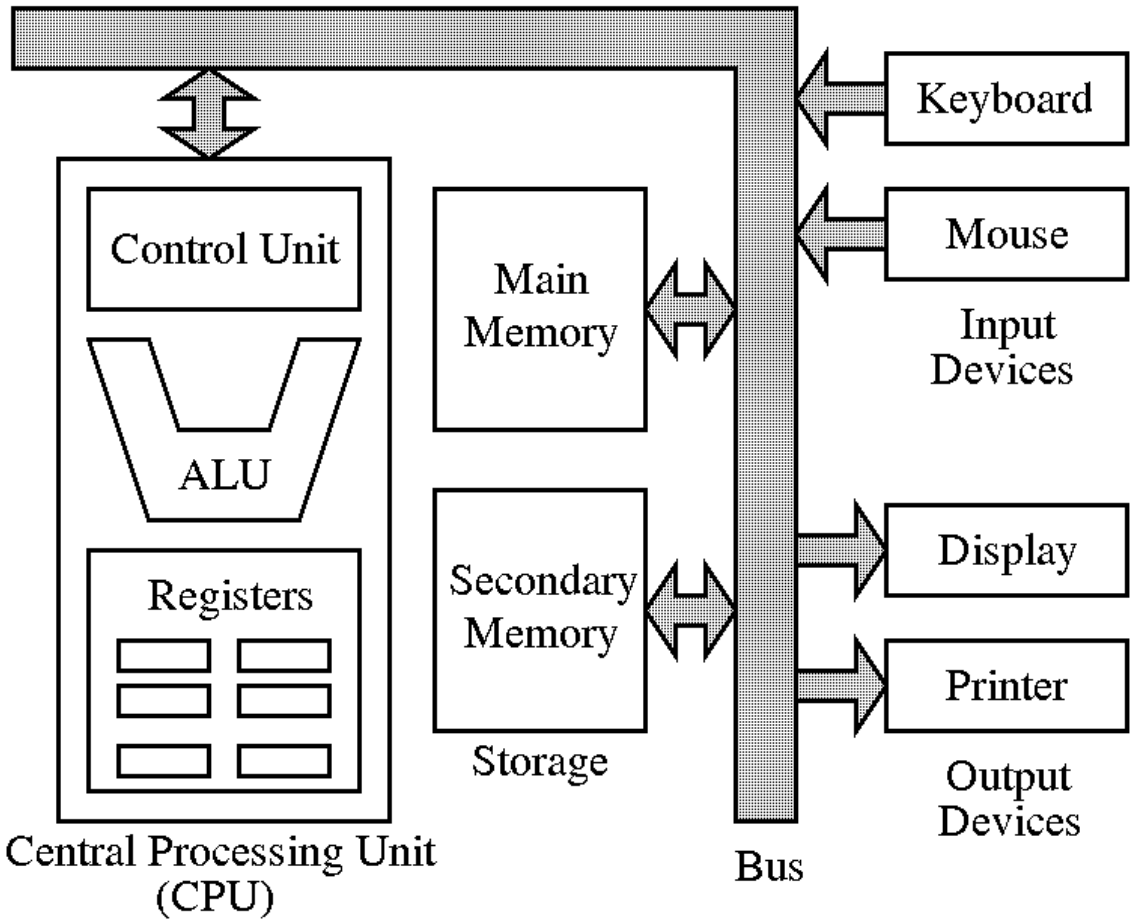
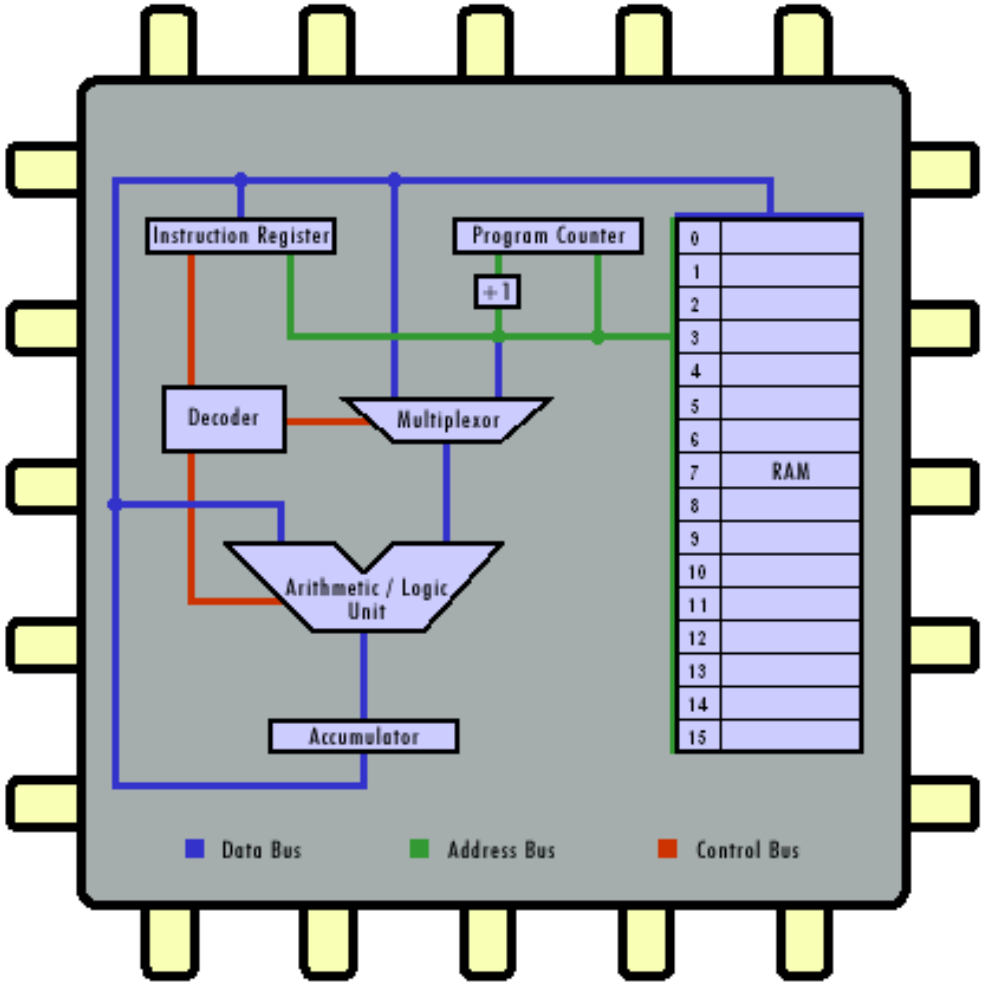


https://www.youtube.com/watch?v=5BpgAHBZgec

1. Arquitetura de Von Neumann

CPU – Processador

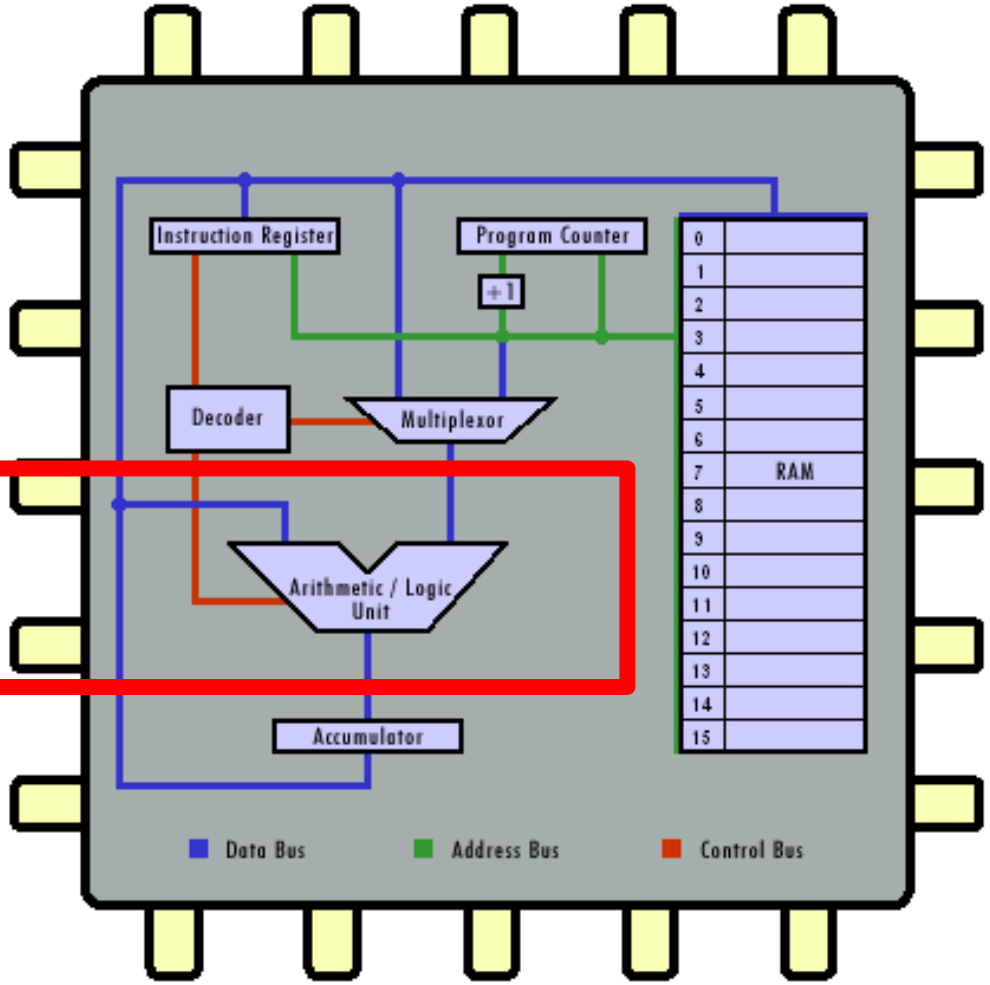


Fonte: http://courses.cs.vt.edu/~csonline/MachineArchitecture/Lessons/CPU/index.html

Arquitetura de Von Neumann

CPU – Processador

ULA / ALU
Unidade Lógico-Aritmética

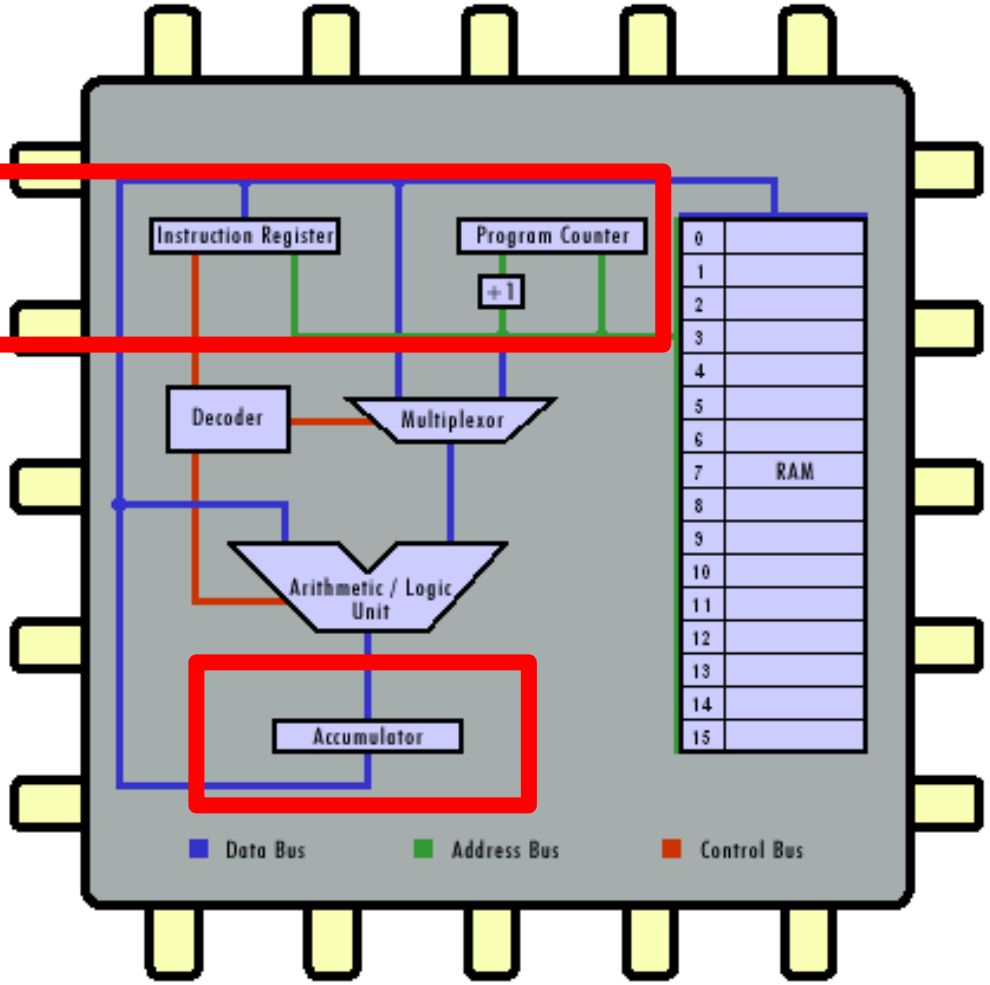


Fonte: http://courses.cs.vt.edu/~csonline/MachineArchitecture/Lessons/CPU/index.html

1. Arquitetura de Von Neumann

CPU – Processador

Registradores



Registradores

Program Counter: PC (CP)
Instruction Register: IR (RI)
Accumulator: Acc (AC)
Status Register - Flags: Flags

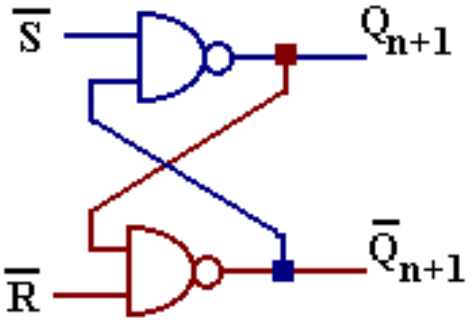
Fonte: http://courses.cs.vt.edu/~csonline/MachineArchitecture/Lessons/CPU/index.html

2. Memória – Conceitos Básicos

FLIP-FLOP RS Básico

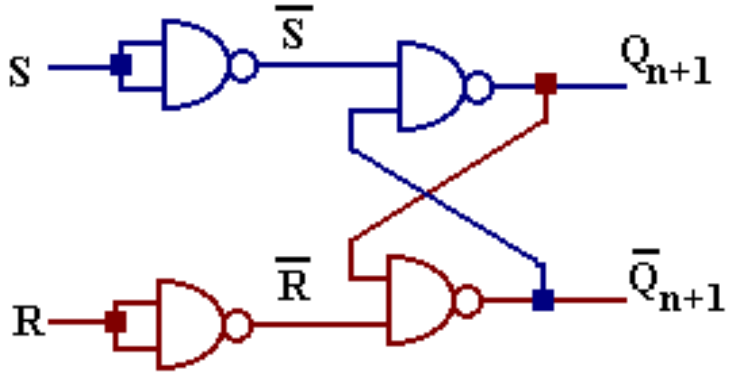
Memória de 1 bit

FLIP-FLOP RS



$\overline{S}$	$\overline{R}$	Q_{n+1}	$\overline{Q}_{n+1}$	
0	0	proibida		
0	1	1	0	Estado Set
1	0	0	1	Estado Reset
1	1	Q_n	$\overline{Q}_n$	Latch (memória)

FLIP-FLOP RS



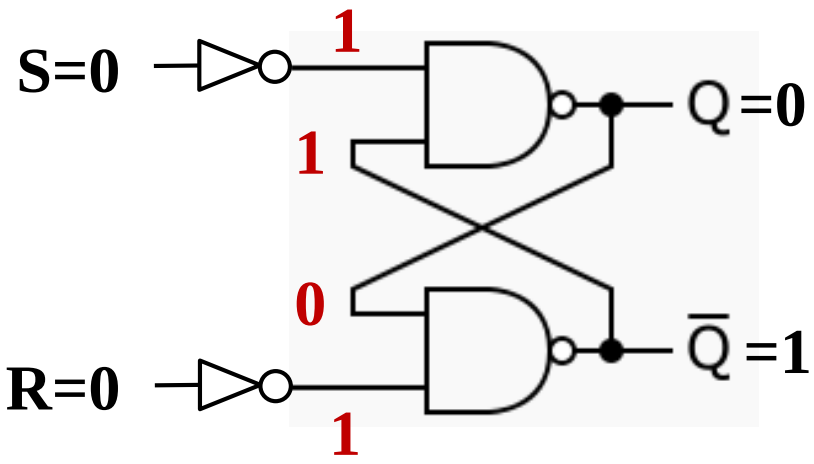
S	R	Q_{n+1}	$\overline{Q}_{n+1}$	
0	0	Q_n	$\overline{Q}_n$	Latch (memória)
0	1	0	1	Estado Reset
1	0	1	0	Estado Set
1	1	proibida		

Fonte: http://endigital.orgfree.com/sequencial/sequencial.htm

2. Memória – Conceitos Básicos

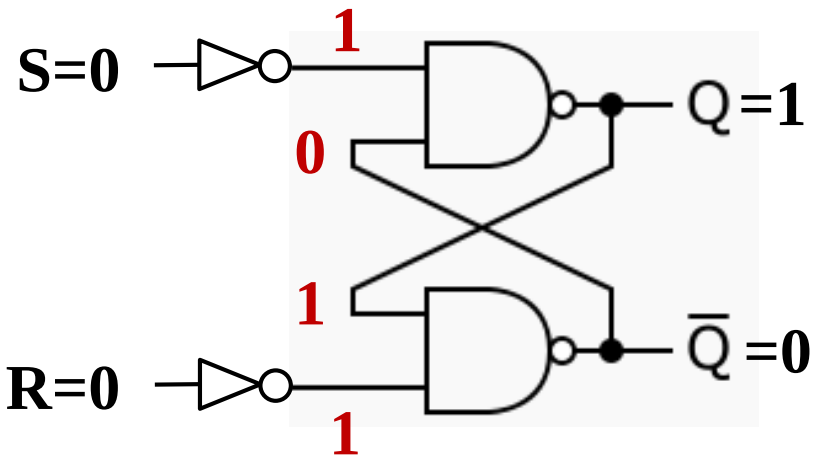
FLIP-FLOP RS Básico

Memória de 1 bit



$Q_{(t-1)} = 0$

$\overline{Q}_{(t-1)} = 1$



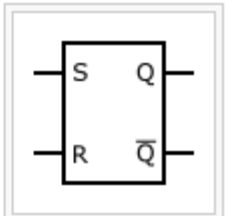
$Q_{(t-1)} = 1$

$\overline{Q}_{(t-1)} = 0$

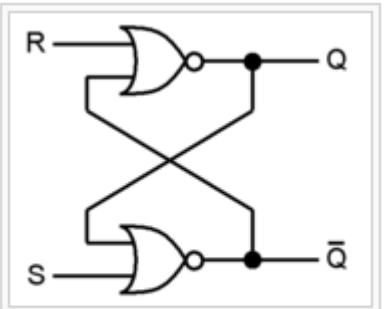
2. Memória – Conceitos Básicos

SR LATCH (FLIP-FLOP)

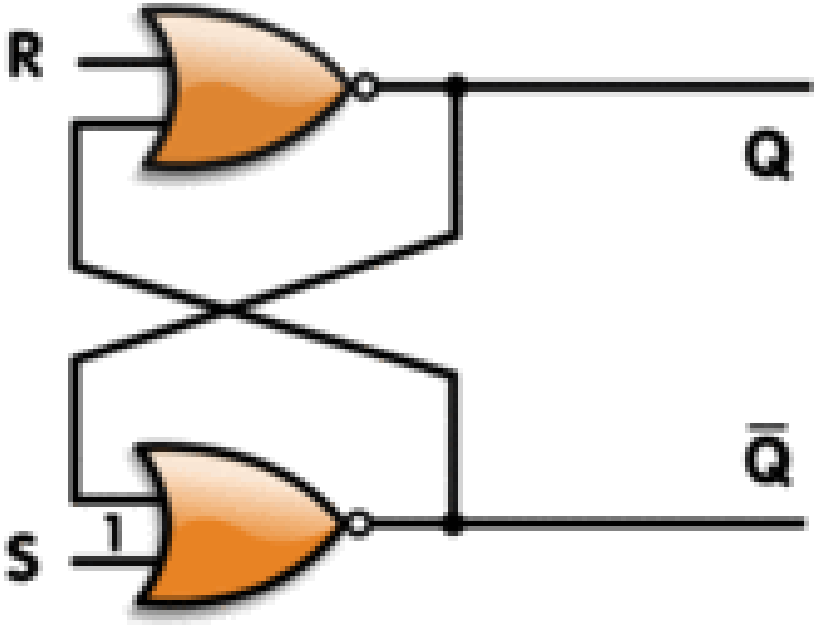
SR latch operation		
S	R	Action
0	0	Keep state
0	1	Q = 0
1	0	Q = 1
1	1	Restricted combination



The symbol for an SR latch.



SR latch

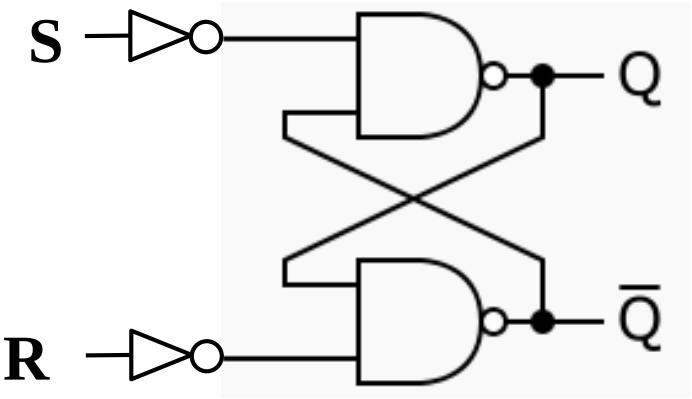


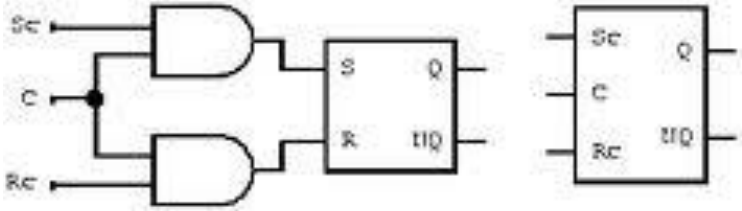
Memória de 1 bit

2. Memória – Conceitos Básicos

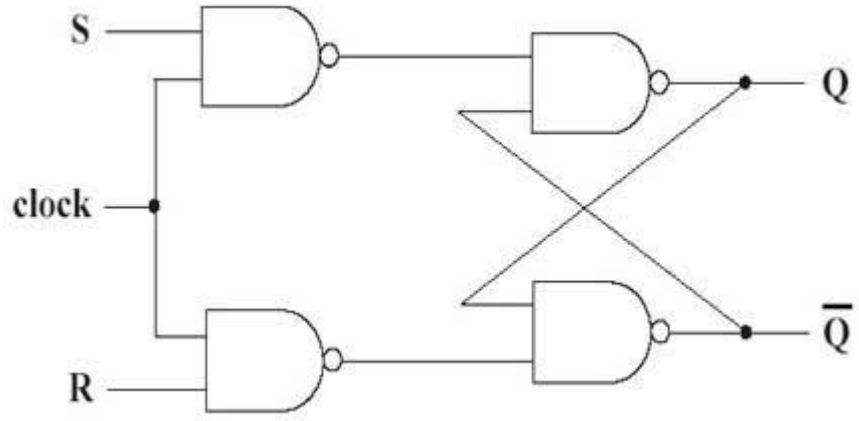
FLIP-FLOP RS com Clock

Memória de 1 bit





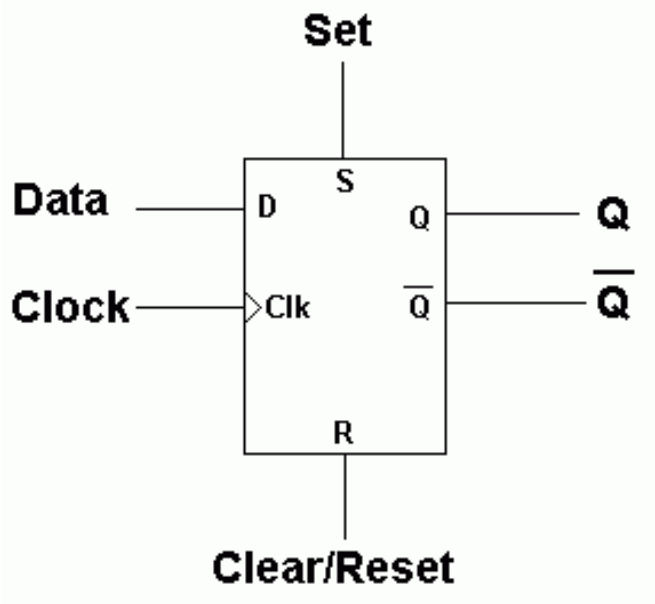
S_C	R_C	C	Q	$\overline{Q}$
x	x	0	no change	
0	0	1	no change	
0	1	1	0	1
1	0	1	1	0
1	1	1	undefined	
0	0	p	no change	
0	1	p	0	1
1	0	p	1	0
1	1	p	undefined	



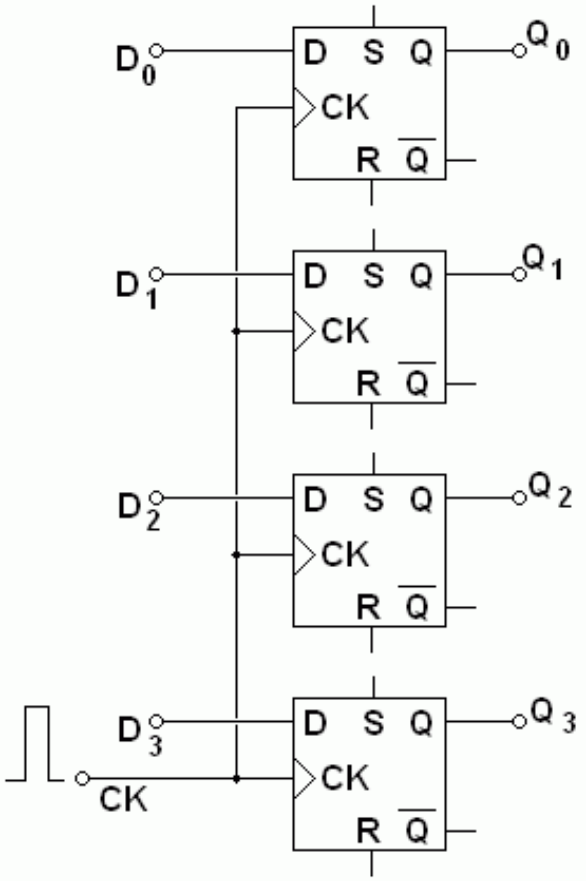
Flip-Flop:
RS, RS + Clock,
D, JK, Master-Slave

2. Memória – Conceitos Básicos

D LATCH (FLIP-FLOP)



Memória de 1 bits

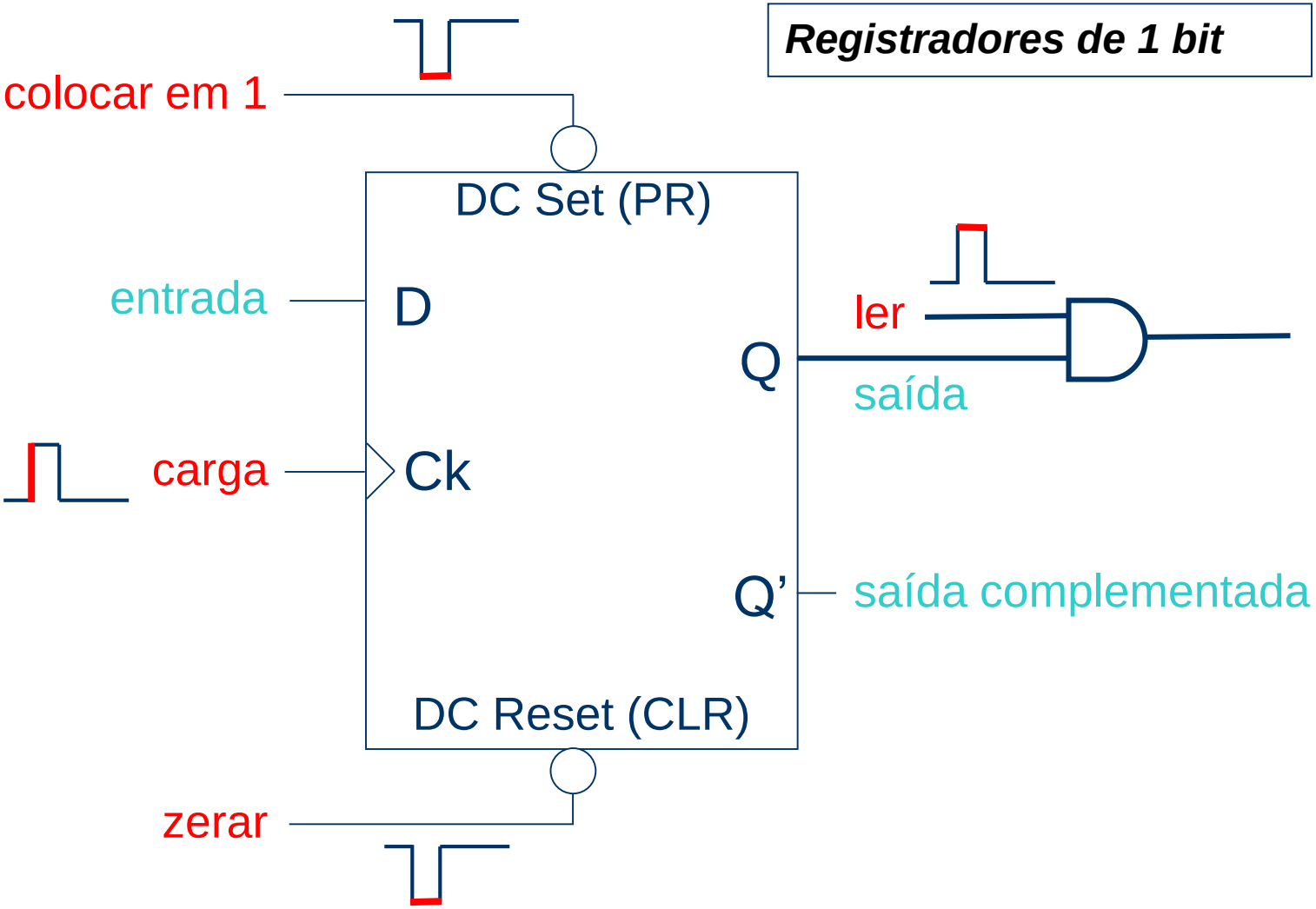


Memória de 4 bits

2. Memória – Conceitos Básicos

Unidade de Memória

Registradores de 1 bit



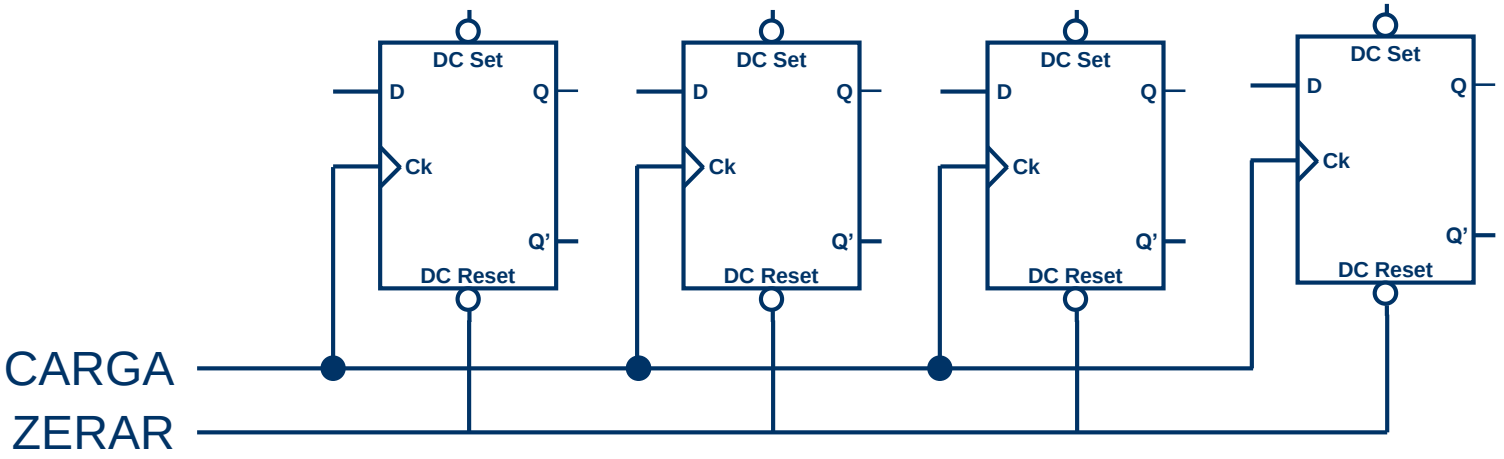
Fonte: ftp://ftp.inf.ufrgs.br/pub/inf107/ (RegMemAlu)

2. Memória – Registradores

Unidade de Memória

- um flip-flop por bit
- sinais de controle comuns a todos os flip-flops

Registradores de de vários bits



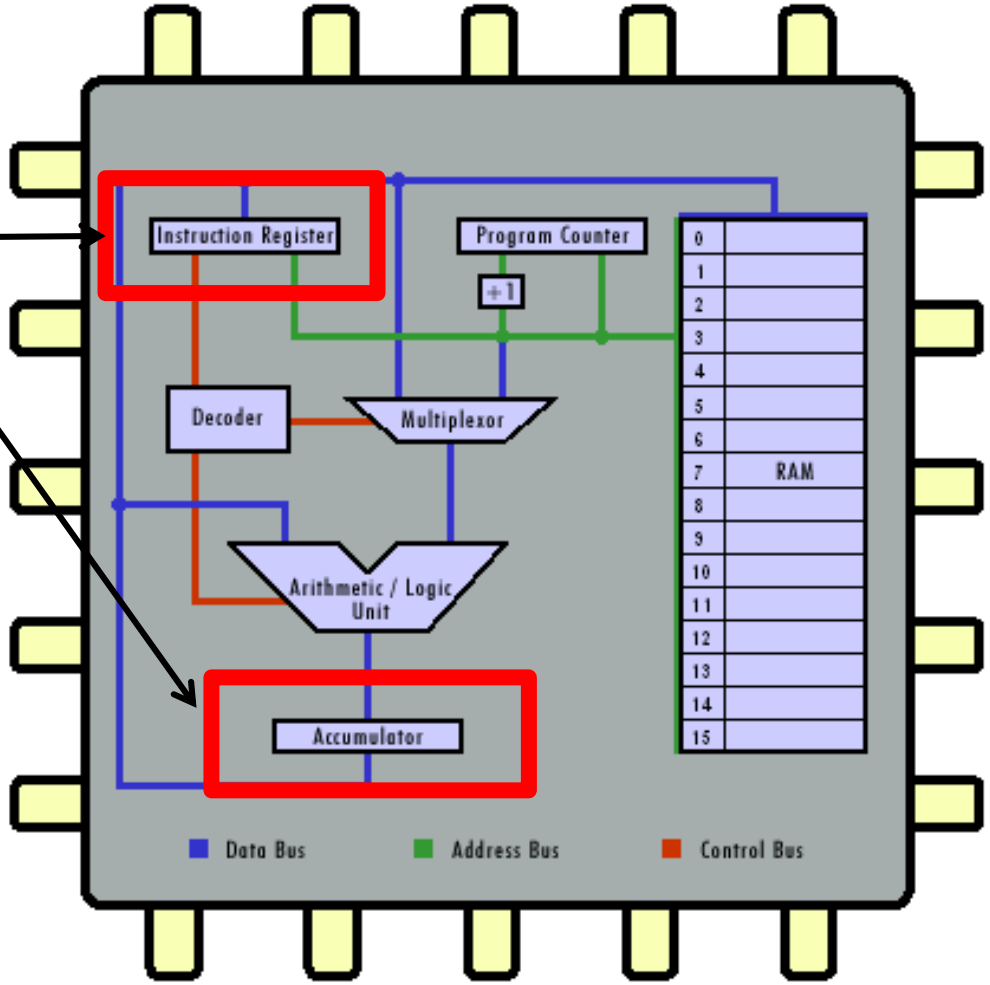
Quando lê as entradas ?
- nas bordas positivas do sinal **CARGA**

Quando zera todos os bits ?
- quando o sinal **ZERAR** passa de 1 para 0

2. Memória – Registradores

CPU – Processador

Registradores



Registradores

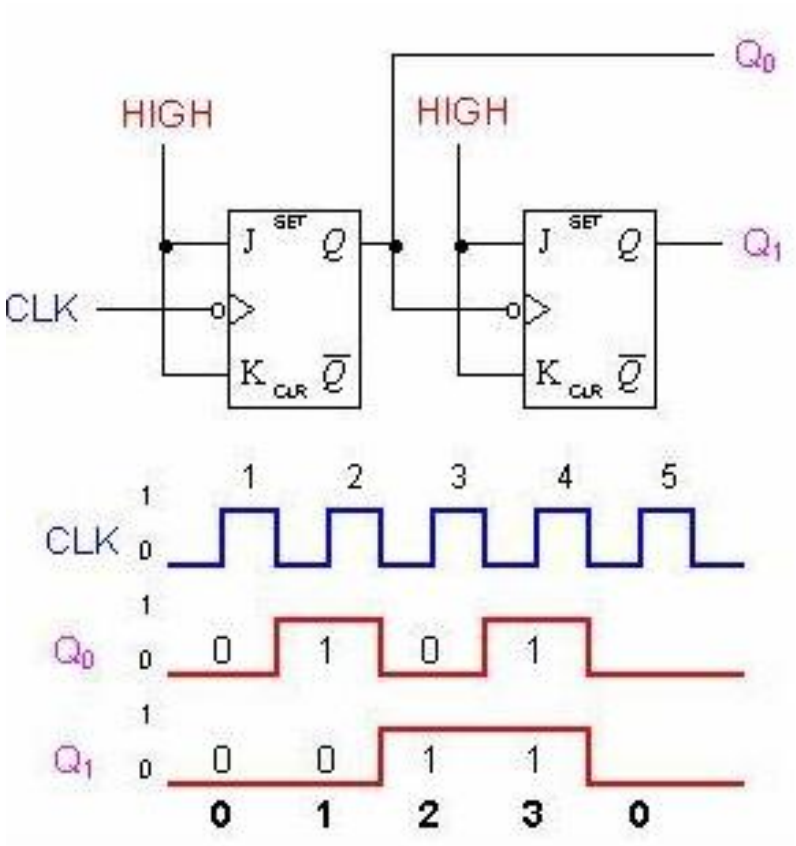
Instruction Register: IR (RI)
Accumulator: Acc (AC)
Status Register - Flags: Flags

Fonte: http://courses.cs.vt.edu/~csonline/MachineArchitecture/Lessons/CPU/index.html

2. Memória – Registradores

Registrador - Contadores

JK master-slave sensíveis à borda de **descida**

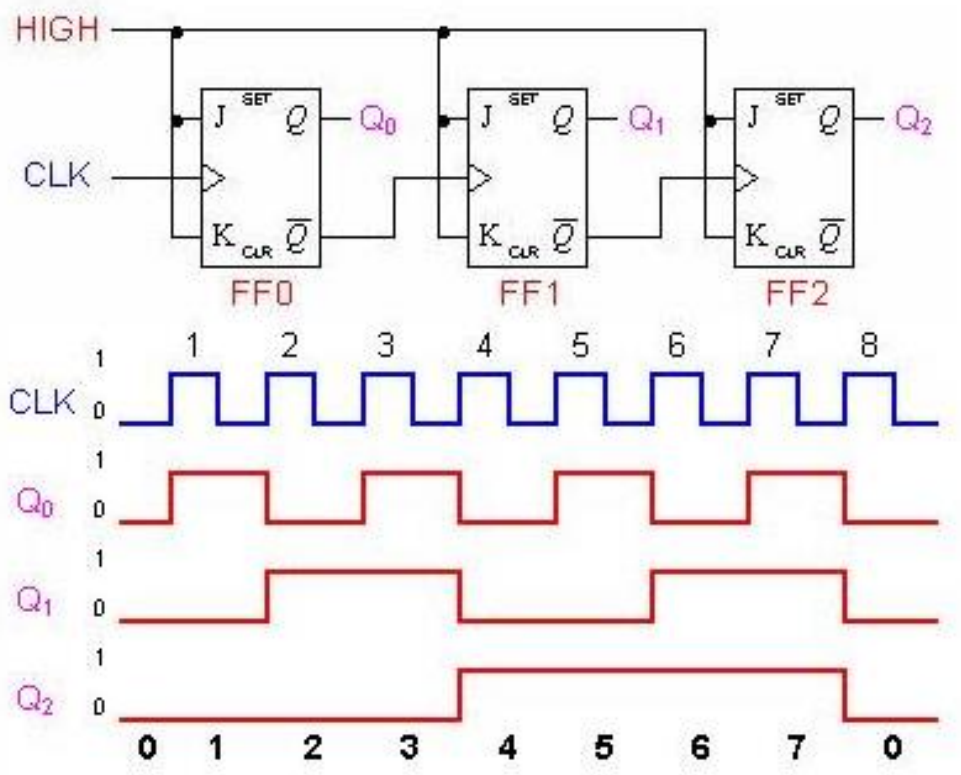


Fonte: http://endigital.orgfree.com/sequencial/sequencial.htm

2. Memória – Registradores

Registrador - Contadores

flip-flops JK master-slave sensíveis à borda de **subida** do controle CLOCK

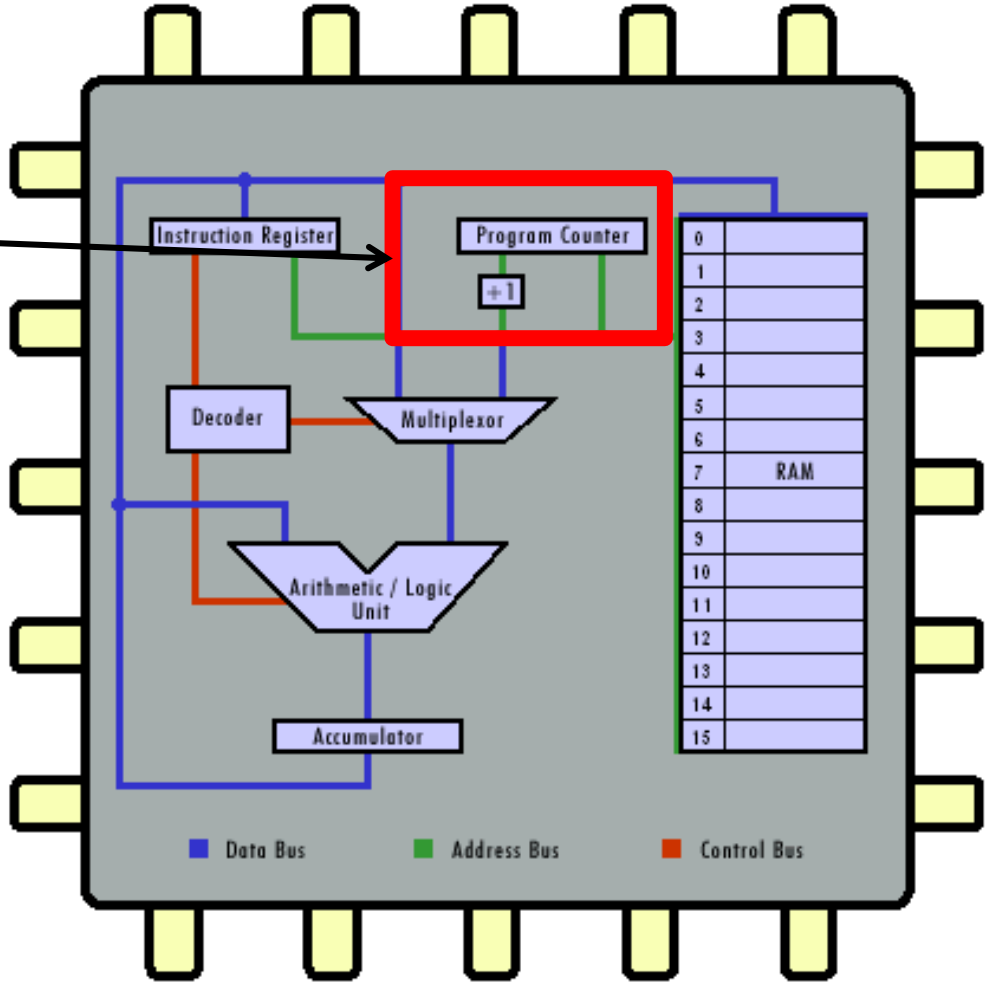


Fonte: http://endigital.orgfree.com/sequencial/sequencial.htm

2. Memória – Registradores

CPU – Processador

Registradores



Registradores

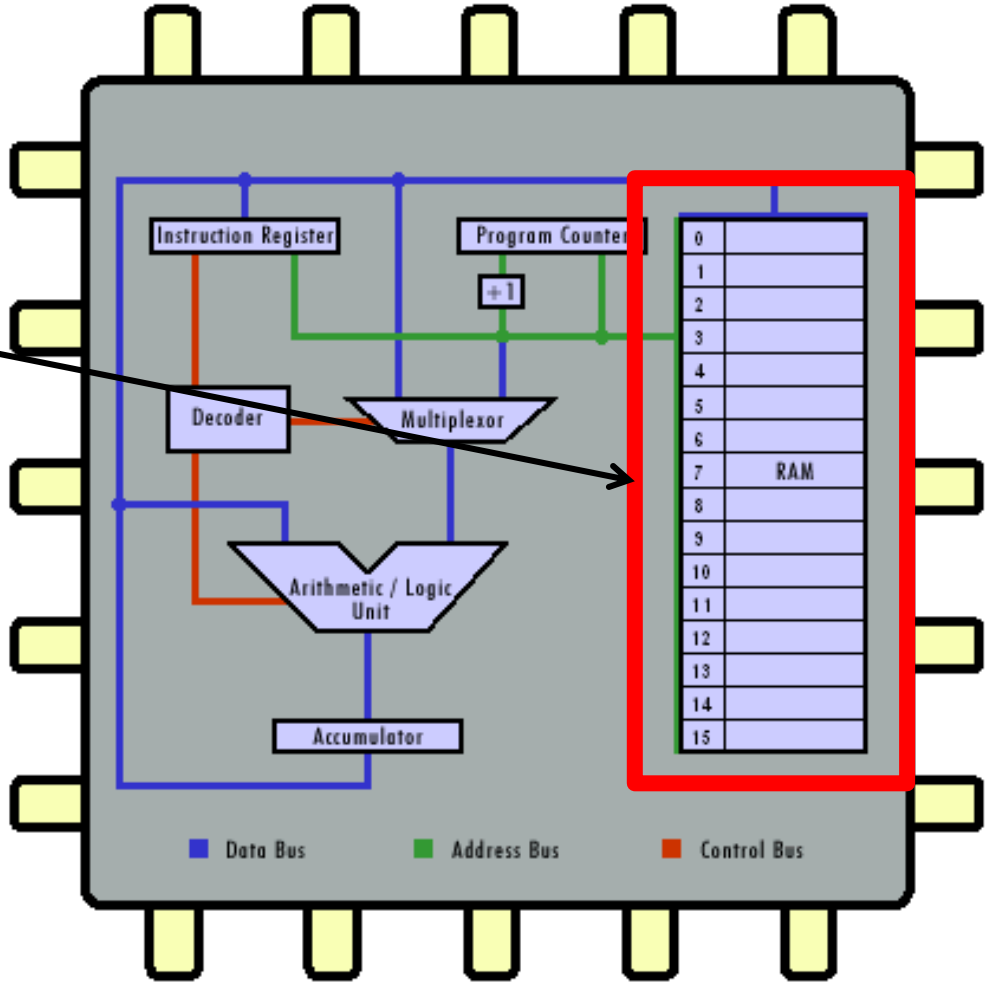
Program Counter: PC

Fonte: http://courses.cs.vt.edu/~csonline/MachineArchitecture/Lessons/CPU/index.html

2. Memória – Registradores

CPU – Processador

Banco de Memória

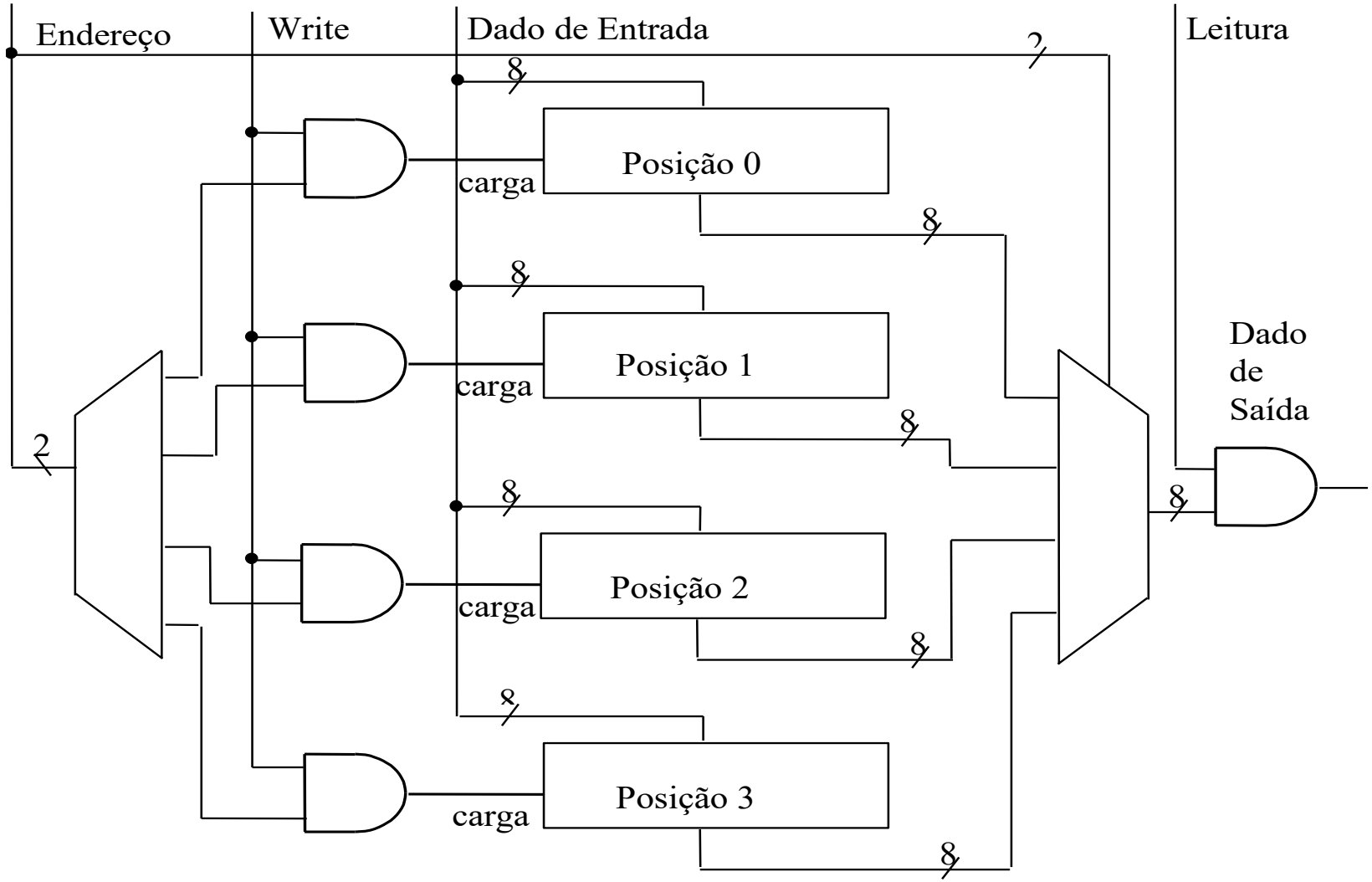


Fonte: http://courses.cs.vt.edu/~csonline/MachineArchitecture/Lessons/CPU/index.html

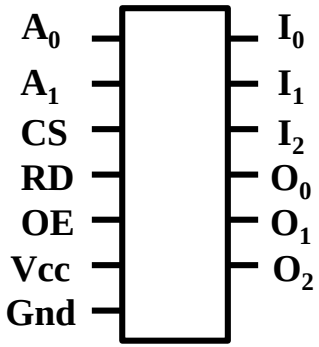
2. Memória – Banco de Memória

Unidade de Memória

Memória com seleção linear



Memória



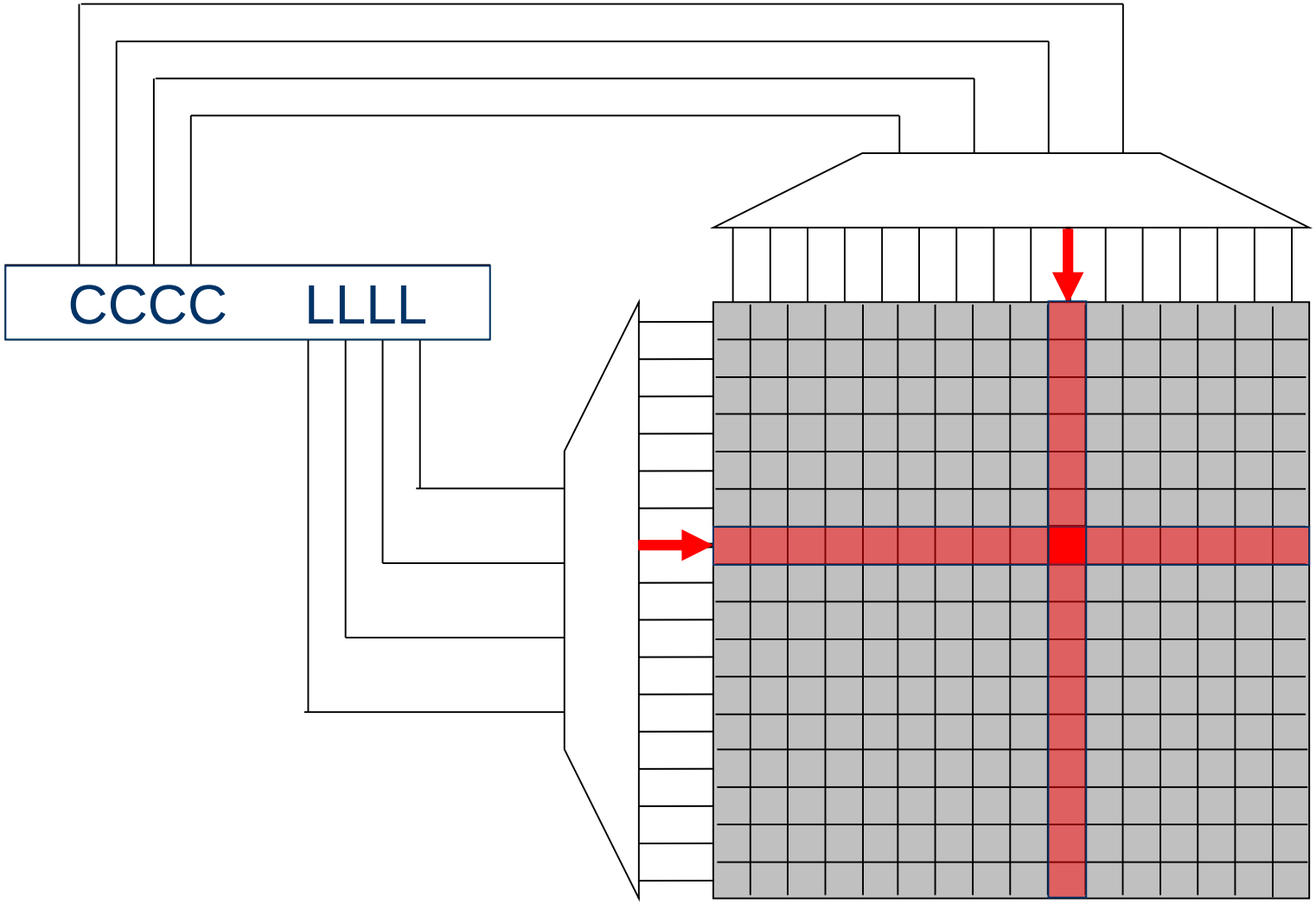
Memória 4 x 3:
4 Endereços de 3 bits cada

Endereços: A_0 .. A_1
Dados (in): I_0 .. I_2
Dados (out): O_0 .. O_2
CS = Chip Select
RD = Read
OE = Output Enable

2. Memória – Banco de Memória

Unidade de Memória

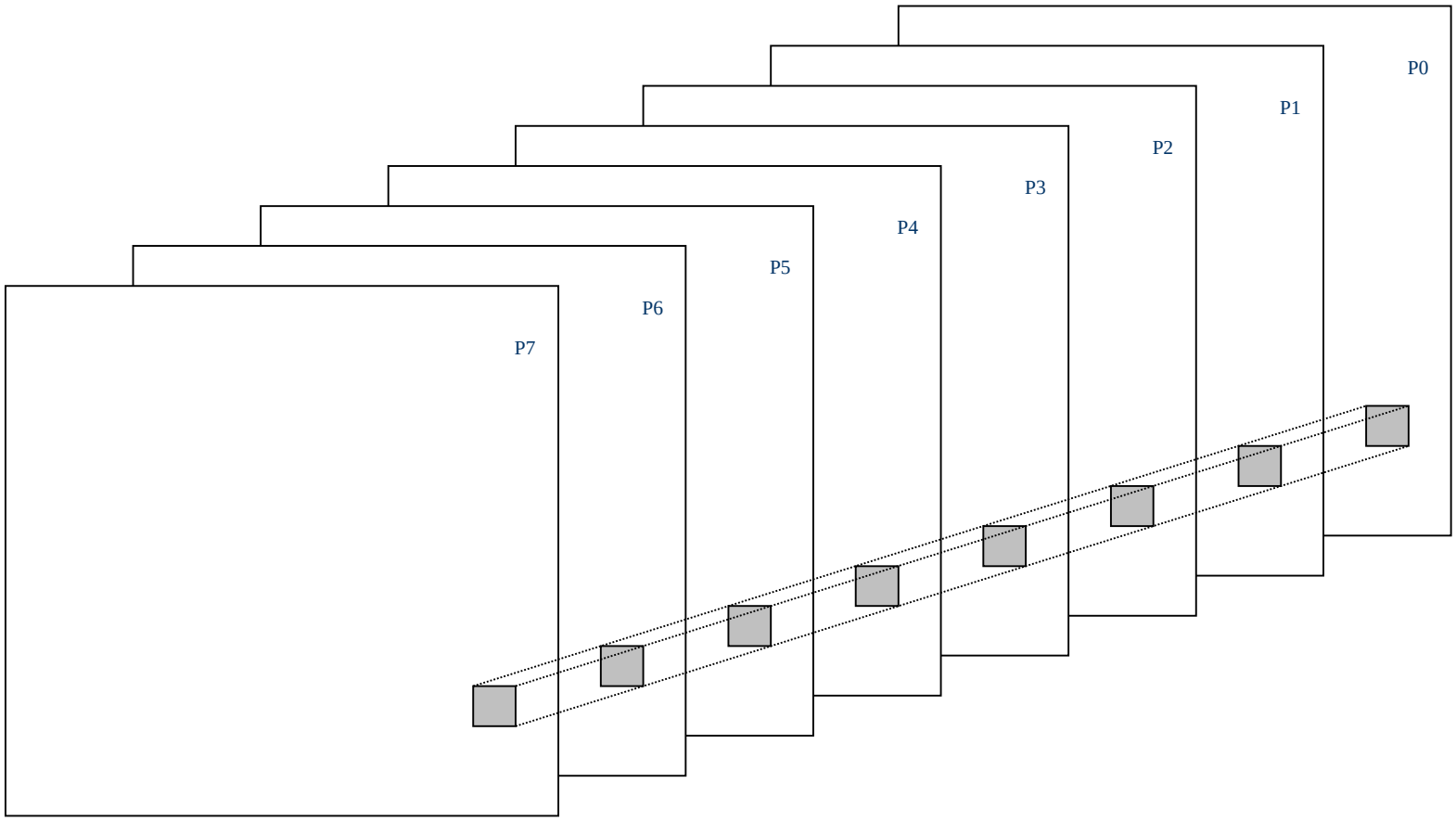
Memória com seleção matricial (um "plano")



2. Memória – Banco de Memória

Unidade de Memória

Memória com seleção de plano
(1 bit em cada "plano")

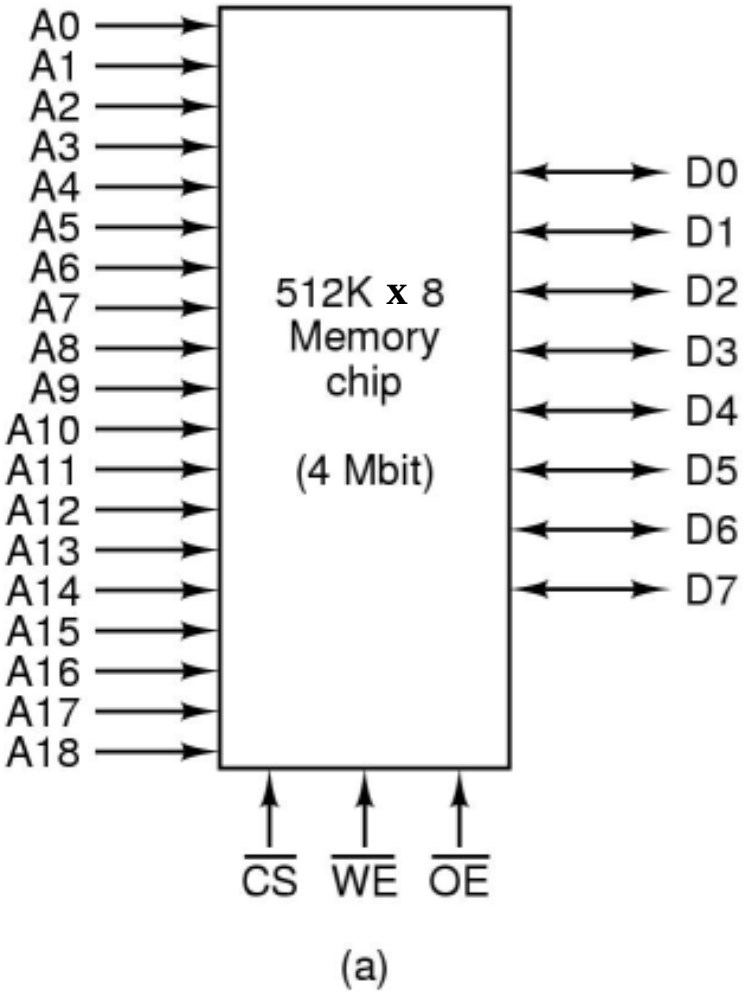


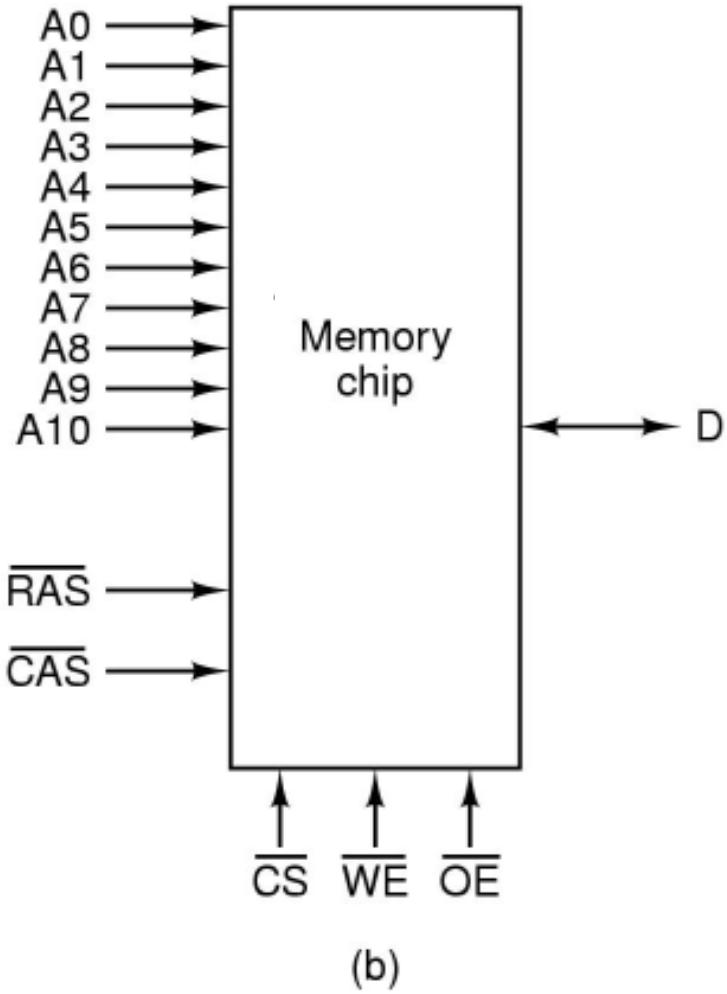
(1 "plano" pode ser 1 circuito integrado de memória "*n*k × 1 bit")

2. Memória – Banco de Memória

Unidade de Memória

Static and Dymanic RAM



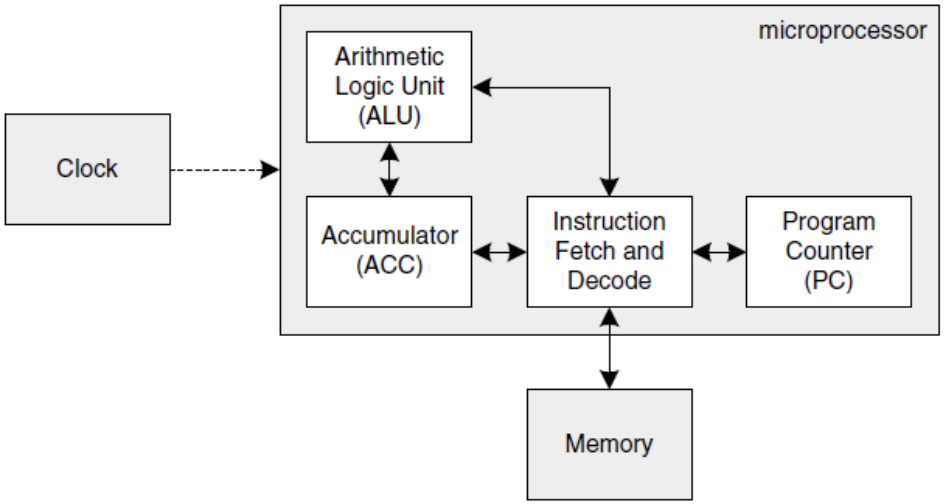


Fonte: http://www.carlosfelgueiras.hpg.com.br/Cursos/ArqComp/aula_5.html

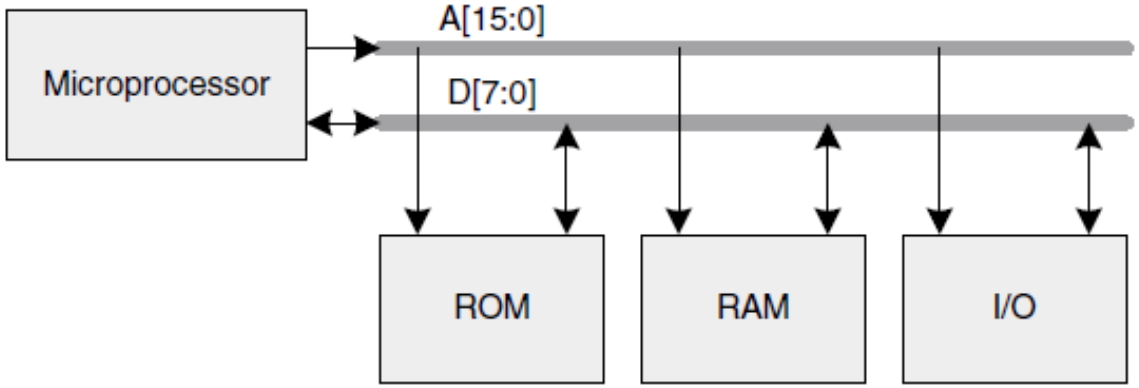
2. Memória, Registradores e E/S

Arquitetura de Computadores

Fonte: Mark Balch - Complete Digital Design



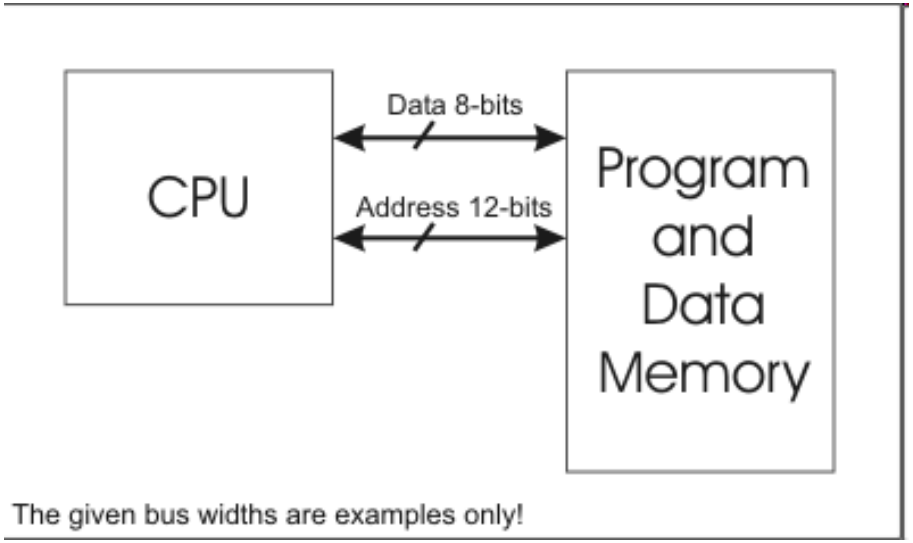
Simple microprocessor



Microprocessor buses

2. Arquitetura de Von Neumann

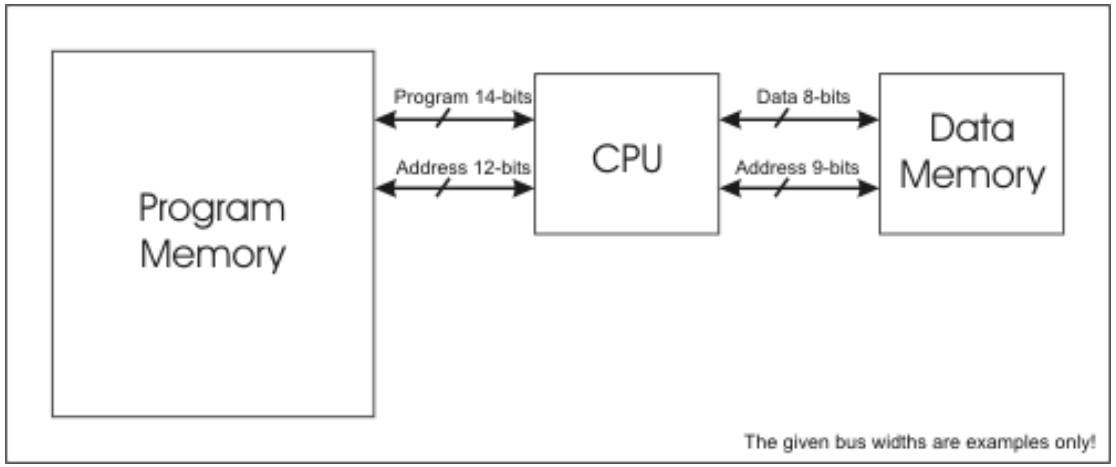
Arquitetura: *Von Neumann x Harvard*



Máquina de Von Neumann

Instruções:
Operador + Operando

IAS
8 bits - Operação (OPcode)
12 bits - Operando (Endereço)



Arquitetura de Harvard

- Separação entre memória de programa e memória de dados

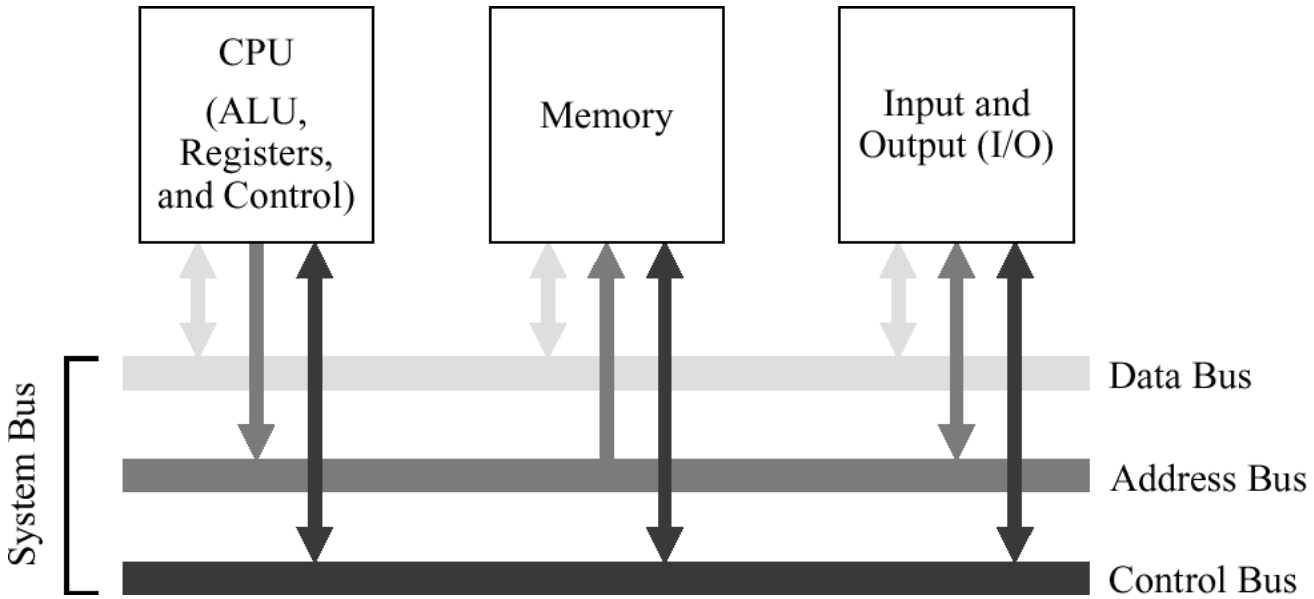
- Busca de instruções e operandos pode ser simultânea (barramentos separados)

Fonte: http://www.elec.canterbury.ac.nz/PublicArea/Staff/hof/p10-embed/p10-tutorial/p13.html

2. Arquitetura de Von Neumann

Arquitetura de Computadores:

Barramentos: Endereços, Dados e Controle

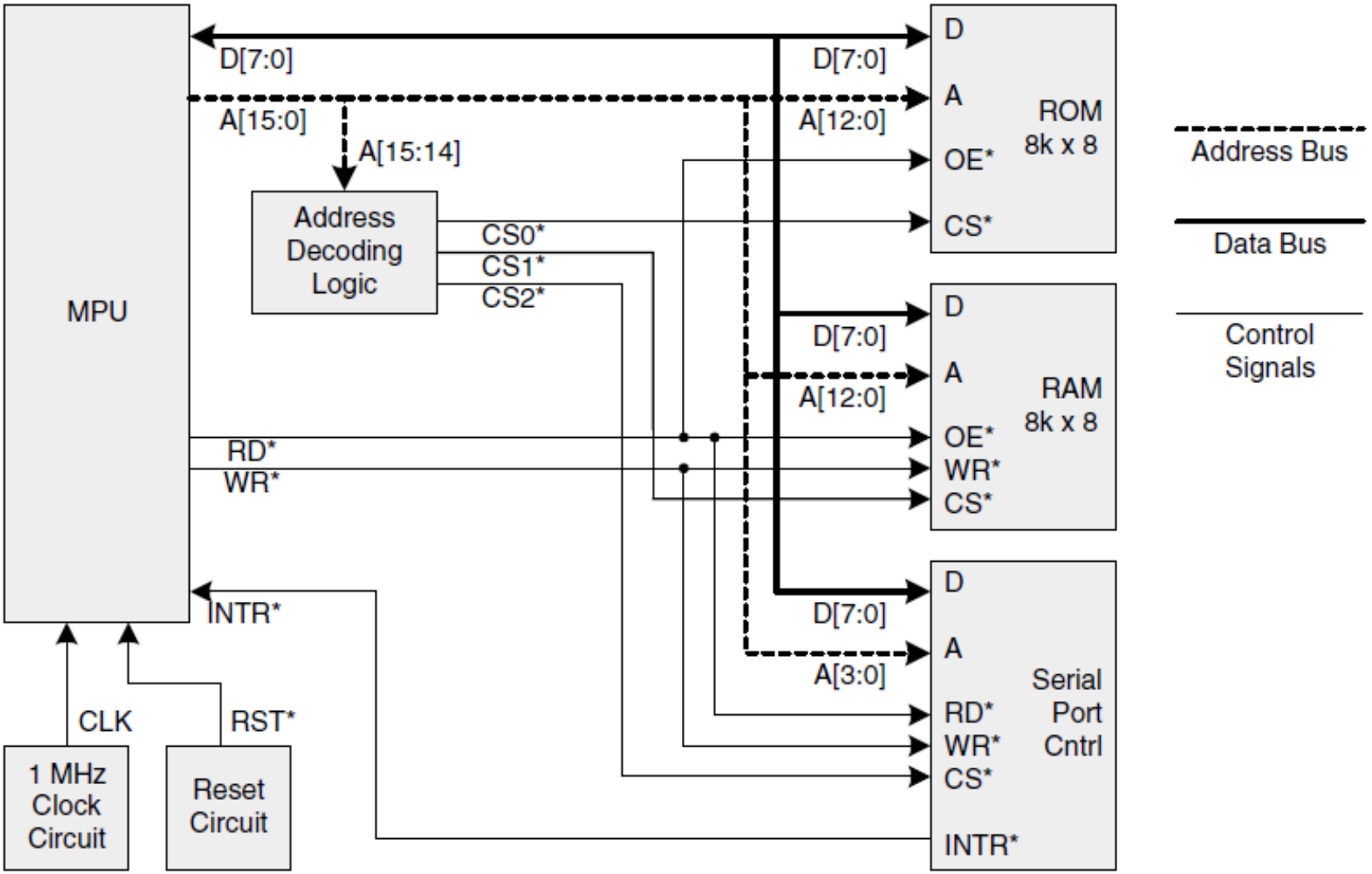


Fonte: http://williamstallings.com/COA6e.html

2. Arquitetura de Von Neumann

Arquitetura de Computadores

Eight-bit computer block diagram



2. Arquitetura de Von Neumann

Unidade de Controle - UC

- Responsável por gerar todos os sinais que controlam as operações no exterior do CPU, e ainda por dar todas as instruções para o correto funcionamento interno do CPU [UC é o "Maestro da Orquestra"];

- Junto a Unidade de Controle temos um decodificador de instruções, que analisa e decodifica o Operador da Instrução (OPcode);

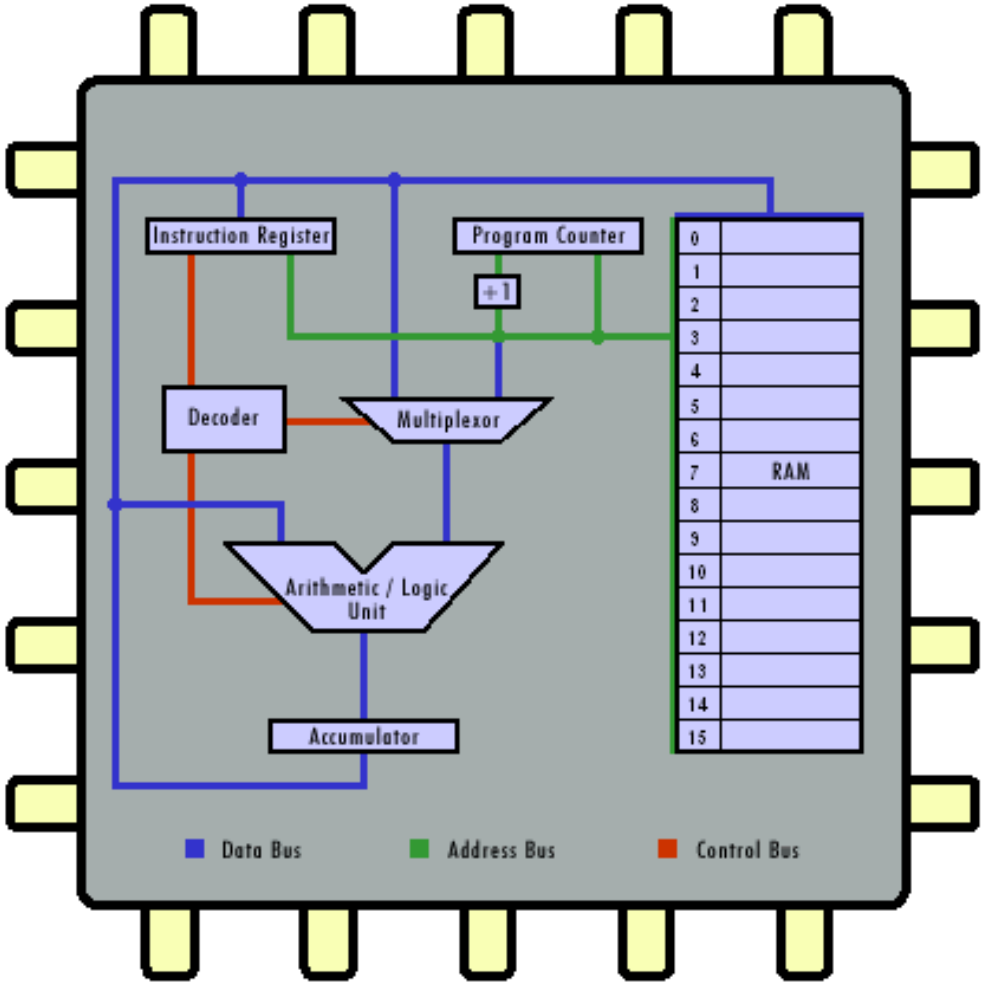
- A unidade de controle executa três ações básicas intrínsecas e pré-programadas pelo próprio fabricante do processador, são elas:
  - (i) busca (fetch)
  - (ii) decodificação
  - (iii) execução

- Assim sendo, todo processador, ao iniciar sua operação, realiza uma operação cíclica, tendo como base essas três ações. A unidade de controle usualmente é fixa, onde esta define o Conjunto de Instruções do Processador: CPU *Instruction Set*

2. Arquitetura de Von Neumann

Unidade de Controle - UC

Show time...



Fonte: http://courses.cs.vt.edu/~csonline/MachineArchitecture/Lessons/CPU/index.html

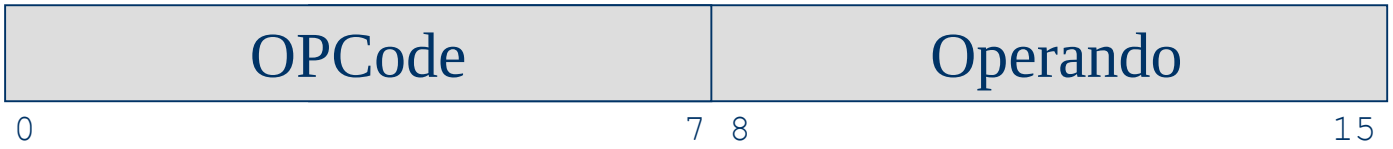
2. Arquitetura de Von Neumann

Unidade de Controle - UC

CPU Instruction Set

Código de Instruções

Operador da Instrução + Operando(s)



Exemplo: Instrução de 16 Bits

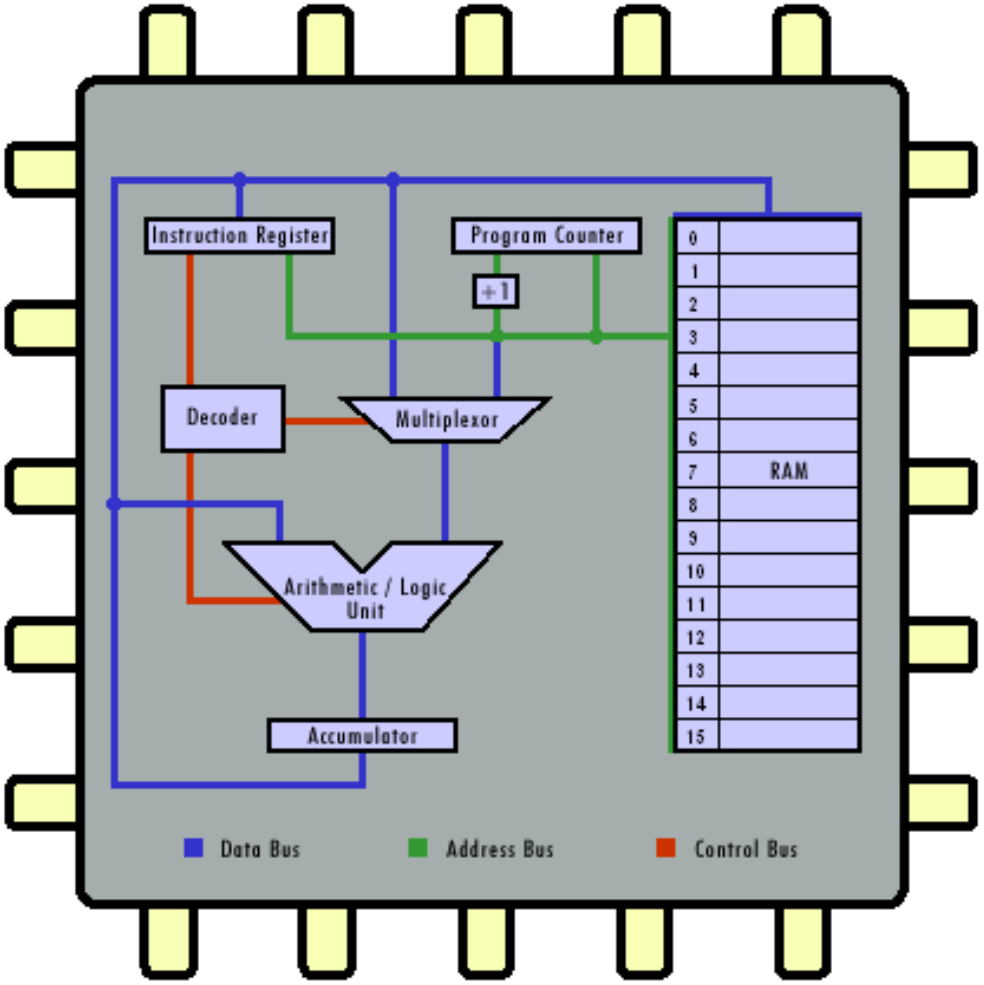
Tipos de Instruções...
Arquiteturas de 4, 3, 2, 1 e 0 endereços

Tipos de Instruções... Conjunto de Instruções Microprogramado
Tipos de Instruções... RISC, CISC, VLIW
Tipos de Instruções... Modo de Endereçamento
Tipos de Instruções... Instruções de Controle, Privilegiadas, etc.

Fonte: ftp://ftp.inf.ufrgs.br/pub/inf107/ (Arquiteturas de 0,1,2,3,4 endereços)

1. Arquitetura de Von Neumann

Unidade de Controle - UC



Elementos importantes:

PC - Program Counter
AC - Accumulator
IR - Instruction Register

Address Bus: *n* bits
Data Bus : *m* bits

Flags da ULA (S - Status)
Z - Zero C - Carry
N - Negative V - Overflow

Memória: RAM / ROM
System/User Program, Data, Stack (Pilha), I/O, Interrupts

Fonte: http://courses.cs.vt.edu/~csonline/MachineArchitecture/Lessons/CPU/index.html

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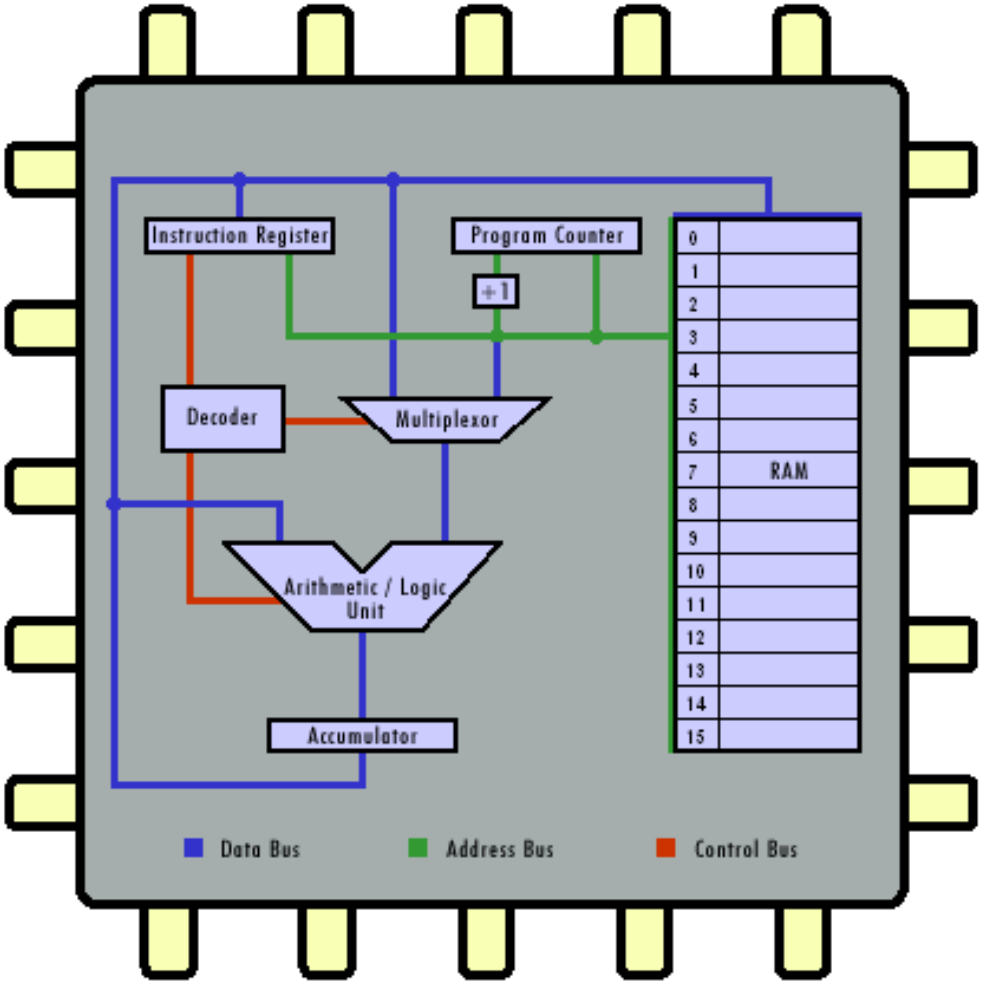


µProc - Elementos

PC - Program Counter
AC - Accumulator
IR - Instruction Register
SP - Stack Pointer
Ix - Index Register
BR - Base Registers

Address Bus: *n* bits
Data Bus : *m* bits

Flags da ULA (S - Status)
Z - Zero C - Carry
N - Negative V - Overflow
P - Parity I - Interrupt

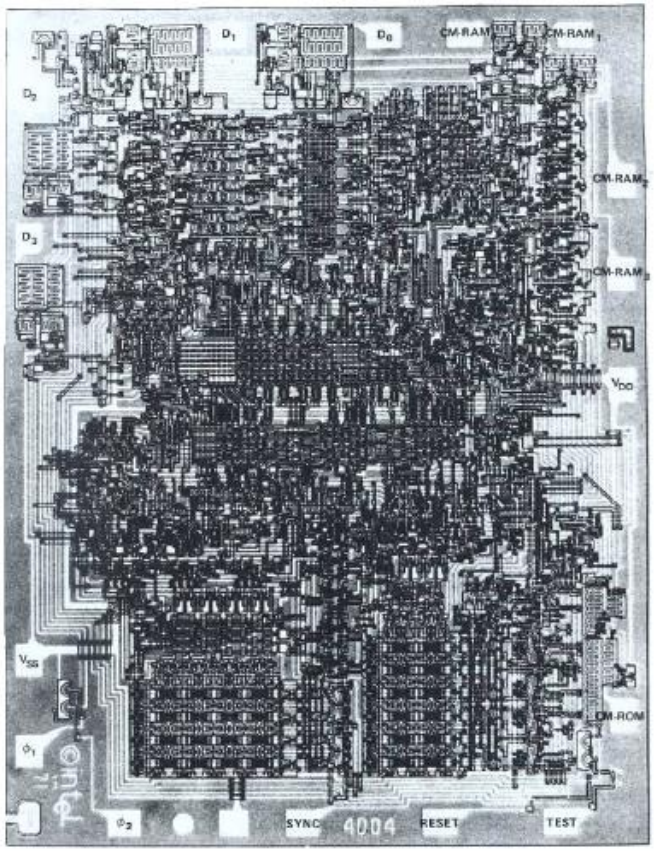
Fonte: http://courses.cs.vt.edu/~csonline/MachineArchitecture/Lessons/CPU/index.html

3. Arquitetura de Microprocessadores - Intel 4004

Intel 4004 (1971)

MCS-4™
FOUR-BIT PARALLEL MICROCOMPUTER SET

16-pin DIP package
P-channel Silicon Gate MOS
Minimum system: CPU and one ROM
4-bit parallel CPU with 45 instructions



Features

- Microprogrammable General Purpose Computer Set
- 4-Bit Parallel CPU With 46 Instructions
- Instruction Set Includes Conditional Branching, Jump to Subroutine and Indirect Fetching
- Binary and Decimal Arithmetic Modes
- Addition of Two 8-Digit Numbers in 850 Microseconds
- 2-Phase Dynamic Operation
- 10.8 Microsecond Instruction Cycle
- CPU Directly Compatible With MCS-4 ROMs and RAMs
- Easy Expansion — One CPU can Directly Drive up to 32,768 Bits of ROM and up to 5120 Bits of RAM
- Unlimited Number of Output Lines
- Packaged in 16-Pin Dual In-Line Configuration
- Directly Compatible With 4004 CPU
- Interface 1702A PROMs Directly to 4004 CPU -- Completely Eliminates TTL Interface
- Permits Program Storage in Alterable Memory
- Execute MCS-4 Programs from any Mix of Standard Intel PROMs, ROMs and RAMs
- Expanded I/O Port Capability
- Each Port May be Both Input and Output -- Up to 16 4-bit Input Ports and 16 4-bit Output Ports
- I/O Ports and Control Lines are TTL Compatible
- Number of I/O Ports is Independent of the Size of the Program Memory
- New Instruction WPM (Write Program Memory) is Used for Loading Alterable Program Storage (RAM)

3. Arquitetura de Microprocessadores - Intel 4004

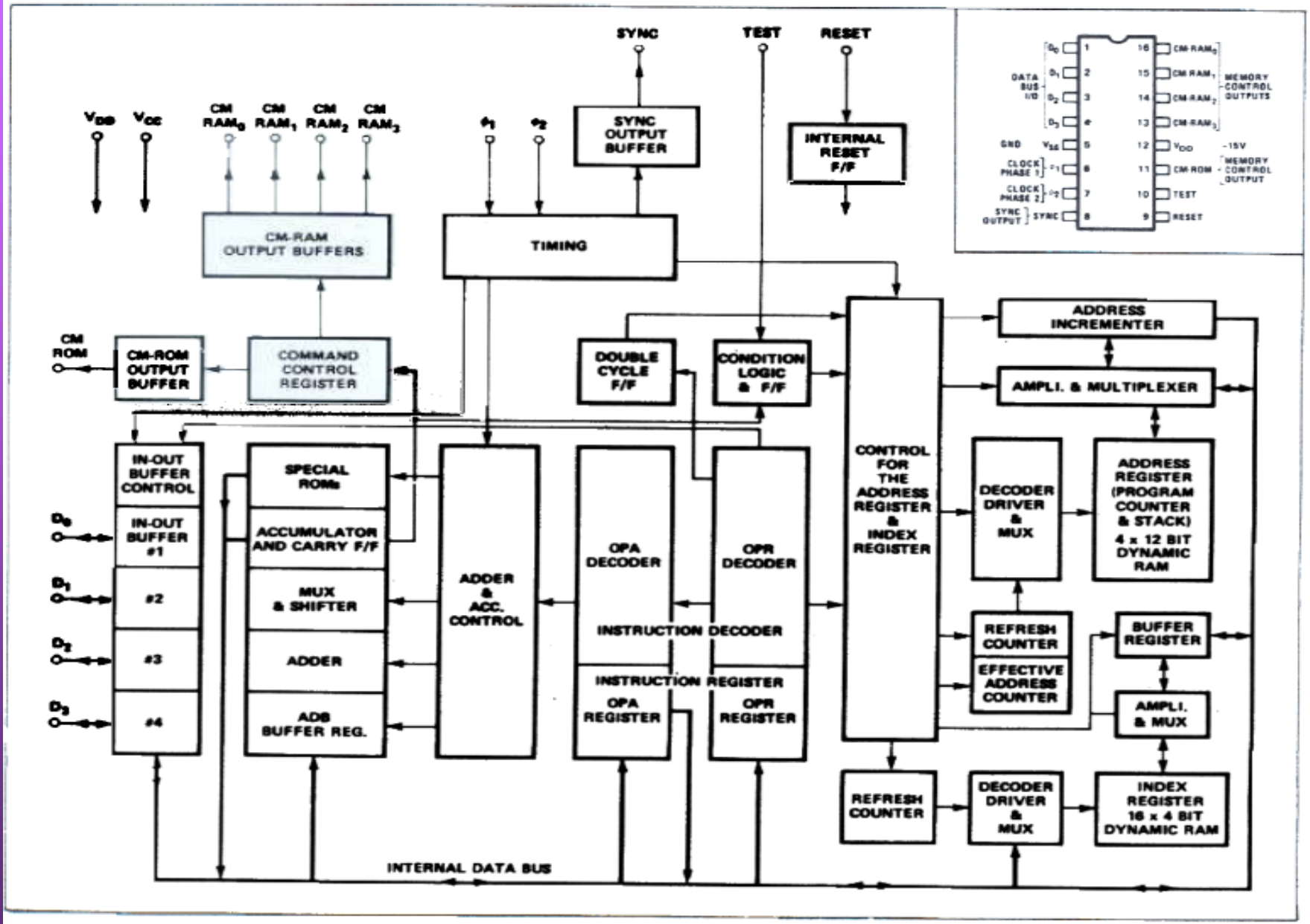
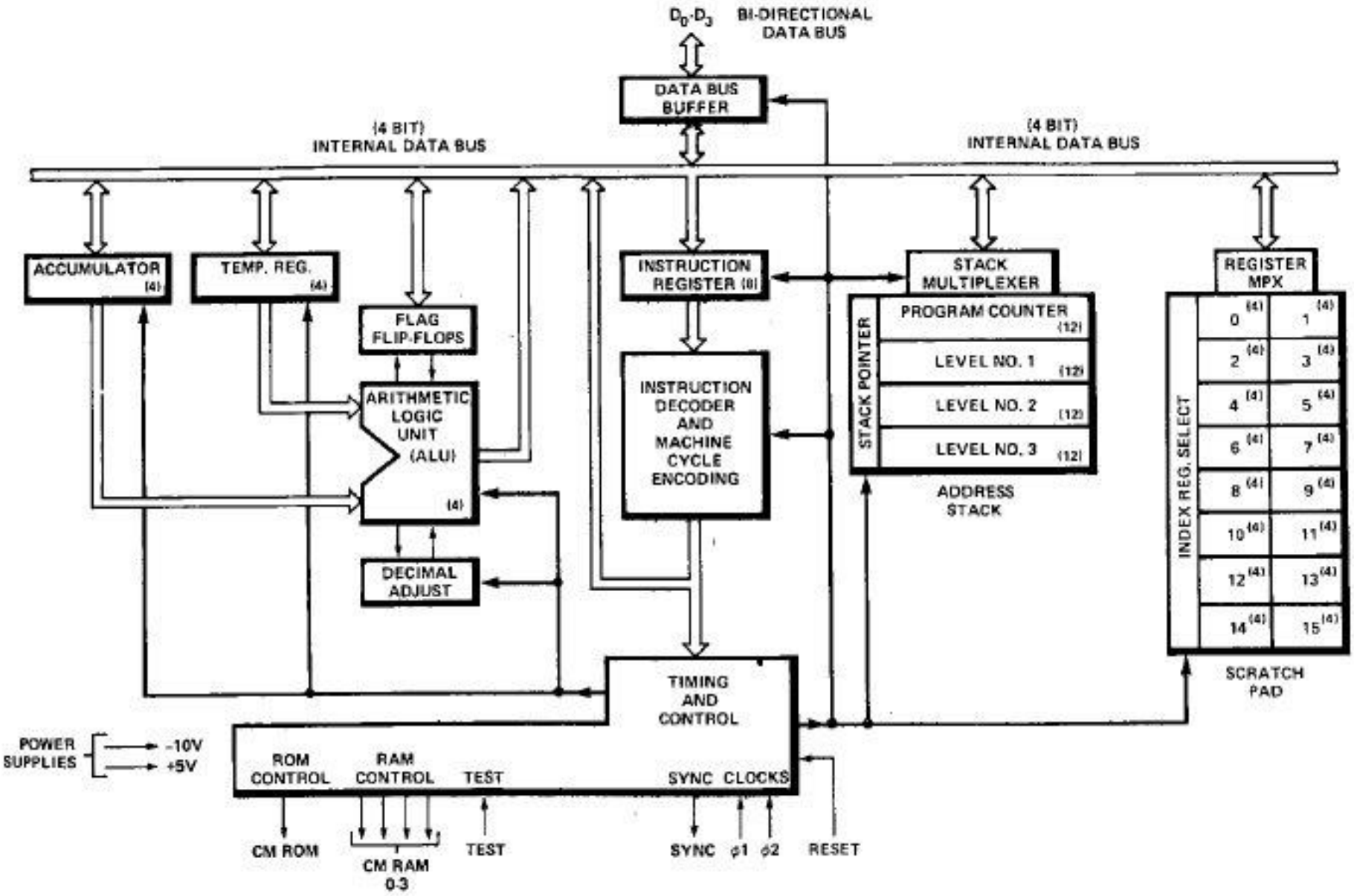
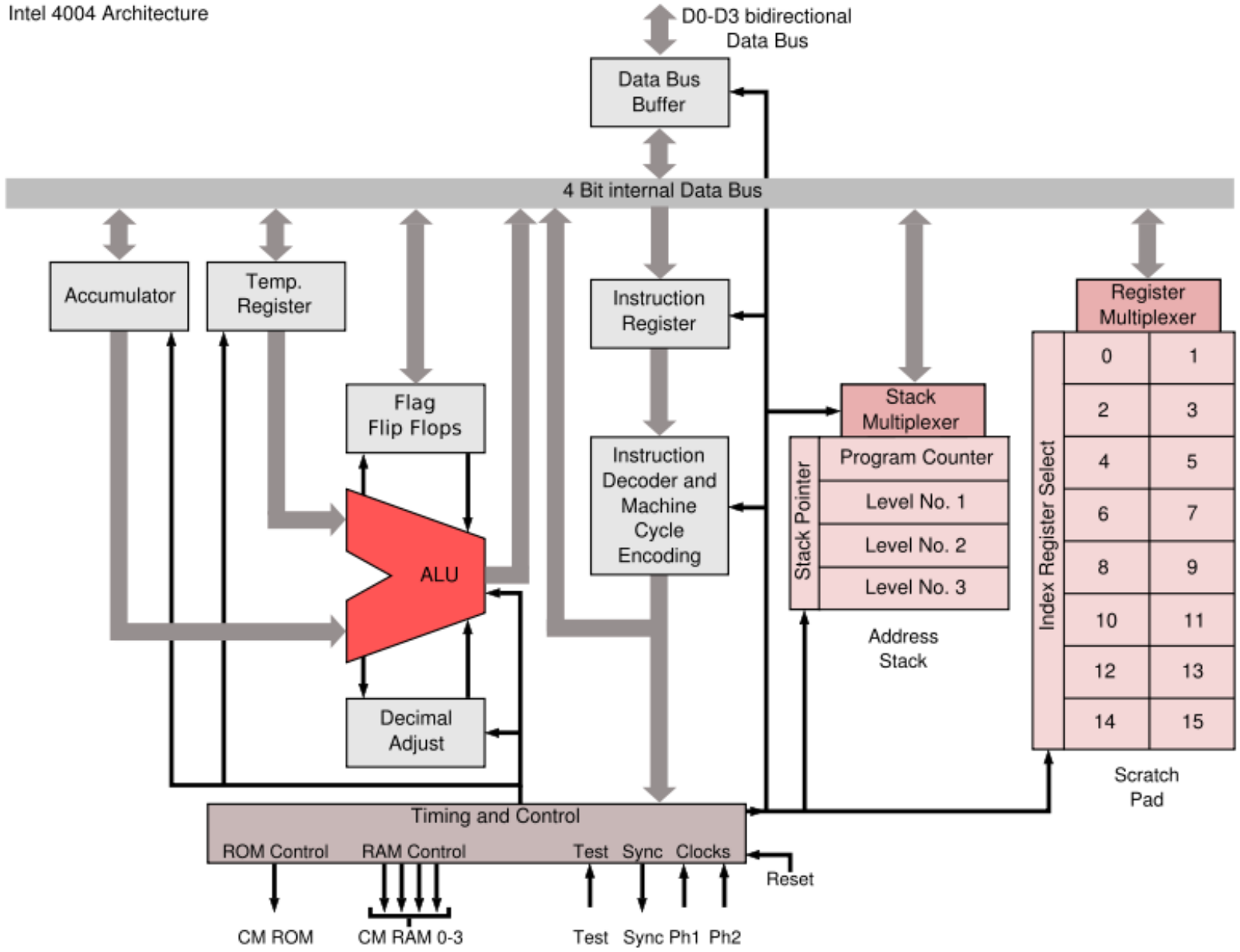


Figure 3. 4004 CPU Block Diagram

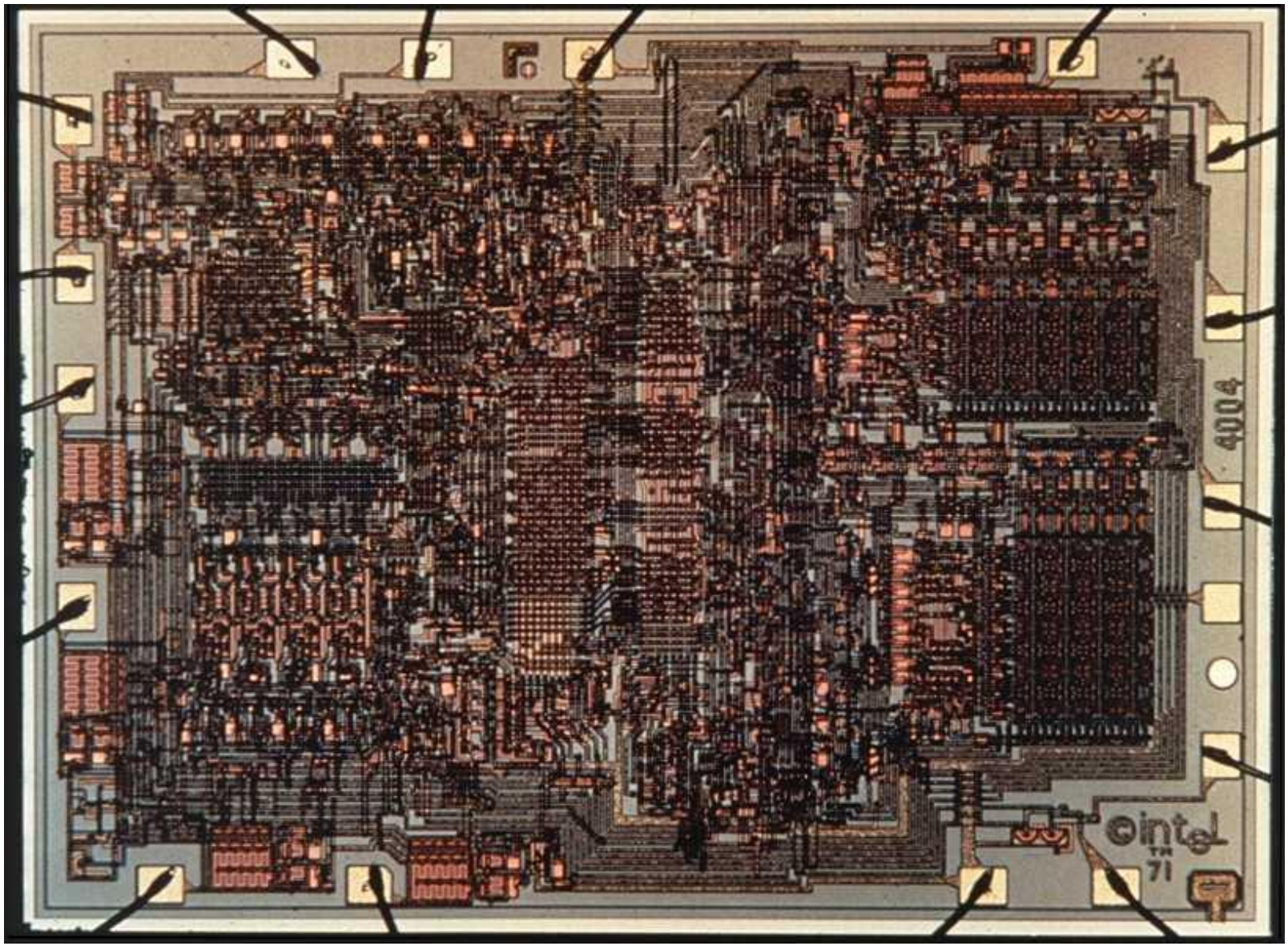
3. Arquitetura de Microprocessadores - Intel 4004



3. Arquitetura de Microprocessadores - Intel 4004



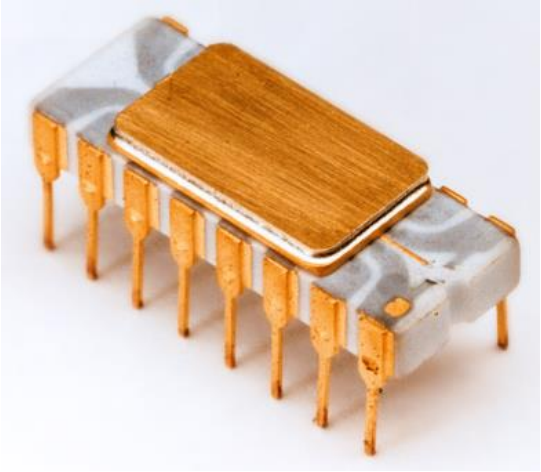
3. Arquitetura de Microprocessadores - Intel 4004

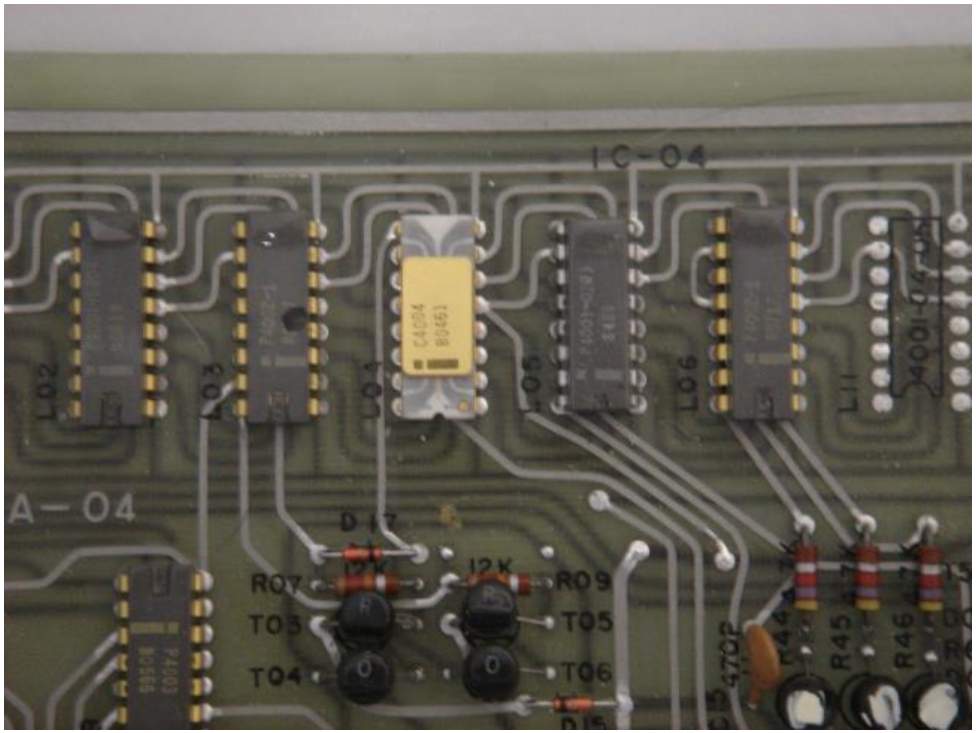


3. Arquitetura de Microprocessadores - Intel 4004

Intel 4004

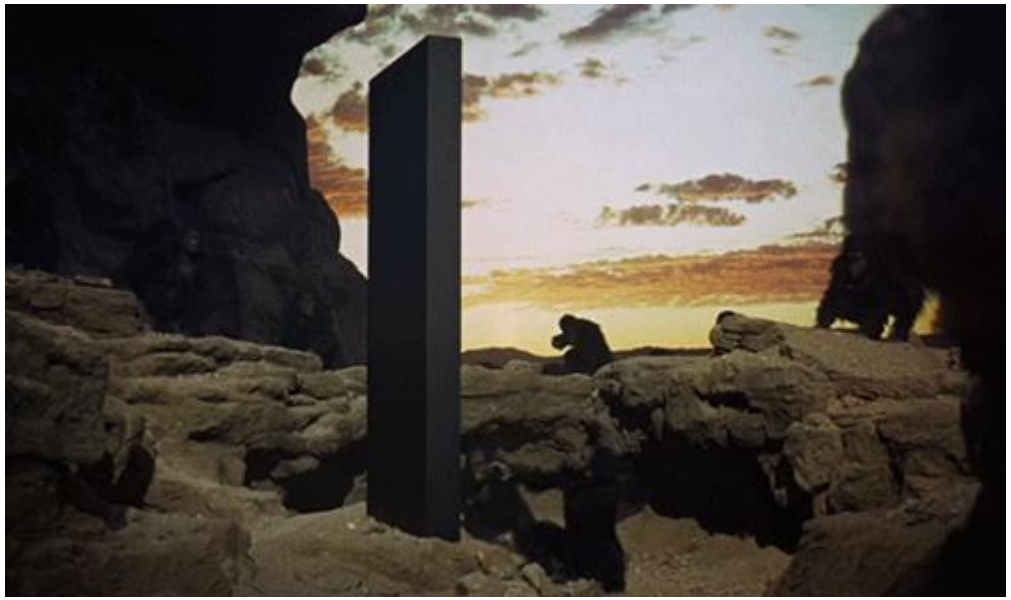
Busicom - Nippon Calculating Machine Corp changed its name to Business Computer Corporation, was a Japanese company that owned the rights to the first microprocessor but sold them back to Intel. They made electronic calculators and the first using the new Intel 4004 processor was the Busicom 141-PF[1]





4. Arquiteturas Didáticas

Começando do Começo...



4. Arquiteturas Didáticas

Neander - Computador Hipotético [Weber 2001*]

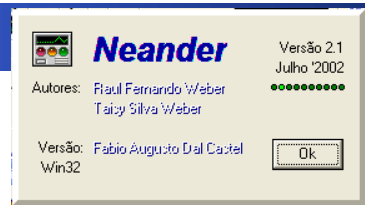
Arquitetura: características gerais

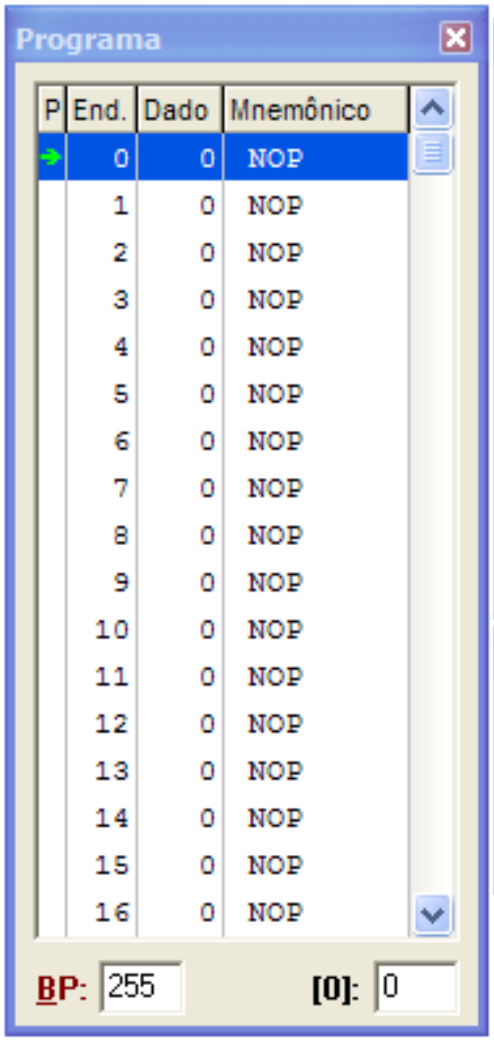
- Largura de dados e endereços de 8 bits (bus)
- Dados representados em complemento de 2
- Acumulador de 8 bits (AC - Accumulator)
- Apontador de programa de 8 bits (PC - Program Counter)
- Registrador de Instruções de 8 bits (IR - Instruction Reg.)
- Registrador de estado (flags) com 2 códigos de condição: Negativo (N) e Zero (Z)
- Endereçamento de memória total de 256 bytes

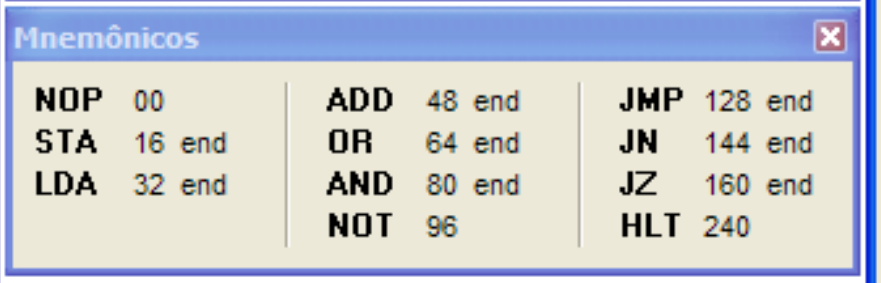
* ftp://ftp.inf.ufrgs.br/pub/inf107/

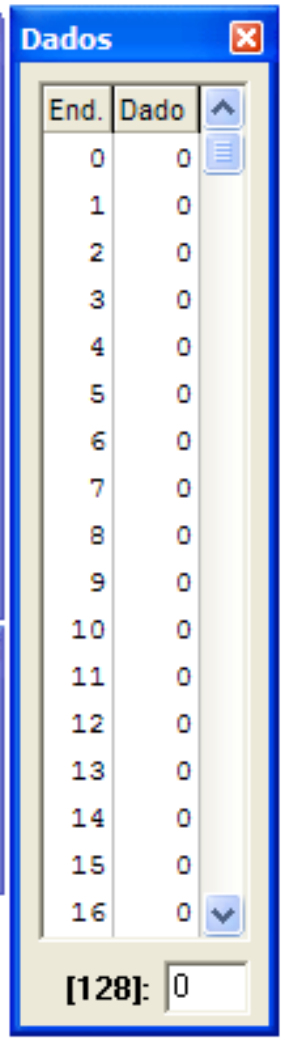
4. Arquiteturas Didáticas

Neander => Simulador WNeander









Simuladores Didáticos
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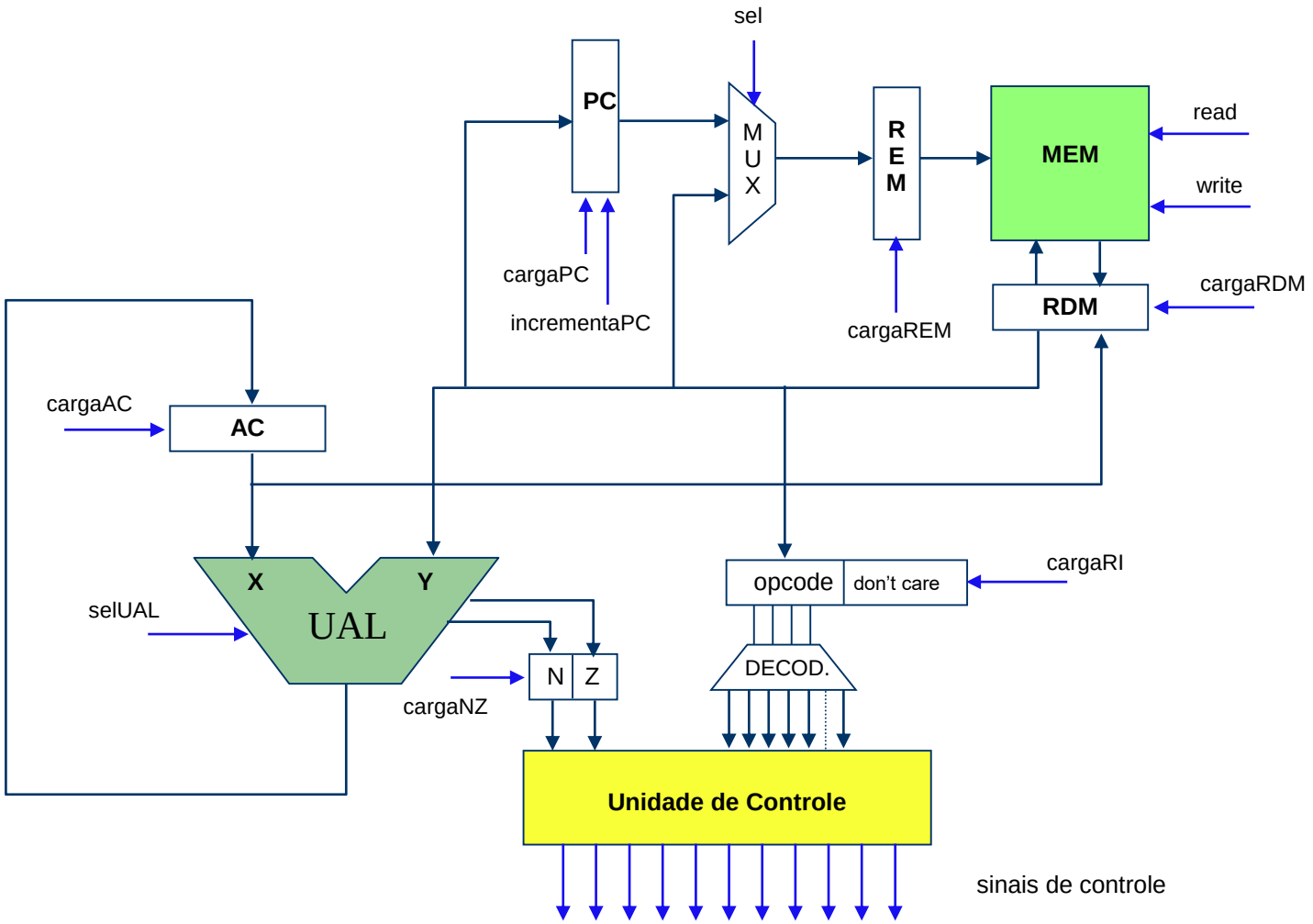

* ftp://ftp.inf.ufrgs.br/pub/inf107

Versão Web: http://inf.ufrgs.br/~vbuaraujo/sw/neander/

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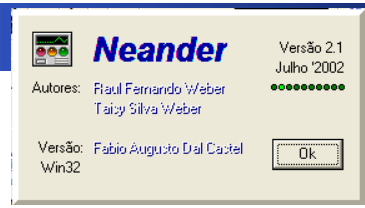

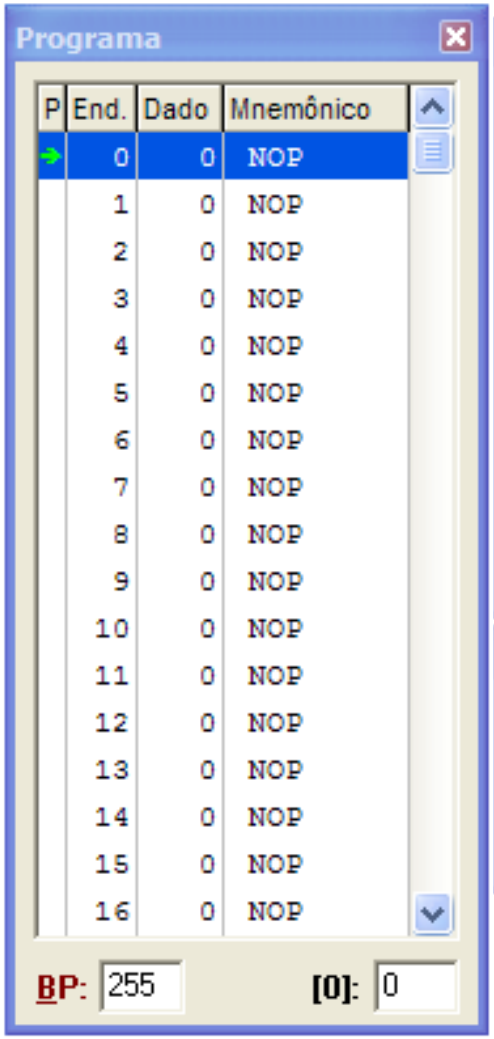

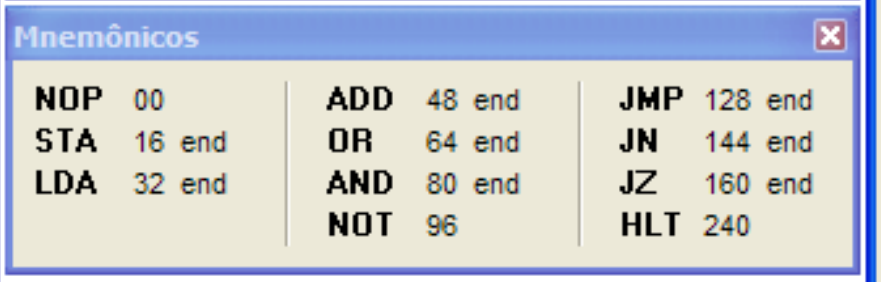

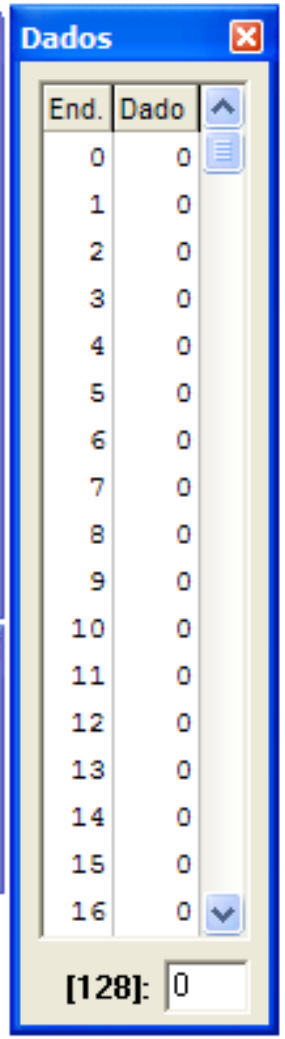

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4. Arquiteturas Didáticas

Evolução do Neander... Ahmes, Ramses, Cesar

Quadro comparativo

Arquitetura	Endereços	Dados	Nro. Instruções	Registradores
NEANDER	8 bits 256 bytes	8 bits Compl.2	11 instruções (OpCode: 4bits)	AC, PC, IR, Flags (N,Z) REM, RDM
AHMES	8 bits	8 bits	24 instruções (Neander ext.)	PC, IR, REM, RDM Flags (N, Z, C, B, V)
RAMSES	8 bits	8 bits	Modos de End. 4 modos x 16 instr.	PC, IR, RA, RB, RX Flags (N, Z, V, C)
CESAR	16 bits 64 Kbytes	16 bits	Inúmeras	R0 a R6 (uso geral) R7 (PC)

Simuladores Didáticos
ftp://ftp.inf.ufrgs.br/pub/inf107/
ftp://ftp.inf.ufrgs.br/pub/inf108/
http://pt.wikipedia.org/wiki/Máquinas_hipotéticas_da_Universidade_Federal_do_Rio_Grande_do_Sul

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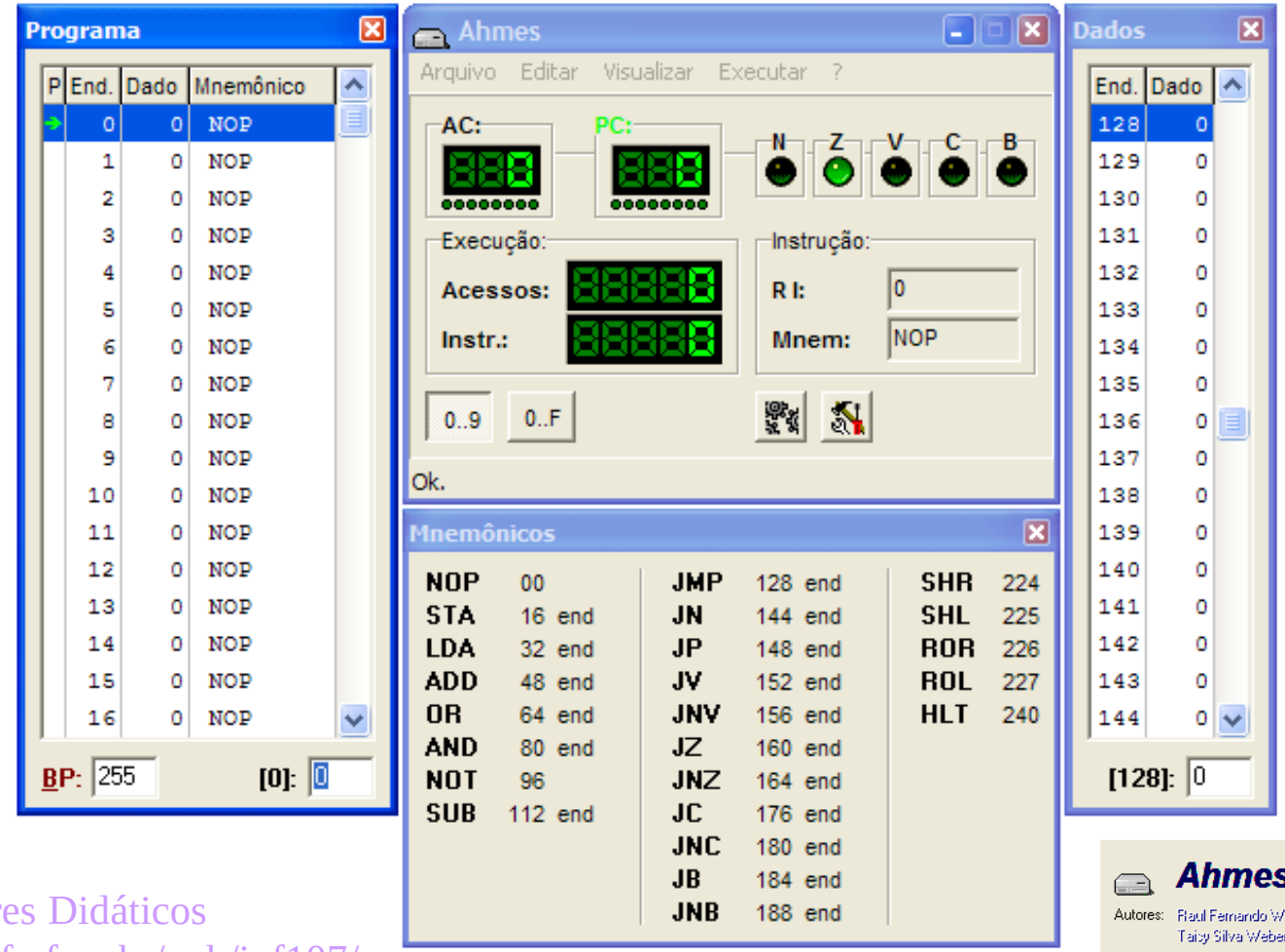

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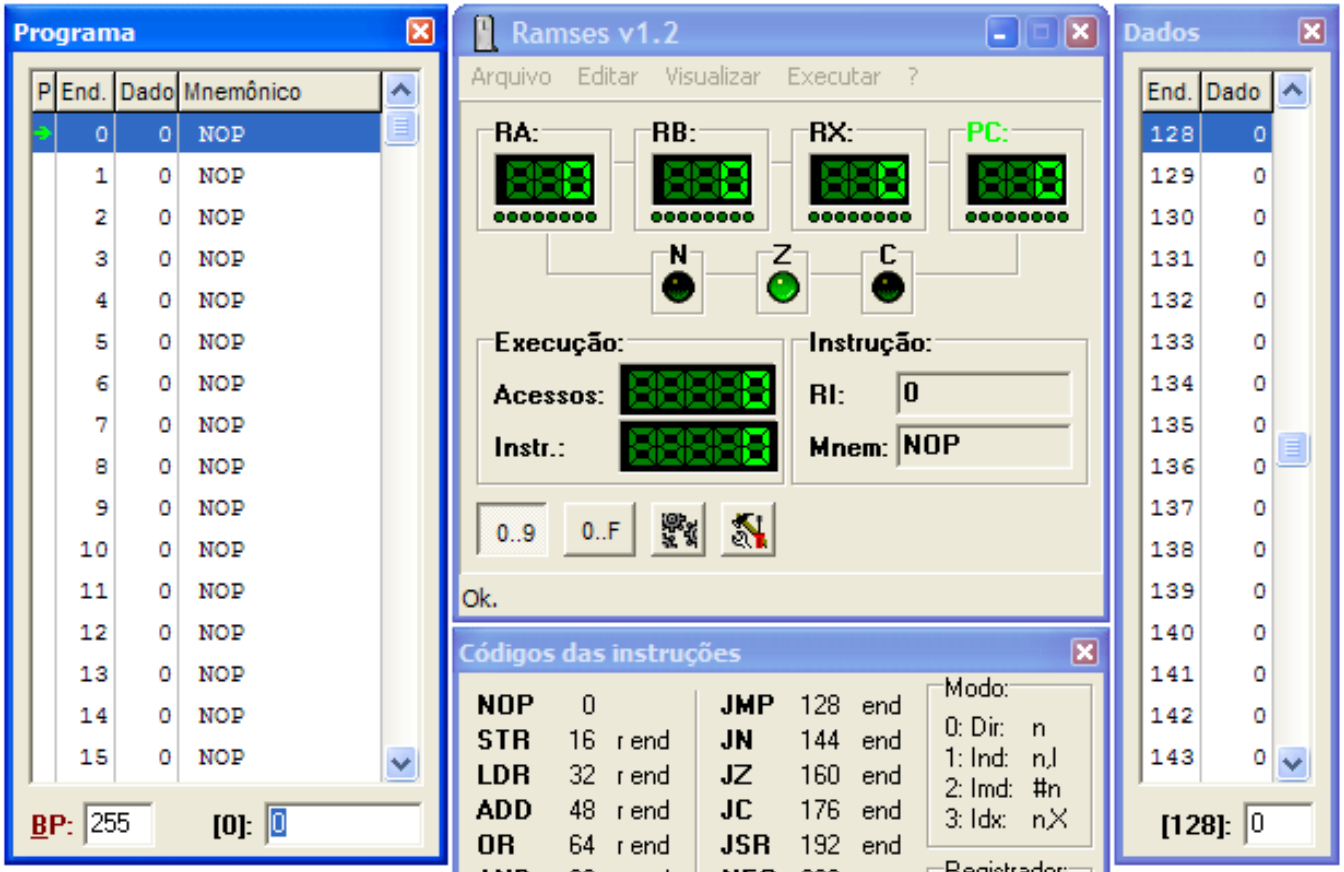

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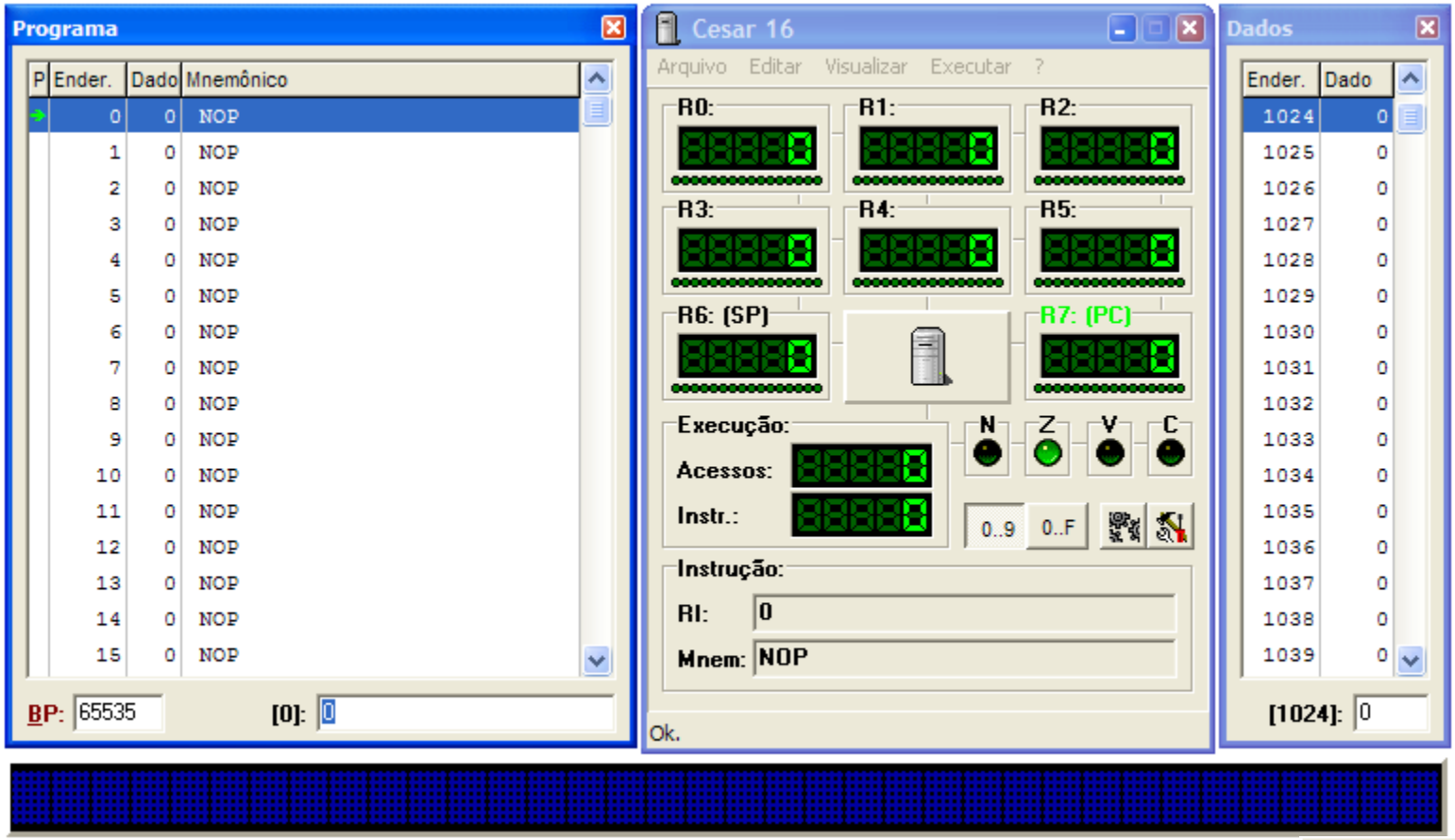

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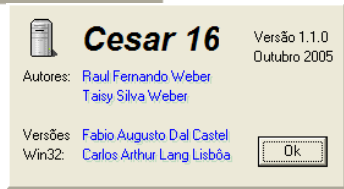

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INFORMAÇÕES SOBRE A DISCIPLINA

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ICMC - Instituto de Ciências Matemáticas e de Computação
SSC - Departamento de Sistemas de Computação

Prof. Fernando Santos OSÓRIO
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