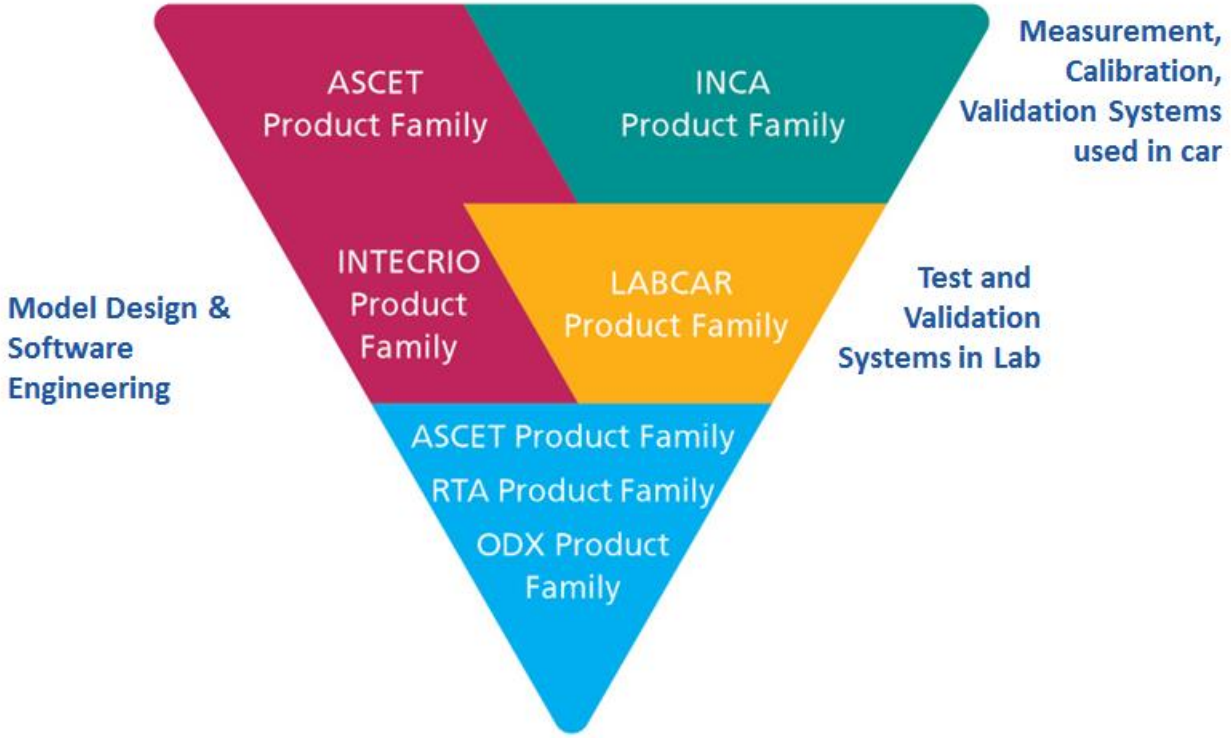
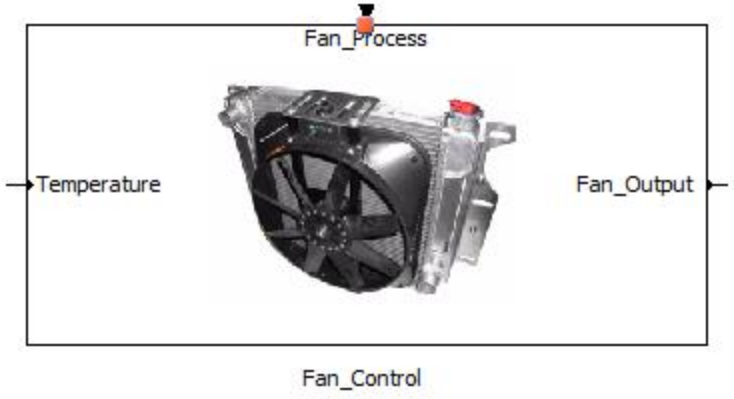
# V-Cycle

Pedro C. Rossetti

# V-Cycle



# V-Cycle



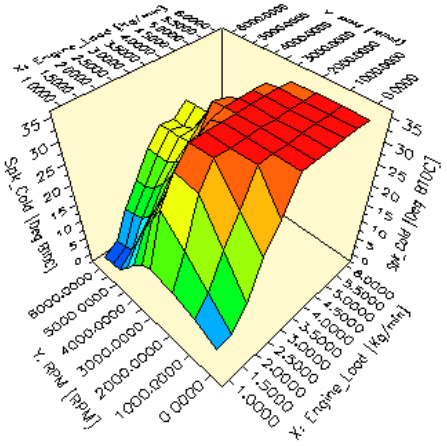

**This is enabled to be calibrated**

```
if (Temperature > 100){
    Fan_Output = true;
}
else {
    Fan_Output = false;
}
```

```
if (Temperature > Temp_Threshold){
    Fan_Output = true;
}
else {
    Fan_Output = false;
}
```

Combined Editor [1]

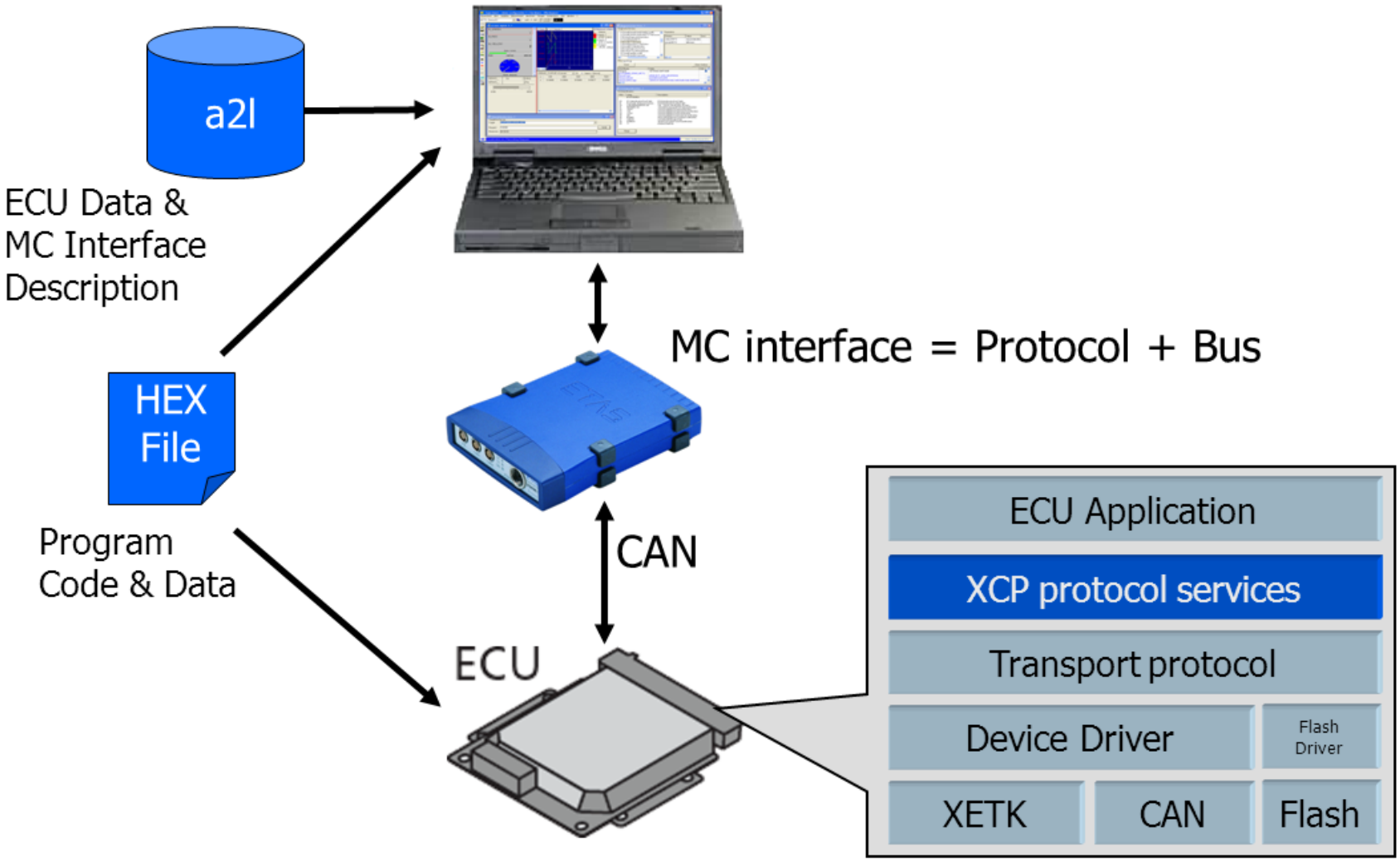
Spk_Cold <Map> [Deg BTDC] x: Engine_Load [Kg/min] y: RPM [RPM]



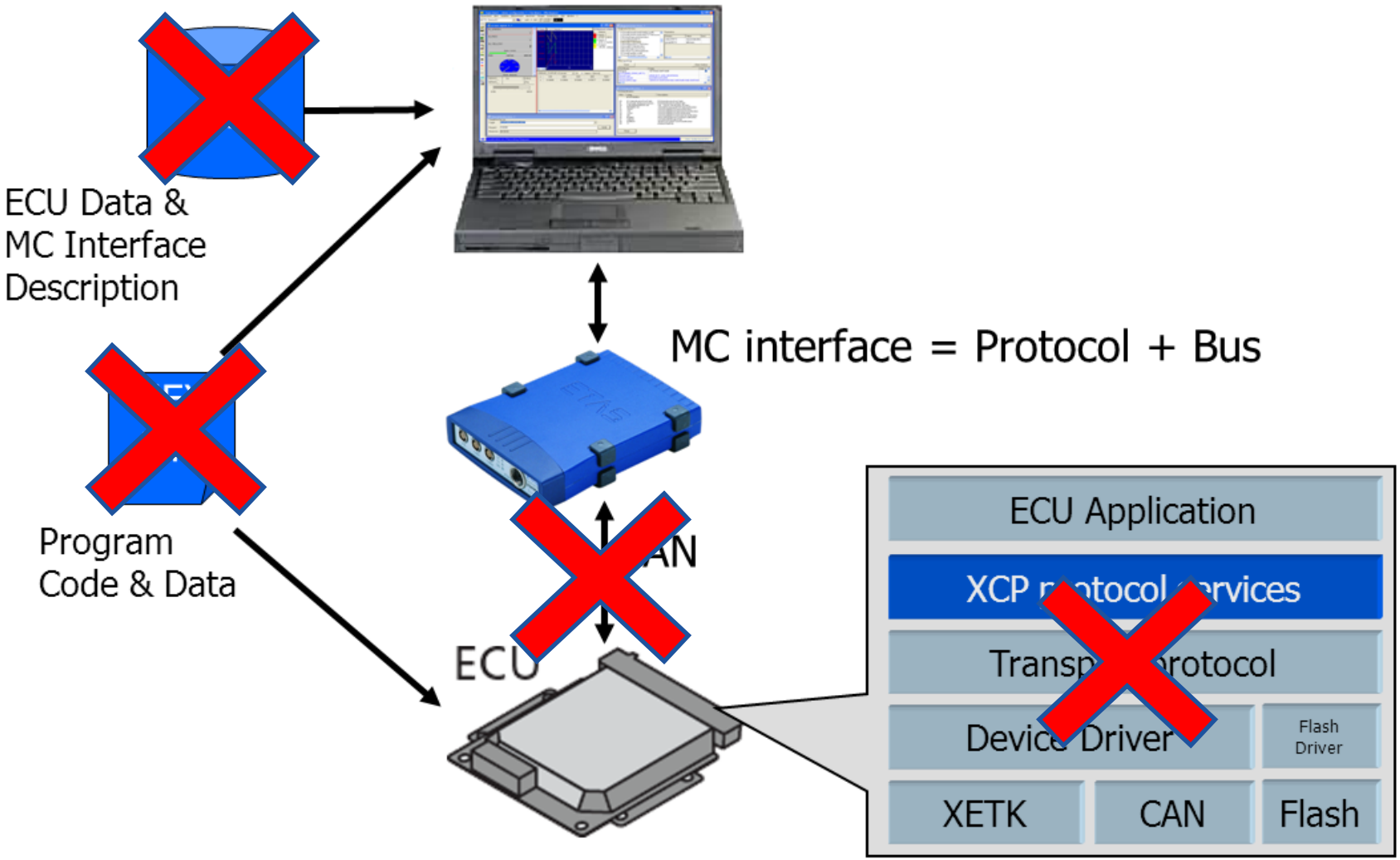

| y \ x | 1.0000 | 1.5000 | 2.0000 | 2.5000 | 3.0000 | 3.5000 | 4.0000 | 4.5000 | 5.0000 | 5.5000 | 6.0000 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0.0000 | 4.5000 | 5.2500 | 10.5000 | 20.2500 | 26.2500 | 34.1323 | 34.1323 | 34.1323 | 34.1323 | 34.1323 | 34.1323 |
| 1000.0000 | 7.5000 | 12.0000 | 20.2500 | 27.0000 | 34.1323 | 34.1323 | 34.1323 | 34.1323 | 34.1323 | 34.1323 | 34.1323 |
| 2000.0000 | 9.7500 | 18.0000 | 29.2500 | 34.1323 | 34.1323 | 34.1323 | 34.1323 | 34.1323 | 34.1323 | 34.1323 | 34.1323 |
| 3000.0000 | 11.2500 | 24.0000 | 30.0000 | 34.1323 | 34.1323 | 34.1323 | 34.1323 | 34.1323 | 34.1323 | 34.1323 | 33.7500 |
| 3500.0000 | 9.7500 | 19.5000 | 23.2500 | 28.5000 | 30.7500 | 33.0000 | 34.1323 | 34.1323 | 34.1323 | 33.7500 | 30.0000 |
| 4000.0000 | 7.5000 | 15.0000 | 18.0000 | 23.2500 | 23.0000 | 28.5000 | 33.7500 | 33.0000 | 29.2500 | 29.2500 | 27.0000 |
| 4500.0000 | 3.7500 | 9.0000 | 13.5000 | 19.5000 | 22.5000 | 25.5000 | 28.5000 | 29.2500 | 24.7500 | 25.5000 | 25.5000 |
| 5000.0000 | 0.7500 | 4.5000 | 10.5000 | 16.5000 | 21.0000 | 24.7500 | 24.7500 | 27.0000 | 22.5000 | 23.2500 | 24.7500 |
| 5500.0000 | 0.0000 | 2.2500 | 9.7500 | 15.0000 | 21.0000 | 24.7500 | 24.0000 | 27.0000 | 21.7500 | 21.7500 | 23.2500 |
| 6000.0000 | 0.0000 | 2.2500 | 9.0000 | 15.0000 | 21.0000 | 24.7500 | 24.0000 | 27.0000 | 21.0000 | 21.0000 | 21.7500 |

| | | |
|---|---|---|
| Lambda_Max | 1.1963 | [] |
| Lambda_Min | 0.8057 | [] |

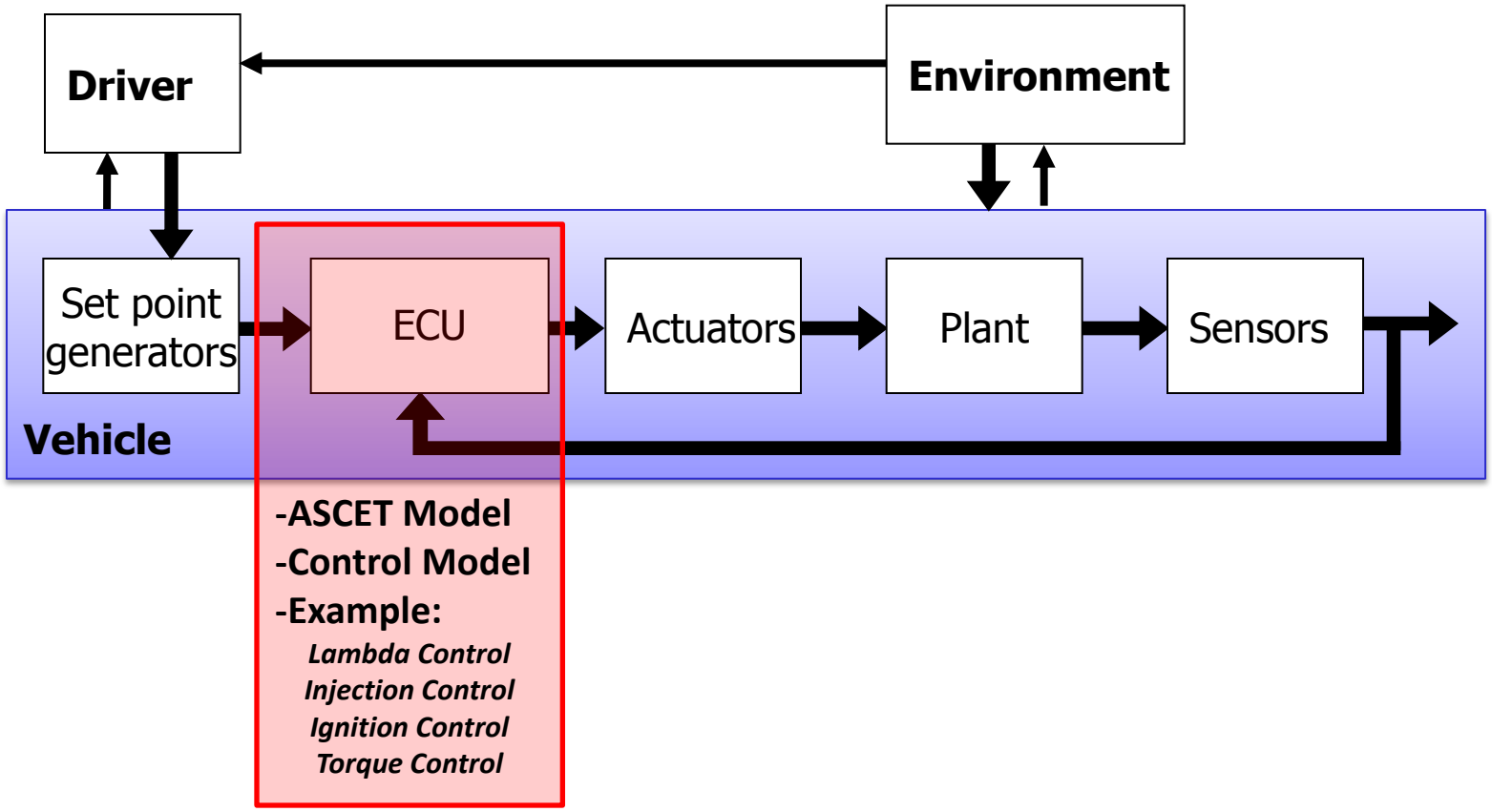
# V-Cycle
## Development ECU ≠ Series ECU



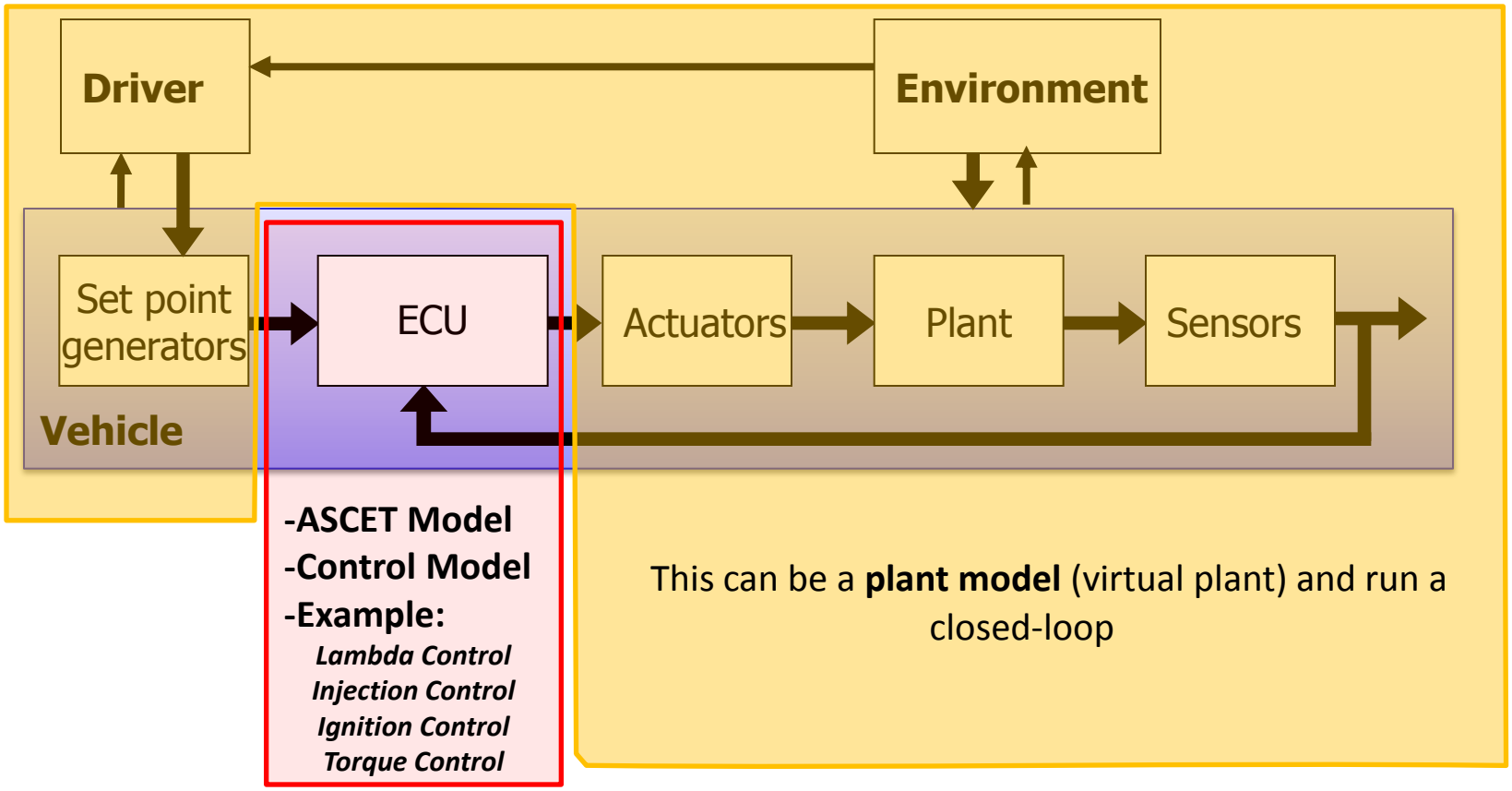
# V-Cycle
## Development ECU ≠ Series ECU



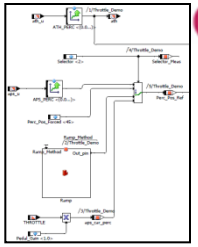
## Basic Control Definition



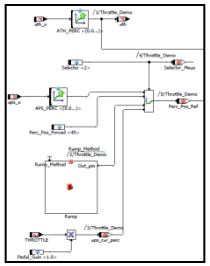
## Closed-Loop Simulation



# V-Cycle
## V-Model - Overview



**ASCET - MD**
Model & Control Design



**INTECRIO ASCET - RP**
Rapid Prototyping (RT simulation)

```
/* Generated by ASCET SE AddOn */
/* (C) 2009 ETAS (ETAS GmbH) */

/*-------------------------------------------------------------------------
 *    Include files
 *-------------------------------------------------------------------------*/

#include "T_60ms_Delayed.h"
#include "globalH.h"
#include "asd_os_dyn.h"
extern void _040GK2GR00001NG7004G4ELDA4A02_ESDL_CAN_IO_ES910_Flow_Control(void);



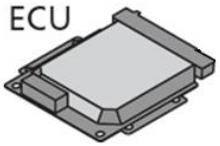
#ifdef ITPC
        TASK_MONITOR_DEF(T_60ms_Delayed, "T_60ms_Delayed");
#else
        TASK_MONITOR_DEF(T_60ms_Delayed,  threadPrio035);
#endif /* ITPC */

/*----- Software task "T_60ms_Delayed" -----*/

        void T_60ms_Delayed_processList()
        {
                #ifdef ITPC
                        LOG_TASK_TRACE_POINT(4);
                #endif
                _040GK2GR00001NG7004G4ELDA4A02_ESDL_CAN_IO_ES910_Flow_Control();
                #ifdef ITPC
                        LOG_TASK_TRACE_POINT(4);
                #endif
}
```

**ASCET - SE**
Code Generation

**RTA Family**
SW Integration

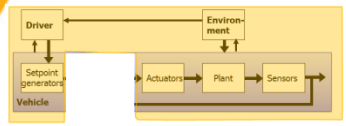



HiL

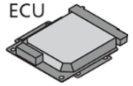
LABCAR

INCA

**Virtual Test & Validation (Plant Model)**



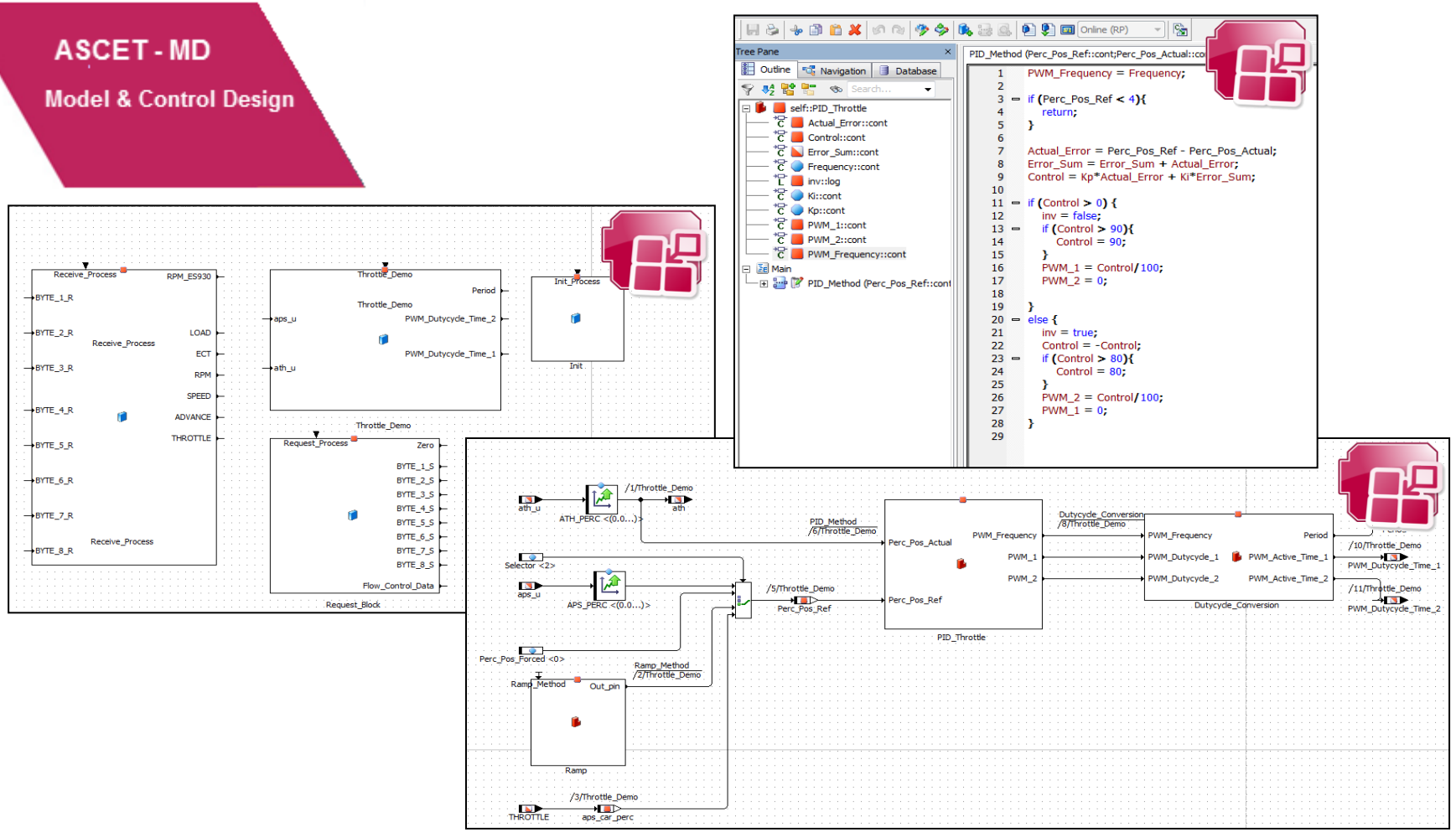

**INCA**
Measurement & Calibration



ETAS

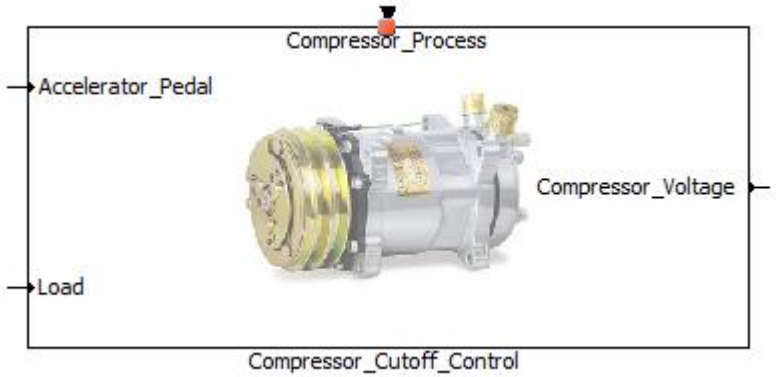
**ASCET - MD**

**Model & Control Design**




# Model Based ≠ Block Diagram

ASCET - MD
Model & Control Design




## INPUTS:

- Load
- Accelerator Pedal

## PARAMETERS

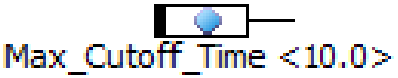
- Load Threshold
- Accelerator Pedal Threshold
- Max Cut-off time

## OUTPUT:

- Compressor Voltage



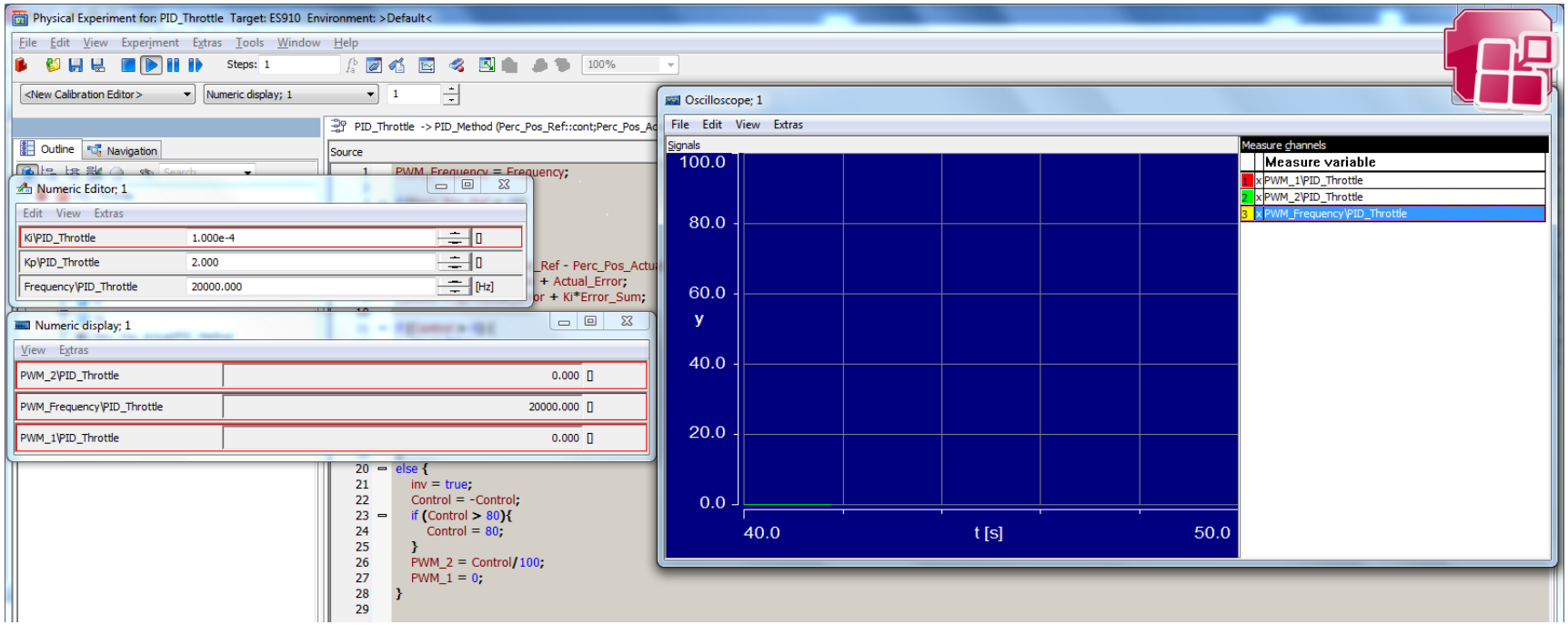





# V-Cycle
## Model Based Development

**ASCET - MD**

**Model & Control Design**



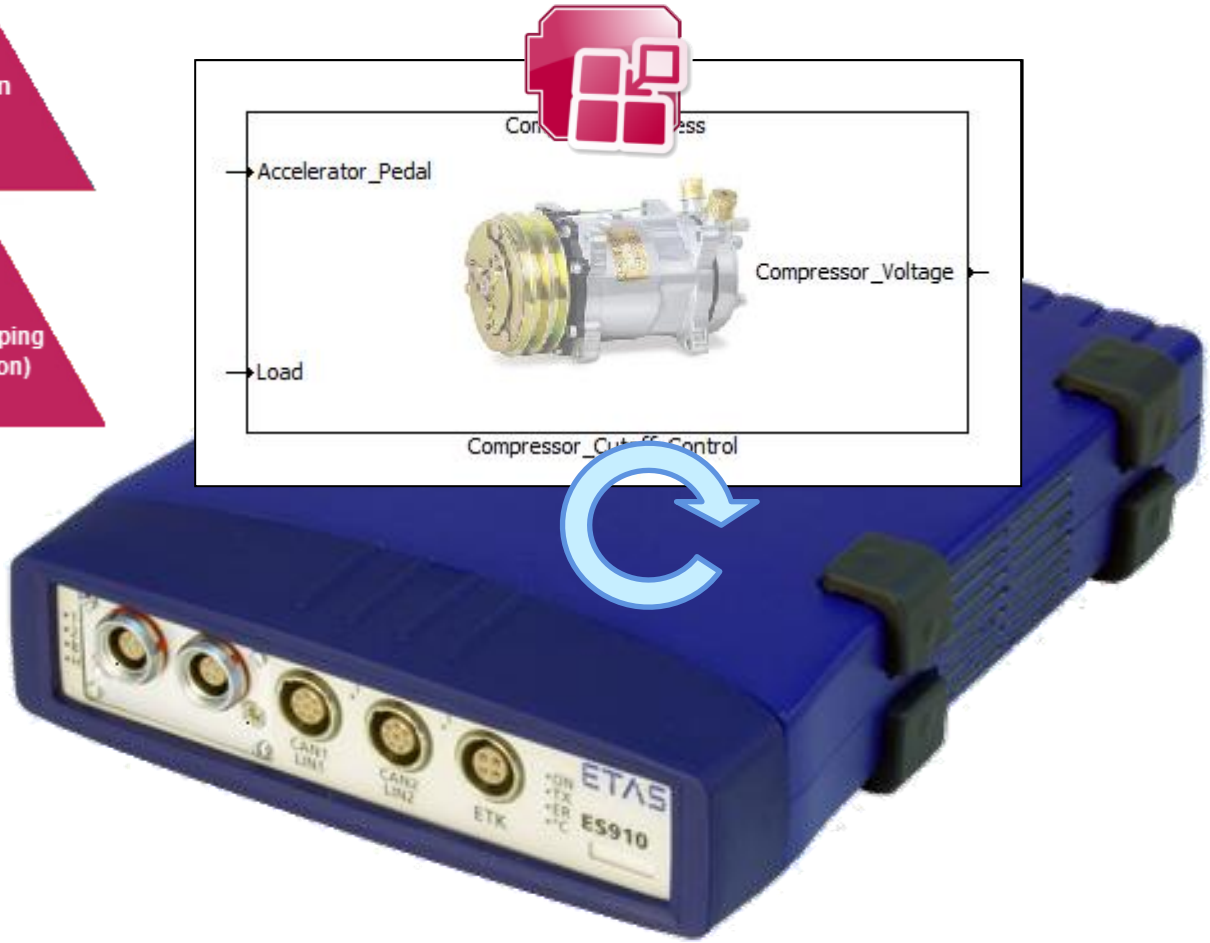

– **Virtual Simulation:** this is not a real time simulation and the model runs on PC with virtual and controlled stimulation of the inputs

**ASCET - MD**

Model & Control Design

**INTECRIO**
**ASCET - RP**

Rapid Prototyping
(RT simulation)




**ES910: Rapid Prototyping (RP) Hardware**

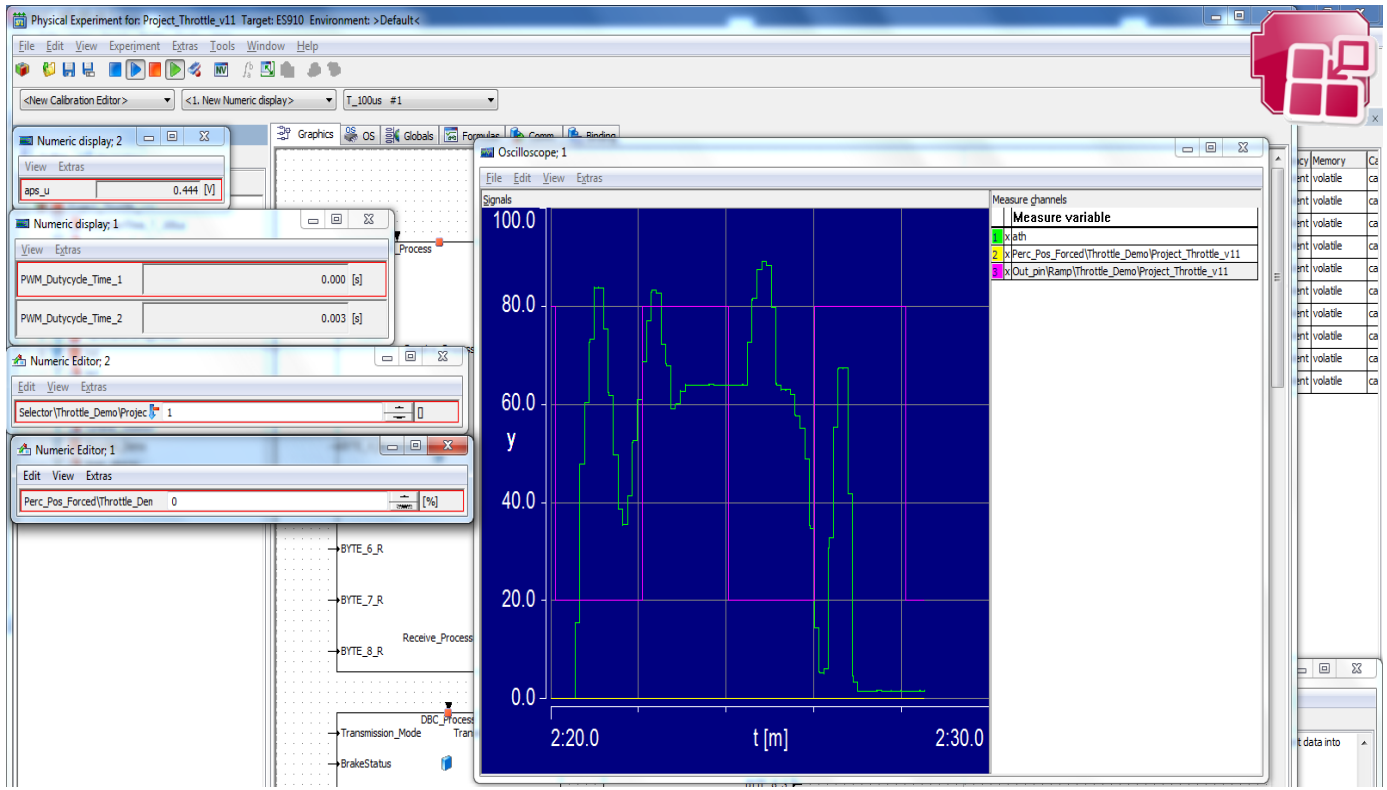
# V-Cycle
## Model Based Development

**ASCET - MD**

Model & Control Design

**INTECRIO ASCET - RP**

Rapid Prototyping (RT simulation)




– **Real Time Simulation:** The ASCET model runs on RP with virtual inputs. The HW is dedicated to execute the code and it runs in real time

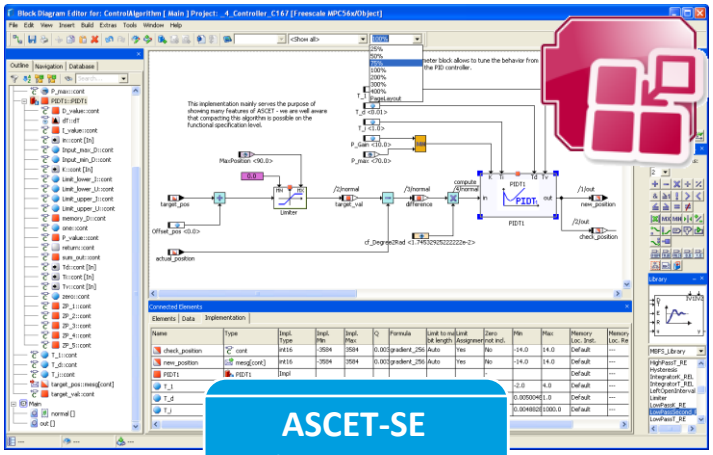
# V-Cycle
## Model Based Development

ASCET - MD
Model & Control Design

INTECRIO
ASCET - RP
Rapid Prototyping
(RT simulation)

ASCET - SE
Code Generation

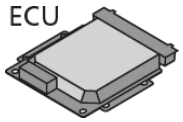
RTA Family
SW Integration



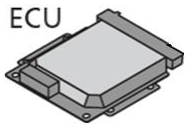
ASCET-SE
Code Generation

a2l
ECU Data &
MC Interface
Description

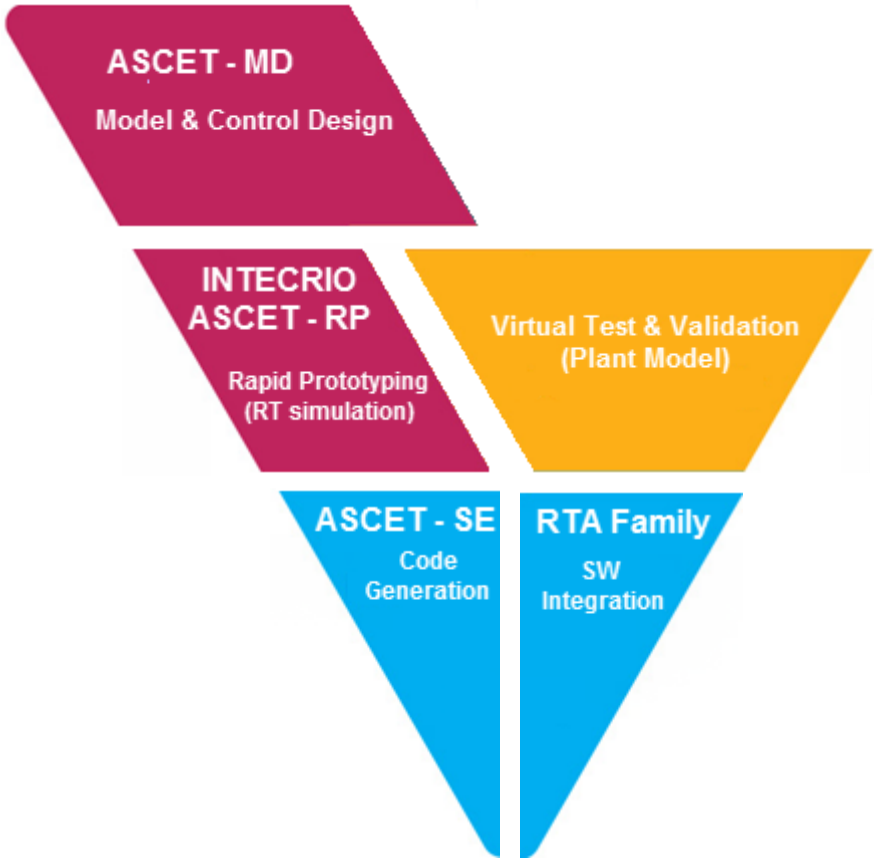
HEX
File
Program
Code & Data



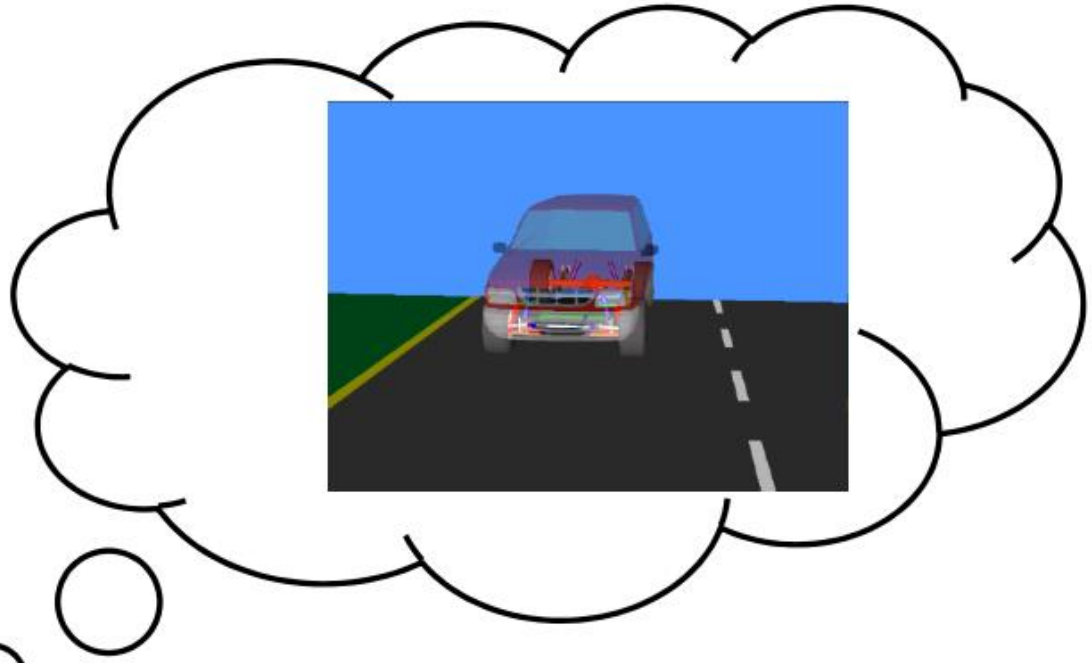

Implementation of the function in the ECU

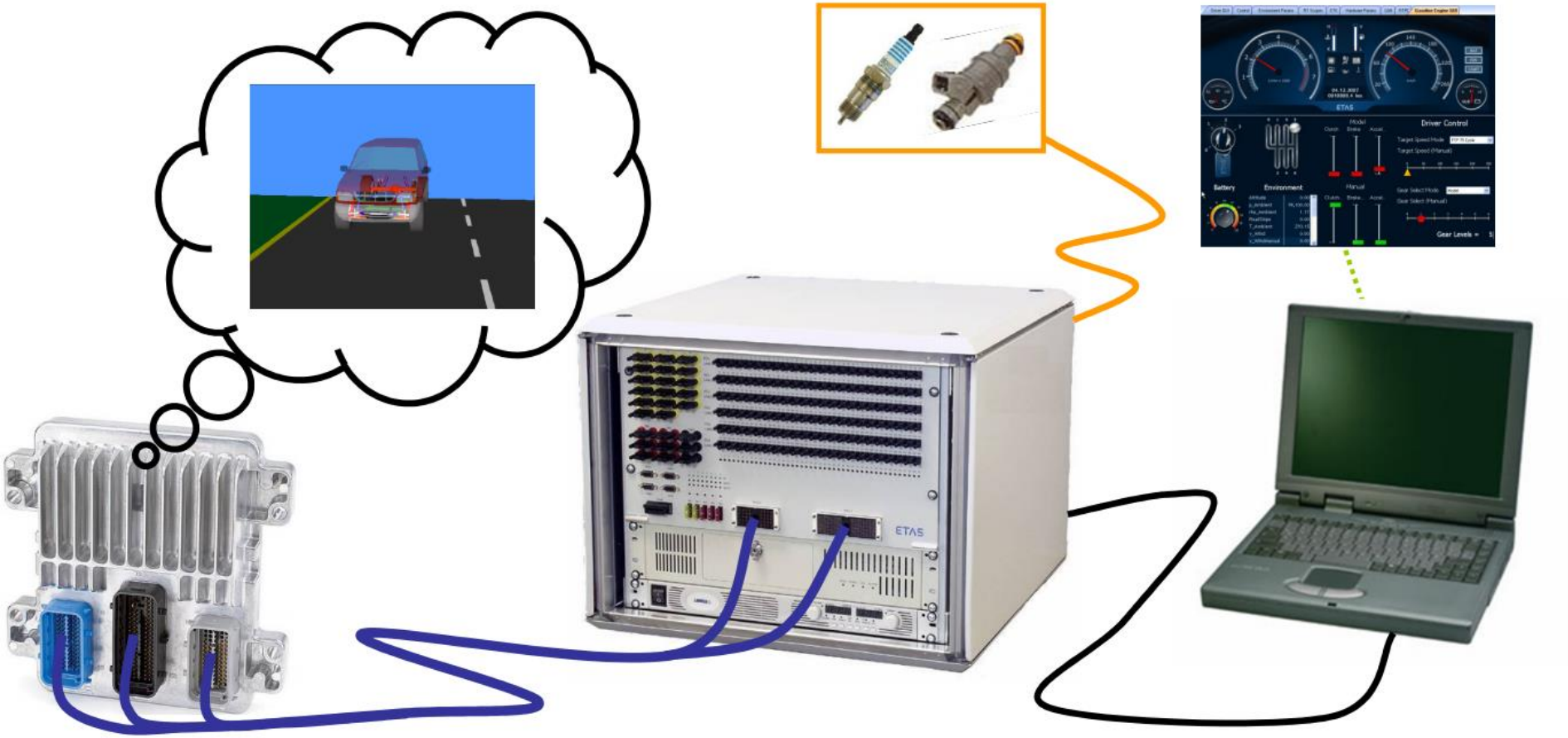
# V-Cycle
## Test & Validation

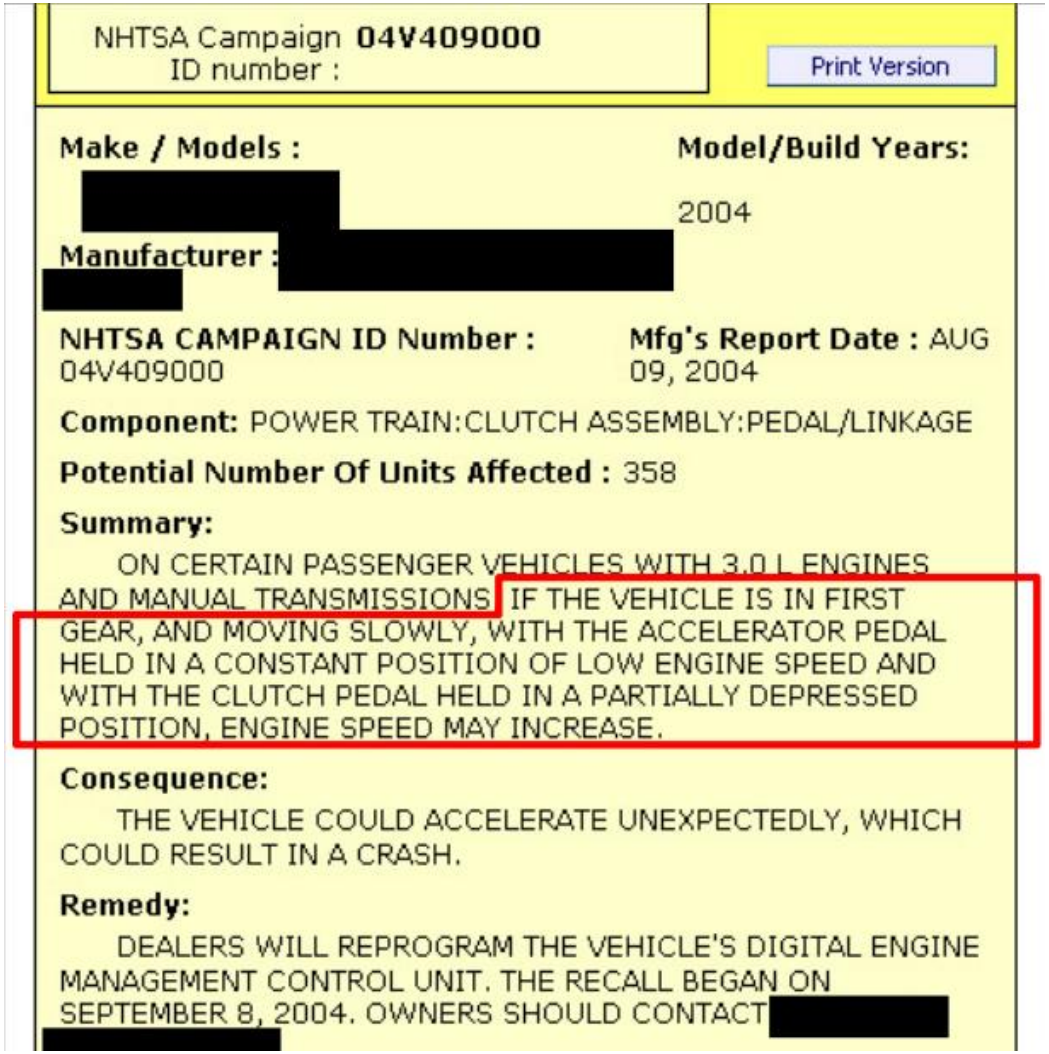


# V-Cycle
## Test & Validation



# V-Cycle
## Test & Validation





NHTSA Campaign **04V409000**
ID number :

Print Version

**Make / Models :** [redacted]

**Model/Build Years:** 2004

**Manufacturer :** [redacted]

**NHTSA CAMPAIGN ID Number :** 04V409000

**Mfg's Report Date :** AUG 09, 2004

**Component:** POWER TRAIN:CLUTCH ASSEMBLY:PEDAL/LINKAGE

**Potential Number Of Units Affected :** 358

**Summary:**

ON CERTAIN PASSENGER VEHICLES WITH 3.0 L ENGINES AND MANUAL TRANSMISSIONS, IF THE VEHICLE IS IN FIRST GEAR, AND MOVING SLOWLY, WITH THE ACCELERATOR PEDAL HELD IN A CONSTANT POSITION OF LOW ENGINE SPEED AND WITH THE CLUTCH PEDAL HELD IN A PARTIALLY DEPRESSED POSITION, ENGINE SPEED MAY INCREASE.

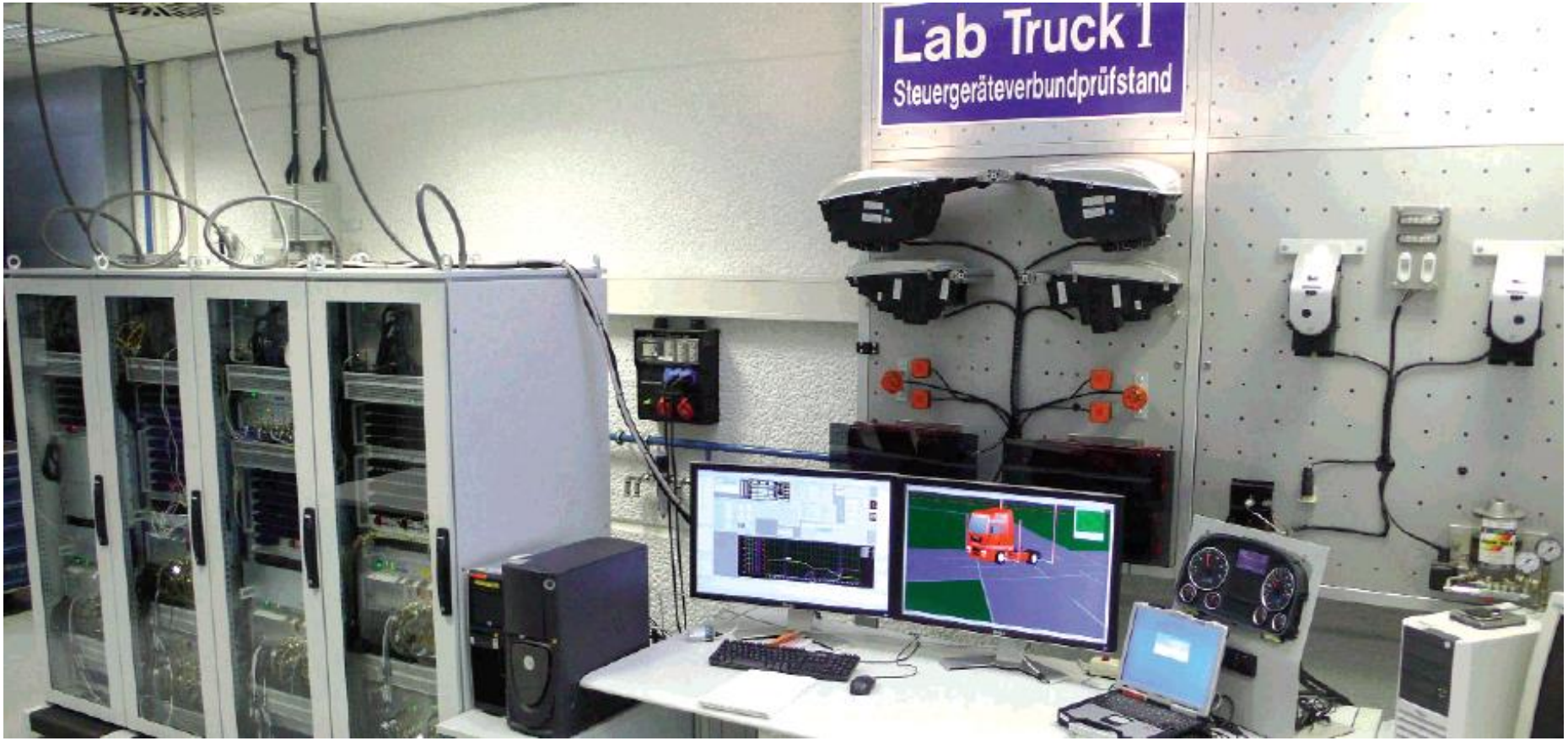
**Consequence:**

THE VEHICLE COULD ACCELERATE UNEXPECTEDLY, WHICH COULD RESULT IN A CRASH.

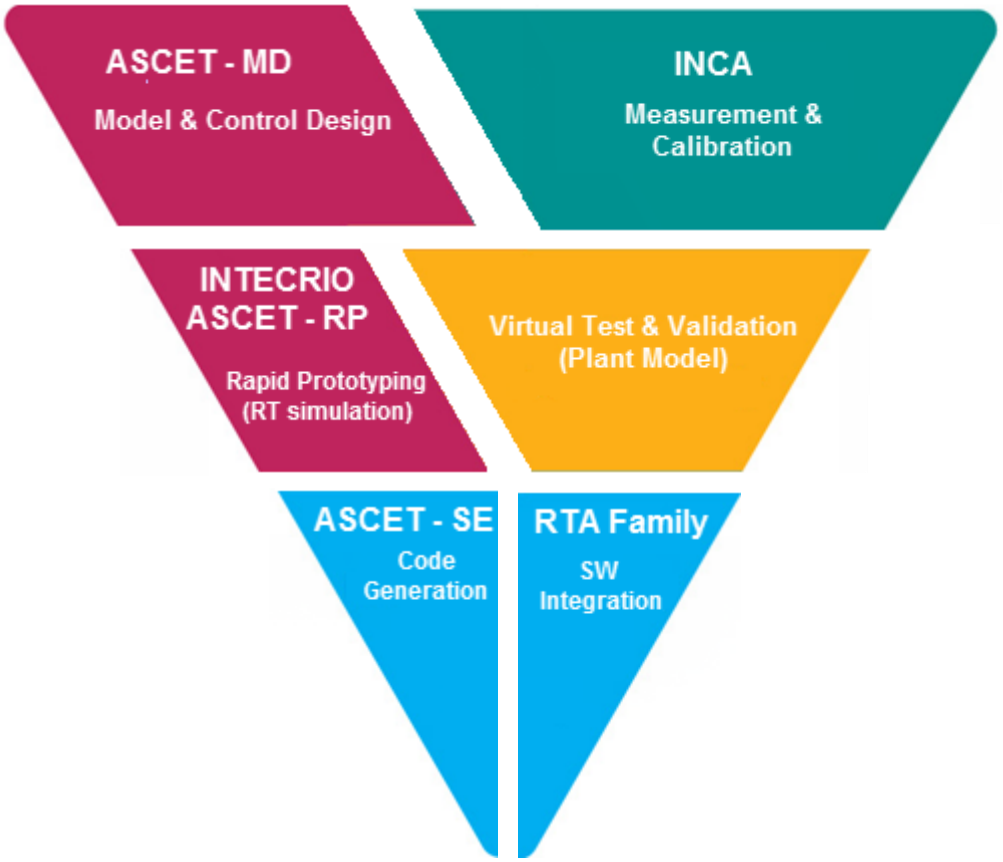
**Remedy:**

DEALERS WILL REPROGRAM THE VEHICLE'S DIGITAL ENGINE MANAGEMENT CONTROL UNIT. THE RECALL BEGAN ON SEPTEMBER 8, 2004. OWNERS SHOULD CONTACT [redacted]

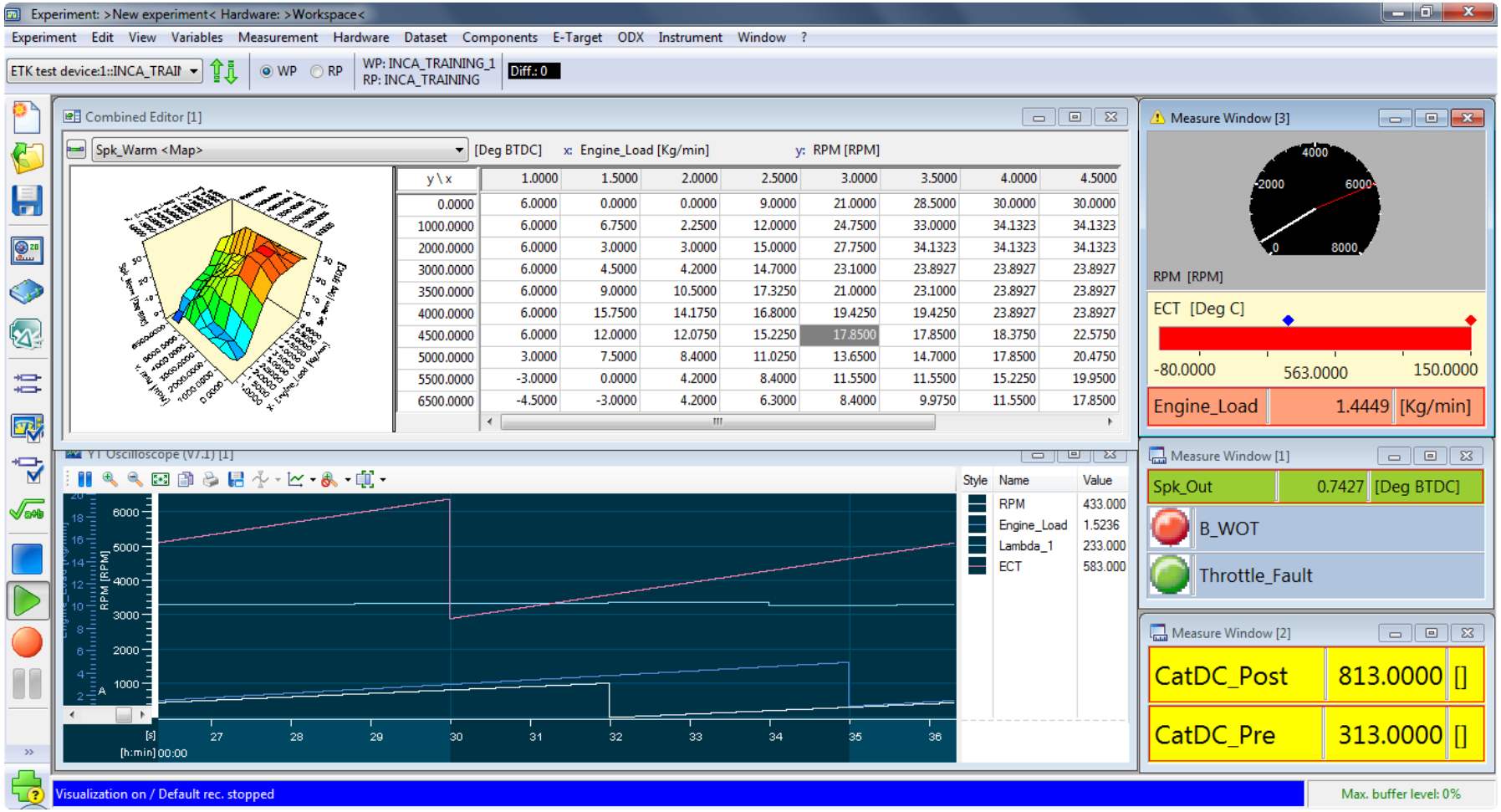
# V-Cycle
## Test & Validation



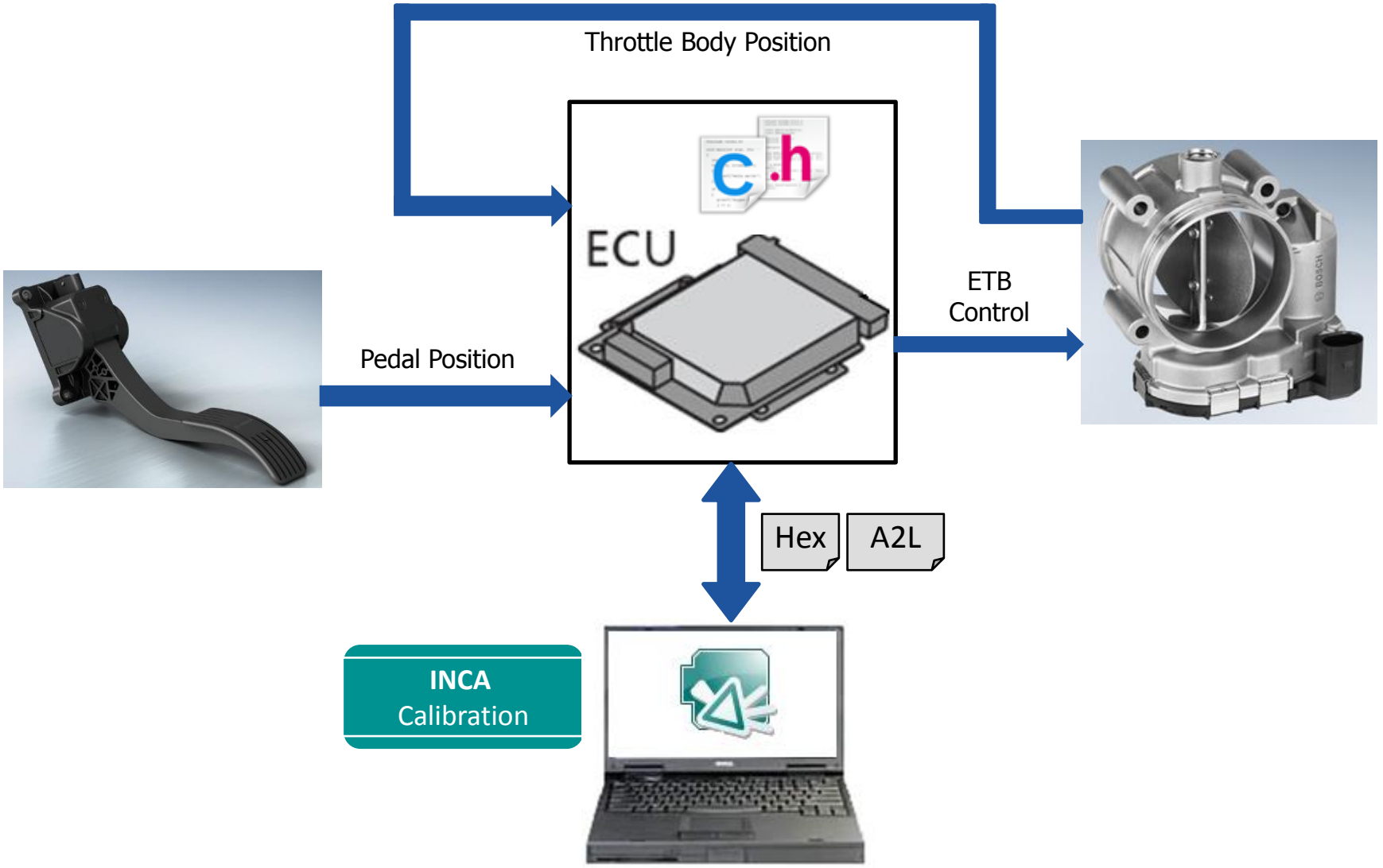
# V-Cycle
## Measurement & Calibration



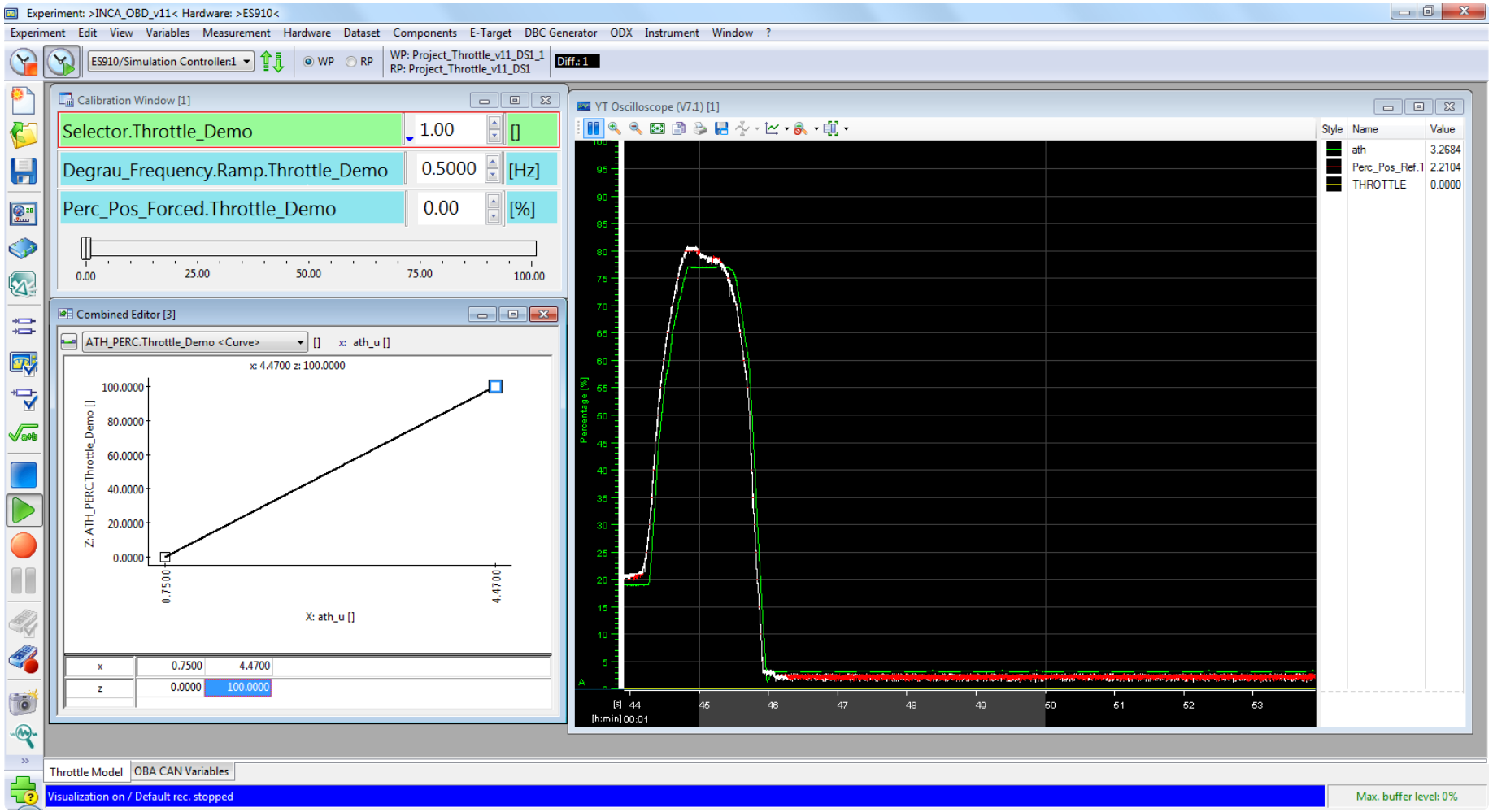
# V-Cycle
## Measurement & Calibration



# V-Cycle
## Measurement & Calibration



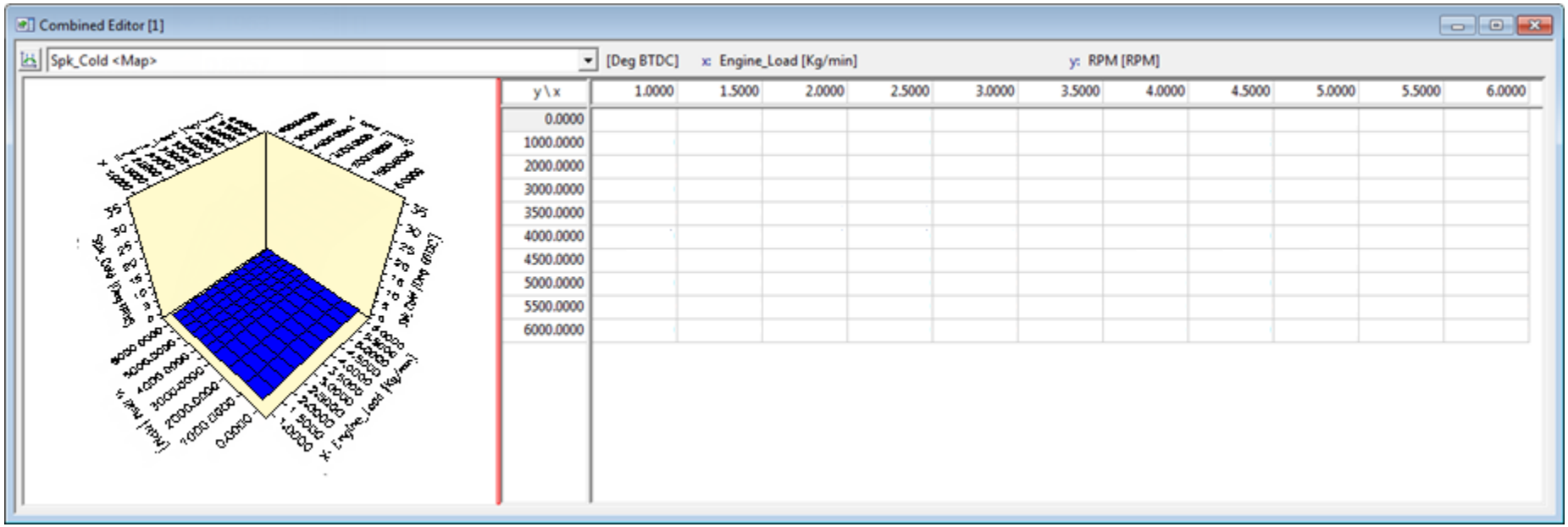
# V-Cycle
## Measurement & Calibration




– **Real Test:** SW & HW of a real ECU with real inputs and real plant. This controller can be calibrated by INCA using .a2l and .hex files

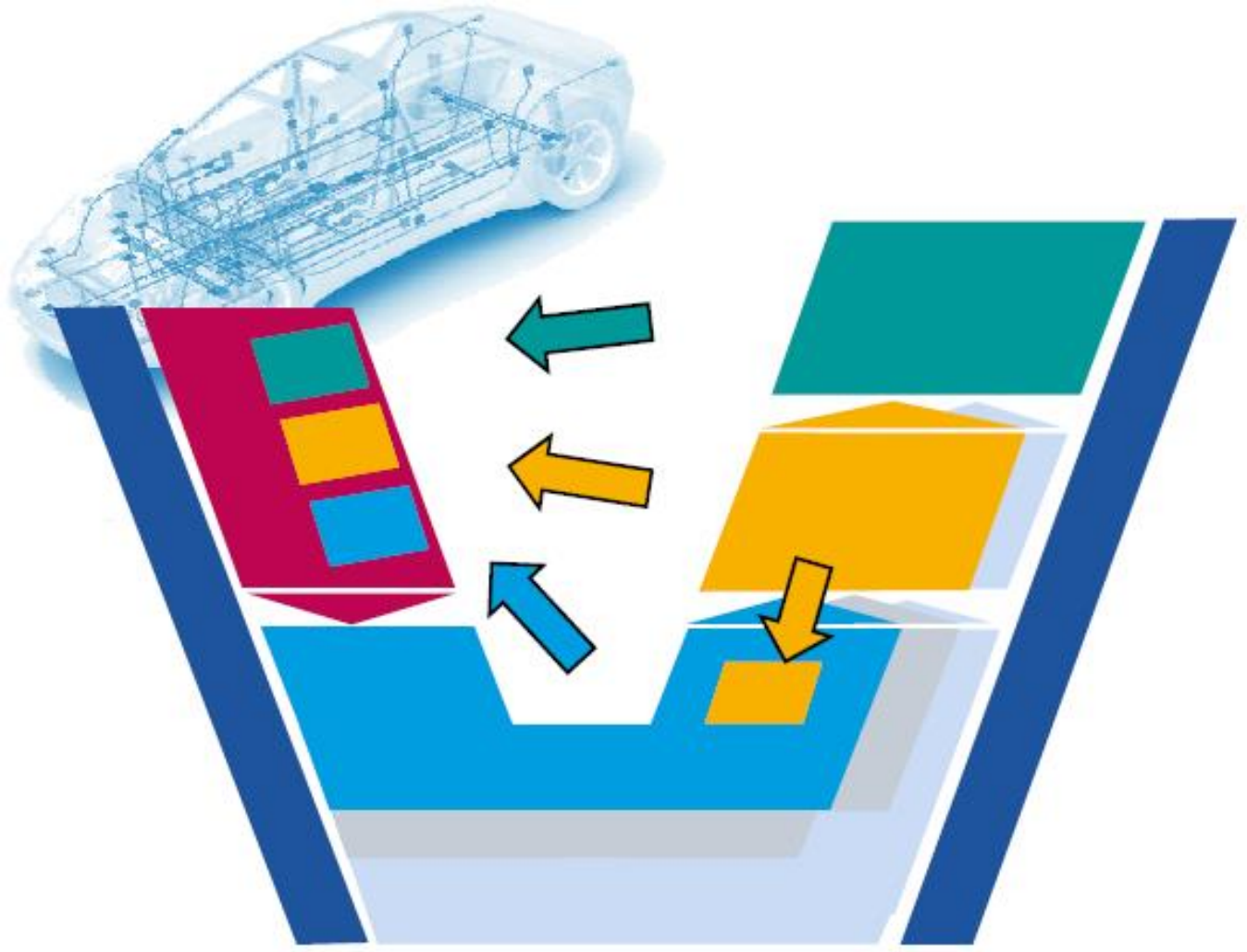
# V-Cycle

## V-Model – Improving Eficiency of the Control Design



# V-Cycle

## V-Model – Improving Eficiency of the Control Design

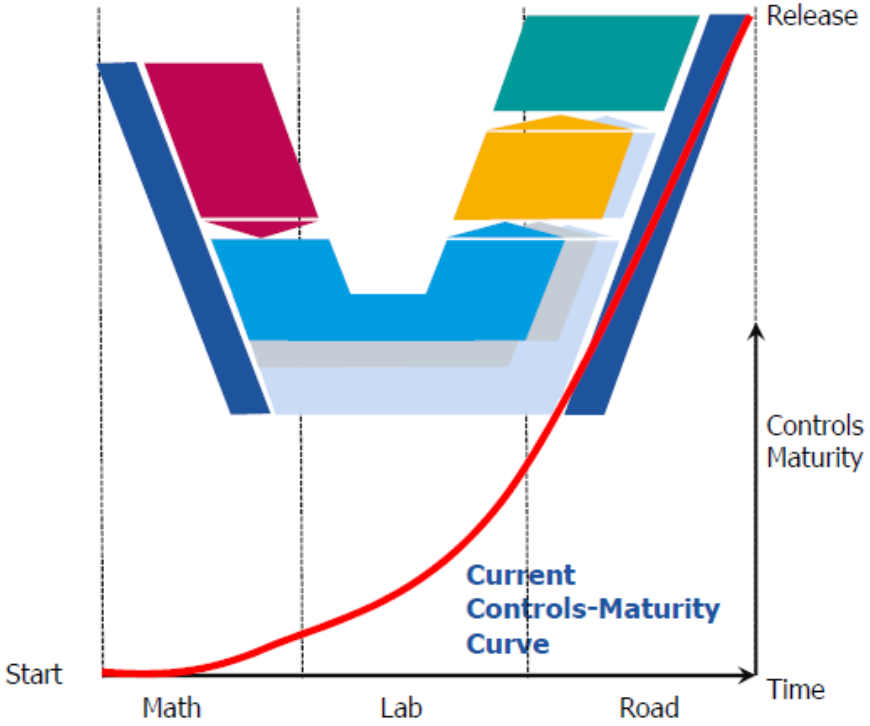


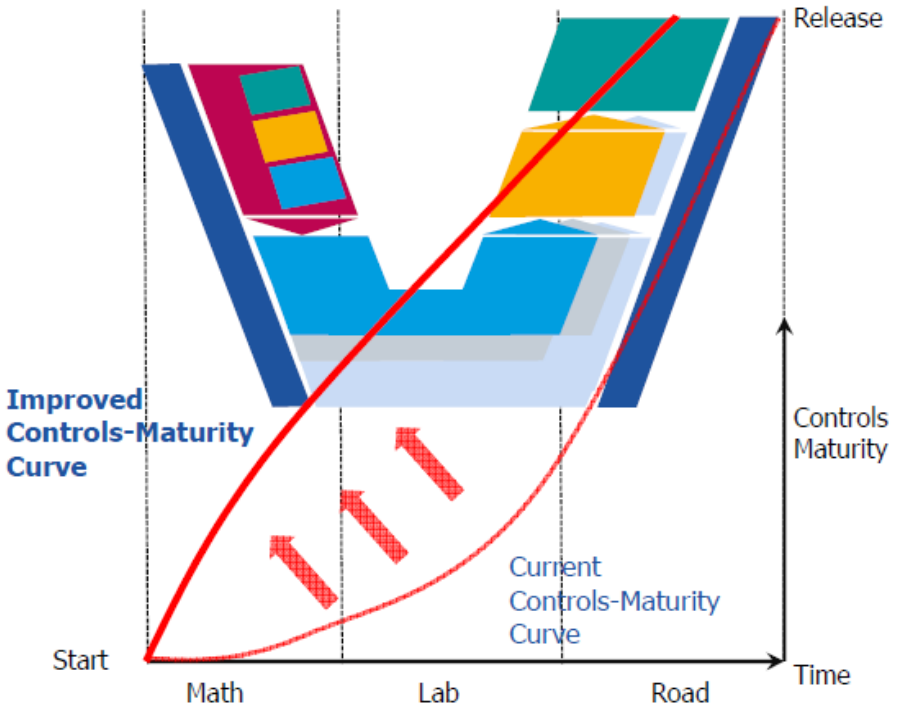
# V-Cycle

## V-Model – Improving Eficiency of the Control Design

**Benefits:**

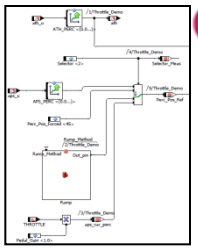
- **Faster completion**
- **Less risk**
- **Less stress: fewer trips to the boss's office…**



# V-Cycle

## V-Model - Improving Eficiency of the Control Design



ASCET - MD

Model & Control Design

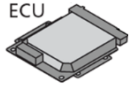
Rap. Prot

ASCET - RP

INCA-EIP

INCA

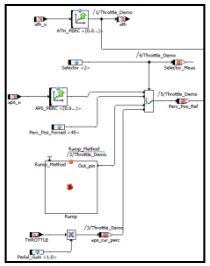
Measurement & Calibration




MiL

ASCET - MD

INCA-SIP

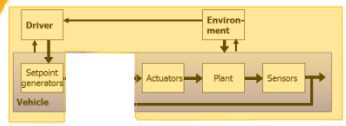


INTECRIO

ASCET - RP

Rapid Prototyping (RT simulation)

Virtual Test & Validation (Plant Model)




SiL

INTECRIO

INCA-EIP

HiL

LABCAR

INCA

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/* (C) 2009 ETAS (ETAS GmbH) */

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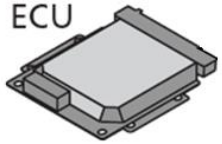
                #ifdef ITPC
                        LOG_TASK_TRACE_POINT(4);
                #endif
}
```

ASCET - SE

Code Generation

RTA Family

SW Integration

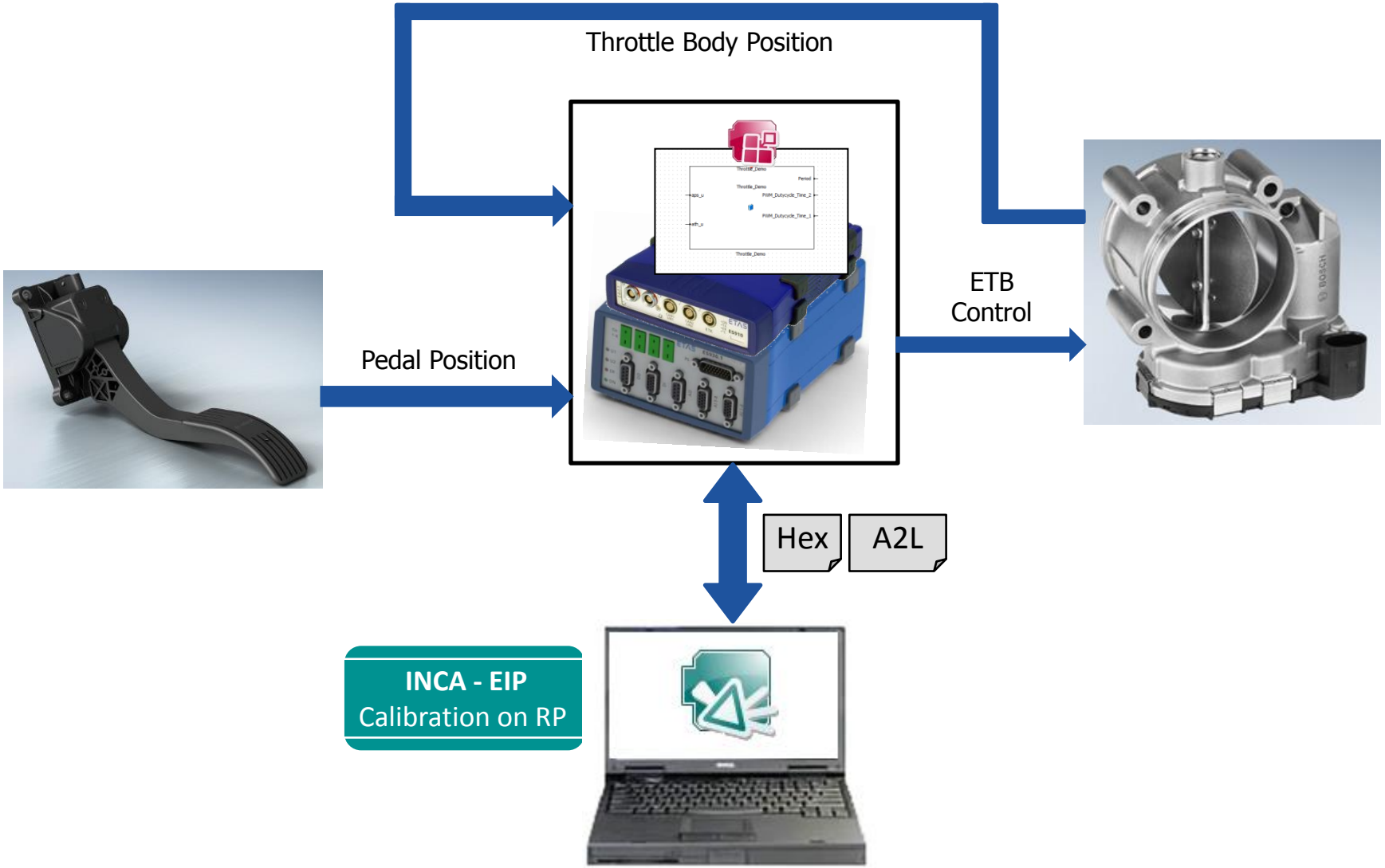



Non-Real Time Simulation

Real Time Simulation

# V-Cycle

## V-Model – Rapid Prototype using a Real Plant



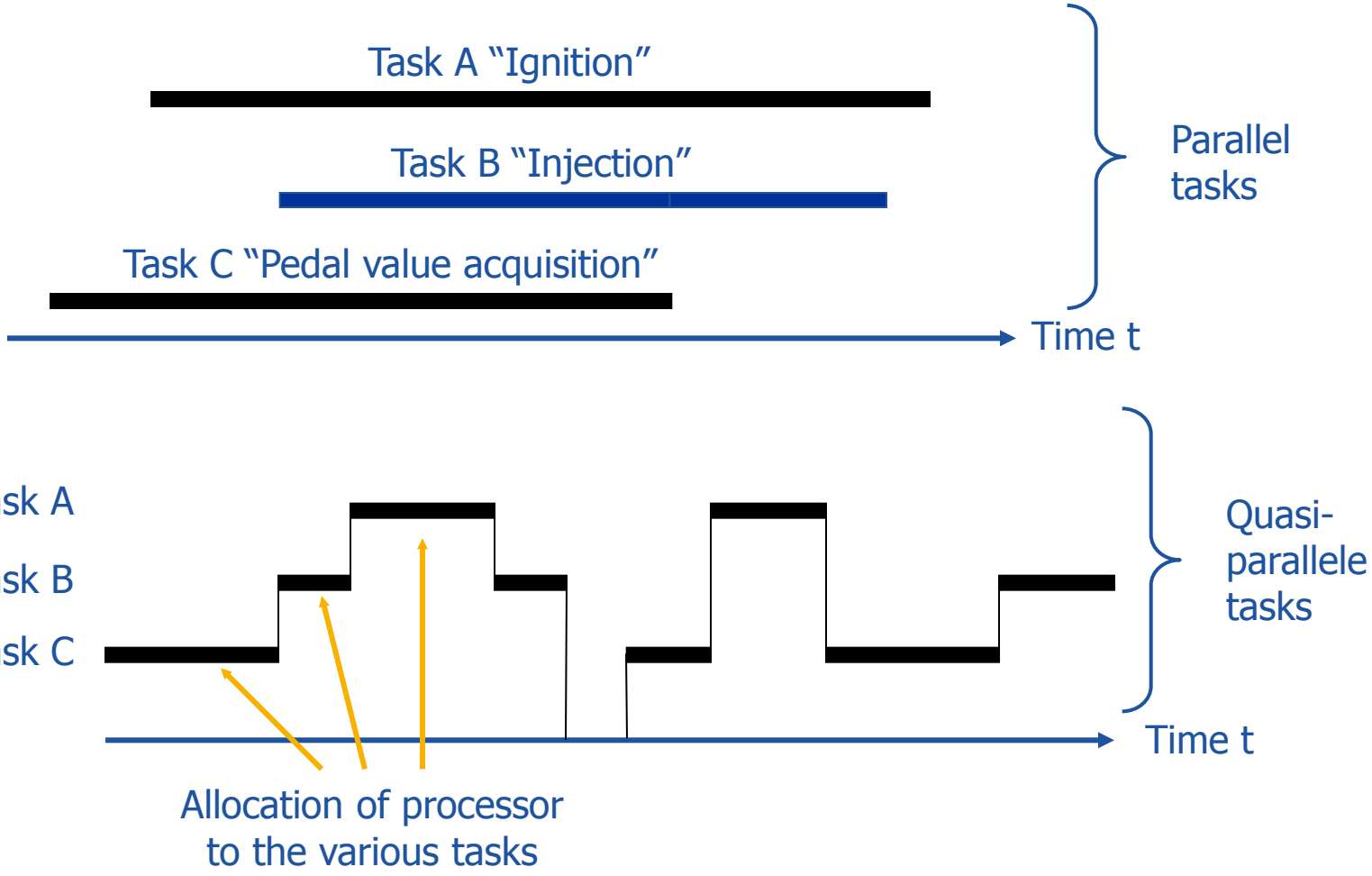
## Operating Systems:

- Control and processing of a variety of tasks on a single processor;
- Management and allocation of resources as processor, I/O and memory;
- Interface between tasks.

## Task:

- Unit of work that is managed by the OS and executed by the processor;
- Using a one core controller, hence, at one time only one task can be executed;
- OS can switch between tasks according to the priority and the scheduling. The step can be so fast that creates the impression of parallel processing. The term is **quasi-parallel**.

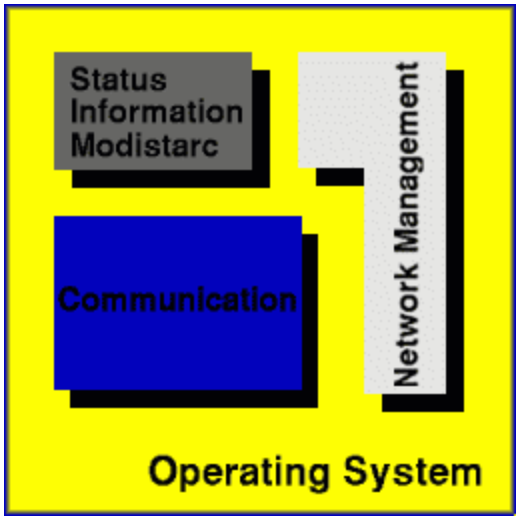
# V-Cycle
## Real Time Operating System (RTA – OSEK)



## OSEK/VDX

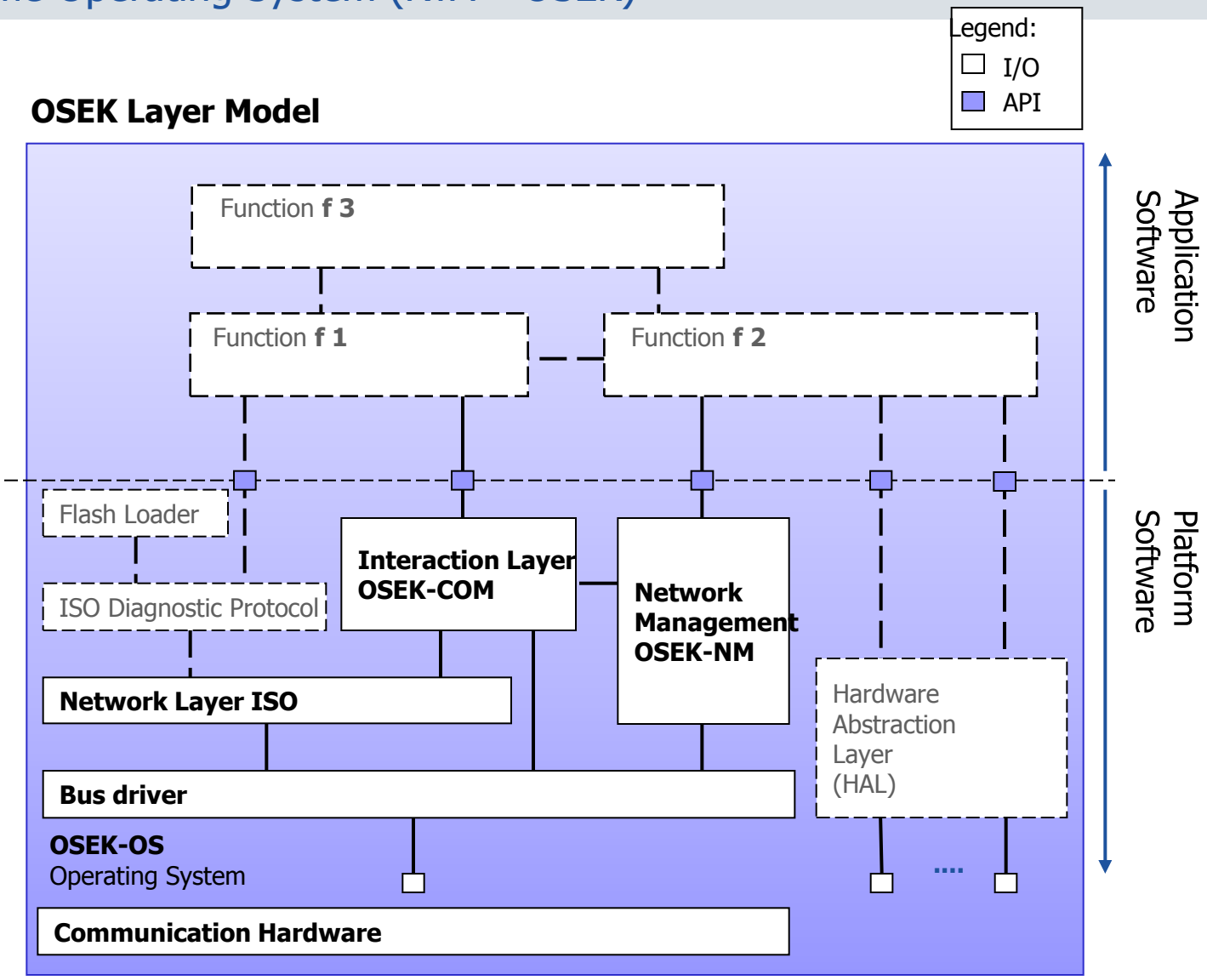
Open systems and the corresponding interfaces for automotive electronics.

Consortium of automobile industry representatives pursues the objective of defining standards to be applied to automotive system software.




Aiming at an industry standard for an open-ended architecture for distributed control units in vehicles

### OSEK Layer Model



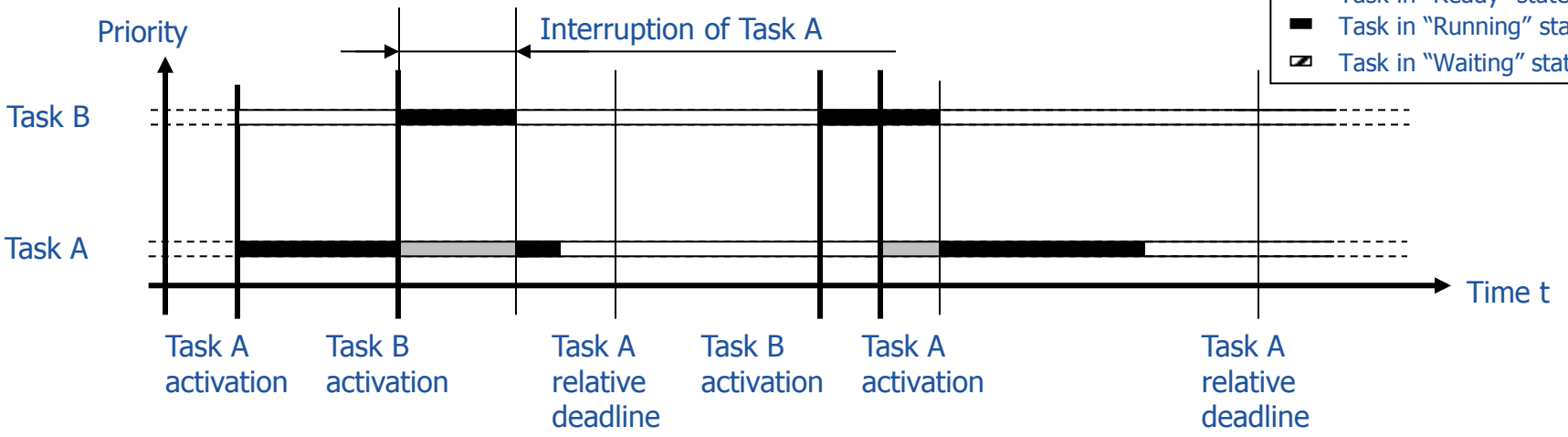
## Scheduling

The scheduling is made considering the priority and the type of chosen processor: Preemptive (preemp) or Cooperative (coop).

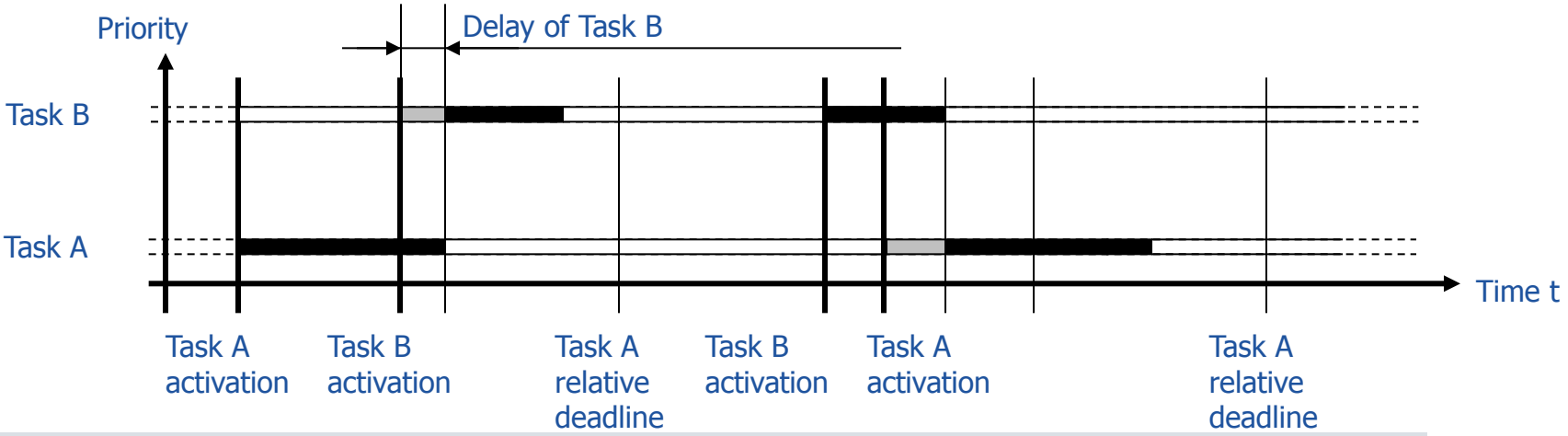
- **PREEMPTIVE PROCESSOR:** a higher-priority task may interrupt the execution of a lower-priority task. So the task switching occurs exactly when the H-P task is needed.

- **COOPERATIVE PROCESSOR:** a higher-priority task is unable to interrupt the execution of a lower-priority task. So the task switching occurs only after the conclusion of the L-P task and because of that the execution of a H-P task is delayed by the L-P task.

– **Preemptive Processor:**




– **Cooperative Processor:**



Thanks **Prof. Dr. Dieter Nazareth** for providing a training of Model Based Development of Automotive Software

Thank you

Muchas gracias

谢谢

Tack så mycket

Děkuji

धन्यवाद

Hvala

Mille Grazie

Merci

감사합니다.

Obrigado

Спасибо!

有難うございました

Vielen Dank

Kiitos

Д‘якую