Automotive Electronics

Product Information
Companion IC with 5V ADC - CY100

BOSCH
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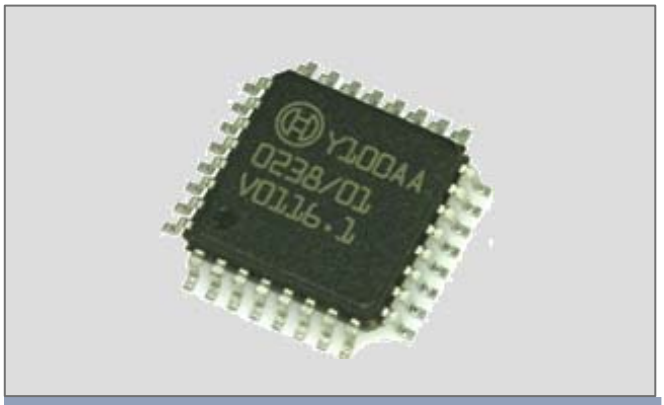


Eight channel 10 bit A / D converter with 5 V interface for 3.3 V or 2.5 V controllers for automotive, truck and 42 V applications

The CY100 is designed to assist a low voltage microcontroller in automotive applications. The eight channel 10 bit analogue-to-digital converter ADC operates half-automatically with 5 V-inputs. Because of the possibility of slew rate limitation, the ISO interface can operate both in BSS and LIN applications. Two signal stages with diagnosis can be used to control small signal loads like light emitting diodes (LEDs). With the SPI interface the controller can communicate without real time conditions up to 2 Mbaud.

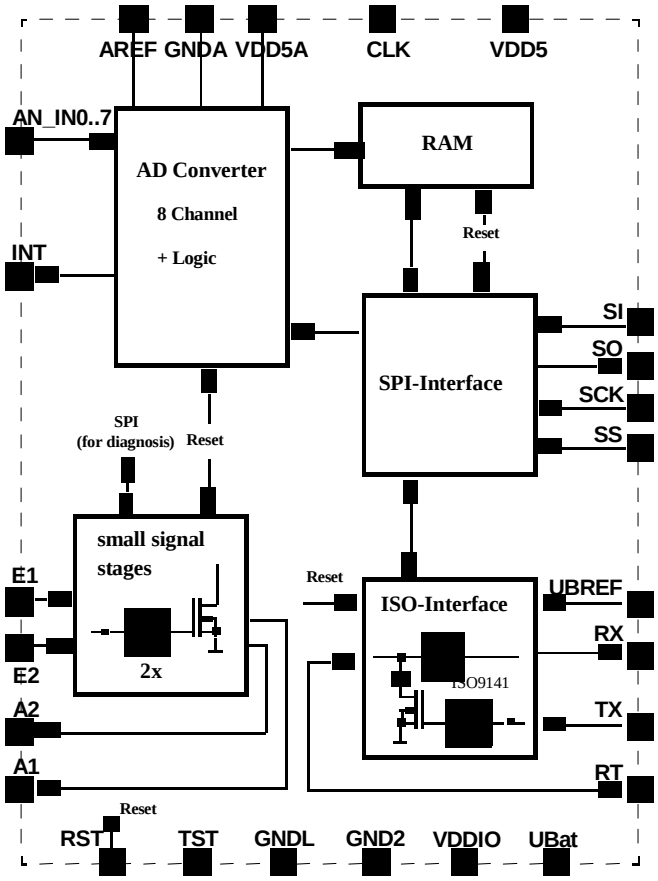
Customer benefits:

- Excellent system know-how
- Smart concepts for system safety
- Secured supply
- Long- term availability of manufacturing processes and products
- QS9000 and ISO/TS16949 certified

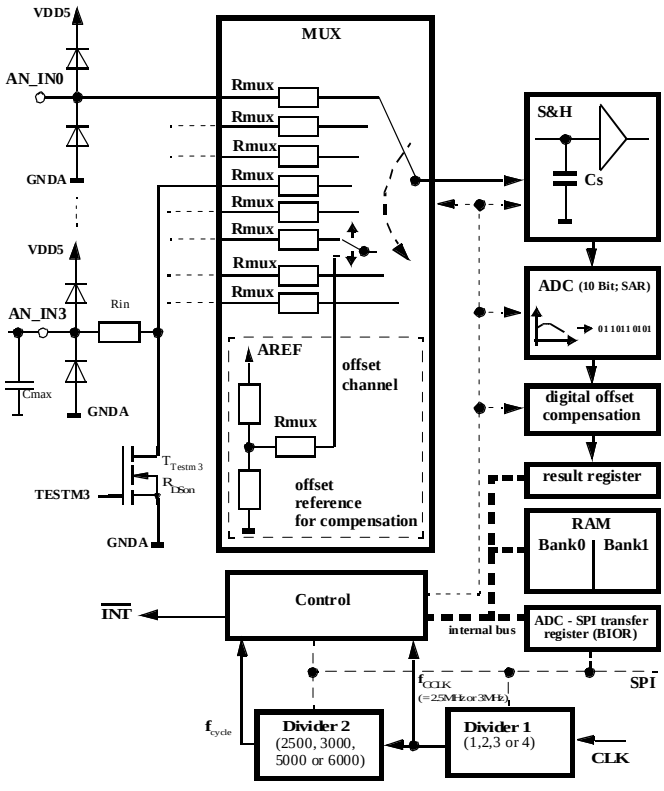
Features

- Eight channel 10 bit A / D converter
- Approved ISO interface , slew rate limitation, bidirectional serial interface driver according ISO 9141
- Two small signal stages with diagnostics
- SPI interface
- All I / O – ports designed for 2.5 V to 3.6 V logic level
- Package : LQFP32

Block diagram



Application example



Pin description

Pin	Name	Function
16	RX	Receiver output driver ISO 9141
15	TX	Transmitter input driver ISO 9141
14	RT	Input/output driver ISO 9141
13	UB_REF	UB-Reference for theISO 9141 receiver
9	A1	Output small signal stage 1
10	A2	Output small signal stage 2
8	E1	Input small signal stage 1
7	E2	Input small signal stage 2
32	AN_IN0	Analog input 0
31	AN_IN1	Analog input 1
30	AN_IN2	Analog input 2
29	AN_IN3	Analog input 3
28	AN_IN4	Analog input 4
27	AN_IN5	Analog input 5 (only half sample rate of the others channels)
26	AN_IN6	Analog input 6
25	AN_IN7	Analog input 7
22	CLK	CLK-input for the A-to-D Converter (Necessary to enable the CY100)
23	INT	Interrupt-Output for the A-to-D Converter
17	SS	SPI slave-select signal
19	SO	Slave-Out signal (SPI data output)
18	SI	Slave-In signal (SPI data input)
20	SCK	SPI serial clock input
1	AREF	Analog reference voltage for the ADC
2	VDD5A	Analog supply voltage 5 V
3	GNDA	Analog ground
12	UBat	UBat Pin for ESD protection
6	VDD5	5 V - digital supply
21	VDDIO	3.3 V / 2.5 V - supply for IO
5	GND1	Digital-ground mainly for 'on chip' digital modules
11	GND2	Digital-ground mainly for 'on chip' power modules like ISO, KSA and SPI
4	RST	Reset-input
24	TST	not used -> to be connected to ground

Maximum ratings

Parameter	Min	Max	Unit
Maximum Voltage, RT	-15	60	V
Maximum Voltage, UBat, UB_REF	-2	60	V
Maximum Voltage, A1, A2	-0.6	60	V
Maximum Voltage, VDD5,	-0.3	6	V
VDD5A, AREF	-0.3	4	V
Maximum Voltage, VDDIO	-0.3	U_{VDD5}	V
Maximum Voltage,AN_INx, CLK		+ 0.3	
E1, E2, RST, SCK, SI, SS, TX	-0.3	U_{VDDIO}	V
Maximum Voltage, INT, RX, SO		+ 0.3	
Frequency operating range	2.5	12	MHz
Maximum SPI transfer rate		2	MBd
Operating temperature T_j	-40	150	°C
Thermal resistance		60	K/W
ESD HBM, MIL883D 3015			
100pF / 1.5kΩ			
A1, A2, RT	- 4	+ 4	kV
All other pins	- 2	+ 2	kV

A/D Converter (ADC)

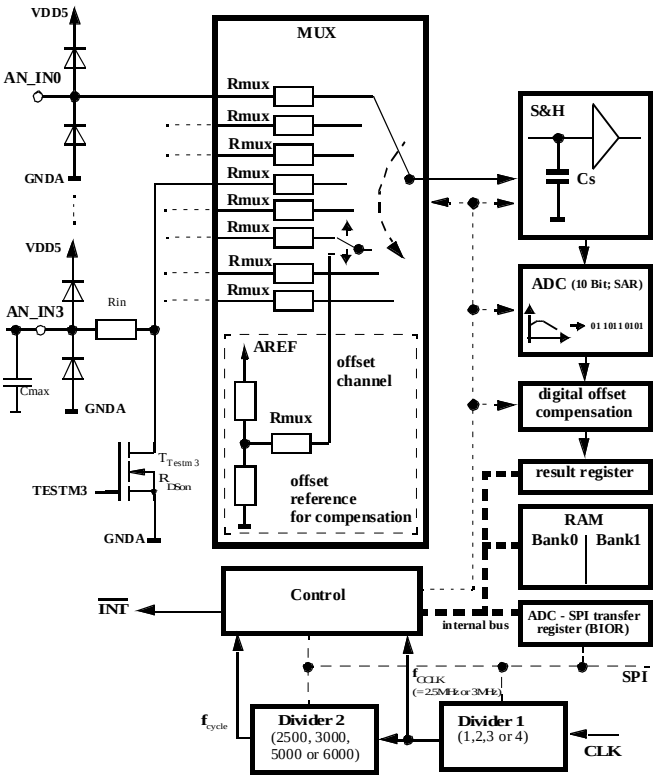
The CY100 uses a 10 Bit SAR (successive approximation register) Converter with S&H (sample and hold) element. The total error (gain, offset, non linearity) is less than 2 LSB and less than 4 LSB near ground or AREF. The CY100 has an internal offset compensation algorithmus. The conversion and sample time for each channel is faster than 125 us. The ADC is mixed to 8 external input channels except channel 5, which is additional multiplexed with the internal channel for the CY100 offset compensation on chip.

So a converting time of 1 ms of channel 0 to 4 and 6 to 7 can reached, whereas channel 5 can be converted every 2 ms. All 8 channels are running in timed mode without jitter.

The input voltage range is 0 V. 5.5 V. The input pins AN_INx are clamped to VDD5 and GND by an ESD protection diode. The ADC has a separate reference input pin AREF.

After conversion of all 8 channels the results are storaged in the result RAM. After ending the conversion of channel 7 the output INT becomes active (low). This output can be used to trigger a microcontroller with interrupt or DMA request.

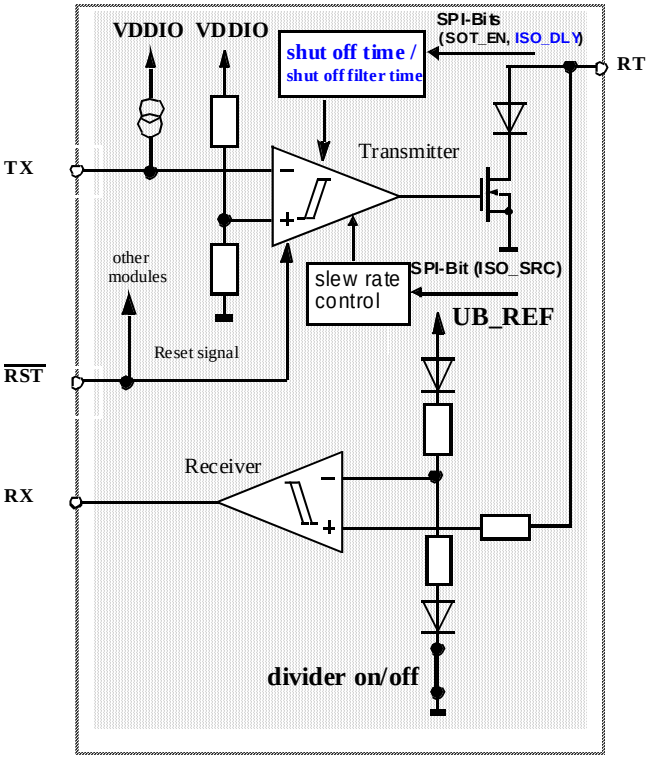
Parameter	Min	Max	Unit
Input range	-0.3	U_{VDD5A} + 0.3	V
Switched capacitance		20	pF
Resolution for the input range		10	Bit
Conversion time for each channel (f=2,5 MHz)		122	µs
Maximum sample rate		1	kHz
AREF = 5 V :			
Resolution, 0.1 V < AN_INx < 4.9 V		± 2	LSB
Resolution, AN_INx ≤ 100 mV		± 4	LSB
Resolution, AN_INx ≥ 4.9 V		± 4	LSB



Serial Interface / ISO Driver

Integrated in the CY100 is one bi-directional serial interface driver, enabling data transfer according to ISO 9141. The driver can be used, for example, as the diagnosis interface, for an immobilizer or for a generator interface. If the interface is not used, the transmitter side can be deployed as a small-signal stage.

The input/output pin RT is protected against destruction from ISO impulses 3a and 3b.



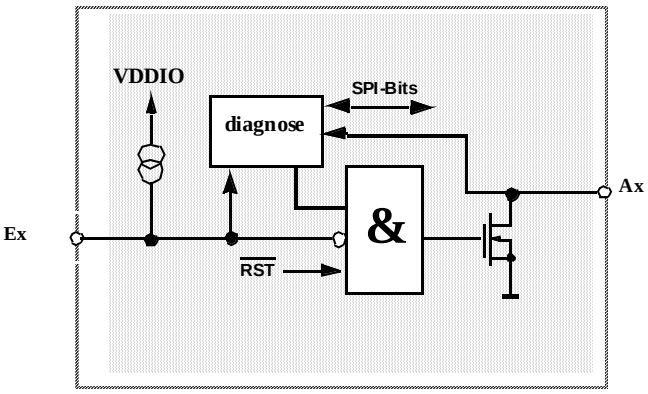
Parameter	Min	Max	Unit
RT low level at I_{RT} = 40 mA		1.4	V
RT nominal output current		50	mA
RT off state input current	-5	10	µA
RT slew rate limitation, negative edge, deactivatable	1	3	V/µs
RX1 low output voltage		U_{VDDIO}	V
RX1 high output voltage	U_{VDDIO} – 0.4		V
TX1 low level	-0.3	0.3 * U_{VDDIO}	V
TX1 high level	0.7 * U_{VDDIO}	U_{VDD5} + 0.3	V

Small signal stags

Two identical small-signal stages with open-drain outputs are integrated in the CY100. The output stages are mainly for digital outputs, for the control of “semi-intelligent” actors (e.g. semi-conductor relays) and for driving LEDs.

The inputs E1 and E2 are realized as comparators with VDDIO - dependent threshold. The inputs have pull-up current sources, so that in case of an open input, the output stages are disabled. The phase of the outputs is non-inverting.

The output stages are disabled (transistors switched off), when the reset signal on RST is active.



The transmit-function has to be enabled via SPI soft reset after an active RST (low). The open-drain outputs are current-limited, in addition the output voltage on Ax (x=1; 2) is monitored for plausibility. If the voltage at Ax still exceeds a certain defined threshold after switch on the output transistor and after a predefined time tvoff, a short- circuit to battery is detected and the stage is turned off.

The output stages can also be diagnosed. The error conditions short-circuit to battery (SCB), short-circuit to ground (SCG) and open-load (OL) are detected. Error detection is done selectively according to the output stage condition: OL and SCG are detected when the output stage is disabled; SCB is detected when the output stage is on. The errors OL, SCB and SCG are filtered.

Parameter	Min	Max	Unit
A1, A2 maximum voltage	-0.6	60	V
A1, A2 nominal output current		50	mA
A1, A2 regulated short circuit current	50	120	mA
A1, A2 on resistance		12	Ω
Switching time E1 to A1, E2 to A2		2	µs

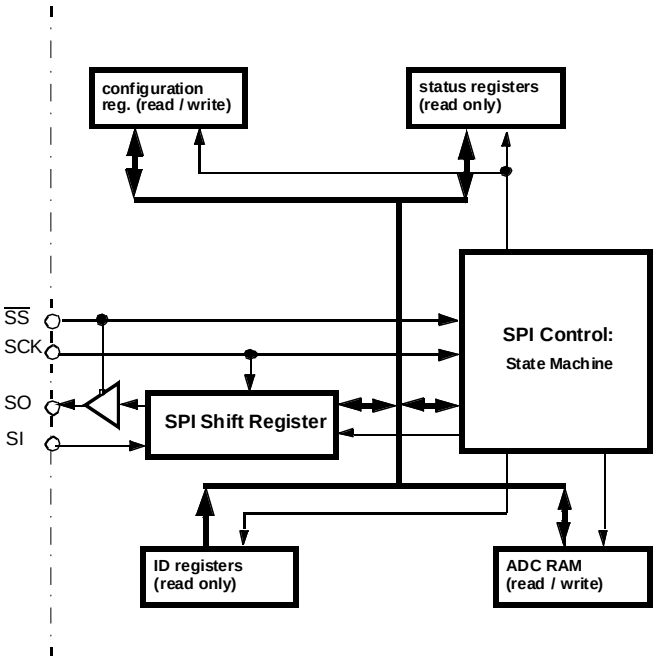
The OL diagnosis can be disabled individually via the SPI interface for each output stage for applications, for which the diagnostic current can disturb (e.g. LEDs). Disable means, zero diagnostic current for OL and deactivated error indication OL.

SPI Interface

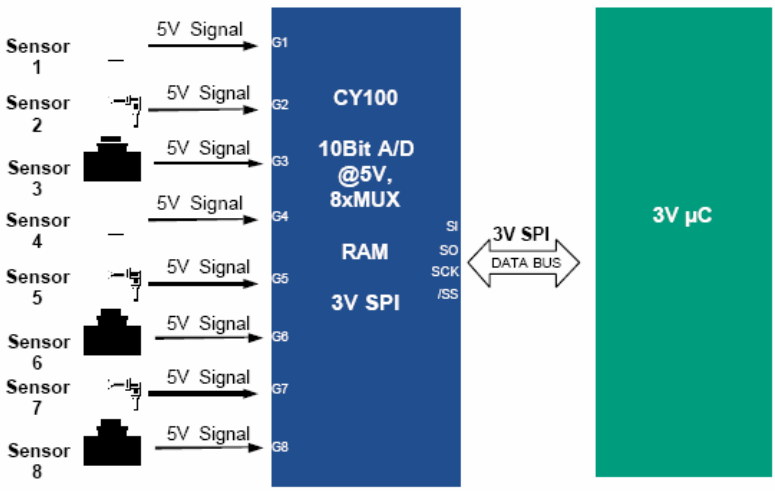
The serial SPI interface establishes a communication link between CY100 and the systems microcontroller. The CY100 always operates in slave mode whereas the controller provides the master function. The maximum baud rate is 2 MBaud.

Applying an active slave select signal at SS CY100 is selected by the SPI master. SI is the slave in data input, SO the slave out data output. Via the serial clock input SCK the SPI clock is provided by the SPI master. In case of inactive slave select signal (high) or active reset the data output SO is high impedance (tistate).

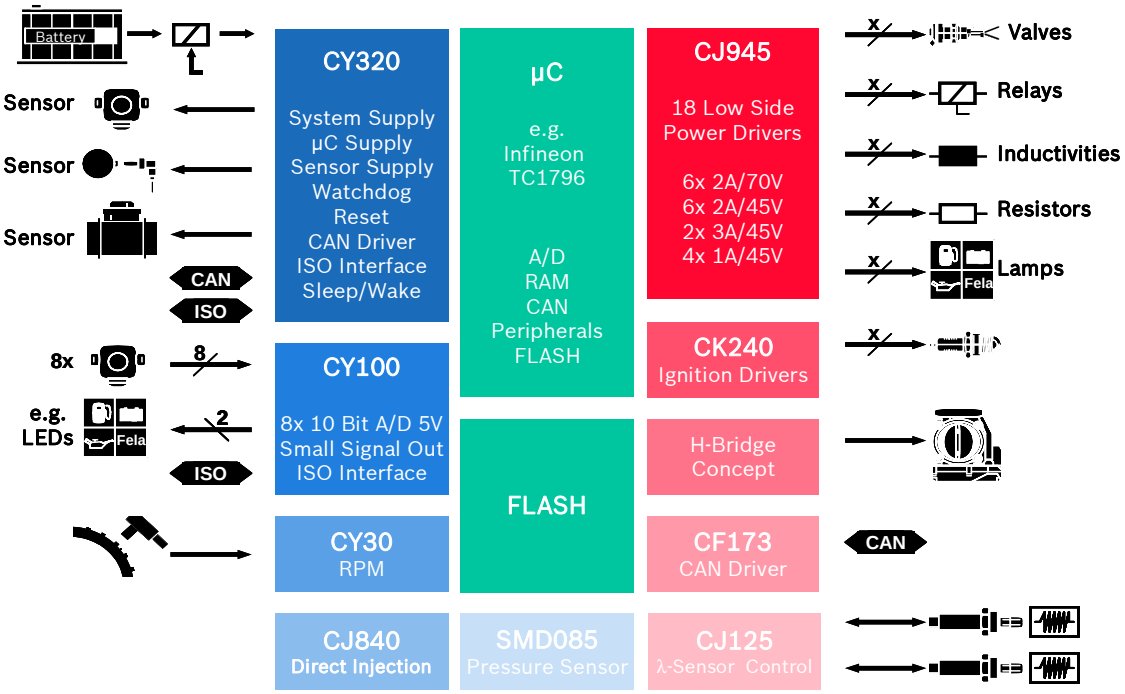
The first two bits of an instruction are used to realize an extended device-addressing. This gives the opportunity to operate up to 4 slave-devices sharing one common SS signal from the master-unit.



System application example



Chipset



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