ESCOLA POLITÉCNICA DA
UNIVERSIDADE DE SÃO PAULO
Departamento de Engenharia de Sistemas Eletrônicos
PSI - EPUSP

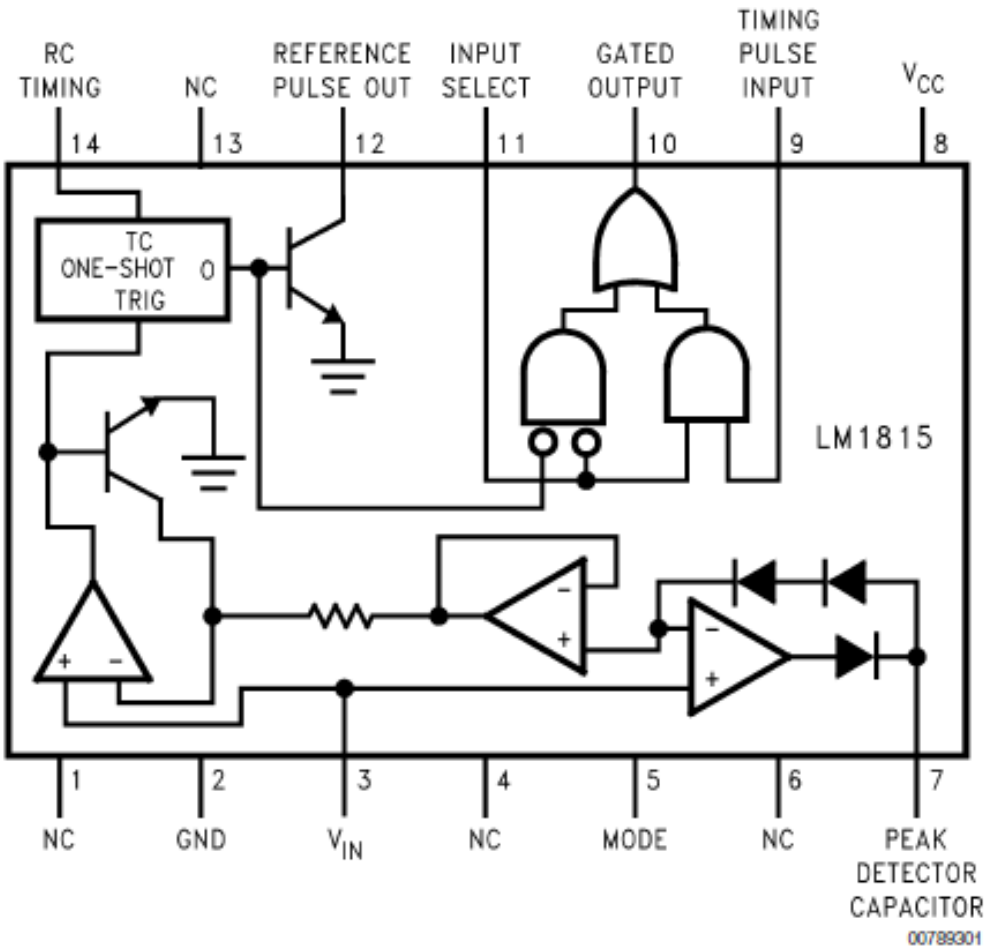
PSI 2618
CIRCUITOS ELÉTRONICOS AUTOMOTIVOS

Circuitos Integrados de Interface

Prof. Armando Laganá

LM1815

Connection Diagram



Top View
Order Number LM1815M or LM1815N
See NS Package Number M14A or N14A

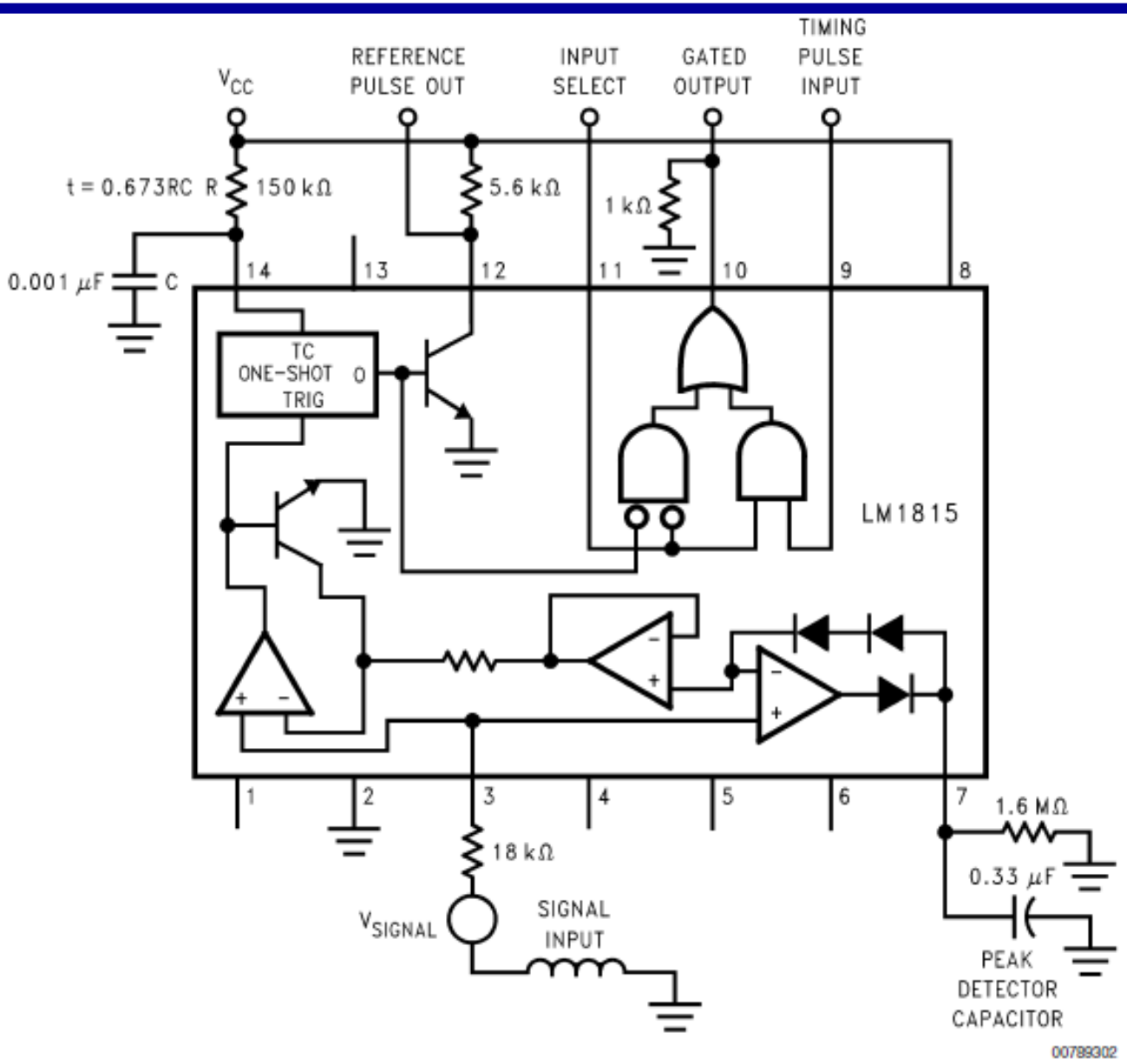


FIGURE 1. LM1815 Adaptive Sense Amplifier

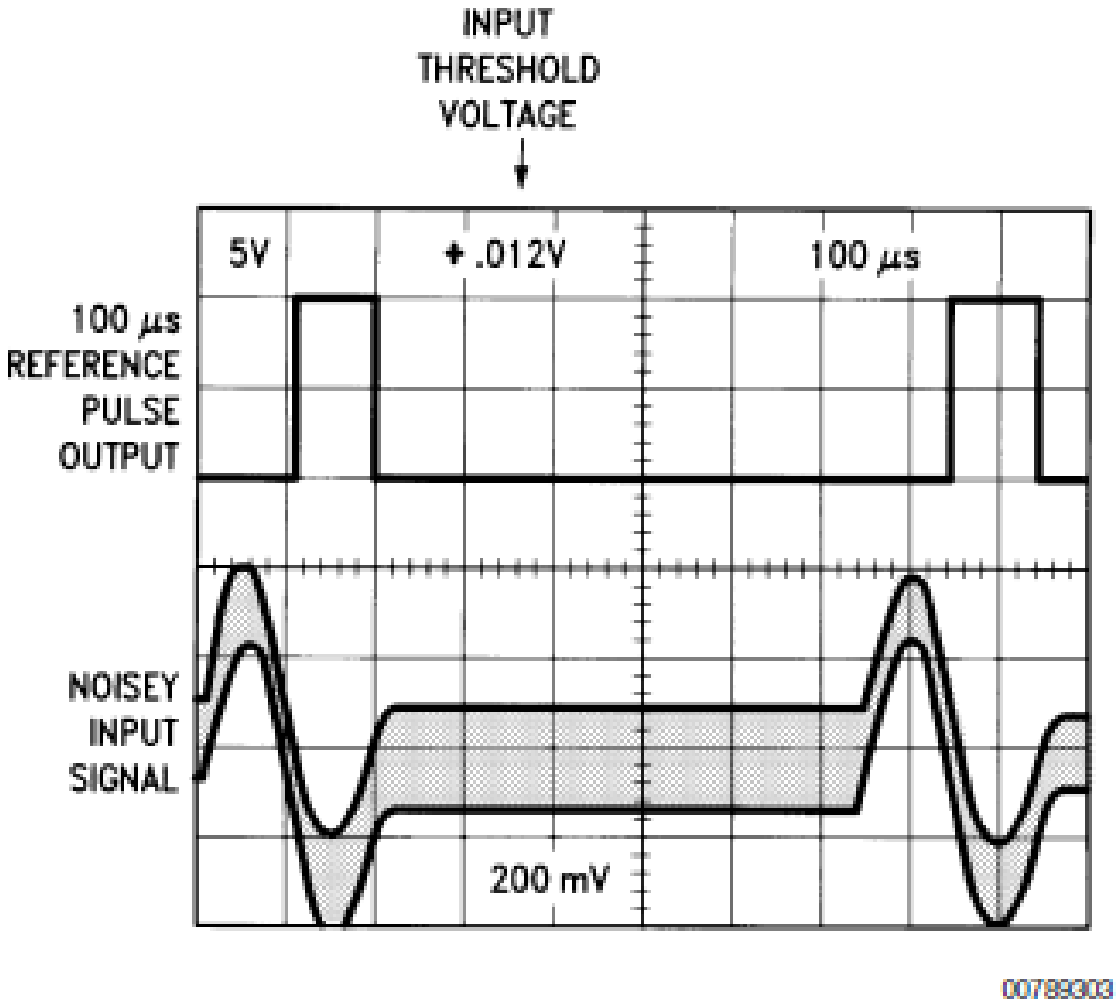
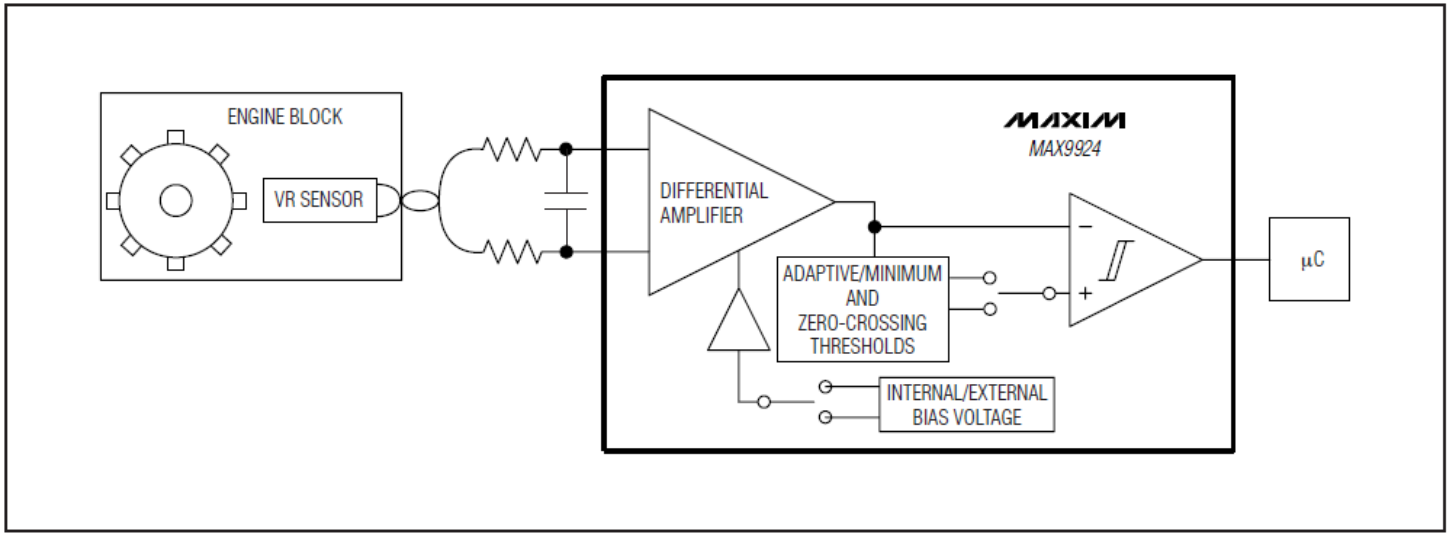


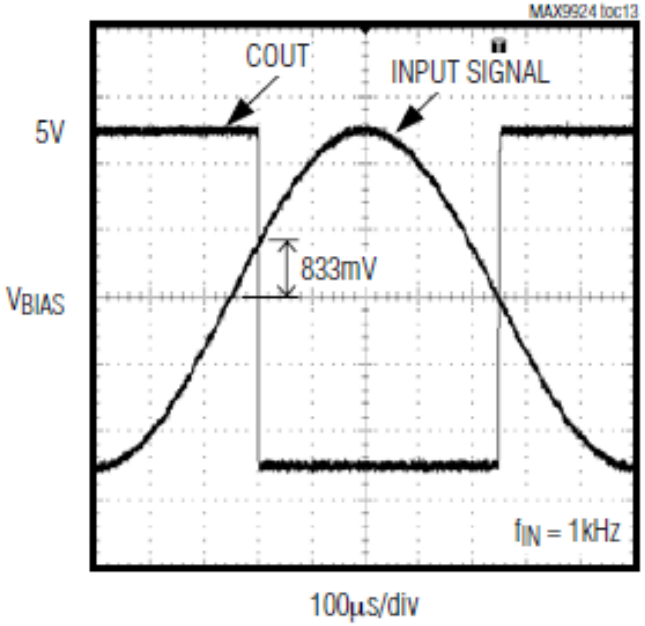
FIGURE 2. LM1815 Oscillograms

Variable Reluctance Sensor Interfaces with Differential Input and Adaptive Peak Threshold

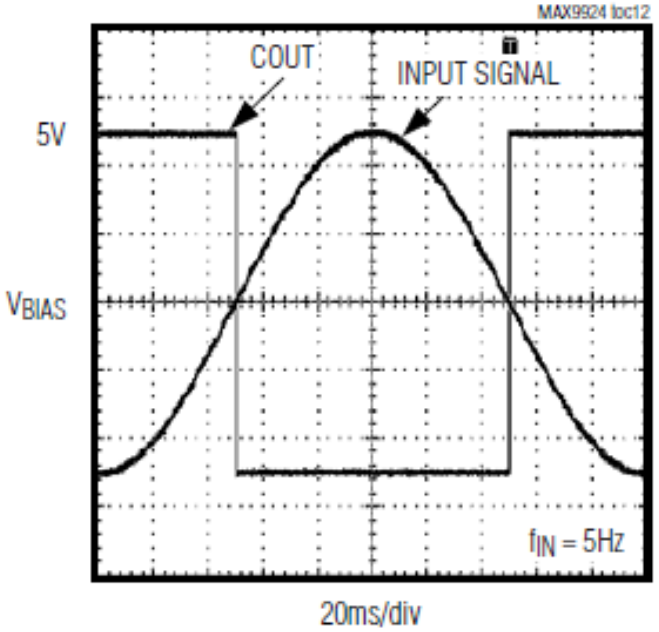
MAX9924–MAX9927



INPUT SIGNAL vs. COUT WITH WATCHDOG TIMER EXPIRED



INPUT SIGNAL vs. COUT WITH WATCHDOG TIMER EXPIRED

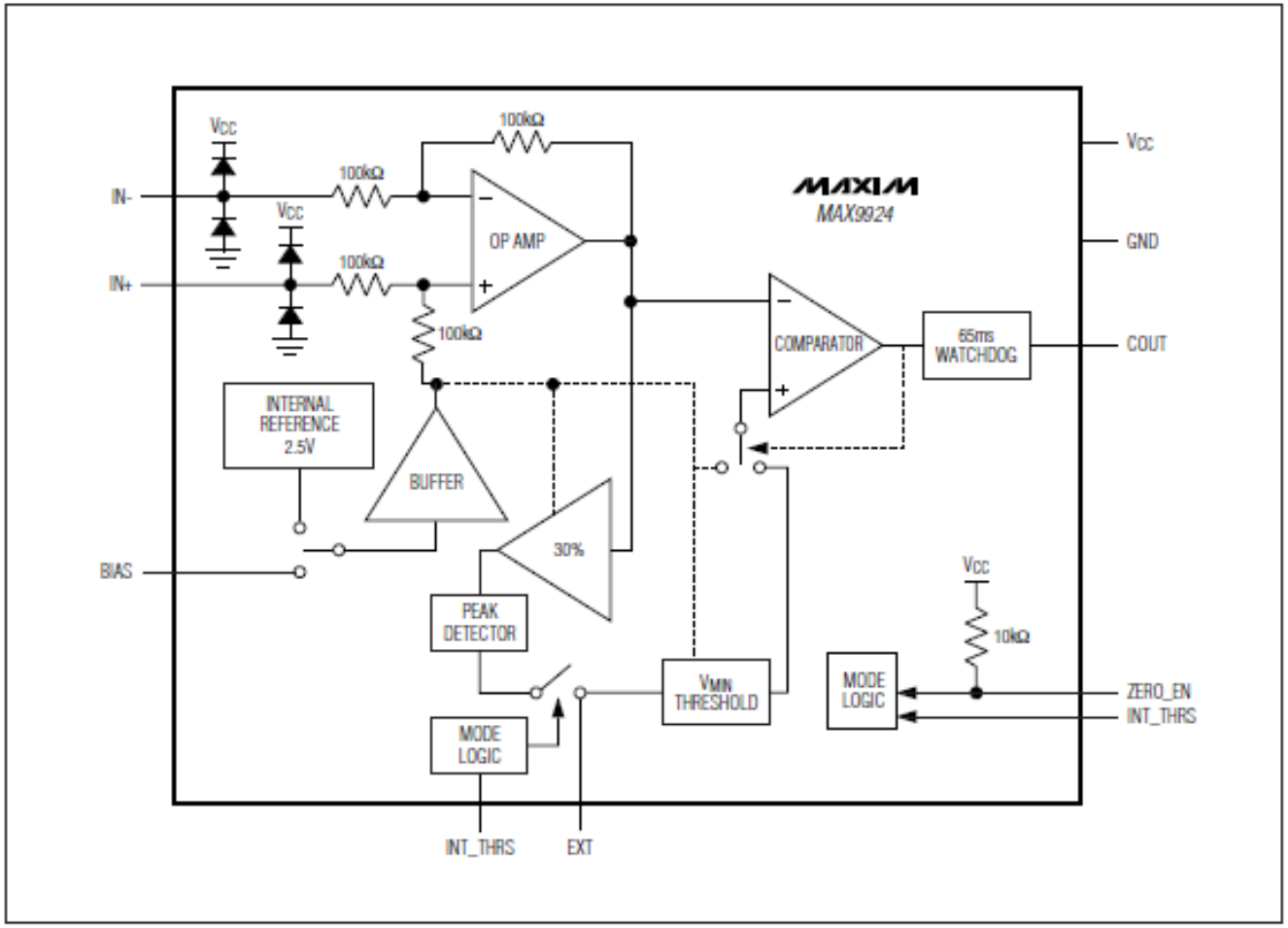


Pin Description

PIN				NAME	FUNCTION
MAX9924	MAX9925	MAX9926	MAX9927		
1	1	—	—	IN+	Noninverting Input
2	2	—	—	IN-	Inverting Input
—	3	—	—	OUT	Amplifier Output
3	—	—	—	N.C.	No Connection. Not internally connected.
4	4	—	—	BIAS	Input Bias. Connect to an external resistor-divider and bypass to ground with a 0.1µF and 10µF capacitor.
5	5	11	11	GND	Ground
6	6	13	—	ZERO_EN	Zero-Crossing Enable. Mode configuration pin, internally pulled up to V_{CC} with 10kΩ resistor.
7	7	—	—	COUT	Comparator Output. Open-drain output, connect a 10kΩ pullup resistor from COUT to V_{PULLUP}.
8	8	—	—	EXT	External Reference Input. Leave EXT unconnected in Modes A1, A2. Apply an external voltage in Modes B, C.
9	9	—	—	INT_THRS	Internal Adaptive Threshold. Mode configuration pin.
10	10	14	14	V_{CC}	Power Supply
—	—	1	1	INT_THRS1	Internal Adaptive Threshold 1. Mode configuration pin.
—	—	2	2	EXT1	External Reference Input 1. Leave EXT unconnected in Modes A1, A2. Apply an external voltage in Modes B, C.
—	—	3	3	BIAS1	Input Bias 1. Connect to an external resistor-divider and bypass to ground with a 0.1µF and 10µF capacitor.
—	—	4	4	COUT1	Comparator Output 1. Open-drain output, connect a 10kΩ pullup resistor from COUT1 to V_{PULLUP}.
—	—	5	5	COUT2	Comparator Output 2. Open-drain output, connect a 10kΩ pullup resistor from COUT2 to V_{PULLUP}.
—	—	6	6	BIAS2	Input Bias 2. Connect to an external resistor-divider and bypass to ground with a 0.1µF and 10µF capacitor.
—	—	7	7	EXT2	External Reference Input 2. Leave EXT unconnected in Modes A1, A2. Apply an external voltage in Modes B, C.
—	—	8	8	INT_THRS2	Internal Adaptive Threshold 2. Mode configuration pin.
—	—	9	9	IN2+	Noninverting Input 2
—	—	10	10	IN2-	Inverting Input 2
—	—	12	—	DIRN	Rotational Direction Output. Open-drain output, connect a pullup resistor from DIRN to V_{PULLUP}.
—	—	—	12	OUT2	Amplifier Output 2
—	—	—	13	OUT1	Amplifier Output 1
—	—	15	15	IN1-	Noninverting Input 1
—	—	16	16	IN1+	Inverting Input 1

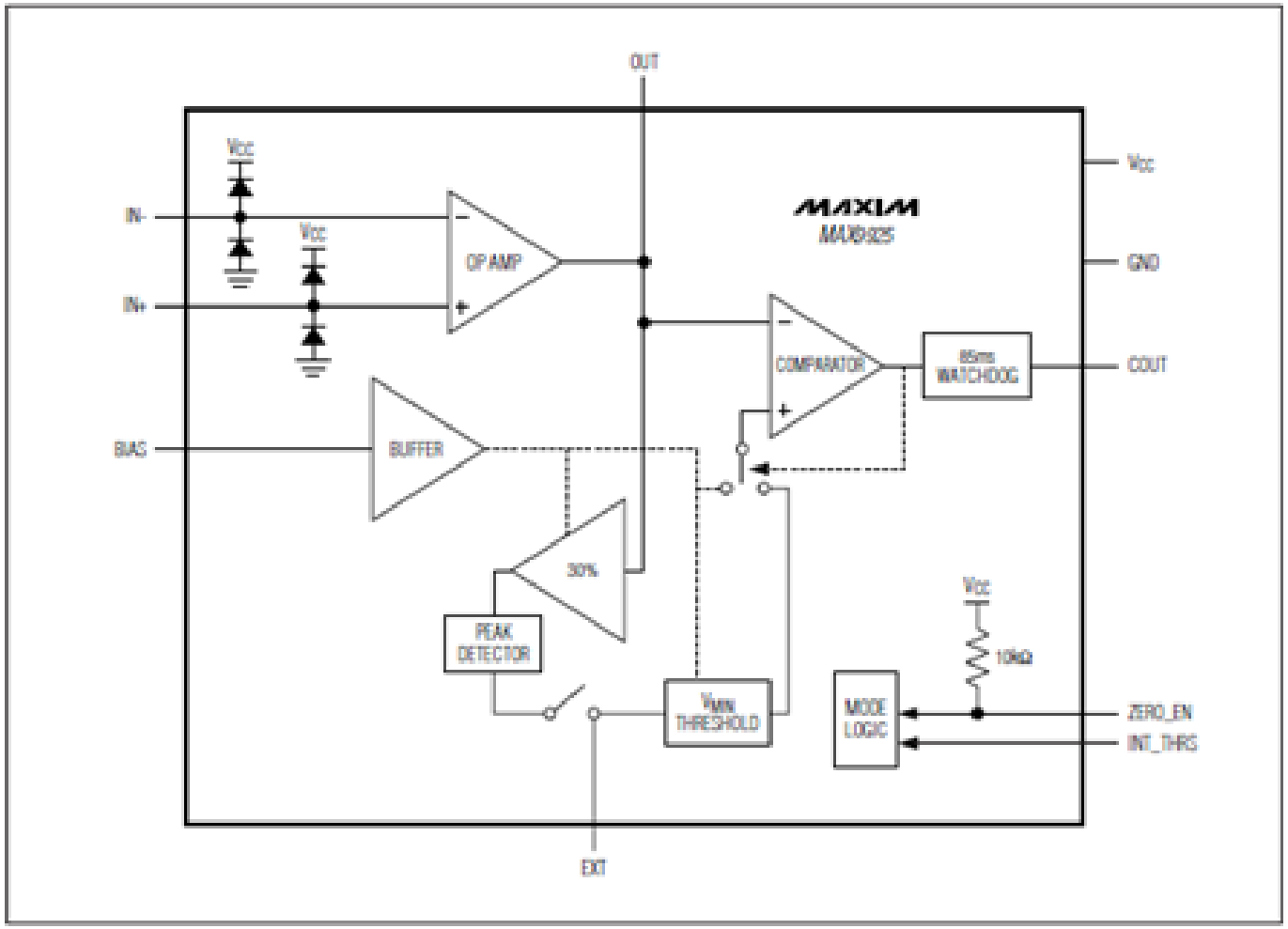
Variable Reluctance Sensor Interfaces with Differential Input and Adaptive Peak Threshold

Functional Diagrams



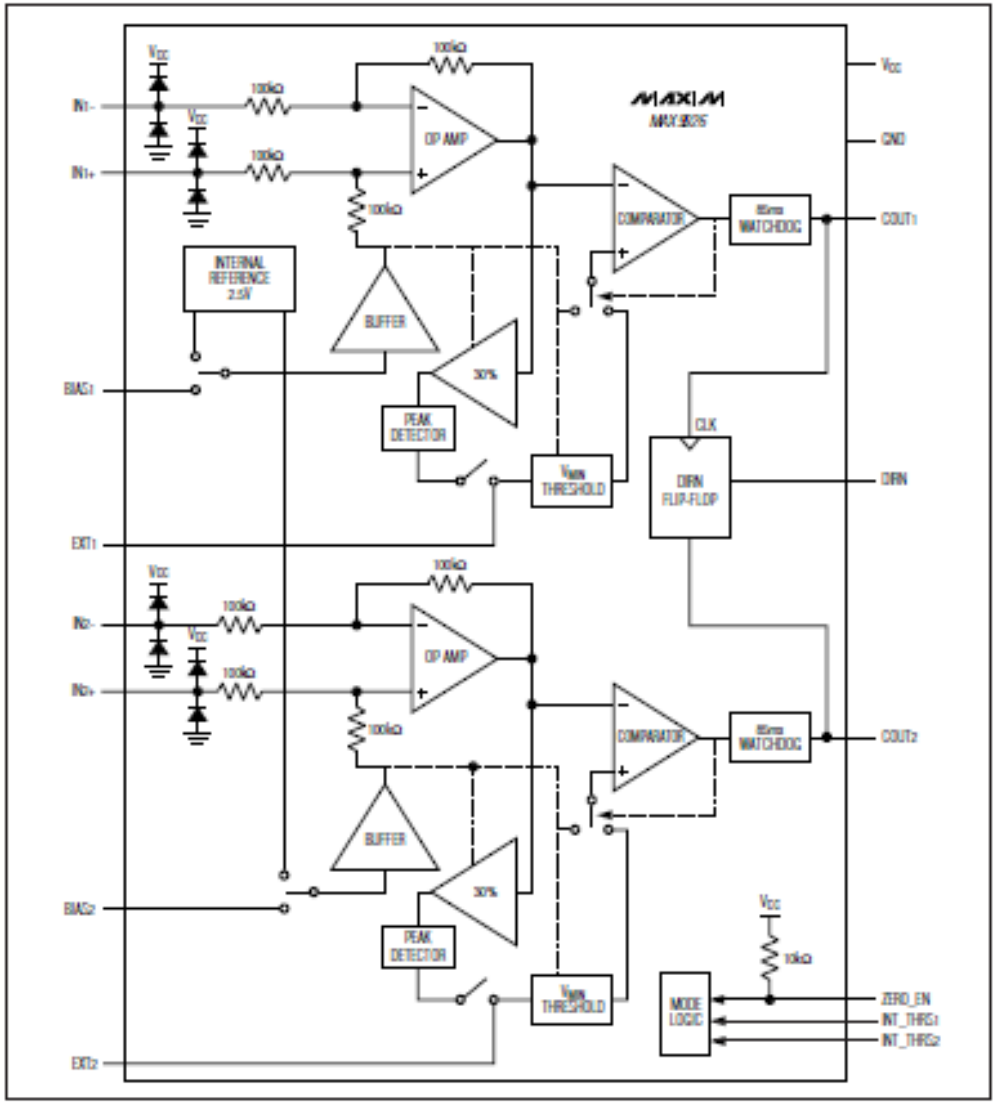
Variable Reluctance Sensor Interfaces with Differential Input and Adaptive Peak Threshold

Functional Diagrams (continued)

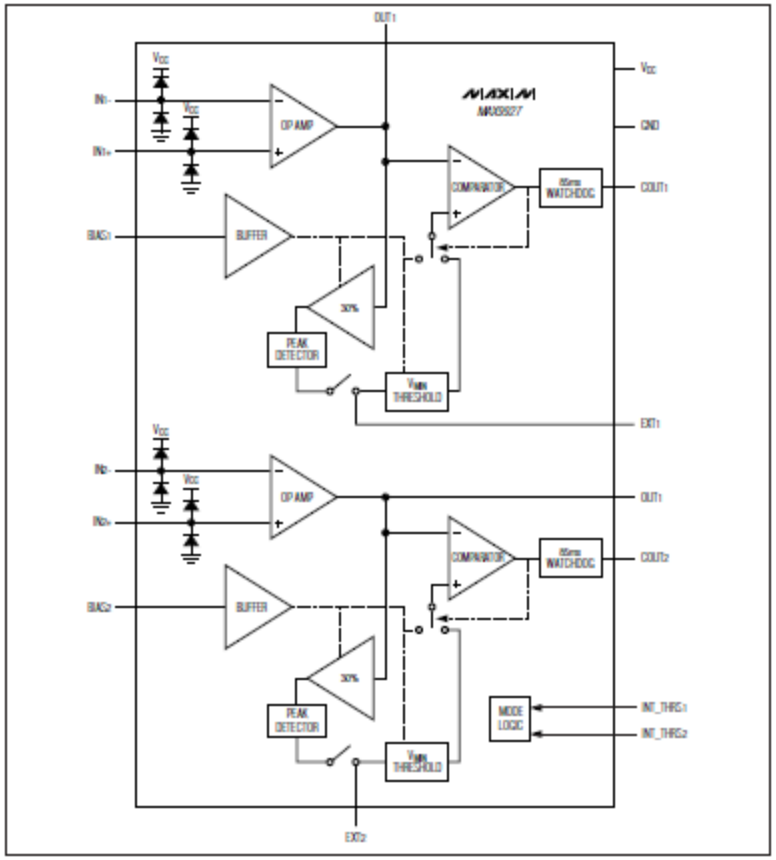


Variable Reluctance Sensor Interfaces with Differential Input and Adaptive Peak Threshold

Functional Diagrams (continued)



Functional Diagrams (continued)



internal comparator produces output pulses by compar

Table 1. MAX9924/MAX9926 Operating Modes

OPERATING MODE	SETTING		DEVICE FUNCTIONALITY		
	ZERO_EN	INT_THRS	ZERO CROSSING	ADAPTIVE PEAK THRESHOLD	BIAS VOLTAGE SOURCE
A1	VCC	VCC	Enabled	Enabled	External
A2	GND	GND	Enabled	Enabled	Internal Ref
B	VCC	GND	Enabled	Disabled	External
C	GND	VCC	Disabled	Disabled	External

Table 2. MAX9925 Operating Modes

OPERATING MODE	SETTING		DEVICE FUNCTIONALITY	
	ZERO_EN	INT_THRS	ZERO CROSSING	ADAPTIVE PEAK THRESHOLD
A1	VCC	VCC	Enabled	Enabled
B	VCC	GND	Enabled	Disabled
C	GND	VCC	Disabled	Disabled

Table 3. MAX9927 Operating Modes

OPERATING MODE	SETTING	DEVICE FUNCTIONALITY	
	INT_THRS	ZERO CROSSING	ADAPTIVE PEAK THRESHOLD
A1	VCC	Enabled	Enabled
B	GND	Enabled	Disabled

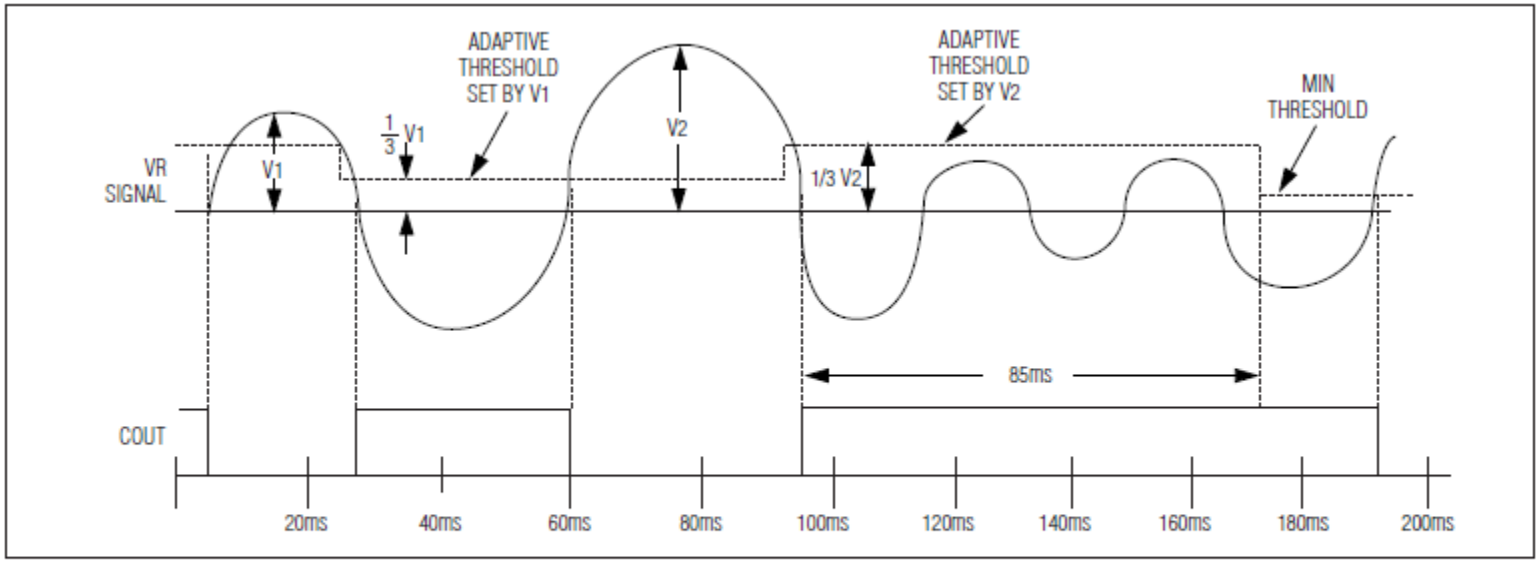


Figure 1. Adaptive Peak Threshold Operation

$$V_{TH} = \left(\frac{R1(V_{PULLUP} - V_{BIAS})}{R1 + R2 + R_{PULLUP}} \right) + V_{BIAS}$$

$$V_{TL} = \left(\frac{R2}{R1 + R2} \right) \times V_{BIAS}$$

Variable Reluctance Sensor Interfaces with Differential Input and Adaptive Peak Threshold

Application Circuits

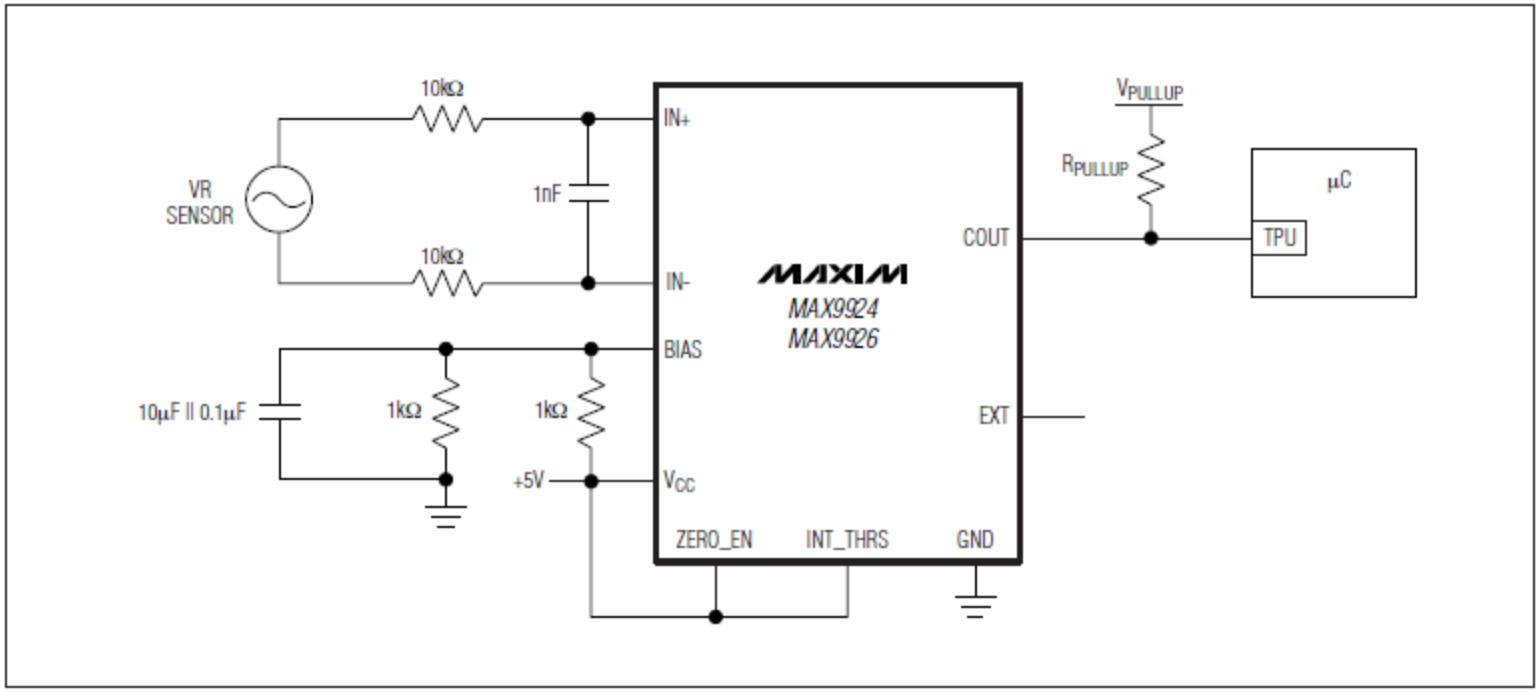


Figure 2. MAX9924/MAX9926 Operating Mode A1

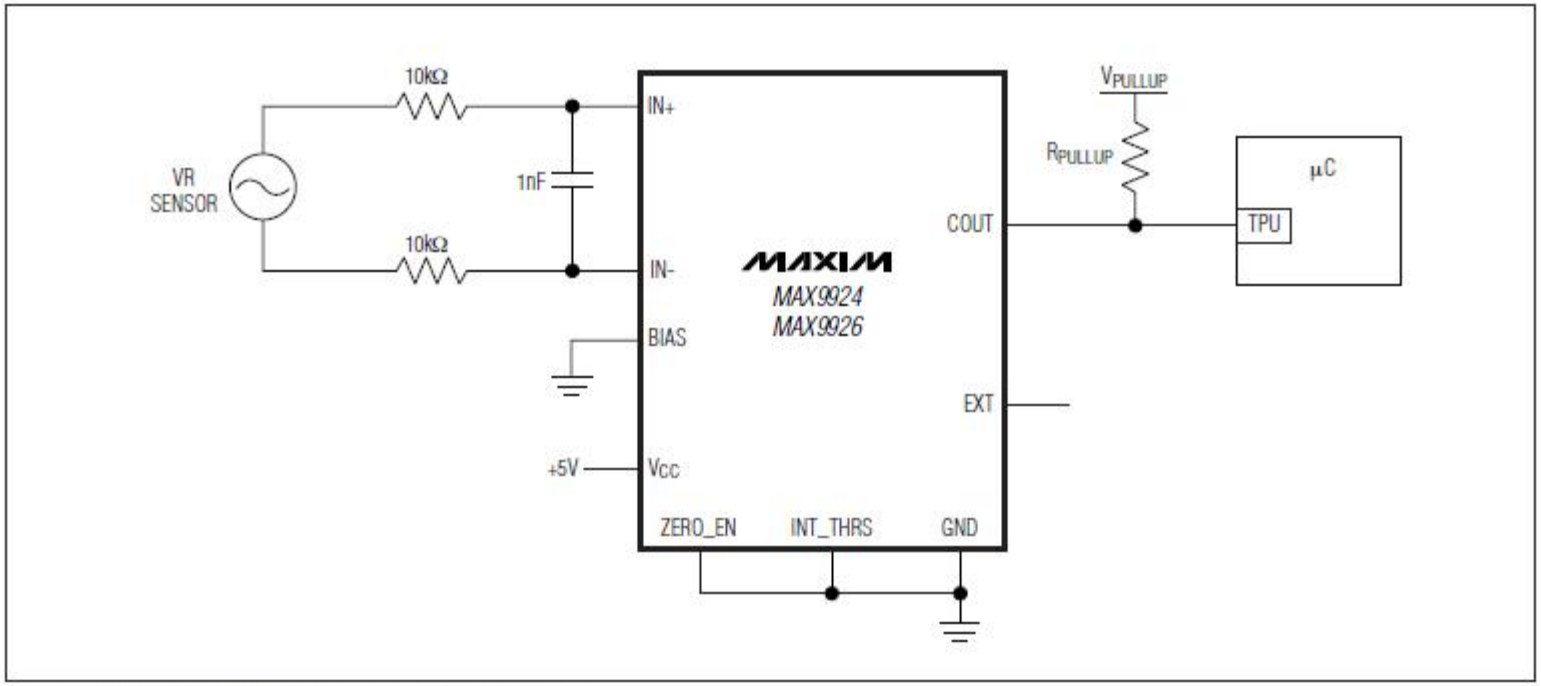


Figure 3. MAX9924/MAX9926 Operating Mode A2

Application Circuits (continued)

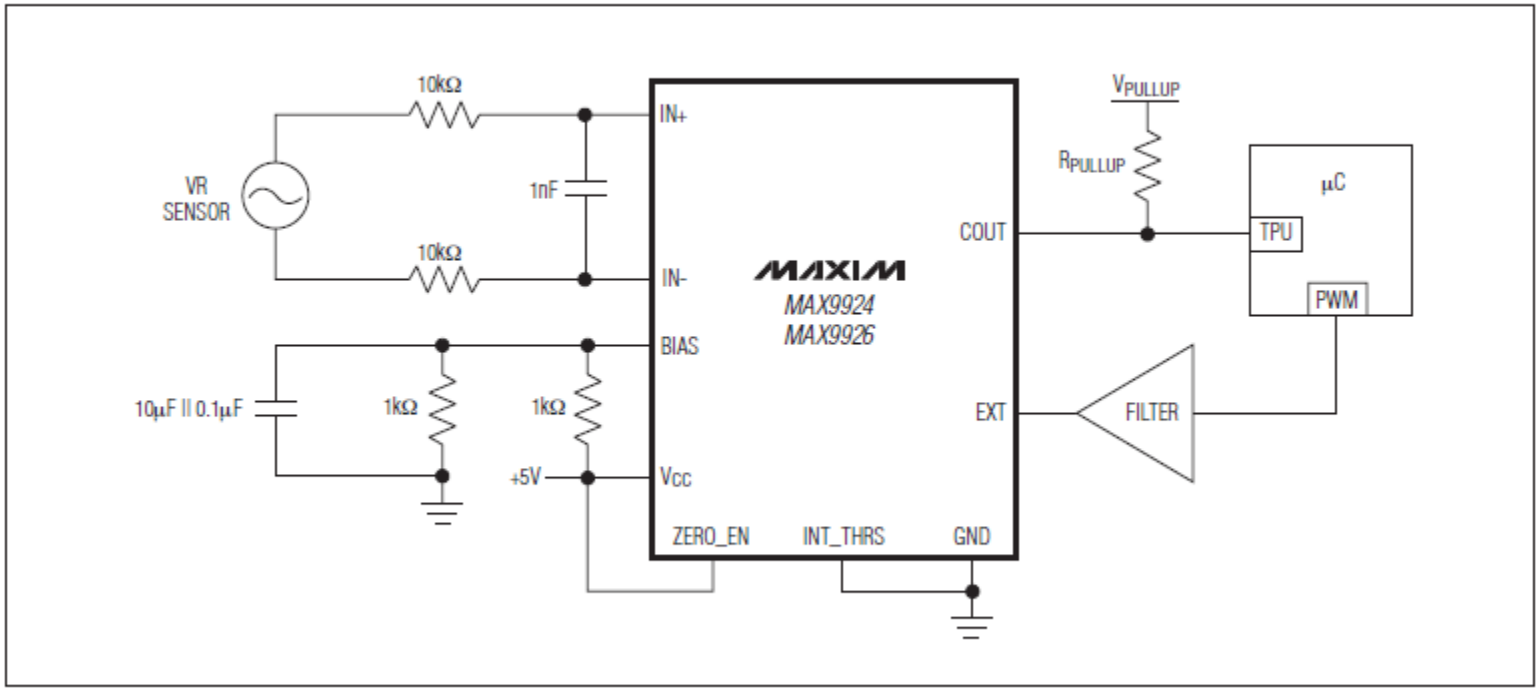


Figure 4. MAX9924/MAX9926 Operating Mode B

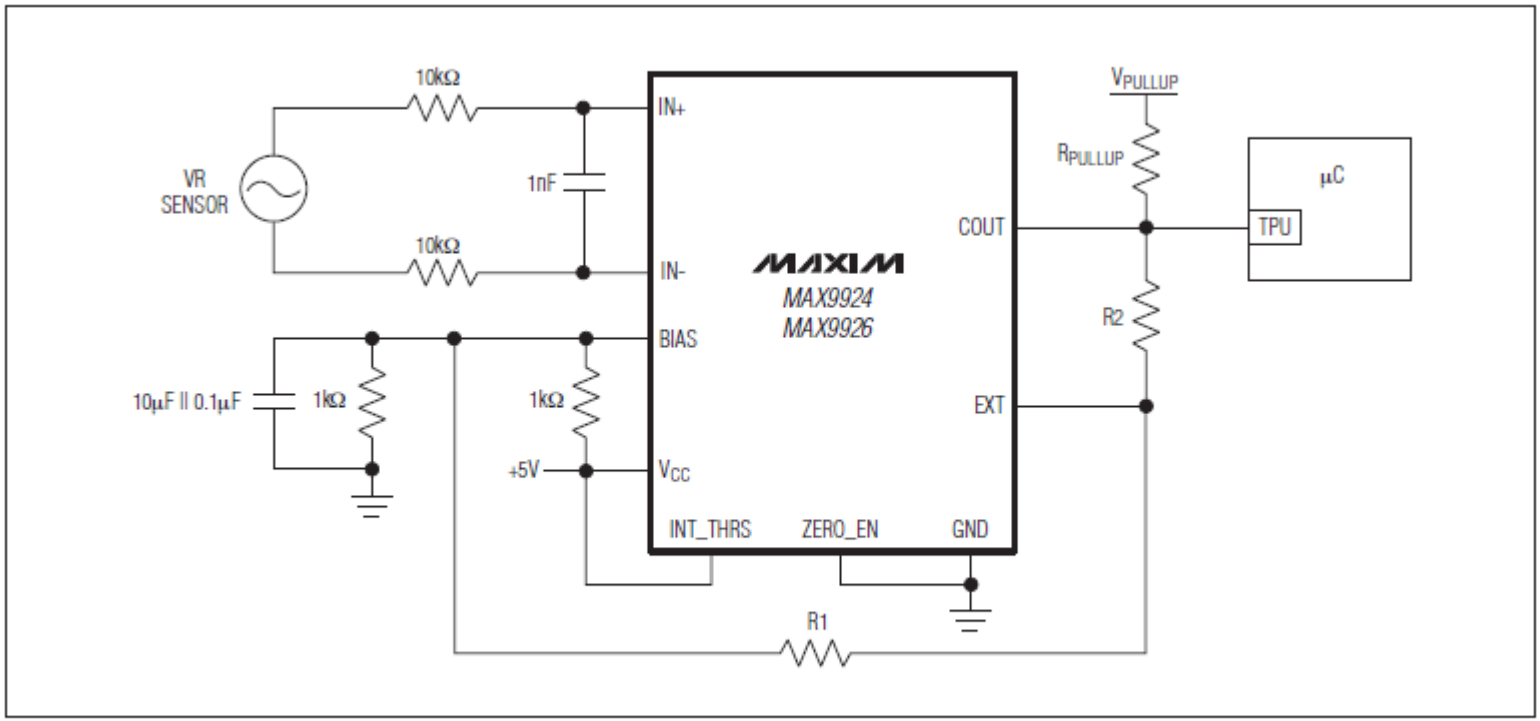


Figure 5. MAX9924/MAX9926 Operating Mode C

Application Circuits (continued)

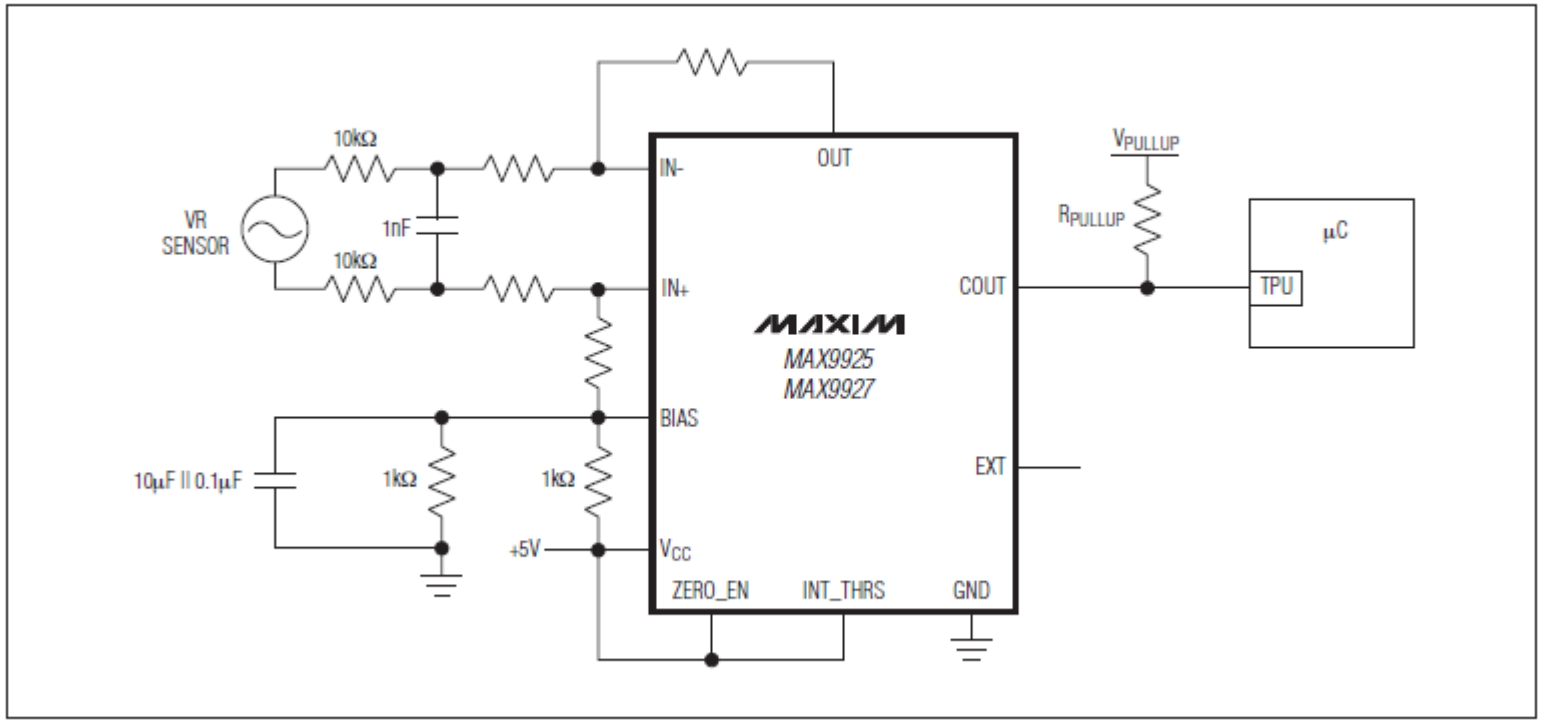


Figure 6. MAX9925/MAX9927 Operating Mode A

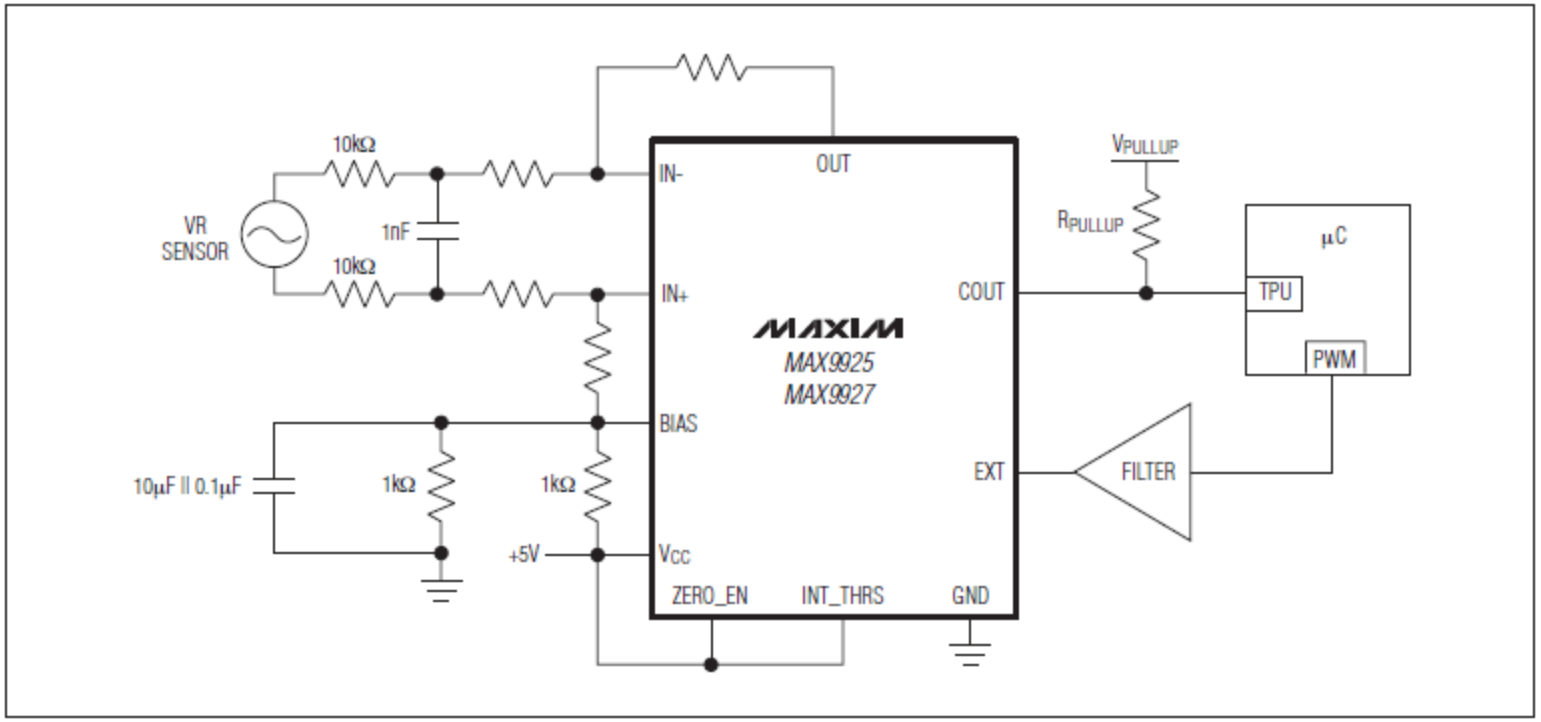


Figure 7. MAX9925/MAX9927 Operating Mode B

Application Circuits (continued)

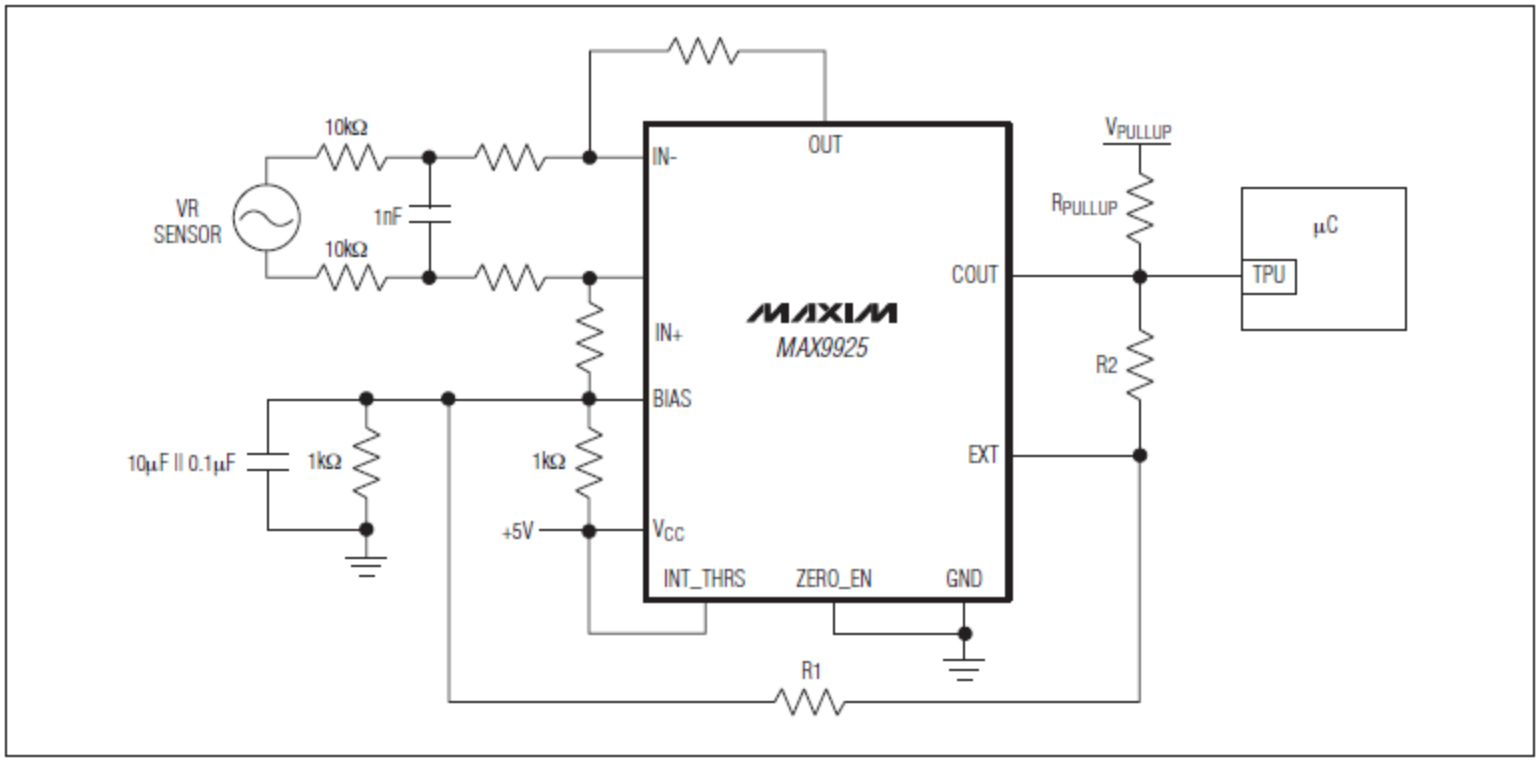
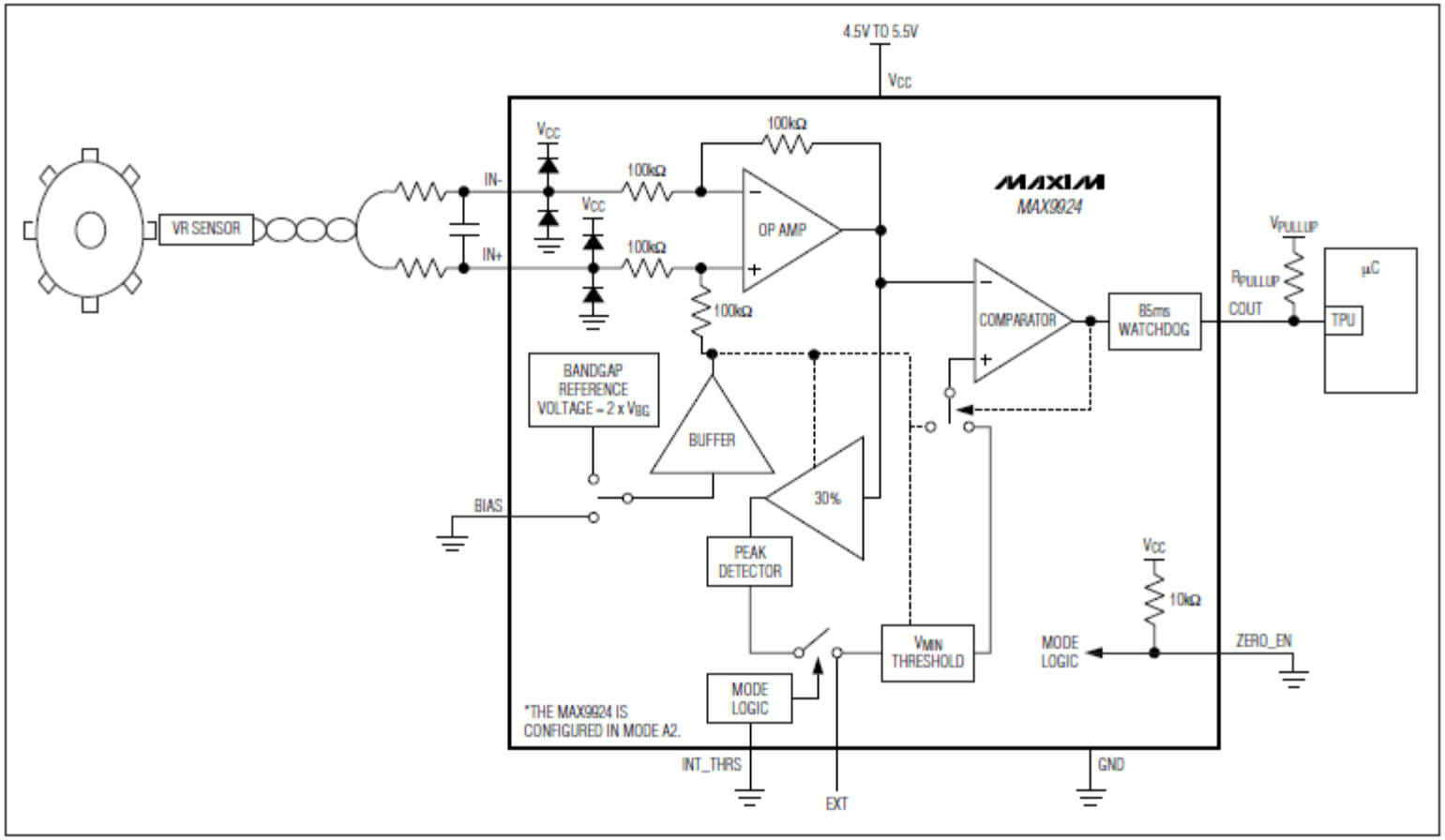


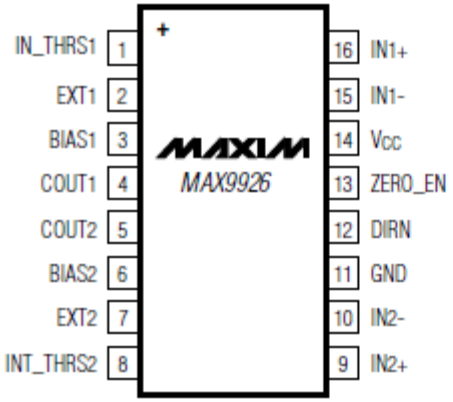
Figure 8. MAX9925 Operating Mode C

Typical Operating Circuit

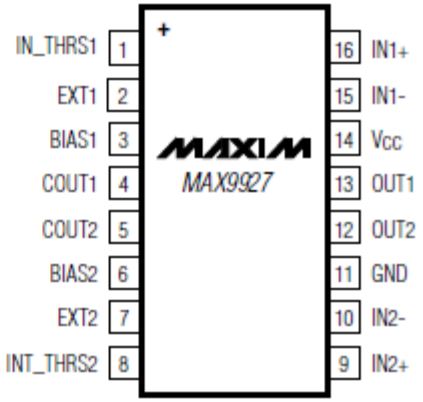


Pin Configurations

TOP VIEW

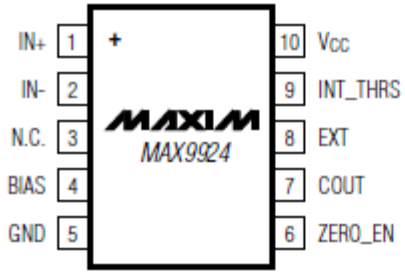


QSOP

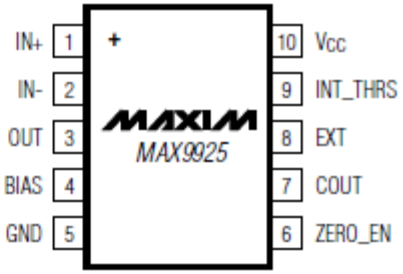


QSOP

TOP VIEW

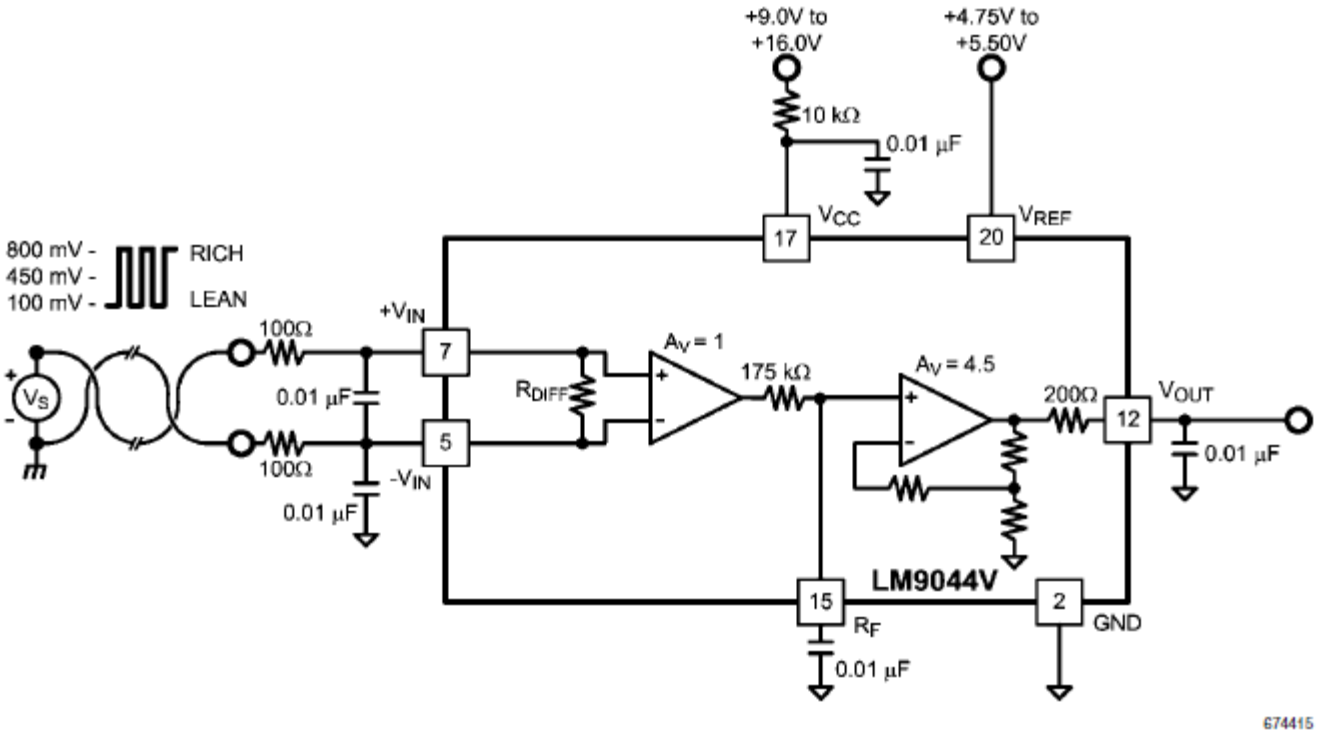


µMAX

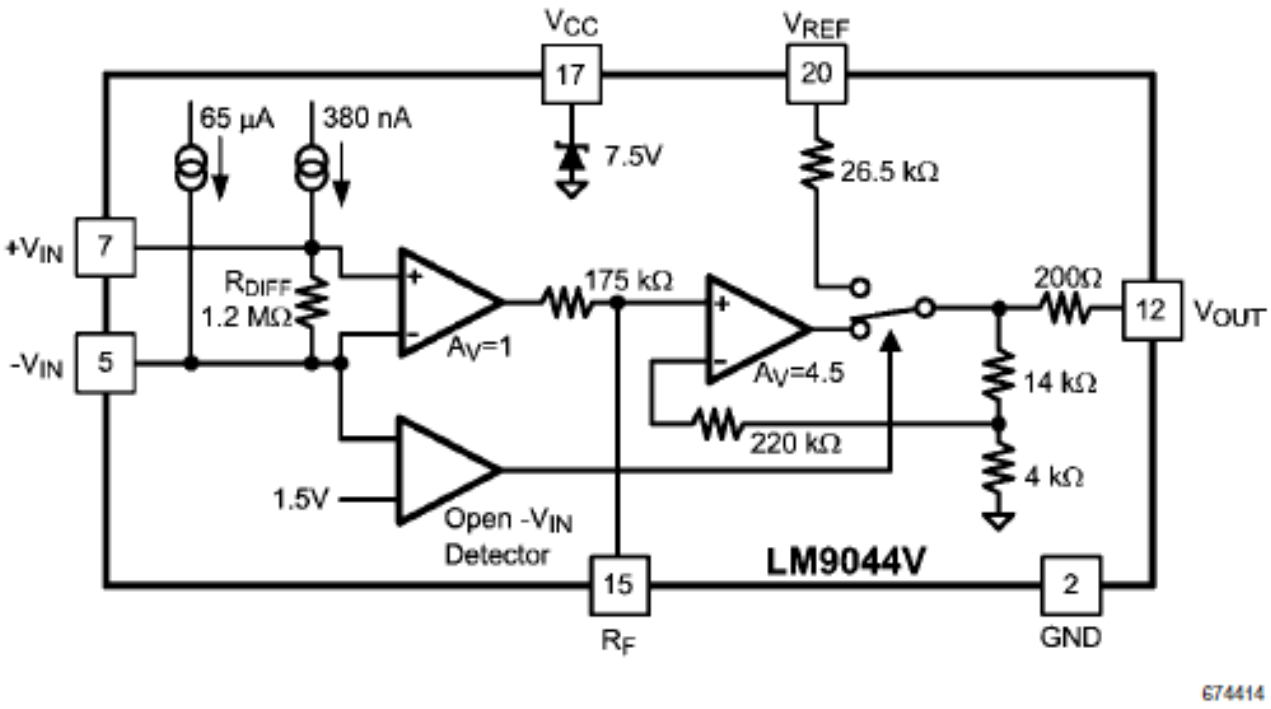


µMAX

LM9044


+9.0V to
+16.0V
+4.75V to
+5.50V
10 kΩ
0.01 µF
17
VCC
20
VREF
800 mV -
450 mV -
100 mV -
RICH
LEAN
100Ω
+VIN
7
AV = 1
175 kΩ
AV = 4.5
200Ω
12
VOUT
0.01 µF
VS
0.01 µF
RDIFF
5
100Ω
-VIN
0.01 µF
LM9044V
15
RF
0.01 µF
2
GND
674415

Block Diagram



MC33975

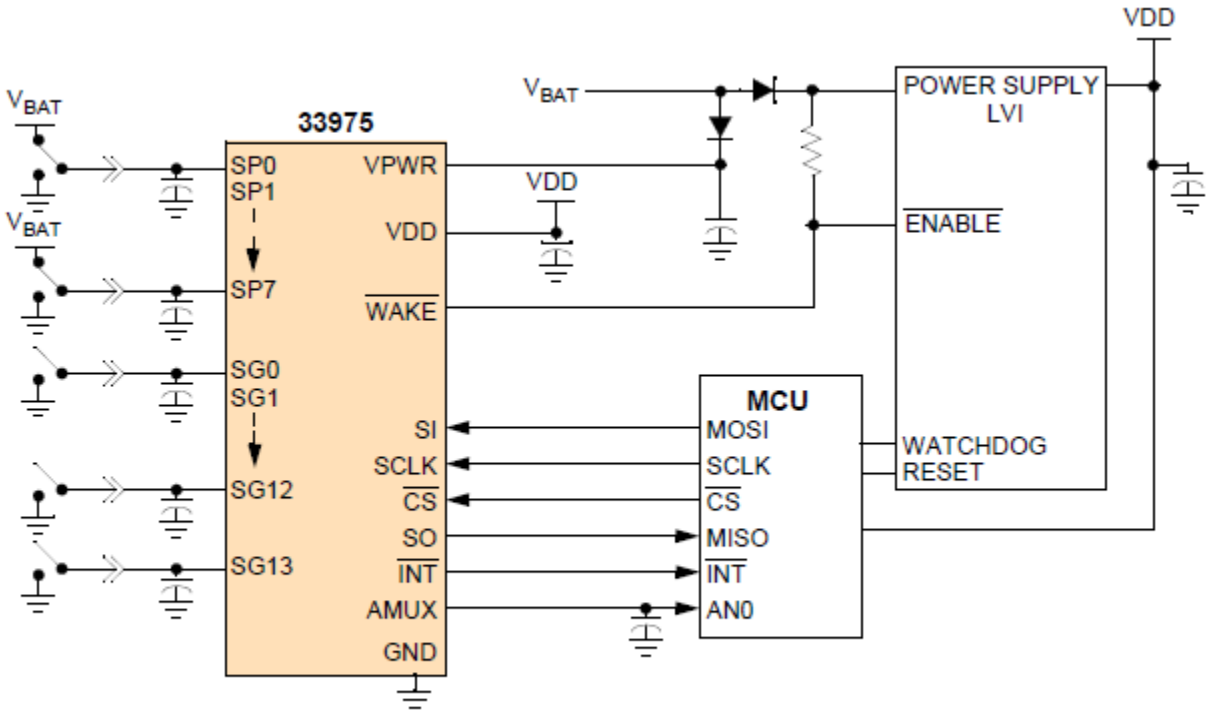
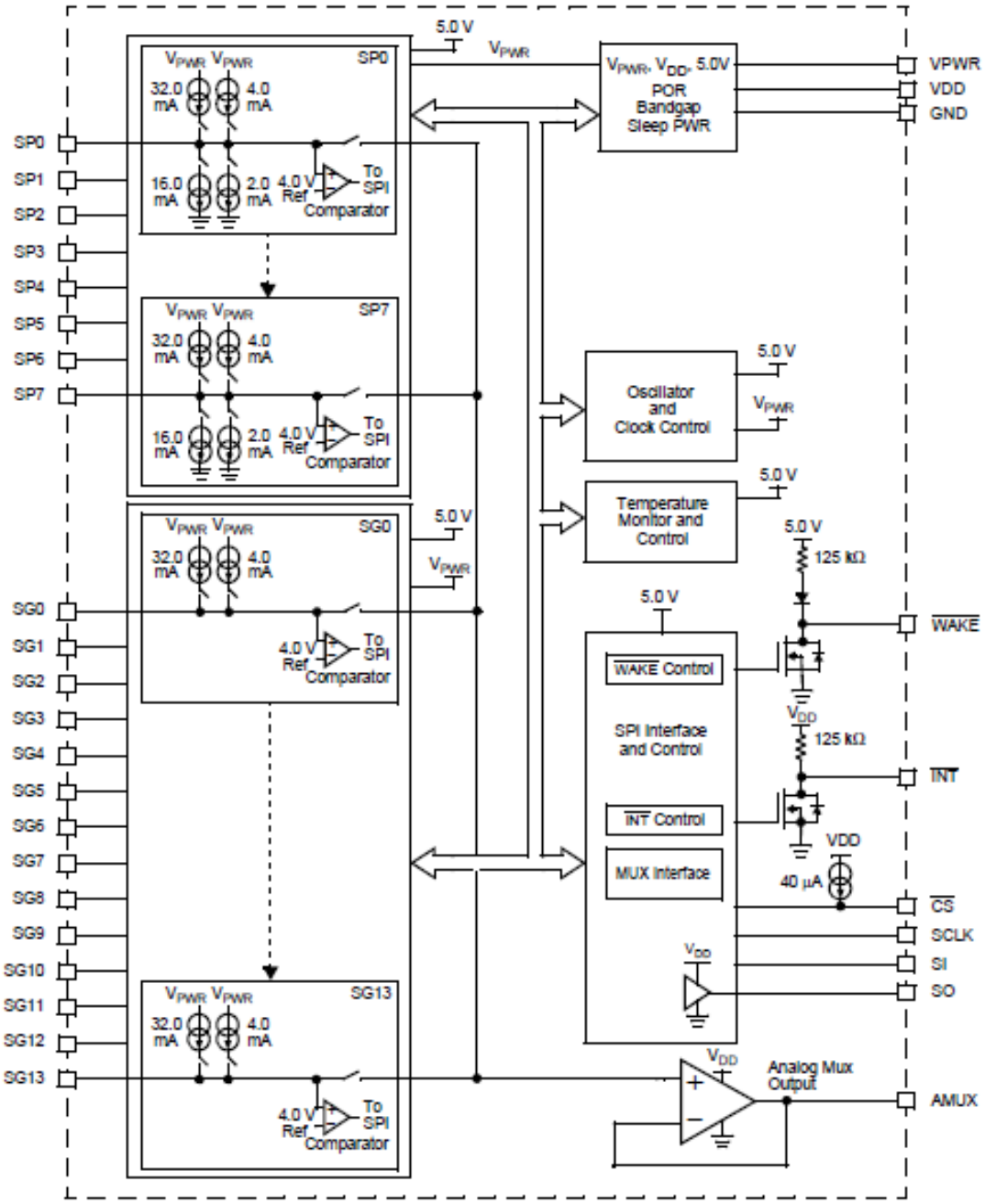
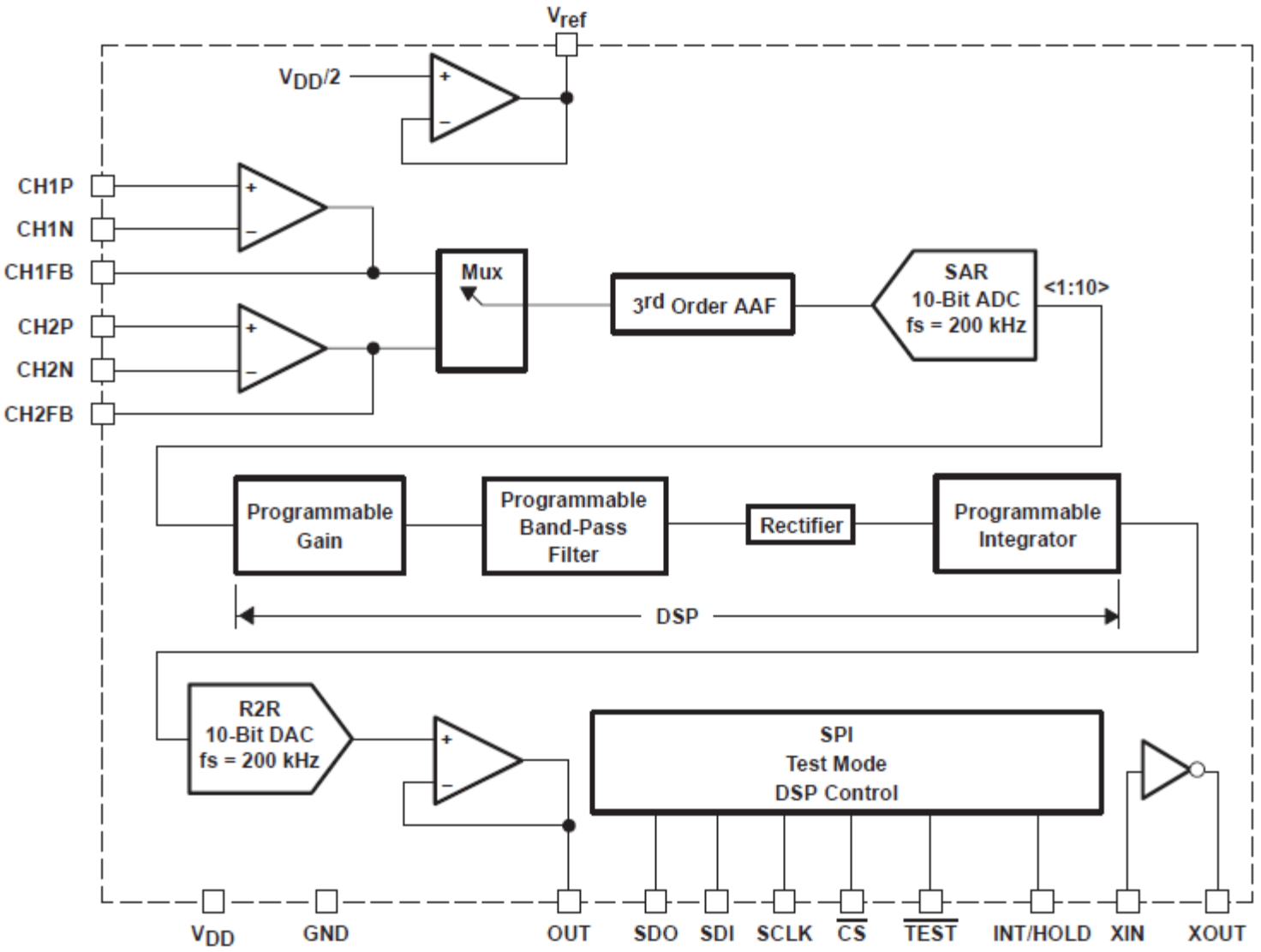


Figure 1. 33975 Simplified Application Diagram


SP0
SP1
SP2
SP3
SP4
SP5
SP6
SP7
SG0
SG1
SG2
SG3
SG4
SG5
SG6
SG7
SG8
SG9
SG10
SG11
SG12
SG13
5.0 V
VPWR
VPWR, VDD, 5.0V
POR
Bandgap
Sleep PWR
VPWR
VDD
GND
VPWR VPWR
SP0
32.0 mA
4.0 mA
16.0 mA
2.0 mA
4.0 V Ref
To SPI
Comparator
SP7
SG0
SG13
Oscillator and Clock Control
Temperature Monitor and Control
125 kΩ
WAKE
WAKE Control
SPI Interface and Control
INT
INT Control
MUX Interface
40 µA
CS
SCLK
SI
SO
Analog Mux Output
AMUX

TPIC8101
KNOCK SENSOR INTERFACE

functional block diagram



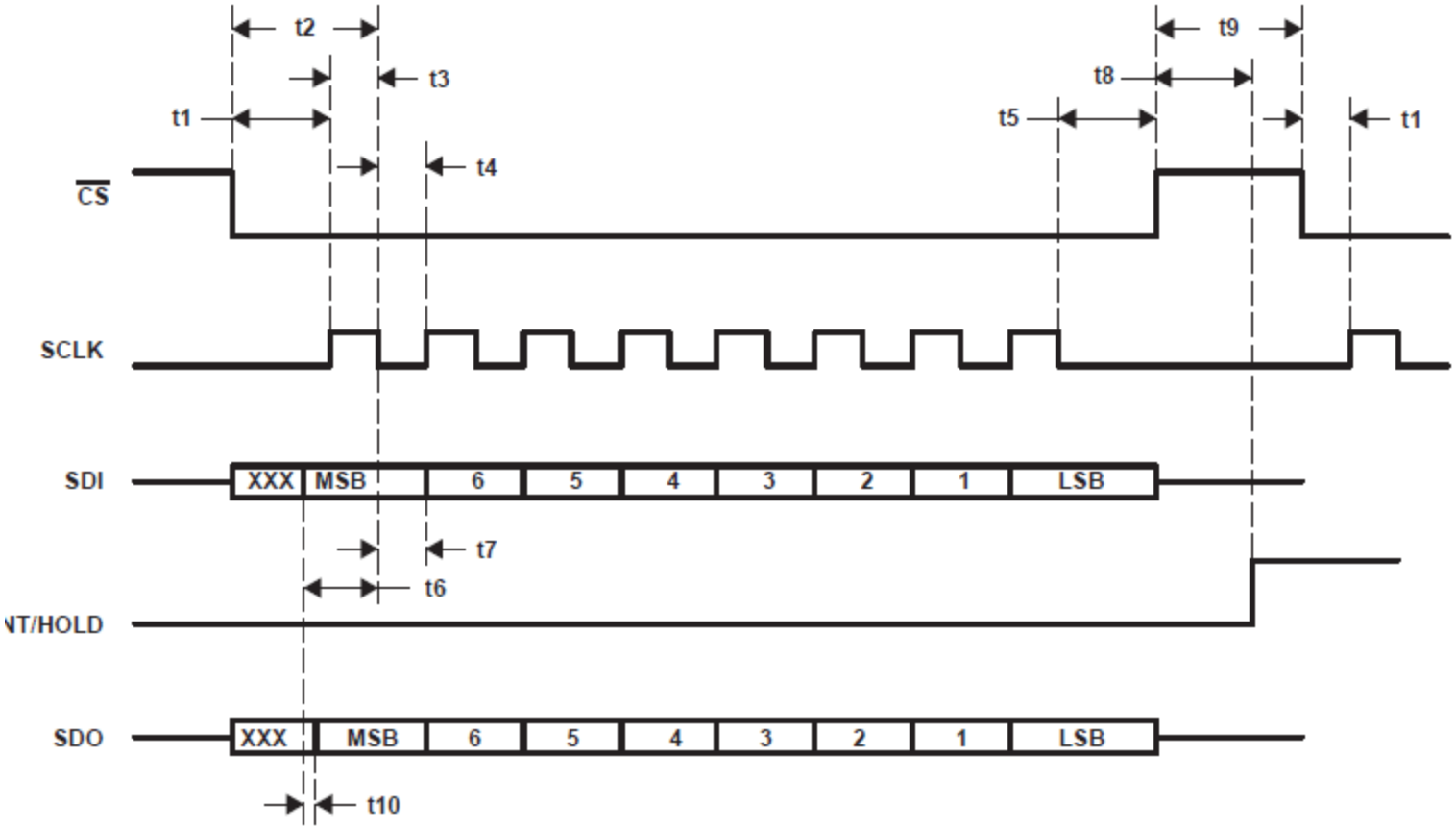
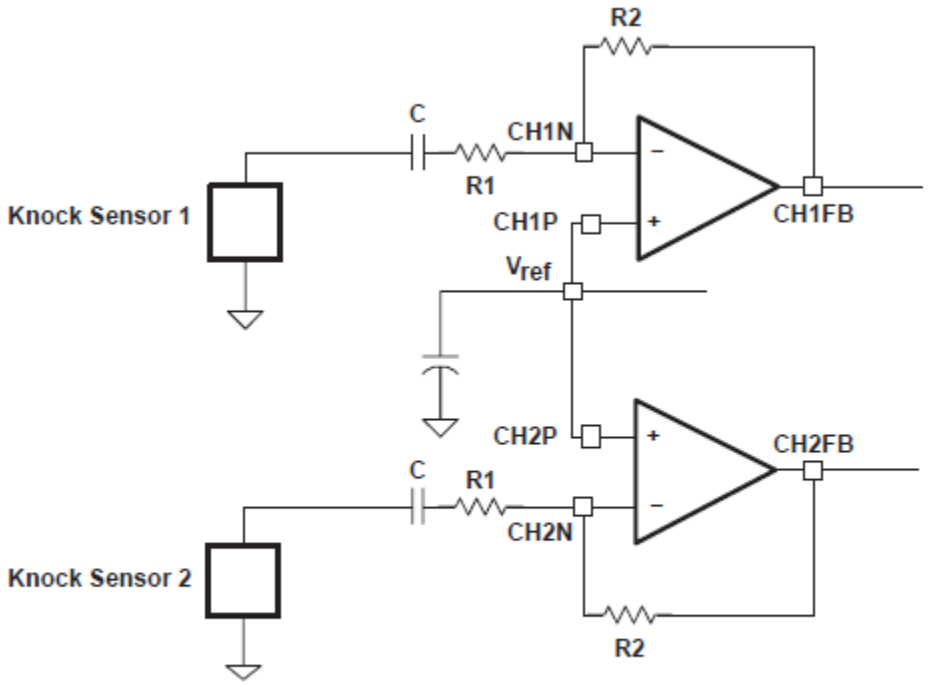


Figure 1. Serial Peripherial Interface (SPI)



capacitor C is not mandatory and may be removed in some application circuits.

Figure 2. Input Signal Configuration

Table 1. Integrator Programming

DECIMAL VALUE (D4...D0)	INTEGRATOR TIME CONSTANT (µSEC)	BAND-PASS FREQUENCY (kHz)	GAIN	DECIMAL VALUE (D5...D0)	BAND-PASS FREQUENCY (kHz)	GAIN
0	40	1.22	2	32	4.95	0.421
1	45	1.26	1.882	33	5.12	0.4
2	50	1.31	1.778	34	5.29	0.381
3	55	1.35	1.684	35	5.48	0.364
4	60	1.4	1.6	36	5.68	0.348
5	65	1.45	1.523	37	5.9	0.333
6	70	1.51	1.455	38	6.12	0.32
7	75	1.57	1.391	39	6.37	0.308
8	80	1.63	1.333	40	6.64	0.296
9	90	1.71	1.28	41	6.94	0.286
10	100	1.78	1.231	42	7.27	0.276
11	110	1.87	1.185	43	7.63	0.267
12	120	1.96	1.143	44	8.02	0.258
13	130	2.07	1.063	45	8.46	0.25
14	140	2.18	1	46	8.95	0.236
15	150	2.31	0.944	47	9.5	0.222
16	160	2.46	0.895	48	10.12	0.211
17	180	2.54	0.85	49	10.46	0.2
18	200	2.62	0.81	50	10.83	0.19
19	220	2.71	0.773	51	11.22	0.182
20	240	2.81	0.739	52	11.65	0.174
21	260	2.92	0.708	53	12.1	0.167
22	280	3.03	0.68	54	12.6	0.16
23	300	3.15	0.654	55	13.14	0.154

Table 2. Default SPI Mode

NO.	CODE	COMMAND (t)	DATA	RESPONSE (t)
1	010 D[4:0]	Set the prescaler and SDO status	OSC_{IN} frequency D[4:1]=0000=> 4 MHz D[4:1]=0001=> 5 MHz D[4:1]=0010=> 6 MHz D[4:1]=0011=> 8 MHz D[4:1]=0100=> 10 MHz D[4:1]=0101=> 12 MHz D[4:1]=0110=> 16 MHz D[4:1]=0111=> 20 MHz D[4:1]=1000=> 24 MHz D[0]=0 => SDO active D[1]=1=> SDO high impedance	SDI (010 D[4:0])
2	1110 000 D[0]	Select the channel	D[0]=0 => Channel 1 selected D[1]=1=> Channel 2 selected	SDI (1110 000 D[0])
3	00 D[5:0]	Set the band-pass center frequency	D[5:0] (see Table 1)	SDI (00 D[5:0])
4	10 D[5:0]	Set the gain	D[5:0] (see Table 1)	SDI (10 D[5:0])
5	110 D[4:0]	Set the integration time constant	D[4:0] (see Table 1)	SDI (100 D[4:0])
6	0111 0001	Set SPI configuration to the advanced mode	None	SDI (0111 0001)

NOTE: Command #6 is to enter into the advanced mode.

O IN P 11 C RESET

PRINCIPLES OF OPERATION

Table 3. Advanced SPI Mode

NO.	CODE	COMMAND (t)	DATA	RESPONSE (t)
1	010 D[4:0]	Set the prescaler and SDO status	OSC_{IN} frequency D[4:1]=0000=> 4 MHz D[4:1]=0001=> 5 MHz D[4:1]=0010=> 6 MHz D[4:1]=0011=> 8 MHz D[4:1]=0100=> 10 MHz D[4:1]=0101=> 12 MHz D[4:1]=0110=> 16 MHz D[4:1]=0111=> 20 MHz D[4:1]=1000=> 24 MHz D[0]=0 => SDO active D[1]=1=> SDO high impedance	Byte 1 (D7 to D0) of the digital integrator output
2	1110 000 D[0]	Select the channel	D[0]=0 => Channel 1 selected D[1]=1=> Channel 2 selected	D9 to D8 of digital integrator output followed by six zeros
3	00 D[5:0]	Set the band-pass center frequency	D[5:0] (see Table 1)	Byte 1 (MSB) of the 00000001
4	10 D[5:0]	Set the gain	D[5:0] (see Table 1)	Byte 2 (LSB) 11100000
5	110 D[4:0]	Set the integration time constant	D[4:0] (see Table 1)	SPI configuration (MSB)01110001(LSB)
6	0111 0001	Set SPI configuration to the advanced mode	None	Inverted SPI configuration (MSB)10001110(LSB)

Table 4. Programming in TEST Mode

NO.	TEST DESCRIPTION	SDI COMMAND MSB.....LSB	RESPONSE	NOTE
T1	AAF individual test	1111 0000	ADC clock	Deactivates the input and output op amps AAF input connected to CH1FB terminal AAF output connected to OUT terminal
T2	In-line test to AAF output	1111 0000	None	Deactivates the output op amp AAF output connected to OUT terminal
T3	Output buffer individual test	1111 0010	None	Opens the feedback loop of the output buffer and deactivates the input op amp and AAF CH1FB connected to positive input terminal of op amp CH2FB connected to negative input terminal of op amp
T4	ADC/DAC individual test (with the output buffer)	1111 0011	ADC data	Deactivates the input op amps and AAF INT/HOLD = ADC_Sync OSC_{IN} = ADC_SCLK DAC shifted in from SDI terminal
T5	ADC/DAC individual test (without the output buffer)	1111 0100	ADC data	Deactivates the input op amps, AAF, and output buffer INT/HOLD = ADC_Sync OSC_{IN} = ADC_SCLK DAC is shifted in from SDI terminal
T6	In-line test to ADC output	1111 0011	ADC data	INT/HOLD = ADC_Sync OSC_{IN} = ADC_SCLK DAC shifted in from SDI terminal
T7	Reading of digital clamp flag	1111 1000	Clamp flag D[2:0]	Implies command 6 (advanced SPI mode) D[0]: Gain stage clamp status D[1]: BPF stage clamp status D[2]: INT stage clamp status D=0 => No clamp activated D=1 => Clamp activated

TYPICAL CHARACTERISTICS

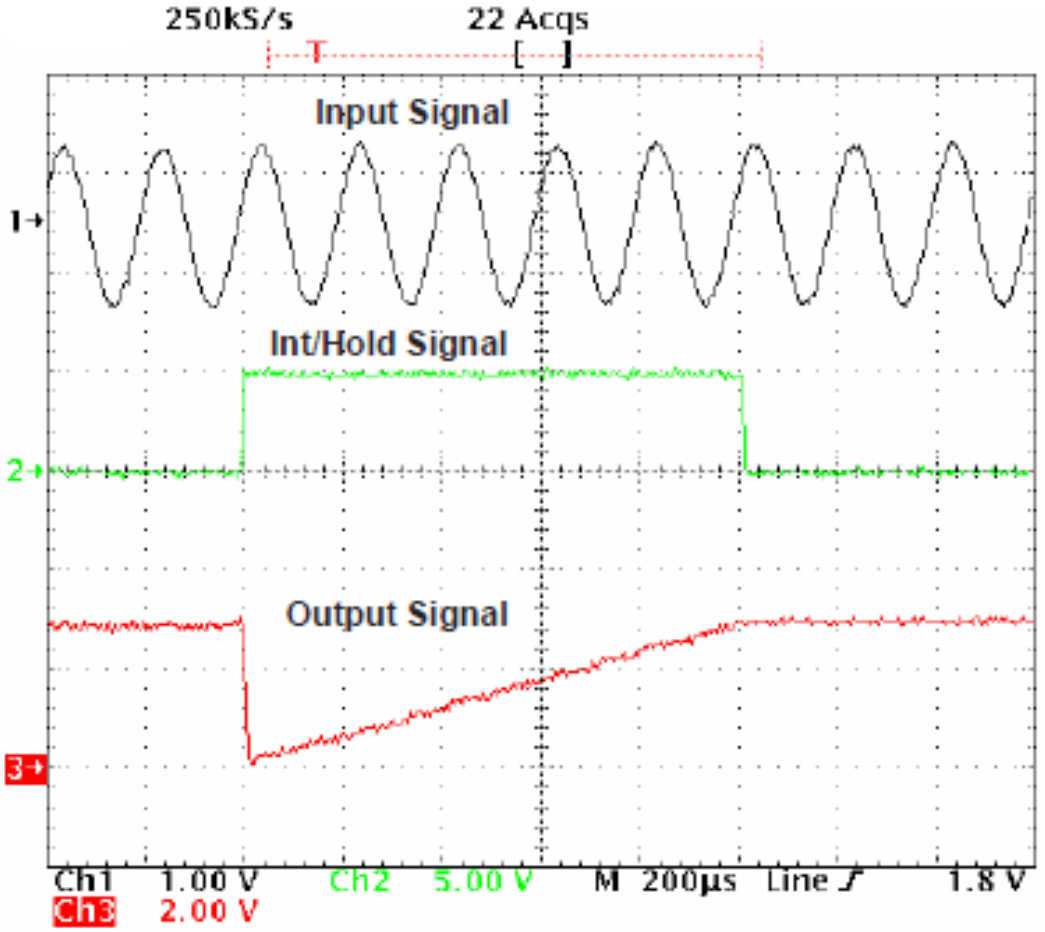


Figure 3. Amplified Input Signal Process

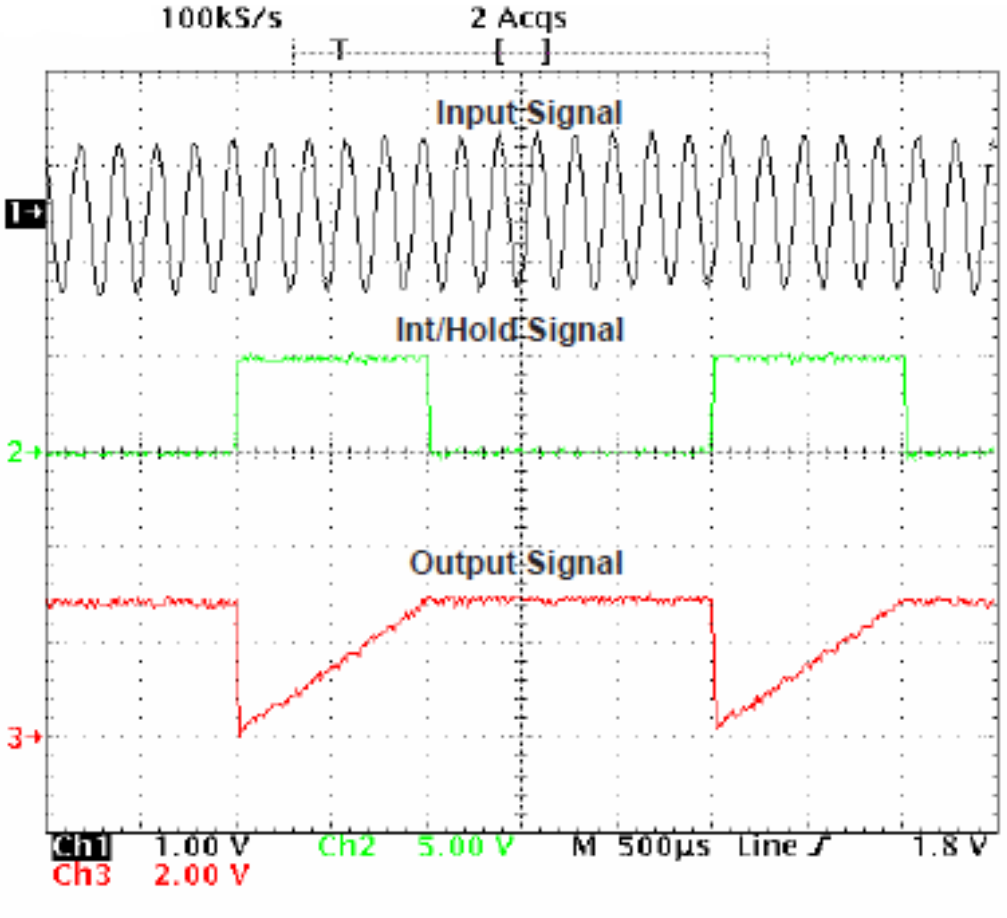
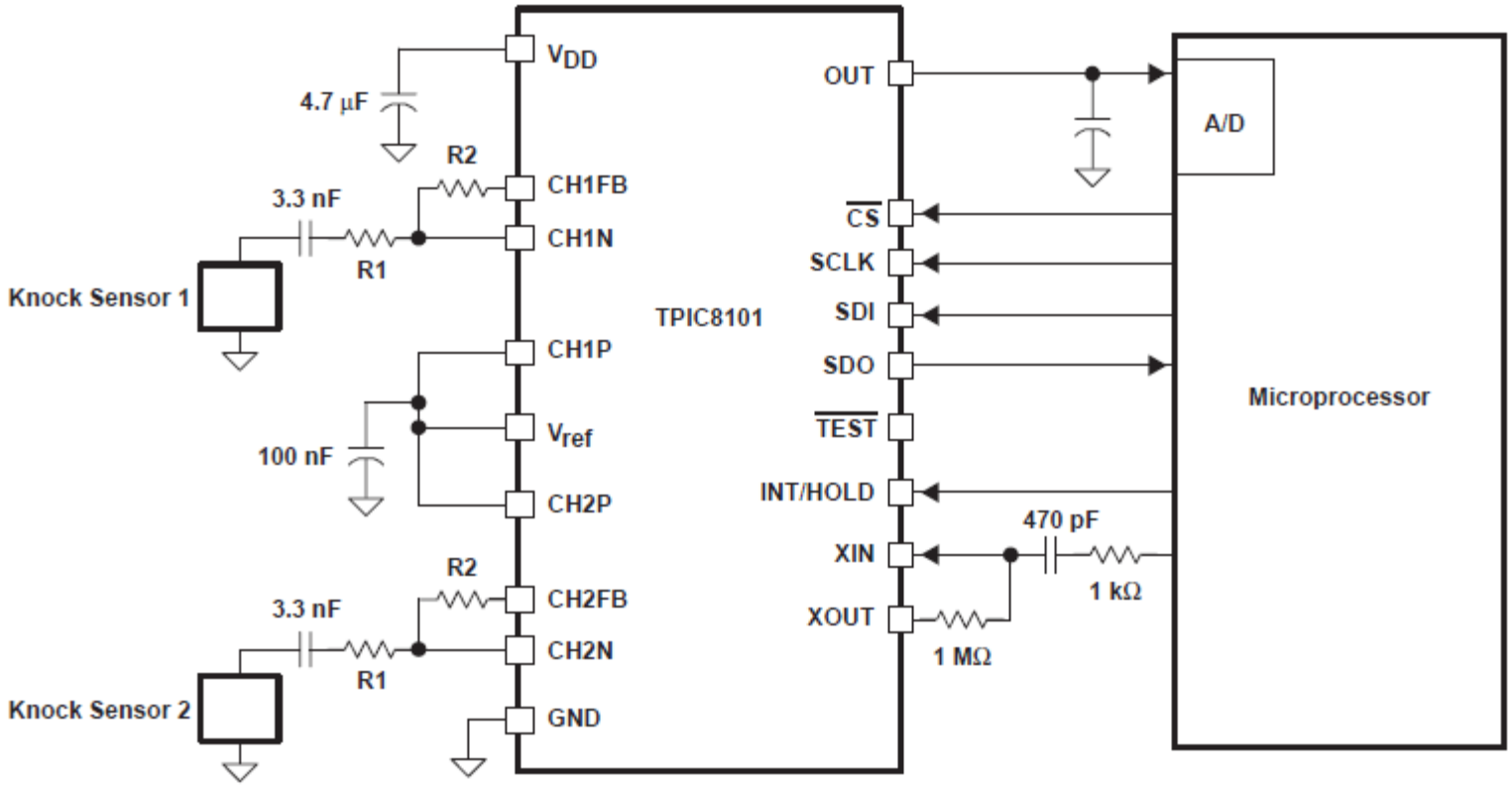


Figure 4. Input Signal Processing

application schematic



NOTE: R1 is greater than 25 kΩ.