Application Note AN-57
TOPSwitch™ Family

9 Simple Steps to Stable Control Loops in Designs Using TOPSwitch Families of Switcher ICs

Introduction

Feedback circuit design can be often intimidating. In this application note we will introduce a simple step-by step approach to designing a stable voltage mode feedback circuit for the TOPSwitch families of integrated switcher ICs.

What will happen if a power supply is allowed to operate in an unstable mode? This question is often unanswered in text books and yet it is important to identify and understand. An unstable power supply may go through cycles of erratic switching and rapid duty-cycle variations. The output voltage can oscillate with large amplitudes, producing an audible noise from the power supply. Instability may occur only under certain load and line conditions.

An empirical "try until something works" tactic is time consuming and prone to error. Loop stabilization is not all that difficult to do, with concepts like placement of poles and zeros, understanding the transfer functions and using simple linear control theory, a stable design can be quickly achieved.

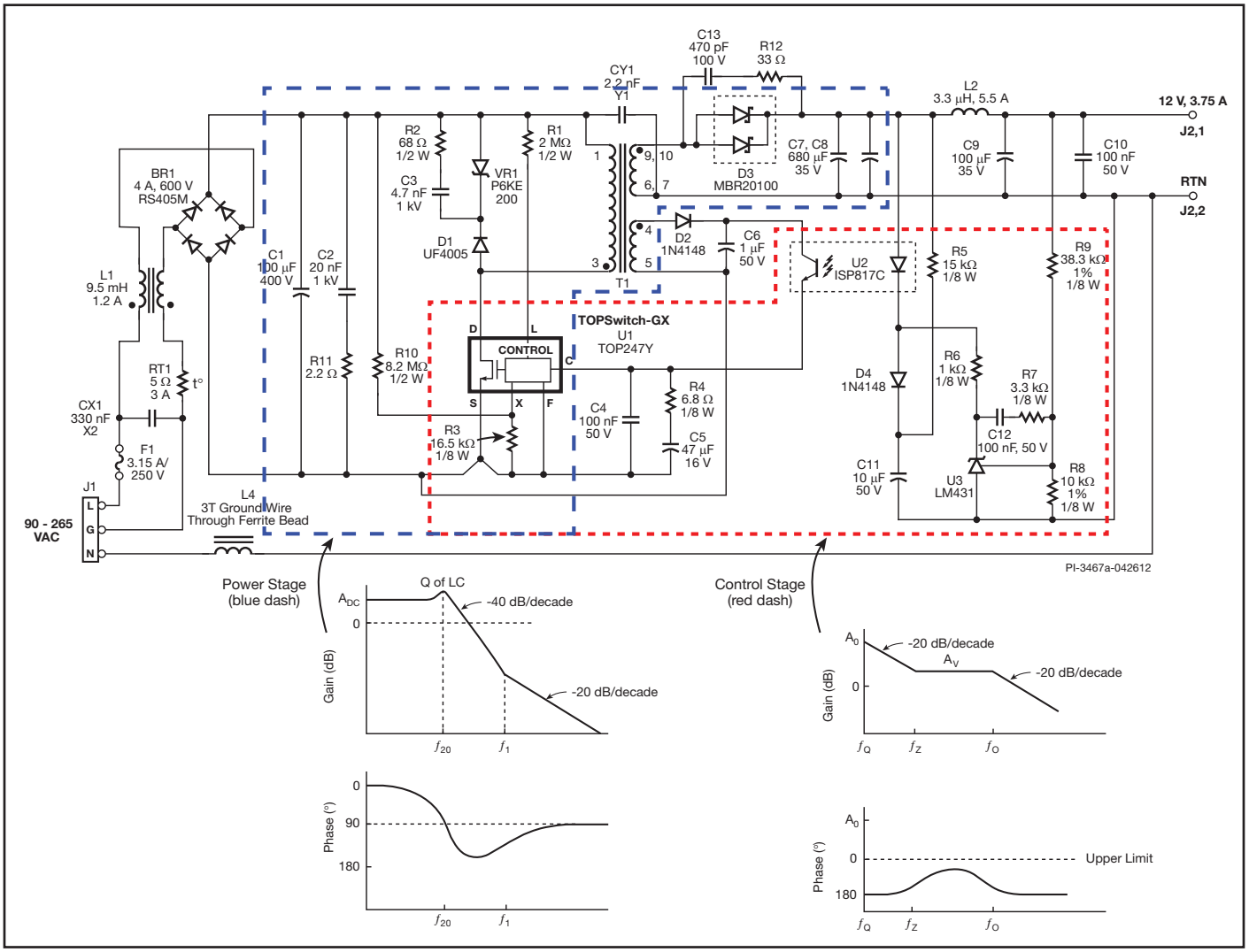

Figure 1. Schematic of a Typical Off-Line Flyback Converter Using the TOPSwitch Integrated Switcher ICs.

Scope

This application note first covers the basics of control theory, bode plots and pole zero responses. It then goes into more detail describing the power stage transfer function and controller transfer function.

Some basic knowledge of linear control theory including bode plots, broad familiarity with transfer functions will be beneficial to properly understand loop stability. Without getting into the complicated mathematics this document first describes a simple 9-step practical approach to designing stable control loops. A worked example is also shown demonstrating the validity of this approach in real designs.

Often times engineers do not have network analyzers to plot the loop response of a power supply. For these cases a section on time domain analysis and interpretation has also been included. For those designers who are interested in a more thorough analysis on the loop, the detailed transfer functions of the power and control stages are also provided in Appendix A and Appendix B at the end of this document.

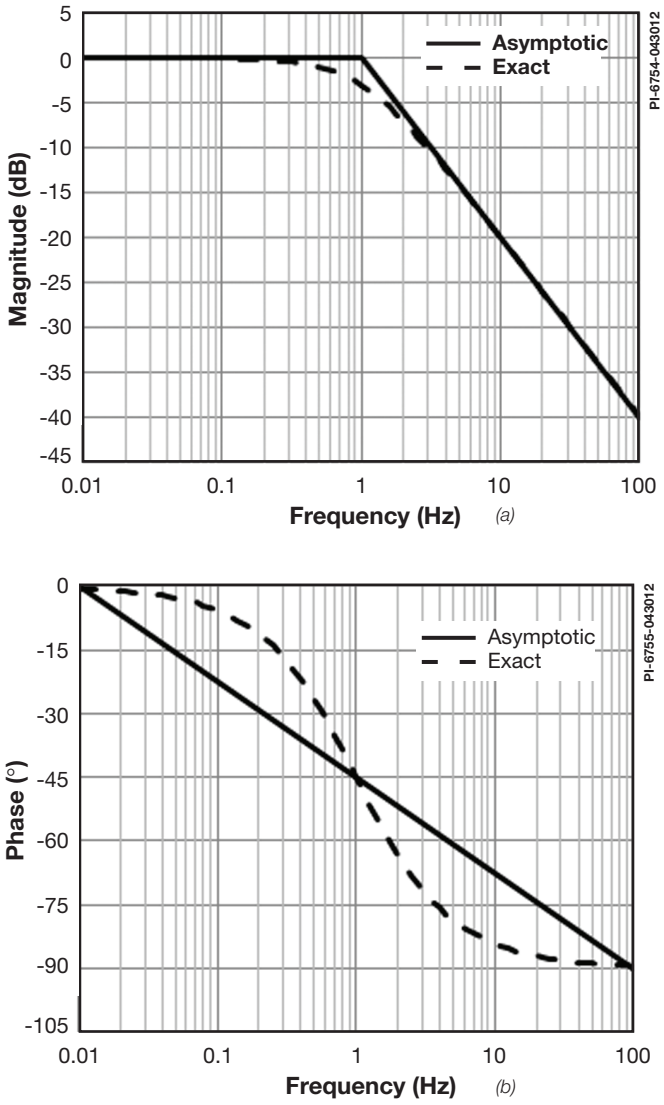

Figure 2. First Order Magnitude and Phase Response for a Pole (Asymptotic and Exact Curves).

Linear Control Theory Basics

We will take a little time to refresh the reader's memory regarding some basic linear control theory. Experienced readers can jump to the "Step-by-Step Design Procedure" if they feel comfortable with the basic concepts of first order and second order responses and bode diagrams.

First Order Response

Single pole response introduces a slope of -20 dB/decade (or +20 dB/decade for a single zero type of response) above the corner frequency and is shown in Figures 2a and 2b respectively. The total phase shift is -90° (or +90° for a zero) it can be seen from Figure 2a that the asymptotic curve (straight line) is 3 dB higher than the exact curve at the corner frequency. A slope of ±20 dB / decade is also referred to as a ±1 slope in some literature.

Second Order Response

The second order response is shown in Figure 3a and 3b as would be seen for an LC network. The magnitude curve has a

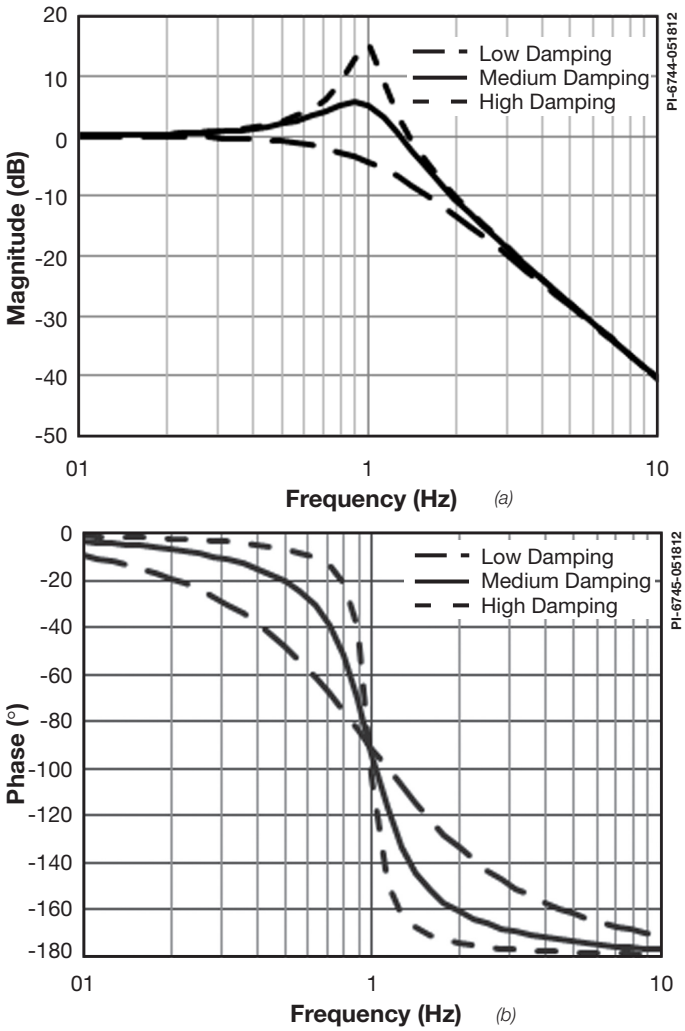

Figure 3. Bode Diagram for a Second Order Magnitude and Phase Response With Varying Damping Factors.

slope of -40 dB/decade (or -2 slope)after the LC corner frequency (also known as resonant frequency) and has a total phase lag of 180°. The gain peaking and rate of fall of the phase depends on the value of zeta (ξ) and the Q factor of the LC circuit. Zeta (ξ) is the damping factor and Q is the quality factor of the LC circuit. Both these parameters are dimensionless and describe how underdamped a resonant circuit is. Higher the damping in the LC circuit, lesser the peaking and slower the decay in the phase.

Absolute Stability, Relative Stability and Conditional Stability

When a system is subjected to a disturbance there are two ways it can respond when the disturbance is removed. One is that it settles down to an equilibrium state and the other is that it does not – and it remains unstable. If it achieves some equilibrium state it is said to be "absolutely stable".

Relative stability refers to two indicators that point out just how close the system is to becoming unstable. These two indicators are gain margin and phase margin. To understand these two indicators it is essential to note that when a system becomes unstable its phase lag is 180° and its loop gain is equal to 0 dB. Gain margin indicates the amount by which the gain can increase before the system becomes unstable when the phase lag is 180°. Phase margin indicates the amount by additional phase lag the system can tolerate before it becomes unstable when the gain is equal to 0 dB. Typically a system should be designed to have a minimum of 6 dB gain margin and 45° phase margin. This is to ensure stability over production units, age, temperature and load transients. It is not uncommon to see organizations set targets of 10 dB gain margin and 60° phase margin for their power supplies.

A conditionally stable system is one where the gain remains above 0 dB when the phase dips below 180° but then comes back above 180° before gain crosses 0 dB. You should avoid designing conditionally stable systems. This is because there are several situations when the gain of the loop can suddenly decrease (for example start-up, transient or other conditions that can lead to a saturated error amplifier) causing the system to become unstable.

Why Do We Need a Control Loop?

Instinctively one will answer the above questions with a "to control the output voltage and hold it steady", which is perfectly correct. However in the process of "holding the output voltage steady" under all conditions of load and line, there are certain challenges associated. For example when there is an increase in the line voltage the output voltage will rise. To counter this, in response, the duty cycle should reduce in order to bring the output voltage to its original condition. These changes (or perturbations) on the output may cause the response to be oscillatory or unstable. This is why it is important to have sufficient phase and gain margins to guarantee stable operation over the entire operating range.

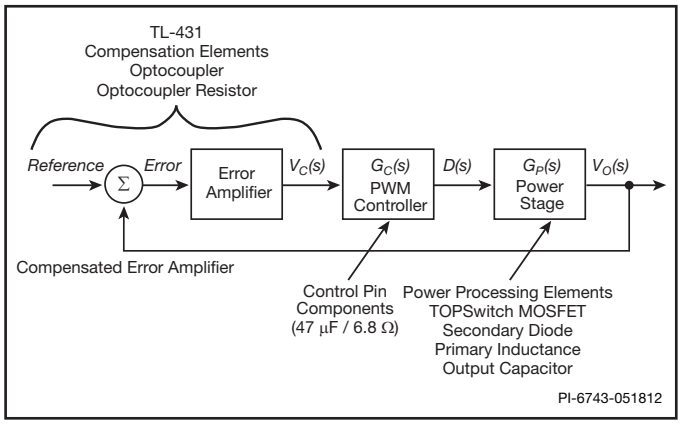

Figure 4. Voltage Mode Control - Block Diagram Representation.

Voltage Mode Feedback

The traditional voltage mode control mechanism is shown in Figure 4 where the output voltage is compared with a reference voltage to generate an error signal. This error signal is fed into a compensated error amplifier, which produces a control signal. The control signal is then processed by the PWM generator to generate the appropriate duty cycle to control the switch on-time and regulate the output voltage.

Right Half Plane (RHP) Zero

The transfer function of a flyback power supply operating in the continuous conduction mode (CCM) contains an inherent right half plane pole zero (RHP zero) often cited as a reason to avoid CCM. RHP zeros have the magnitude response of a zero but the phase response of a pole and are very difficult to compensate. In a physical circuit they cause the power supply output to initially respond in the opposite direction than that directed by the controller. The amount of time before the output responds in the correct direction is a function of the RHP zero frequency. To understand this mechanisim, consider a fixed frequency flyback converter operating in CCM.

The output capacitor is charged by the inductor current delivered during the primary switch off-time. An initial increase in the duty cycle of the switch increases the current (and therefore energy stored) in the inductor. However since the switching frequency is fixed, an increase in duty cycle results in a reduction in the off-time which is the available time for the inductor to transfer its stored energy to the output capacitor and load. This results in a reduction in energy transferred, causing an initial drop in the output voltage.

Since in DCM there is a finite idle time (time when both the primary-side switch and secondary diode are off), the reduction in off-time does not affect energy transfer during the switching cycle. The RHP zero is therefore only seen in CCM.

Step-by-Step Design Procedure

Note: This analysis assumes that the post filter does not affect the loop response until its resonant frequency. Design the post filter such that LPF and CPF resonate at a frequency greater than 10 kHz to achieve this.

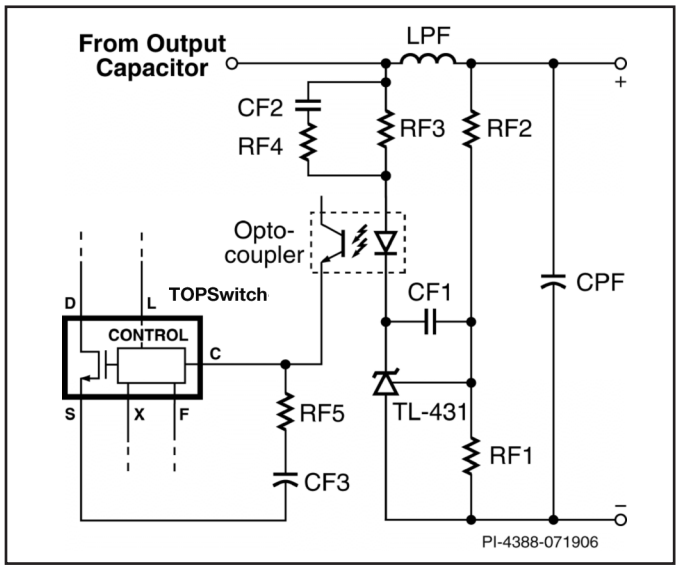

Figure 5. Components of the Feedback Loop.

Step 1 – Setting Loop Performance Parameters

Calculate expected location of the RHP zero.

Using equation 12, from Appendix A, calculate the location of the RHP zero at low-line. We have

$$\omega_{RHP} = \frac{R_O}{L_E \times D}$$

Select a Reasonable Crossover Frequency $f_{CROSSOVER}$
The crossover frequency should be below one tenth of the switching frequency and below one fifth the frequency of the RHP zero. Higher crossover frequencies do result in higher bandwidth, but often increases sensitivity to noise. A reasonable crossover frequency for TOPSwitch circuits can be anywhere from 500 Hz to 3 kHz. For more than 80% of designs, 1 kHz is a good starting point for crossover frequency target.

Select Desired Open-loop Phase Margin
Higher phase margin ensures less overshoot to step load changes. Usually a phase margin of at least 45° is required, start with 60° which is within the recommended range of 45° to 75°.

Step 2 – Select the Output Filter Capacitor C_O

The filter capacitor should be chosen such that the rated ripple current of the capacitor chosen should exceed the calculated capacitor ripple current. Higher voltage rated capacitors will tend to have lower capacitance value for the same ripple current rating than smaller voltage rated capacitors. It is recommended that the LC tank formed by the output capacitor and the effective inductance L_E (given in equation 13) should have its resonant frequency >500 Hz. This may call for using a lower value output capacitance with a larger voltage rating to satisfy ripple current requirements.

It should be noted that the effective inductance L_E is derived from the magnetizing inductance and duty ratio. L_E comes from the small signal model of the flyback converter and is not a physical component.

Step 3 – Selection of RF5 and CF3

A typical control loop circuit is shown in Figure 5. Resistor RF5 and CF3 together with the internal impedance of the control pin (approximately 15 Ω) forms a pole-zero pair in the frequency response. This pole-zero pair does not actively participate in the loop compensation. See Appendix B for a more detailed treatment of these two components and the resulting pole-zero pair.

Capacitor CF3 is a capacitor that provides power to the TOPSwitch internal circuitry and also determines the auto-restart time period. As such it has little bearing on the control loop response. Standard values for this component are between 10 μF and 100 μF, the recommended value being 47 μF.

RF5 is a small resistor, which is used in series with CF3. The purpose of this resistor is to introduce a stable series resistance (in addition to the ESR of CF3) and to shift the pole-zero pair

frequencies $f_{ZERO(TOP)}$ and $f_{POLE(TOP)}$ as close to each other as permissible. RF5 should be chosen between 0 Ω to 22 Ω.

$$CF3 = 47\ \mu F$$
$$0\ \Omega \le RF5 \le 22\ \Omega \qquad (1)$$

Larger values of RF5 tend to bring the pole zero pair formed by $f_{ZERO(TOP)}$ and $f_{POLE(TOP)}$ closer together. However, since the control pin is also the power source pin for the controller inside the TOPSwitch, the value of RF5 cannot be indefinitely increased. Values above 22 Ω should be avoided, the recommended value being 6.8 Ω.

Step 4 – Selection of Optocoupler

The optocoupler CTR can play a significant role in the overall loop gain. A nominal CTR value of 1 is recommended with a specified range e.g. 0.8 to 1.6. Higher CTR's should be compensated with larger gain limiting resistor (RF3) values and vice versa.

Step 5 – Selection of Error Amplifier and Reference

For low cost power supplies very often the error amplifier and reference come bundled together in a single package. The error amplifier and reference IC which is most popular and which provides good performance is the TL431. It is available in two varieties depending on the reference voltage. For low output voltages (3.3 V and below) use the 1.25 V reference and for higher output voltages use the 2.5 V reference. The 1.25 V reference also needs lower bias currents and can be used for low standby input power applications.

Step 6 – Selection of RF1

Resistor RF1 typically does not influence the loop response and does not appear in any of the gain phase equations. It sets the resistive divider such that the TL431 circuit gets appropriate bias current vs. input current of REFERENCE pin. A 10 kΩ resistor is a good initial choice for this resistor. Too high a value tends to starve the error amplifier of bias current while too small a value tends to increase the power dissipation. Generally RF1 is recommended to be in the range of 2 kΩ and 50 kΩ.

Step 7 – Selection of RF2

Resistor RF2 determines the output voltage and once RF1 has been fixed, it can be easily calculated from the following expression

$$RF2 = RF1 \times \frac{(V_O - V_{REF})}{V_{REF}} \qquad 2$$

where
V_O – is the output voltage.

V_{REF} – is the reference voltage of the TL431 (usually 2.5 V or 1.25 V). Thus for a 12 V output RF2 will be 38 kΩ with RF1 set at 10 kΩ. It is recommended that resistors RF1 and RF2 be 1% resistors.

Step 8 – Selection of Compensation Capacitor CF1

Select the compensation capacitor such that the location of the zero f_{ZERO} together with f_{POLE} (the 7 kHz internal pole of the TOPSwitch ($f_{TOPSWITCH}$) provide maximum phase boost at the desired crossover frequency $f_{CROSSOVER}$, which is usually 1 kHz. From equation (25) in Appendix B, it can be seen that f_{ZERO} is determined by the RC network, which is formed by the input resistor of TL-431 (RF2) and the compensation network capacitor (CF1) of the TL 431. Choose f_{ZERO} in the range of 100 Hz. If the design is expected to operate in discontinuous mode as well then it is recommended that f_{ZERO} be set at 50 Hz rather than 100 Hz to avoid conditional stability in discontinuous conduction mode. Select the capacitor using

$$CF1 = \frac{1}{2\pi \times f_{ZERO} \times RF2} \qquad 3$$

Step 9 – Selection of Gain Adjusting Resistor RF3

Resistor RF3 sets the gain of the open-loop transfer function. This component has the effect of shifting the entire magnitude plot up or down without affecting the phase response. Ideally one should plot the individual power stage and control stage transfer function (provided in Appendix A and B) and then determine the gain reduction required at the desired crossover frequency to determine the value of this resistor RF3.

In order to determine the value of RF3 analytically, plot the open-loop transfer function (magnitude and phase) of the product of the power stage P(s), which is the product of equation 10 and equation 14, and the controller $G_{CONTROLLER}(s)$, which is the product of equation 22 and equation 23. Assume RF3 = 1 while computing the gain of the controller K_C. Thus

$$K_C = \frac{K_{TOP} \times K_{TL431}}{1} \qquad 4$$

From the magnitude determine how much the gain must be lowered at the gain crossover. This reduction in gain (without affecting the phase) should come from gain limiting resistor RF3. If "X" is the excess gain at the desired crossover frequency, measured in dB we have

$$RF3 = 10^{\frac{X\,dB}{20}}\Omega \qquad 5$$

PI Expert automatically plots the transfer functions to determine the value of RF3 using this approach.

Table 1 below suggests starting values for this resistor based on experimental data from off-line flyback designs. It is worth mentioning however that since the value of RF3 is a function of damping, output voltage and basic loop gain these values will not be optimal for all designs. These are merely starting values, which have been found to work well in many designs. These values can tend to have the effect of providing more gain to the system. Thus if after using these values the transient response is poor or unsatisfactory, a good starting point for fine tuning the feedback circuit maybe to start progressively increasing the value of RF3 slowly and repeating transient load testing.

The table also lists the max resistor value (used with an opto-coupler of CTR = 100) to guarantee voltage regulation. The chosen value of RF3 should not exceed the value in this column. Higher values may limit the optocoupler LED current and cause loss of regulation.

Output Voltage (V)	RF3 Starting Value (Ω)	RF3 Maximum Value (Ω)
5	200 (100)	470 (233)
12	910 (470)	2700 (1300)
15	1300 (680)	3600 (1800)
24	2000 (1000)	6800 (3300)
48	3900 (2000)	14700 (7320)

Table 1. Resistor Values for RF3 in TOPSwitch-JX Designs (Value in ( ) for Other TOPSwitch Families)

If an optocoupler with higher CTR is used, the starting values should be increased appropriately. For example if an opto-coupler with CTR of 400% is used on a 12 V power supply, the starting value and the maximum value of RF3 should be increased by a factor of 4.

Step 10 (if necessary) – Selection of Phase Boost Network (RF4 and CF2)

Resistor RF4 and CF2 are optional components and may not be required in many designs. If after step 9 there is insufficient phase margin, or if there are more than 3 outputs in the power supply inclusion of the phase boost network formed by RF4 and CF2 may be required. RF4 and CF2 can be calculated using equations (6) and (7)

$$RF4 = \frac{RF3}{9} \qquad 6$$

$$CF2 = \frac{9}{10 \times (2\pi \times RF3 \times f_{CROSSOVER})} \qquad 7$$

Multi-Mode Control in TOPSwitch

The newer generations of TOPSwitches have four distinct modes of operation. The design of the IC is such that the transition between each of these modes is seamless. From a control loop standpoint, you should test the loop at the worst case – full load. While doing transient testing or while inspecting the power supply operation in time domain if you see the frequency of operation in the multi-cycle modulation (MCM) mode below 25 kHz this is an indication that the loop may be unstable or conditionally stable.

Worked Example

Let us apply this procedure to design a controller for a 12 V, 30 W design. The basic electrical parameters we need for this circuit are summarized in Table 2.

Component	Value	Description
C_{OUT}	1360 µF	Output Filter Capacitor
L_P	827 µH	Primary Inductance
L_E	41 µH	Effective Inductance
D	0.55	Operating Duty Cycle
V_{IN}	80 V	DC Input Voltage
ESR	33 mΩ	Filter Capacitance Equivalent Series Resistance
Q	0.15	Q Factor of LC Tank Circuit
R_O	3.2 Ω	Effective Load Resistance

Table 2. Basic Electrical Parameters.

Q factor is a lossless damping factor introduced in the transfer function of the flyback topology which inherently possesses high damping (low ξ). The Q factor is set at 0.15, which is a good starting point for an isolated flyback design using TOPSwitch.

Step 1 – Setting Loop Performance Parameters

Calculate Expected Location of the RHP Zero

Using equation 4 calculate the location of the RHP zero at low-line. We have

$$\omega_{RHP} = \frac{R_O}{L_E \times D} = \frac{3.2\,\Omega}{41\,\mu H \times 0.55} = 141\,krad/s \simeq 23\,kHz$$

The RHP zero occurs at 23 kHz so the crossover frequency must be well below 23 kHz. It is recommended that the maximum crossover frequency should be below one fifth of the RHP zero frequency (4.6 kHz in this example).

Select a Reasonable Crossover Frequency $f_{CROSSOVER}$

The crossover frequency should be below one tenth of the switching frequency and below one fifth the frequency of the RHP zero.

For this design we will stick to the recommended target crossover frequency of 1 kHz. This is because this is a universal input design and at higher input voltages the gain of the power stage is higher resulting in higher crossover frequencies.

Select Desired Open-Loop Phase Margin

Higher phase margin ensures less overshoot to step load changes. A reasonable phase margin for can be between 45° to 75°.

Select 45° as target phase margin for this design.

Step 2 – Select the Output filter Capacitor C_{OUT}

The filter capacitor should be chosen such that the rated ripple current of the capacitor chosen should exceed the calculated capacitor ripple current. Higher voltage rated capacitors will tend to have lower capacitance value for the same ripple current rating than smaller voltage rated capacitors. Another recommendation is that the LC tank formed by the output capacitor and the effective primary inductance L_E (given in equation 13) should have resonant frequency after about 500 Hz in continuous mode operation. This may call for using a smaller value capacitance with larger voltage rating to satisfy ripple current requirements.

Step 3 – Selection of RF5 and CF3

Using the guidelines outlined in equation 1 we can select RF5 and CF3 as follows

$$CF3 = 47\,\mu F$$
$$RF5 = 6.8\,\Omega \qquad (8)$$

Step 4 – Selection of Optocoupler

Select an optocoupler with a nominal CTR of 100. Examples of such optocouplers are PC817A or LTV817A. Higher CTR optocouplers offer a reduction in no load input power (due to reduced steady-state operating current requirement). Examples of such optocouplers are PC817D or LTV817D.

Step 5 – Selection of Error Amplifier and Reference

Select the TL431 with reference voltage of 2.5 V for this design. For lower output voltages a lower voltage reference of 1.25 V may be used.

Step 6 – Selection of RF1

As RF1 does not factor in any of the gain phase equations it can be set at 10 kΩ.

Step 7 – Selection of RF2

From equation 2 we have

$$RF2 = 10\,k\Omega \times \frac{(12\,V - 2.5\,V)}{2.5\,V} = 38\,k\Omega$$

Select closest available 1% resistor if calculated value is not a standard resistor value. Select 38.3 kΩ.

Step 8 – Selection of Compensation Capacitor CF1

Compensation capacitor CF1 sets the pole very close to 0 Hz and also sets the zero frequency. Select the capacitor such that the zero frequency is around 100 Hz. Using equation 23 we have

$$C_{TL431} = \frac{1}{2\pi \times 100\,Hz \times 38\,k\Omega} = 41.88\,nF$$

Select next higher value of capacitor of calculated value is not a standard capacitor value. Select 47 nF.

Step 9 – Selection of RF3

Set RF3 = 1 Ω and plot the combined transfer function from Equations 10, 11, 15 and 25. This is the overall magnitude response of the power supply (Figure 6).

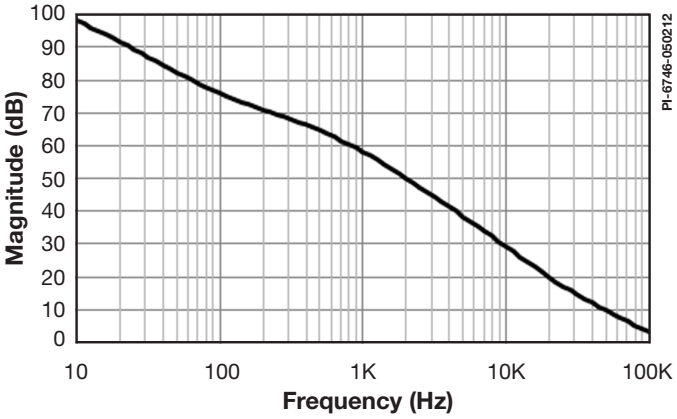

Figure 6. Magnitude Response with RF3 = 1 Ω Gives the Amount of Gain Reduction Required in Order to Crossover at 1 kHz.

From Figure 6 we can see that there is an excess gain of about 60 dB at the desired crossover frequency of 1 kHz which needs to be reduced by increasing RF3. Thus using equation (5) we have

$$RF3 = 10^{\frac{60.096}{20}} = 1.03\,k\Omega$$

Select next smaller standard resistor value (1 kΩ). Alternatively a starting value could have been selected from Table 1.

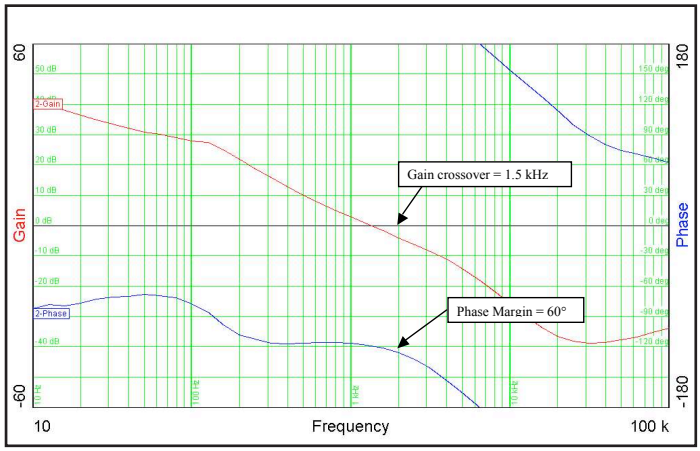

Figure 7. Actual Gain Phase Response Using Component Values as Calculated From the Step-by-Step Procedure.

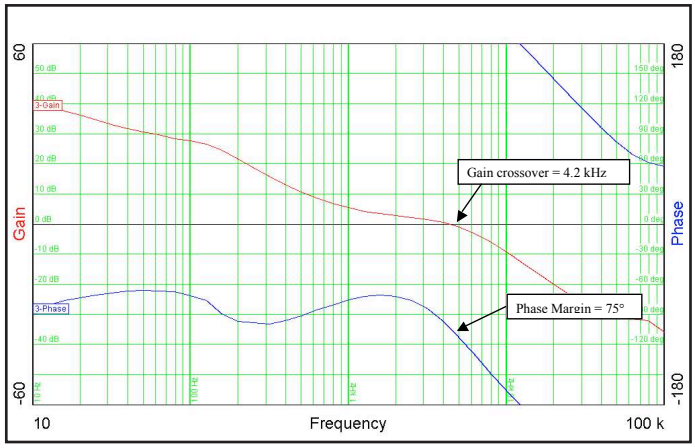

Figure 8. Gain Phase Response Using the Phase Boost Network.

Plot the Actual Gain Phase Response and Check Which Component Values Need Fine Tuning

Plot the actual gain phase response of the power supply (see section Gain Phase Measurement Technique Using Current Injection) with the calculated values (Figure 7).

As shown in Figure 7 the gain phase response is slightly different than predicted. The actual crossover frequency is about 1.5 kHz and the phase margin is about 60° (which is good). In fine-tuning this design the designer may want to increase the value of RF3 further to bring down the crossover frequency nearer to 1 kHz (target). The calculations make assumptions on the design parasitics and therefore these differences should not be surprising. The transfer function circuit realized with the components calculated above is shown in Figure 21 and 22. It has 2 poles and 1 zero actively taking part in the compensation of the loop and is commonly referred to as the "type 2 controller circuit" or simply the "type 2 circuit". More detailed information on type 2 controllers can be found in Appendix B.

Another area where the designer may experiment with component values is increasing CF1 compensation capacitor. This will tend to flatten the response around the lower frequency region providing more gain at 120 Hz frequency and may prove to reduce line frequency ripple component in the output voltage.

In addition the designer may experiment with the control loop design by trying the phase boost network (see Appendix B). This circuit should be used if there is insufficient phase margin from the type 2 circuit. This circuit modification (introduction of the phase boost network) is not needed for this example but it is shown nevertheless, for the purpose of illustration.

For this design using equations (6) and (7) we have
RF4 = 110 Ω
CF2 = 1 µF

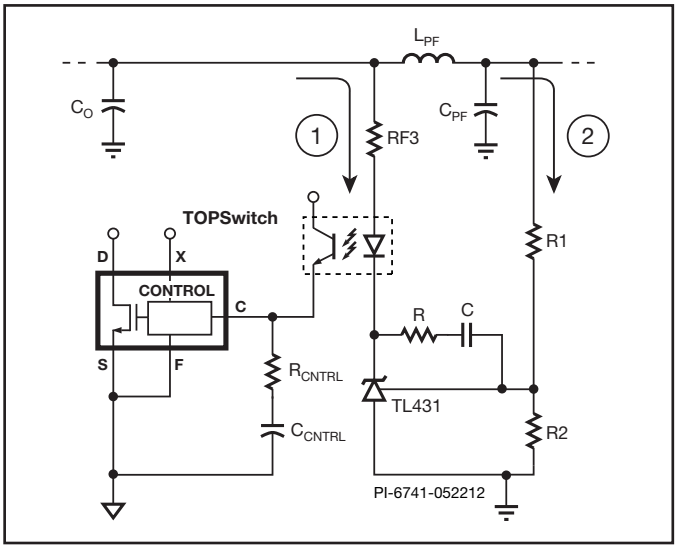

Figure 9. Two Feedback Paths Exist Which Make it Impossible to Break the Loop on Secondary Side.

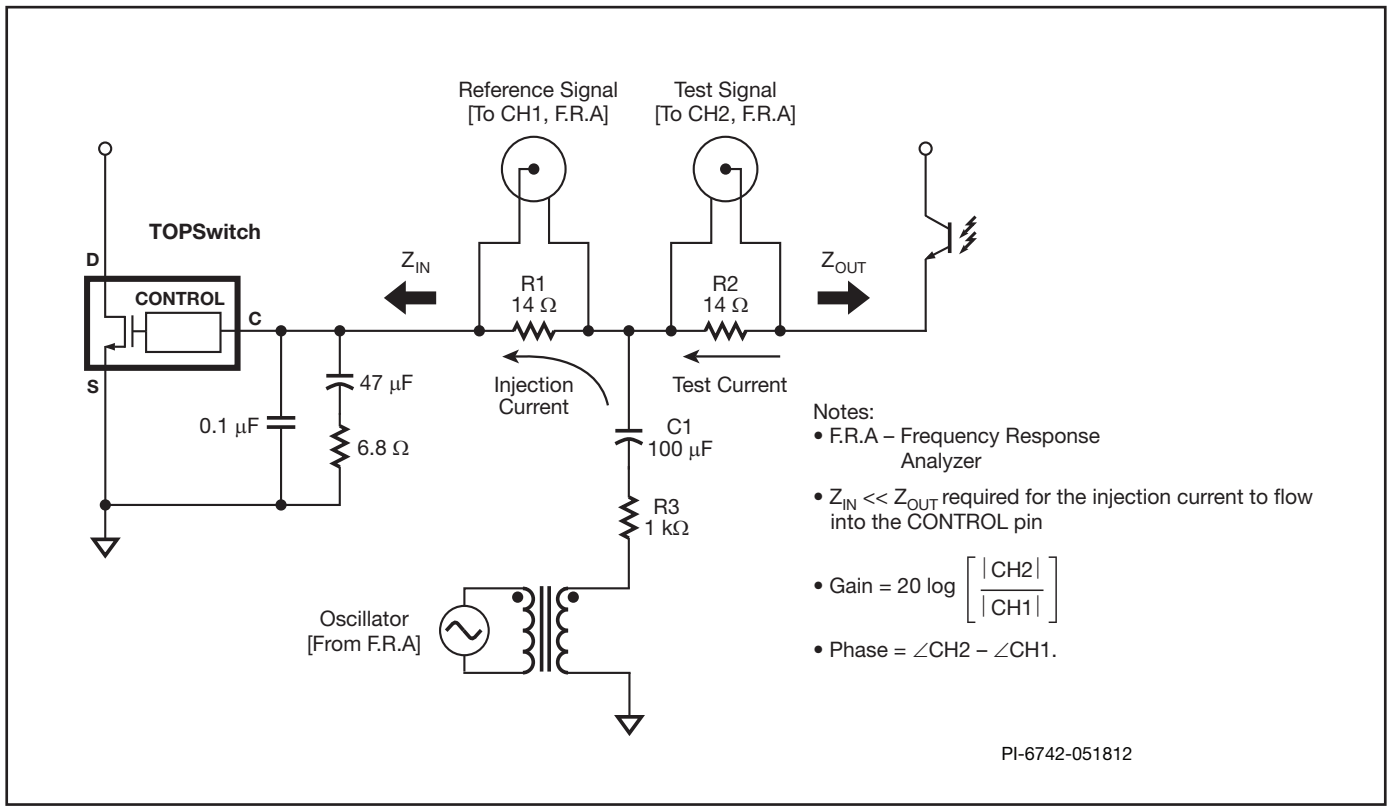

Figure 10. Circuit Diagram for Bench Verification of Gain Phase Response Using Current Injection Method.

Using the above values Figure 8 shows the actual phase plot with the phase boost network. The transfer function is shown in Figure 25.

Figure 8 shows that the phase boost network gives an additional 15° of phase margin. The crossover frequency has increased to 4.2 kHz and this should be addressed by fine-tuning (increasing) the value of RF3 in order to crossover nearer to 1 kHz to 2 kHz. The resultant circuit with the phase boost network has 3 poles and 2 zeros taking part in the compensation and is commonly known as the “type 3 controller” or simply as “type 3” circuit.

Gain Phase Measurement Technique Using Current Injection

One of the most important steps in loop measurement is to determine where the loop should be broken and the perturbation signal injected. Referring to Figure 9 two separate paths exist in a control scheme involving secondary side feedback using the TL431 (or any op-amp). Breaking the loop at one of these locations would lead to incorrect results since one path (Path 1) dominates the high frequency feedback signal contribution and the other (Path 2) dominates the low frequency feedback signal contribution.

However if the loop is broken between the optocoupler and the control pin this point will contain the combined signal from both paths (Path 1 and Path 2 from Figure 9). However, in breaking the loop at this point, we are faced with the situation that the input impedance Z_{IN} (looking into the TOPSwitch) is much smaller than the output impedance Z_{OUT} (looking into the emitter side of the optocoupler). We can get around this problem by injecting a current signal at the injection point rather than a voltage signal. The concept of bode plot measurements remains the same, the only difference being that we compare the magnitude and phase of two current signals.

Figure 10 shows an arrangement describing how to make a gain phase plot for open-loop using the current injection method. It should be noted that the power supply under test must be isolated from the mains (AC input) to avoid risk of electrical shock.

Referring to Figure 10, the reference signal represents the error input to the loop and the test signal is the response so gain is CH2/CH1. Generally, the excitation signal must be larger at lower frequency because of the small reference signal due to higher loop gain and smaller at higher frequency to avoid small signal distortion. Monitor the AC output ripple to make sure that the injected signal is not being distorted, it should be close to a sine wave as possible. Try different signal levels and find a reasonable band of amplitudes that gives a constant result for given frequency selections. Also longer integration times with more sampling is usually required at low frequency (below 200 Hz) to get consistent results. It is difficult to measure gain above 50 dB with any consistency because of the low signal to noise ratio. Since the loop is broken on the primary side be sure to isolate the analyzer from the AC input to avoid noise coupling which will give significant errors.

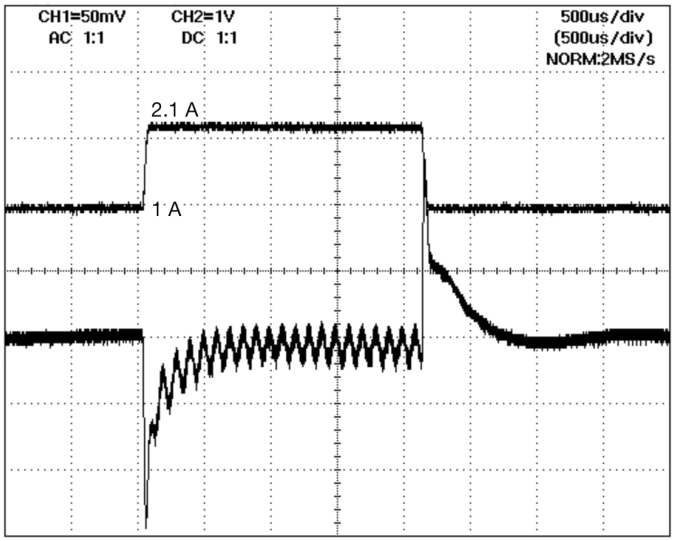

Figure 11. Transient Response 1 A to 2.5 A of Example Power Supply with Excessive Gain (RF3 Replaced with a 50 Ω Resistor).

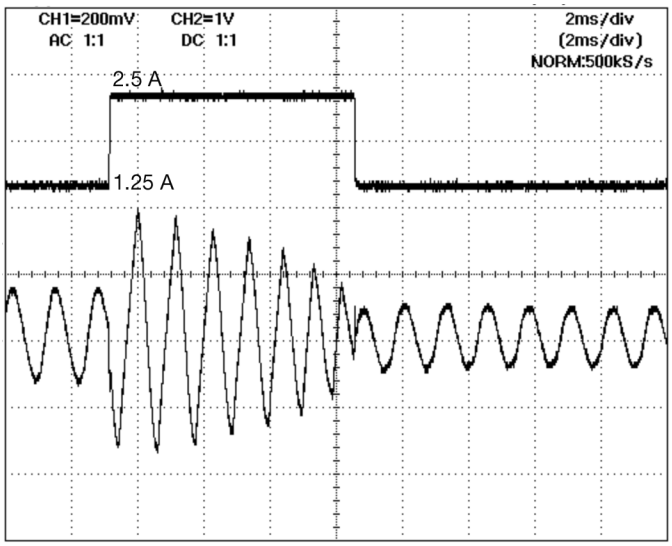

Figure 13. Transient Response of Example Power Supply with CF1 Replaced with a 2.2 nF Capacitor.

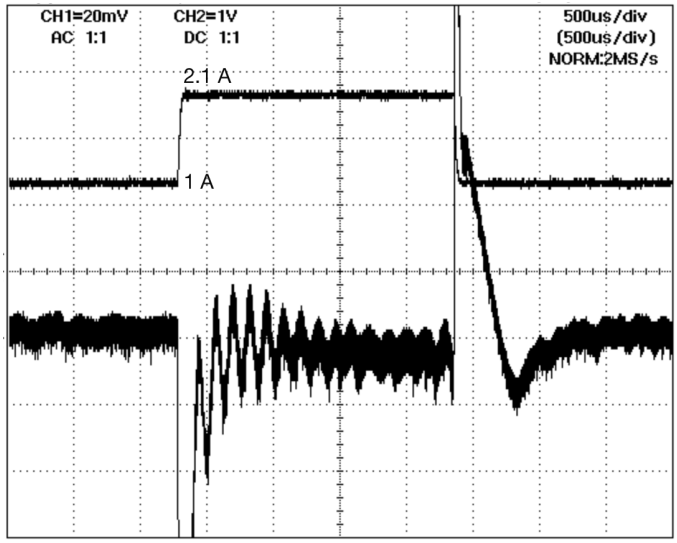

Figure 12. Replacing RF3 with 200 Ω (Reducing the Gain) Tends to Stabilize the System.

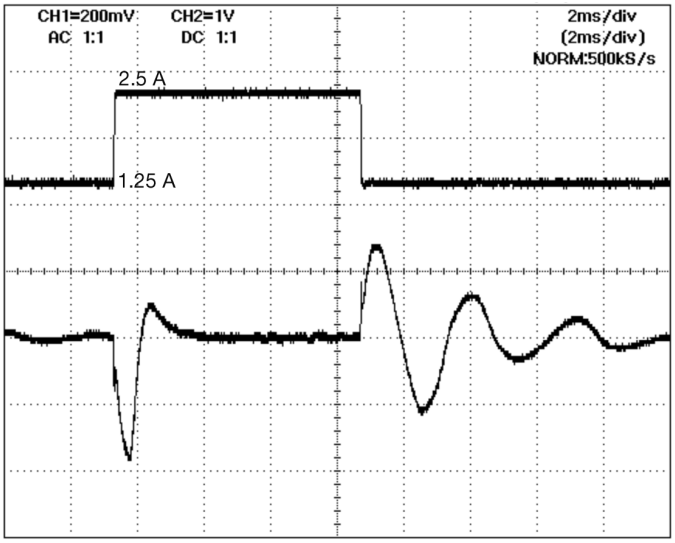

Figure 14. Transient Response of Example Power Supply with CF1 Replaced with a 10 nF Capacitor.

Transient Load Testing

Even if you have a network or frequency response analyzer, transient load testing should always be done as a means to test the absolute stability of the power supply. Loop gain measurements gives guidance about relative stability but transient load testing proves performance under real world non-linear conditions. It subjects the power supply to large signal variations and effects of possible error-amplifier saturation. Transient load testing is a very convenient and way to test the stability performance of the power supply. It is also an inexpensive method, which does not require use of sophisticated equipment. And while it does not provide accurate information about phase margin or gain margin it does provide important information as to whether or not the power supply is stable.

A series of transient load scope shots are presented below. We will also analyze each plot to see what information is revealed.

First we will take the example of design shown in Figure 1 and intentionally modify it in a manner to introduce instability and see how this instability manifests itself on the transient load plot. Let us first increase the gain to the point that it will cause instability. Let us replace resistor RF3 (R6 in Figure 1) from 1 kΩ to 50 Ω. Instability in the power supply is obvious by the audible noise emanating from it. Figure 11 shows the transient load plot for this design.

One can see the oscillatory nature when the power supply is loaded (to 2.1 A) such that it operates in continuous conduction mode (CCM). This is oscillating at about 10 kHz. Moreover

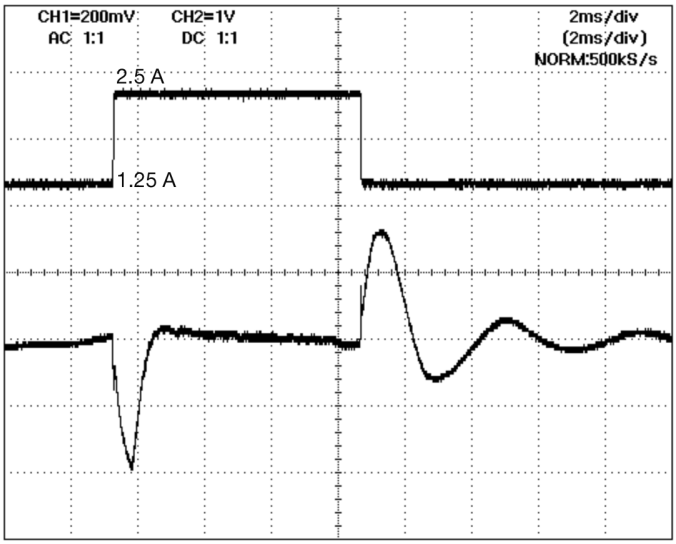

Figure 15. Transient Response of Example Power Supply with CF1 Replaced with a 22 nF Capacitor.

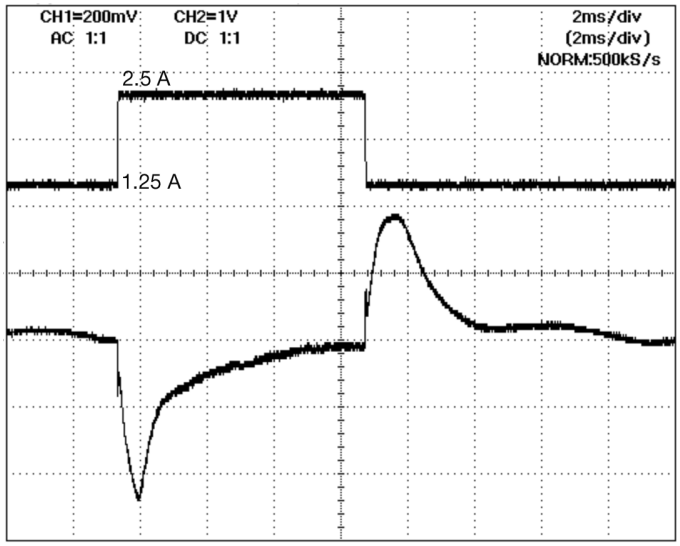

Figure 16. Transient Response of Example Power Supply with CF1 Replaced with the Original 100 nF Capacitor.

when the load is reduced (to 1 A), due to the supply operating in discontinuous conduction mode (DCM) the gain is drastically reduced having the effect of stabilizing the power supply. This is seen in the fact that there are no oscillations on the lower step of the load.

Let us now increase the resistor RF3 to 200 Ω. This has the effect of reducing the gain and should tend to stabilize the system and provide some phase margin. The corresponding response is shown in Figure 11. We can see from Figure 12 that the system is now just stable but still has very little phase margin, indicated by damped oscillations before settling down to a steady-state while loaded at 2.1 A.

Let us now replace the resistor RF3 to its original value of 1 kΩ. Let us see the effect of reducing capacitance CF1 (C12 in Figure 1) of the compensation circuit. From our knowledge of controller transfer function (see Appendix B) we expect the location of the compensation zero to shift higher in frequency. This also has the effect of lower phase boost and should thus translate to lower phase margin. Let us use a value of 2.2 nF instead of the original 0.1 μF. Figure 13 shows the transient load plot.

What we see here is a step load from 1.25 A to 2.5 A (50% to 100%) It is important to note here that at 1.25 A the supply operates in DCM and at 2.5 A the supply operates in CCM.

Let us first analyze the transient response when load is 2.5 A. The effect of lowering the compensation capacitor has reduced the phase margin. This is apparent from the damped oscillations. Clearly this design would be unacceptable from the phase margin in CCM viewpoint. However in DCM we see an even more interesting phenomenon. When the load is dropped to 1.5 A we see that the power supply enters DCM. The supply violates conditional stability and oscillates.

Let us see the effect of slowly increasing the value of the compensation capacitor from 2.2 nF up to its original value of 0.1 μF where we know it stabilizes the power supply. Figure 14 shows the transient response with a value of 0.01 μF.

We see here that while the phase margin problem is reduced the phase margin in DCM is still very low. The oscillations are damped but pronounced. Figure 15 shows the effect of using a 22 nF capacitor.

The phase margin is better, indicated by smaller amplitude oscillation. Increasing the capacitor to 100 nF solves this problem (Figure 16). The supply is stable under both CCM and DCM for this condition of line voltage. The same testing should be performed at high and low-line voltages to make sure that power supply is stable over entire operating range.

Appendix A

The Power Stage Transfer Function

The power stage comprises of the transformer, TOPSwitch, secondary diode and output capacitor. The power stage transfer function for a flyback converter operating in continuous conduction mode can be represented as

$$P(s) = G(s) \times H(s) \quad (9)$$

where
G(s) is the transfer function of the non-linear switching elements (the switch, transformer and secondary side diode) and is given by

$$G(s) = K_P \times \left(1 - \frac{s}{\omega_{RHP}}\right) \quad (10)$$

where
K_P, the gain of the power stage is a function of the output voltage V_O and operating duty cycle D, is given by

$$K_P = \frac{V_O}{D \times (1 - D)} \times \frac{N_S}{N_P} \quad (11)$$

In addition, the power stage contributes a right half plane zero (RHP zero).

This zero cannot be compensated for but fortunately in off-line low voltage applications it occurs far beyond the desired crossover frequency and in most cases it does not significantly affect design performance. The RHP zero frequency can be calculated using the expression

$$\omega_{RHP} = \frac{R_O}{L_E \times D} \quad (12)$$

where
R_O is the output load impedance and L_E is the effective inductance referred to the secondary side and is given by the expression

$$L_E = \frac{L \times \left(\frac{N_S}{N_P}\right)^2}{(1 - D)^2} \quad (13)$$

where
N_S = Number of secondary turns
N_P = Number of primary turns
L = Primary inductance of transformer
D = Duty cycle of primary switch

H(s) is the transfer function of the LC filter formed by the effective inductance L_E and the output capacitor,

$$H(s) = \frac{\omega_N \left(1 + \frac{s}{\omega_{ESR}}\right)}{s^2 + \frac{2\zeta\omega_N}{Q} \times s + \omega_N^2} \quad (14)$$

where
ω_N = Natural frequency of LC tank
ω_{ESR} = Zero frequency of ESR of output capacitor

Figure 17 shows the magnitude response of the power stage P(s) and also the response from the separate components G(s) (shown in the Figure as G(s) and H(s) that form the power stage.

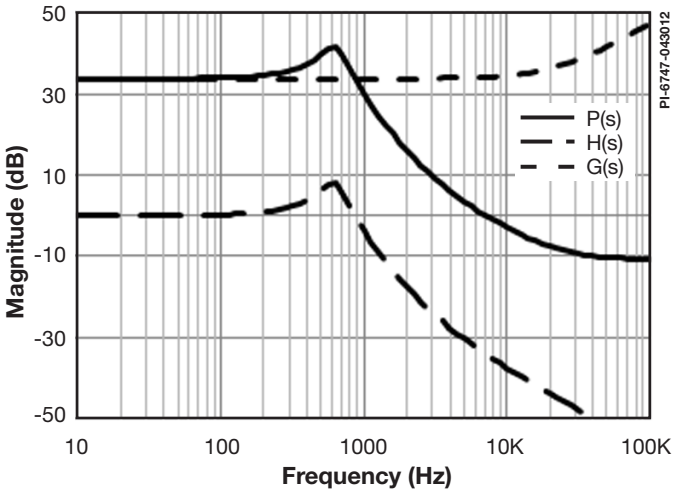

Figure 17. Magnitude Response of the Ideal Power Stage.

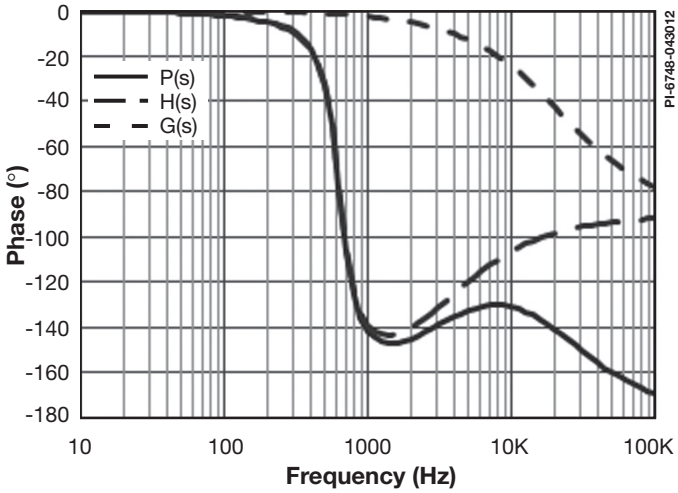

Figure 18. Phase Response of the Ideal Power Stage.

Figure 18 shows the corresponding phase response in the frequency domain.

The LC tank circuit contributes a double pole at the corner frequency of L_E and C_O and its response is a standard second order response containing a resonant frequency a damping factor and a Q factor. The characteristic of this double pole H(s) is given by

$$H(s) = \frac{1}{L_E \times C_O} \times \left(\frac{1}{s^2 + \frac{s}{Q} \times \left(\frac{1}{R_O \times C_O} + \frac{r}{D \times L_E}\right) + \frac{1}{L_E \times C_O}}\right) \quad (15)$$

where
r = ESR of output capacitor
R_O = Equivalent output resistance of load
Q = Q-factor of the LC circuit
C_O = Output capacitance

Additionally, the output capacitor's ESR contributes a zero to the transfer function and the location of this zero is given by

$$\omega_{ESR} = \frac{1}{rC_O} \quad 16$$

The Q factor influences the crossover peaking of the double pole. Notice in Figure 17 that the peaking occurs at the resonant frequency of the LC filter. However, for flyback power supplies, the overall damping effect is so prominent that very little or no gain peaking is observed at the double pole crossover frequency. This could be physically attributed to the fact that the windings and traces have sufficient ohmic resistance to provide damping at resonance. Thus the Q factor value is much lower in practical situations and should be therefore adjusted such that at the double pole frequency there is no gain peaking.

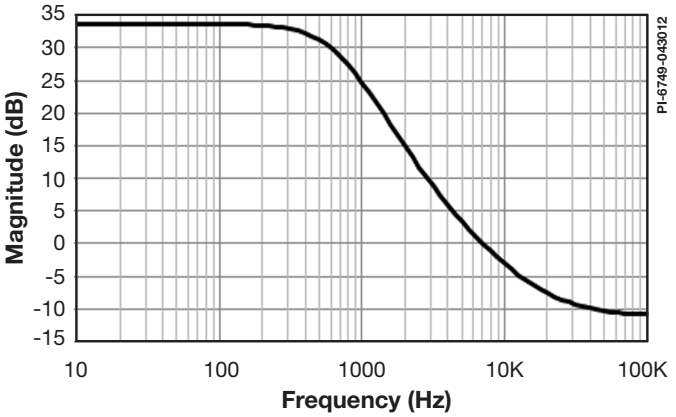

Figure 19. Magnitude Response of a Low Q Power Stage Shows No Gain Peaking at Resonant Frequency.

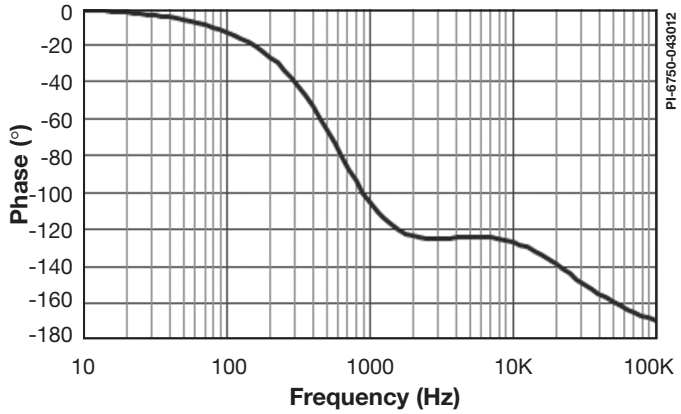

Figure 20. Phase Response of Low Q Circuit.

In practical circuits a Q value of 0.1 to 0.3 has proven to give useful overall results.

Power Stage Response in DCM

If the power supply is in discontinuous conduction mode (DCM) the transfer function is different and is characterized by the following equation

$$P(s) = K_P \times \frac{1 + \frac{s}{\omega_{ESR}}}{1 + \frac{s}{\omega_P}} \quad 17$$

Where
ω_P = Frequency of pole formed by R_O and C_O.

The gain K_P is lower than in CCM by a factor of (1-D), which causes the power supply to crossover at a much lower frequency

$$K_P = \frac{V_O}{D} \times \frac{N_S}{N_P} \quad 18$$

The transfer function has a zero contributed by the ESR of the output capacitor, which occurs at the same frequency as in CCM and is given by equation (16). This is an approximate expression of the transfer function for DCM and it ignores the pole created by inductor and also ignores the RHP zero since both these occur at very high frequencies and do not affect the response in the region of interest. There is no double pole in the response in DCM and the only pole that results is formed by the output capacitance and the load and the frequency at which it appears is given by,

$$f_P = \frac{2}{2\pi \times R_O \times C_O} \quad 19$$

It should be clear from equation (16) that since there is no double pole in DCM response it is much easier to stabilize than a CCM circuit. The other difference is that the power system gain in DCM operation is much lower than in CCM operation and this aspect can also be very easily handled while designing the loop.

APPENDIX B

Control Circuit – Design and Objectives

Ideally the goal for any control loop should be to have a high gain at DC frequency and high crossover frequency (high bandwidth), which will allow the circuit to respond rapidly to perturbations, i.e. minimize the dynamic load response time. The bandwidth should not be unnecessarily higher than is required because in that case the loop becomes noise sensitive to attack the feedback circuit.

The loop gain of the amplifier at DC (0 Hz) should be as high as possible. This minimizes the steady-state error and ensures good load regulation.

In voltage mode control there is no inherent rejection of line frequency ripple on the DC bus capacitor voltage, which results in an increase in the line frequency ripple in the output voltage. This is why you should have a high gain all the way up to 120 Hz after which the magnitude should steadily fall and crossover at the desired frequency. In TOPSwitch devices there is a feed-forward feature which modulates the duty cycle based on the DC bus ripple. This greatly reduces this 120 Hz (or 100 Hz) line frequency component in the output voltage ripple.

Type 1, Type 2 and Type 3 Compensation Circuits

The stabilization of loops in power supplies can be achieved by using one of three popular controller types. These three circuit types provide different degrees of freedom to manipulate the phase and gain response curves. These three circuits have come to be known as type 1, type 2 and type 3 circuits in some literature.

The first circuit (type 1) only adds a pole at 0 Hz. It is a single pole compensation circuit. However, it is rarely used for TOPSwitch applications.

The second circuit (type 2) adds another pole zero pair to the type 1 circuit thus providing phase boost to the overall phase response. It is a 2 pole 1 zero type of compensation circuit.

The third circuit (type 3) adds yet another pole zero pair to provide some more phase boost to the phase response of the circuit. It is a 3 pole 2 zero type of compensation circuit.

Controller Model

The “controller” is the TOPSwitch and the TL431. Thus the combined characteristic of the controller should be achieved by the combination of the TOPSwitch and the TL431 characteristic.

Figure 21 and Figure 22 show the magnitude and phase response respectively, of the type 2 compensation circuit. This circuit has characteristics of a 2 pole and 1 zero response with the zero sandwiched between the poles. One pole is placed at a very low frequency (limited by the open-loop gain of the TL431) and the other zero is placed at a frequency greater than the desired crossover frequency. The zero is then placed at a frequency much lower than the loop gain crossover.

At low frequencies the controller acts like an integrator with high gain, which is only limited by the open-loop gain of the TL431 (about 55-60 dB).

At high frequencies the controller again acts like an integrator.

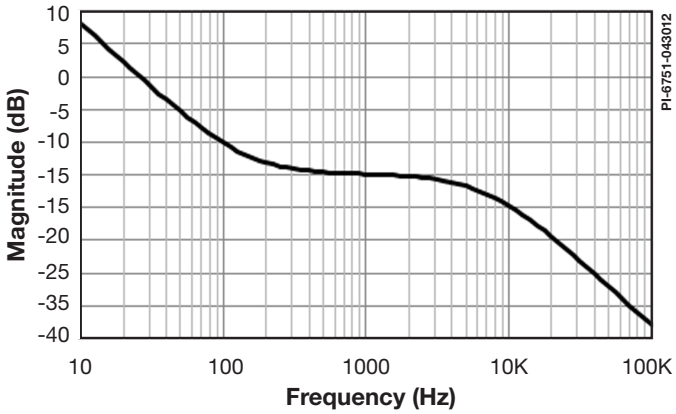

Figure 21. Magnitude Response of the Typical Type 2 Controller.

At mid frequencies the gain response flattens out and the phase is boosted (Figure 21). This is one of the most critical aspects of the controller design – the relative position of the poles and zero in order to get the maximum possible phase boost at the desired crossover frequency

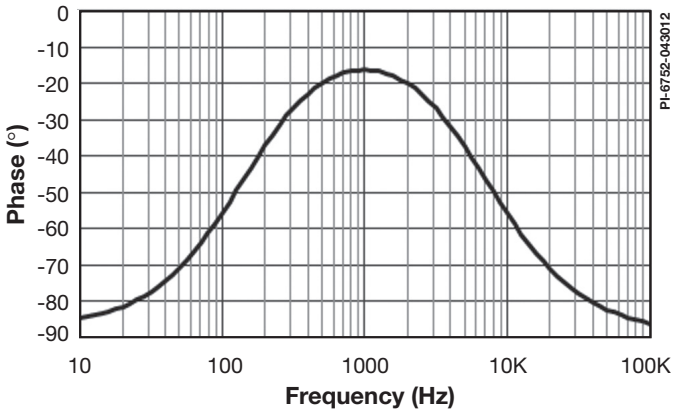

Figure 22. Phase Response of the Typical Type 2 Controller Circuit.

Figure 21 shows the location of the poles and zeros. We will now delve into the design of the circuit that will introduce these poles and zeros and also looks at how to control their position in the frequency domain in order to meet our control objectives.

It was pointed out earlier that the TOPSwitch and the TL431 circuit together form the controller. Let us now take a closer look at the model of the TOPSwitch and TL431 and see how they can help us to achieve the controller gain phase characteristic

Modeling the TOPSwitch

In addition to serving as the gate for control signals, the control pin also provides power for the control circuitry (like auto-restart, UV/OV lockout, hysteretic thermal shutdown etc) inside the TOPSwitch. This is achieved by using a 47 µF capacitor (CF3) at the control pin. In addition, a small value series resistor (RF5) is also recommended (Figure 23)

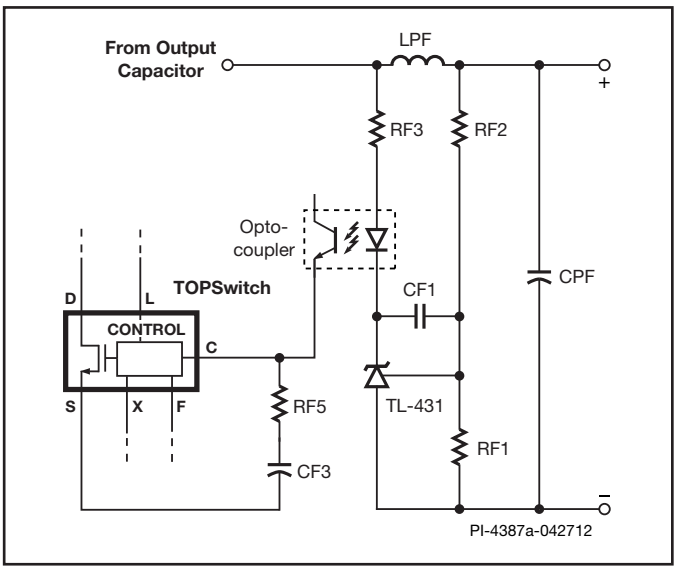

Figure 23. Type 2 Controller Circuit Realization.

The control circuitry inside the TOPSwitch has a shunt regulator which maintains the control pin voltage at 5.8 V and a series impedance Z_C maintains the input impedance at the control pin constant. This Z_C is in the range of 10 Ω - 20 Ω. These two components, CF3 and RF5, which are external to the TOPSwitch, together with the input impedance of the control pin Z_C form a pole zero pair. The pole and zero frequencies are given by

$$f_{ZERO(TOP)} = \frac{1}{2\pi \times CF3 \times RF5} \quad (20)$$

$$f_{POLE(TOP)} = \frac{1}{2\pi \times CF3 \times Z_C} \quad (21)$$

In addition, there is also an internal 7 kHz pole ($f_{TOPSWITCH}$) within the controller and serves as a noise filter. Since TOPSwitch accepts a current signal input I_C, the Transfer function is expressed in the form described by equation (22)

$$G_{TOP}(s) = \frac{D(s)}{I_C(s)} = K_{TOP} \times \frac{\left(1 + \frac{s}{\omega_{ZERO(TOP)}}\right)}{\left(1 + \frac{s}{\omega_{POLE(TOP)}}\right) \times \left(1 + \frac{s}{\omega_{TOPSWITCH}}\right)} \quad (22)$$

where
K_{TOP} is the gain of the TOPSwitch controller.

This gain (K_{TOP}) of the TOPSwitch can be obtained from the curves of duty cycle (d) against control pin current (IC) from the data sheets. The gain of the stage is the slope of this curve and is equal to 0.2 / mA.

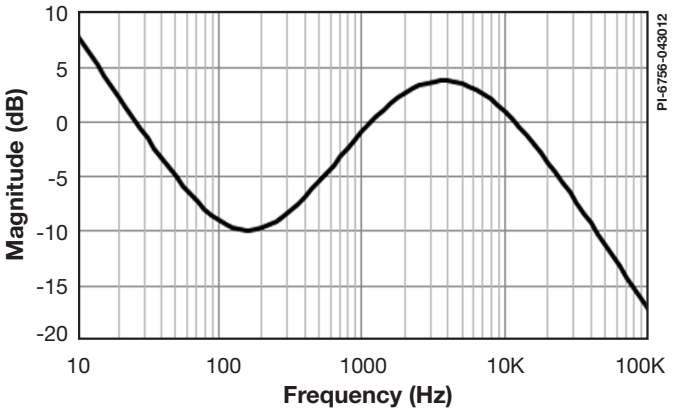

Figure 24. Magnitude Response of Circuit Shown in Figure 26. 3 Poles and 2 Zeros are Strategically Placed to Provide Boost in the Phase.

For the TOPSwitch-JX family the gain is double (0.4 / mA).

Modeling the TL431

The TL431 circuit is shown in Figure 23 and feeds a current signal into the TOPSwitch IC CONTROL pin through the optocoupler. With this in mind it is easy to see that the transfer function of interest is $I_C(s)$ to $V_O(s)$. For the purpose of simplicity if we replace the TL431 with a non- ideal opamp then using linear circuit theory we can write down the transfer function as

$$G_{TL431}(s) = \frac{I_C(s)}{V_O(s)} = K_{TL431} \times \frac{\left(1 + \frac{s}{RF2 \times CF1}\right)}{\left(1 + \frac{s}{K_{TL431} \times RF2 \times CF1}\right)} \quad (23)$$

where
K_{TL431} = Open-loop gain of TL431.

Revisiting the Controller Model

Now that we have established the transfer functions of the individual controller stages we can combine the TL431 and TOPSwitch transfer functions to form the controller transfer function.

$$G_{CONTROLLER}(s) = G_{TL431}(s) \times G_{TOP}(s) \quad (24)$$

Also, noting that the pole zero pair formed by $\omega_{POLE(TOP)}$ and $\omega_{ZERO(TOP)}$ are very close to each other and by a first degree of approximation cancel each other out as the value of RF5 approaches the value of Z_C. Neglecting this pole zero pair we can write the approximate transfer function of the controller as

$$G_{CONTROLLER}(s) \approx K_C \times \frac{\left(1 + \frac{s}{RF2 \times CF1}\right)}{\left(1 + \frac{s}{K_T \times RF2 \times CF1}\right) \times \left(1 + \frac{s}{2\pi f_{TOPSWITCH}}\right)} \quad (25)$$

where
K_C is the total controller gain.

This equation is now very similar to the type 2 controller.

Generally speaking, the type 2 controller is sufficient to obtain 45° or greater of phase margin and crossover at about 1 kHz. If there is need for additional phase margin the controller can be slightly modified to give more phase boost. This is referred to as the "phase boost circuit" and will be described later on in the document.

When initially selecting the compensation circuit use the type 2 compensation circuit, and then if there is insufficient phase margin and all attempts to fine tune the circuit have failed, then use the modified type 2 circuit.

In theory, the location of one of the poles is at the origin (0 Hz). But due to finite gain of the TL431 this pole usually occurs at around 0.05 Hz. This also explains why the phase lag at DC (0 Hz) is 0° and not -90°.

The pole frequency is fixed at 7 kHz ($f_{TOPSWITCH}$) since there is a 7 kHz internal pole readily available with all TOPSwitch devices. Thus

$$f_{POLE} = f_{TOPSWITCH} = 7\ kHz \qquad 26$$

The zero frequency should be carefully chosen so as to provide maximum phase boost at the desired crossover frequency (usually 1 kHz is a good choice).

Place the zero at

$$f_{ZERO} = \frac{f_{CROSSOVER}^{2}}{f_{POLE}} \qquad 27$$

For 1 kHz crossover frequency then

$$f_{ZERO} = \frac{1\ kHz \times 1\ kHz}{7\ kHz} = 143\ Hz \qquad 28$$

In practice, select f_{ZERO} to be 100 Hz so that the gain component will remain high at 120 Hz and reduce the line frequency ripple on the output.

Phase Boost Network

This network is seldom required. Some cases where this circuit may be required are

- Multiple of outputs.
- The power stage is underdamped (high Q circuit).
- Despite all efforts, the type 2 circuit does not provide adequate phase margin.

This circuit gives the ability to add another 20° - 30° of phase margin (Figure 26) over the conventional type 2 circuit, which generally gives a total phase boost of up to about 60°.

This phase boost network circuit is shown in Figure 26. An RC network is placed in parallel with RF3. The idea here is to provide a boost in phase without affecting the magnitude response prior to gain crossover. The principle of this circuit is that the phase of a first order system starts to change long before the corner frequency. Thus if we place a zero (f_{ZERO_2})

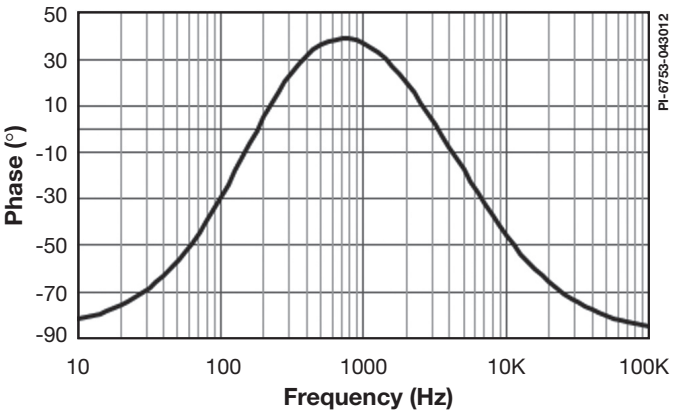

Figure 25. Phase Boost of Up to 90° Can be Achieved with the Use of Circuit Shown in Figure 26.

just after the gain crossover frequency we will see that the loop phase is boosted even though the magnitude response remains relatively unchanged until the corner frequency is reached. Place the pole (f_{POLE_2}) a decade above the zero so as to roll off the response. Thus we can write the design equations as follows

$$f_{ZERO\_2} = f_{CROSSOVER} \qquad 29$$

$$f_{POLE\_2} = 10 \times f_{ZERO\_2} \qquad 30$$

In some cases it may be necessary to actually extend the location of f_{ZERO_2} such that it occurs at a location beyond the crossover frequency.

With elementary control theory and use of equations 29 and 30 we can very easily derive the design equations for the components RF4 and CF2 as expressed in equation 6 and equation 7.

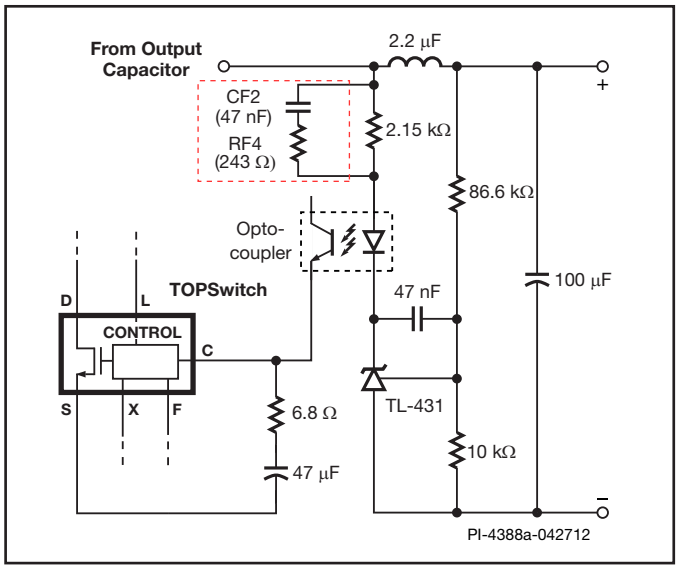

Figure 26. Phase Boost Network (RF4 and CF2) Placed Across RF3 Resistor to Increase Phase at Gain Crossover.

Revision	Notes	Date
A	Initial Release.	06/12

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