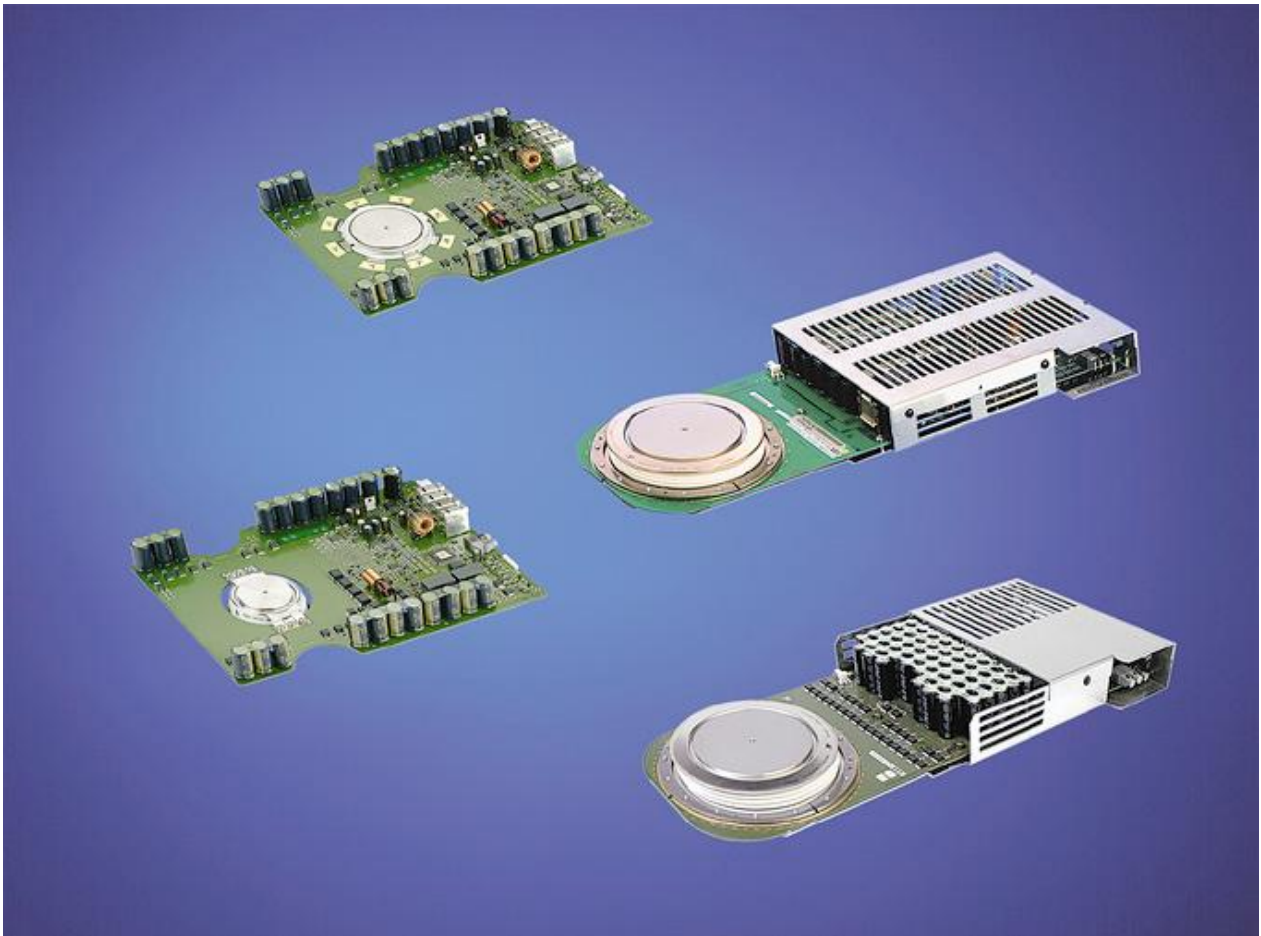


# Integrated Gate Commutated Thyristors

## Application Note

# Applying IGCTs



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# Applying IGCTs

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October 2007

## 1 Introduction

The Integrated Gate Commutated Thyristor (IGCT) has become the power semiconductor of choice in Medium Voltage Industrial Applications. Also in Energy Management and the Traction markets, the versatility of this power switch has enabled performance improvements and cost savings in a variety of applications.

The outstanding feature of the IGCT - leading to its name and its main advantages - is not only the silicon wafer itself, but the way it is driven by the gate - the electrical and mechanical gate-drive design. The "hard-drive" concept at the heart of IGCT operation requires the mechanical integration of gate driver and semiconductor into one single unit with low circuit inductance. It also implies a number of new converter features, which make IGCT converters different from GTO or IGBT converters. It is the scope of this application note to make designers familiar with the datasheets and the use of IGCTs in their main application areas. The following features are important to remember:

- no turn-off snubber is needed in applications without series connection; where turn-off snubbers are used, they are considerably smaller than those of GTOs
- the customer control interface is reduced to a power supply , an optical control input and an optical status feedback output
- gate drive geometry is an important parameter in mechanical stack design.

It should be noted that "IGCT" is a generic reference to the complete device. "GCT" refers to the semiconductor press-pack component. Further distinctions can be made to distinguish *RC-IGCTs* (reverse-conducting), *RB-IGCTs* (reverse blocking) and *AS-IGCTs* (asymmetric with neither reverse blocking nor reverse-conducting capability). ABB sells only *IGCTs* whereas other manufacturers may offer the GCT and gate-unit separately. The term "SGCT" is also used by some suppliers to designate a "symmetric blocking" device, known here as an *RB-IGCT* per the above definition.

This application note covers the asymmetric and reverse conducting IGCTs. The first part is a user's guide to IGCT datasheets. In the 2<sup>nd</sup> part application-specific topics are illustrated.

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## 2 Table of contents

<b>1</b>	<b>INTRODUCTION</b>	<b>2</b>
<b>2</b>	<b>TABLE OF CONTENTS</b>	<b>3</b>
<b>3</b>	<b>DATASHEET USER'S GUIDE</b>	<b>5</b>
3.1	KEY PARAMETERS AND FEATURES	5
3.2	BLOCKING	6
3.3	MECHANICAL DATA	7
3.4	GCT DATA	8
3.4.1	On-state of IGCT	8
3.4.2	Turn-on switching	10
3.4.3	Turn-off switching	11
3.5	GATE UNIT DATA	13
3.5.1	Power supply	13
3.5.2	Optical control input/output	13
3.5.3	Connectors	14
3.5.4	Visual feedback	14
3.6	THERMAL	15
3.7	DIAGRAMS	17
3.7.1	GCT on-state current vs. on-state voltage	17
3.7.2	GCT surge current vs pulse width and number of pulses	18
3.7.3	GCT turn-off characteristics	18
3.7.4	Gate unit related diagrams	19
3.8	DIODE-SPECIFIC DATA OF REVERSE CONDUCTING IGCTs (FROM DATASHEET 5SHX 26L4510)	20
3.8.1	Diode On-state	20
3.8.2	Diode turn-on	20
3.8.3	Diode turn-off	21
3.8.4	Thermal data	21
<b>4</b>	<b>IGCT APPLICATION-SPECIFIC TOPICS</b>	<b>22</b>
4.1	IGCTs IN VOLTAGE SOURCE INVERTERS (VSI)	22
4.1.1	Design criteria	23
4.1.2	Determining the design parameters	24
4.1.3	Determining the value of the di/dt limiting inductor	25
4.1.4	Determining the value of the clamp capacitor $C_{CL}$ and the damping resistor $R_S$	25
4.1.5	Stray inductance $L_{CL}$	27
4.1.6	Influence of the clamp diode type	28
4.1.7	Overview of parameter influences	29
4.1.8	Use of additional snubber	29
4.2	RETRIGGERING OF AN IGCT	31
4.2.1	Introduction	31
4.2.2	When are external retrigger pulses required?	31
4.2.3	How are external retrigger pulses released?	32
4.2.4	What is the best timing for the external retrigger?	33
4.2.5	Applications requiring retrigger pulses	33
4.3	SERIES CONNECTION OF IGCTs	34
4.3.1	Design criteria	36

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4.3.2	Snubber concepts .....	36
4.3.3	Scaling of clamp design .....	37
4.3.4	Factors influencing turn-off voltage sharing.....	37
4.3.5	Optional anode voltage monitoring .....	40
4.3.6	Conclusions.....	40
4.4	PROTECTION .....	41
4.4.1	Consequence of a GCT or diode failure in a 3-level phase-leg.....	41
<b>5</b>	<b>GLOSSARY .....</b>	<b>42</b>
<b>6</b>	<b>ADDITIONAL NOTES.....</b>	<b>43</b>
6.1	REFERENCES.....	43
6.2	APPLICATION SUPPORT .....	43

### 3 Datasheet user's guide

This section is a detailed guide to the correct understanding of an IGCT data sheet. Parameters and ratings will be defined and illustrated by figures where appropriate, while following the sequence in which parameters appear in the datasheet. For explanation purposes, data and diagrams associated with IGCT type 5SHY 35L4510 have been used, but because all IGCTs have similar datasheets, this guide is applicable to all IGCTs. Additionally a 5SHX 26L4510 datasheet is used to explain the diode parameters of reverse-conducting devices.

The datasheets distinguish between maximum rated values and characteristic values. Maximum rated values indicate limits beyond which damage to the device may occur. Characteristic values are parameters defined under typical application conditions.

ABB reserves the right to change datasheets without notice. Therefore, for the latest version, please visit our website at [www.abb.com/semiconductors](http://www.abb.com/semiconductors).

#### 3.1 Key Parameters and features

$V_{\text{DRM}}$	=	4500 V	<b>Asymmetric Integrated Gate- Commutated Thyristor 5SHY 35L4510</b>
$I_{\text{TGQM}}$	=	4000 A	
$I_{\text{TSM}}$	=	$32 \times 10^3$ A	
$V_{(\text{T0})}$	=	1.4 V	
$r_{\text{T}}$	=	0.325 mW	
$V_{\text{DC-link}}$	=	2800 V	

Doc. No. 5SYA1232-02 June 07

- High snubberless turn-off rating
- Optimized for medium frequency (<1 kHz) and wide temperature range
- High reliability
- High electromagnetic immunity
- Simple control interface with status feedback
- AC or DC supply voltage
- Contact factory for series connection



These key *features* briefly describe the IGCT without reference to operating conditions. The data presented here also appears in the corresponding section of the data sheet, together with operating or test conditions. For example,  $I_{\text{TSM}} = 32 \times 10^3$  A can also be found in the on-state section, where this value applies at  $t_p = 10$  ms and  $T_{vj} = 125$  °C, with zero reapplied voltage.

## 3.2 Blocking

### Maximum rated values

Parameter	Symbol	Conditions	min	typ	max	Unit
Rep. peak off-state voltage	$V_{\text{DRM}}$	Gate Unit energized			4500	V
Permanent DC voltage for 100 FIT failure rate of GCT	$V_{\text{DClink}}$	Ambient cosmic radiation at sea level in open air. Gate Unit energized			2800	V
Reverse voltage	$V_{\text{RRM}}$	IGCT in	off-state		17	V
			on-state		10	V

### Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
Rep. peak off-state current	$I_{\text{DRM}}$	$V_{\text{D}} = V_{\text{DRM}}$ , Gate Unit energized			50	mA

### $V_{\text{DRM}}$

$V_{\text{DRM}}$  is the maximum repetitive voltage in the forward direction. The IGCT is able to block this voltage at line frequencies of 50 or 60 Hz, assuming a sinusoidal voltage waveform.  $V_{\text{DRM}}$  is a maximum rating; if exceeded, leakage current and power loss may increase rapidly and may lead to thermal runaway and subsequent blocking degradation.

Although  $V_{\text{DRM}}$  specifies the IGCT's quasi-static blocking capability, it is, in fact, the maximum dynamic voltage,  $V_{\text{DM}}$ , that IGCTs can withstand following turn-off. It is important to note that the IGCT can only block rated voltage if the gate unit is energized.

### $V_{\text{DC-link}}$

$V_{\text{DC-link}}$  is the maximum continuous DC voltage for a specified failure rate (100 FIT for example), due to cosmic radiation. Exceeding this voltage does not immediately lead to device failure, but the probability of a cosmic radiation failure increases progressively with applied DC voltage. A detailed explanation and IGCT type-specific calculations are printed in the application note 5SYA2046 "Failure rate of IGCTs due to cosmic rays".

### $V_{\text{RRM}}$

$V_{\text{RRM}}$  is the maximum repetitive voltage in the reverse direction. For all asymmetric IGCTs, this value is in the range of 17 V. It is determined by the reverse blocking capability of the gate-to-cathode junction ( $V_{\text{GRM}}$ ). The datasheet distinguishes between off-state ( $V_{\text{RRM}} = 17$  V) and "on-state" ( $V_{\text{RRM}} = 10$  V). The reduced reverse voltage rating in the "on-state" is determined by the status feedback, which sends an error signal if a reverse voltage greater than 10 V is detected while the device is gated "on". If the controller does not use the feedback signal, it is possible to allow reverse voltages of up to 17 V with the device gated "on".

In these conditions, the term "on-state" refers to the gating status i.e. the controller may order the device to be "on" but circuit conditions may require the anti-parallel diode to conduct, a condition which will cause a forward voltage across the diode and hence, negatively across the IGCT; in this condition it is the diode part of the GCT/diode combination which is in the on-state.

Thus when an anti-parallel freewheeling diode conducts, an IGCT reverse voltage appears due to stray inductance and to the diode's forward recovery voltage spike at high di/dt. If this exceeds the rated value,  $V_{\text{RRM}}$ , the IGCT will be driven into reverse avalanche. This condition is not harmful for the device, provided avalanche time and current are below 10  $\mu\text{s}$  and rated  $I_{\text{TGM}}$ , respectively.

### $I_{\text{DRM}}$

$I_{\text{DRM}}$  specifies the maximum leakage current, when  $V_{\text{DRM}}$  is applied. It is measured at  $T_{\text{vj max}}$ , with sinusoidal voltage pulses ( $t_p = 10$  ms) and an energized gate unit.

### 3.3 Mechanical data

#### Maximum rated values

Parameter	Symbol	Conditions	min	typ	max	Unit
Mounting force	$F_m$		36	40	44	kN

#### Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
Pole-piece diameter	$D_p$	$\pm 0.1$ mm		85		mm
Housing thickness	H		25.3		25.8	mm
Weight	m				2.9	kg
Surface creepage distance	$D_s$	Anode to Gate	33			mm
Air strike distance	$D_a$	Anode to Gate	10			mm
Length	l	$\pm 1.0$ mm		439		mm
Height	h	$\pm 1.0$ mm		40		mm
Width IGCT	w	$\pm 1.0$ mm		173		mm

#### $F_m$

$F_m$  is the mounting force necessary to establish a good electrical and thermal contact. It is very important that  $F_m$  stays within the specified limits, even under limiting operating temperature. Thermal expansions and tolerances of stack parts have to be considered in the design of the clamping system. Too low a mounting force results in increased thermal resistance and - particularly at high currents - in damage to the dry interfaces *within* the housing that may provoke degradation. Also the individual cathode segments might not all be correctly contacted, leading to an increase in  $V_T$  and drastic reduction of  $I_{TSM}$  and  $I_{TGQM}$ .

Exceeding  $F_m$  leads to increased mechanical stress on the silicon wafer, particularly where thermal cycling is severe. This reduces life-expectancy of the device and can lead to premature wear-out of the cathode segment metallization with subsequent gate-to-cathode short circuits.

Besides a correct mounting force, it is also vital that the pressure is distributed homogeneously over the contact area. If not, the copper pole pieces of the housing may deform plastically, which in turn, may lead to localized mechanical stress on the silicon wafer with subsequent degradation of the device performance or even fracturing of the wafer. Details concerning a correct clamping system are described in Application Note 5SYA2036 "Recommendations regarding mechanical clamping of Press Pack High Power Semiconductors".

*Note:* If no external force is applied across a press-pack semiconductor, the silicon wafer will probably not contact the pole pieces at all. For even the most basic device verifications (blocking or gating checks by service personnel), a minimum clamping force of about 1 kN is required to establish contact for *low-current* measurements.

#### $D_p, H, l, h, w$

These mechanical parameters are described in the outline drawing in the datasheet.

#### m

The weight of the complete device, including the gate unit.

#### $D_s$

The surface creepage distance is defined as the *shortest path along the ceramic surface* between the anode flange and the gate contact.

#### $D_a$

The air strike distance is defined as the *shortest direct path* between the anode side and the gate contact.

### 3.4 GCT Data

#### 3.4.1 On-state of IGCT

Maximum rated values <sup>1)</sup>

Parameter	Symbol	Conditions	min	typ	max	Unit
Max. average on-state current	$I_{T(AV)M}$	Half sine wave, $T_C = 85\text{ °C}$ , Double side cooled			1700	A
Max. RMS on-state current	$I_{T(RMS)}$				2670	A
Max. peak non-repetitive surge on-state current	$I_{TSM}$	$t_p = 10\text{ ms}$ , $T_j = 125\text{ °C}$ , sine wave after surge: $V_D = V_R = 0\text{ V}$			$32 \times 10^3$	A
Limiting load integral	$I^2t$				$5.12 \times 10^6$	$A^2s$
Max. peak non-repetitive surge on-state current	$I_{TSM}$	$t_p = 30\text{ ms}$ , $T_j = 125\text{ °C}$ , sine wave after surge: $V_D = V_R = 0\text{ V}$			$21 \times 10^3$	A
Limiting load integral	$I^2t$				$6.62 \times 10^6$	$A^2s$
Stray inductance between GCT and antiparallel diode	$L_D$	Only relevant for applications with antiparallel diode to the IGCT			300	nH
Critical rate of rise of on-state current	$di_T/dt_{cr}$	For higher $di_T/dt$ and current lower than 100 A an external retrigger puls is required.			200	A/ $\mu$ s

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
On-state voltage	$V_T$	$I_T = 4000\text{ A}$ , $T_j = 125\text{ °C}$		2.35	2.7	V
Threshold voltage	$V_{(T0)}$	$T_j = 125\text{ °C}$ $I_T = 1000 \dots 4000\text{ A}$			1.4	V
Slope resistance	$r_T$				0.325	m $\Omega$

#### $I_{T(AV)M}$ , $I_{T(RMS)}$

The max. average and root-mean-square on-state currents, respectively. These values are established with given boundary conditions.  $I_{T(AV)M}$  and  $I_{T(RMS)}$  are the average and RMS values of the half-sinusoidal on-state current when the junction operates at its maximum temperature with the case temperature fixed at a given value, here 85 °C.

These figures give a comparative value for current handling capability at low frequency (negligible switching losses). They are mainly used to compare different products for on-state performance and they indicate a maximum current capability for the defined temperatures. As with all comparisons, the thermal conditions must be considered as they may differ from product to product and between suppliers, which substantially influences the current ratings.

The user can easily calculate  $I_{T(AV)M}$  and  $I_{T(RMS)}$ , under varying conditions, from the following equations:

$$I_{T(AV)M} = 2 \frac{\sqrt{V_{(T0)}^2 + r_T \cdot P^2 \cdot P_{(AV)M} - V_{(T0)}}}{r_T \cdot P^2} \quad \text{with:} \quad P_{(AV)M} = \frac{T_{vj\max} - T_C}{R_{th(jc)}}$$

$$I_{T(RMS)} = I_{T(AV)M} \frac{P}{2}$$

The definitions for  $I_{T(AV)M}$  and  $I_{T(RMS)}$  originate from classic phase control thyristor practice, which mainly applies to line frequency applications at 50 and 60 Hz. Since in most IGCT applications, the current waveforms are far from sinusoidal and the switching losses form a considerable part of total power losses,  $I_{T(AV)M}$  and  $I_{T(RMS)}$  have no real practical meaning. However, they may be useful for comparison with other products, as already mentioned.



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## **$I_{TSM}$**

Max. non-repetitive surge current is the max. allowed and pulse-width dependent peak value of a half-sinusoidal surge current, applied at an instant when the IGCT is operating at its maximum junction temperature. Although, in practice, the case temperature prior to a surge is always below 125 °C, both the junction and the housing are heated to 125 °C when the surge current limit is established. This worst-case test condition provides an additional margin to the real stress in an application. For surge current requirements that do not resemble a sine half wave or cannot be covered by a sine half wave shown in Fig. 8, please contact your nearest representative or the address shown at the end of this application note for evaluation.

During a surge, the junction heats up to a temperature well above its rated maximum value. Therefore, the thyristor is no longer able to block rated voltage, so the  $I_{TSM}$  values are valid only for  $V_D = V_R \approx 0$  V after the surge, i.e. without reapplied voltage.

Though a single surge does not cause any irreversible damage to the silicon wafer, it should not be allowed to occur too frequently.

## **$I^2t$**

Limiting surge current load integral  $I^2t$  is an abbreviation and stands for  $\int I_T^2 dt$ . This value is derived from the  $I_{TSM}$  value discussed above, according to the following expression:

$$I^2t = \int_0^{t_p} I_T^2(t) dt = \frac{I_{TSM}^2 \cdot t_p}{2} \quad (\text{for half-sinusoidal waveforms})$$

To protect the IGCT, the  $I^2t$  of a semiconductor fuse must be lower than the maximum  $I^2t$  of the IGCT. The constraints for  $I_{TSM}$  applies similarly to  $I^2t$ .

## **$L_D$**

Stray inductance between IGCT and anti-parallel diode: for optimized switching behavior, it is recommended to minimize  $L_D$  as much as possible. Typical application values are in the range of 30 ... 50nH. However, in the datasheets for asymmetric IGCTs, a maximum  $L_D$  is defined and ABB has verified proper operation up to this high value.

## **$di_T/dt_{cr}$**

This is the critical rate of rise of forward current at IGCT turn-on. Please refer to the detailed description in section 4.3.

## **$V_T$**

$V_T$  is the on-state voltage at a given on-state current  $I_T$  (normally  $I_{TGQM}$ ) and at maximum junction temperature.  $V_T$  is influenced, within limits, by the irradiation dose that determines minority carrier lifetime. A lower  $V_T$  automatically implies a higher  $E_{off}$ , and vice versa. Maximum and typical values are shown.

### $V_{(T0)}$ , $r_T$

In many cases, it is convenient and sufficiently accurate to approximate the on-state characteristic (max. values) by a straight line, determined by  $V_{T0}$  and  $r_T$ :

$$V_T(I_T) = V_{(T0)} + I_T \cdot r_T$$

The current range over which this expression yields acceptable accuracy is indicated by the condition  $I_T = 1000 - 4000$  A (for the 5SHY 35L4510).

When average and RMS values of on-state current,  $I_{T(AV)}$  and  $I_{T(RMS)}$ , are known, the on-state power loss,  $P_{on-state}$ , is readily calculated using  $V_{(T0)}$  and  $r_T$ :

$$P_{on-state} = V_{(T0)} \cdot I_{T(AV)} + r_T \cdot I_{T(RMS)}^2$$

### 3.4.2 Turn-on switching

#### Maximum rated values <sup>1)</sup>

Parameter	Symbol	Conditions	min	typ	max	Unit
Critical rate of rise of on-state current	$di_T/dt_{cr}$	$f = 0..500$ Hz, $T_j = 125$ °C, $V_D = 2800$ V, $I_{TM} \leq 4000$ A			1000	A/ $\mu$ s

#### Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
Turn-on delay time	$t_{don}$	$V_D = 2800$ V, $T_j = 125$ °C			3.5	$\mu$ s
Turn-on delay time status feedback	$t_{don SF}$	$I_T = 4000$ A, $di/dt = V_D / L_i$ $L_i = 5$ $\mu$ H			7	$\mu$ s
Rise time	$t_r$	$C_{CL} = 10$ $\mu$ F, $L_{CL} = 0.3$ $\mu$ H			1	$\mu$ s
Turn-on energy per pulse	$E_{on}$				1.5	J

The definitions of turn-on switching parameters are illustrated on the last page(s) of the IGCT datasheets, with typical anode voltage and current waveforms along with electrical command-signal (CS) and status-feedback signal (SF). These waveforms are reproduced in Fig. 1 and Fig. 2 shows the test circuit.

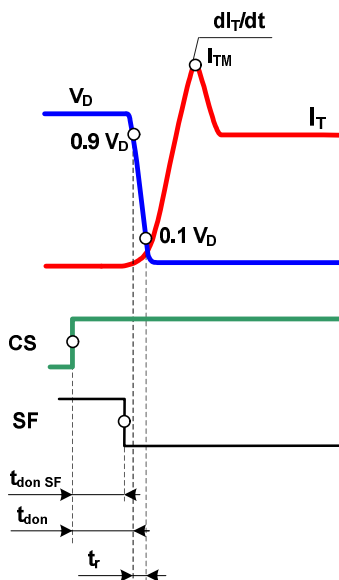


Fig. 1 Turn-on waveforms

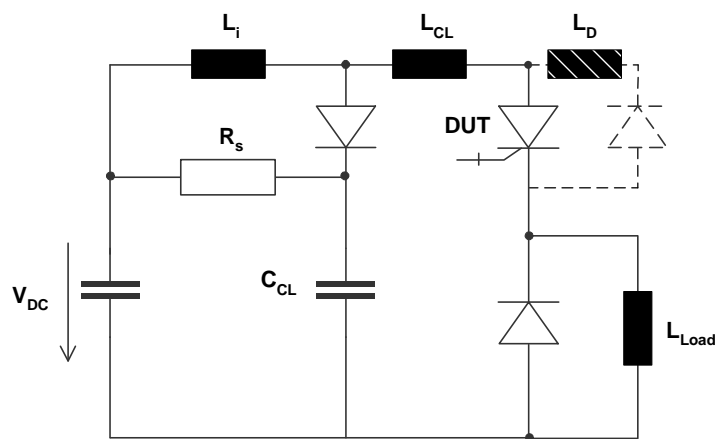


Fig. 2 Turn-on test circuit

### $di_T/dt_{cr}$

The maximum permissible on-state  $di_T/dt$  at turn-on. The maximum  $di_T/dt$  is very much gate current dependent (rate-of-rise-of-gate-current,  $di_G/dt$  and peak gate current amplitude  $I_{GM}$ ). A large gate current ensures that all IGCT cathode segments are turned on simultaneously and within a short time ensuring fast, uniform conduction and avoiding localized conduction and “hot spots”, which could destroy the IGCT. In most applications, turn-on of the IGCT causes a diode turn-off. The maximum diode turn-off  $di/dt$  usually limits the allowed rate of commutation. The turn-on gate conditions ( $di_G/dt$ ,  $I_{GM}$ ) of the gate-unit are designed to amply cover the (turn-off)  $di/dt$  capabilities of fast switching diodes. It would be possible to realize higher  $di_T/dt_{cr}$  for the IGCT but this would unnecessarily increase the losses, input power and cooling requirements of the gate-unit.

### $t_{don}$ , $t_{don SF}$ , $t_r$

Turn-on delay time, turn-on delay time status-feedback and anode voltage fall time, respectively. These definitions are illustrated in Fig. 1.

### $E_{on}$

Turn-on energy per pulse  $E_{on}$  is defined as the time integral of power  $P(t) = I_T(t) \cdot V_D(t)$  during turn-on (from start of commutation until  $V_D$  reaches the static on-state  $V_T$ ):

$$E_{on} = \int I_T(t) \cdot V_D(t) dt$$

The turn-on power losses,  $P_{turn-on}$  of the IGCT, are calculated as follows:

$$P_{turn-on} = f \cdot E_{on}$$

where  $f$  is the switching frequency.

### 3.4.3 Turn-off switching

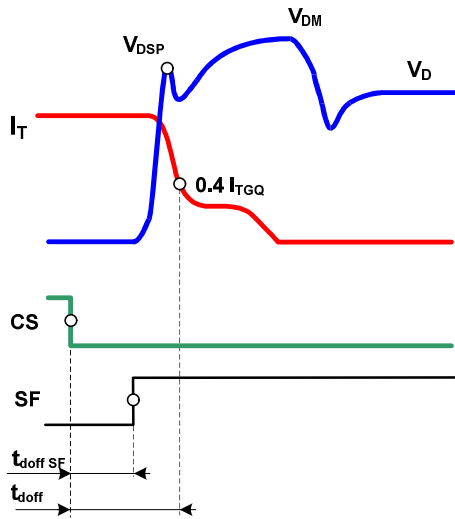
#### Maximum rated values <sup>1)</sup>

Parameter	Symbol	Conditions	min	typ	max	Unit
Max. controllable turn-off current	$I_{TGQM}$	$V_{DM} \leq V_{DRM}$ , $T_j = 125^\circ\text{C}$ , $V_D = 2800\text{ V}$ , $R_S = 0.65\ \Omega$ , $C_{CL} = 10\ \mu\text{F}$ , $L_{CL} \leq 0.3\ \mu\text{H}$			4000	A

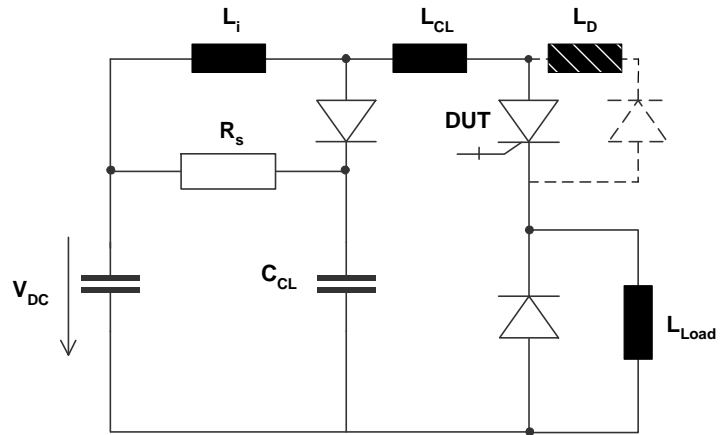
#### Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
Turn-off delay time	$t_{doff}$	$V_D = 2800\text{ V}$ , $T_j = 125\ ^\circ\text{C}$			7	$\mu\text{s}$
Turn-off delay time status feedback	$t_{doff SF}$	$V_{DM} \leq V_{DRM}$ , $R_S = 0.65\ \Omega$ $I_{TGQ} = 4000\text{ A}$ , $L_i = 5\ \mu\text{H}$ $C_{CL} = 10\ \mu\text{F}$ , $L_{CL} = 0.3\ \mu\text{H}$			7	$\mu\text{s}$
Turn-off energy per pulse	$E_{off}$			19.5	22	J

The definitions of the turn-off switching parameters, are illustrated on the last page(s) of the IGCT datasheets, with typical anode voltage and current waveforms along with the electrical command-signal and status-feedback signal. These waveforms are reproduced in Fig. 3 and Fig. 4 shows the test circuit.



**Fig. 3** Turn-off waveforms



**Fig. 4** Turn-off Test circuit

### **$I_{TGQM}$**

$I_{TGQM}$  is the maximum anode current that can be turned-off under the specified conditions. The value of  $I_{TGQM}$  depends on commutation voltage  $V_D$ , junction temperature  $T_{vj}$  and the on-time  $t_{on}$ . These dependencies are specified in the diagram “Safe Operating Area” of the datasheet (see Fig. 11). Turn-off switching outside the safe operating area must be avoided. It may lead to immediate failure even for a single event.

All asymmetric and reverse conducting IGCTs are specified with a “clamp circuit” that limits the voltage but not the  $dv/dt$ . This type of  $di/dt$  snubber is normally used in voltage-source inverters (VSI). Reverse blocking IGCTs are specified with an R-C snubber, which additionally limits the  $dv/dt$  at turn-off. This is a typical snubber for current source inverters (CSI). A low snubber or clamp-inductance is necessary to limit the over-voltage spike  $V_{DSP}$ . Excessive  $V_{DSP}$  can lead to dynamic avalanche breakdown of the GCT and excessive losses.

### **$t_{doff}$ , $t_{doff SF}$**

Turn-off delay time and turn-off delay time status-feedback respectively. These definitions are given in Fig. 3. For more information on the status-feedback see Application Note 5SYA2031 “Applying IGCT Gate Units”

### **$E_{off}$**

Turn-off energy per pulse  $E_{off}$  is defined as the time integral of the power  $P(t) = I_T(t) \times V_D(t)$  during turn-off (from start of commutation until  $I_T$  reaches the static leakage current value):

$$E_{off} = \int I_T(t) \cdot V_D(t) dt$$

The turn-off power losses,  $P_{turn-off}$ , are calculated as follows:

$$P_{turn-off} = f \cdot E_{off}$$

where  $f$  is the switching frequency.

$E_{off}$  can be varied to a certain extent by electron and/or proton irradiation as described earlier in this section for  $V_T$ .  $E_{off}$  varies, to a first approximation, linearly with  $I_{TGQM}$  and  $V_D$ . It is also highly dependent on  $T_{vj}$ .

### 3.5 Gate Unit Data

The important aspects of the gate unit are described in detail in Application Note 5SYA2031 “Applying IGCT Gate Units”.

#### 3.5.1 Power supply

*Maximum rated values <sup>1)</sup>*

Parameter	Symbol	Conditions	min	typ	max	Unit
Gate Unit voltage (Connector X1)	$V_{GIN,RMS}$	AC square wave amplitude (15 kHz - 100kHz) or DC voltage. No galvanic isolation to power circuit.	28		40	V
Min. current needed to power up the Gate Unit	$I_{GIN Min}$	Rectified average current see application note 5SYA 2031	2.1			A
Gate Unit power consumption	$P_{GIN Max}$				100	W

*Characteristic values*

Parameter	Symbol	Conditions	min	typ	max	Unit
Internal current limitation	$I_{GIN Max}$	Rectified average current limited by the Gate Unit			8	A

#### $V_{GIN,RMS}$ :

The gate unit supply voltage is the input voltage range within which the gate unit should be operated.

#### $I_{GIN Min}$ :

The minimum supply current that is required to power up the gate unit properly.

#### $P_{GIN Max}$ :

The maximum gate unit supply power that is allowed for operation.

#### $I_{GIN Max}$ :

The gate unit's internal power supply has a current limitation that limits the supply current to this value.

#### 3.5.2 Optical control input/output

*Maximum rated values <sup>1)</sup>*

Parameter	Symbol	Conditions	min	typ	max	Unit
Min. on-time	$t_{on}$		40			$\mu s$
Min. off-time	$t_{off}$		40			$\mu s$

*Characteristic values*

Parameter	Symbol	Conditions	min	typ	max	Unit
Optical input power	$P_{on CS}$	CS: Command signal SF: Status feedback	-15		-1	dBm
Optical noise power	$P_{off CS}$				-45	dBm
Optical output power	$P_{on SF}$	Valid for 1mm plastic optical fiber (POF)	-19		-1	dBm
Optical noise power	$P_{off SF}$				-50	dBm
Pulse width threshold	$t_{GLITCH}$	Max. pulse width without response			400	ns
External retrigger pulse width	$t_{retrig}$		600		1100	ns

2) Do not disconnect or connect fiber optic cables while light is on.

#### $t_{on}$ :

The IGCT requires time to fully turn-on. Therefore, the turn-off behavior is different when the IGCT is turned on for too short a time. The specified characteristics and the turn-off capability cannot be guaranteed when this minimum time is not maintained.

**t<sub>off</sub>:**

Similar to the min. on-time, also the minimum off-time has to be maintained.

**P<sub>on CS</sub>:**

The range of the optical power that is required to achieve a correct on-command.

**P<sub>off CS</sub>:**

The max. optical noise power is the maximum level of the optical input power that keeps the IGCT in off-state.

**P<sub>on SF</sub>:**

The optical power level of the feedback signal when HIGH.

**P<sub>off SF</sub>:**

The max. optical power level of the feedback signal when LOW.

**t<sub>glitch</sub>:**

The gate unit has an input filter to avoid a short disturbance on the command signal being interpreted as a switching command.

**t<sub>retrig</sub>:**

Pulse width range of the command signal required to release a retrigger pulse.

### 3.5.3 Connectors

Parameter	Symbol	Description
Gate Unit power connector	X1	AMP: MTA-156, Part Number 641210-5 <sup>3)</sup>
LWL receiver for command signal	CS	Agilent, Type HFBR-2528 <sup>4)</sup>
LWL transmitter for status feedback	SF	Agilent, Type HFBR-1528 <sup>4)</sup>

2) Do not disconnect or connect fiber optic cables while light is on.

3) AMP, [www.amp.com](http://www.amp.com)

4) Avago Technologies, [www.avagotech.com](http://www.avagotech.com)

This paragraph defines the optical and supply power connector. Further information can be found on the supplier web sites.

### 3.5.4 Visual feedback

Parameter	Symbol	Description	Color
Gate OFF	LED1	"Light" when GCT is off	(green)
Gate ON	LED2	"Light" when gate-current is flowing	(yellow)
Fault	LED3	"Light" when not ready / Failure	(red)
Power supply voltage OK	LED4	"Light" when power supply is within specified range	(green)

The meaning of the visual feedback LEDs is described in the Application Note 5SYA2031 "Applying IGCT Gate Units"

### 3.6 Thermal

#### Maximum rated values <sup>1)</sup>

Parameter	Symbol	Conditions	min	typ	max	Unit
Junction operating temperature	$T_{vj}$		-40		125	°C
Storage temperature range	$T_{stg}$		-40		60	°C
Ambient operational temperature	$T_a$		-40		50	°C

#### Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
Thermal resistance junction-to-case of GCT	$R_{th(j-c)}$	Double side cooled			8.5	K/kW
Thermal resistance case-to-heatsink of GCT	$R_{th(c-h)}$	Double side cooled			3	K/kW

#### $T_{vj}$

The operating junction temperature. The lower limit of  $T_{vj}$  is determined mainly by the turn-on and turn-off characteristics of the IGCT. Extremely low temperatures may raise latching current to the point at which the device no longer turns on and also the turn-off capability reduces with decreasing temperature according to Fig. 11. The upper limit, on the other hand, is determined by the blocking capability of the main pn junction. Leakage current rises exponentially with temperature and thermal instabilities may start to appear at high voltage.

#### $T_{stg}$

The storage temperature range for short-term events. To maximize the storage life time we recommend storage at a stable temperature of  $20\text{ °C} \pm 10\text{ °C}$  and a relative humidity below 55 %.

#### $T_a$

The operating ambient temperature.  $T_a$  defines the temperatures at which the gate unit works reliably.  $T_a$  is the air temperature around the gate-unit components (especially the electrolytic capacitors) during operation. Temperatures below  $T_{a\ min}$  reduce  $I_{TGQM}$  because of an increase in gate unit impedance.  $T_{a\ max}$  is the ambient temperature at which ageing of the gate unit becomes important. For a lifetime of 20 years, the case temperature of the electrolytic capacitors should be limited to  $60\text{ °C}$ . Fig. 5 shows the effect of light forced air-cooling on the allowable turn-off current as a function of switching frequency. In cases where  $T_a$ ,  $T_{case\ GCT}$  or cooling conditions differ significantly from the datasheet, we recommend measuring the case temperature of the electrolytic capacitors.

The operating range is also limited by the power supply capability of the gate unit. This is shown by the curve  $P_{GIN\ Max}$ .

#### Max. Turn-off current for Lifetime operation

- calculated lifetime of on-board capacitors 20 years
- with slightly forced air cooling (air velocity > 0.5 m/s)
- strong air cooling allows for increased ambient temperature

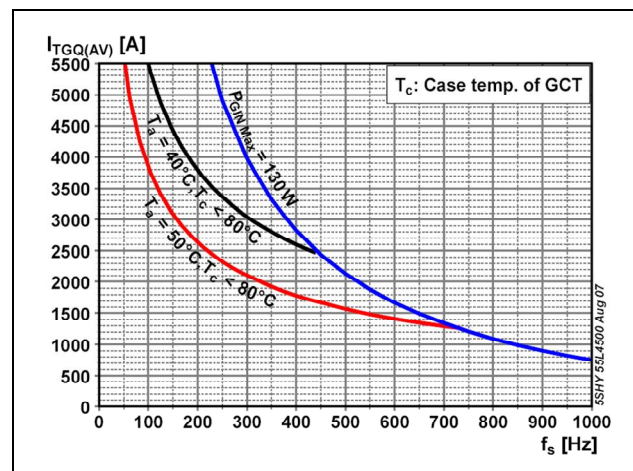


Fig. 5 Max. turn-off current vs. frequency for lifetime operation (example 5SHY 55L4500)

### $R_{th(j-c)}$

Thermal resistance from junction (silicon wafer) to case with double-side cooling. As a free-floating IGCT has several dry interfaces inside the ceramic housing, it is evident that  $R_{th(j-c)}$  depends on  $F_m$ . Datasheet figures are, therefore, based on the nominal mounting force as specified in the mechanical-data sub-section. Reverse-conducting IGCTs have two separately specified values, one for the GCT-part and one for the diode-part. The data are specified under the condition that the GCT and diode parts are at the same temperature. Homogeneous mounting pressure is vital for reliable IGCT operation; this is particularly important for  $R_{th(j-c)}$ .

### $R_{th(c-h)}$

Thermal resistance from case to heat sink (surface of IGCT housing to surface of heat sink) is defined at nominal mounting force  $F_m$ . Since  $R_{th(c-h)}$  is a dry interface between two surfaces, it depends a great deal on the quality of the surfaces and the homogeneity of the mounting pressure. The specified  $R_{th(c-h)}$  is achieved when the heat sink surface is of a similar quality to that of the IGCT surface i.e. when its flatness is of the order of 15  $\mu\text{m}$ , its roughness is of the order of 1  $\mu\text{m}$  and the per-unit-area mounting pressure is uniform across the surface to within  $\pm 15\%$ . The latter requirement calls for careful design of the clamping system. Details concerning a proper clamping system are described in Application Note 5SYA2036 "Recommendations regarding mechanical clamping of Press Pack High Power Semiconductors".

### $Z_{th(j-c)}(t)$

Transient thermal impedance,  $Z_{th(j-c)}(t)$ , emulates the rise of junction temperature versus time, when a constant power is dissipated in the junction. It is defined as the temperature difference junction-to-case, divided by the power:

$$Z_{th(j-c)}(t) = \frac{\Delta T_{(j-c)}(t)}{P}$$

Analytical function for transient thermal impedance:

$$Z_{th(j-c)}(t) = \sum_{i=1}^n R_i(1 - e^{-t/\tau_i})$$

i	1	2	3	4
$R_i(\text{K/kW})$	5.562	1.527	0.868	0.545
$\tau_i(\text{s})$	0.5119	0.0896	0.0091	0.0024

Fig. 6a

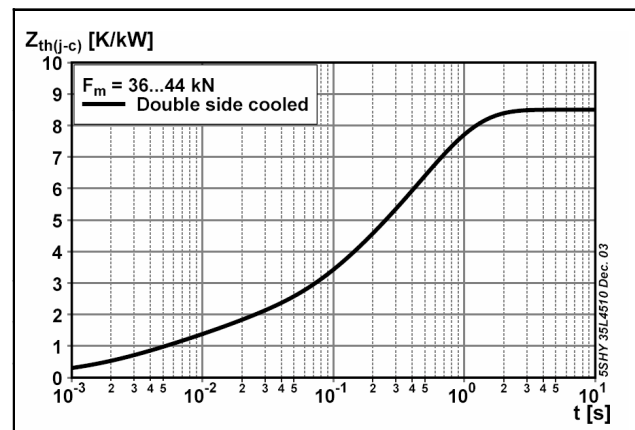


Fig. 6b Transient thermal impedance (junction-to-case) vs. time (max. values)

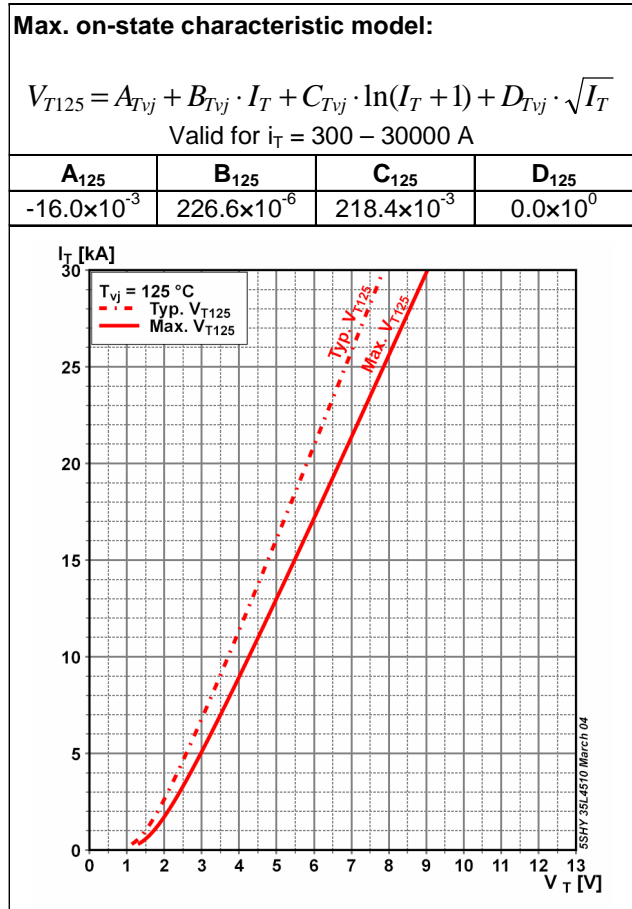
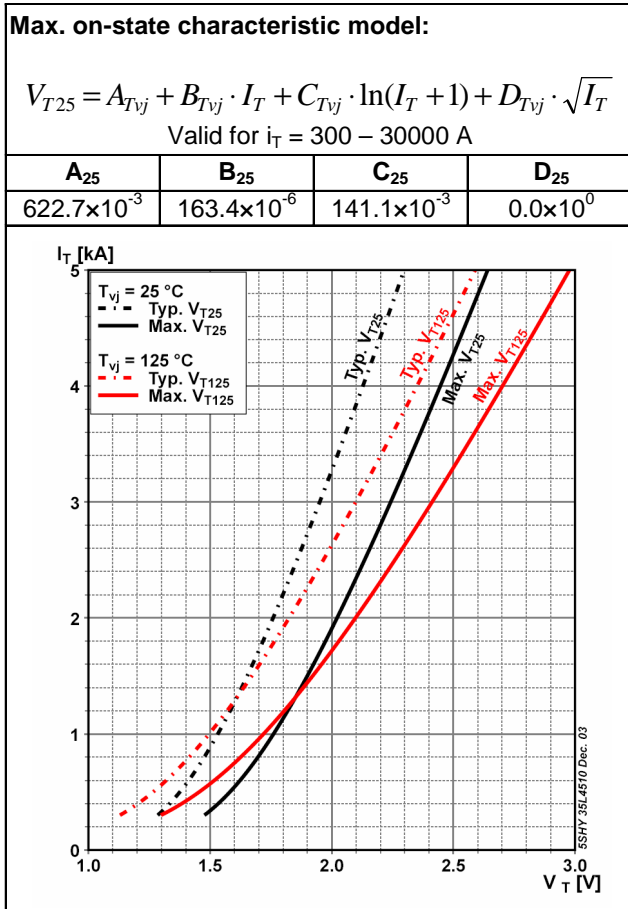
This function can be specified as a curve as shown in Fig. 6b, or by an analytical approximation with the superposition of four exponential terms (Fig. 6a), as shown above. The analytical expression is particularly useful for computer calculations.



### 3.7 Diagrams

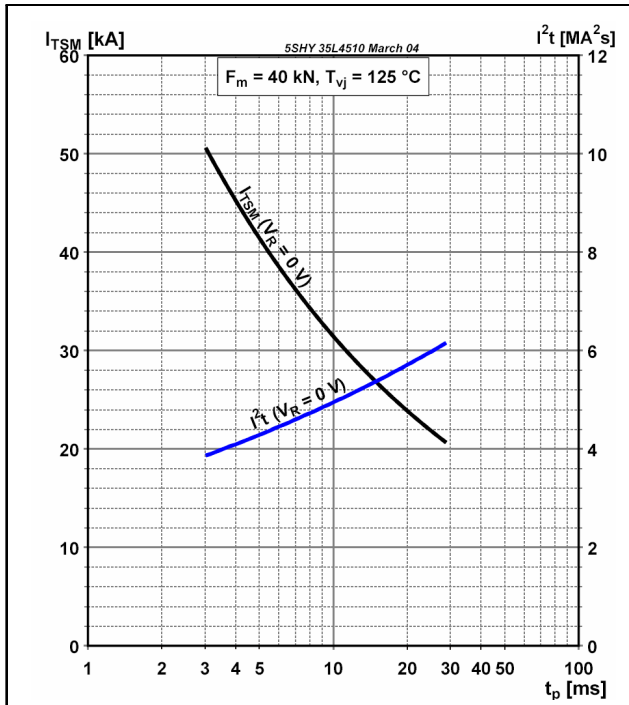
#### 3.7.1 GCT on-state current vs. on-state voltage

Figs. 7a and 7b show on-state voltage as a function of on-state current for  $T_{vj} = 25\text{ °C}$  and  $125\text{ °C}$ . Both, typical and maximal values are given. These curves can be used to calculate on-state losses. The max. curves are characterized by the equations shown above the diagrams.

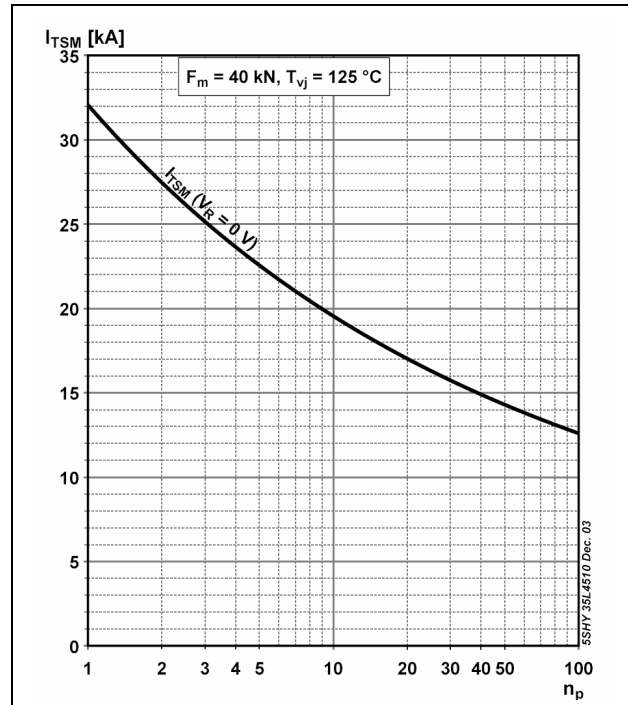


### 3.7.2 GCT surge current vs pulse width and number of pulses

Figs. 8 and 9 specify the surge current ratings and corresponding fusing integrals. The relationship between these two ratings was examined in the on-state parameter section. The constraints linked to  $I_{TSM}$  and  $\int i^2 t$  mentioned there also apply to Fig. 9.



**Fig. 8** Surge on-state current vs. pulse length, half-sine wave.



**Fig. 9** Surge on-state current vs. number of pulses, half-sine wave, 10 ms, 50Hz

The maximum  $I_{TSM}$  shown in Fig. 8 should not be exceeded even for shorter pulses. For surge current requirements that do not resemble a sine half wave or cannot be covered by a sine half wave shown in Fig. 8, please contact your nearest representative or the address shown at the end of this application note for evaluation.

### 3.7.3 GCT turn-off characteristics

Fig. 10 shows GCT turn-off losses vs turn-off current. The curves are determined in the test circuit of the datasheet. In VSI topologies with clamp circuits, the losses vary approximately linearly with DC-link voltage  $V_D$  and turn-off current  $I_{TGO}$ .

Fig. 11 specifies the turn-off safe operating area in a VSI clamp-circuit. Two parameters mainly determine the turn-off capability:

- the impedance of the turn-off gate channel increases with decreasing ambient temperature of the gate unit; this limits max. turn-off current  $I_{TGQM}$  independently of turn-off voltage
- The max. turn-off power capability of the GCT limits turn-off current as a function of turn-off voltage.

For these reasons, the safe operating area (Fig. 11) depends on device type and varies according to the dominant constraint (gate-unit type, DC voltage, temperature etc).

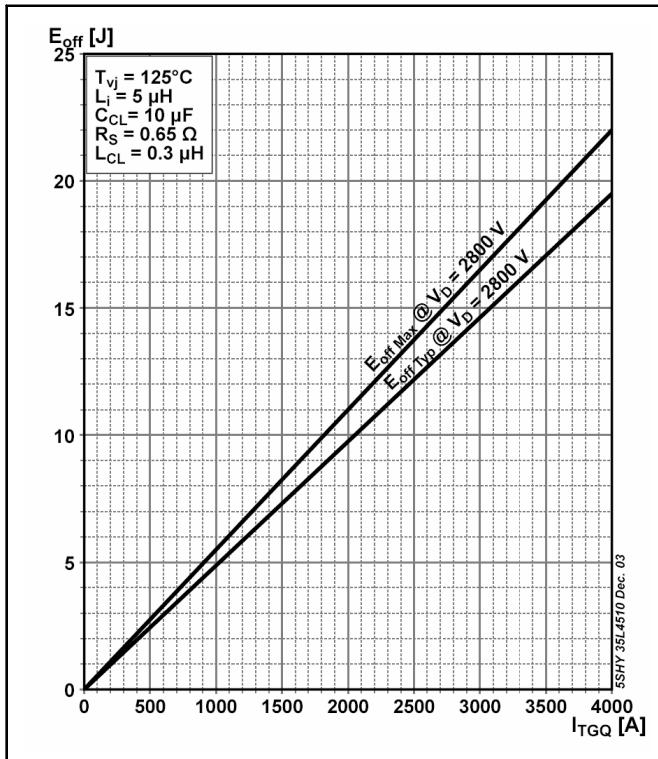


Fig. 10 GCT turn-off energy per pulse vs. turn-off current

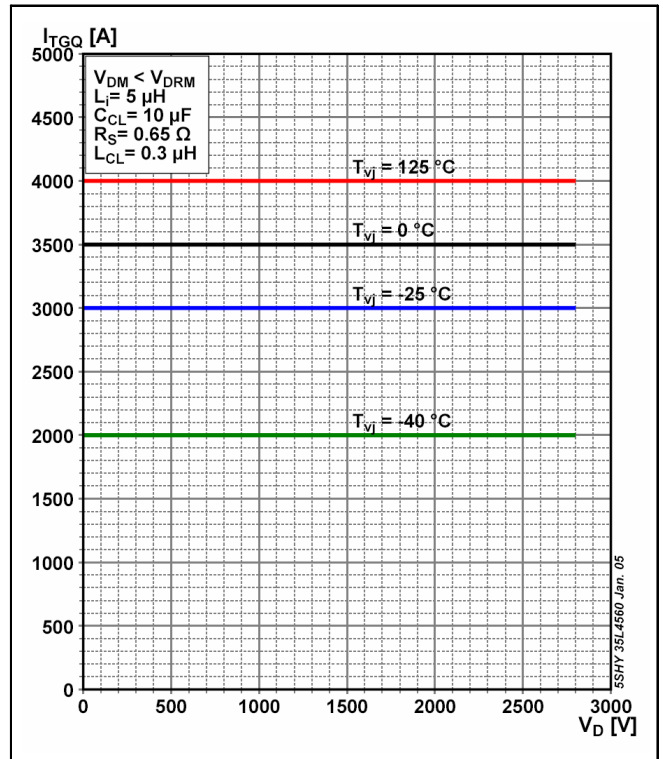


Fig. 11 Safe Operating Area

### 3.7.4 Gate unit related diagrams

#### Power Consumption

The total power consumption of the IGCT Gate Unit is strongly load-dependent as can be seen in Fig. 12. Turn-off current  $I_{TGQ}$ , switching frequency  $f_s$ , junction temperature  $T_{vj}$  and device technology (gate charge  $Q_{gq}$ ) have a major influence on power consumption. The power supplied to the gate-unit falls into two parts:

- a small thermal dissipation in the gate circuit and in the gate-cathode junction; this is dependent on switching frequency and ambient temperature since the “back-porch” current is increased at low temperature to ensure latching.
- the bulk of the supplied power is transferred to the load once the cathode is commutated off.

Gate Unit limitations must be checked before the operating range in a specific application is determined. For the thermal limitations see Fig. 5.

## Burst capability

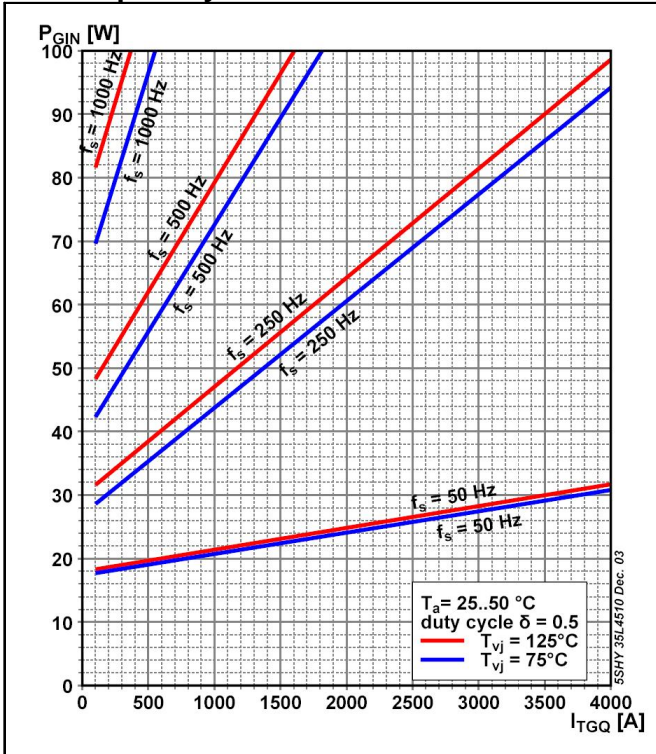


Fig. 12 Max. Gate Unit input power in chopper mode

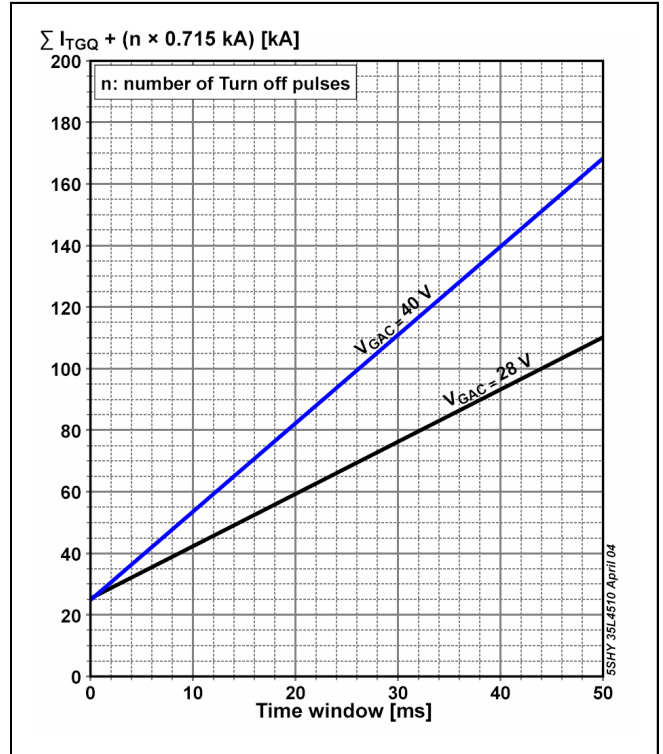


Fig. 13 Burst capability of Gate Unit

The gate unit of the IGCT has a large capacitor bank which stores energy for turn-on pulse, back-porch current and turn-off pulse. Since the turn-off pulse needs a large charge and the gate unit power supply has an internal current limitation ( $I_{GIN\text{ Max}}$ ), triggering with very high frequencies is limited according to Fig. 13. The diagram shows only the limitation of the gate unit. Independent of this the minimum on- and off-times ( $t_{on}$ ,  $t_{off}$ ) have to be maintained. Also the junction temperature of the GCT has to be taken into account. Thus the burst capability may be limited by the switching losses in the IGCT rather than the gate unit.

## 3.8 Diode-specific data of reverse conducting IGCTs (from datasheet 5SHX 26L4510)

### 3.8.1 Diode On-state

On-state data and diagrams are described in the same way as the on-state data of the GCT-part. Please refer to section 3.4.1 and diagrams Fig. 6 ... 9.

### 3.8.2 Diode turn-on

#### Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
Peak forward recovery voltage	$V_{FRM}$	$di_F/dt = 650\text{ A}/\mu\text{s}$ , $T_{vj} = 125^\circ\text{C}$			80	V
		$di_F/dt = 3000\text{ A}/\mu\text{s}$ , $T_{vj} = 125^\circ\text{C}$			250	V

#### $V_{FRM}$

Peak forward recovery voltage: Please refer section 4.1.6.

### 3.8.3 Diode turn-off

#### Maximum rated values

Parameter	Symbol	Conditions	min	typ	max	Unit
Max. decay rate of on-state current	$di/dt_{crit}$	$I_{FM} = 2200 \text{ A}$ , $T_{vj} = 125 \text{ °C}$ $V_{DClink} = 2800 \text{ V}$			650	A/ $\mu$ s
Max. decay rate of on-state current	$di/dt_{crit}$	$I_{FM} = 3200 \text{ A}$ , $T_{vj} = 125 \text{ °C}$ $V_{DClink} = 2800 \text{ V}$			650	A/ $\mu$ s

#### Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
Reverse recovery current	$I_{RM}$	$I_{FM} = 2200 \text{ A}$ , $V_{DC-Link} = 2800 \text{ V}$			900	A
Reverse recovery charge	$Q_{rr}$	$-di_F/dt = 650 \text{ A}/\mu\text{s}$ , $L_{CL} = 300 \text{ nH}$ $C_{CL} = 10 \mu\text{F}$ , $R_S = 0.8 \Omega$ ,			2800	$\mu\text{C}$
Turn-off energy	$E_{rr}$	$T_{vj} = 125\text{°C}$ , $D_{CL} = 5\text{SDF } 10\text{H}4520$		2.7	4	J

#### $di/dt_{crit}$

Max. decay rate of on-state current defines the minimum value of  $(L_i + L_{CL})$  according to:

$$(L_i + L_{CL}) = \frac{V_{DClink}}{di/dt}$$

where  $V_{DClink}$  is the voltage drop across  $(L_i + L_{CL})$  during turn-off of the diode (see Fig. 4 for test circuit). It is important to respect the “diode safe operating area” diagram of the datasheet and to ensure that  $L_{CL}$  be as low as possible. Typical applications work in a range of  $L_{CL} = 150 \dots 250 \text{ nH}$ . Large stray clamp inductance increases the electrical stress on the diode during turn-off and also reduces the turn-off capability of the switch.

#### $I_{RM}$ , $Q_{rr}$ , $E_{rr}$

Reverse recovery current, reverse recovery charge and diode turn-off energy are specified under application-specific conditions. Additional data is available in the datasheet diagrams.

### 3.8.4 Thermal data

In addition to the thermal data of the IGCT, the datasheets of reverse conducting IGCTs have thermal data for the diode part. The data is documented in the same way as in section 3.6.  $R_{th}$  and  $Z_{th}$  are specified without heat flow between the GCT-part and diode-part.

## 4 IGCT application-specific topics

### 4.1 IGCTs in Voltage Source Inverters (VSI)

Reverse conducting IGCTs (RC-IGCT), asymmetric IGCTs (AS-IGCT) and their corresponding diodes are qualified and tested in test circuits built according to the circuit diagram below. It is an equivalent circuit for the switching events occurring in a VSI circuit, be it of 2-level or 3-level topology.

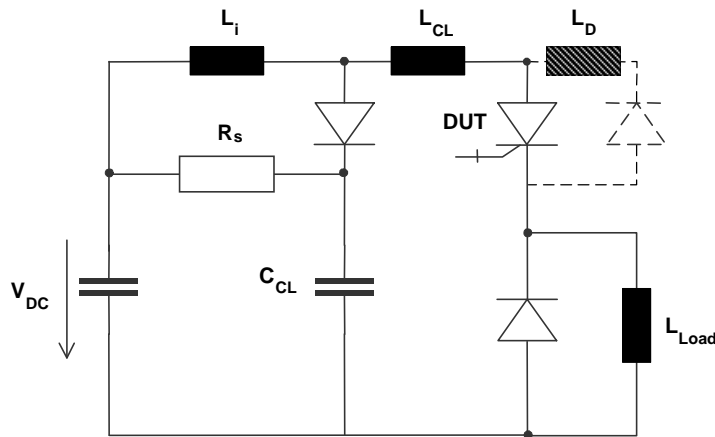


Fig. 14 Test circuit as shown in the datasheet

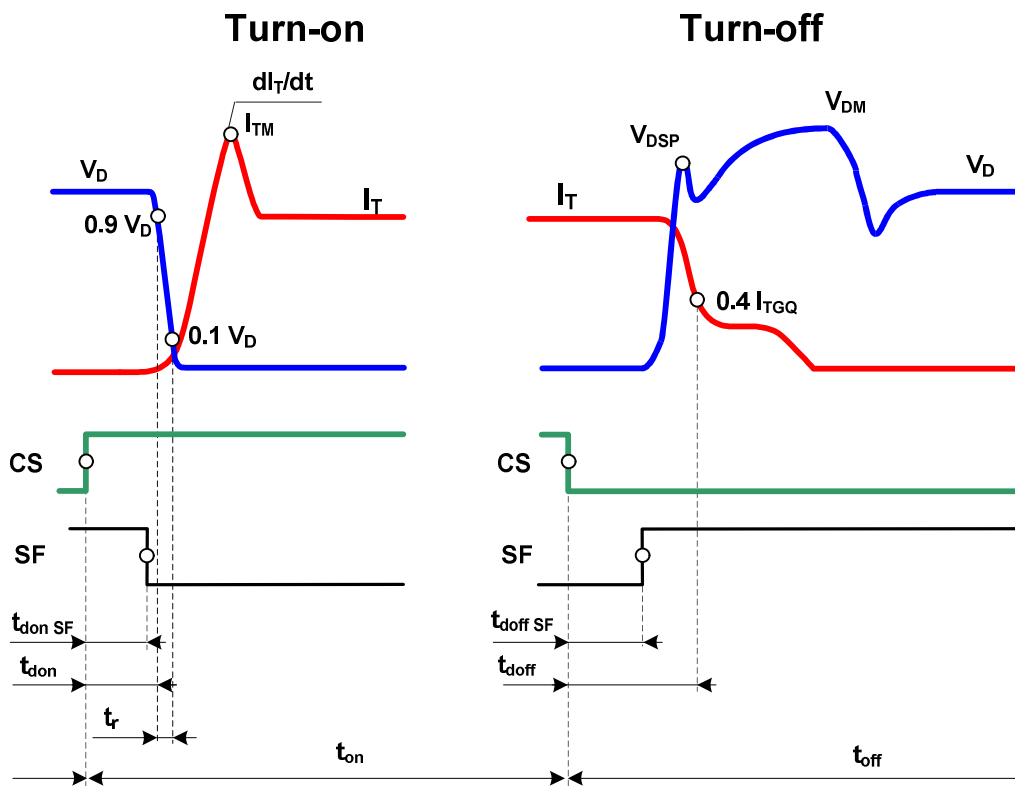


Fig. 15 General current and voltage waveforms with IGCT-specific symbols.

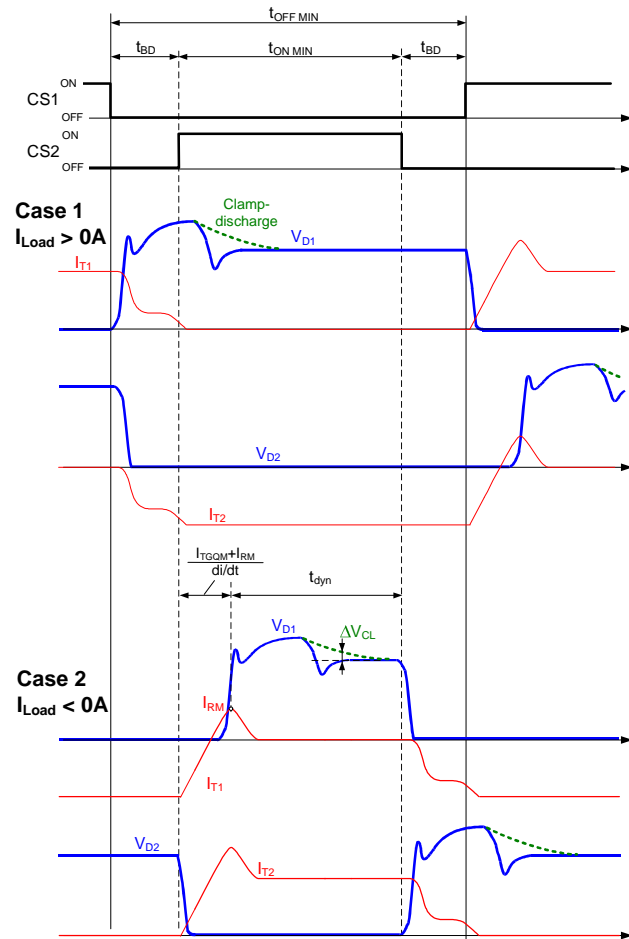
### 4.1.1 Design criteria

For the design of an inverter, several considerations have to be taken into account. The main concerns are:

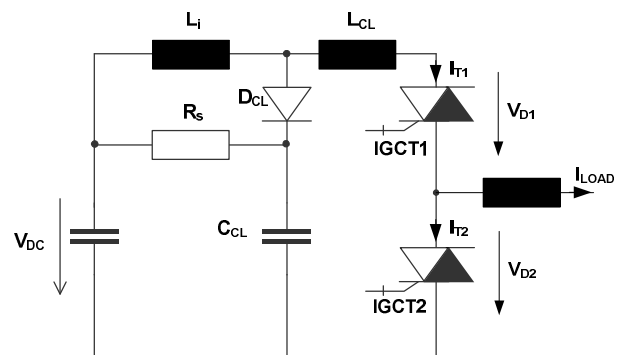
#### Critical di/dt of the freewheeling diode

In order to meet the turn-off di/dt requirements of the freewheeling diode, the turn-on di/dt of the IGCT has to be limited.

#### Minimum dead times $t_{ON MIN}$ and $t_{OFF MIN}$



Definitions



Inverter circuit

For the control scheme, the dead time between switching transients should be as small as possible. On the other hand, IGCTs should not be turned on or turned off whilst the clamp circuit is still conducting. Due to the blocking delay time  $t_{BD}$ , which is the necessary delay time between turn-off and turn-on of a switching pair within a VSI phase leg,  $t_{ON MIN}$  and  $t_{OFF MIN}$  are not equal:

$$t_{OFF MIN} = t_{ON MIN} + 2 \times t_{BD} \quad \text{with:} \quad t_{ON MIN} \geq \frac{I_{TGQM} + I_{RM}}{di/dt} + t_{dyn}$$

In IGCT circuits, a blocking-delay-time  $t_{BD}$  of about 10  $\mu$ s is typical.

These restrictions are due to the conditions of the clamp circuit. However there are also restrictions because of the IGCT itself. This is because the GCT needs time to reach its steady state. Therefore, it is mandatory to maintain the minimum on and off-times  $t_{ON}$  and  $t_{OFF}$  in the datasheet. If these minimum times are violated, the specified SOA of the device may not be met.

## Maximum device voltage $V_{DM}$

The voltage overshoot  $V_{DM}$  is not allowed to exceed the rated repetitive blocking voltage of either the IGCT or the diode:

$$V_{DM} < V_{DRM}, V_{RRM}$$

The voltage overshoot is also important because of cosmic ray. In some designs the cosmic ray failure rate due to this over-voltage can become dominant compared to the dc-link voltage. The reason for this is that the cosmic failure rate increases disproportionately to the applied voltage. For more information to this topic, please consult Application Note 5SYA2046 "Failure rate of IGCTs due to cosmic ray"

## Clamp voltage overshoot $\Delta V_{CL}$

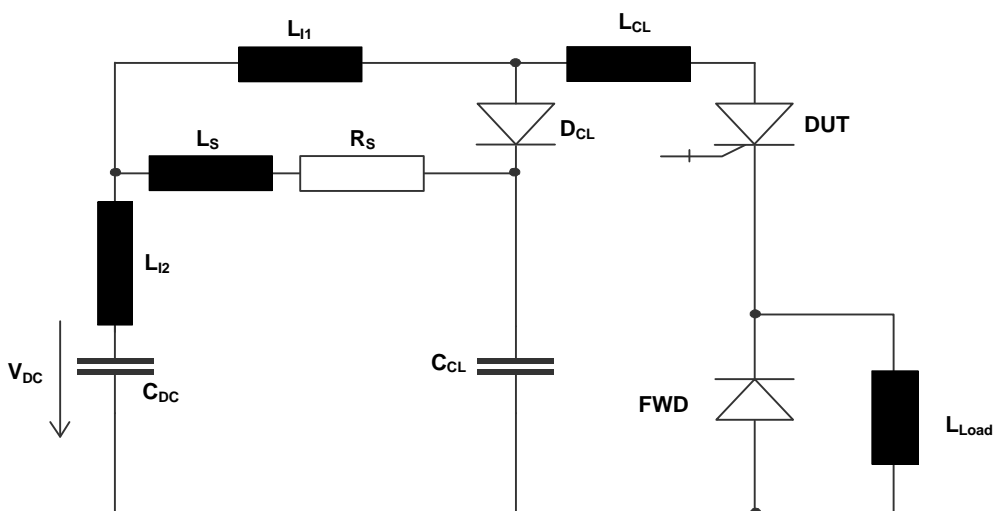
To stay within the safe operating area of IGCTs and diodes, the clamping capacitor voltage transient  $\Delta V_{CL}$  must be close to zero again before the next switching transition takes place. If this condition is not fulfilled, the switching voltage  $V_D$  will be higher than  $V_{DC}$  and may exceed max.  $V_D$  of the datasheet (see Fig. 11).

## Clamp diode current $I_{DCL}$

Not only the clamping capacitor over-voltage, but also the clamping diode current,  $I_{DCL}$ , must be close to zero before the IGCT turns on again. If not, the clamping diode, at IGCT *turn-on*, will itself *turn-off* at a high  $di/dt$  value (limited by the stray inductance  $L_{CL}$  only) in excess of the  $di/dt$  capability of the clamping diode.

### 4.1.2 Determining the design parameters

The values for  $L_i$ ,  $C_{CL}$  and  $R_S$  given in the conditions column of the data sheet are established values and can be used as a starting point for the design. However, these values do not consider the parasitic parameters that are present in all real applications. Figure 16 depicts the test circuit as in the datasheet but extended to show the most important parasitic parameters.



**Fig. 16** Circuit as shown in the data sheet, extended with parasitic inductances

$C_{DC}$  DC-link capacitor

$L_I$   $di/dt$  limiting inductor; the  $di/dt$  limiting inductor  $L_I$  is normally divided in two parts:

$L_{I1}$ : discrete inductor to achieve the required  $di/dt$

$L_{I2}$ : stray inductance of the DC-link capacitor; this part is not damped by  $R_S$  and therefore strongly contributes to the voltage overshoot  $V_{DM}$  and should be minimized

$R_S$  damping resistor, used to dissipate the clamp circuit energy



---

$L_S$	stray inductance of damping resistor, should be minimized
$C_{CL}$	clamp capacitor, used to clamp the IGCT over-voltage; it also initially absorbs some of the energy stored in the di/dt limiting inductor
$L_{CL}$	stray inductance of the clamp - should be minimized
$D_{CL}$	clamp diode, should have a small forward recovery $V_{FR}$ .

#### 4.1.3 Determining the value of the di/dt limiting inductor

In a VSI, as in most power electronic circuits, a diode *turn-off* is caused by an IGCT *turn-on* and the diode's turn-off di/dt capability is, in most cases, lower than the turn-on di/dt capability of the IGCT. This is especially true in common applications without a turn-off snubber. Hence the di/dt choke  $L_I$  must be large enough to allow operation within the di/dt range of the diode even at the highest DC-link voltages. Typical values for ABBdiodes are between 200 and 1000 A/μs depending on diode wafer size and switching voltage.

Diode switching losses and surge currents are also dependent on the choke size and these considerations may require a larger inductance value. This, however, will come at the cost of a slower clamp circuit transient ( $t_{dyn}$ ) and longer switching dead times.

The minimum size of the di/dt inductor can be calculated from the maximum dc-voltage and the maximum allowed di/dt:

$$L_I = L_{I1} + L_{I2} > \frac{V_{DC\max}}{di/dt_{\max}} (-L_{CL})$$

The stray inductance of the clamp ( $L_{CL}$ ) is normally disregarded.

#### 4.1.4 Determining the value of the clamp capacitor $C_{CL}$ and the damping resistor $R_S$

Because of the parasitic parameters, it is difficult to determine an analytic method for calculating the optimal values for  $C_{CL}$  and  $R_S$ . We, therefore, recommend the following procedure to optimize  $C_{CL}$  and  $R_S$ :

- implement the above circuit (Fig. 16) in a circuit simulation tool, e.g. SPICE
- use an ideal switch that changes its impedance from on-state to off-state within about 2 μs
- choose the values of the datasheet as starting point for  $C_{CL}$  and  $R_S$
- insert estimated values for  $L_{I2}$  and  $L_S$
- run IGCT turn-off switching simulations with worst case conditions ( $V_{DC}$ ,  $I_{TGQM}$ )
- iteratively adjust the values of  $C_{CL}$  and  $R_S$  to obtain the desired results:
  - $V_{DM} < V_{DRM}$  (increase  $C_{CL}$  or decrease  $R_S$ )
  - damping of loop  $R_S - C_{CL} - C_{DC} - L_{I2} - L_S$  so that the clamp diode does not conduct again after its turn-off (increase  $R_S$ )
  - clamp diode blocks before an associated IGCT switches on again
  - clamp capacitor is discharged to its static value before an associated IGCT switches on or off again (decrease  $C_{CL}$  or  $R_S$ )
- the stray inductances may differ from the anticipated values and other parameters may influence the design; the above simulations together with accurate verification measurements will ideally be part of the design iterations.

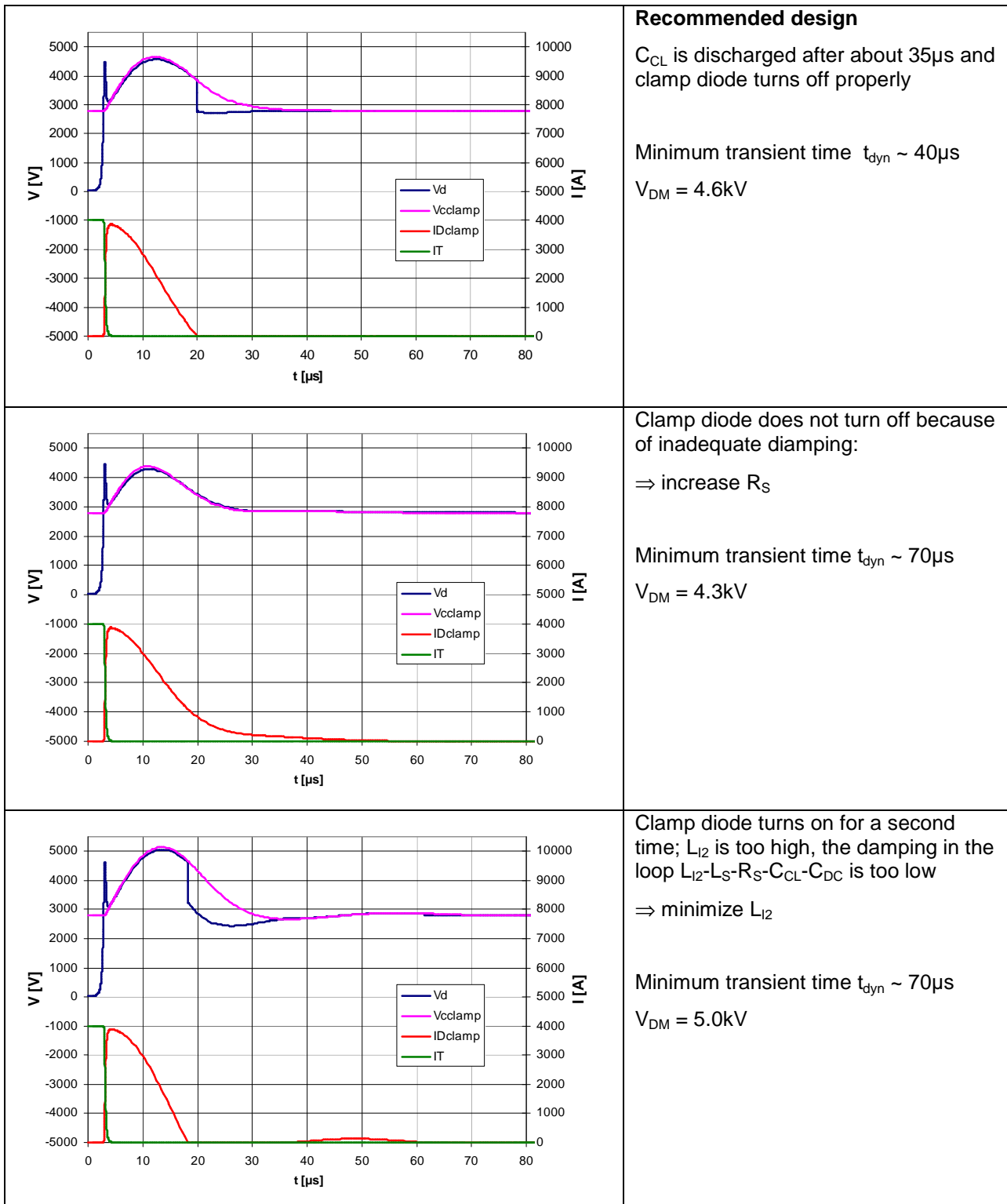
For this simulation, the turn-off behavior of the IGCT is not relevant. The IGCT can therefore be modeled as a simple ideal switch with a defined transition time. For example in SPICE, a voltage controlled switch can be used as follows:

.MODEL IGCT VSWITCH Roff=1e4 Ron=10.0e-3 Voff=0.0V Von=1.0V

This switch can then be controlled with a voltage ramp that goes from 1V to 0V within 5 $\mu$ s.

The first voltage spike in the simulation ( $V_{DSP}$ ) has to be ignored, since it is highly IGCT dependent (and not simulated by this simple model). It is also not relevant for the design of  $C_{CL}$  and  $R_S$ .

The following figures show examples of simulated IGCT turn-off waveforms. All designs work with a 6kV device, however the allowable minimum turn-off times differ. To avoid stress on the clamp diode, the IGCT should not be switched while the clamp diode is still conducting.



**Fig. 17** Determine size of clamp capacitor  $C_{CL}$  and damping resistor  $R_S$  for freewheeling diode

In the above paragraph, the design of the clamp circuit parameters was shown for IGCT turn-off. Naturally the freewheeling diode (FWD) also needs a clamp. Whereas for the IGCT, the turn-off current determines the clamp overshoot voltage, for the freewheel diode, it is the reverse recovery current  $I_{RM}$  that causes the overshoot. Since in most applications, the maximum IGCT turn-off current is larger than the maximum diode reverse recovery current, the clamp design of the IGCT *normally* also suits the diode turn-off.

The power losses in the damping resistor  $R_S$  can be calculated with confidence from the turn-off current and the value of the di/dt limiting inductor.

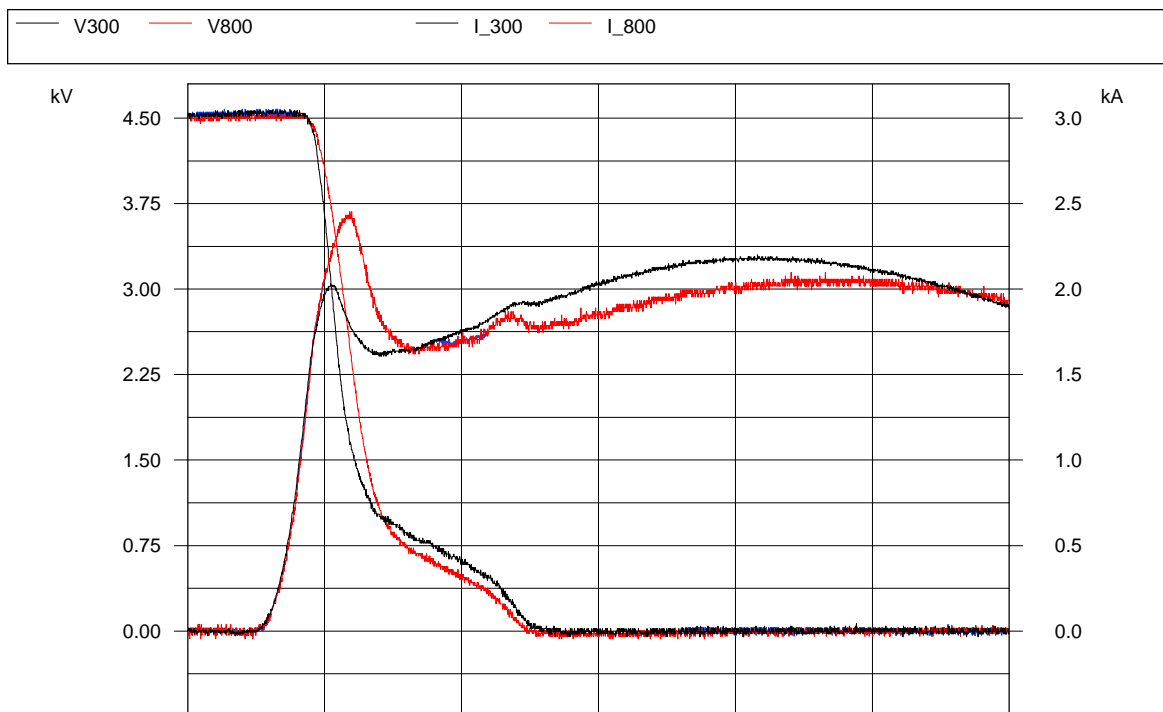
$$E_{Rs} = \frac{I_{TGQ}^2 \cdot L_I}{2} \text{ for IGCT turn-off respectively } E_{Rs} = \frac{I_{RM}^2 \cdot L_I}{2} \text{ for diode turn-off.}$$

This calculation only takes into account the switching events in the specific phase-leg. Since in most applications several phase-legs are connected to the same dc-link capacitor, there is an interaction between the phase-legs that may lead to additional losses in the clamp resistor.

#### 4.1.5 Stray inductance $L_{CL}$

The stray inductance  $L_{CL}$  is the overall inductance in the loop comprising  $C_{CL}$ ,  $D_{CL}$ , DUT and FWD. It is determined by the geometry of bus bars, cables, heat sinks and the devices in the commutation circuit. This inductance has a major influence on the first voltage overshoot peak  $V_{DSP}$  (Fig. 15) and the switching losses of both IGCT and diode. Switching losses increase and the safe operating area decreases when the loop inductance increases. The test circuit stray inductance  $L_{CL}$  is given for each IGCT or diode product in the datasheet.

Fig.18 shows the influence of the stray inductance  $L_{CL}$  on the switching waveforms of IGCT type 5SHY 35L4510 by comparing waveforms with 300 and 800 nH stray inductances.



**Fig. 18** Influence of stray inductance on turn-off behavior ( $L_{CL} = 300\text{nH}$  and  $800\text{nH}$ )

As can be seen in Fig. 18, the voltage overshoot increases by about 700V. The turn-off energy in this example is 10.6 Ws (300 nH) and 12.0 Ws (800 nH)

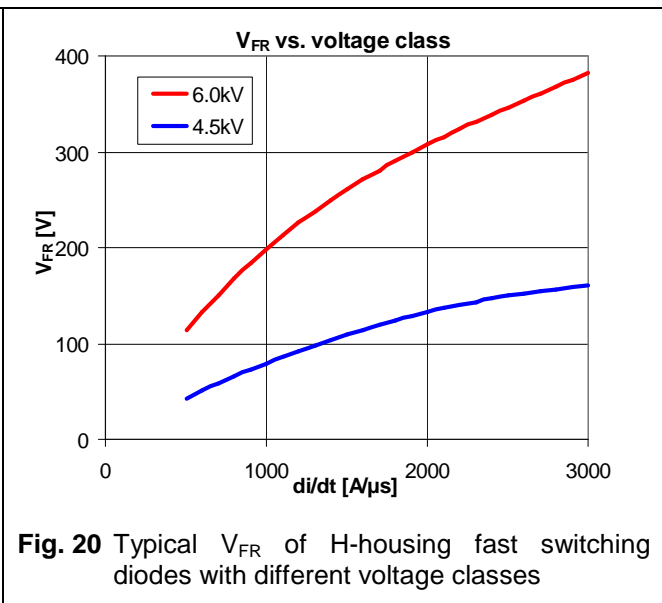
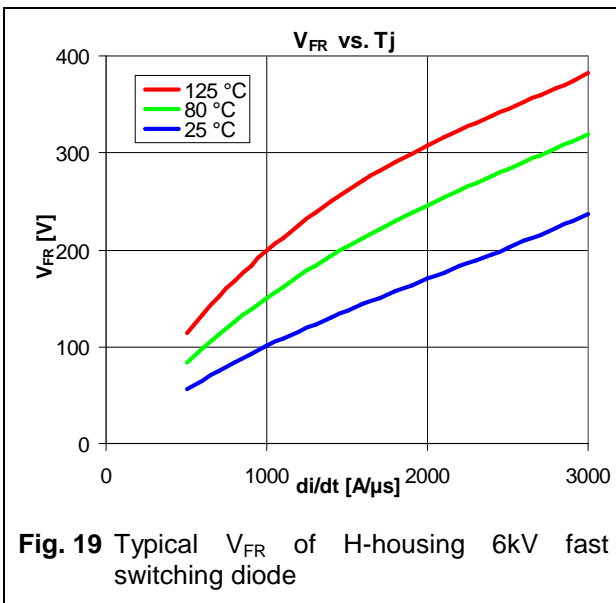
High values of  $L_{CL}$  increase the instantaneous power of the IGCT. This reduces the turn-off capability. Also the device voltage tends to snap off at the end of the tail current leading to an increased voltage overshoot and additional electromagnetic emission.

- ⇒ The stray inductance  $L_{CL}$  should be minimized
- ⇒ To meet the specified SOA and switching losses,  $L_{CL}$  has to be equal to or less than the value specified in the datasheet.

#### 4.1.6 Influence of the clamp diode type

For selection of the clamp diode, the forward recovery ( $V_{FR}$ ) has to be considered. When the current from the IGCT is commutated to the clamp diode, the diode reacts with an initially higher forward voltage drop. This is because the number of free charge carriers is initially much lower than in steady state and the diode's conductivity is still low.

The  $V_{FR}$  is strongly dependent on the voltage class, diameter and temperature of the diode as well as the forward  $di/dt$ . Figs. 19 and 20 show typical curves for 4.5 kV and 6.0 kV ABB diodes with "H-housings" (68 mm wafers). The active silicon area of the diode influences  $V_{FR}$  by determining  $di/dt$  per unit area.



The forward recovery behavior of the clamp diode has the same effect as stray inductance in the clamp circuit in that it increases the peak voltage  $V_{DSP}$ . The clamp design, shown in the conditions column of the datasheet for  $I_{TGQM}$  and  $E_{off}$ , is valid for an ABB diode of the same voltage class as the IGCT and a housing type that is one size smaller than that of the IGCT.

In applications where SOA and  $E_{off}$  are critical, it is recommended to use a clamp diode of the same voltage class as the IGCT and to minimize the clamp inductance.

#### 4.1.7 Overview of parameter influences

The following table shows which parameter influences which value in which direction, since the influence of the parameters is not obvious at first glance.

		increase of ...					
		$C_{cl}$	$L_{l1}$	$L_{l2}$	$L_{CL}$	$L_S$	$R_S$
influence on ...	GCT turn-off losses	∅	ö	ö	öö	ö	ö
	GCT turn-on losses	ö	∅	∅	ö	ö	ö
	FWD turn-off losses	∅	∅	∅∅	öö	ö	∅
	clamp resistor losses	ö	öö	öö	ö	ö	ö
	$V_{DM}$	∅∅	öö	öö	ö	ö	öö
	$V_{DSP}$	ö	ö	ö	öö	ö	ö
	$t_{dyn}$	öö	öö	öö	ö	öö	1)

- öö increase
- ö slight increase
- ö no significant influence
- ∅ slight decrease
- ∅∅ decrease
- 1) optimum has to be found

#### 4.1.8 Use of additional snubber

It may be convenient to use a snubber across the IGCT in addition to the clamp circuit. Under certain circumstances a snubber can increase the turn-off capability of the IGCT because it reduces the peak instantaneous power. But there are other limiting parameters, therefore, please contact your nearest representative or the address shown at the end of this application note if you intend to extend the SOA by using a snubber.

A snubber increases the overall losses. However, it can reduce the turn-off losses of the IGCT and therefore allow for a higher maximum power of the converter while still using the same semiconductors.

A snubber generates an inrush current in the GCT during turn-on. We recommend selecting the snubber component values so that this inrush current does not exceed about 20% of the rated  $I_{TGM}$  of the device.

The following diagrams show loss comparisons of snubberless, RCD- and RC-snubber operation. Fig. 23 depicts the turn-off losses of the GCT. Fig. 24 shows the sum of the switching and snubber losses at a turn-on and a turn-off event. The RCD snubber results in the lowest turn-off losses. However the total switching losses are slightly higher than for snubberless operation. The effect of the RC snubber is less distinct than with the RCD snubber.

The comparison was done at the following test conditions:

IGCT-Type 5SHY 35L4510  
 $T_j = 125\text{ °C}$ ,  $V_D = 2800\text{ V}$ ,  $R_{snub} = 3.6\ \Omega$ ,  $C_{snub} = 1\ \mu\text{F}$

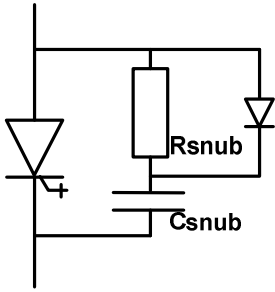


Fig. 21 RCD-snubber

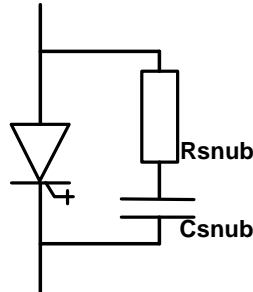


Fig. 22 RC-snubber

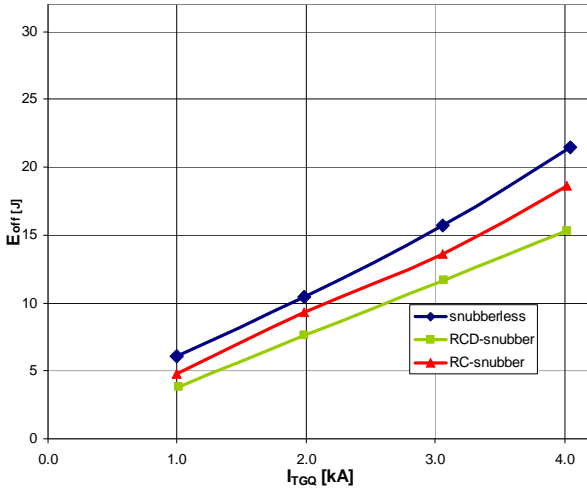


Fig. 23 Turn-off losses

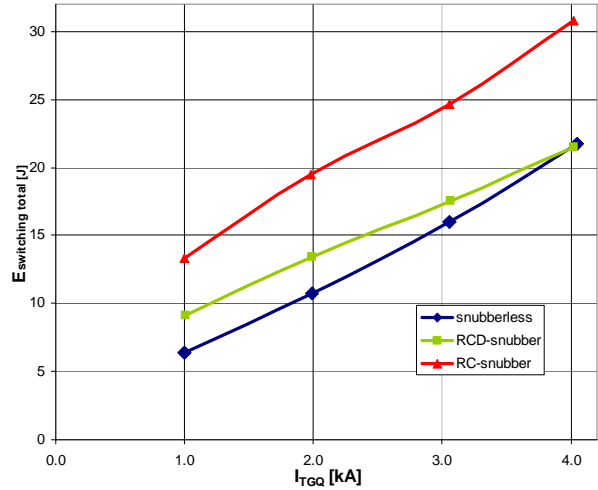


Fig. 24 sum of switching losses ( $E_{off} + E_{on} + E_{snubber}$ )

Fig. 25 shows how the losses are distributed between IGCT and snubber. The values  $E_{snubber\ off}$  and  $E_{snubber\ on}$  are the amounts of energy that are dissipated in the snubber circuit during a turn-off a turn-on event respectively.

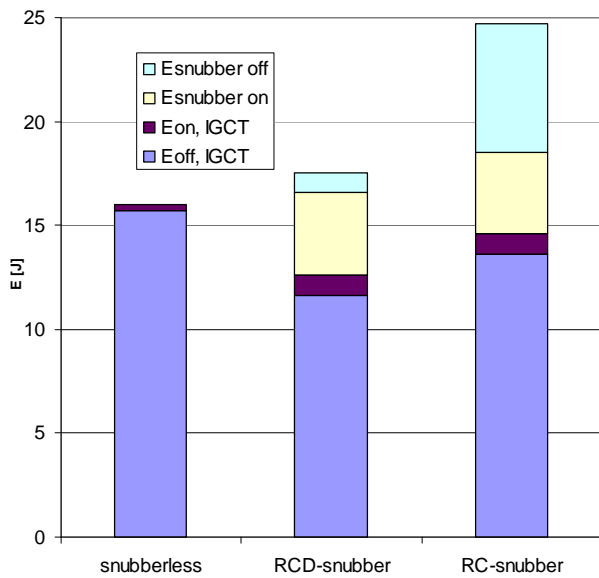


Fig. 25 Loss distribution (2800V, 3000A, 125°C)

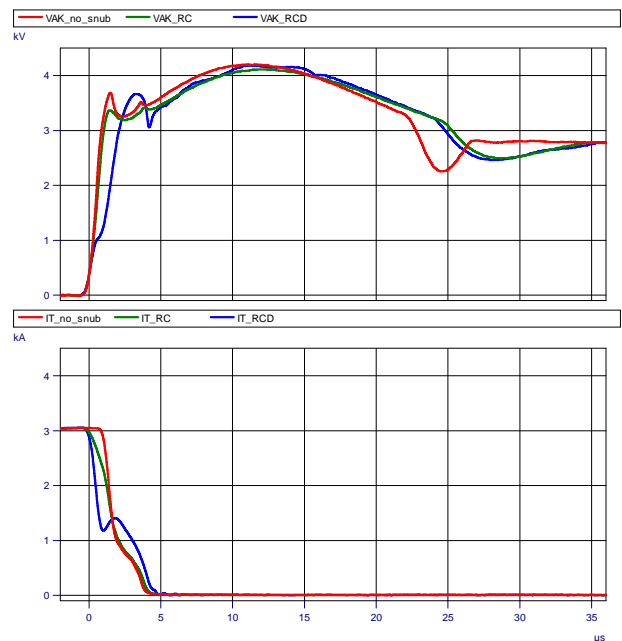


Fig. 26 comparison of turn-off waveforms (2800V, 3000A, 125°C)

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## 4.2 Retriggering of an IGCT

### 4.2.1 Introduction

The IGCT is basically a thyristor and requires a trigger pulse to turn on. A continuous gate current (back-porch current) is needed to hold it in the on-state when the GCT current drops below its holding current. In many applications the switch current even changes direction. In this case, an anti-parallel diode takes over the current and a slightly negative voltage appears across the GCT, more precisely, across the gate-cathode terminals in the case of asymmetric or RC devices, which tends to increase the forward gate-current. To protect the gate unit against an uncontrollable rise of gate current due to this negative voltage, the back porch current has to be reduced.

The GCT is not “conditioned” to conduct when the current finally commutates away from the diode and back to the GCT, since the gate current is reduced and furthermore, is flowing from the gate to the anode instead of to the cathode,. Therefore, when the switch’s current direction changes back from the anti-parallel diode to the IGCT, the GCT behaves like an inadequately gated thyristor. The GCT experiences a rising anode voltage accompanying the forward current, the product of which is termed “power pulse”. The power of such pulses is small, but because it does not occur homogenously over the whole GCT area, it results in a localized hot spot and may lead to thermal instability and possible destruction of the device.

To avoid this indeterminate triggering, a “retrigger pulse” is issued by the gate unit. The GCT is then completely and homogenously triggered by a sufficient supply of carriers to the p-base resulting in normal turn-on. Any remaining voltage peak is considered forward recovery.

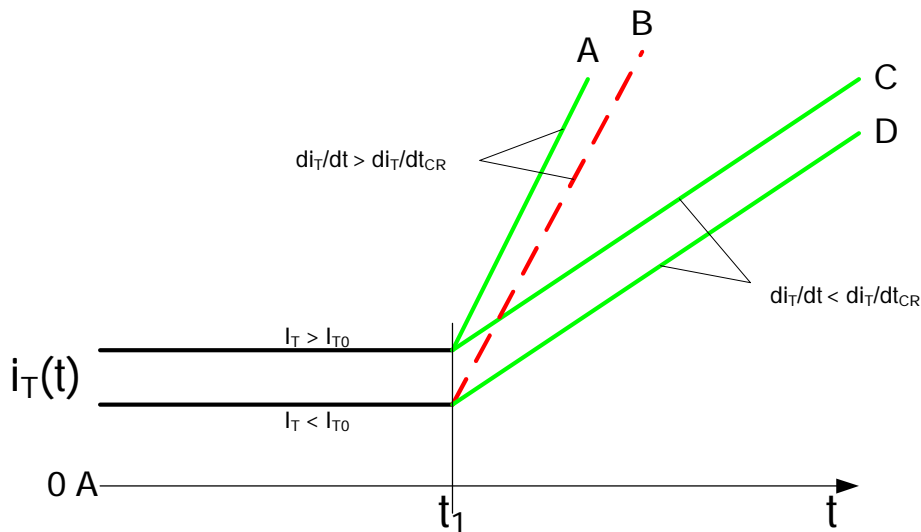
There are two different ways by which a retrigger may be released:

- a) internal retrigger: released by the gate unit itself when it detects zero crossing of the gate to cathode voltage
- b) external retrigger: released by the controller via the fiber optic command signal.

For low  $di_T/dt$  e.g. the zero crossing of the load current, the internal retrigger is sufficient, but for high  $di_T/dt$ , an external retrigger from the converter controller is recommended, as the instruction can then be synchronous with the event requiring the re-trigger (e.g. snubber discharge provoked by another phase). The self-retrigger is of the same amplitude as the external retrigger but is subject to a small delay due to the acquisition of the anode polarity change, a delay which might be unacceptable at high  $di/dt$ .

### 4.2.2 When are external retrigger pulses required?

External retrigger pulses are required when a fast  $di_T/dt$  occurs while the GCT is conducting little or no current. When the GCT is conducting large currents, i.e. the device is operating well above its holding current, high  $di_T/dt$  will not affect the GCT. Low  $di/dt$  is also not critical because either the gate unit can react with an internal retrigger pulse or the dissipated power is too low to harm the GCT. The critical current and  $di_T/dt$  levels are specified in the datasheet under “On-state: critical rate of rise of on-state current,  $di_T/dt_{CR}$ ”.



**Fig. 27** Triggering conditions <sup>1)</sup>

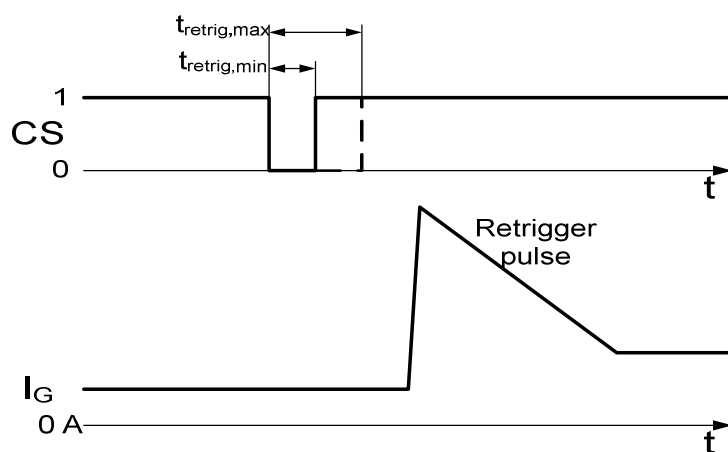
Fig. 27 above shows four different cases:

- A) / C) - the current prior to the  $di_T/dt$  is high enough not to require a retrigger irrespective of the  $di/dt$  value.
- B) - the current prior to the  $di_T/dt$  is too low; an external retrigger has to be released at  $t_1$
- D) - the  $di_T/dt$  is low enough for the IGCT to handle it without an external retrigger pulse.

<sup>1)</sup> The level of the initial current  $I_{T0}$  can be found in the datasheet in conditions section of "Critical rate of on-state current"

### 4.2.3 How are external retrigger pulses released?

An external retrigger pulse can be released by fiber optic command signal. During the on-state of the IGCT, the optical command signal is interrupted for a short period,  $t_{retrig}$  (see datasheet). This tells the gate unit to "re-arm" and then release a trigger pulse.



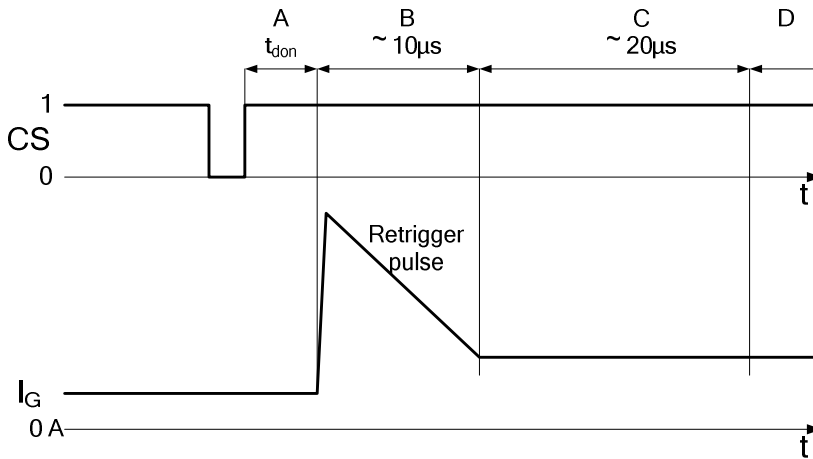
**Fig. 28** Release of external retrigger pulse

It is important to maintain the specified pulse-width  $t_{retrig}$  according to the datasheet, since too short a pulse will be ignored and too long a pulse will result in turn-off of the IGCT.



#### 4.2.4 What is the best timing for the external retrigger?

Fig. 29 shows the time response in four phases.



**Fig. 29** Phases of an external retrigger pulse

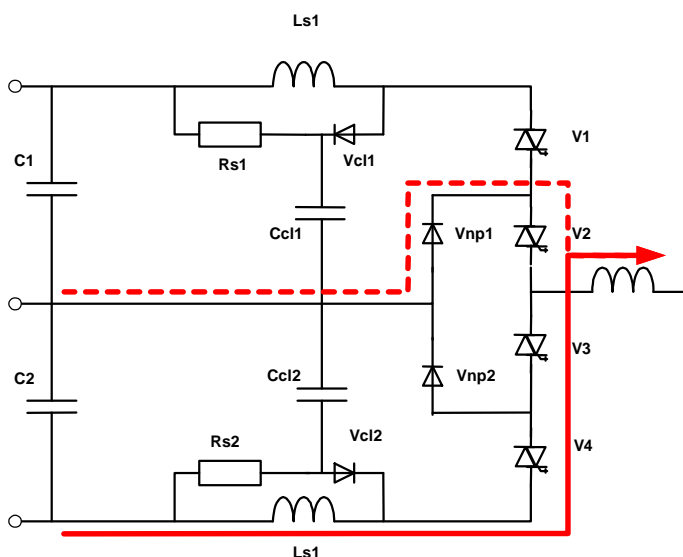
- A) delay time from command signal to retrigger pulse; retrigger not yet effective
- B) current pulse into gate; retrigger is fully effective.
- C) memory time, retrigger remains effective unless negative voltage was applied to the anode-cathode during phase B or C
- D) retrigger is no longer effective

It is therefore recommended that the release of the retrigger pulse be such that the  $di_T/dt$  occurs during phase B.

As mentioned earlier, in many applications, the  $di_T/dt$  is caused by the switching of another IGCT. Since the delay of the retrigger (phase A) is equal to the normal turn-on delay of an IGCT, synchronization of the retrigger command with the turn-on command of the high- $di/dt$ -originating IGCT is both possible and ideal.

#### 4.2.5 Applications requiring retrigger pulses

The occurrence of  $di_T/dt$  that requires retrigger pulses is not always obvious. One example is the 3-level VSI converter.



**Fig. 30** Commutation in 3-level VSI

We will analyze the following commutation:

Load current flows through the anti-parallel diodes of V4 ( $V_{4D}$ ) and V3 ( $V_{3D}$ ). Now  $V_{4GCT}$  is turned off and a few microseconds later,  $V_{2GCT}$  is turned on, while  $V_{3GCT}$  stays turned on. After this commutation, V4 will sustain the DC-link voltage of C2. However, before this happens, a reverse recovery current flows through the flooded diodes  $V_{4D}$  and  $V_{3D}$ .

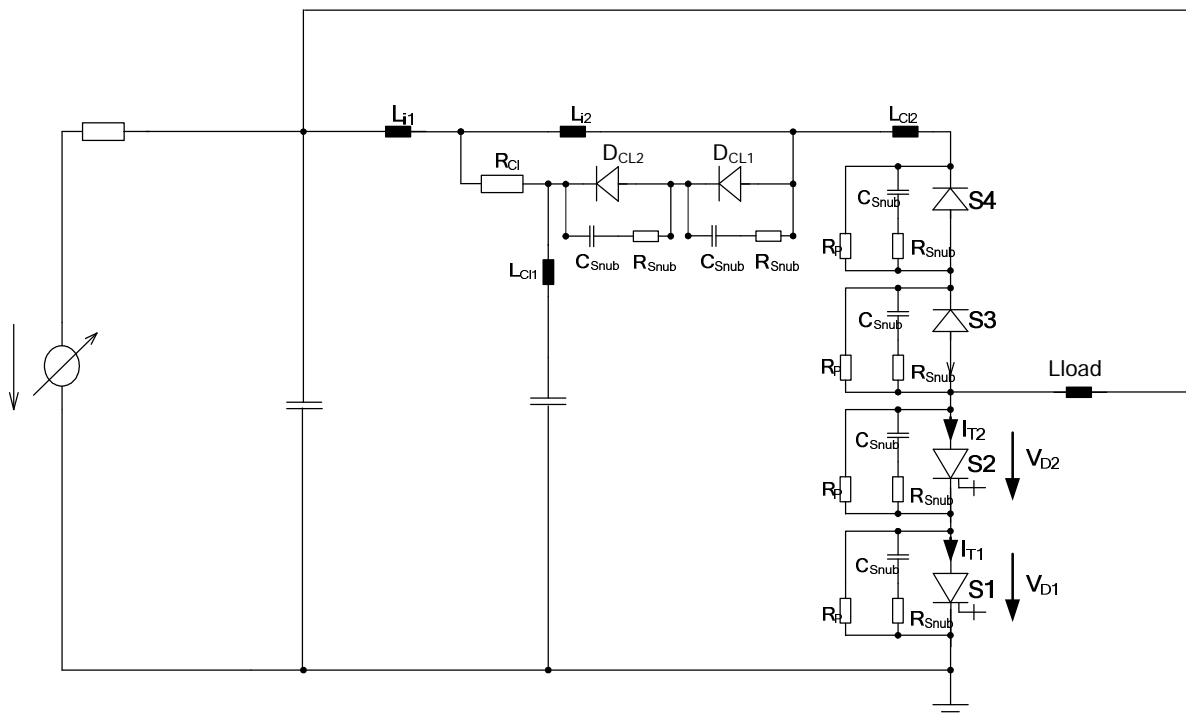
If the reverse recovery current of  $V_{4D}$  is larger than that of  $V_{3D}$ ,  $V_{3GCT}$  would have to take over the current difference, but  $V_{3GCT}$  is not conditioned for this and responds with a voltage spike (power pulse). In adverse conditions, voltage pulses of up to 2kV and 1 to 2 $\mu$ s duration may be observed. The application of an external retrigger pulse to  $V_{3GCT}$  in synchronism with  $V_{2GCT}$  is therefore highly recommended.

This is only one example for the causes of power pulses, but there are other possibilities. In particular, applications with RC-snubbers and clamp circuits common to all three phases must be carefully analyzed with regards to inter-phase snubber charge/discharge cycles. The circuit designer should look for cases where power pulses could occur and apply the appropriate external retriggering.

### 4.3 Series connection of IGCTs

Due to its technology, the IGCT is more suitable for series connection than for example the GTO. The GTO has a storage time of the order of 25  $\mu$ s, while the IGCT's storage time is reduced to about 1  $\mu$ s because of hard gate-commutation. The spread of storage time for the IGCT is thus very small which makes series connection possible with small equalizing snubbers.

However, series connection requires sharing snubbers for all blocking conditions, i.e. during turn-on, turn-off and in the off-state (under dc-voltage).



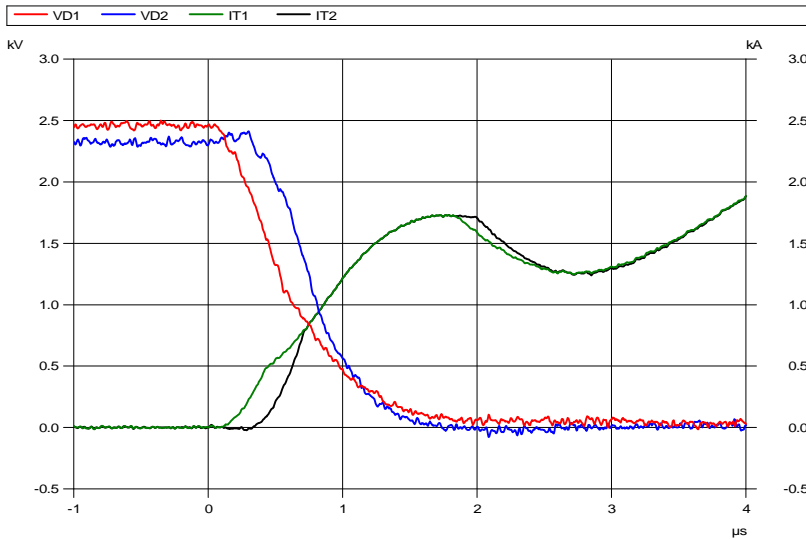
**Fig. 31** Schematic of test circuit

In designs with RC or RCD snubbers, the turn-off process is clearly more critical than that of turn-on. The most critical issue of the turn-on process is a time delay between the control signals of the series-

connected IGCTs. If one device is fired before the others, current starts to rise through this device and through the snubbers of the other devices, thereby charging their snubbers with a rate-of-rise determined by the  $di/dt$  inductor.

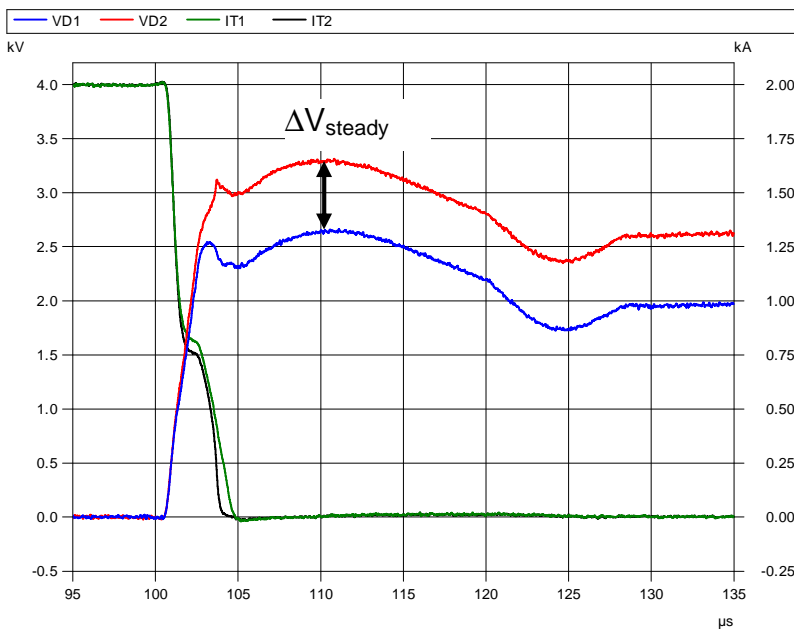
Fig. 32 shows the turn-on process in a series connection of two devices in a two-level phase-leg with sharing RC-snubbers across each device and a clamp circuit (test circuit of Fig. 31).

Device S2 is fired with a delay of 300ns with respect to device S1. The delayed firing causes an insignificant initial rise of the blocking voltage across device S2.



**Fig. 32** Turn-on process with RC snubber ( $1\Omega / 500\text{nF}$ ) per device

The turn-off process is more complex as the following sections will describe. Fig. 33 shows the turn-off of two series connected IGCTs illustrating the fact that parameter spread has a significant influence on the voltage sharing resulting in a voltage unbalance  $\Delta V_{\text{steady}}$ .



**Fig. 33** Turn-off process with RC snubber ( $1\Omega / 500\text{nF}$ ) per device

### 4.3.1 Design criteria

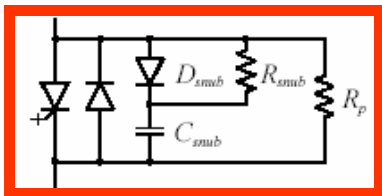
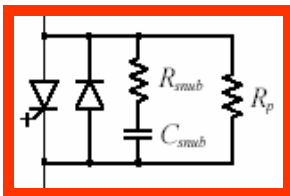
To design a converter with series-connected IGCTs, it is important to consider the following (boundary) conditions:

Peak and DC sharing	The voltage across each device must at all times stay at or below the rated value ( $V_{DRM}$ , $V_D$ ).
Cosmic Ray	The peak and DC voltage sharing is important for reliability since the failure rate is highly voltage dependent (see Application Note 5SYA2046 "Failure rate of IGCTs due to cosmic ray").
Redundancy	The most common failure mode of an IGCT is short circuit; the other series connected IGCTs must then be able to take over the voltage of a failed device, if continued operation is required.
Overall efficiency and cost aspects	The voltage sharing of the series connection can easily be improved by increasing the snubber size, but this will reduce overall efficiency and may increase converter cost; a compromise must be found between voltage sharing, efficiency and cost.

### 4.3.2 Snubber concepts

As discussed above, series connection of IGCTs always requires snubbing to share the voltage across the series-connected devices. A dynamic sharing snubber is required for voltage equalizing during switching. The most common of these are RC- and RCD snubbers. Additionally, a static sharing resistor ( $R_p$ ) is required. This is needed to compensate the leakage current differences of the devices and to neutralize the voltage differences after imbalanced turn-off.

The following table lists the advantages and disadvantages of both dynamic snubbers.

Concept	One RCD-snubber and static sharing resistor $R_p$ per IGCT 	One RC-snubber and static sharing resistor $R_p$ per IGCT 
Advantage	+ Effective turn-off snubbing + minor stress during turn-on	+ Effective turn-off snubbing + low number of components + damping effect
Disadvantage	- large time constant for static balancing - tends to voltage overshoot due to low damping - needs an additional diode per switch - large time constant of snubber discharge	- increased turn-on losses of IGCT. - large time constant for static balancing

### 4.3.3 Scaling of clamp design

In designs with clamp circuits, the clamp components can be scaled according to the following rules ( $n$  = number of series connected devices):

$$C_{CL}(n) = \frac{C_{CL}}{n}$$

$$R_S(n) = R_S \cdot n$$

$$L_I(n) = L_I \cdot n$$

$$L_{CL}(n) \leq L_{CL} \cdot n$$

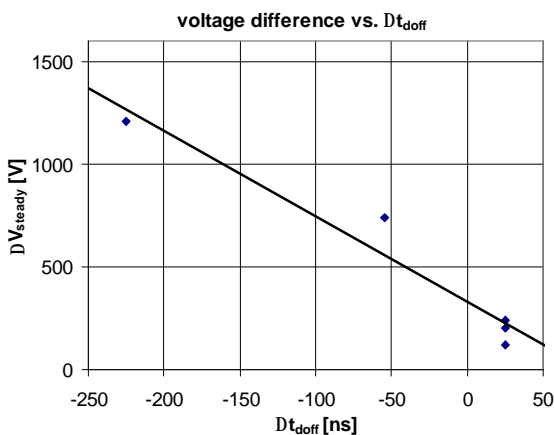
### 4.3.4 Factors influencing turn-off voltage sharing

In this section, we show the dependence of voltage sharing on various parameters for the case of an RC-snubber in a series connection with  $n = 2$  (see Fig. 31). The diagrams show test results with an RC-snubber of  $1\Omega / 500\text{nF}$  (unless otherwise mentioned).

#### 4.3.4.1 Variations of IGCT parameters

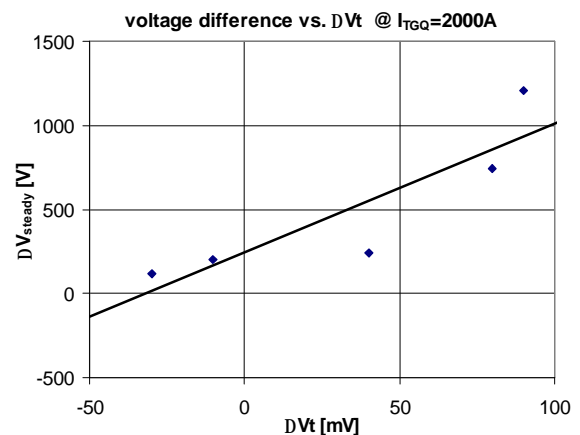
The main IGCT parameters which influence voltage sharing in series connection are shown below. Since there are other influencing parameters, the measurements do not show ideal voltage sharing even with seemingly identical devices.

$T_{\text{doff}}$ ,  $V_T$ :



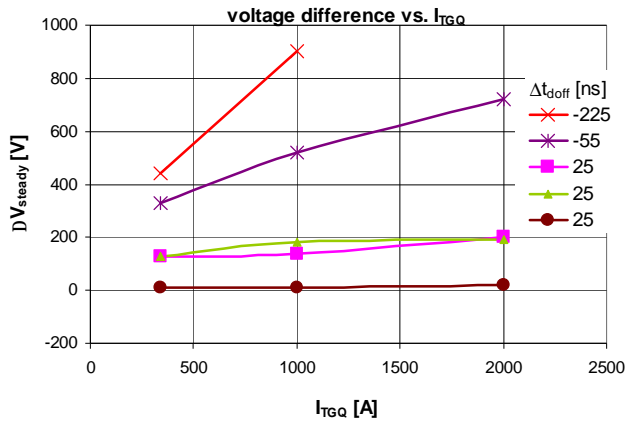
**Fig. 34**  $t_{\text{doff}}$  dependency

Differences in turn-off delay time directly influence voltage sharing; the device with the higher delay takes over less voltage



**Fig. 35**  $V_T$  dependency

Since  $t_{\text{doff}}$  varies with on-state voltage  $V_T$ , voltage sharing is also influenced by differences in  $V_T$



**Fig. 36**  $I_{TGQ}$  dependence

Devices with similar  $t_{doff}$  show good voltage sharing with low current dependence; with high  $\Delta t_{doff}$ , voltage sharing becomes highly current dependent.

- Best results can be achieved if the series-connected IGCTs have very similar  $t_{doff}$  and  $V_T$  values.

### $I_{DRM}$

Leakage current determines static voltage sharing. The differences in the leakage current tend to redistribute the snubber capacitor voltages and lead to static voltage asymmetries. To avoid these asymmetries, additional measures for static sharing are recommended

The simplest method of static sharing is the use of sharing resistors ( $R_p$ ) in parallel with the IGCTs. These resistors constitute a voltage divider that is additionally biased by the leakage current difference. These resistors have, therefore, to be chosen with a low enough resistance to handle the leakage current difference. Since many applications use anti-parallel freewheel diodes with IGCTs, the leakage current of these diodes also has to be considered.

ABB has extensive experience in the banding of IGCTs and diodes for series connection. For details, please contact your nearest representative or the address shown at the end of this application note.

#### 4.3.4.2 Variations of converter parameters

##### Command signal timing

Time differences between the command signals of series-connected IGCTs directly influence voltage sharing as shown in Fig. 37.

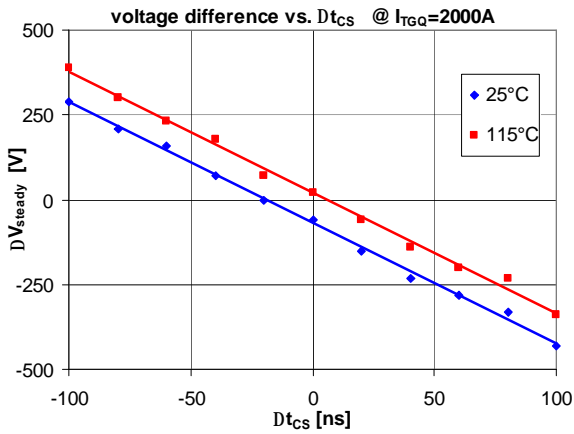


Fig. 37 Command signal dependency

##### Snubber capacitor ( $C_{Ssub}$ )

The RC-snubber is mainly a capacitive voltage divider biased by a charge difference from the IGCTs, therefore, the larger the capacitors, the better the voltage sharing as Fig. 38 shows. It is also important to minimize capacitor tolerances.

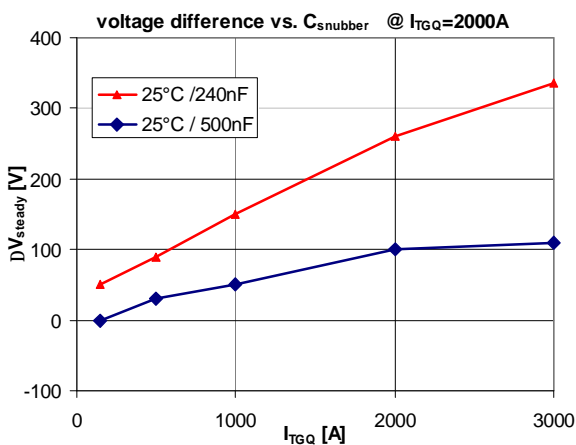


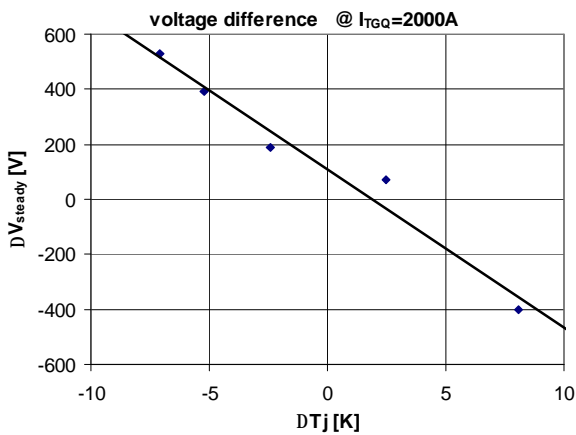
Fig. 38 Snubber capacity dependency

## Snubber resistor ( $R_{\text{Snub}}$ )

The snubber resistor is needed to limit the inrush current of the IGCT during turn-on. It also damps oscillations and minimizes overshoot during turn-off, if correctly chosen. A small resistor will increase the turn-on losses of the IGCT and reduce the damping effect. A large resistor will decouple the snubber capacitor and reduce its dynamic sharing ability. The time constant of the snubber should be of the order of the rise time of the IGCT voltage.

## Junction temperature differences:

The junction temperature has a significant influence on voltage sharing as shown in Fig. 39.



**Fig. 39**  $\Delta T_{\text{VJ}}$  dependency

The influence of junction temperature has to be considered in the design of the stack. In a stack with several series connected devices, often each heat sink serves two devices. However, the last heat sink in a stack contacts only one device. This device is, therefore, better cooled and may have a lower junction temperature. The same applies for stacks with redundant devices. If the redundant device fails, it generates less loss and therefore the neighboring devices will also have a lower junction temperature.

### 4.3.5 Optional anode voltage monitoring

In series connection, it is important to know if a GCT or a freewheeling diode has failed. For this purpose some IGCT types are available with an optional feedback signal that indicates the state of the anode voltage. Detailed information on this topic can be found in the application note 5SYA2031 "Applying IGCT Gate Units".

### 4.3.6 Conclusions

The series connection of IGCTs is possible with relatively small snubbers. However, the leaner the snubber design, the more severe is the impact of the factors influencing voltage sharing.

It is mandatory to verify the design thoroughly under worst-case conditions. This includes worst-case parameter variations and verification under switching conditions at rated frequency.



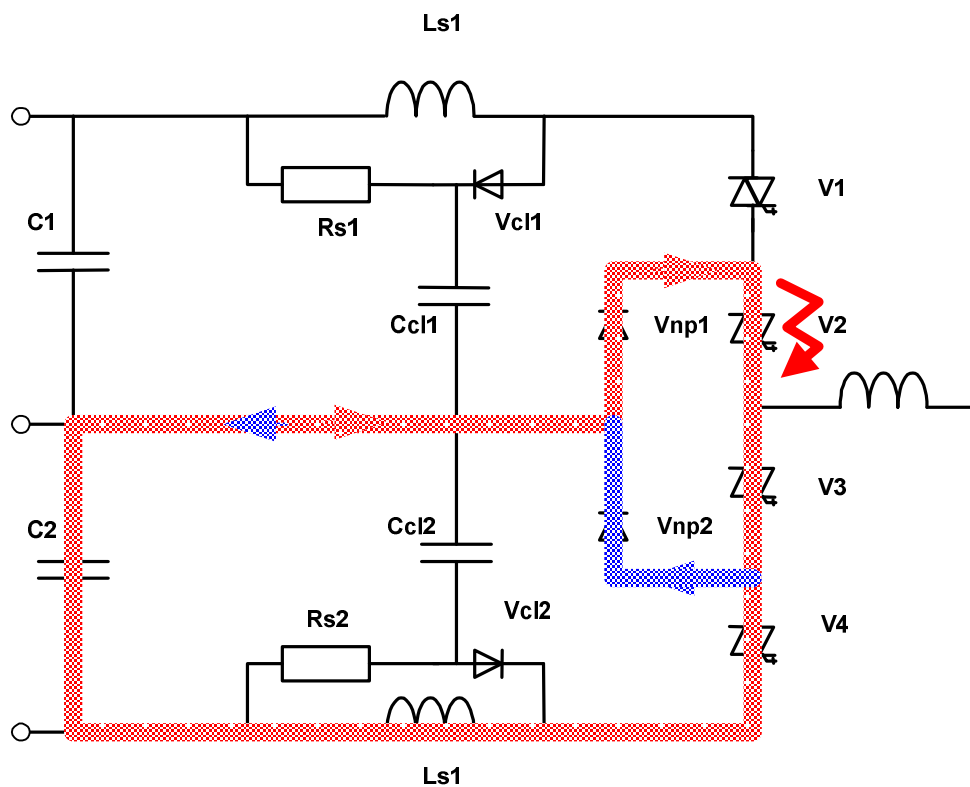
## 4.4 Protection

Unlike e.g. the IGBT, the IGCT does not limit its current. Therefore, in the case of a short circuit, the IGCT current can rise to an uncontrollable level and measures have to be taken to avoid destruction of the device.

### 4.4.1 Consequence of a GCT or diode failure in a 3-level phase-leg (example)

A failure of an IGCT normally results in a short circuit. To limit consequential damage, the protection concept has to be carefully investigated.

As an example, we will have a closer look at a phase-leg of a three-level converter. Let's assume that IGCT V2 fails during its turn-off. This does not have immediate catastrophic results. However, as soon as V4 is turned on, a short circuit current starts to rise through C2, Vnp1, V2, V3, V4, and Ls1. This is called a shoot-through.



**Fig. 40** Current path in case of a shoot through

The consequence of a shoot-through depends on the surge current that follows and on the reaction of the control electronics to this event.

- The surge current may be small enough allowing the components in the loop to survive
- The surge current is a damped oscillation and therefore changes direction. The negative current finds its path through Vnp2 and in reverse through V4. If the voltage drop across V4 exceeds 17 V the GCT V4 may be damaged. To avoid this reverse voltage a freewheeling path may be provided.
- A protective turn off of V4 is, in most cases, not suitable because the surge current rises too fast above a controllable level. Any attempt to turn-off then will inevitably lead to failure of V4.
- To decrease the surge current stress of the single device, it may be useful to distribute the current to additional components.

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- The best solution would be to avoid turning on V4 in the first place. This would avoid the discharge of the capacitor C2 completely. However, it may be difficult to detect the failure in time. The status feedback of the IGCT can detect a failure of the GCT, but depending on the extent of the failure on the GCT wafer, this may take too long. It is, therefore, not recommended to base the protection concept solely on the status feedback signal of the IGCT.
  - The discharge of the dc-link capacitor might be followed by a slower surge current, caused for example by the grid or the inertia of a motor. This current also has to be taken in account when the surge current is rated.

## 5 Glossary

AS-IGCT	Asymmetric IGCT
Back porch current	Continuous current, delivered to the GCT gate as holding current
CSI	Current source inverter
DUT	Device Under Test
FWD	Free Wheeling Diode
Gate unit	Driver board for the GCT
GCT	Gate Commutated Thyristor
IGCT	Integrated Gate Commutated Thyristor (GCT with gate unit)
RB-IGCT	Reverse Blocking IGCT
RC-IGCT	Reverse Conducting IGCT
SOA	Safe Operating Area
VSI	Voltage source inverter

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## 6 Additional notes

### 6.1 References

- 1) 5SZK9107 "Specification of environmental class for pressure contact IGCTs, OPERATION", available on request, please contact your nearest representative or the address shown at the end of this application note
- 2) 5SYA2031 "Applying IGCT Gate Units"
- 3) 5SYA2036 "Recommendations regarding mechanical clamping of Press-pack High Power Semiconductors"
- 4) 5SYA2048 "Field measurements on High Power Press Pack Semiconductors"
- 5) 5SYA2051 "Voltage ratings of high power semiconductors"
- 6) 5SYA2046 "Failure Rates of IGCTs due to Cosmic Rays"

The application notes, References 2 to 6, are available at [www.abb.com/semiconductors](http://www.abb.com/semiconductors)

### 6.2 Application support

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