GP-6 ANALOG COMPUTER

OPERATOR'S MANUAL

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1. GP-6 OPERATING PROCEDURES

1.0 CONNECTION OF EXTERNAL READOUT INSTRUMENTS

The GP-6 functions in the slow time and/or high speed repetitive operation modes. Slow time outputs are normally recorded with an XY plotter; repetitive operation outputs are normally displayed with an oscilloscope having DC horizontal and vertical inputs. Slow time outputs also may be recorded with a strip chart recorder; repetitive operation outputs also may be displayed with an oscilloscope having a DC vertical input and an internal time base with an external trigger.

It is noted that the GP-6 is furnished with various options that must be considered for connection and calibration of readout instruments.

1. Slow time only (no internal time base.)
2. Slow time only (internal time base provided.)
3. High speed repetitive operation only (internal time base provided.)
4. Slow time and repetitive operation (internal slow and high speed time bases provided.)

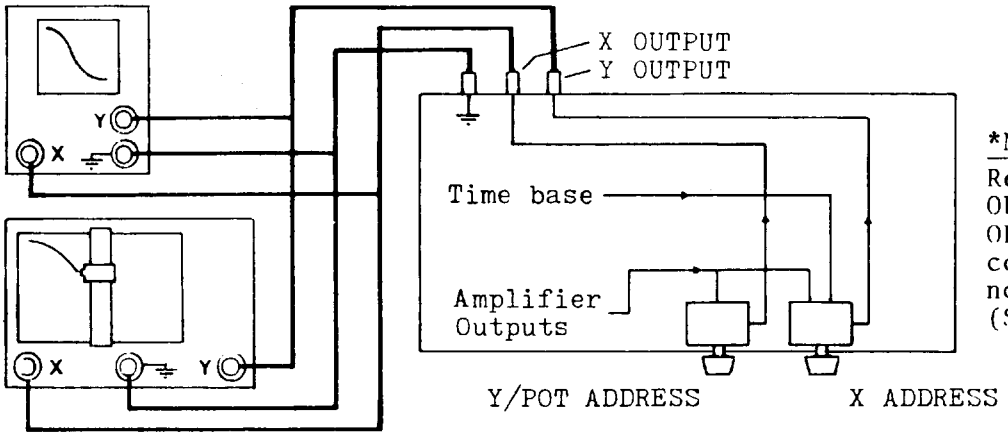


Figure 1-1

*Note:
Rear terminals OP OUTPUT and OP INPUT must be connected for normal operation. (See para. 2.8)

Rear terminals on the GP-6 offer convenient connections to the X and Y inputs of the plotter and/or oscilloscope. The three connections are shown in Fig. 1-1 and listed below:

1. Common ground.
2. "Y OUTPUT" to the plotter and/or oscilloscope Y (vertical) input,
3. "X OUTPUT" to the plotter and/or oscilloscope X (horizontal) input.

If the oscilloscope's internal time base and external trigger is to be used for display of repetitive solutions, the external trigger input should be connected to the "OP OUTPUT" rear terminal. The OP Output mode control logic is a convenient trigger for repetitive outputs.

1.1 CALIBRATION OF READOUT INSTRUMENTS

The readout plotter or oscilloscope is calibrated so that the full scale horizontal and vertical axes extend between the computer's negative and positive reference (minus to plus ten volts) as shown in Fig. 1-2.

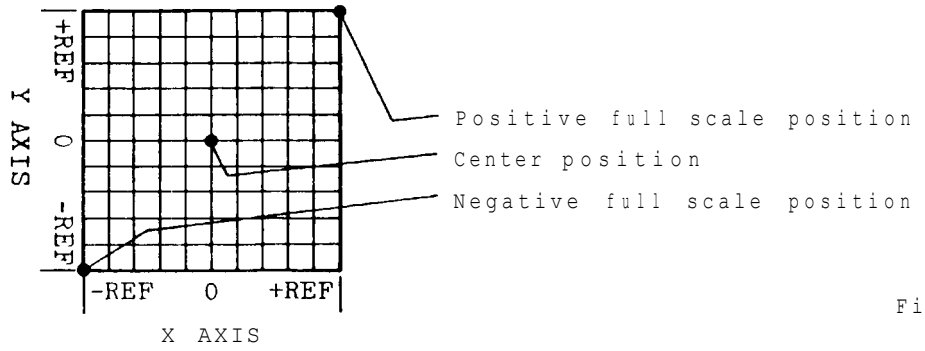


Figure 1-2

The following are procedures for input scaling adjustments:

1. Position the Mode Selector switch to "OPR."
2. Depress the "1C" mode control push button.
3. Position both the "Y/POT ADDRESS" and "X ADDRESS" switches to "GND."
4. Adjust the plotter or oscilloscope Y and X zero controls until the plotter's pen or oscilloscope's dot is in the graph or display center position as shown in Fig. 1-2.
5. Position the "Y/POT ADDRESS" and "X ADDRESS" switches to "-REF."
6. Adjust the plotter or oscilloscope Y and X scale controls until the plotter's pen or oscilloscope's dot is in the graph or display negative full scale position as shown in Fig. 1-2.
7. Position the "Y/POT ADDRESS" and "X ADDRESS" switches to "+REF."
8. Check the pen or dot. It should be in the positive full scale position.
9. Repeat the above procedures if necessary.

The readout instruments are calibrated to present either Y vs Time or Y vs X curves depending on the positions of the Y and X address switches. Amplifier outputs appear as variables that function within their full scale negative and positive operating ranges. The time base is presented so that the negative full scale co-ordinate is a zero time condition and the positive full scale co-ordinate is the compute time period. Time co-ordinates, therefore, depend on the operator's choice of a time period that is adjustable within a range of 10 to 100 computer time scaled seconds.

If the oscilloscope internal time base is to be used for the repetitive display, the high speed time scale ratio of 400:1 must be considered. One computer time scaled second is equal to 2.5 milliseconds of real time.

1.2 SETTING COEFFICIENT POTENTIOMETERS

Coefficients are set in a potentiometer setting mode with the internal readout meter that is either a digital voltmeter or null meter depending on the option that is furnished. Procedures for setting coefficient potentiometers are listed as follows:

1. Coefficients are set after all patching is completed. (It is noted that when used as normal attenuators the bottom ends of potentiometers 7 and 8 must be patched to ground.)
2. Position the "MODE SELECTOR" switch to "POT SET."
3. Position the "Y/POT ADDRESS" switch to the number of the potentiometer to be set.

4a Where the digital voltmeter is employed the coefficient value is displayed. Adjust the potentiometer until the desired setting is observed.

4b Where the null meter is employed the potentiometer must be nulled against a preset potential. Prior to setting the coefficient potentiometer adjust the null potentiometer until the calibrated dial shows the desired coefficient value. Place the adjacent toggle switch in the up position. Adjust the coefficient potentiometer until the null meter needle is in a null (center) position.

1.3 SETTING THE COMPUTE TIME PERIOD

The Compute Time Period is the full scale X axis co-ordinate for response curves produced by the XY plotter or displayed on the oscilloscope when the computer's internal time base is employed.

Procedures for setting the Compute Time Period are as follows: (Note- only units furnished with the internal time base have the Compute Time Period setting feature.)

1. Position the "MODE SELECTOR" switch to "POT SET."
2. Position the "Y/POT ADDRESS" switch to "GND/X."
3. Position the X ADDRESS" switch to "CTP."

4a Where the digital readout is employed, the display shows CTP/100 computer time scaled seconds. Adjust the "COMPUTE TIME" control until the desired Compute Time Period is observed.

4b Where the null meter is employed, first set the null potentiometer to the desired CTP/100 value. Place the adjacent toggle switch into the down position. Adjust the "COMPUTE TIME" control until a null condition is observed.

1.4 STATIC MEASUREMENT OH AMPLIFIER OUTPUTS

The amplifier address and internal readout meter may be used for the static measurement of amplifier outputs.

1.4.1 Measurement of amplifier outputs in the Pot Set mode. (The "MODE SELECTOR" switch is in the "POT SET" position.)

1. Position the "Y/POT ADDRESS" switch to "GND/X."
2. Position the "X ADDRESS" switch to the number of the amplifier output to be measured.

3a Where the digital readout is employed the addressed amplifier output is displayed. Its polarity is automatically indicated.

3b Where the null meter is employed first the toggle switch must be in the position for the correct output polarity. If the amplifier output is positive the toggle switch must be in the up position; if the output is negative the toggle switch must be down. Adjust the null potentiometer until a null condition is observed. The null potentiometer dial reading is the measured amplifier output.

1.4.2 Measurement of amplifier outputs in the Operate mode. (The "MODE SELECTOR" switch is in the "OPR" position.)

1. Patch the rear terminal "Y OUTPUT" to rear terminal "METER INPUT."
2. Position the "Y/POT ADDRESS" switch to the number of the amplifier output to be measured.
3. Follow above procedures 3a or 3b to measure the desired amplifier output.

1.4.3 Measuring the sum of integrator inputs. The sum of integrator inputs, as rcquired in standard program static check procedures, may be measured as follows:

1. Position the "MODE SELECTOR" switch to "OPR."
2. Depress the "IC" mode control push button.
3. Patch the "SJ" jack of the integrator input to be measured to the "SJ" jack of an unused amplifier; the unused amplifier is to have a 1 resistor feedback.
4. Measure the summer amplifier output using the procedures of 1.4.2. The summer output is the inverted sum of the integrator inputs.

1.5 PROBLEM SOLUTION

Problem solution is oriented primarily to the XY graph or display. Following programming, patching, setting of coefficients, program check out and setting the compute time period, the program is ready to be run. Computed variables are ready to be recorded, displayed and evaluated.

The principle graphical readout is the response curve where dependent variables (amplifier outputs) are presented as functions of the independent variable time. To obtain response curves:

1. Position the "Y/POT ADDRESS" switch to the number of the amplifier output that is to be the curve's ordinate.
2. Position the "X ADDRESS" switch to "TIME."

3a For XY plotter readout, depress the "IC" mode control push button. (All integrators are placed into the initial condition mode.)

4a Depress the "OP" push button. (All integrators are simultaneously placed into an operate or run state and the plotter produces the Y vs Time response curve.)

3b For oscilloscope readout, depress the "RO" mode control push button. (The response of all integrators is increased by a factor of 400; all integrators are repeatedly switched from initial condition to operate modes and the complete response curves appear on the oscilloscope display.

If the response curve is to be evaluated in physical units, the amplifier output scale factor (maximum estimated amplitude) is the full scale Y axis co-ordinate and the function operates within the range of zero to plus or minus the scale factor value. The full scale real time co-ordinate is the compute time period divided by the time scale factor.

If the operator determines that the compute time period is either too long or too short for convenient readout, the "COMPUTE TIME" control may be adjusted and a new compute time period established. It is emphasized that adjustment of the "COMPUTE TIME" control does not alter the response function but varies only the period that is observed. (If the full range "COMPUTE TIME" control adjustment does not meet readout requirements, a new time scale factor must be selected and coefficient settings recalculated.)

An alternate graphical readout is the phase-plane curve (a variable plotted against its derivative) or a curve of one variable plotted against another variable. To produce such curves position the "X ADDRESS" switch to the amplifier output that is to be the abscissa and follow above procedures 3a and 4a or 3b.

It is noted that the curves displayed on the oscilloscope are identical to graphs produced by the XY plotter. If the oscilloscope and plotter are used for the simulation analysis it is convenient to connect both readout instruments and leave the plotter in a stand-by condition when not being used. The analysis may then be conducted as follows:

1. Evaluate functions in the repetitive operation mode with the oscilloscope display. A view of the total output curves and the quick response to parameter changes is often valuable to an understanding of problem characteristics. When hard copy is desired the curve may then be plotted.
2. Depress the "IC" mode control push button.
3. Activate the plotter.
4. Depress the "OP" push button and plot the curve that was displayed on the oscilloscope.

In addition to the initial condition and operate modes described in above procedures 3a and 4a, output functions may be placed into a hold condition. At any time during a run computer time may be stopped by depressing the "HD" mode control push button. The hold mode enables the operator to evaluate the static values of variable at desired points in time. From the hold mode the run may either be continued by re-depressing the "OP" pushbutton or the function may be returned to the initial condition state by depressing the "IC" push button.

1.6 SLAVING TWO OR MORE COMPUTERS

When problem requirements exceed the capacity of one unit two or more GP-6 computers may be slaved into a single operating system.

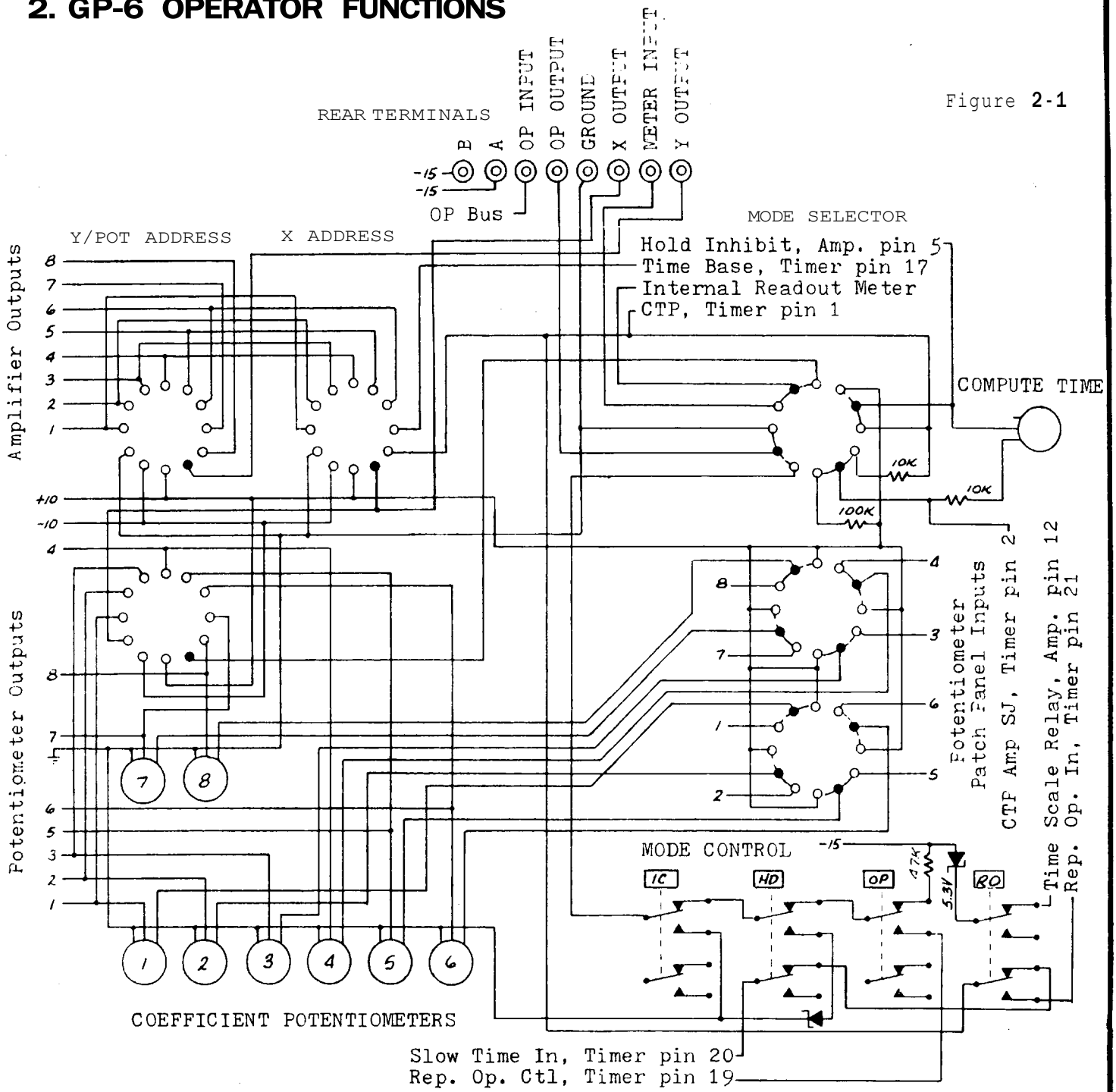
1. Designate a unit to be the master; others shall then be slaves to the master.
2. Connect a common ground between units through rear terminals "GND."
3. Program each unit and then patch interconnections. Patching between panels is identical to patching within a panel.
4. On all slave units remove the shoring wire between rear terminals "OP OUTPUT" and "OP INPUT."
5. Connect the rear terminal "OP OUTPUT" of the master to the "OP INPUT" terminals of all slave units.
6. The modes of all slaved units will then be controlled by operation of the master computer.

1.7 POWER

The 115 volt A.C. power switch is a part of the Compute Time control. To turn power "on" rotate the Compute Time control clockwise from the "OFF" position. The above pilot light indicates a power-on condition.

2. GP-6 OPERATOR FUNCTIONS

Figure 2-1



2.0 GP-6 OPERATOR FUNCTIONS

Figure 2-1 is a schematic of operator functions. Descriptions of individual functions are described in the following.

2.1 Y/POT ADDRESS

The Y/Pot Address switch is an 11 position, 2 pole rotary switch. One section selects amplifier outputs for external readout; the other section selects coefficient potentiometer outputs Cor setting attenuator constants. The amplifier selector wiper is connected to the rear terminal "Y OUTPUT;" the potentiometer selector is connected to the Mode Selector switch and is the input to the internal readout meter in the Pot Set mode. Tt is noted that the "GND/X" position of the potentiometer section is connected to the X Address switch wiper so that the internal readout meter may be used to measure the X Address selections in the Pot Set mode.

2.2 X ADDRESS

The X Address switch is an 11 position, 1 pole rotary switch. It selects amplifier outputs, the internal time base and the CTP output for both external and internal readout. The wiper is connected to the rear terminal "X OUTPUT" and the "GND/X" position of the Y/Pot Address switch, potentiometer section.

2.3 MODE SELECTOR

The Mode Selector switch is a 2 position, 12 pole rotary switch. It provides a number of functions that distinguish the computer's Pot Set and Operate modes.

2.3.1 Setting of Coefficient Potentiometers

The top end input to each coefficient potentiometer is connected to one of 8 poles. In the OPR position the poles are switched to the patch panel input; in the POT SET position the poles are switched to positive reference. Thus in the Pot Set mode the inputs to all potentiometers are replaced by positive reference and the potentiometer output values are measurements of voltage divider ratios.

2.3.2 Internal Readout Meter

One pole is connected to the internal readout meter input. In the POT SET position the pole is switched to the X Address switch wiper; in the OPR position the pole is switched to the rear terminal "METER INPUT."

2.3.3 Integrator Mode Control

One pole is connected to the rear terminal "OP OUTPUT." In the Pot Set mode the pole is switched to ground; in the OPR position the pole is switched to the push button mode control selection. Thus in the Pot Set mode all integrators are placed into an initial condition state; in the OPR mode integrators are controlled by the push button mode switches.

2.3.4 CTP Amplifier

Two poles are used to program the CTP amplifier as shown in Figures 2-1 and 2-2. The CTP amplifier is located on the Timer board assembly.

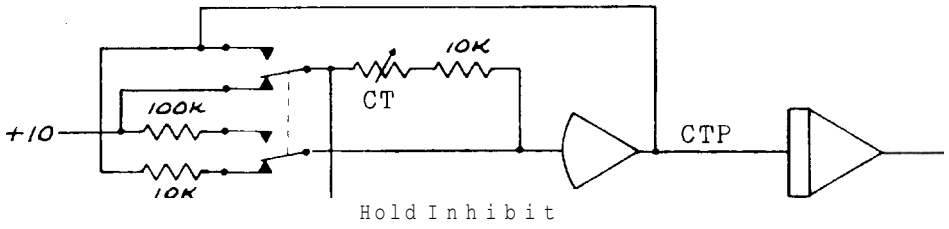


Figure 2-2

In the OPR position, positive reference is applied through the Compute Time control (100K ohms) and a series 10K ohm resistor to the CTP amplifier summing junction. A 10K ohm resistor is the feedback, therefore,

$$CTP = -10/(CT + 10) \times Reference.$$

in the POT SET position, positive reference is applied through a 100K ohm resistor to the CTP amplifier summing junction. The Compute Time control and 10K ohm resistor is the feedback, therefore,

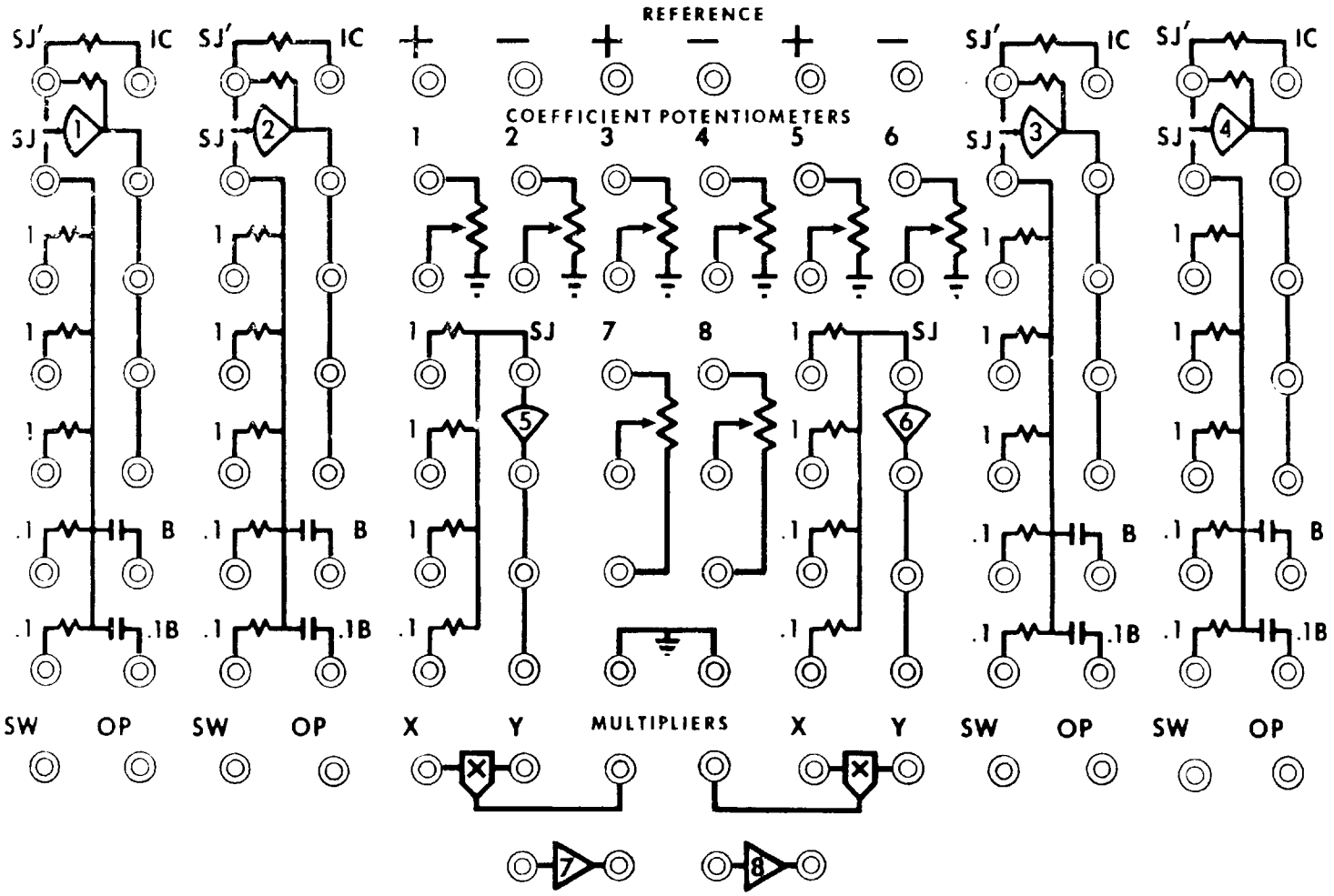
$$CTP = -(CT + 10)/100 \times Reference.$$

The CTP amplifier output in the POT SET position is one tenth the reciprocal of its value in the OPR position. As the CTP output is the input to the time base integrator, its reciprocal is a measurement of the Compute Time Period.

2.3.5 Hold Inhibit

In the normal integrator initial condition mode the hold switch is shut off, thereby isolating the input resistor network. It is necessary, however, to set potentiometers with their resistor loads connected. Therefore, during the pot set mode each

3. GP-6 PATCH PANEL



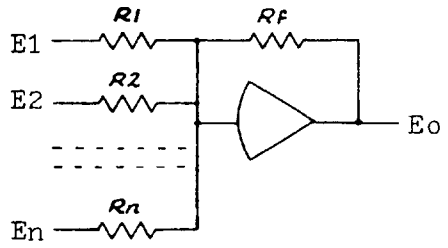
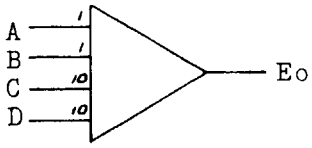
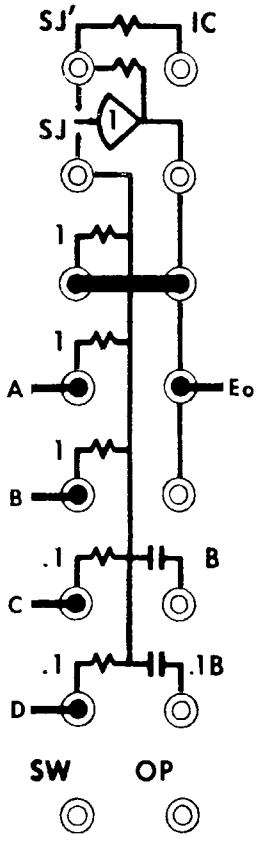
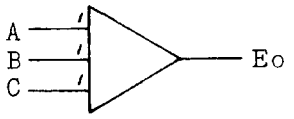
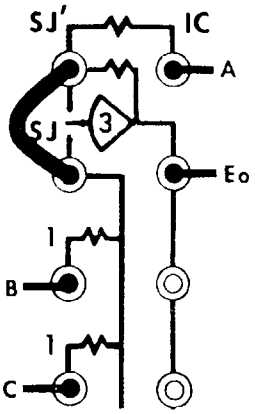
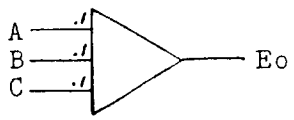
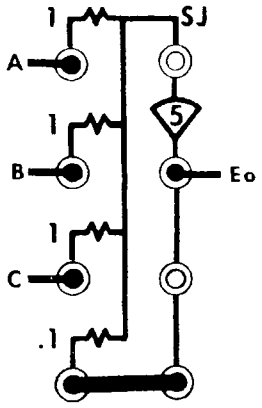
Patch panel graphics represent networks as they arc applied in normal analog computer programming. Amplifiers 1 thru 6 may be used as summers or high gain operational amplifiers; amplifiers 1 thru 4 have electronic switch networks and may also be programmed as integrators, track/store amplifiers and single pole, double throw electronic switches. Amplifiers 7 and 8 are inverters. Potentiometers 1 thru 6 are attenuators. Potentiometers 7 and 8 have their bottom ends open and may be used as voltage dividers or attenuators. Multiplier networks have current outputs; with one amplifier each may he used as a multiplier, divider, squarer or square root extractor.

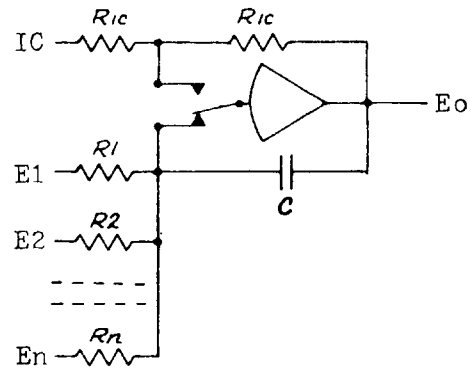
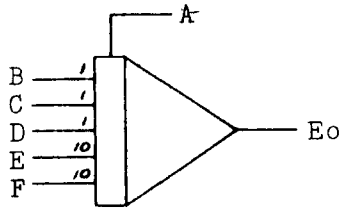
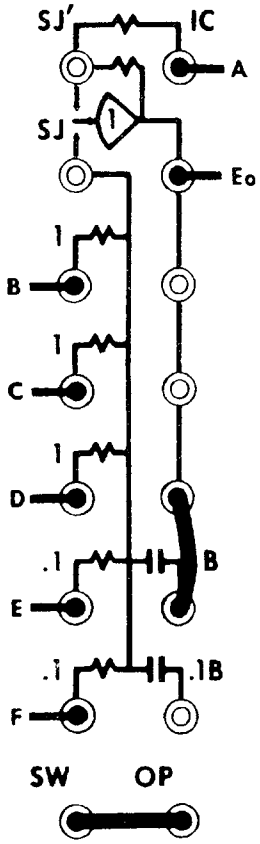
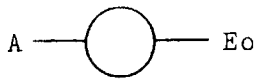
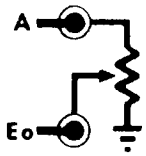
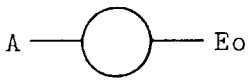
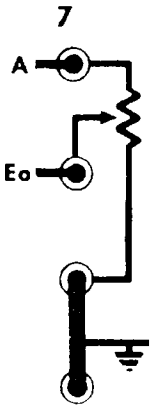
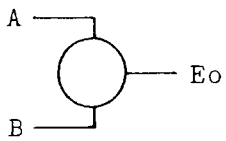
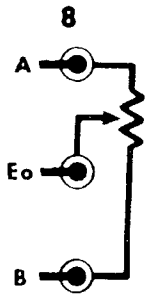
The following is a description of patch panel symbols:

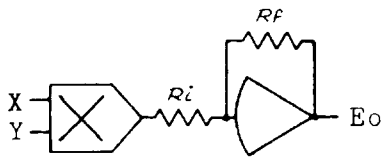
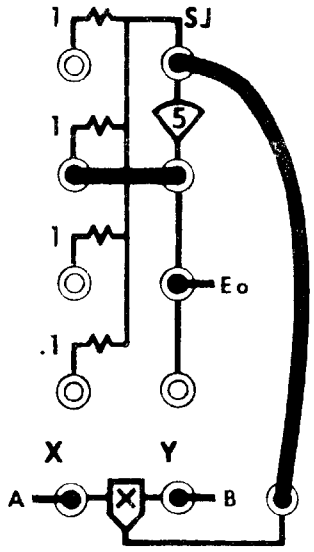
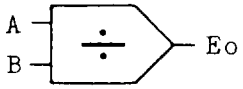
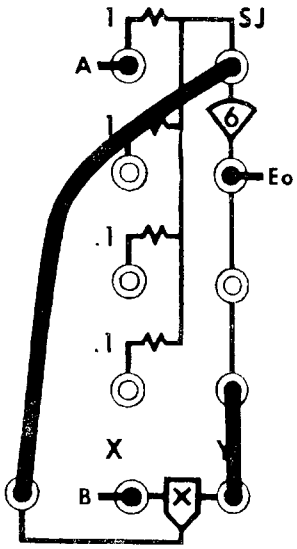
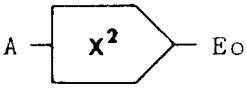
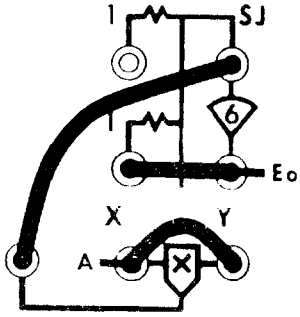
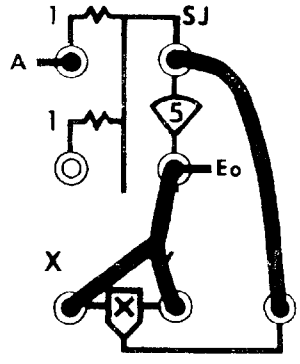
SYMBOL	COLOR CODE	DESCRIPTION
+	Red	Positive reference, considered unity, 1.0 for normalized programming. (Actual amplitude is 10 volts.)
—	Yellow	Negative reference
5		High gain operational amplifier.
3		High gain operational amplifier with electronic switch.
7		Inverter
	Red	Amplifier output.
SJ	Gray	The summing junction for amplifiers 1 thru 6. (Active for amplifiers 1 thru 4 when a logic "1" is applied to the "SW" switch control jack or when there is no switch control patching.)

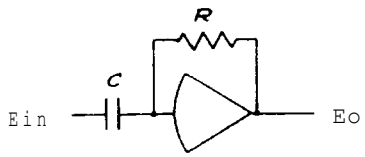
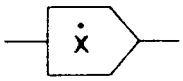
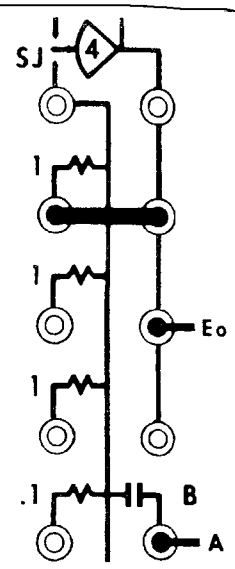
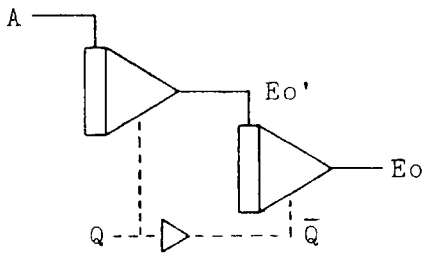
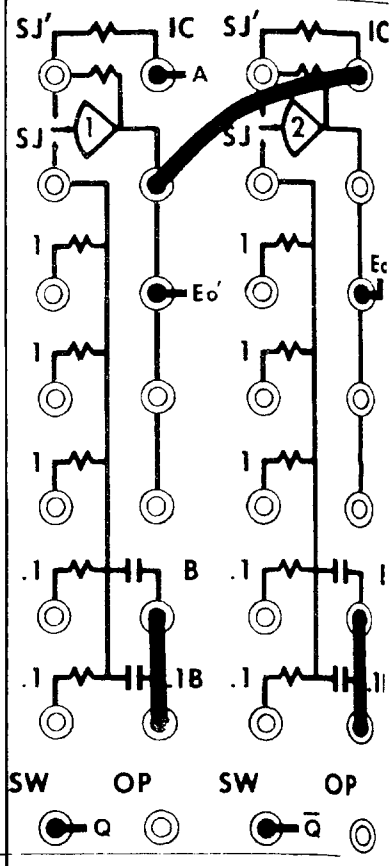
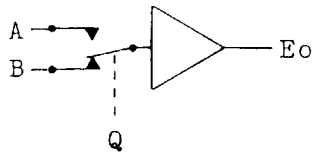
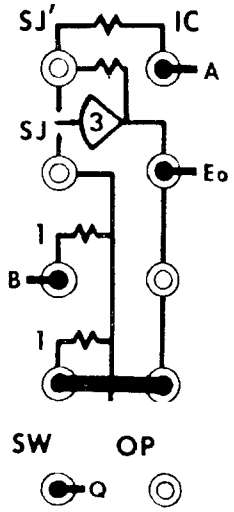
SYMBOL	COLOR CODE	DESCRIPTION
SJ'	Gray	Alternate summing junction for amplifiers 1 thru 4. (Active when a logic "0" is applied to the "SW" switch control jack.)
1	Green	Standard input summing resistor, normalized as a unity value to simplify programming. (Actual value is 50 K ohms.)
.1	Green	Summing resistor input that has a value one tenth the standard. (Actual value is 5 k ohms.)
B	Green	Standard integrating capacitor input, normalized so that the 1 resistor and B capacitor combination produces a one second time constant as referred to programming time scales. (Actual value is 20 ufd in the slow time mode and .05 ufd in the repetitive operation mode.)
.1B	Green	Integrating capacitor input that has a value one tenth the standard. (Actual value is 2 ufd in the slow time mode and .005 ufd in the repetitive operation mode.)
SJ' IC 2	Green	Resistor input to the SJ' summing junction. Amplifier becomes an inverter when SJ' is active. Normally used for integrator initial conditions. Input and feedback resistors may be used for summer operation by patching SJ' to SJ. (Actual value of input and feedback resistor is 50 k ohms.)
	Yellow	Attenuator, input and wiper indicated by standard electrical symbol.
	Yellow	Voltage divider; top, bottom and wiper indicated by standard electrical symbol. Bottom must be patched to ground for attenuator operation. (Potentiometer value is 5 k ohms.)
	Black	System ground.
		Multiplier network.
X	Brown	One of two multiplier inputs.
Y	Brown	One of two multiplier inputs.
	Brown	Multiplier output, a current proportional to the product of inputs "X" and "Y"; normalized so that when connected to the summing junction of an operational amplifier with a 1 resistor feedback, and with reference applied to "X" and "Y", the amplifier output equals reference.
SW	White	Electronic switch control input. With a logic "0" (ground or positive voltage) the SJ' summing junction of the above amplifier is active and SJ shuts off. With a logic "1" (-5 thru -15 volts) SJ is active and SJ' shuts off. With "HD" logic (-2 thru -3 volts) SJ' shuts off, the SJ summing junction is active but the summing resistor network is disconnected. "IID" logic is used for normal integrator hold mode operation.
OP	White	The computer's operate bus; provides integrator mode logic (slow time, repetitive operation or slave) as selected by the operator. Normal integrator operation requires that the "OP" bus be patched to the "SW" switch control input.

PATCH PANEL OPERATIONS

FUNCTION	OPERATION	PATCHING
Summer (amplifiers 1-4)	Fundamental Summer Operation  Eo = -Rf(E1/R1 + E2/R2 ... + En/Rn)  Eo = - (A + B + I0C + 10D) NO PATCHING TO SWITCH CONTROL "SW"	
Summer (amplifiers 1-4 with IC networks)	 Eo = - (A + B + C) NO PATCHING TO SWITCH CONTROL "SW"	
Summer (amplifiers 5 & 6)	 Eo = -(.1A + .1B + .1C)	
Inverter (amplifiers 7 & 8)	Eo = -A	

FUNCTION	OPERATION	PATCHING
Integrator (amplifiers 1-4)	Fundamental Integrator Operation  $Eo = -1/C\int(E1/R1 + E2/R2 \ldots + En/Rn)dt - IC$  $Eo = -\int(B + C + D + 10E + 10F)dt - A$	
Attenuator (pots 1-6)	 Eo = K(A)	
Attenuator (pots 7 & 8)	 Eo = K(A)	
Voltage Divider (pots 7 & 8)	 Eo = K(A - B) + B	

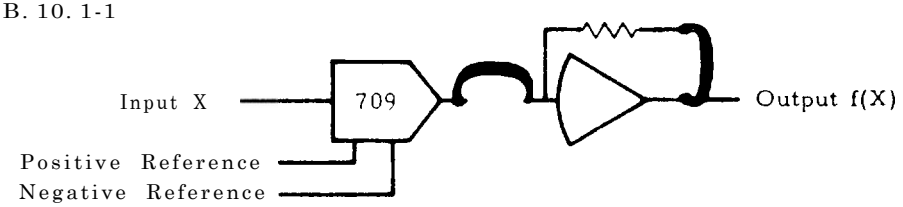
FUNCTION	OPERATION	PATCHING
Multiplier	Fundamental Multiplier Operation  Eo = -(X*Y)  Eo = -(A*B)	
Divider	 Eo = -(A/B) A > 0	
Squarer	 Eo = -A²	
Square Root	 Eo = -√A A < 0	

FUNCTION	OPERATION	PATCHING
Differentiator (amplifiers 1-4)	Fundamental Differentiator Operation  Eo = -RC*dEin/dt  Eo = -dA/dt NO SWITCH CONTROL PATCHING	
Track/Store (amplifiers 1-4)	 Eo' = -A when Q is a logic 0 Eo' = -A' when Q is a logic 1 A' is the stored value of A when Q switches from 0 to 1 Eo = A'(n-1) A'(n-1) is the previous value of A'	
SPDT Electronic Switch (amplifiers 1-4)	 Eo = -A when Q is a Logic "0" Eo = -B when Q is a Logic "1"	

B. 10. 1 THE MODEL 709 VARIABLE DIODE FUNCTION GENERATOR

The Model 709 VDFG is programmed as an input network. For operation, it must be connected to the summing junction of an operational amplifier. When the feedback of this amplifier is a resistor, such as shown in Fig. B. 10. 1-1, the VDFG function appears as its output.

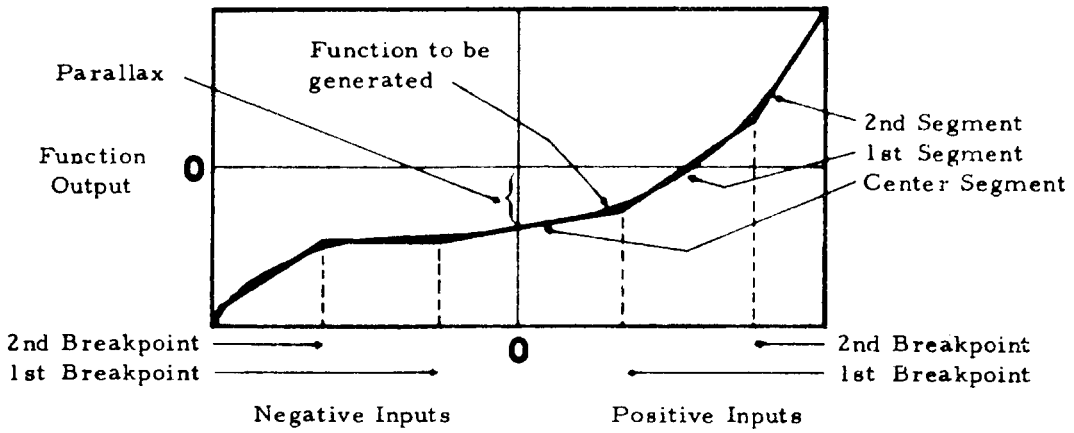
Fig. B. 10. 1-1



The following procedures may be used for setting functions:

1. Construct an output/input plot of the function to be set. The curve should be drawn on graph paper with full scale co-ordinates relating to computer reference. The best straight line approximation to the curve should then be determined. These straight lines will establish the breakpoint locations. Eleven segments are available with the 709 network. A center segment generates the function slope at the X axis origin. Five segments are located on either side of the origin. The intersection of the center segment with the first segment of the positive side is the first positive breakpoint. The intersection of the first and second segment is the second positive breakpoint, etc. Negative breakpoints are similarly numbered on the negative side of the origin. The intersection of the center segment with the Y axis establishes the parallax. For an example of the parallax, center slope and two positive and negative breakpoints, see Fig. B. 10. 1-2.

Fig. B. 10. 1-2



2. Connect computer reference to the "+" and "-" jacks found on the VDFG panel. Patch the VDFG to an amplifier as shown in Fig. B. 10. 1-1.

3. Connect a ramp that sweeps from negative to positive reference as the VDFG input.

4. Set up is easiest when the computer is in the repetitive operation mode and the function is displayed on an oscilloscope. Setting in the slow time mode may be desired, however, because of the increased accuracy offered by an XY plotter readout. In either case, display the VDFG amplifier output as a function of the input. The VDFG will then be set to duplicate the curve drawn in step 1 above.

5. Turn all the positive breakpoint adjustments to their clockwise stops. Turn all the negative breakpoint adjustments to their counterclockwise stops. All breakpoints will then be removed to their farthest position from the origin.

6. Turn the Parallax for the desired intersection at the Y axis.

7. Set the "CTR SLOPE" adjustment for the desired center segment slope.

8. Turn either the first negative or the first positive breakpoint adjustment to the desired first breakpoint location. Trim the first slope adjustment for the desired first segment slope. Repeat this procedure for all the breakpoint and slope adjustments. Always make adjustments in a sequence from the origin.

9. Replace the ramp with the desired program input.

Please note that the generated function, i.e. individual segment slopes, will vary proportionally with the amplifier feedback resistor. The range of individual segment slopes may, therefore, be increased by raising the value of this resistor. Or, slopes may be increased by placing a coefficient attenuator in series with the feedback resistor. In this case, the slope range is increased by the reciprocal of the potentiometer setting.

MODEL 771 TRANSFER FUNCTION SIMULATOR

GENERAL DESCRIPTION

The 771 provides an analog computer simulation of eight basic transfer functions. Each has three sets of parameters. The eight transfer functions and their associated parameter values are outlined in Table 1. The 771 output is the transfer function response to any patched analog input, such as a sine wave, square wave, pulse, etc. It also features a reset mode control to synchronize its use with repetitive operation analog computers or other similar systems.

OPERATING INSTRUCTIONS

power...The 771 has a self contained power supply for use with any 110 volt outlet.

Function Selection...A transfer function and its parameter set is determined by two Selector switches. To select transfer function $G_3(s)$ parameter set A, for example, turn the right hand switch to $G_3(s)$ and the left hand switch to "A."

Operation with External Equipment...A common ground connection is all that is needed to connect the 771 to an external system. The maximum voltage input is plus-minus 10 volts. The rated output voltage is plus-minus 10 volts. Output current is a minimum 5 mas at plus or minus 10 volts.

Mode Control...A logic 0 (0 or positive volts) patched to the "MODE CTL" jack will reset the transfer function to a zero output. The absence of patching or a logic 1 (-2 or more negative volts) will place the unit into a normal operating mode.

Operation with the GP-6 Analog Computer... For operation with the GP-6 analog computer, patch computer ground to the 771 "GND" jack. Patch the computer "OP" terminal to the 771 "MODE CTL" jack.

lime Constants...Transfer function time constants are given in Table 1 both in reference to the GP-6 program seconds and real time. The GP-6 program seconds are for the repetitive operation time scale.

Operation with Other Computers...The repetitive operation mode control operating levels should be checked. If a 0 or positive volt level is the computer's initial condition mode logic and a -2 to -15 volt level is the operate mode logic, then the computer's mode control bus may be connected to the 771 "MODE CTL" jack. Otherwise a level changer must be included as a buffer between the two units.

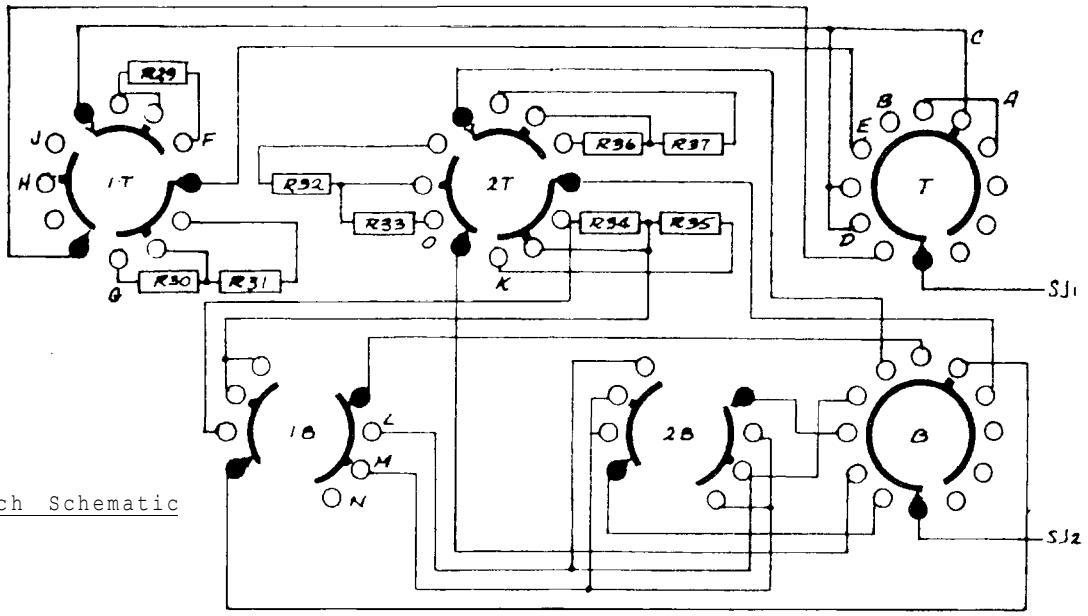
Circuit Description...Transfer functions are simulated through the application of two operational amplifiers and passive R-C networks. Each amplifier has a selection of eight networks. The two amplifiers operate in series. The transfer function selector switch has two poles that program the amplifiers by connecting a network to each of the summing junctions. An input thus passes through a network to amplifier 1; the output of amplifier 1 passes through a network to amplifier 2; the output of amplifier 2 is the transfer function output. The parameter selector switch alters a network's parameters but does not change its basic characteristics. Each of the two amplifiers have an electronic mode switch that reset outputs to zero upon a logic command.

Amplifier Balance... To balance amplifier 1, position the selector switch to $G_2(s)$. The amplifier is programmed as an integrator. In the repetitive operation mode, adjust potentiometer P1 until the output shows a minimum drift. To balance amplifier 2 position the selector switch to $G_3(s)$. Adjust P2 until a minimum output is observed.

TABLE 1

No.	Function	Sym.	Parameters A GP-6	A Actual	B GP-6	B Actual	C GP-6	C Actual	Units
$G_1(s)$	$\frac{1}{Ts + 1}$	T	1	.0025	.1	.00025	.01	.000025	sec.
$G_2(s)$	$\frac{K}{s(Ts + 1)}$	K T	10 1	10 .0025	10 .1	10 .00025	50 .1	50 .00025	 sec.
$G_3(s)$	$\frac{1}{s^2/Wn^2 + 2Ds/Wn + 1}$	D Wn	.2 10	.2 4000	.7 →	.7 →	1 →	1 →	 r/s
$G_4(s)$	$\frac{1}{(T_1s + 1)(T_2s + 1)}$	T_1 T_2	1 1	.0025 → .0025	→	→	→	→	sec. sec.
$G_5(s)$	$\frac{1}{(Ts + 1)(s^2/Wn^2 + 2Ds/Wn + 1)}$	T D Wn	1 .2 10	.0025 .2 → 4000 →	.1	.00025	.01	.000025	sec. r/s
$G_6(s)$	$\frac{K}{s(s^2/Wn^2 + 2Ds/Wn + 1)}$	K D Wn	10 .7 10	10 .7 4000 →	10 .2	10 .2	50 .7	50 .7	 r/s
$G_7(s)$	$\frac{K}{s(T_1s + 1)(T_2s + 1)}$	K T_1 T_2	10 1 1	10 .0025 → .0025	10 → .2	10 → .00050	50 → .1	50 → .00025	 sec. sec.
$G_8(s)$	$\frac{Ts + 1}{s^2/Wn^2 + 2Ds/Wn + 1}$	T D Wn	1 .7 10	.0025 .7 4000 →	.1 .7	.00025 .7	.01 .2	.000025 .2 →	sec. r/s

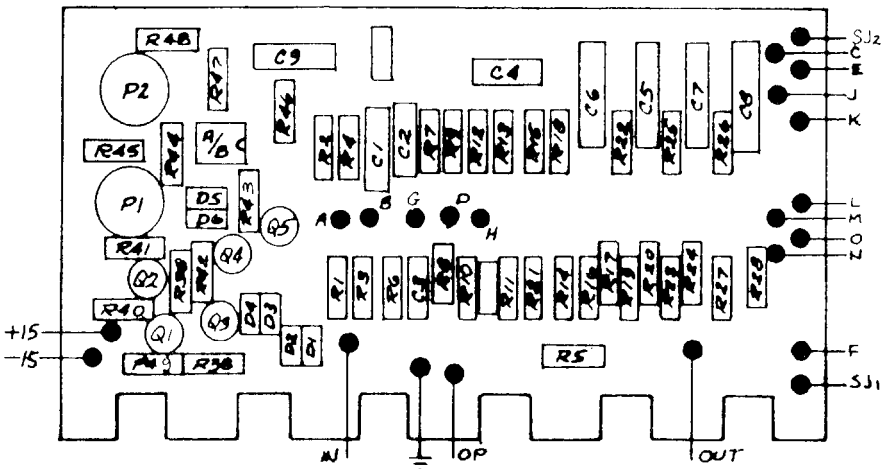
771 TRANSFER FUNCTION SIMULATOR

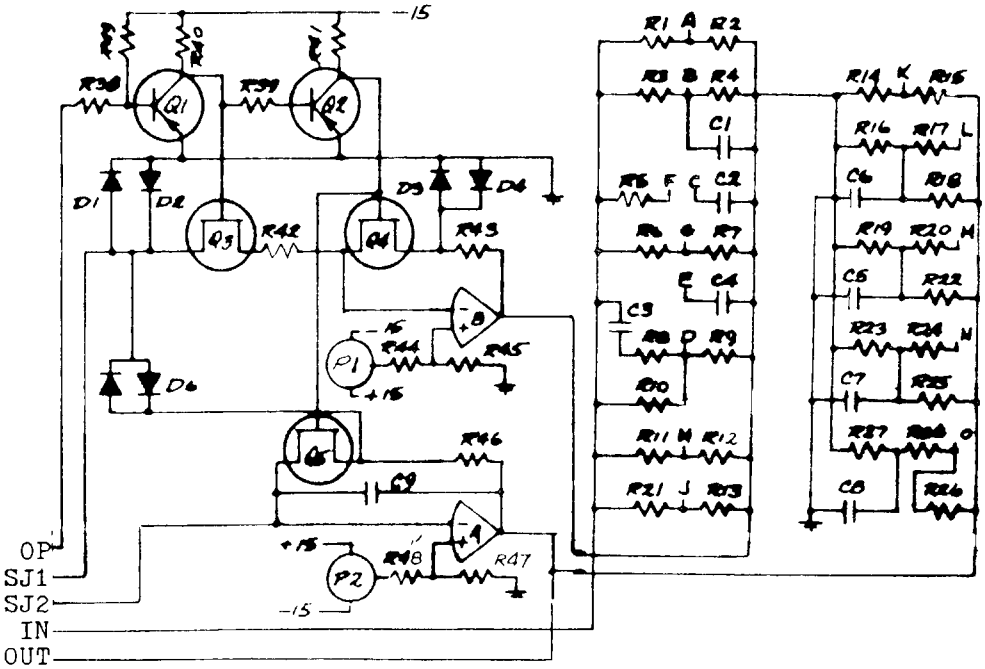


Selector Switch Schematic

Parts List

R8	100	
R17	3.92	K*
R43,R45,R46,R47	4.7	K
R6,R7,(R14,R15)	4.99	K*
(R13,R21)	5.49	K*
(R23,R25)	6.04	K*
(R19,R22)	8.87	K*
R42	10	K
R5,(R1,R2)	10	K*
(R16,R18)	12.1	K*
R38,R40,R41	15	K
R30,R35	22.6	K*
(R27,R28)R33,R36	24.9	K*
R20	28.7	K*
R29	40.7	K*
R39,R49	47	K
R24	47.5	K*
(R3,R4)R26	49.9	K*
(R11,R12)	54.9	K*
R32,R37	200	K*
R31,R34	221	K*
R44,R48	1	M
C1,C5,C7,C8	.047	u
C2,C3,C4,C9	.0047	u
C6	.22	u
P1,P2	50	K
Q1,Q2	2N5138	
Q3,Q4,Q5	2N5163	
Amps A,B	1458	



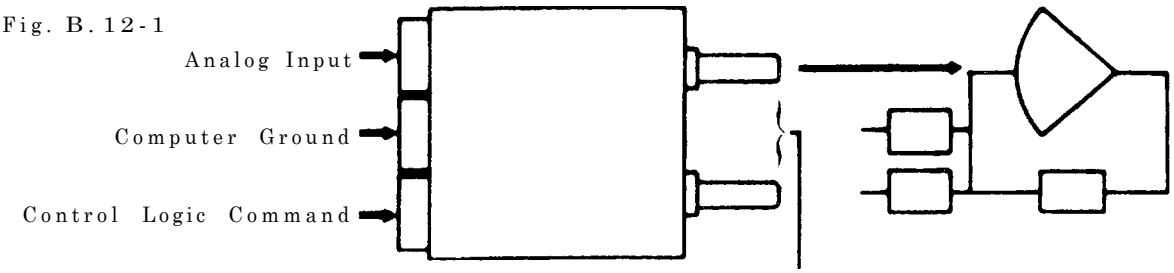


Circuit Schematic

B. 12 SERIES 9300 D/A ELECTRONIC SWITCH MODULES

The 9300 D/A Switch Modules are furnished ready for operation with analog computer amplifiers where the summing junction and output terminations are standard banana jacks having 3/4" hole spacing. Connections are identified by the schematic shown on the switch module. The banana plug connects the module to an amplifier's patch panel summing junction. The analog input variable that is to be switched is patched to the module's input resistor jack. Computer ground must be connected to complete an internal circuit. The logic command to control the switch is patched to the module's switch control input jack.

Fig. B. 12-1



Functions as a shorting plug for Modules 9305 & 9307

With a logic "0" (ground potential) control command, the module performs as a normal input resistor. With a logic "1" command, the input to the summing junction is completely shut off.

The shut-off control voltage varies with the switch module. Models 9302 and 9305 shut off with negative logic. Model 9307 shuts off with positive logic. The voltage level ranges from a minimum of about 3 volts to a maximum 10 volts

A selection of switch modules are available for convenient operation with various analog computer models. These are described as follows:

B. 12. 1 M odel 9302

The Model 9302 is furnished for operation with the Comdyna GP-6 analog computer. It provides a standard gain 1 input, as referenced to the GP-6 patch panel. As shown on the module's schematic, only one of the banana plugs is the active summing junction. The other plug is isolated from any circuit. In patching the 9302 module, the plugs are usually connected to the amplifier's summing junction and output jacks.

B. 12.2 Models 9305 and 9307

M odels 9305 and 9307 are furnished as a 100K ohm input resistor. The two banana plugs are common and may be used as a shorting plug when connected to the patch panel amplifier summing junction.

B. 12. 3 Model 9390 Comparator Feedback Network

The 9390 bottle plug is a feedback element for programming a patch panel amplifier into a comparator. When connected as shown in Fig. B. 12-2, the amplifier will output a proper logic level to control the D/A Switch Modules. The amplifier will produce negative logic control with the plug connected to the summing junction and the jack patched to the output. Positive logic control results when the plug is connected to the output and the jack is patched to the summing junction.

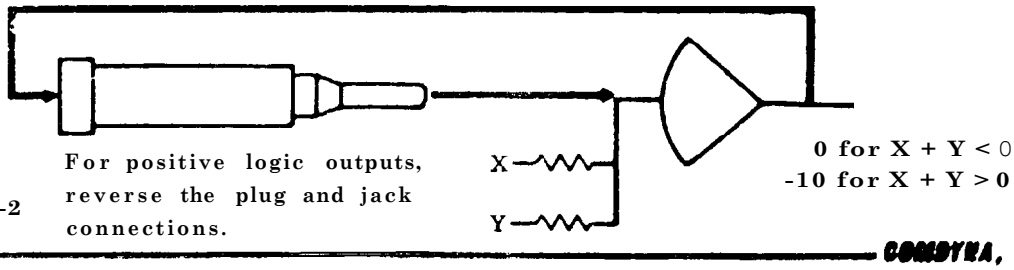


Fig. B. 12-2 **For positive logic outputs, reverse the plug and jack connections.**

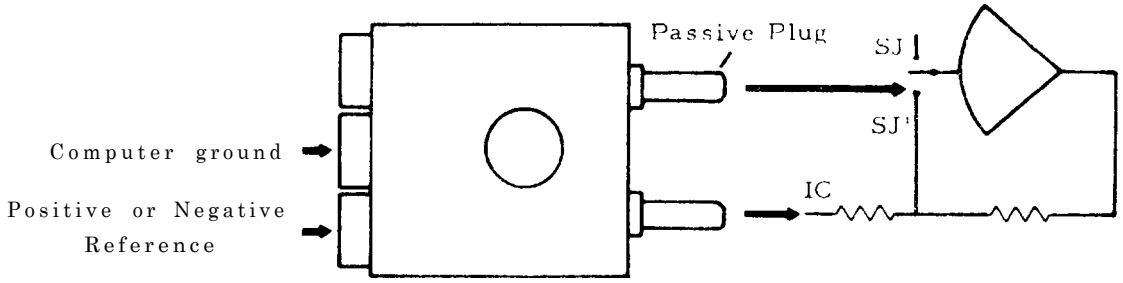
B. 12 BANANA PLUG MODULES

B. 12. 5 Model 9447 Coefficient Potentiometer

The 9447 Module provides a single 5K ohm potentiometer furnished in an ungrounded configuration. It is arranged for convenient use in setting integrator initial conditions with Comdyna analog computers. The module may also he used as a general attenuator, variable resistor or special purpose potentiometer.

For use in setting integrator initial conditions, connect the module as shown in Figure 12-5. Place the computer into the initial condition mode. Adjust the potentiometer until the desired initial condition appears at the amplifier output.

Fig. 12-5

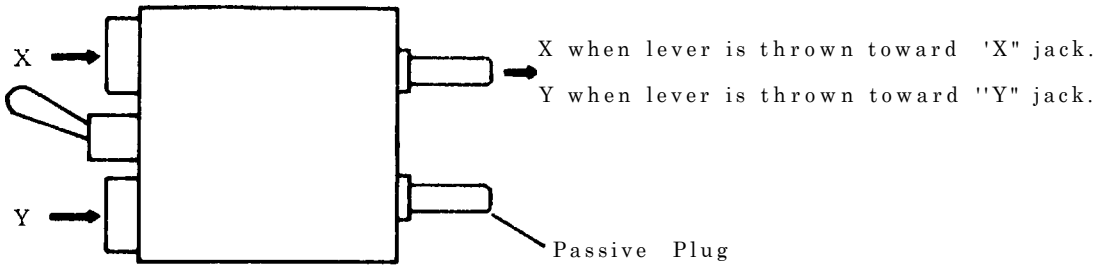


The schematic that appears on the module may be used as a guide for other applications.

B. 12.4 Model 9408 Function Switch

The 9408 Module provides a single pole, double throw mechanical switch for use with any patch panel banana jack. It may be used to switch amplifier inputs or outputs, logic control levels, reference, etc. Switch operation is shown in Figure 12-4.

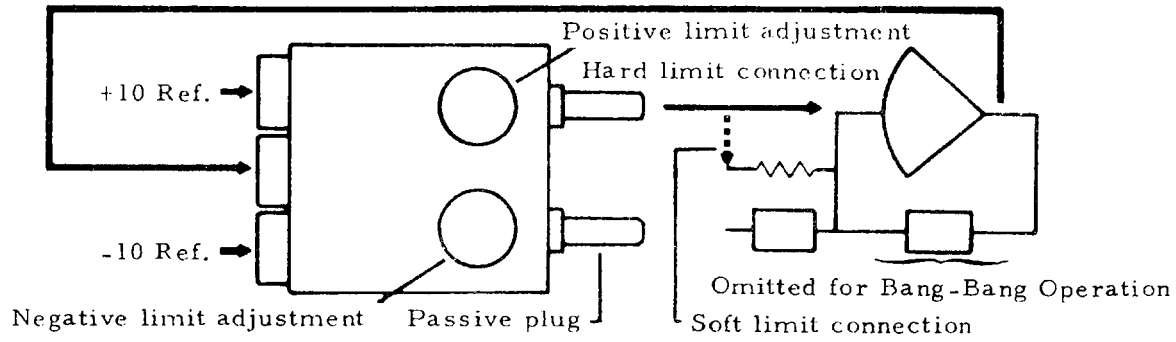
Fig. 12-4



B. 12.6 Model 9517 Limiter

The 9517 Module is an active network for limiting the output of an analog computer operational amplifier. It may be used as the amplifier's sole feedback for a "Bang-Bang" function, or it may be used in parallel with an other element for a hard function limit. It may also be placed in series with a feedback resistor for a soft function limit. The 9517 Module plugs into a standard banana jack patch panel and is programmed as shown in Figure 12-5.

Fig. 12-5

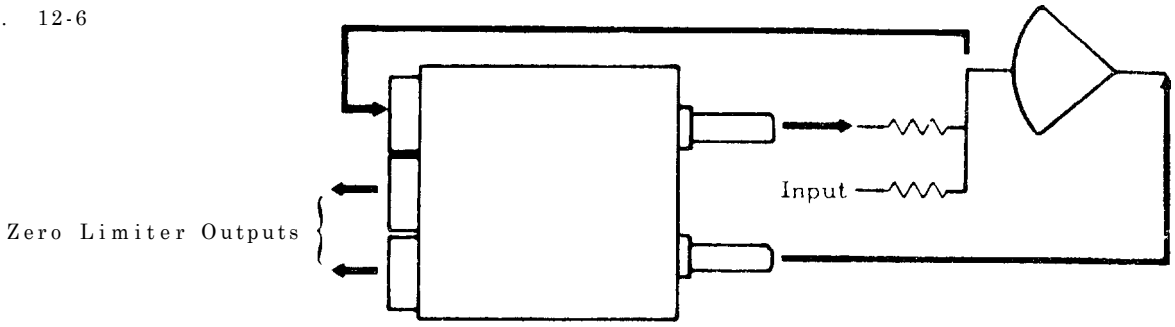


To set the positive and negative output limits, connect the 9517 Limiter as shown in Fig. 12-5. Input -10 Reference to an amplifier input resistor. Adjust the *positive* limit potentiometer until the desired limit amplitude is observed at the amplifier output. Repeat the operation for the negative limit, replacing the -10 Reference with a +10 Reference to the input resistor.

B. 12. 7 Model 9528 Zero Limiter

The 9528 Module provides an amplifier feedback to limit the output to a positive operation only Programming is as shown in Figure 12-6. (Please note that the internal network may not be the same as the schematic appearing on the module.)

Fig. 12-6

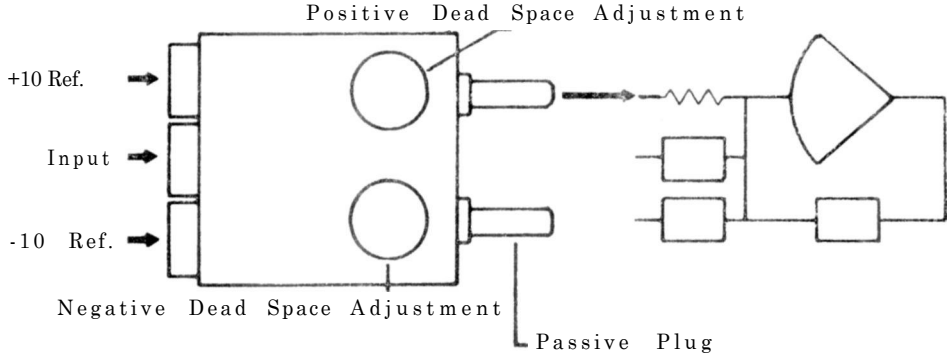


The Zero Limiter output appears at the module jacks. The normal amplifier output should not In- used

13. 12.8 Model 9520 Dead Space

The 9520 Module provides dead space to the input of an operational amplifier. It is plugged to a normal patch panel input resistor as shown in Figure 12-7

Fig. 12-7

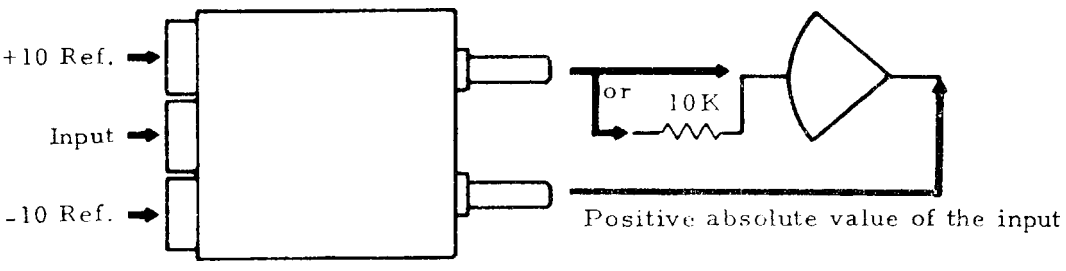


To set the dead space, patch a feedback resistor for a gain 1 or 10 input configuration Apply a positive input equal to the positive dead space amplitude. Adjust the positive dead space potentiometer until an output is noticed. Repeat the procedure for negative dead space with a negative input equal to the desired negative dead space amplitude. The feedback resistor may then be removed and replaced with the desired feedback element.

B. 12. 9 Model 9560 Absolute. Value

The 9560 Module is an active network to generate the positive absolute value of both positive and negative inputs. It contains an internal inverter amplifier to provide this capability. It is plugged to a patch panel and programmed as shown in Figure 12-8.

Fig. 12-8



4. GP-6 CIRCUIT DIAGRAMS

Figure 5-1 is a layout of GP-6 assemblies. Please refer to Section 2 for a wiring schematic and description of system operating functions. Refer to individual drawings for information covering assemblies.

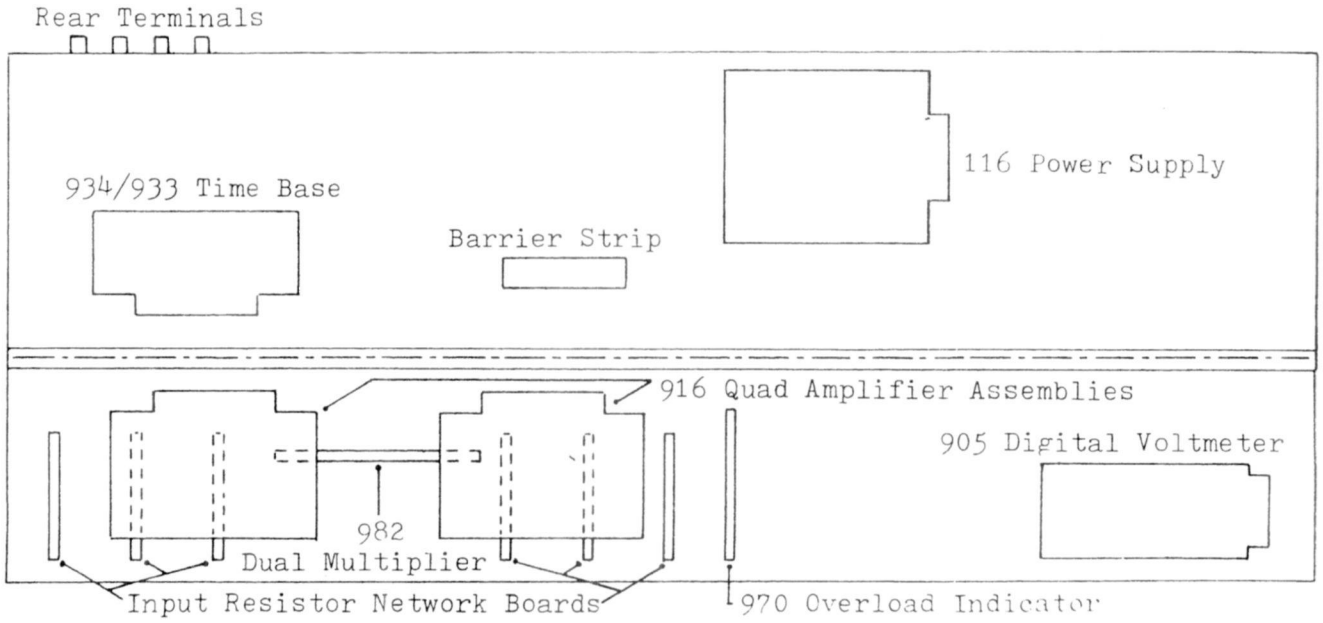


Figure 5.1

Input summing resistors for integrator and summer amplifiers are located on the Resistor Network Boards. Resistors are 5.00K and 50.0K ohms, metal film, 0.1%.

Color coding of power wiring is: +15V -Red; -15V -White; -10V -Yellow; +10V -Orange; Ground -Black.

The following is a parts list for the GP-6 system. Component parts lists are found with individual assembly drawings.

Description	Manufacturer	Part Number
Patch panel jacks	E.F. Johnson	108-09..-001
Rear terminals	E.F. Johnson	111-01..-001
Y/Pot Address switch	Centralab	PA-1005
X Address switch	Centralab	PA-1001
Mode Selector switch	Centralab	PA-1029
Mode Control switch	Switchcraft	65041K-206
Pilot light	Leecraft	36EN2111
Overload indicator	Leecraft	45RNG 3-2111
Coefficient potentiometers	C.T.S.	VA 45D
Compute Time/Power switch	C.T.S.	GC-45-8D
AC power receptacle	Tower Mfg.	1061-2
Fuzeholder	Littlefuze	372001
Fuze, AC power	Littlefuze	8 AG 1 amp.
Amp. & Timer board connectors	Amphenol	143-022-01
Power supply connector	Amphenol	143-012-01
DVM & Multiplier connectors	Amphenol	143-010-01
Barrier strip	TRW	10-164
Barrier strip jumpers	TRW	140-J-1

911-2 QUAD AMPLIFIER ASSEMBLY

The 911 board provides two single input, high gain operational amplifiers and two high gain operational amplifiers with electronic switch/integrator networks.

Amplifiers A and D are the single input amplifiers. The patch panel summing junctions are connected directly to the inverting bases. Balance is obtained by biasing the summing junctions with potentiometers P4 and P3 through voltage dividers R15 and R15 to the non-inverting bases. Back-to-back diodes D1 and D2 offer protection by limiting summing junction potential. Capacitors C1 minimize peaking and thereby increase stability.

Amplifiers B and C are amplifiers with electronic switch/integrator networks. The electronic switches create two summing junctions, SJ and SJ'. When the switch control input (OP) is a logic 0 summing junction SJ' is active; with a logic 1 summing junction SJ is active.

The integrating capacitors are connected to the SJ summing junctions thus an integrator is programmed by patching an amplifier output to a capacitor input. There are two capacitor inputs (B and .1B) that offer a 10:1 time scale selection. The Time Scale Relay provides for the time scale change (400:1) required for slow time and repetitive operation. Where the repetitive operation feature is provided the repetitive operation capacitors are connected directly to the summing junction. Slow time capacitors parallel the repetitive operation capacitors when the relay is energized. (Application of -10 volts to the Relay input energizes the relay.)

Signal switching is performed by N-channel FET transistors Q6 through Q8. Transistors Q1 through Q5 are the FET switch drivers. Q6 is the Hold switch. (Q6 has an on resistance of less than 30 ohms to minimize summing errors.) Voltage divider resistors R14 and R7 are selected so that when OP is greater than -3 volts Q1 conducts and Q6 is on; when OP is less than -1 volt Q6 is shut off. Q7 is the shunt switch; Q8 is the SJ scries switch and Q9 is the SJ' series switch. Table 5-1 shows the switch states for the OP logic inputs. FET transistors conduct with zero gate voltage and shut off with approximately -7 volts gate voltage. Diodes D1 and D2 limit the potentials of SJ and SJ' and therefore limit the FET source to drain potential.

High impedance FET inputs are provided with dual, matched FET transistors Q10. The drain of one FET is connected to the inverting base while the other is connected to the non-inverting base. The FET gates are the amplifier inputs. Balance is obtained by biasing the non-inverting bases with potentiometers P1 and P2 through voltage divider resistors R15 and R16.

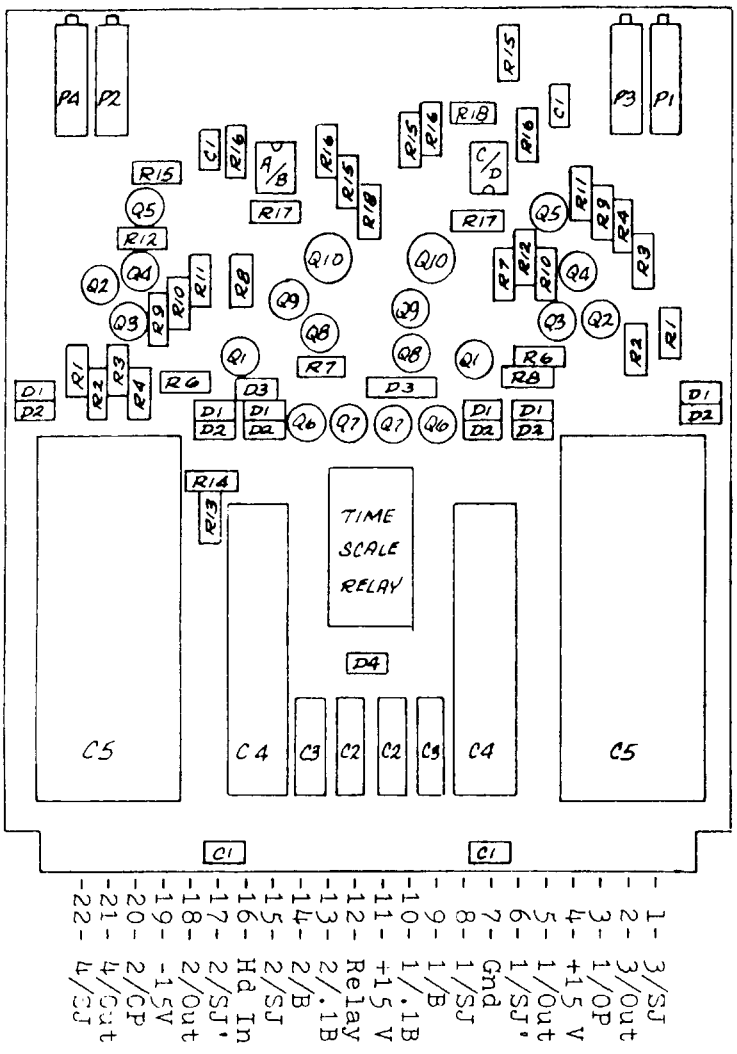
Capacitor C1 offers peaking compensation for the SJ summing junction. Similar compensation for the SJ' summing junction is found on the input resistor network boards.

BALANCING

To balance amplifiers A and D patch resistor feedbacks and adjust potentiometers P3 and P4 until the amplifier outputs are zero potential.

Amplifiers B and C should be balanced as integrators. Program the amplifiers as integrators and place the GP-6 into the repetitive operation mode. Adjust potentiometers P1 and P2 until the amplifier outputs show a zero integration condition.

Assembly Diagram



Parts List

R1, R14	27 K
R2-R4, R7, R9, R11	15 K
R6, R10, R12	47 K
R8	330 K
R13	2.2 K
R15	4.7 K
R16	1 M
R17, R18	100 K
C1	15 uuf
C2	.005 uf*
C3	.05 uf*
C4	2 uf*
C5	20 uf*
Q1-Q5	2N5138
Q6	2N4091
Q7-Q9	2N5163
Q10	E411
P1-P4	50 K
Amplifiers	1458
Relay	4A,24V

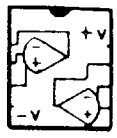
*precision integrating capacitors

Table 5-1

OP Input	Q6	Q7	Q8	Q9
OP > 0	OFF	ON	OFF	ON
-1V > OP > -3V	OFF	OFF	ON	OFF
OP < -5V	ON	ON	OFF	ON

Note: When Hold Inhibit <-1V, Q6 remains ON.

1458 amplifier



Circuit Schematic

116-2 POWER SUPPLY

The 116-2 Power Supply provides plus and minus 15 volts, plus and minus 10 volts, Vcc (plus 5 volts) and B+ (plus 200 volts) power.

Plus and minus 15 volts are regulated supplies with 150 ma each current capacity. Plus and minus 10 volts is a precision tracking reference. Vcc is a regulated logic supply. B+ is an unregulated neon display supply.

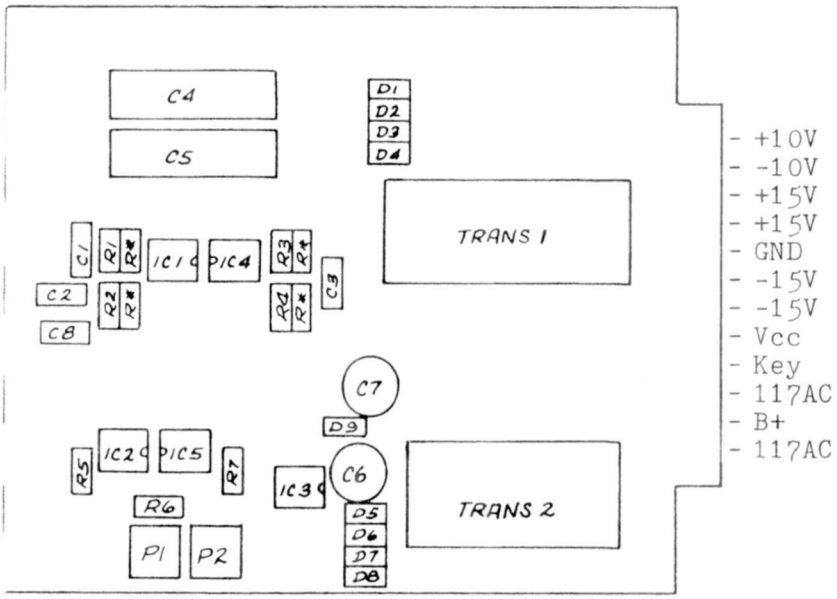
The regulated supplies use the 78MGT and 79MTG programmable regulators. The 78 is a positive regulator; the 79 is a negative regulator. IC 1 generates plus 15 volts with programming resistors R1 and R2. IC 4 similarly generates minus 15 volts with resistors R3 and R4. IC 3 requires only a shorting connection to generate plus 5 volts.

IC's 2 and 5 are arranged in a tracking configuration to generate precision reference. Negative 10 volts reference is fixed; positive 10 volts reference tracks.

Reference Adjustments

Potentiometer P2 adjusts the value of negative 10 volts. Potentiometer should he adjusted so that the sum of negative and positive references equals zero.

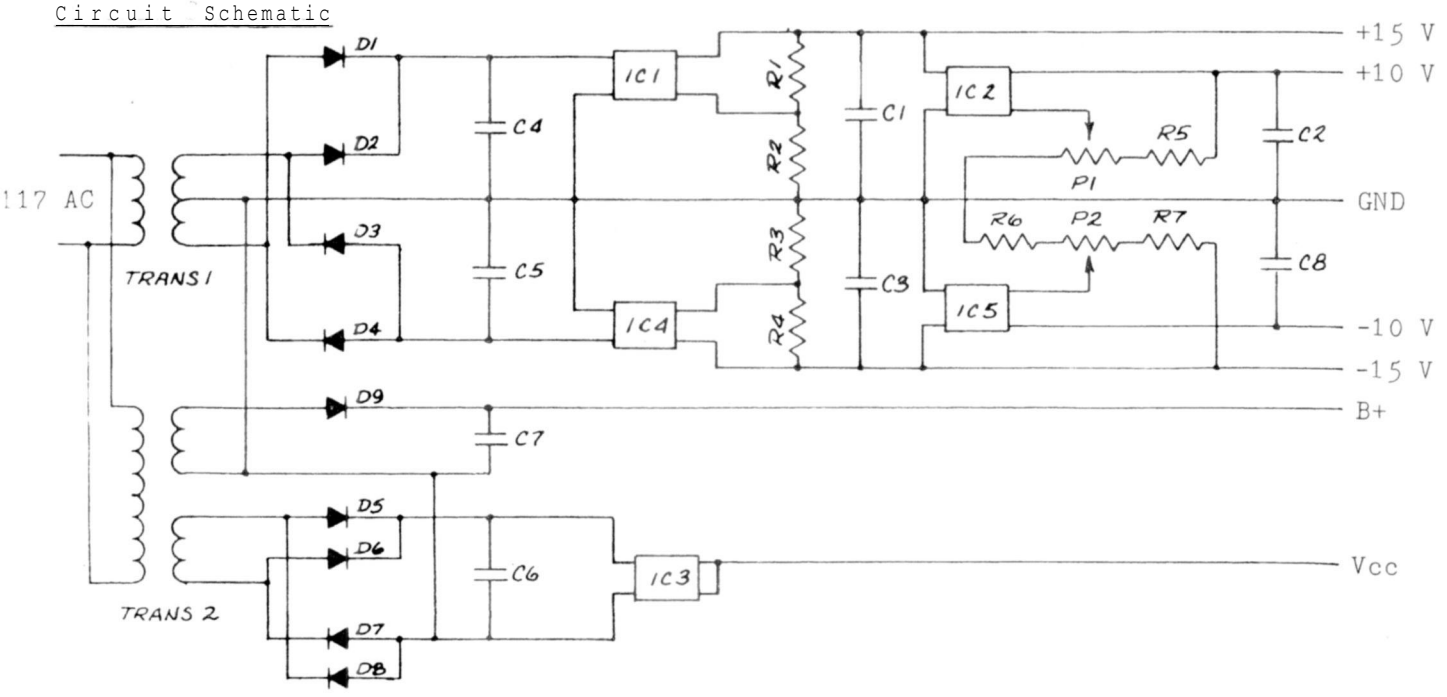
Assembly Drawing



Parts List

R1,R3	12 K
R2	4.7 K
R4	2.2 K
R5	4.99 K
R6	6.98 K
R7	7.05 K
R*	Trimming resistors
C1,C2	.1 uf tant.
C3,C8	1 uf tant.
C4,C5,C6	500 uf 25V
C7	12 uf 250V
D1 thru D8	1N4001
D9	1N4007
IC1,IC2,IC3	78MTGFC
IC4,IC5	79MTGFC
P1	50 ohm cermet
P2	500 ohm cermet
TRANS 1	28V CT/300ma
TRANS 2	125V/15ma, 6.3V/600ma

Circuit Schematic



933-2 TIME BASE

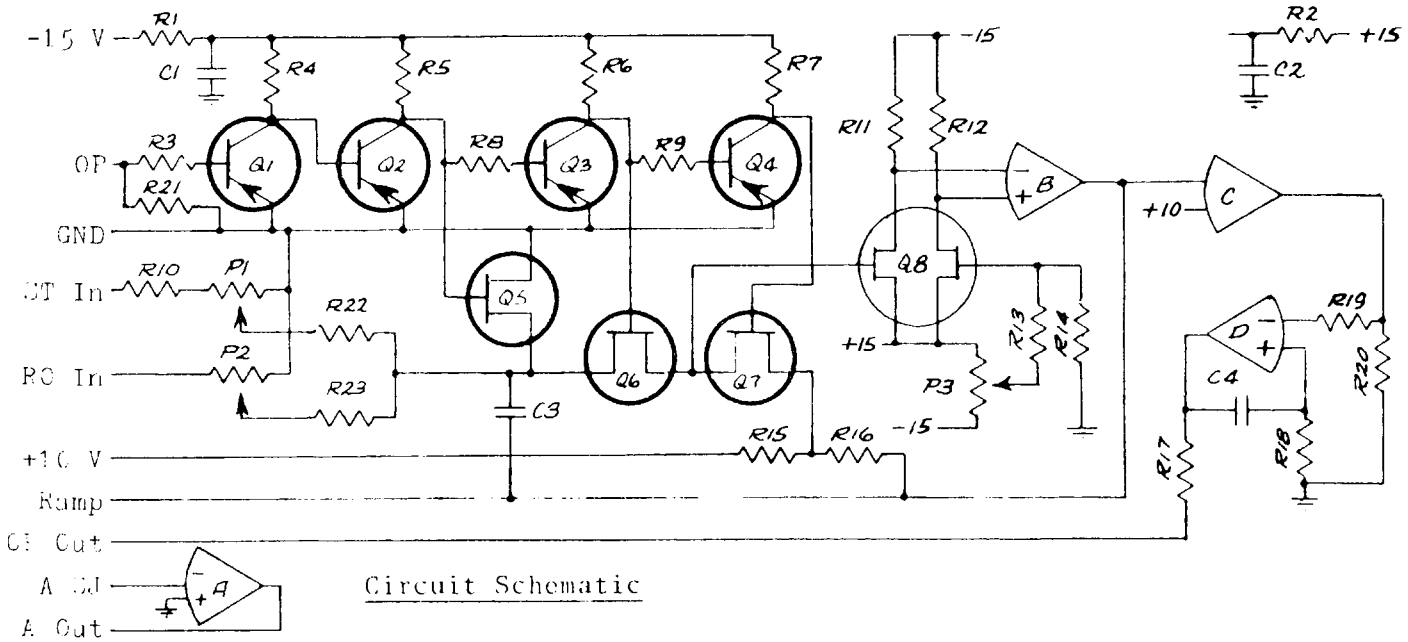
The 933 assembly provides a time base for both slow time and repetitive operation. The slow time base is used for the X input to an XY recorder; the repetitive operation time base is used for the horizontal input to a display oscilloscope. A monostable reset feature is provided for the repetitive mode control logic.

The time base integrator (amplifier B) employs a circuit similar to that furnished for the patch panel integrators. Please refer to the 911 Quad Amplifier drawing for a detailed description of the integrator operation.

An external logic command (OP) controls the time base integrator. A logic 0 (ground or positive voltage) places the integrator into an initial condition state; a logic 1 (less than -1 volt) places the integrator into an operate condition. When used with the GP-6 the slow time base is controlled by the manual push button mode control switches; the repetitive operation time base is controlled by the repetitive mode control logic.

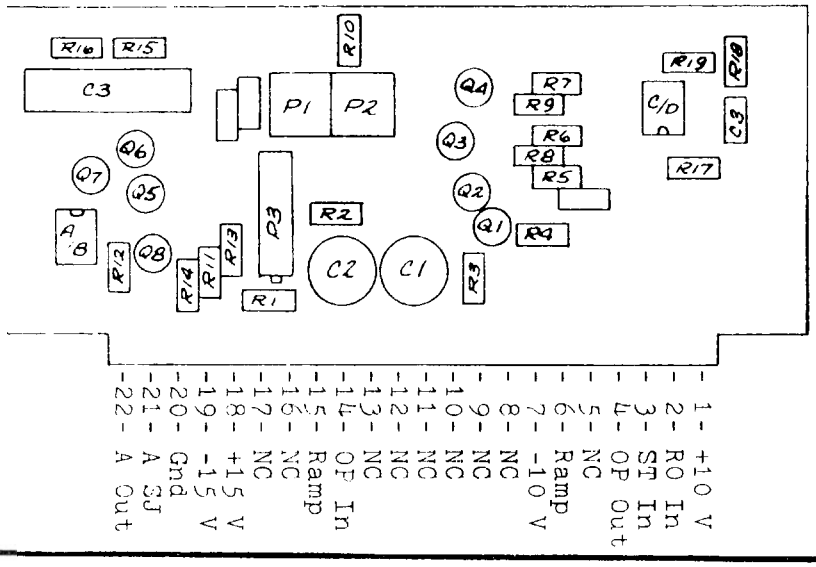
Two separate inputs enable one integrator to be used for slow time and high speed repetitive operation. In both cases capacitor C3 is the integrator feedback.

The repetitive mode control monostable is generated with amplifiers C and D. Amplifier C compares the time base with +10 volts. When the time base exceeds +10 volts the output switches from plus to minus saturation. Amplifier D is then switched to plus saturation. Capacitor C4 pulls the non-inverting base to a positive potential until it is discharged to ground potential. Reset of the time base and patch panel integrators occurs during this period. The output of amplifier C then returns to negative saturation.



Circuit Schematic

Assembly Drawing



Parts List

R1,R2	100 ohm
R3,R8,R9,R19	47 K
R4 thru R7	15 K
R10,R11,R12	100 K
R13,R22	1 M
R14,R20	4.7 K
R15,R16	10 K*
R17	1 K
R18	330 K
R21	27 K
P1,P2,P3	50 K
C1,C2	25 ufd
C3	1 ufd
C4	.02 ufd
Q1 thru Q4	2N5138
Q5 thru Q7	2N5163
Q8	E411
Amps. A thru D	1458

*Matched pair

Capacitors C1 and C2 and resistors R1 and R2 decouple amplifiers C and I) to eliminate power supply disturbance.

Amplifier A is the Compute Time Period amplifier. (See paragraph 2.3.4 for an operating description.)

Adjustments

1. The time base integrator is balanced in the operate mode with a zero input. (It is noted that the GE-6 slow time push button mode control removes the time base input when the "IID" button is depressed. The hold logic (-3 volts) places the time base integrator into an operate mode.) To balance the time base integrator: 1. Monitor the time base output with the digital voltmeter or null meter. 2. Allow the time base to run until the output is approximately zero. 3. Depress the "HD" push button. 4. Adjust potentiometer E3 until zero drift is observed.

2. Slow time and repetitive operation time base rates are adjusted with potentiometers P1 and P2. Both are adjusted to match patch panel integrator time constants.
   2.1 Program a patch panel amplifier as an integrator. Apply positive reference as an initial condition. Patch negative reference to a coefficient potentiometer and patch the wiper to a gain 1 input. Set the potentiometer to a setting of .200. The integrator will then sweep from negative to positive reference in a 10 second period.
   2.2 For the slow time base adjustment observe (with an XY recorder or oscilloscope) the slow time output of the above integrator as a function of the time base. Adjust potentiometer P1 until the function passes through the display's positive reference-positive reference coordinate.
   2.3 For the repetitive operation time base adjustment repeat the above procedures for the repetitive operation mode. Adjust potentiometer P2 until the oscilloscope trace passes through the positive reference-positive reference coordinate point.

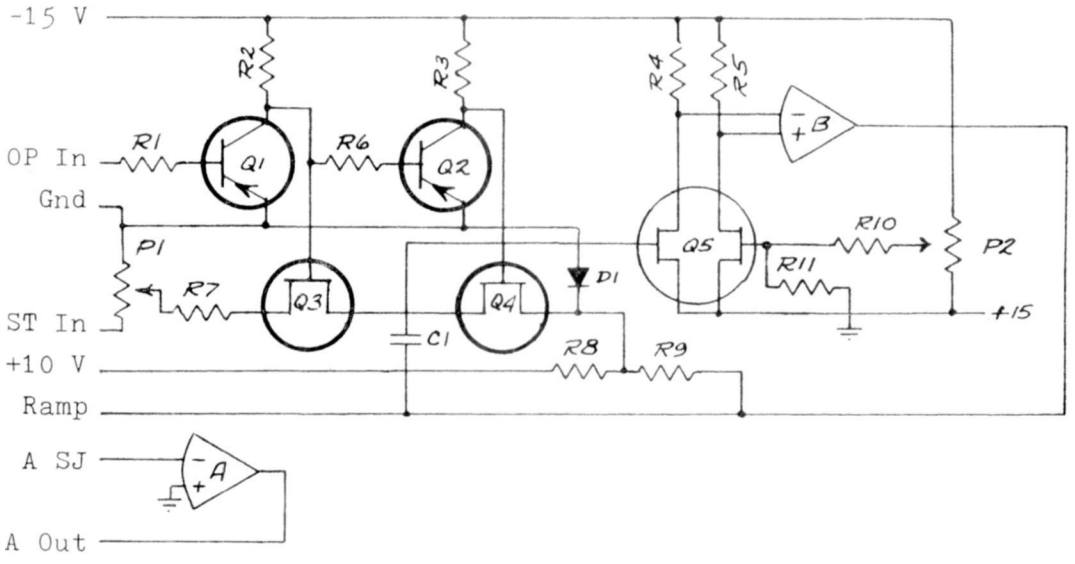
934 TIME BASE

The 934 assembly provides a slow time base only and does not have the repetitive operation feature. Like the 933 unit the integrator employs a dual FET (Q5) input. Mode switching is different. Capacitor C1 is a permanent feedback for amplifier B. In the operate state the input FET (Q3) conducts and the initial condition FET (Q4) is shut off. In the initial condition mode the reverse occurs.

The function of amplifier A is identical to the 933 assembly.

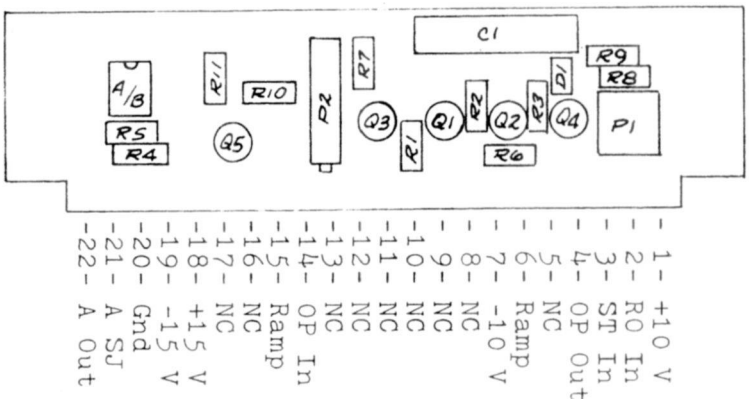
Balancing of integrator B and adjustment of the time base rate follow the same procedures used for the 933 Time Base.

Circuit Schematic



934 Time Base (Continued)

Assembly Drawing



Parts List

R1,R6	47 K
R2,R3	15 K
R4,R5	100 K
R7,R10	1 M
R8,R9	10 K*
R11	4.7 K
P1,P2	50 K
C1	1 ufd
D1	1N4148
Q1,Q2	2N5138
Q3,Q4	2N5163
Q5	E411
Amps. A & B	1458

*Matched pair

970-1 OVERLOAD INDICATOR

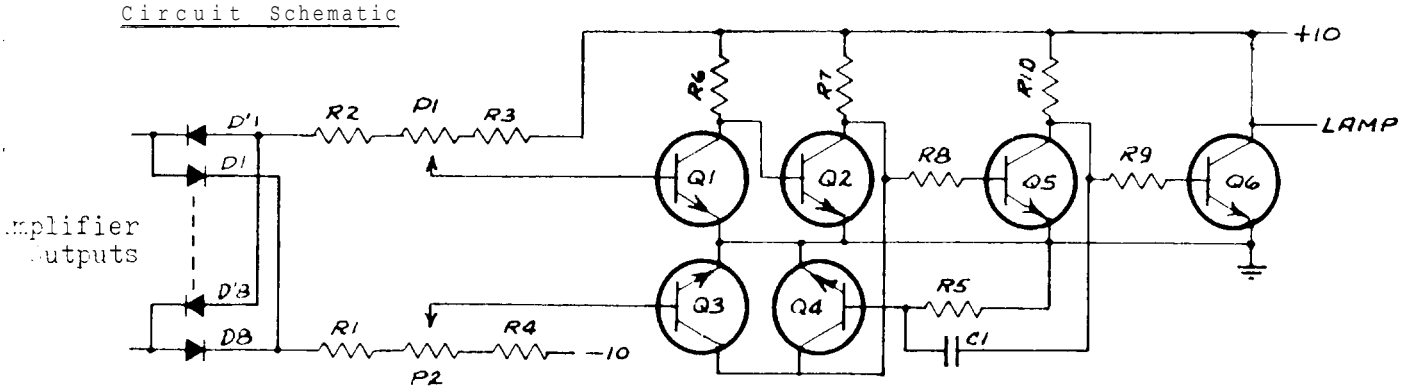
The 970-1 Overload Indicator compares eight amplifier outputs with positive and negative 10 volts reference. When any output exceeds reference a lamp driver conducts.

When a negative overload occurs Q1 shuts off and Q2 conducts. When a positive overload occurs Q3 is turned on, pulling Q2 to an on condition. Positive 15 volts through an incandescent lamp is pulled to ground when Q6 conducts. Resistor R5, capacitor C1 and Q4 provide a temporary latch so that momentary overload outputs are observed by the lamp indicator.

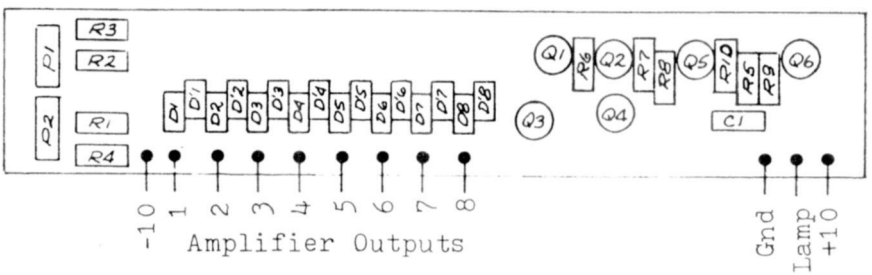
Adjustments

Apply a +10.5 volt level to any amplifier output. (10.5 volts provides a .5 volt overrange.) Adjust potentiometer P2 until the lamp indicator turns on. Apply a -10.5 volt level and adjust P1.

Circuit Schematic



Assembly Drawing



Parts List

R1 thru R4,R6,R7,R10	15 K
R8,R9	4.7 K
R5	27 K
C1	6.8 ufd
P1,P2	5 K
Q1 thru Q6	2N5132
Diodes	1N4148

982-1 DUAL MULTIPLIER NETWORK

The 982 assembly provides two independent multiplier networks that when used with an external operational amplifier can be programmed as a multiplier, divider, squarer and square root extractor.

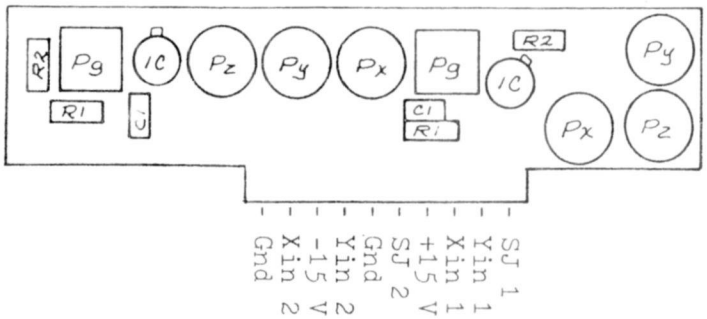
Two inputs (Xin and Yin) are multiplied by integrated circuit IC to produce a voltage output proportional to the product X*Y. The voltage output is converted to a current source by resistor R1. The current source "SJ" is applied to the summing junction of an operational amplifier. The unit is scaled so that when programmed as a multiplier with full scale 10 volt X and Y inputs and a 50 K ohm amplifier feedback, the multiplier output is 10 volts.

Adjustments

Each network is originally adjusted at the factory. The networks should, however, be checked and readjusted, if necessary, during the initial checkout. Thereafter the networks should be periodically checked to assure their most accurate operation. About 10 - 20 minutes should be allowed for warm-up before adjusting or checking.

Adjustment consists of zero offset balancing and a trim for gain and linearity. The suggested procedures for adjustment are as follows:

1. Program the network as a multiplier with a standard gain 1 (50 K ohm) feedback.
2. With inputs X and Y patched to ground adjust potentiometer Pz for a zero output.
3. Program an integrator to sweep from minus to plus 10 volts reference. (for convenience make all adjustments in the repetitive operation mode.) Display the multiplier output vs. the ramp. Patch the ramp to the Y input; the X input should remain patched to ground. Adjust potentiometer Px until a best zero curve is obtained.
4. Reverse the X and Y inputs. Adjust potentiometer Py until a best zero curve is obtained.
5. Readjust Pz if necessary.
6. Patch Reference to the X input and the ramp to the Y input. Sum the multiplier output with the correct polarity of the ramp so that an error curve is displayed. Adjust potentiometer Pg until a best error curve is obtained. Reverse the X and Y inputs and check the error curve. Check the error curve with the opposite polarity Reference for both combinations of inputs. Trim potentiometer Pg until the best error curves for all four combinations of inputs are obtained..

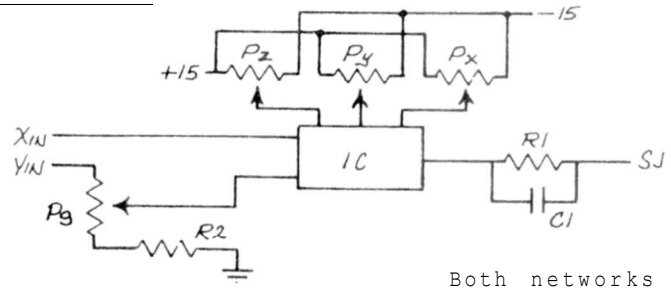


Assembly Drawing

Parts List

R1	49.9 K
R2	10 K
C1	33 pf
Pg	5 K
Pz,Px,Py	20 K
IC	8013 Intersil

Circuit Schematic



Both networks have identical circuits.

905 DIGITAL VOLTMETER

The 905 assembly is a digital voltmeter that functions as a ratiometer of input voltages to computer reference. The full scale 1.000 reading is a unity ratio of the input to the reference value. For normal operation the 1.000 reading is equivalent to 10.00 volts.

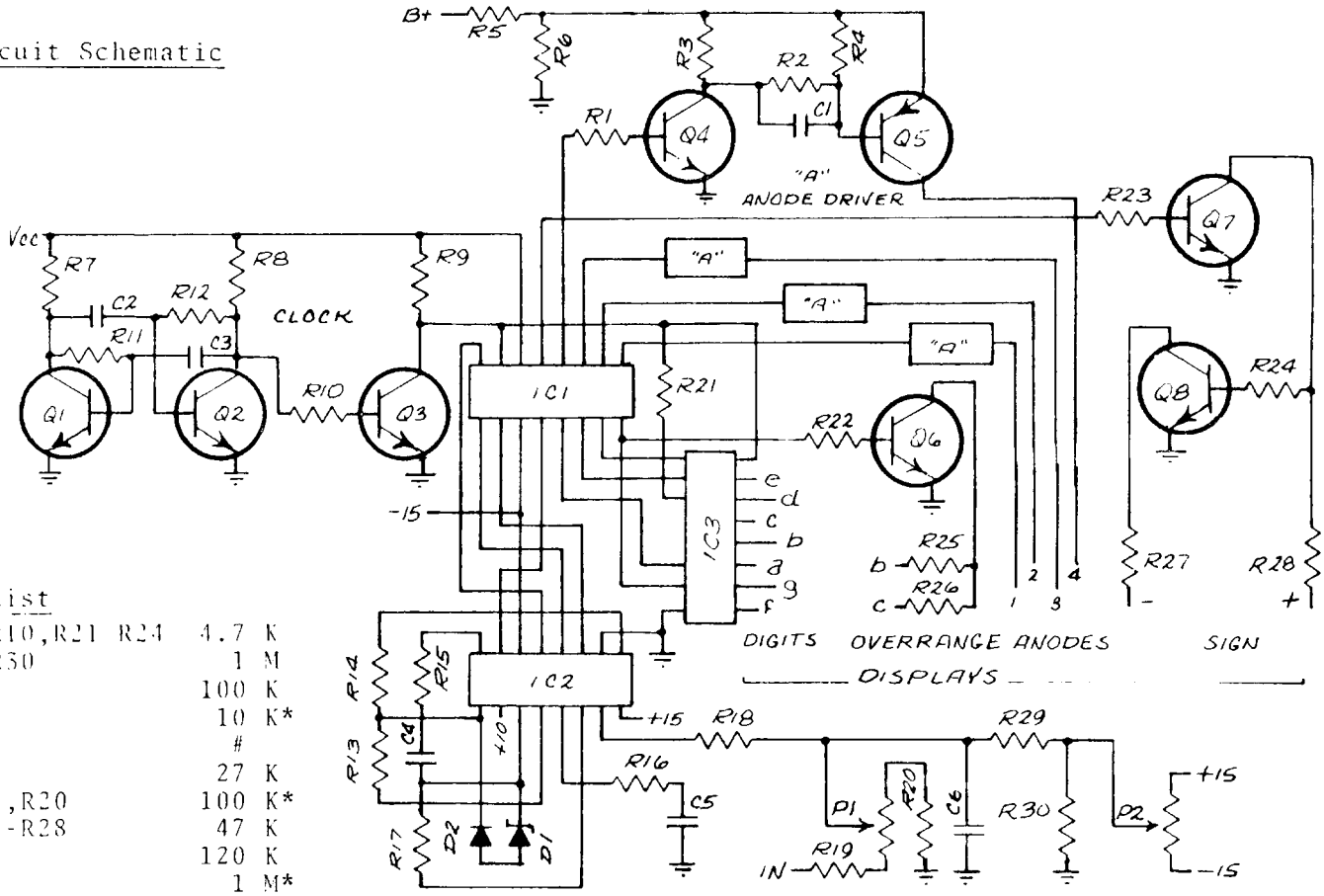
The Siliconix LD 110/LD 111 converter set provides all analog and logic functions. for a detailed description of the internal functions it is suggested that the LD 110/ LD 111 application data sheet be obtained from Siliconix, Inc. The LD 110 (IC 1) provides multiplexed logic outputs. Q4 & Q5 are anode drivers for the three display digits; IC 3 is the decoder driver for the cathode segments. Q6 is the overrange driver. Q7 and Q8 are polarity indicator drivers. Q1 and Q2 provide the clock function.

Adjustments

With a zero input adjust potentiometer P2 until the display shows a zero reading.

With a plus reference (10 volts) input adjust potentiometer P1 until the display shows a +1 .000 reading.

Circuit Schematic



Parts List

R1,R7 R10,R21 R24	4.7	K
R2,R4,R30	1	M
R3,R18	100	K
R5	10	K*
R6	#	
R11,R12	27	K
R13-R15,R20	100	K*
R16,R25-R28	47	K
R17	120	K
R19	1	M*
R29	22	M
C1	300	pf
C2,C3	.001	ufd
C4,C6	.02	ufd
C5	.1	ufd
Q1,Q2,Q5	2N5132	
Q4,Q6-Q8	2N5550	
Q5	2N5400	
IC1	LD 110	
IC2	LD 111	
IC3	DM8880	
D1	1N5240	
D2	1N4148	
+/- Display	Beckman 351	
Unit Display	Beckman 352	

*Metal film resistor

#Added if anode voltage is high.

Assembly Drawing