

PSI2662 – Projeto em Sistemas Eletrônicos Embarcados: Sensores e Atuadores

Contadores e Timers

Escola Politécnica da Universidade de São Paulo

Prof. Gustavo Rehder – grehder@lme.usp.br

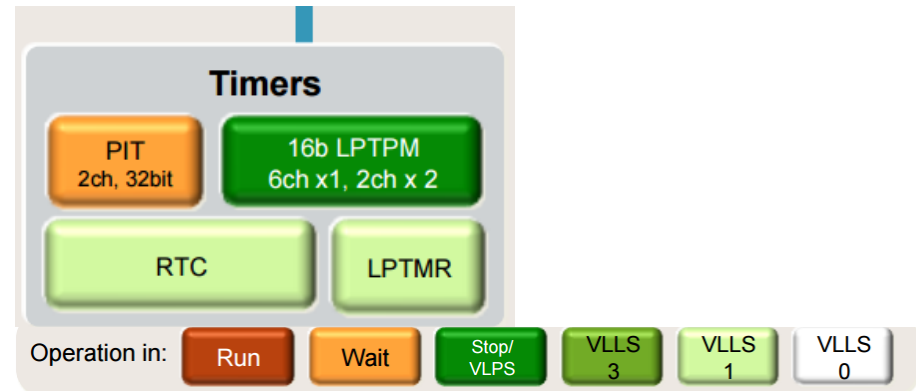


Segundo Semestre de 2015



Timers no KL25Z

- PIT - Periodic Interrupt Timer
 - Gera interrupções periódicas.
- TPM - Timer/PWM Module
 - Conectado a portas de I/O; possui input capture, output compare, pode gerar sinais de PWM; pode gerar interrupções.
- LPTMR - Low-Power Timer
 - Pode operar como timer ou contador in todos os modos de potência; pode “acordar” o sistema com interrupções; pode sincronizar o hardware.
- Real-Time Clock
 - Alimentado por um cristal externo de 32.768 kHz; rastreia tempo em segundos utilizando um registrador de 32 bits; pode gerar um alarme; pode gerar um sinal de 1 Hz e/ou uma interrupção; pode “acordar o sistema com interrupção.
- SYSTICK
 - Parte do Cortex M0+ Core; contador que pode gerar interrupções





System Tick Timer

- Ação executada periodicamente
- 24-bit down counter
- Clock ou Clock/16

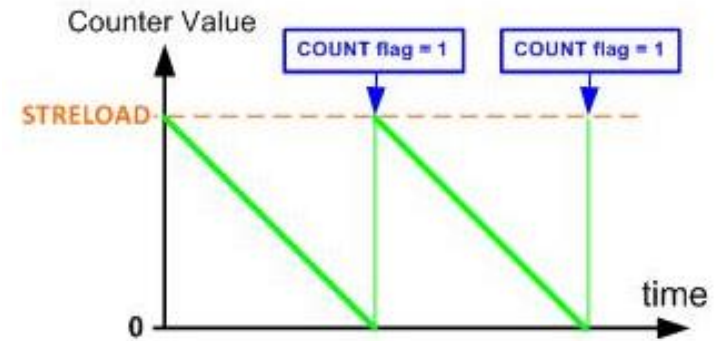


Figure 5-9: System Tick Counting

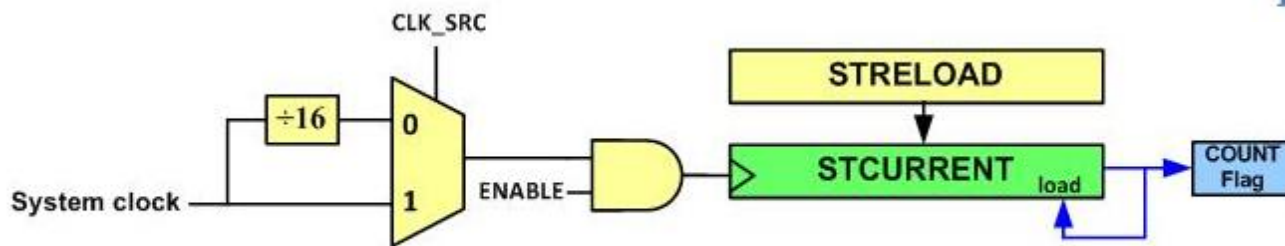


Figure 5-7: System Tick Timer Internal Structure

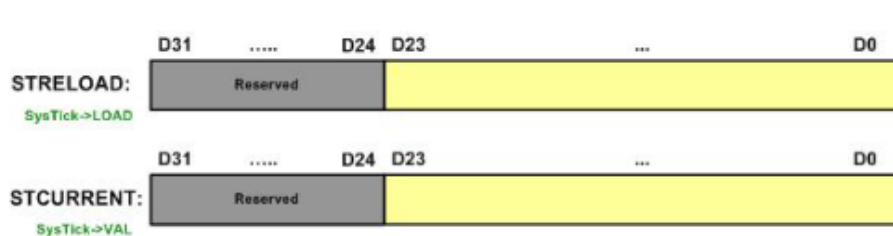


Figure 5-10: STRELOAD vs. STCURRENT



bit	Name	Description
0	ENABLE	Enable (0: the counter is disabled, 1: enables SysTick to begin counting down)
1	INTEN	Interrupt Enable 0: Interrupt generation is disabled, 1: when SysTick counts to 0 an interrupt is generated
2	CLK_SRC	Clock Source 0: System clock divided by 16 1: System clock
16	COUNT	Count Flag 0: the SysTick has not counted down to zero since the last time this bit was read 1: the SysTick has counted down to zero <i>Note: this flag is cleared by reading the STCTRL or writing to STCURRENT register.</i>

Figure 5-8: STCTRL (System Tick Control)



SysTick Contador CodeWarrior (PE)

Incluir (add file...) PDD header em <CodeWarrior Installation Path>\MCU\ProcessorExpert\lib\Kineticis\pdd\inc\

- ▼ SysTick:Init_SysTick
 - ISR Name of INT_SysTick
 - Init
 - ▼ PDD
 - ☑ SysTick_PDD_ClearInterruptFlag
 - ☑ SysTick_PDD_DisableInterrupt
 - ☑ SysTick_PDD_EnableDevice
 - ☑ SysTick_PDD_EnableInterrupt
 - ☑ SysTick_PDD_GetClkSource
 - ☑ SysTick_PDD_GetEnableDeviceStatus
 - ☑ SysTick_PDD_GetInterruptFlag
 - ☑ SysTick_PDD_GetInterruptMask
 - ☑ SysTick_PDD_ReadCalibrationReg
 - ☑ SysTick_PDD_ReadControlStatusReg
 - ☑ SysTick_PDD_ReadCurrentValueReg
 - ☑ SysTick_PDD_ReadReloadValueReg
 - ☑ SysTick_PDD_SetClkSource
 - ☑ SysTick_PDD_WriteControlStatusReg
 - ☑ SysTick_PDD_WriteCurrentValueReg
 - ☑ SysTick_PDD_WriteReloadValueReg

Component Inspector - SysTick Components Library

Properties Methods Clock Diagram

Name	Value	Details
Component name	SysTick	
Device	SysTick	SysTick
▼ Settings		
Clock source	Processor clock	
Reload value	16777215	D
Counter period	1.600 s	
▼ Interrupts		
Interrupt	INT_SysTick	INT_SysTick
Interrupt priority	0 (Highest)	
ISR Name		
Timer interrupt	Disabled	
▼ Initialization		
Timer enable	yes	
Clear counter	yes	
Call Init method	yes	

```
for (;;)
{
if (SysTick_PDD_ReadControlStatusReg (SysTick_DEVICE) &0x10000)
{
Bit1_NegVal ();
}
}
```



Timer/PWM Module

- 3 módulos (TPM_x = TPM0, TPM1 e TPM2)
 - 1 com 6 canais e 2 com 2 canais
 - Contador de 16 bits (up ou down)
 - Modos: Output Compare, Input Capture e PWM

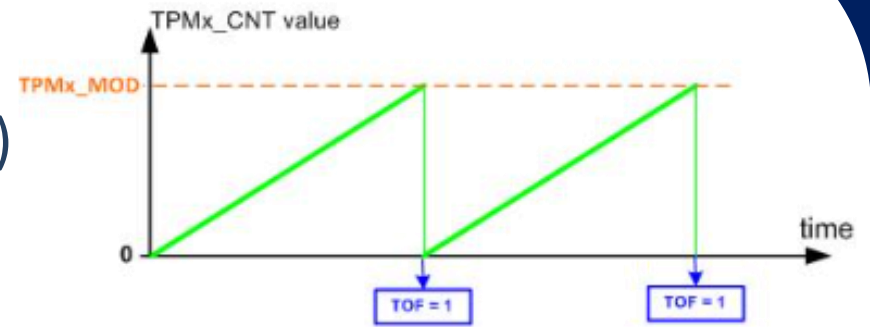


Figure 5-16: The role of TPM_x_MOD

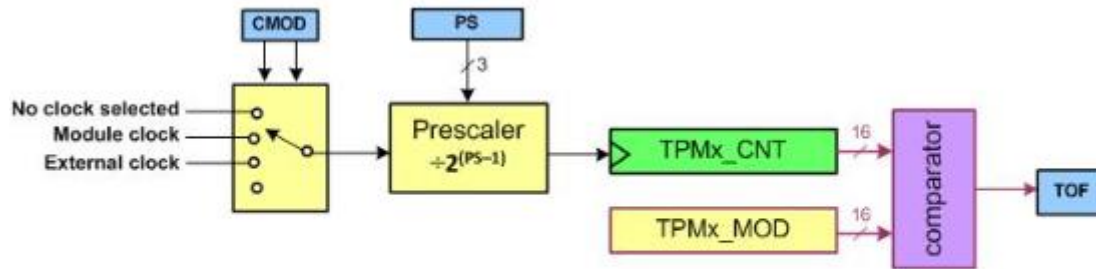


Figure 5-17: CMOD and PS (Prescaler) bits

SIM_SCGC6: 0x103C

D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D2	D1	D0
DAC0	0	RTC	0	ADC0	TPM2	TPM1	TPM0	PIT	0	DMAMUX	FTF	

bit	Name	Description
24	TPM0	TPM0 clock gate control (0: clock disabled, 1: clock enabled)
25	TPM1	TPM1 clock gate control (0: clock disabled, 1: clock enabled)
26	TPM2	TPM2 clock gate control (0: clock disabled, 1: clock enabled)

Figure 5-11: SIM_SCGC6 (SIM Clock Gating Control Register 6)

TPMx_SC: 0x0000

D31	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Reserved		DMA	TOF	TOIE	CPWMS	CMOD		PS			

Figure 5-18: Timer Status and Control (TPM_x_SC) Register

TPMx_CNT: 0x0004

D31	D30	D17	D16	D15	D14	D2	D1	D0
Reserved								COUNT		

Figure 5-13: TPM_x_CNT Register

TPMx_MOD: 0x0008

D31	D30	D17	D16	D15	D14	D2	D1	D0
Reserved								MOD		

Figure 5-14: TPM_x_CNT and TPM_x_MOD registers

SIM_SOPT2: 0x1004

D31	...	D28	D27	D26	D25	D24	D23	...	D19	D18	D17	D16	D15	D8	D7	...	D5	D4	D3	...	D0	
0		UART 9SRC	TPM SRC	0	USBR 0	0	PLFLL SEL	0							CLKOU TSEL	TPMx OUTPUT							0

TPM clock source select selects the clock source for the TPM counter clock

TPMSRC	Selected Clock
00	Clock disabled
01	MCGFLLCLK clock or MCGFLLCLK/2
10	OSCCERCLK clock
11	MCGIRCLK clock

Figure 5-12: SIM_SOPT2 (System Options 2)



TPM Contador CodeWarrior (PE)

Components - timer

- Generator_Configurations
 - FLASH
- OSs
- Processors
 - Cpu:MKL25Z128VLK4
- Components
 - Referenced_Components
 - Bit1:BitIO
 - TPM0:Init_TPM
 - ISR Name of INT_TPM0
 - Init
 - PDD

- TPM_PDD_GetOverflowInterruptFlag
- TPM_PDD_GetOverflowInterruptMask
- TPM_PDD_InitializeCounter
- TPM_PDD_ReadChannelControlReg
- TPM_PDD_ReadChannelValueReg
- TPM_PDD_ReadConfigurationReg
- TPM_PDD_ReadCounterReg
- TPM_PDD_ReadModuloReg
- TPM_PDD_ReadStatusControlReg
- TPM_PDD_SelectChannelEdgeLevel
- TPM_PDD_SelectChannelMode
- TPM_PDD_SelectDBGMode
- TPM_PDD_SelectPrescalerSource
- TPM_PDD_SelectPwmAlignMode
- TPM_PDD_SetDozeEnable
- TPM_PDD_SetGlobalTimeBase
- TPM_PDD_SetPrescaler
- TPM_PDD_WriteChannelControlReg
- TPM_PDD_WriteChannelValueReg
- TPM_PDD_WriteConfigurationReg
- TPM_PDD_WriteModuloReg
- TPM_PDD_WriteStatusControlReg

Name	Value
Component name	TPM0
Device	TPM0
Settings	
Clock gate	Enabled
Clock settings	
Clock source	TPM counter clock
Prescaler	divide by 128
Counter frequency	156.250 kHz
Modulo counter	65535 D
Period	419.430 ms
DBG mode	TPM counter stopped; output pins...
Global time base	Disabled
Counter reload on trigger	Disabled
Counter start on trigger	Disabled
Counter stop on overflow	Disabled
Counter in Doze mode	Enabled
Channels	
Pins	
Interrupts	
Initialization	
Call Init method	yes

```

for (;;)
{
if (TPM_PDD_ReadStatusControlReg (TPM0_DEVICE) & 0x80)
{
TPM_PDD_WriteStatusControlReg (TPM0_DEVICE, TPM_PDD_ReadSta
tusControlReg (TPM0_DEVICE) | 0x80);
Bit1_NegVal ();
}
}

```

TPM clock selection	Internal reference	
Clock frequency [MHz]	0.032768	0.032768 MHz

TPM Output Compare

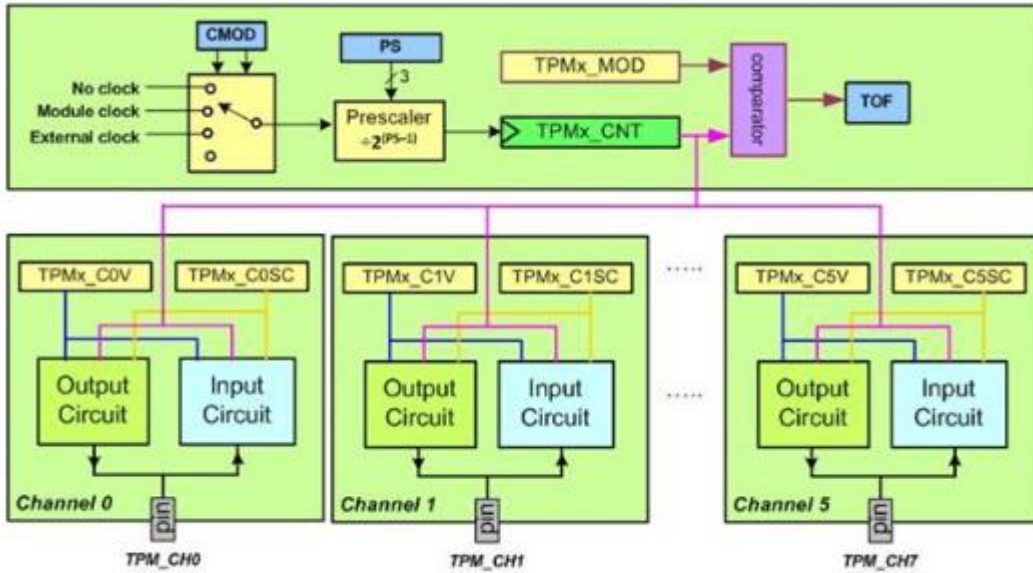


Figure 5-19: The Channels of TPMx

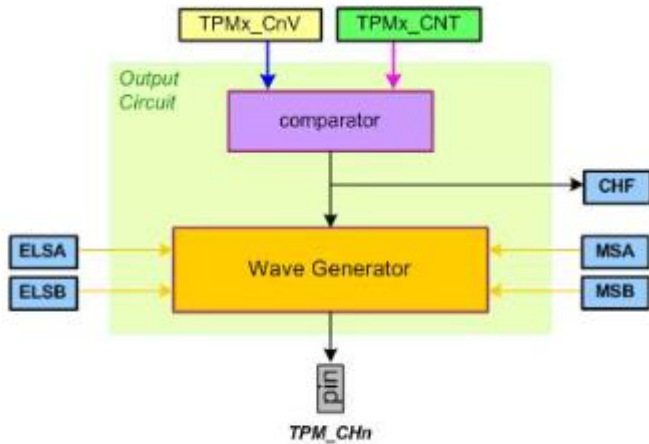


Figure 5-21: Output Circuit



Figure 5-20: TPMx_CnV (TPMx Channel Value) Register



Figure 5-22: TPMxCnSC (TPMx Channel Status and Control)

Flag

Configuração da Saída

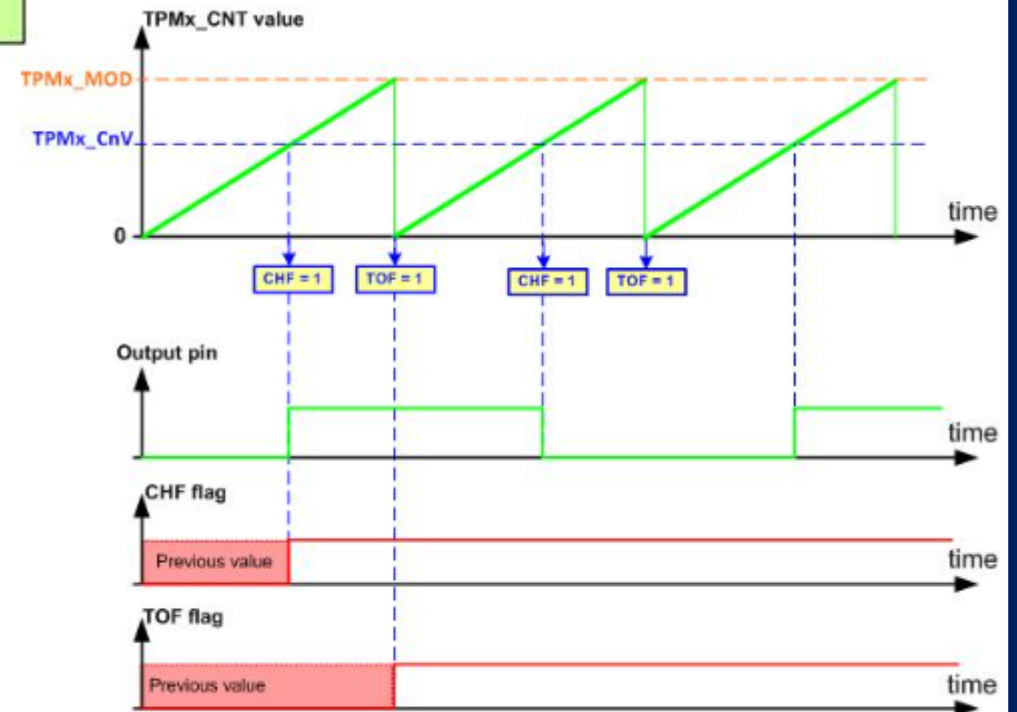


Figure 5-23: In Toggle Mode



TPM Contador CodeWarrior (PE): Output Compare

Name	Value
Clock source	TPM counter clock
Prescaler	divide by 1
Counter frequency	32.768 kHz
Modulo counter	65535 D
Period	2.000 s
DBG mode	TPM counter stopped; output pins...
Global time base	Disabled
Counter reload on trigger	Disabled
Counter start on trigger	Disabled
Counter stop on overflow	Disabled
Counter in Doze mode	Enabled
Channels	
Channel 0	Enabled
Channel mode	Output compare
Output action	Toggle output
Channel value register	65535 D
Pin	Enabled
Pin	TSI0_CH11/PTB18/TPM2_CH0
Pin signal	

PWM

Name	Value
Modulo counter	65535 D
Period	3.125 ms
DBG mode	TPM counter stopped; output pins...
Global time base	Disabled
Counter reload on trigger	Disabled
Counter start on trigger	Disabled
Counter stop on overflow	Disabled
Counter in Doze mode	Enabled
Channels	
Channel 0	Enabled
Channel mode	Edge-aligned PWM
PWM polarity	Low-true
Channel value register	4095 D
Pin	Enabled
Pin	TSI0_CH11/PTB18/TPM2_CH0
Pin signal	
Interrupt/DMA	
Channel 1	Disabled
Pins	

```
for ( ; ; ) { }
```




Input Capture

Frequência e Largura de Pulso

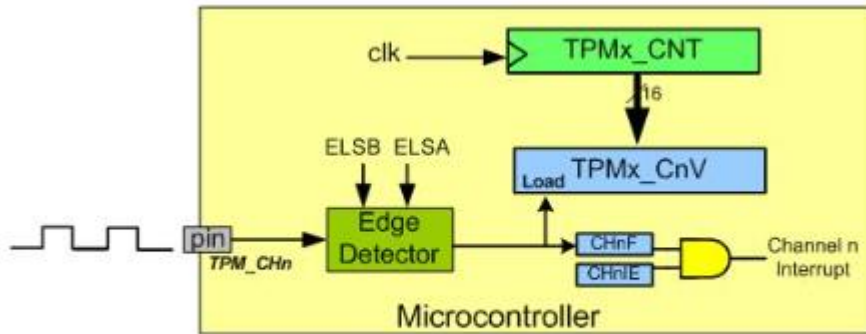


Figure 5-27: Input Edge Time Capturing

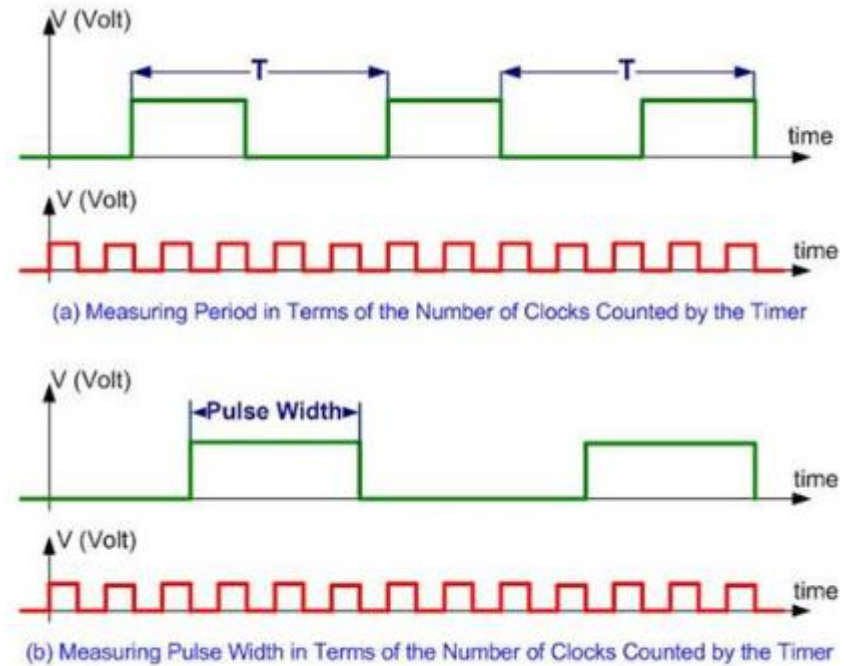


Figure 5-28: Measuring Period and Pulse Width

Eventos

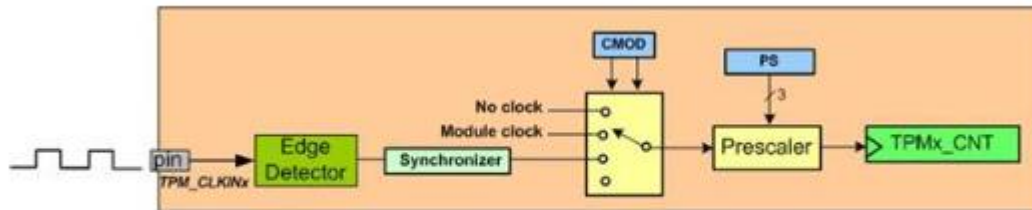






Figure 5-29: Counter Diagram

→ Interrupção



Code Warrior Processor Expert -Timers

 Init_LPTMR
 Init_PIT
 Init_SysTick
 Init_TPM

} Utiliza PDD – configuração direta com registradores

 TimerUnit_LDD

} Auxilia na configuração de qualquer tipo de timer

 TimerInt_LDD



} Interrupção periódica com qualquer tipo de timer

 PWM

} Configuração do PWM utilizando um timer TPM.



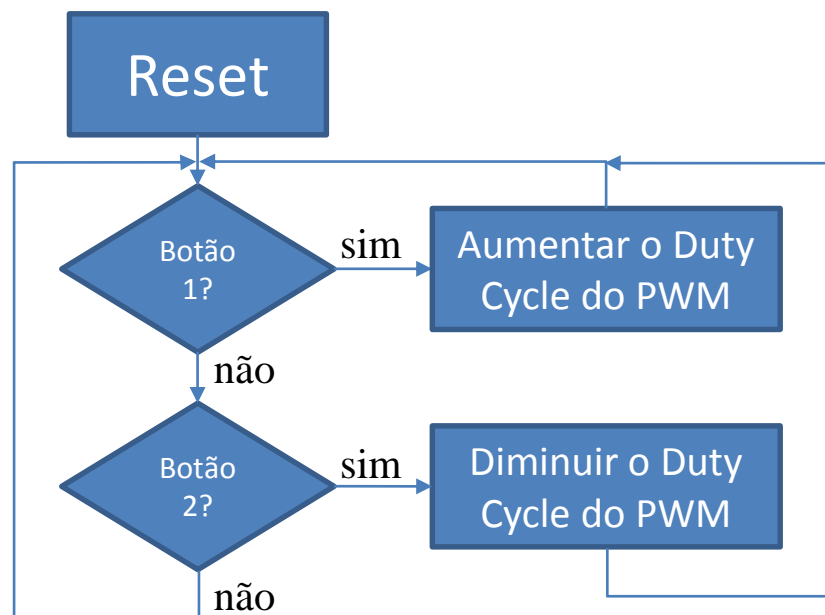
Code Warrior Processor Expert -Outros

-  **Init_GPIO** } Inicialização das portas GPIO – Configurações (pull-up drive strength, filtro etc.)
-  **BitIO** } Configuração de Pinos individuais – Entrada/Saída



Exercício

- Monitorar entradas para aumentar e diminuir o *duty-cycle* de um PWM que alimenta um LED.



ou usar componente PWM do Processor Expert

olhar pinagem

Configurações:

- Timer TPM – PWM



- Entradas digitais

Qual timer usar?
TPM0, TPM1 ou TPM2?
Qual canal?

Qual frequência do timer?

Quais pinos?
Pull-up, pull-down?

Qual frequência da CPU?

Desafio: Utilizar o botão de reset para controlar a intensidade do LED.