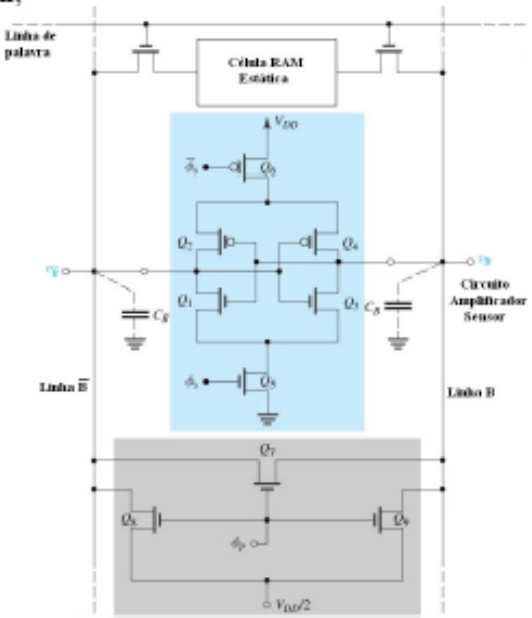
PSI3024 – Eletrônica

Aula 38

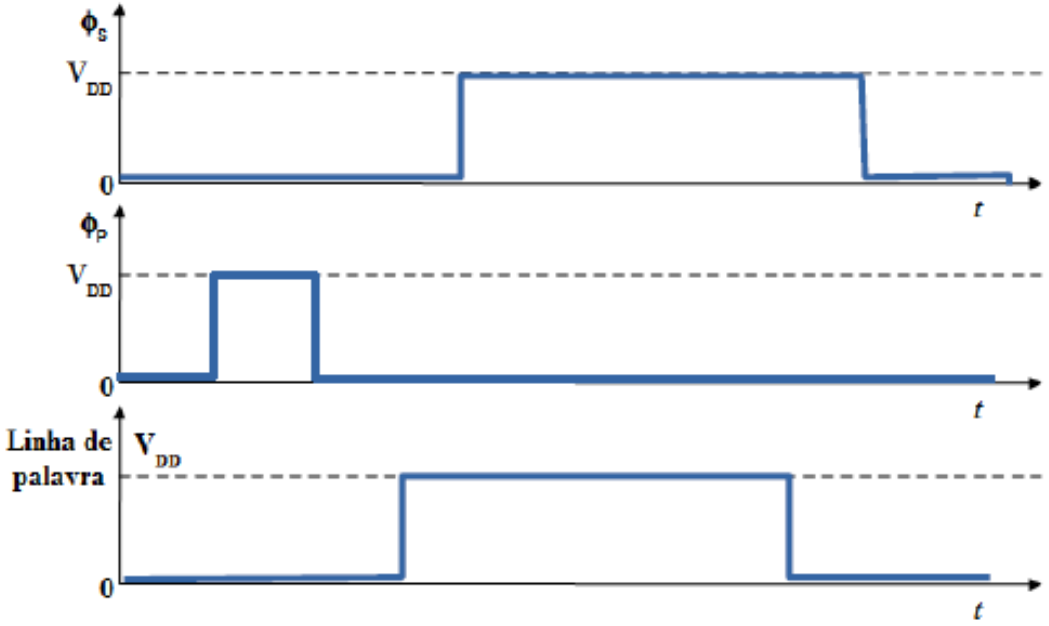
2023

Para o circuito a seguir,



a) Explique a função do bloco formado pelos transistores Q_7, Q_8 e Q_9.

b) Explique o ciclo de leitura da célula de memória RAM estática, através do bloco amplificador sensor e do bloco formado pelos transistores Q_7, Q_8 e Q_9. Inicie a explicação esboçando os perfis temporais das fases ϕ_S e ϕ_P, e "linha de palavra" nos diagramas a seguir.



EXEMPLO 10.3

Considere o inversor pseudo-NMOS fabricado na tecnologia CMOS especificada no Exemplo 10.1, ou seja, $\mu_n C_{ox} = 115\ \mu A/V^2$, $\mu_p C_{ox} = 30\ \mu A/V^2$, $V_{tn} = -V_{tp} = 0{,}4$ V e $V_{DD} = 2{,}5$ V. Seja a razão W/L de Q_N de (0,375 μm/0,25 μm) e $r = 9$. Obtenha:

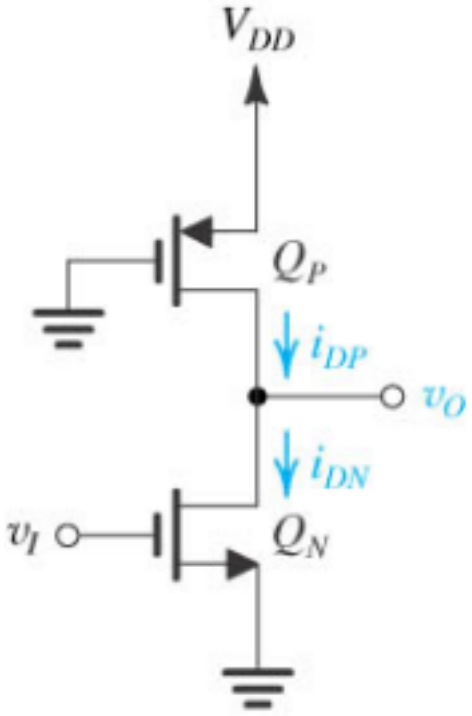
(a) V_{OH}, V_{OL}, V_{IL}, V_{IH}, V_M, MR_H e MR_L

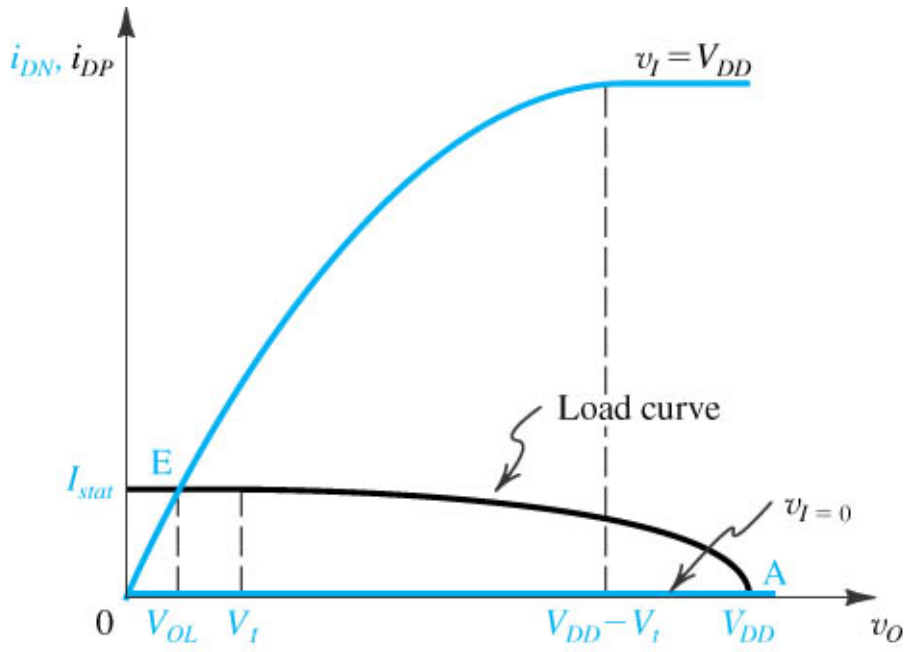
(b) $(W/L)_p$

(c) I_{estat} e P_D

(d) t_{PLH}, t_{PHL} e t_P, supondo uma capacitância total na saída do inversor de 7 fF

Inversor pseudo-NMOS





Região II (segmento BC)

$$k_n = rk_p,$$

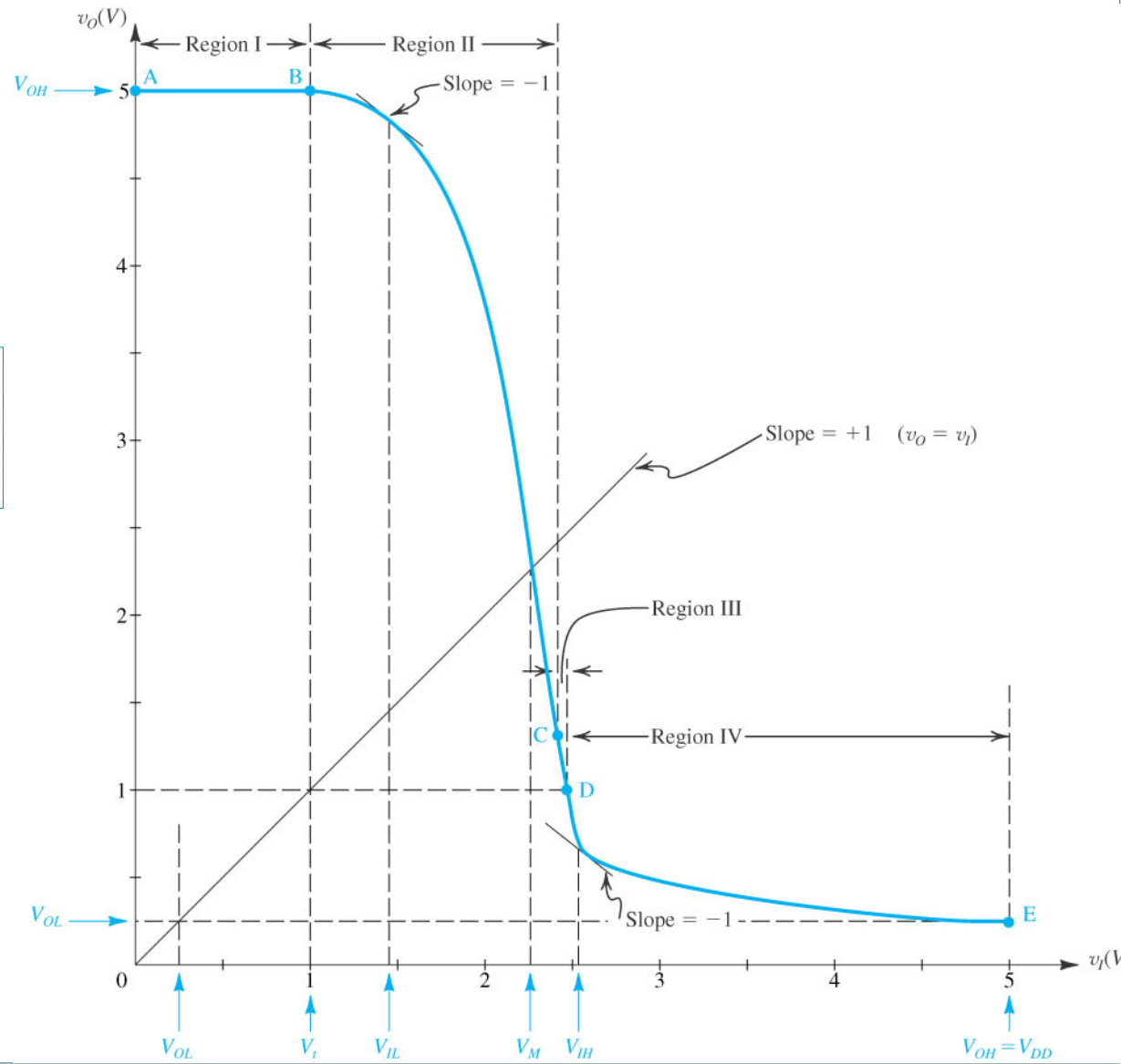
$$v_O = V_t + \sqrt{(V_{DD} - V_t)^2 - r(v_I - V_t)^2}$$

$$V_{IL} = V_t + \frac{V_{DD} - V_t}{\sqrt{r(r+1)}}$$

$$V_M = V_t + \frac{V_{DD} - V_t}{\sqrt{r+1}}$$

(ponto C)

$$v_O = v_I - V_t$$



Região IV (segmento DE)

$$v_O = (v_I - V_t) - \sqrt{(v_I - V_t)^2 - \frac{1}{r}(V_{DD} - V_t)^2}$$

$$k_n = rk_p$$

Região III (segmento CD)

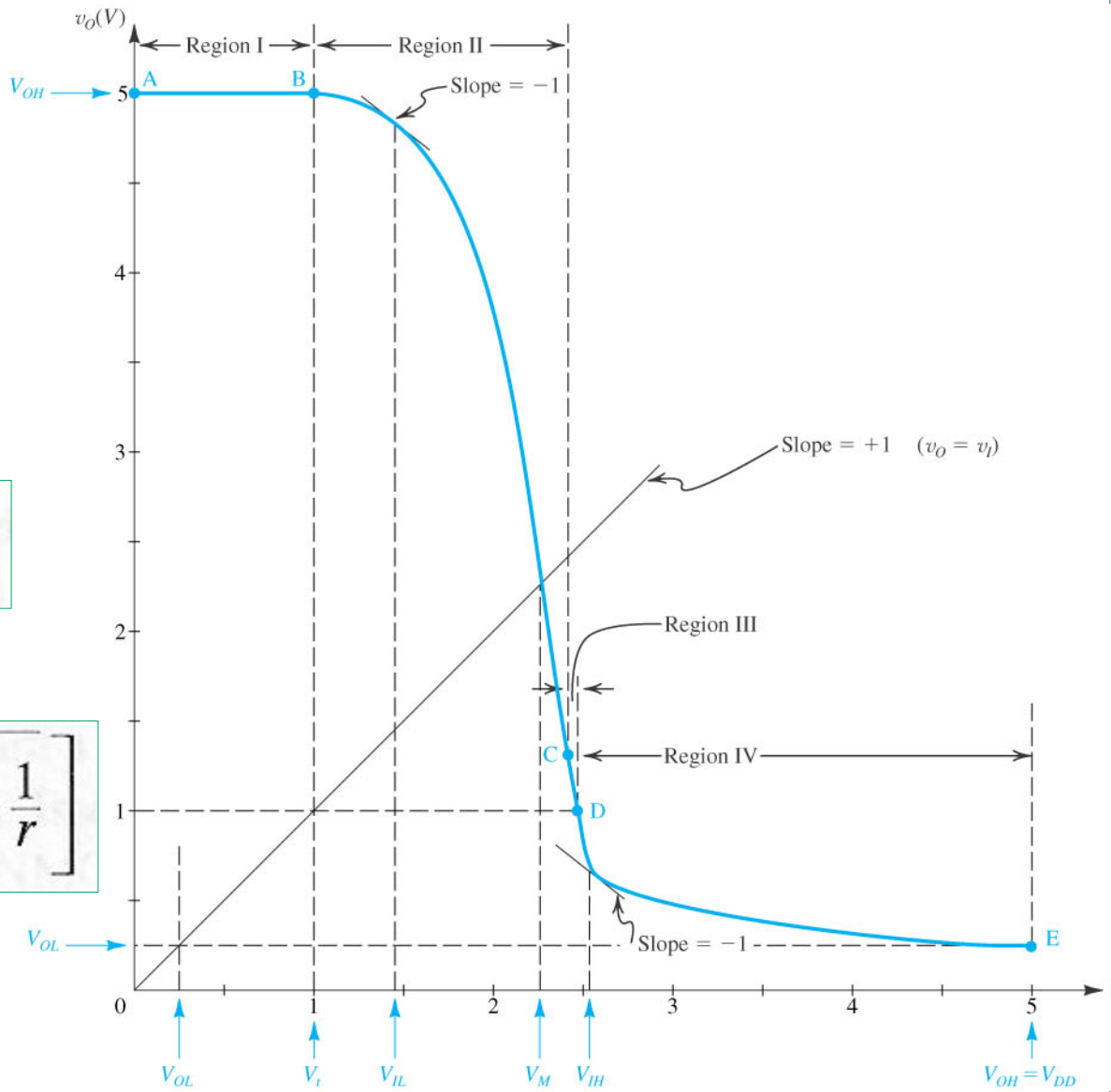
ponto D $\quad v_O = V_t.$

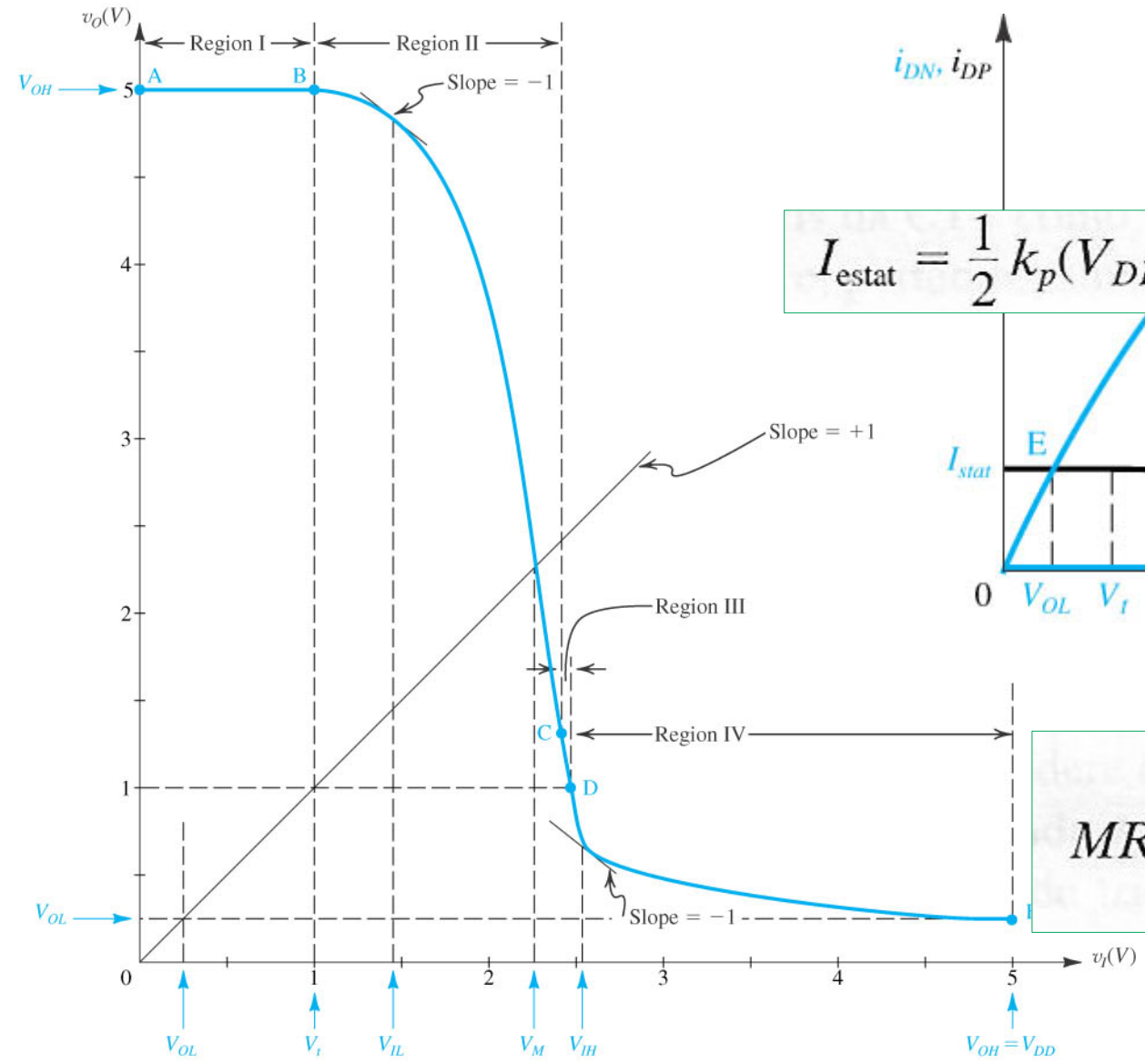
$$\partial v_O/\partial v_I = -1 \text{ e } v_1 = V_{IH},$$

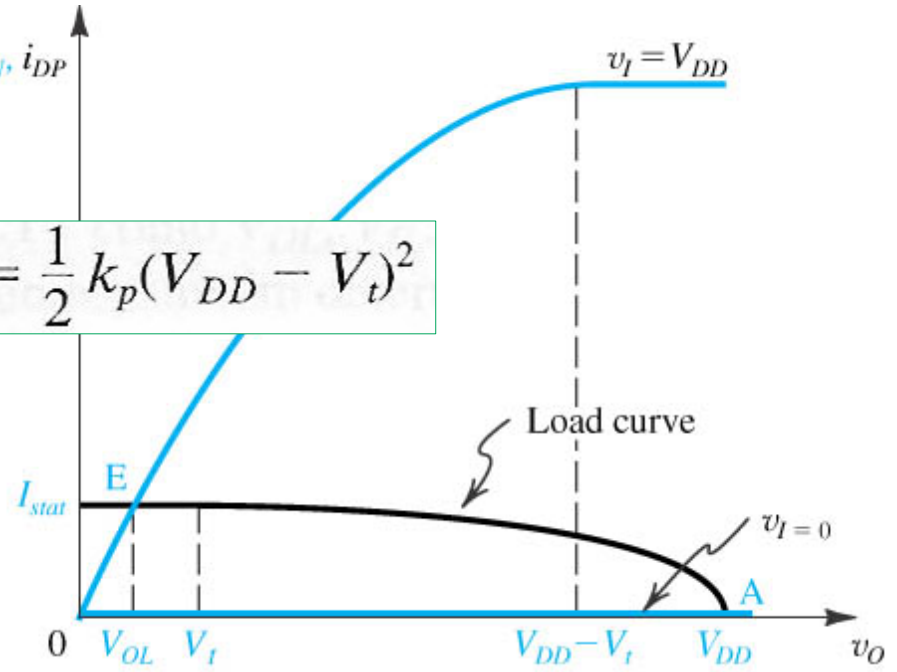
$$V_{IH} = V_t + \frac{2}{\sqrt{3r}}(V_{DD} - V_t)$$

$$v_I = V_{DD}$$

$$V_{OL} = (V_{DD} - V_t)\left[1 - \sqrt{1 - \frac{1}{r}}\right]$$



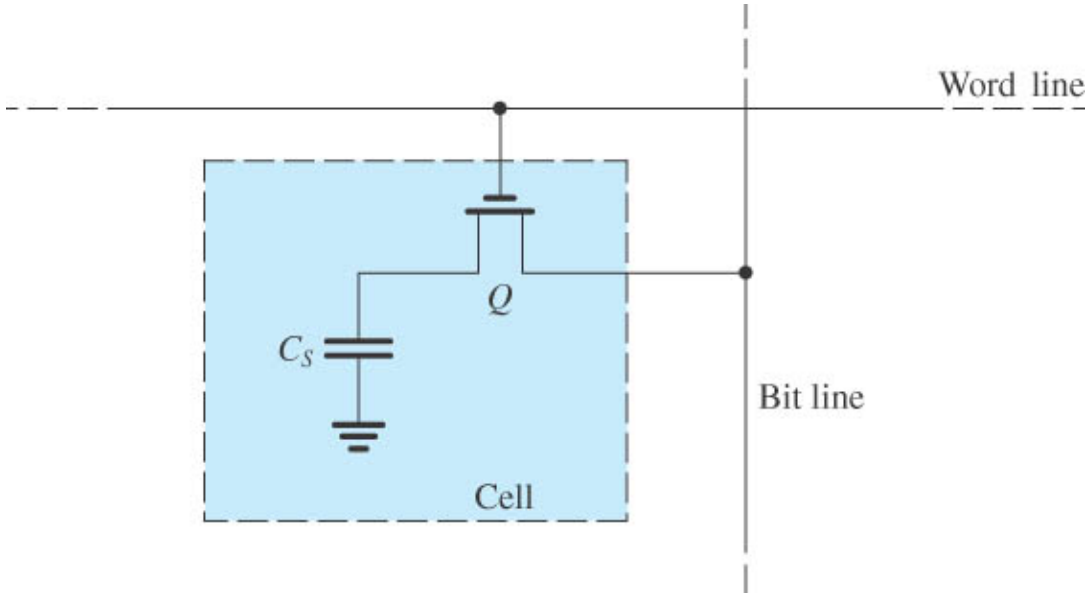




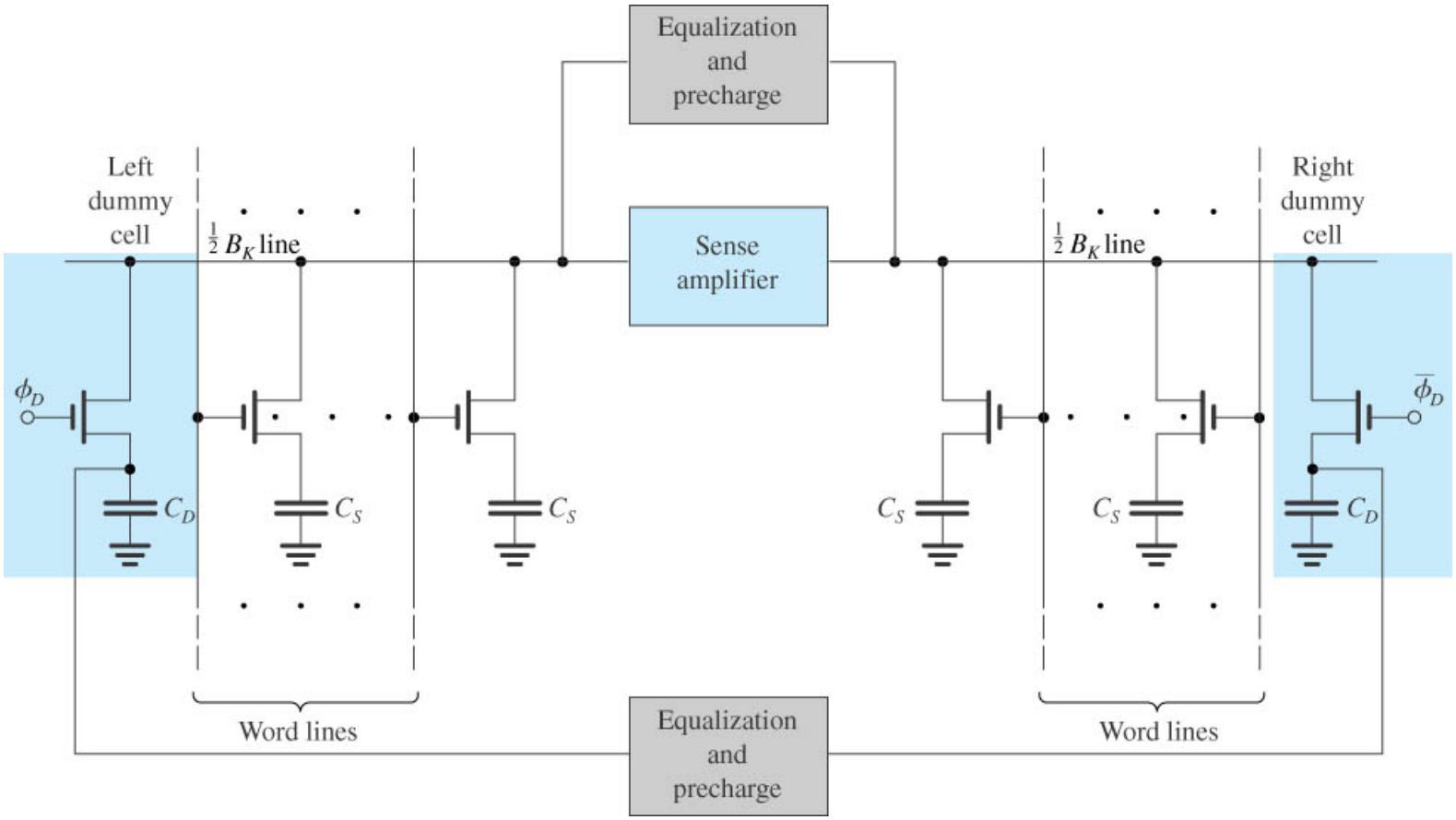
$$I_{\text{estat}} = \frac{1}{2} k_p (V_{DD} - V_t)^2$$

$$MR_H = (V_{DD} - V_t\left(1 - \frac{2}{\sqrt{3r}}\right)$$

$$MR_L = V_t - (V_{DD} - V_t)\left[1 - \sqrt{1 - \frac{1}{r} - \frac{1}{\sqrt{r(r+1)}}}\right]$$

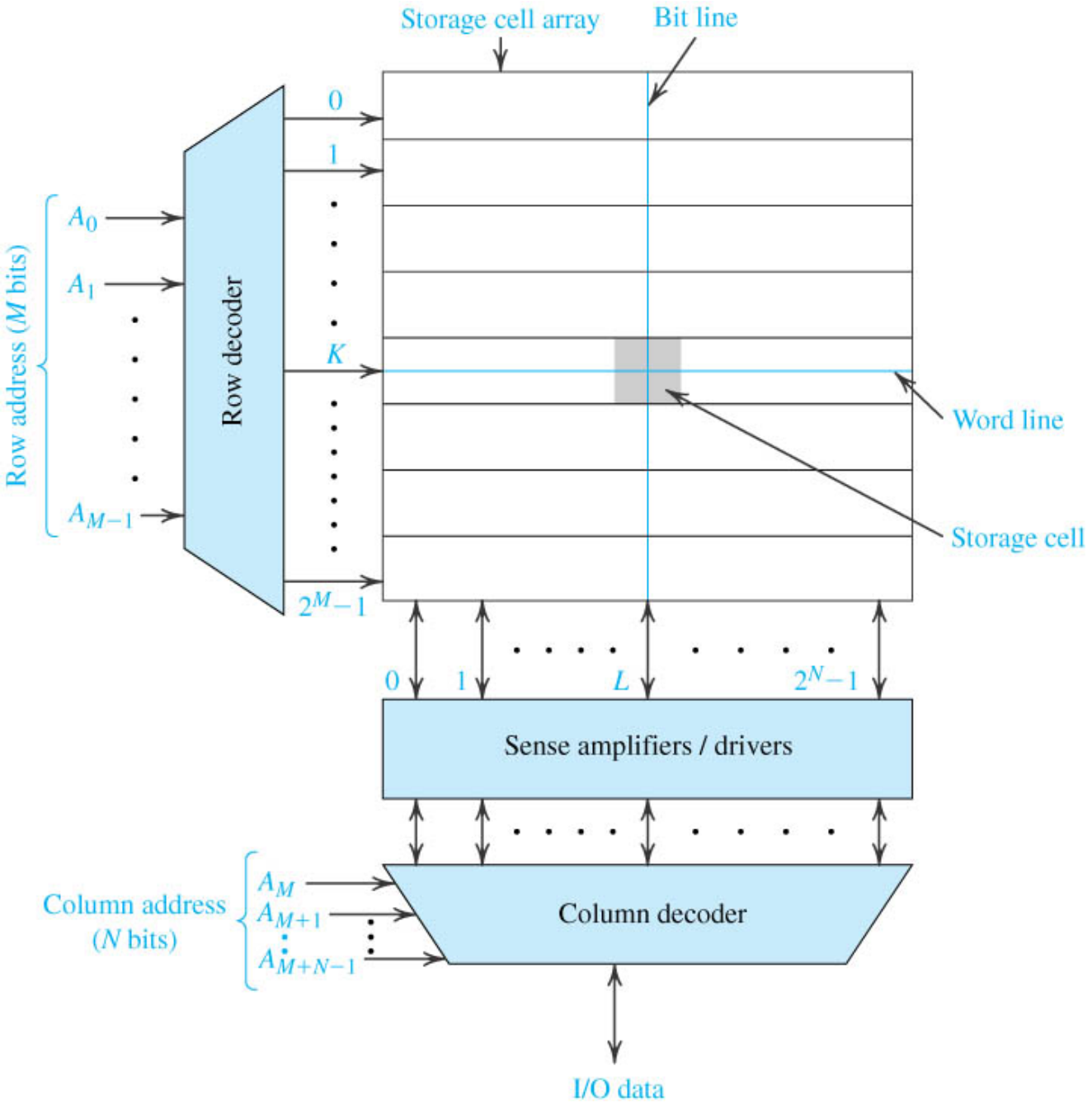


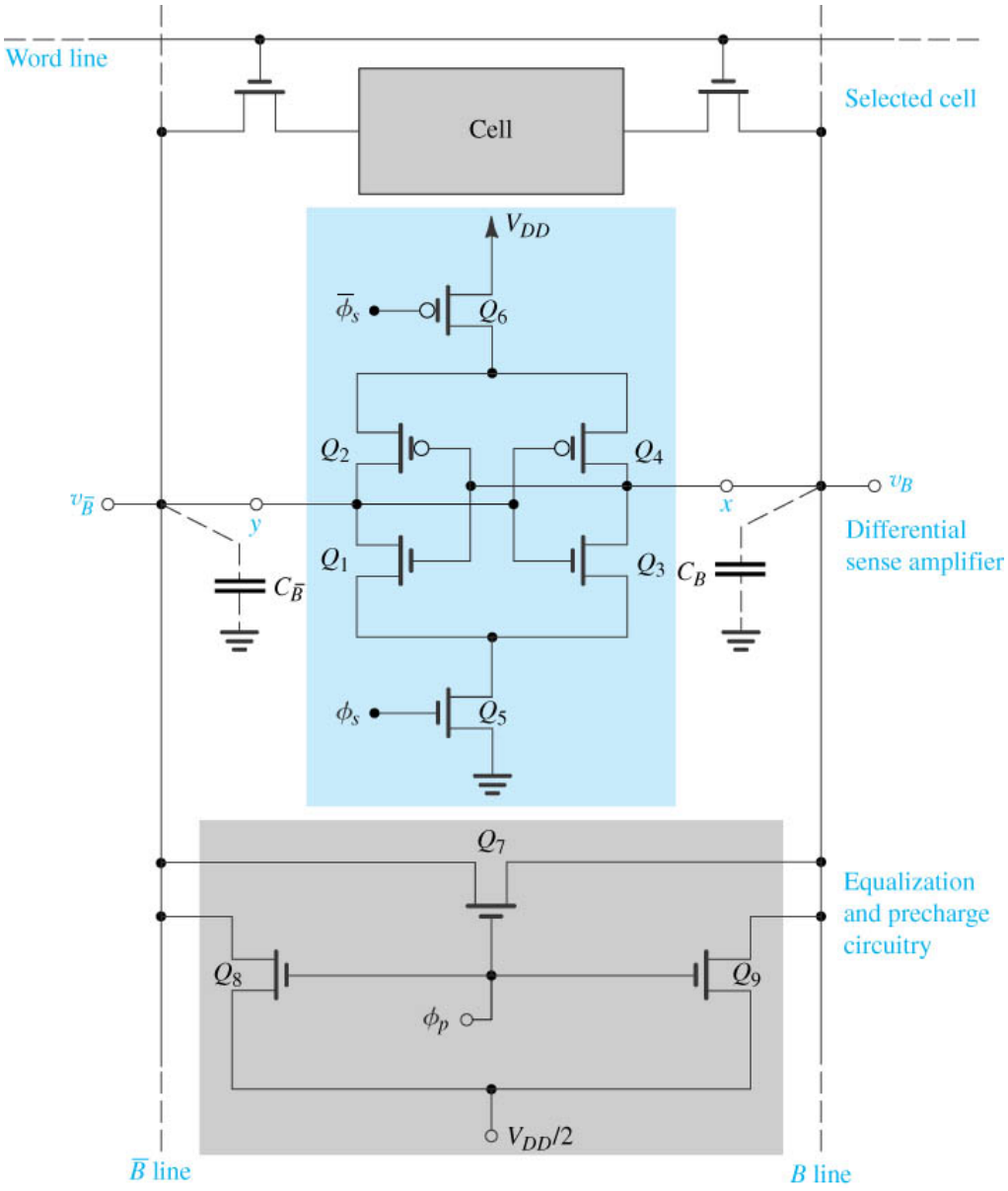
- **Figure 11.21** The one-transistor dynamic RAM cell.



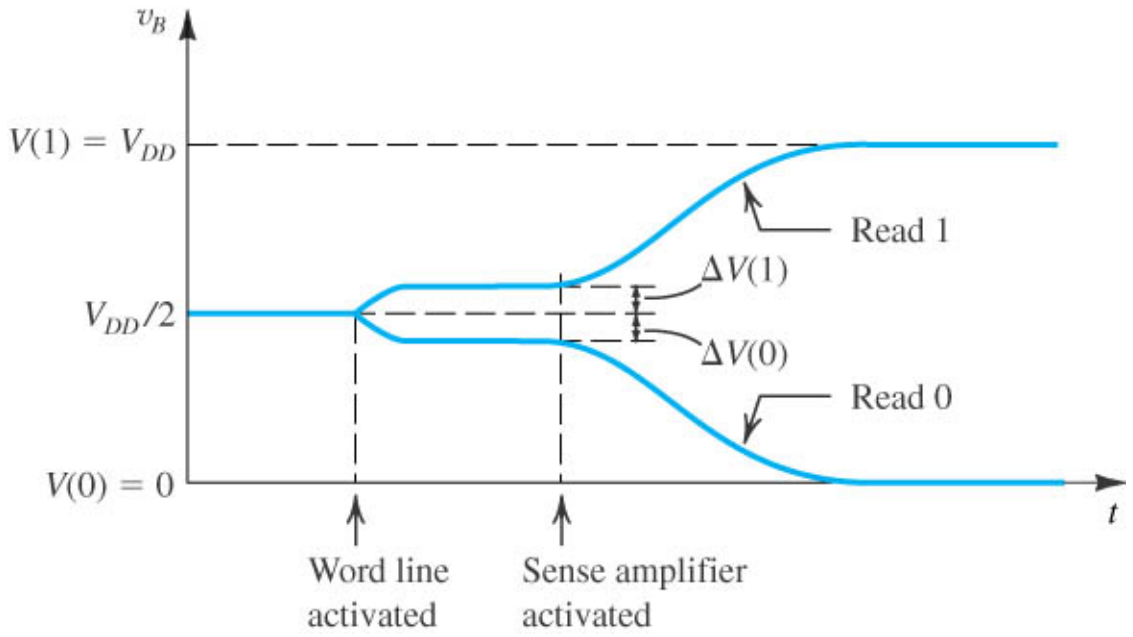
- **Figure 11.25** An arrangement for obtaining differential operation from the single-ended DRAM cell. Note the dummy cells at the far right and far left.

- A 2^{M+N}-bit memory chip organized as an array of 2^M rows $\times$ 2^N columns.

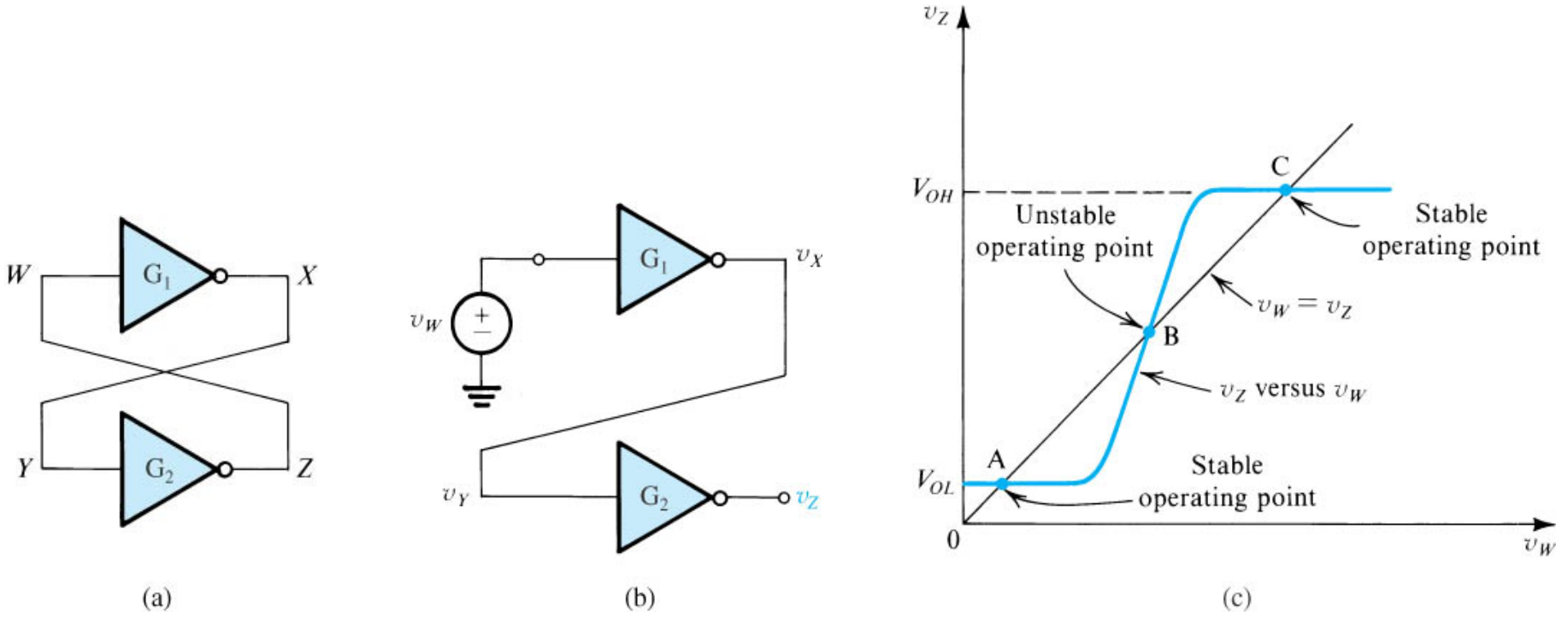




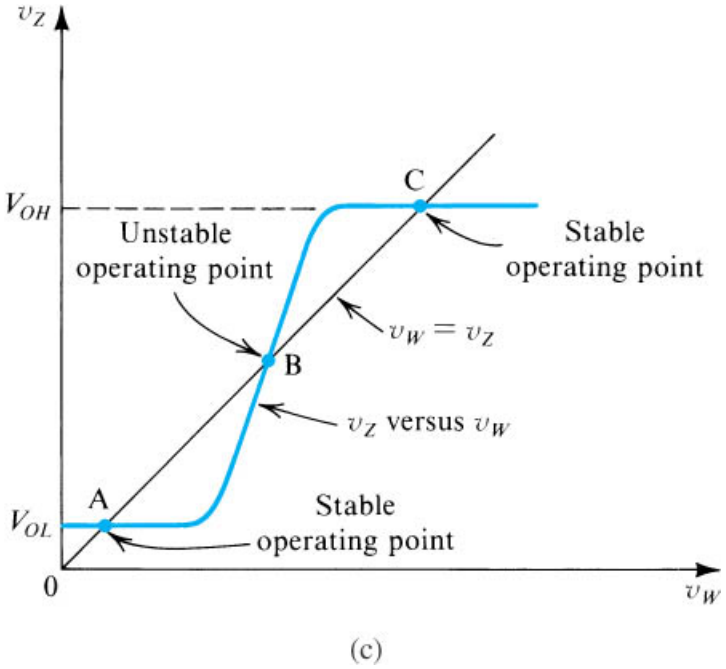
- **Figure 11.23** A differential sense amplifier connected to the bit lines of a particular column. This arrangement can be used directly for SRAMs (which utilize both the *B* and $\overline{B}$ lines). DRAMs can be turned into differential circuits by using the "dummy cell" arrangement shown in Fig. 11.25.



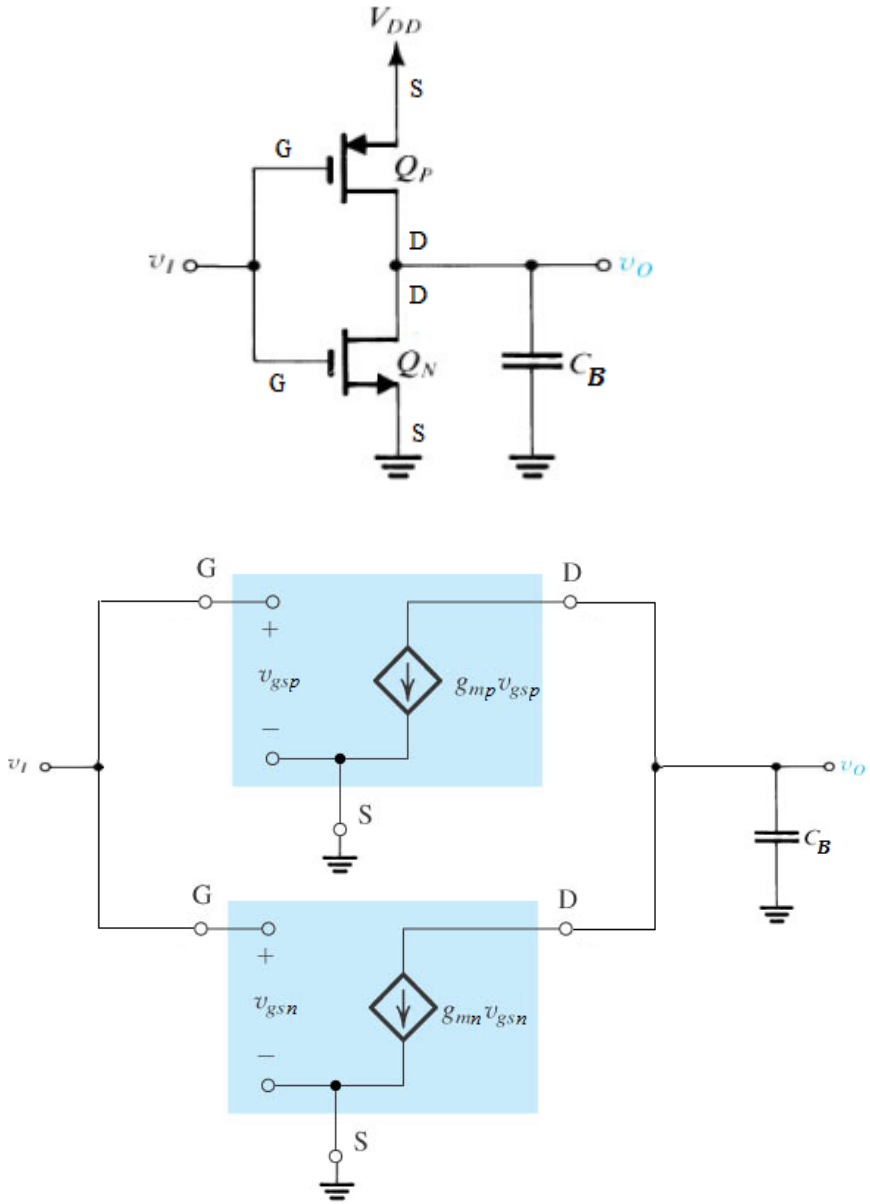
- **Figure 11.24** Waveforms of v_B before and after the activation of the sense amplifier. In a read-1 operation, the sense amplifier causes the initial small increment $\Delta V(1)$ to grow exponentially to V_{DD}. In a read-0 operation, the negative $\Delta V(0)$ grows to 0. Complementary signal waveforms develop on the *B* line.



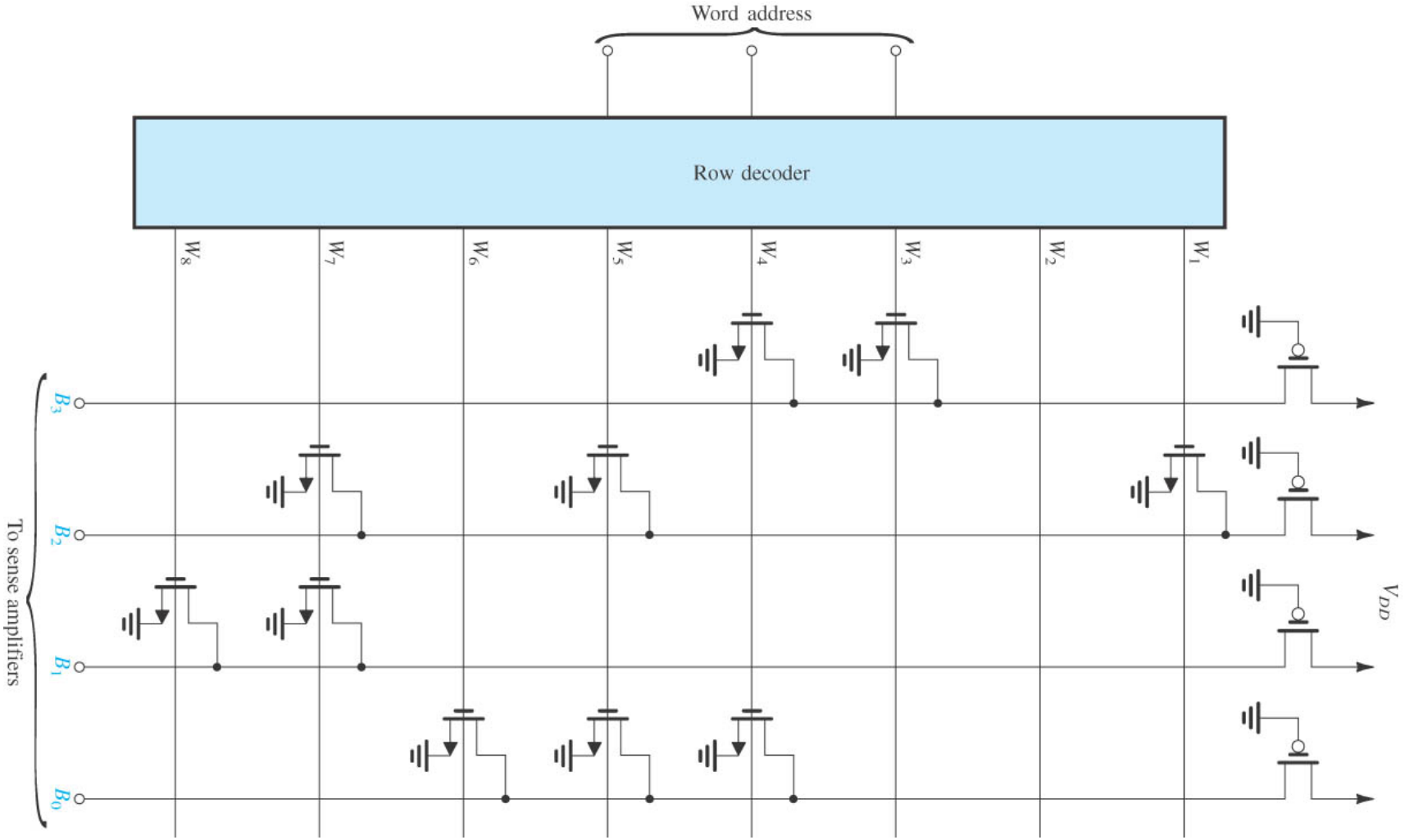
- **Figure 11.1** **(a)** Basic latch. **(b)** The latch with the feedback loop opened. **(c)** Determining the operating point(s) of the latch.



(c)



- **Figure 11.1 (c)** Determining the operating point(s) of the latch.



- **Figure 11.29** A simple MOS ROM organized as 8 words × 4 bits.