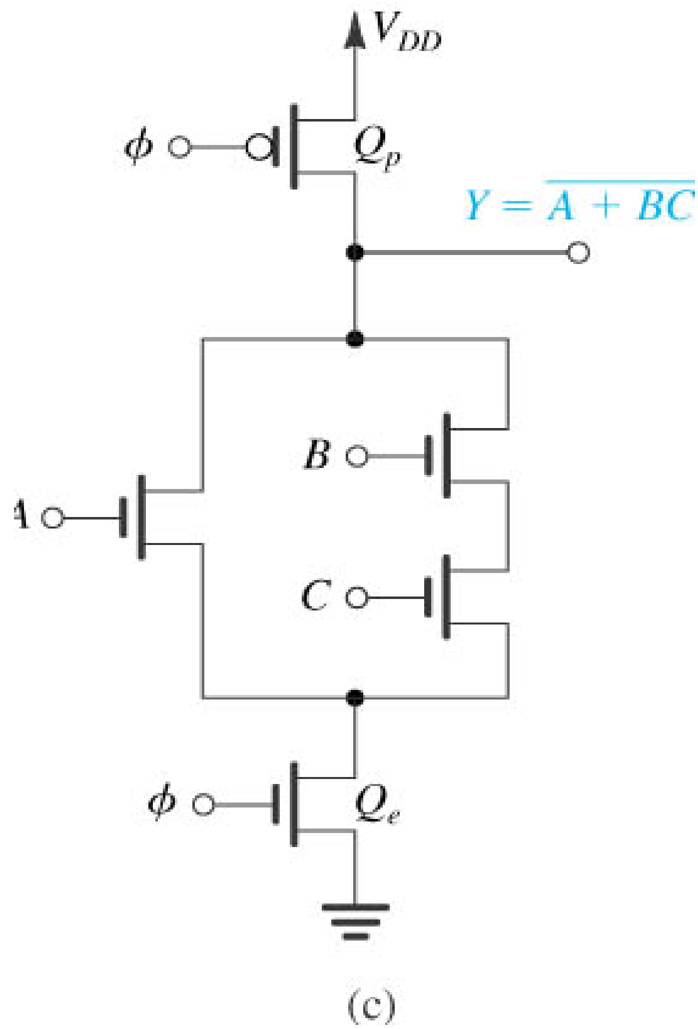
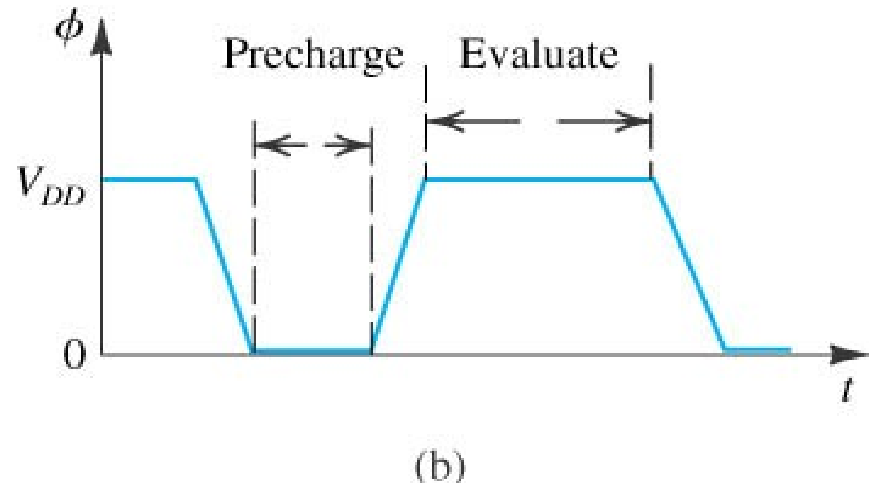
PSI3024 – Eletrônica

Aulas 36 e 37
2023





- **Figure 10.33 (a)** Basic structure of dynamic-MOS logic circuits. **(b)** Waveform of the clock needed to operate the dynamic logic circuit. **(c)** An example circuit.

EXEMPLO 10.3

Considere o inversor pseudo-NMOS fabricado na tecnologia CMOS especificada no Exemplo 10.1, ou seja, $\mu_n C_{ox} = 115\ \mu A/V^2$, $\mu_p C_{ox} = 30\ \mu A/V^2$, $V_{tn} = -V_{tp} = 0{,}4$ V e $V_{DD} = 2{,}5$ V. Seja a razão W/L de Q_N de $(0{,}375\ \mu m/0{,}25\ \mu m)$ e $r = 9$. Obtenha:

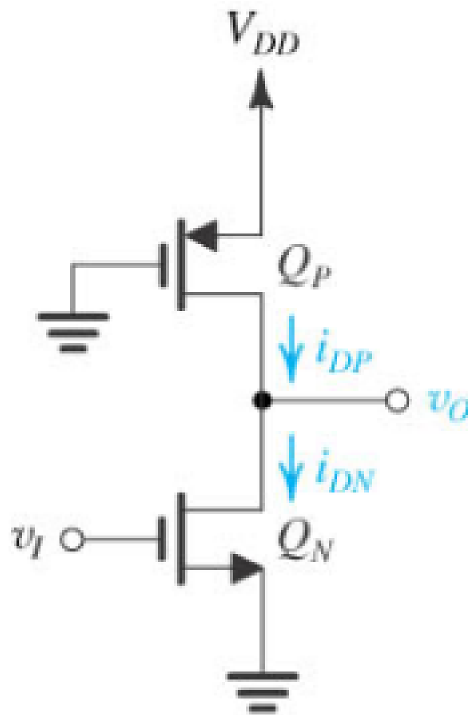
(a) V_{OH}, V_{OL}, V_{IL}, V_{IH}, V_M, MR_H e MR_L

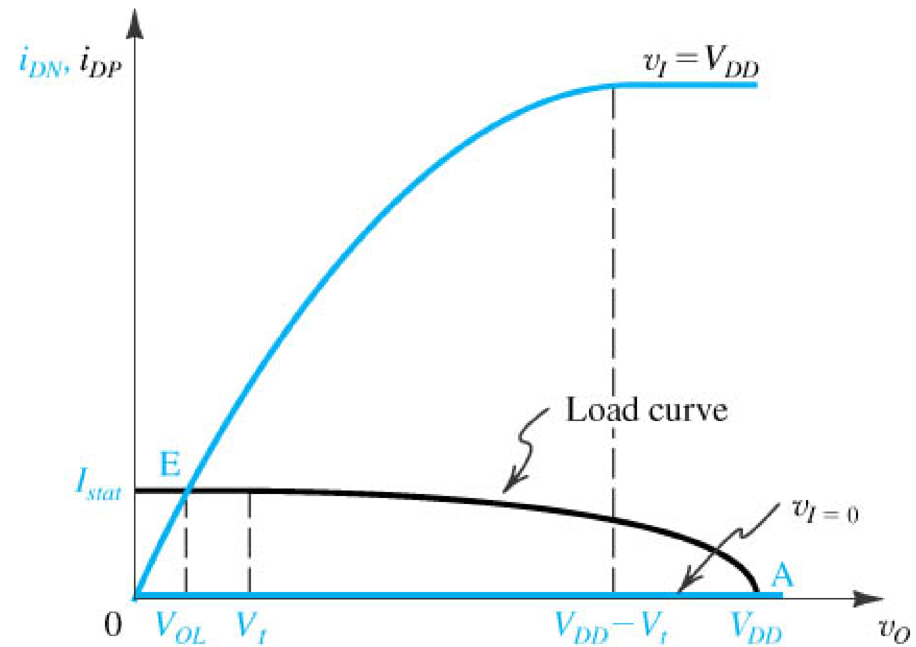
(b) $(W/L)_p$

(c) I_{estat} e P_D

(d) t_{PLH}, t_{PHL} e t_P, supondo uma capacitância total na saída do inversor de 7 fF

Inversor pseudo-NMOS

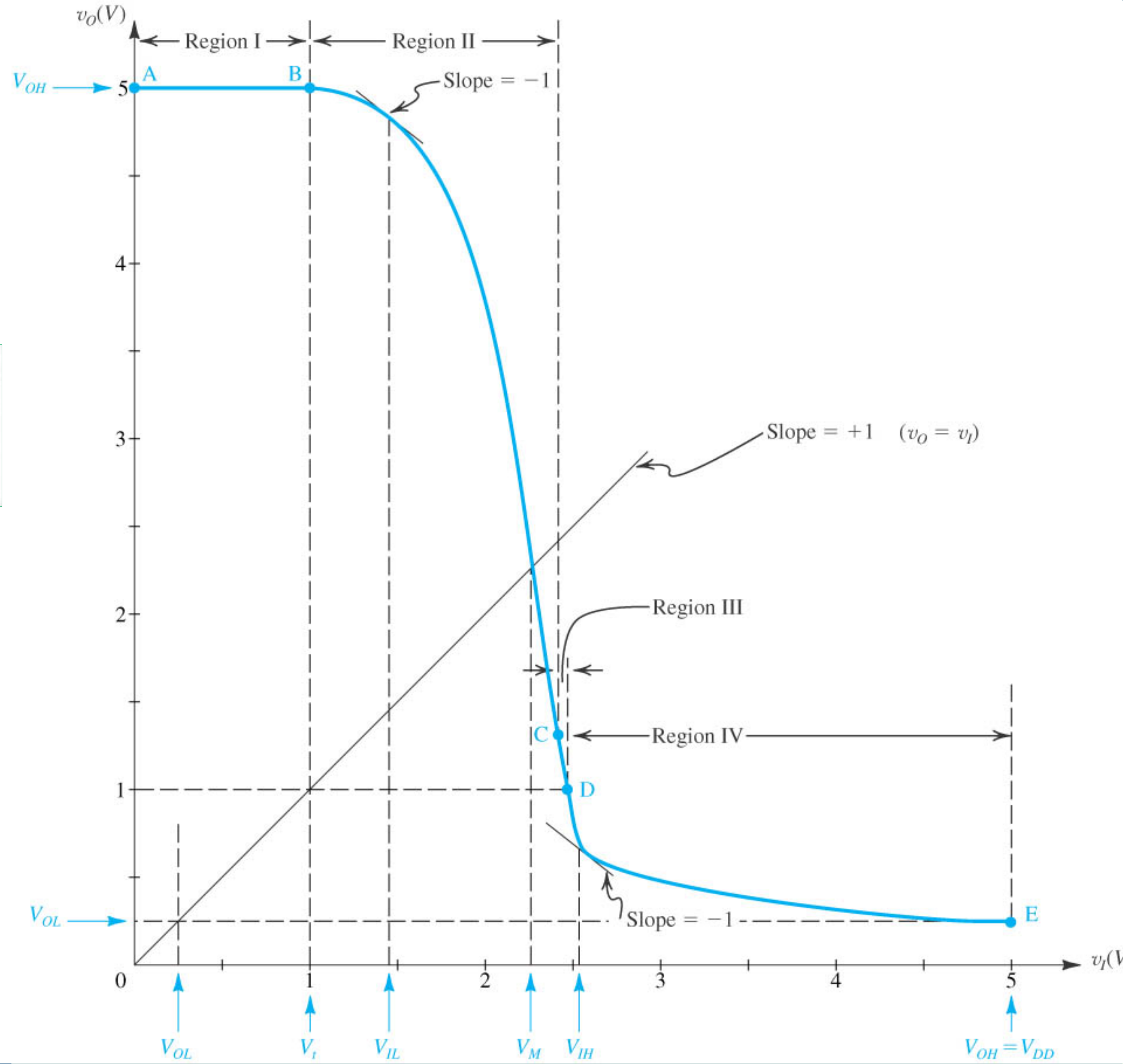




Região II (segmento BC)

$$k_n = rk_p,$$

$$v_O = V_t + \sqrt{(V_{DD} - V_t)^2 - r(v_I - V_t)^2}$$



$$V_{IL} = V_t + \frac{V_{DD} - V_t}{\sqrt{r(r+1)}}$$

$$V_M = V_t + \frac{V_{DD} - V_t}{\sqrt{r+1}}$$

(ponto C)

$$v_O = v_I - V_t$$

Região IV (segmento DE)

$$k_n = rk_p$$

$$v_O = (v_I - V_t) - \sqrt{(v_I - V_t)^2 - \frac{1}{r}(V_{DD} - V_t)^2}$$

Região III (segmento CD)

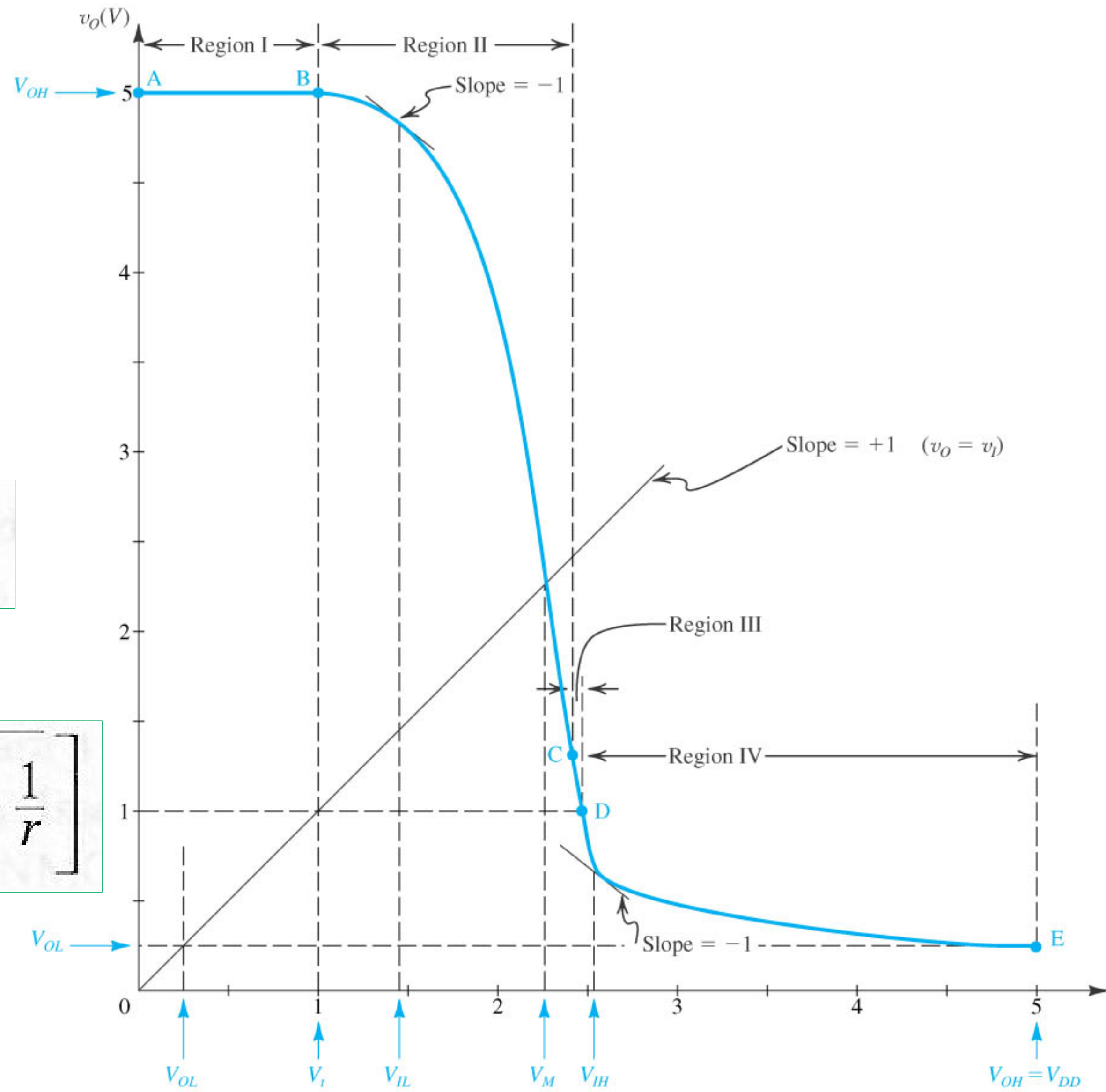
ponto D $v_O = V_t.$

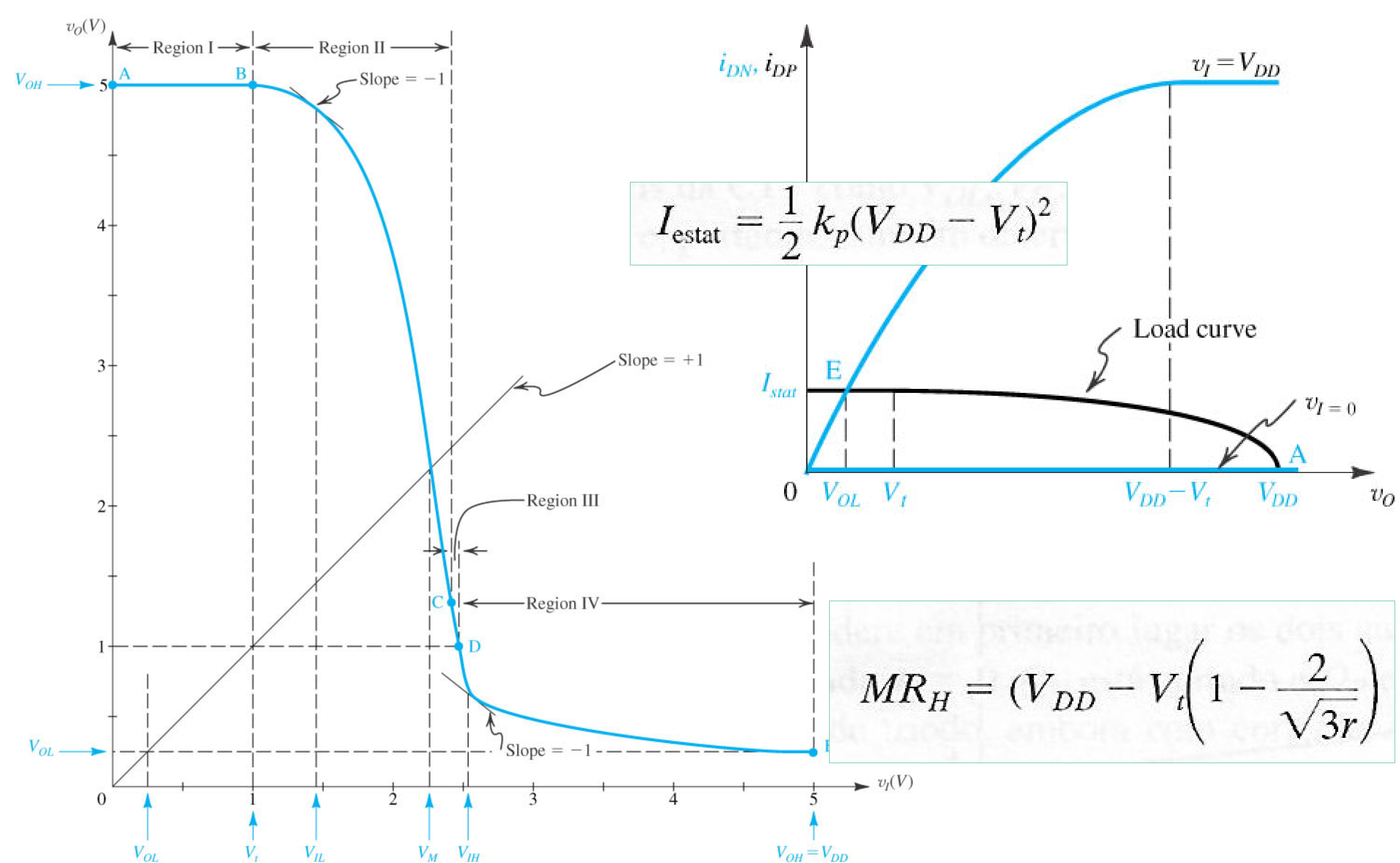
$\partial v_O / \partial v_I = -1$ e $v_1 = V_{IH},$

$$V_{IH} = V_t + \frac{2}{\sqrt{3r}}(V_{DD} - V_t)$$

$$v_I = V_{DD}$$

$$V_{OL} = (V_{DD} - V_t)\left[1 - \sqrt{1 - \frac{1}{r}}\right]$$



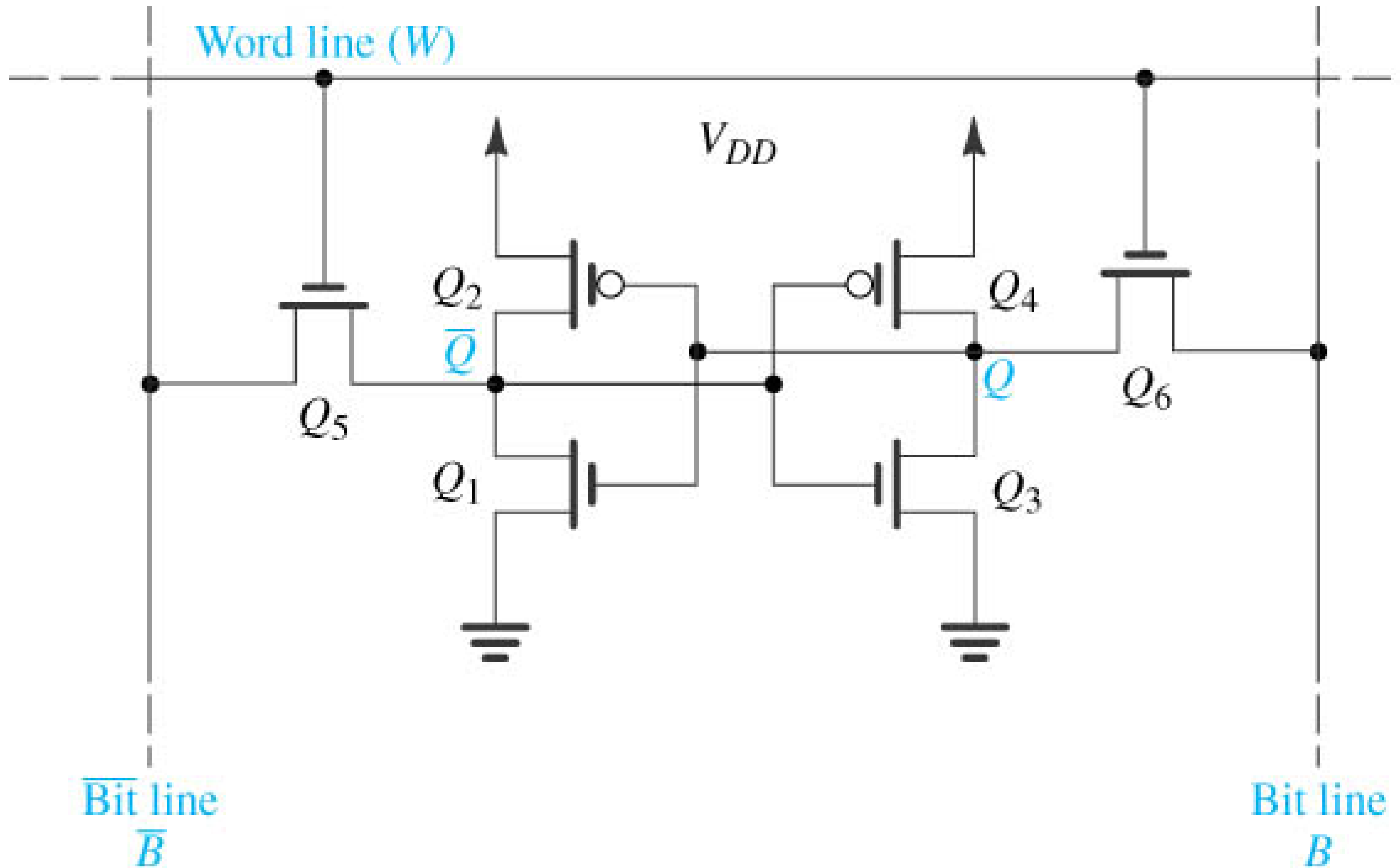


$$I_{\text{estat}} = \frac{1}{2} k_p (V_{DD} - V_t)^2$$

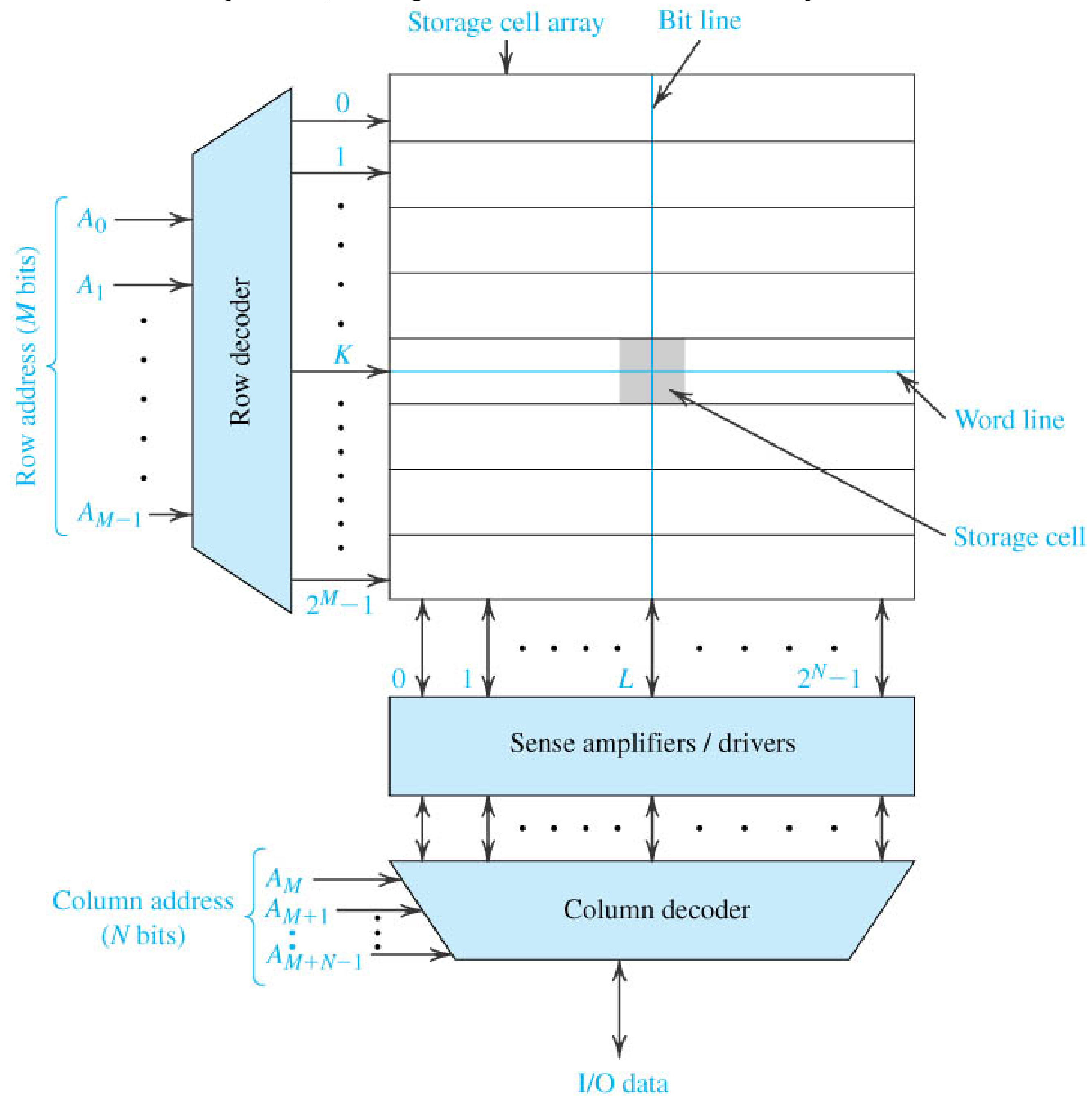
$$MR_H = (V_{DD} - V_t)\left(1 - \frac{2}{\sqrt{3r}}\right)$$

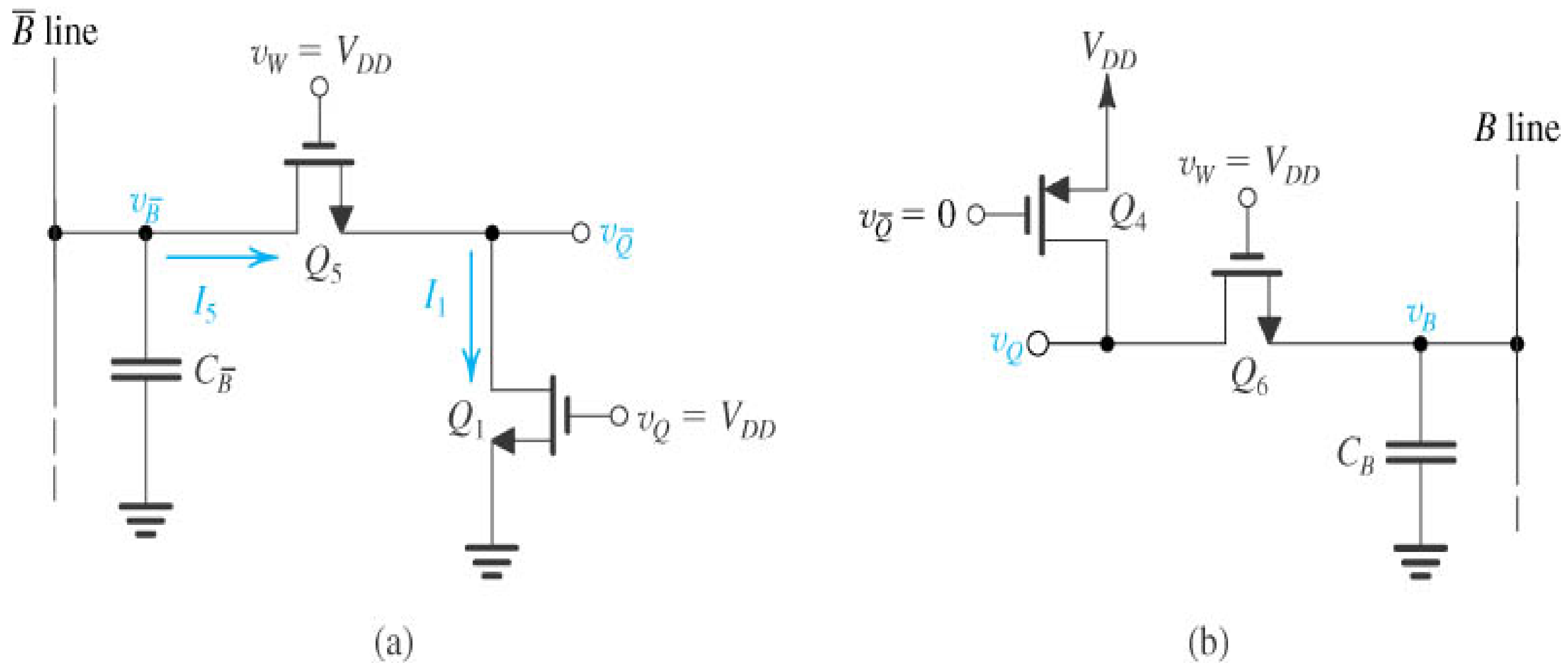
$$MR_L = V_t - (V_{DD} - V_t)\left[1 - \sqrt{1 - \frac{1}{r}} - \frac{1}{\sqrt{r(r+1)}}\right]$$

Célula de Memória SRAM CMOS



- A 2^{M+N}-bit memory chip organized as an array of 2^M rows × 2^N columns.





- **Figure 11.19** Relevant parts of the SRAM cell circuit during a read operation when the cell is storing a logic 1. Note that initially v_Q = V_{DD} and v_Q = 0. Also note that the *B* and *B* lines are usually precharged to a voltage of about $V_{DD}/2$. However, in Example 11.2, it is assumed for simplicity that the precharge voltage is V_{DD}.

EXEMPLO 11.2

A intenção deste exemplo é analisar a operação dinâmica da célula CMOS SRAM da Figura 11.18. Considere a célula sendo fabricada em uma tecnologia de processo para a qual $\mu_n C_{ox} = 50\ \mu A/V^2$, $\mu_p C_{ox} = 20\ \mu A/V^2$, $V_{tn0} = -V_{tp0} = 1$ V, $2\phi_f = 0,6$ V, $\gamma = 0,5\ V^{1/2}$ e $V_{DD} = 5$ V. Suponha que os transistores da célula tenham $(W/L)_n = 4/2$, $(W/L)_p = 10/2$ e suponha os transistores de acesso com $(W/L) = 10/2$. Supondo que a célula esteja armazenando um 1 e que a capacitância de cada linha de bit seja de 1 pF, determine o tempo necessário para surgir uma tensão de 0,2 V. Para simplificar a análise, suponha que as linhas B e $\overline{B}$ estão pré-carregadas em V_{DD}.

$$I_1 = \mu_n C_{ox}\left(\frac{W}{L}\right)_1\left[(V_{DD} - V_{t1})v_{\bar{Q}} - \frac{1}{2}v_{\bar{Q}}^2\right]$$

$$I_1 = 50 \times \frac{4}{2}\left[(5 - 1)v_{\bar{Q}} - \frac{1}{2}v_{\bar{Q}}^2\right]$$

$$I_5 = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_5(V_{DD} - v_{\bar{Q}} - V_{t5})^2$$

$$V_{t5} = 1 + 0{,}5\,(\sqrt{v_{\bar{Q}} + 0{,}6} - \sqrt{0{,}6})$$

$V_{t5} = 1$ V e, portanto, I_5 será

$$I_5 = \frac{1}{2} \times 50 \times \frac{10}{2}(5 - v_{\bar{Q}} - 1)^2$$

resolvendo para $v_{\bar{Q}}$ resulta em $v_{\bar{Q}} = 1{,}86$ V

segunda iteração,

O resultado é $V_{t5} = 1,4$ V.

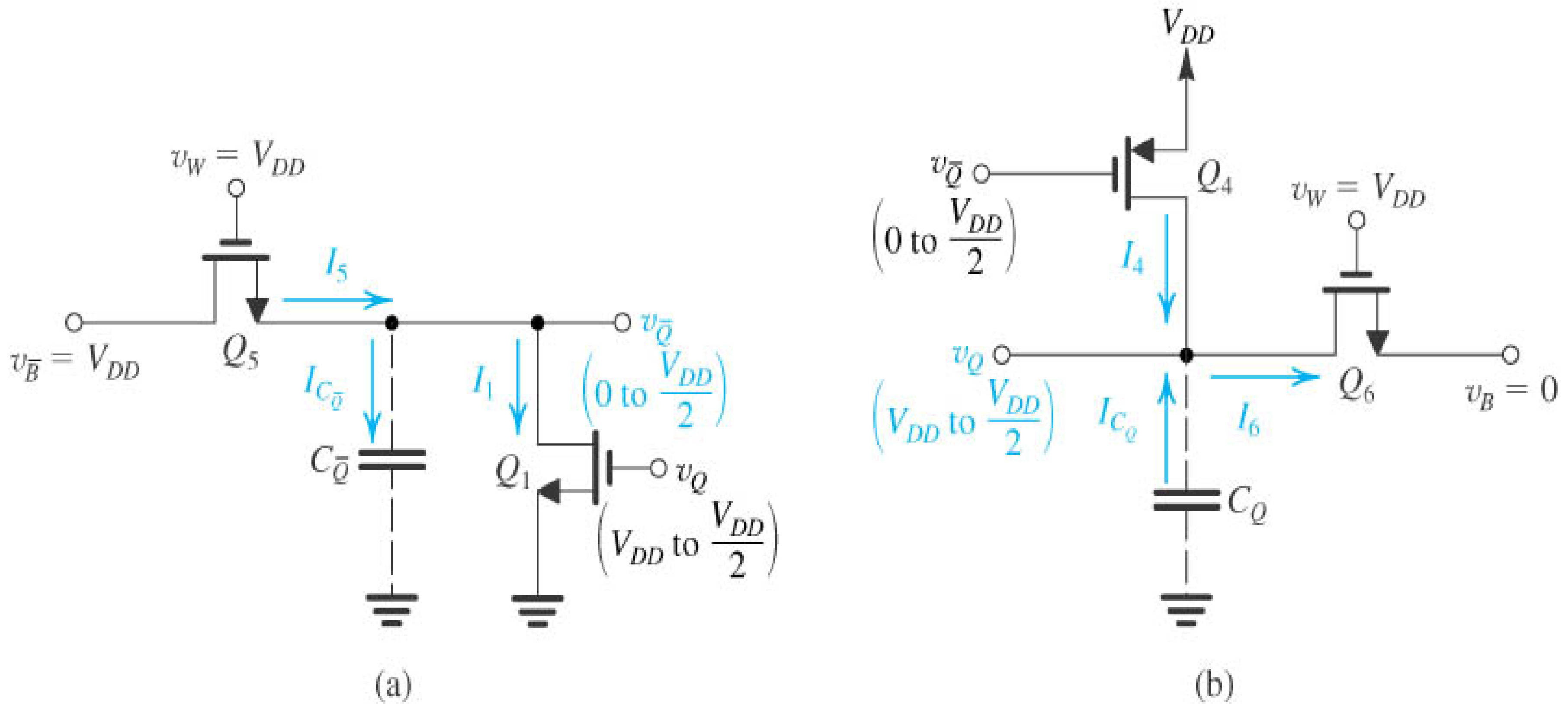
$$v_{\overline{Q}} = 1,6 \text{ V}$$

$$I_5 = 0,5 \text{ mA}$$

$v_{\overline{Q}}$ é menor que $V_{DD}/2$

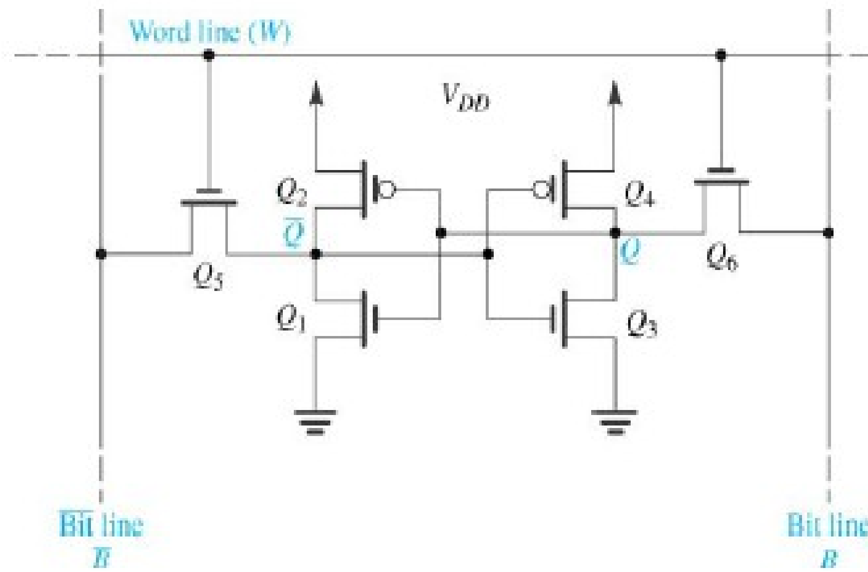
$$\Delta t = \frac{C_{\overline{B}} \Delta V}{I_5}$$

$$\Delta t = \frac{1 \times 10^{-12} \times 0,2}{0,5 \times 10^{-3}} = 0,4 \text{ ns}$$



- **Figure 11.20** Relevant parts of the SRAM circuit during a write operation. Initially, the SRAM has a stored 1 and a 0 is being written. These equivalent circuits apply before switching takes place. **(a)** The circuit is pulling node $\bar{Q}$ up toward $V_{DD}/2$. **(b)** The circuit is pulling node Q down toward $V_{DD}/2$.

Para a célula de memória SRAM na figura a seguir, as linhas B e $\overline{B}$ são energizadas com $V_{DD}/2$ durante o ciclo de leitura e os transistores Q_5 e Q_6 são habilitados através da aplicação de uma tensão V_{DD} na *Word line* (W) quando passamos a ter $v_Q = 3{,}75$ V e $v_{\overline{Q}} = 1{,}25$ V. Determine as correntes $I_5 = I_1$ e $I_4 = I_6$ e obtenha o intervalo de tempo Δt necessário para que a diferença de potencial ΔV entre as linhas B e $\overline{B}$ seja de 0,2V a fim de ativar o amplificador sensor de leitura supondo que as correntes $I_5 = I_1$ e $I_4 = I_6$ permaneçam aproximadamente constantes. Suponha que o efeito de corpo nos transistores Q_5 e Q_6 seja desprezível, ou seja, a tensão de limiar não muda ($V_{tn} = 1V$).



Dados:

$V_{DD} = 5$ V

$k_p' = 10\ \mu A/V^2$ (20 μA/V²)

$k_n' = 20\ \mu A/V^2$ (40 μA/V²)

$|V_{tp}| = |V_{tn}| = 1V$

$\lambda = 0$

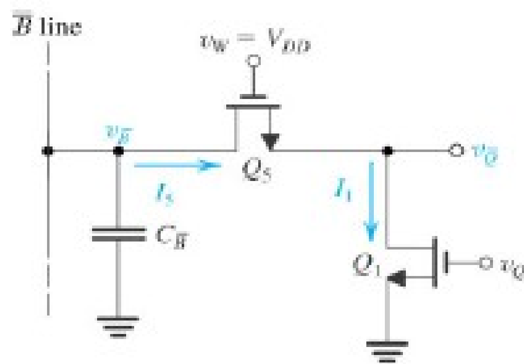
$(W/L)_{Q4} = 6$

$(W/L)_{Q6} = 3$

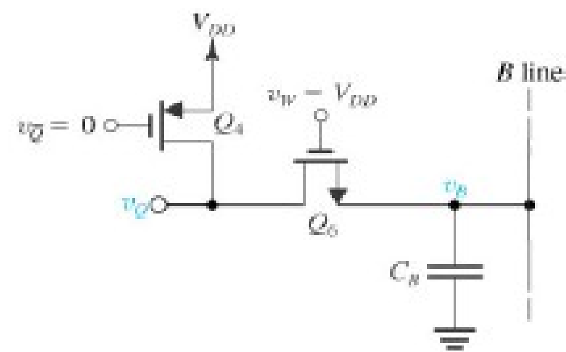
$(W/L)_{Q5} = 3$

$(W/L)_{Q1} = 3$

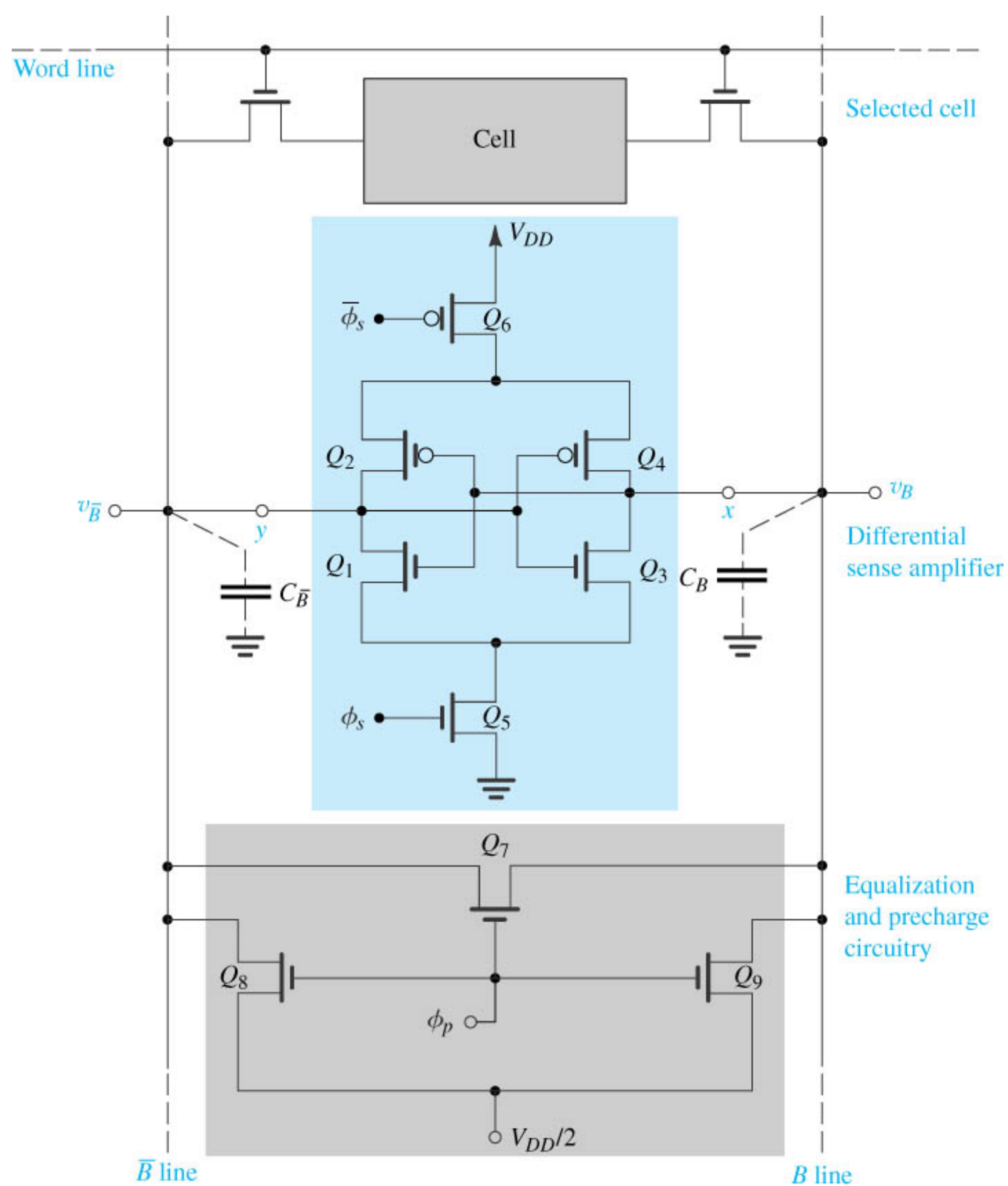
$C_B = C_{\overline{B}} = 1pF$



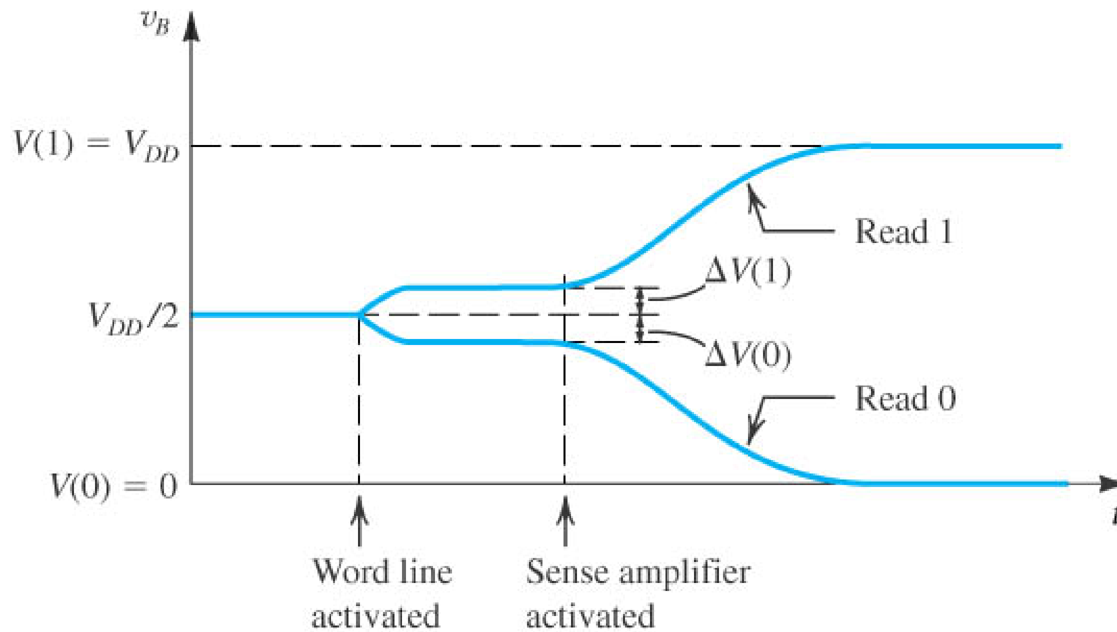
(a)



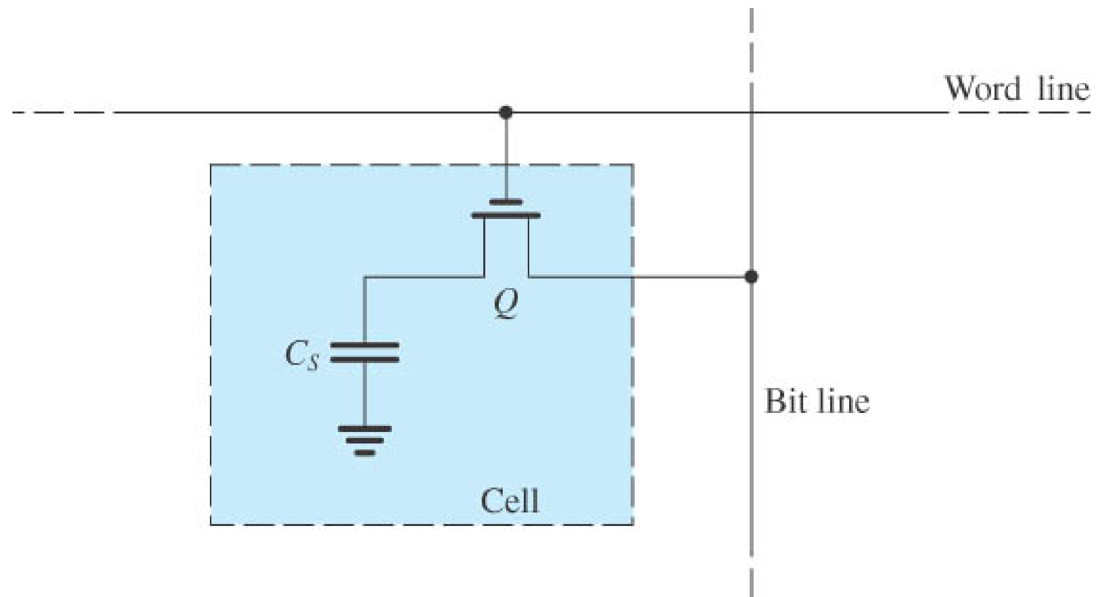
(b)



- **Figure 11.23** A differential sense amplifier connected to the bit lines of a particular column. This arrangement can be used directly for SRAMs (which utilize both the B and $\overline{B}$ lines). DRAMs can be turned into differential circuits by using the "dummy cell" arrangement shown in Fig. 11.25.

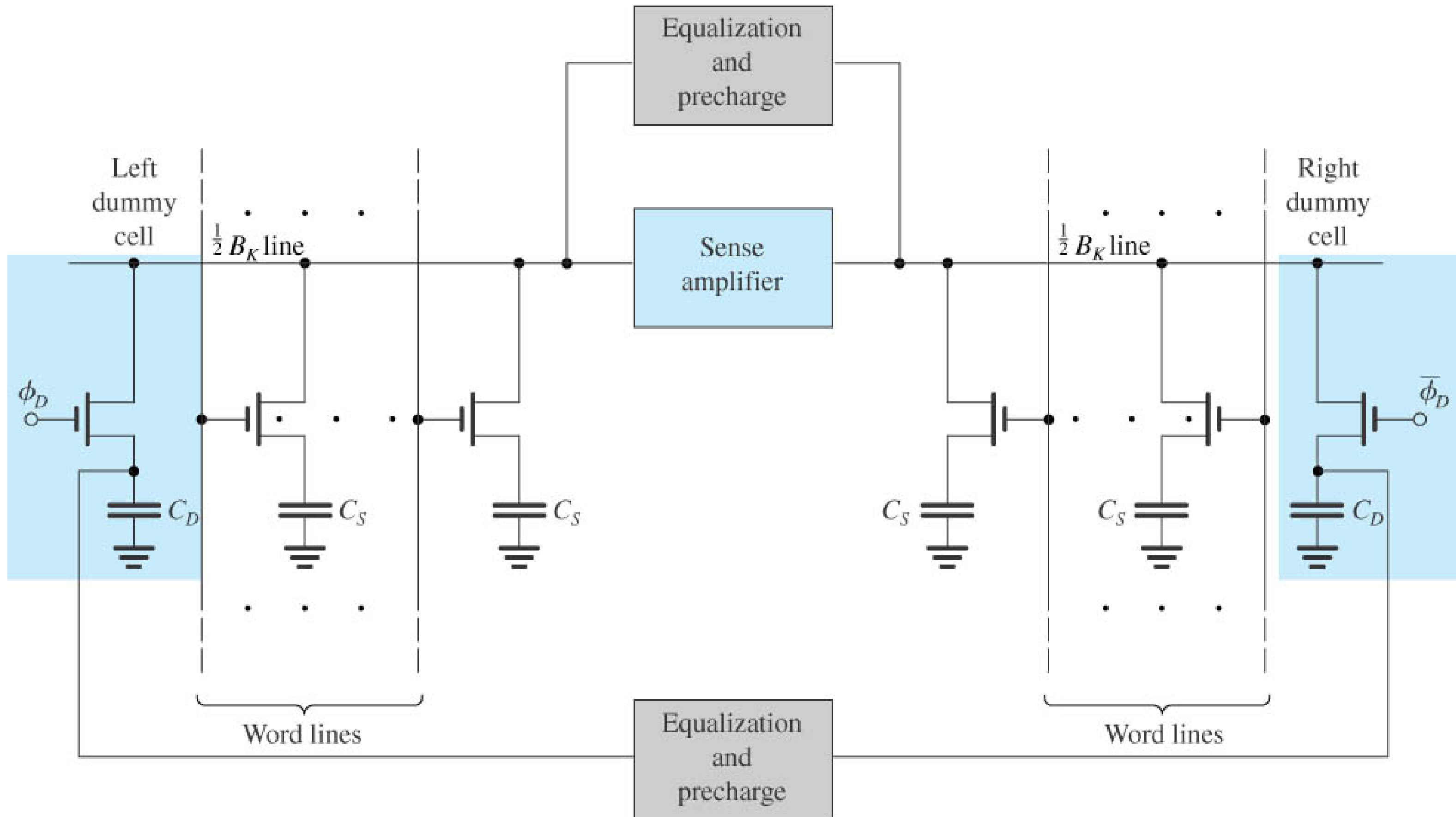


- **Figure 11.24** Waveforms of v_B before and after the activation of the sense amplifier. In a read-1 operation, the sense amplifier causes the initial small increment $\Delta V(1)$ to grow exponentially to V_{DD}. In a read-0 operation, the negative $\Delta V(0)$ grows to 0. Complementary signal waveforms develop on the $\bar{B}$ line.



- **Figure 11.21** The one-transistor dynamic RAM cell.

- **Figure 11.22** When the voltage of the selected word line is raised, the transistor conducts, thus connecting the storage capacitor C_S to the bit-line capacitance C_B.



- **Figure 11.25** An arrangement for obtaining differential operation from the single-ended DRAM cell. Note the dummy cells at the far right and far left.