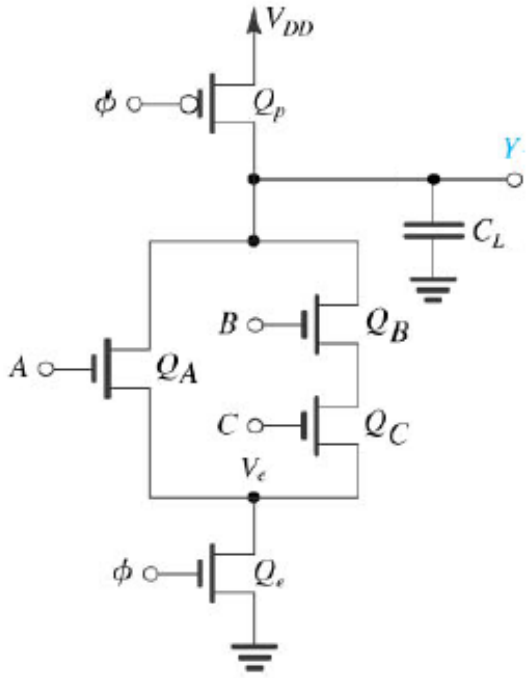
PSI3024 – Eletrônica

Aula 35

2023

Teste 15 - 2° semestre de 2023

Para a porta lógica dinâmica mostrada na figura a seguir, determine o tempo de atraso máximo da mesma considerando as razões W/L fornecidas para os transistores Q_P, Q_A, Q_B e Q_C. Sabe-se que a razão W/L do transistor Q_e é elevada e que $V_e \cong 0$ V quando o mesmo está habilitado para $\phi = V_{DD}$.
Calcule na condição de maior atraso o valor de $i_{DNmedio} = (i_{DN}(0) + i_{DN}(t_P))/2$.

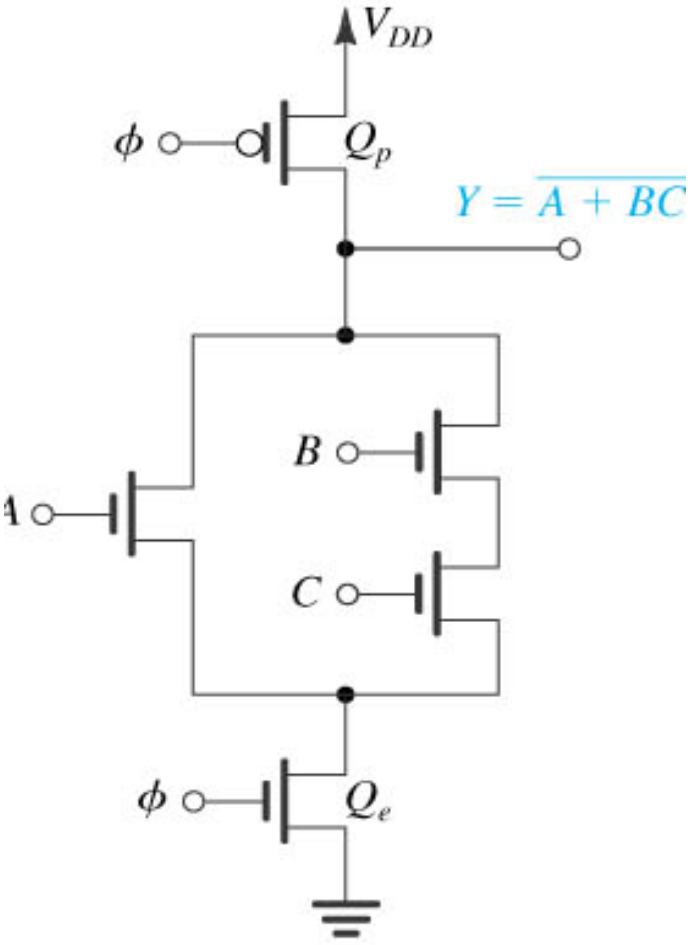


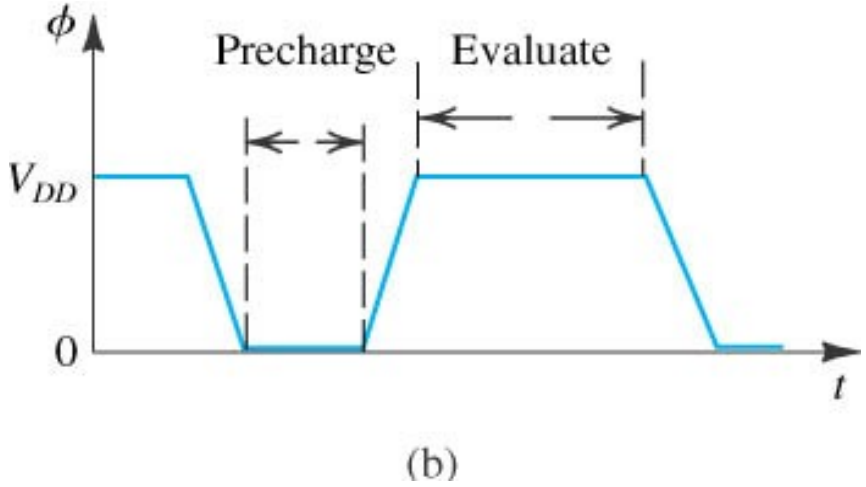
Dados:

$V_{DD} = 5$ V
$k_p' = 100$ nA/V^2
$k_n' = 200$ nA/V^2
$|V_{tp}| = |V_{tn}| = 1$V
$\lambda = 0$
$V_e \cong 0$ V p/ $\phi = V_{DD}$
$(W/L)_{Qp} = 6$
$(W/L)_{QA} = 3$
$(W/L)_{QB} = 6$
$(W/L)_{QC} = 6$
$C_L = 446{,}25$ fF

Dados:

$V_{DD} = 5$ V
$k_p' = 200$ nA/V^2
$k_n' = 400$ nA/V^2
$|V_{tp}| = |V_{tn}| = 1$V
$\lambda = 0$
$V_e \cong 0$ V p/ $\phi = V_{DD}$
$(W/L)_{Qp} = 6$
$(W/L)_{QA} = 3$
$(W/L)_{QB} = 6$
$(W/L)_{QC} = 6$
$C_L = 446{,}25$ fF





- **Figure 10.33 (a)** Basic structure of dynamic-MOS logic circuits. **(b)** Waveform of the clock needed to operate the dynamic logic circuit. **(c)** An example circuit.

EXEMPLO 10.3

Considere o inversor pseudo-NMOS fabricado na tecnologia CMOS especificada no Exemplo 10.1, ou seja, $\mu_n C_{ox} = 115\ \mu A/V^2$, $\mu_p C_{ox} = 30\ \mu A/V^2$, $V_{tn} = -V_{tp} = 0{,}4$ V e $V_{DD} = 2{,}5$ V. Seja a razão W/L de Q_N de (0,375 μm/0,25 μm) e $r = 9$. Obtenha:

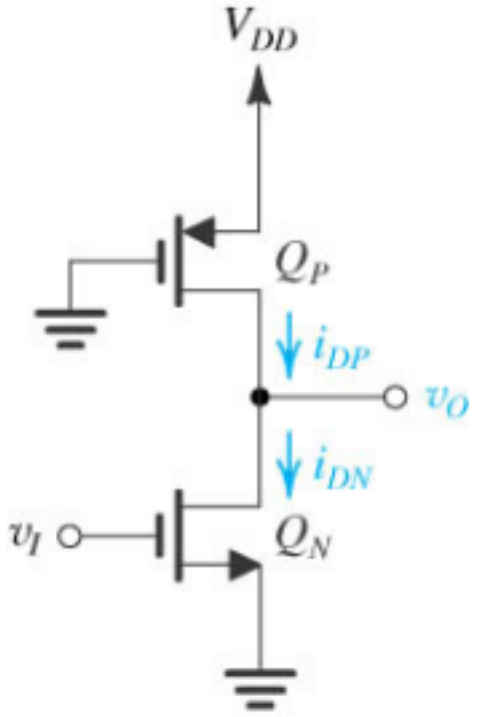
(a) V_{OH}, V_{OL}, V_{IL}, V_{IH}, V_M, MR_H e MR_L

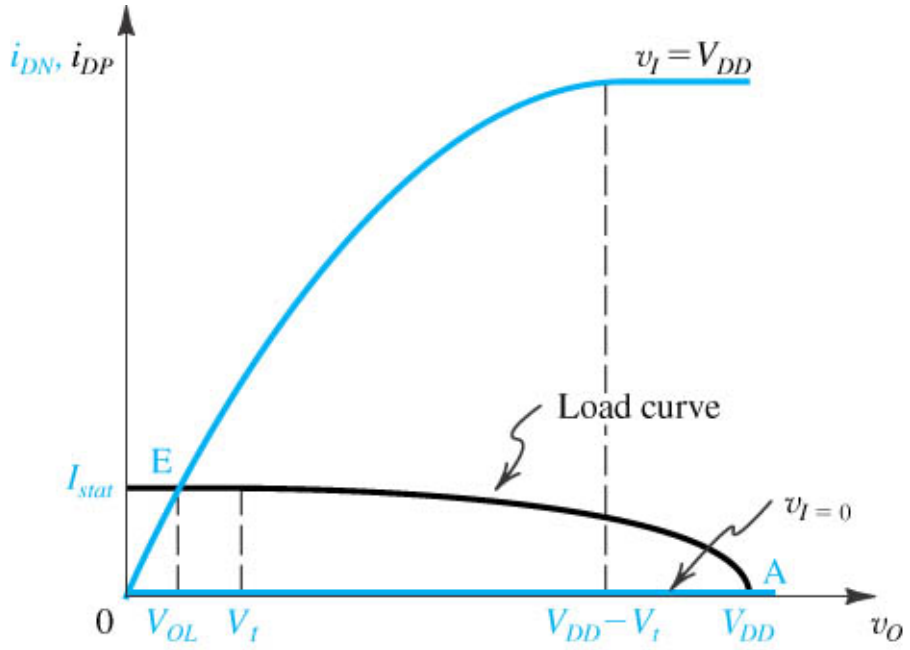
(b) $(W/L)_p$

(c) I_{estat} e P_D

(d) t_{PLH}, t_{PHL} e t_P, supondo uma capacitância total na saída do inversor de 7 fF

Inversor pseudo-NMOS





Região II (segmento BC)

$$k_n = rk_p,$$

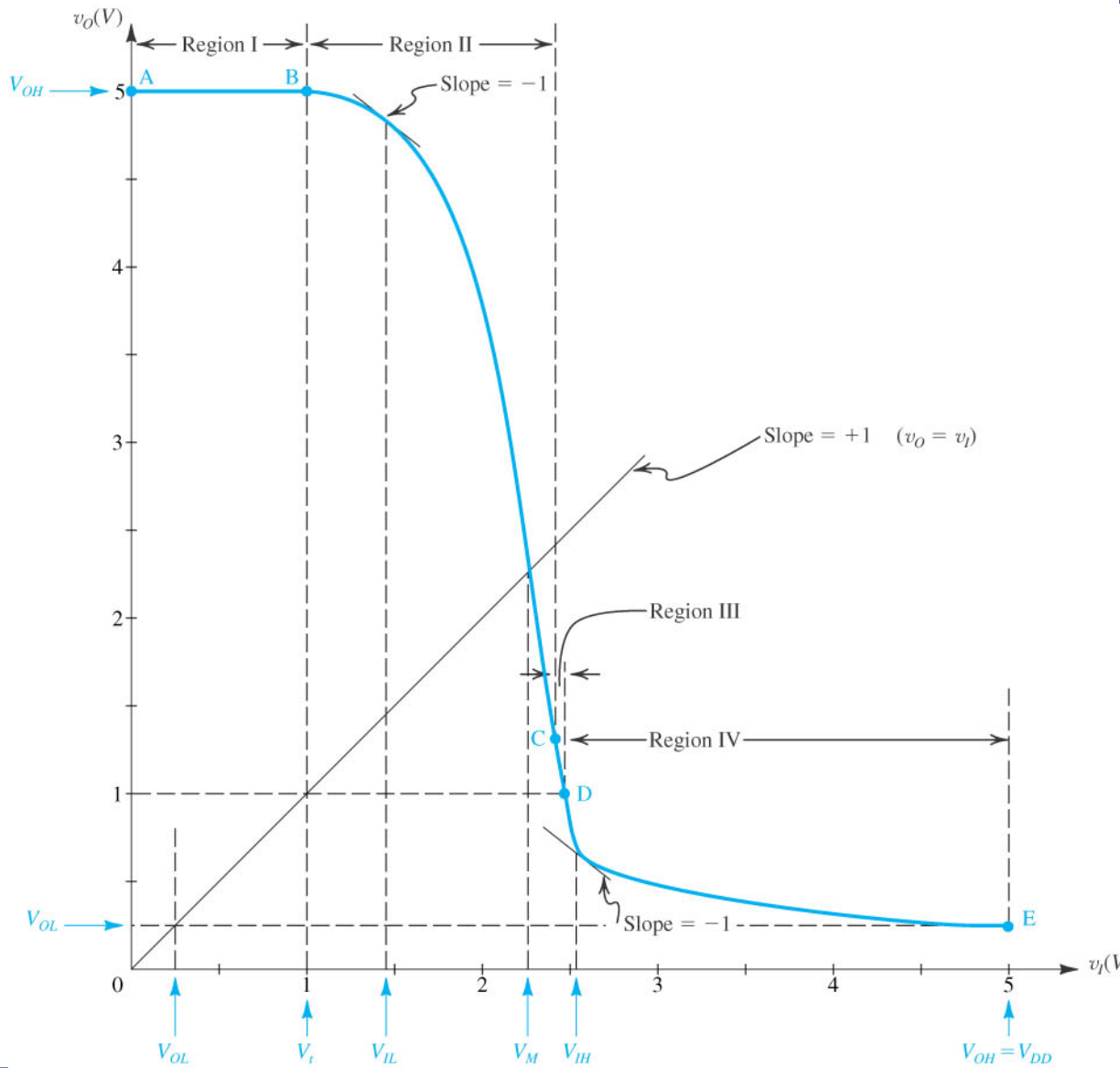
$$v_O = V_t + \sqrt{(V_{DD} - V_t)^2 - r(v_I - V_t)^2}$$

$$V_{IL} = V_t + \frac{V_{DD} - V_t}{\sqrt{r(r+1)}}$$

$$V_M = V_t + \frac{V_{DD} - V_t}{\sqrt{r+1}}$$

(ponto C)

$$v_O = v_I - V_t$$



Região IV (segmento DE)

$$v_O = (v_I - V_t) - \sqrt{(v_I - V_t)^2 - \frac{1}{r}(V_{DD} - V_t)^2}$$

$$k_n = rk_p$$

Região III (segmento CD)

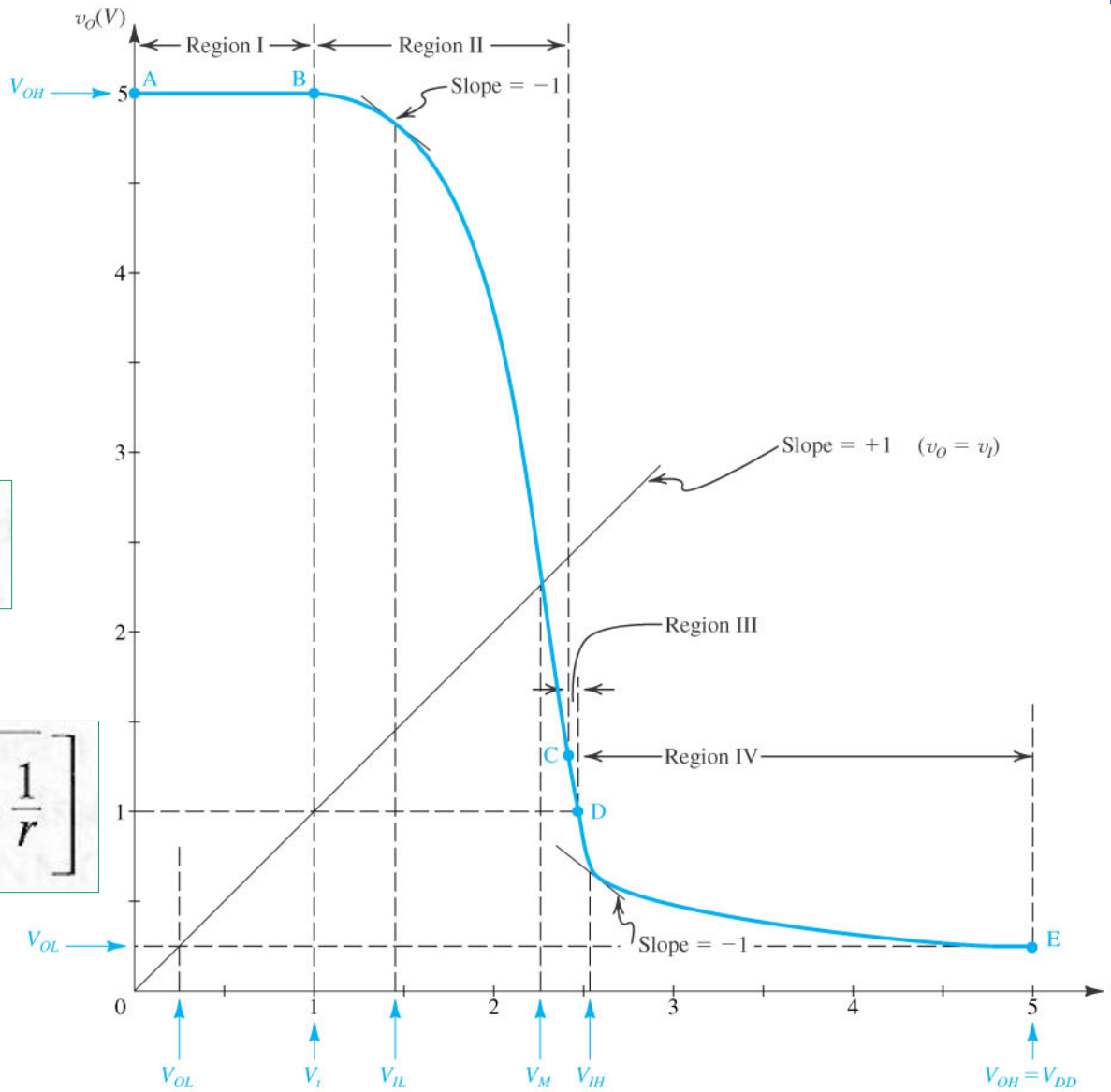
ponto D $\quad v_O = V_t.$

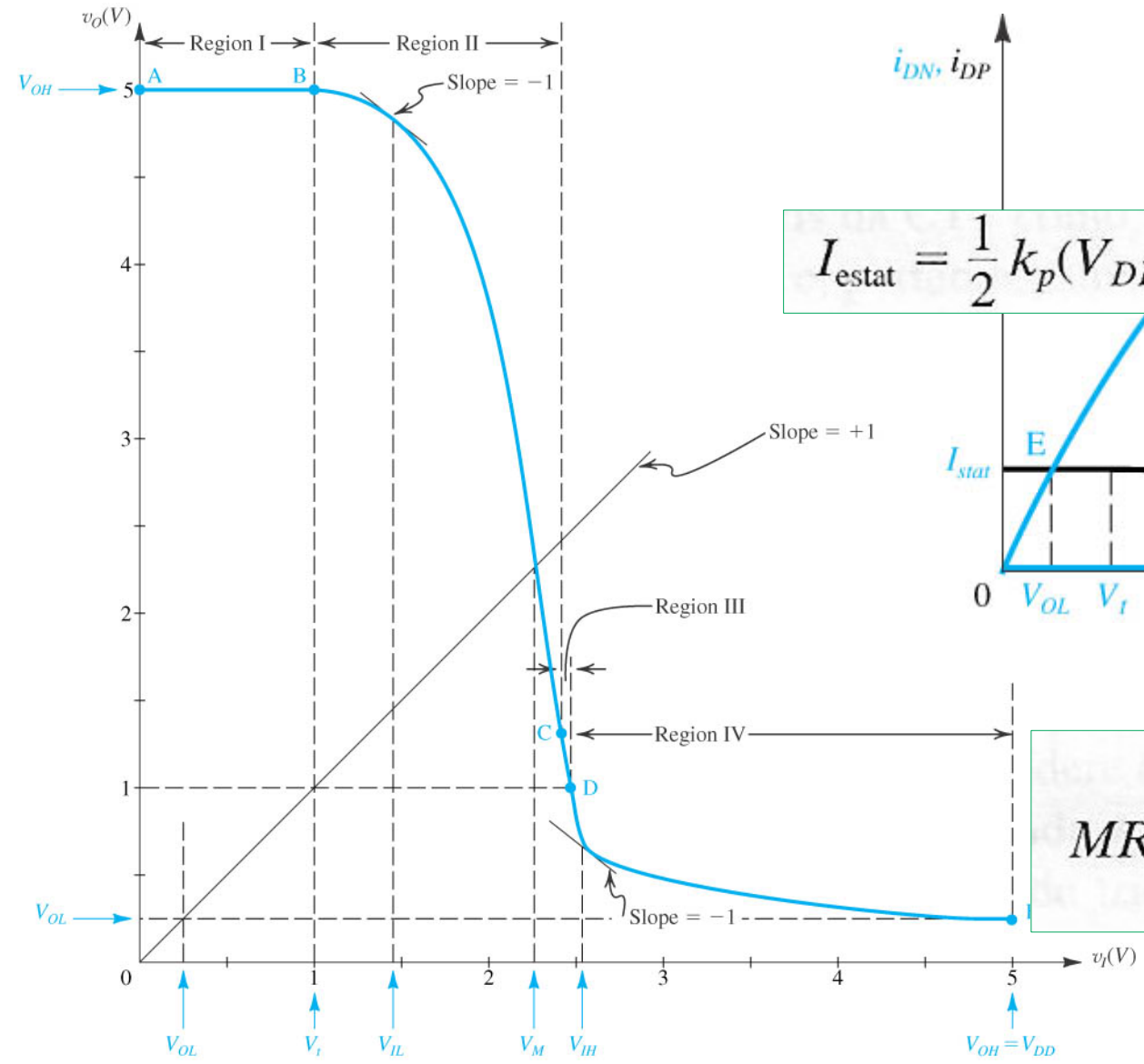
$$\partial v_O/\partial v_I = -1 \text{ e } v_1 = V_{IH},$$

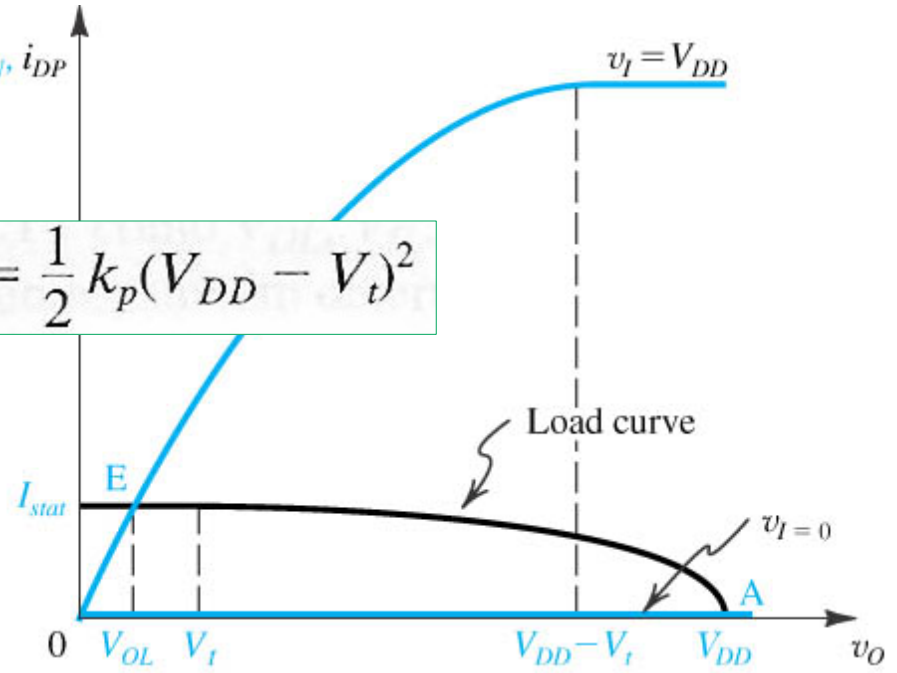
$$V_{IH} = V_t + \frac{2}{\sqrt{3r}}(V_{DD} - V_t)$$

$$v_I = V_{DD}$$

$$V_{OL} = (V_{DD} - V_t)\left[1 - \sqrt{1 - \frac{1}{r}}\right]$$





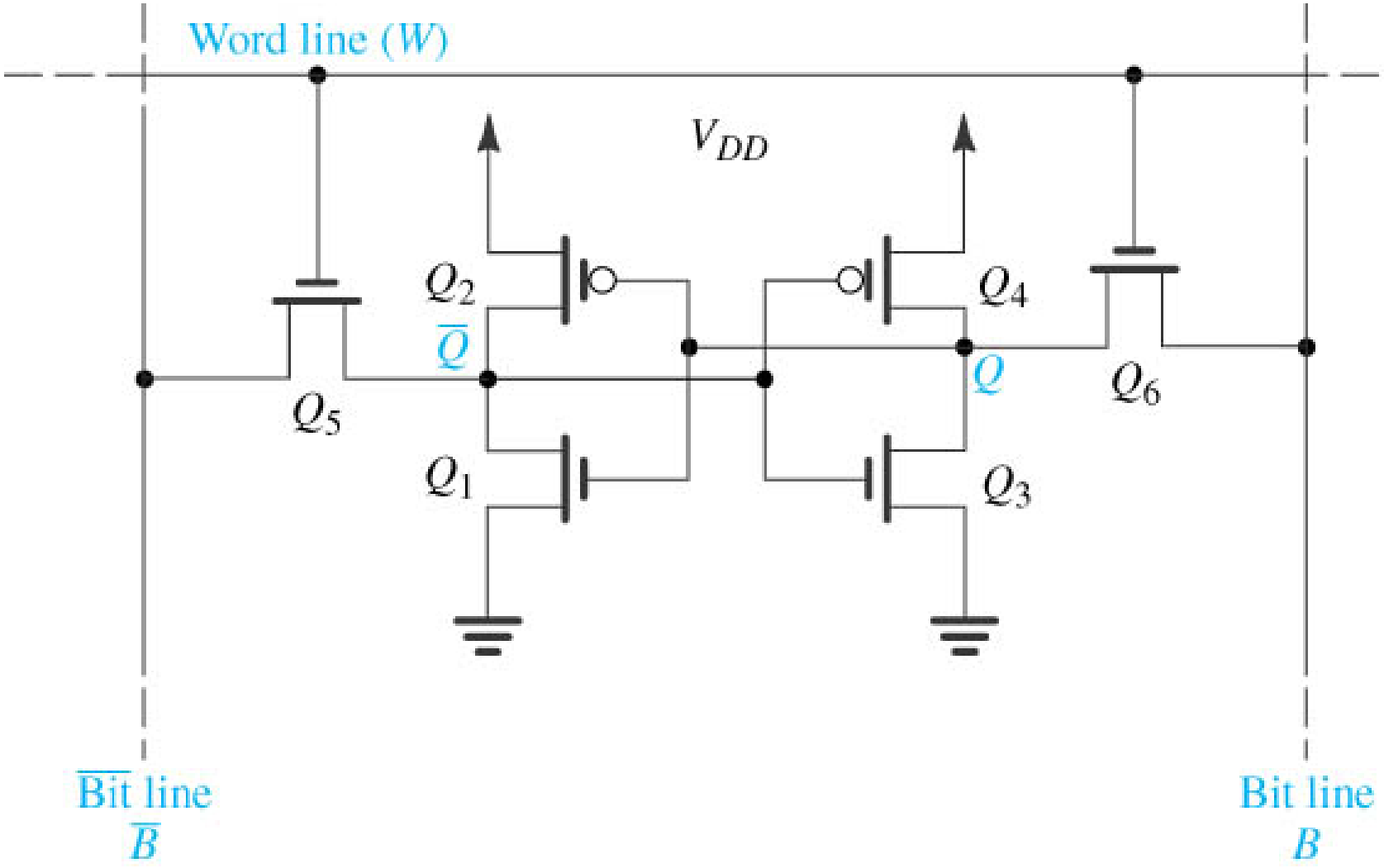


$$I_{\text{estat}} = \frac{1}{2} k_p (V_{DD} - V_t)^2$$

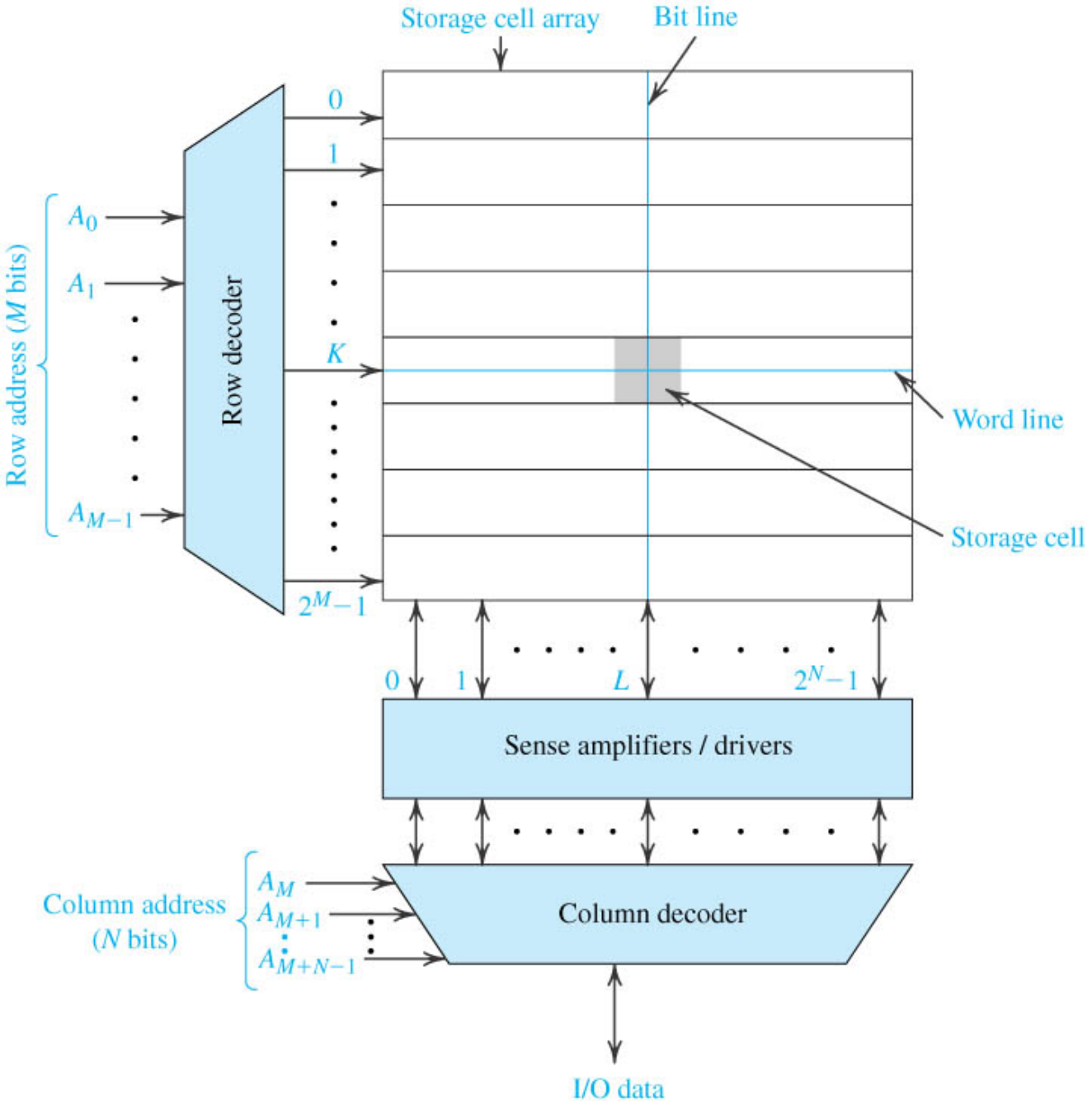
$$MR_H = (V_{DD} - V_t\left(1 - \frac{2}{\sqrt{3r}}\right)$$

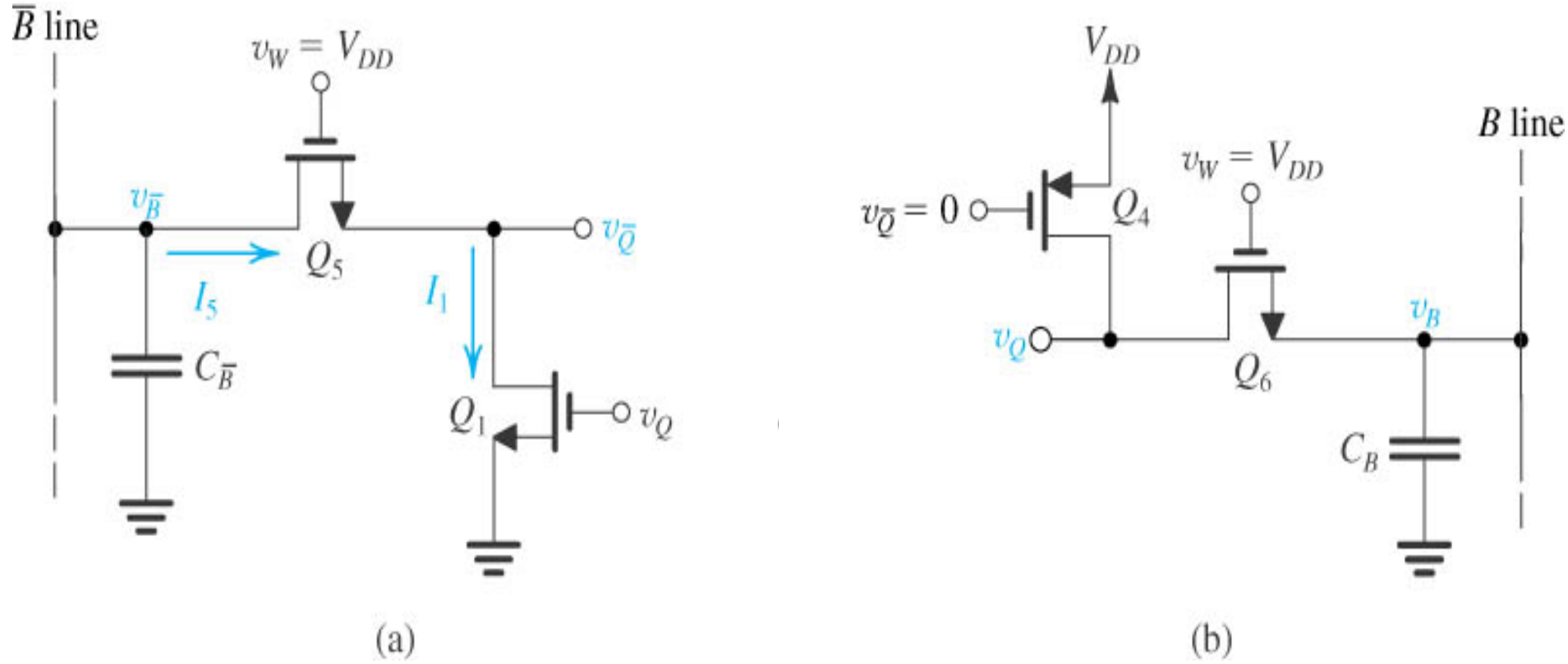
$$MR_L = V_t - (V_{DD} - V_t)\left[1 - \sqrt{1 - \frac{1}{r} - \frac{1}{\sqrt{r(r+1)}}}\right]$$

Célula de Memória SRAM CMOS



- A 2^{M+N}-bit memory chip organized as an array of 2^M rows $\times$ 2^N columns.





- **Figure 11.19** Relevant parts of the SRAM cell circuit during a read operation when the cell is storing a logic 1. Note that initially $v_{\overline{Q}} = V_{DD}$ and $v_Q = 0$. Also note that the B and $\overline{B}$ lines are usually precharged to a voltage of about $V_{DD}/2$. However, in Example 11.2, it is assumed for simplicity that the precharge voltage is V_{DD}.