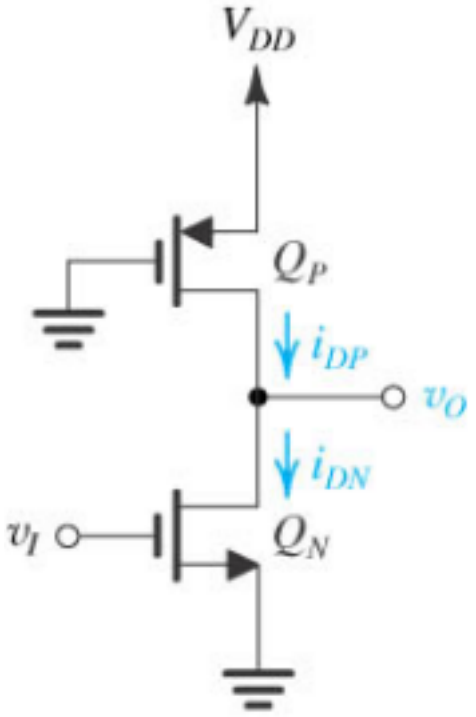
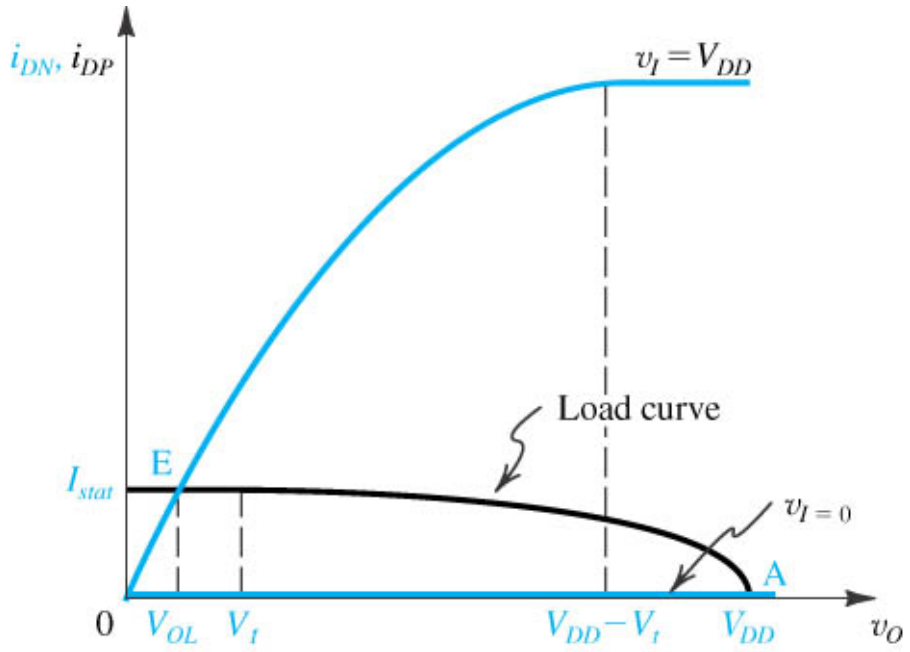
PSI3024 – Eletrônica

Aulas 33 e 34

2023

Inversor pseudo-NMOS





EXEMPLO 10.3

Considere o inversor pseudo-NMOS fabricado na tecnologia CMOS especificada no Exemplo 10.1, ou seja, $\mu_n C_{ox} = 115\ \mu A/V^2$, $\mu_p C_{ox} = 30\ \mu A/V^2$, $V_{tn} = -V_{tp} = 0{,}4$ V e $V_{DD} = 2{,}5$ V. Seja a razão W/L de Q_N de (0,375 μm/0,25 μm) e $r = 9$. Obtenha:

(a) V_{OH}, V_{OL}, V_{IL}, V_{IH}, V_M, MR_H e MR_L

(b) $(W/L)_p$

(c) I_{estat} e P_D

(d) t_{PLH}, t_{PHL} e t_P, supondo uma capacitância total na saída do inversor de 7 fF

Região II (segmento BC)

$$k_n = rk_p,$$

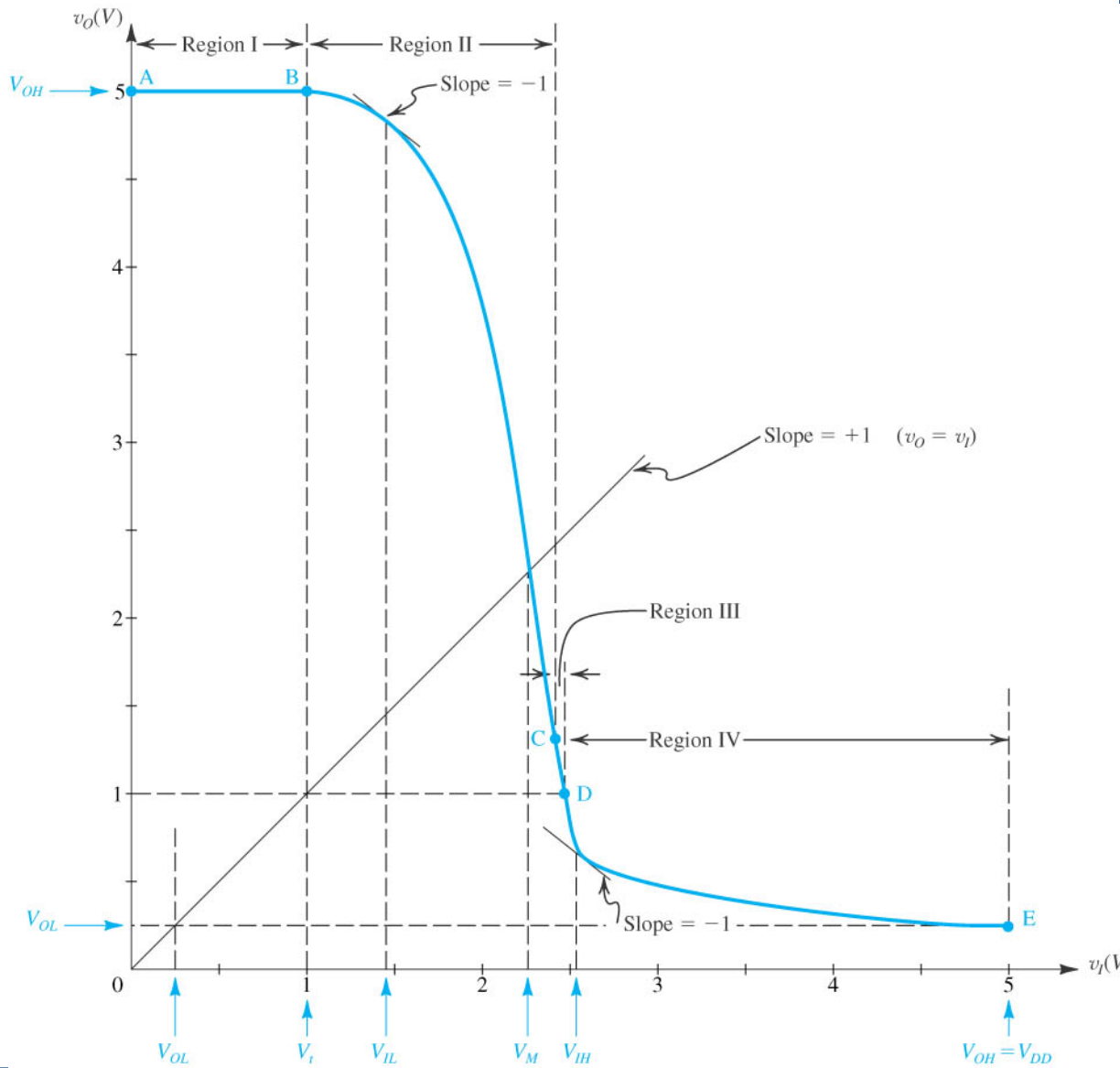
$$v_O = V_t + \sqrt{(V_{DD} - V_t)^2 - r(v_I - V_t)^2}$$

$$V_{IL} = V_t + \frac{V_{DD} - V_t}{\sqrt{r(r+1)}}$$

$$V_M = V_t + \frac{V_{DD} - V_t}{\sqrt{r+1}}$$

(ponto C)

$$v_O = v_I - V_t$$



Região IV (segmento DE)

$$v_O = (v_I - V_t) - \sqrt{(v_I - V_t)^2 - \frac{1}{r}(V_{DD} - V_t)^2}$$

$$k_n = rk_p$$

Região III (segmento CD)

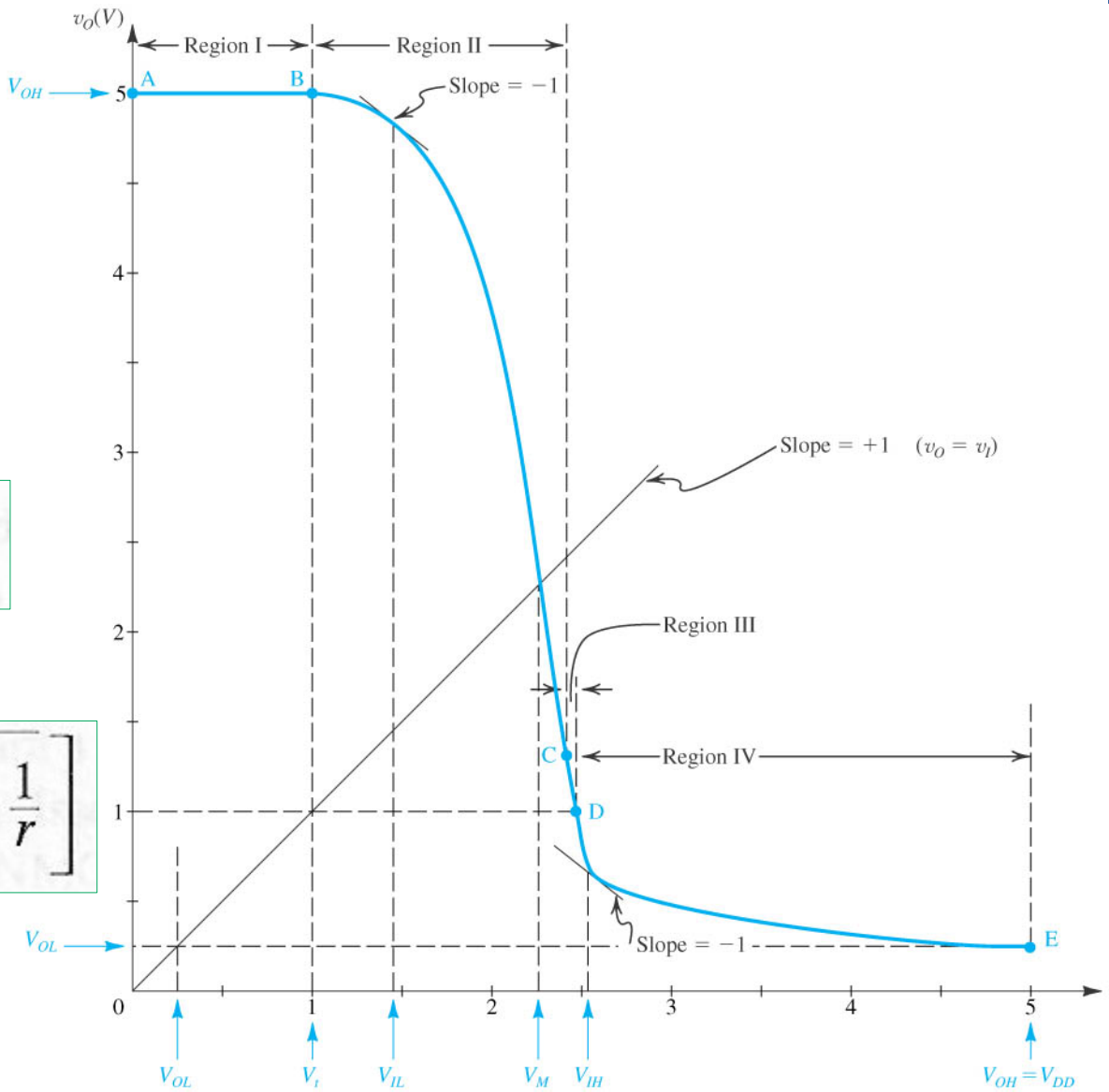
ponto D $v_O = V_t$.

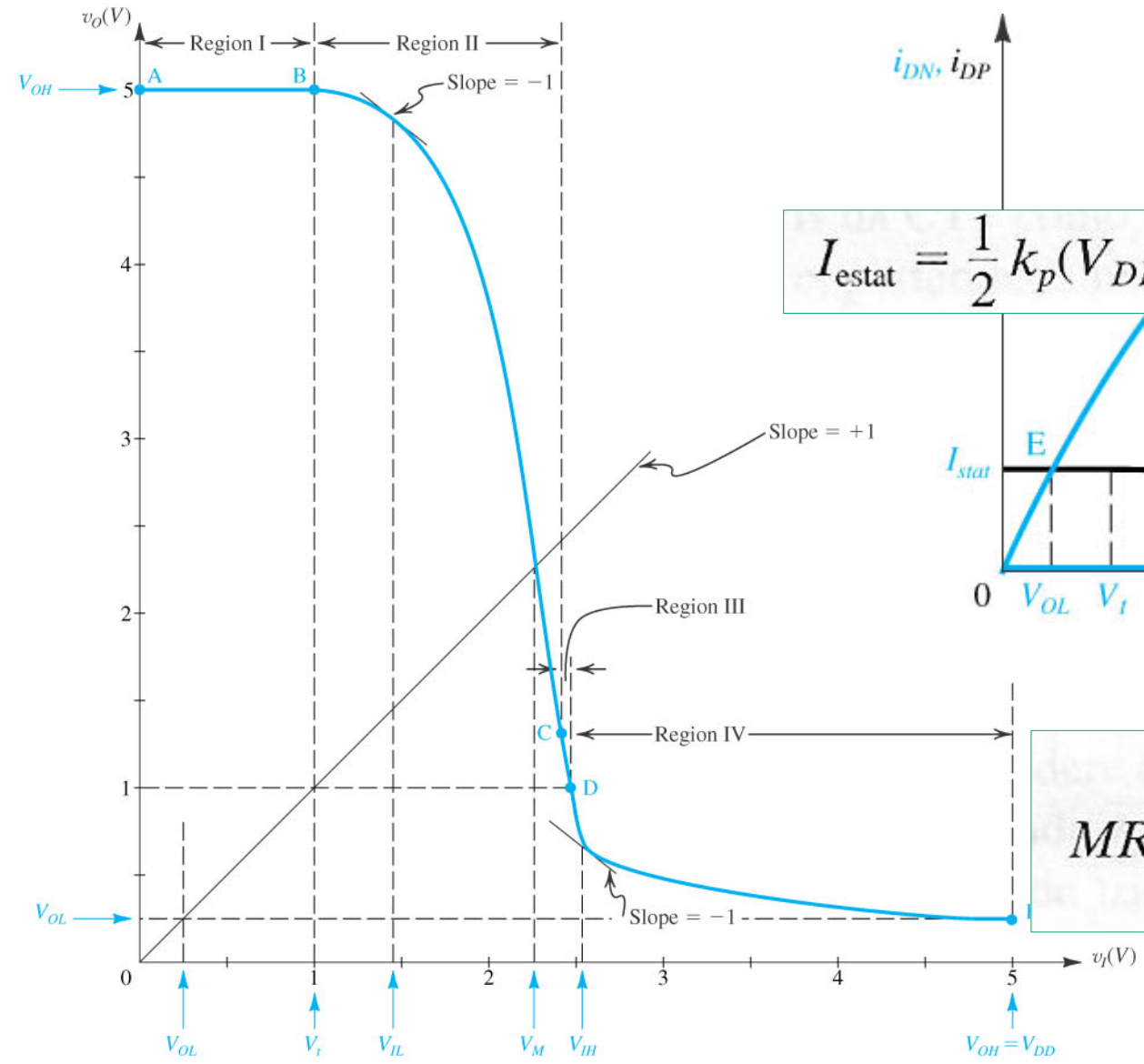
$$\partial v_O/\partial v_I = -1 \text{ e } v_1 = V_{IH},$$

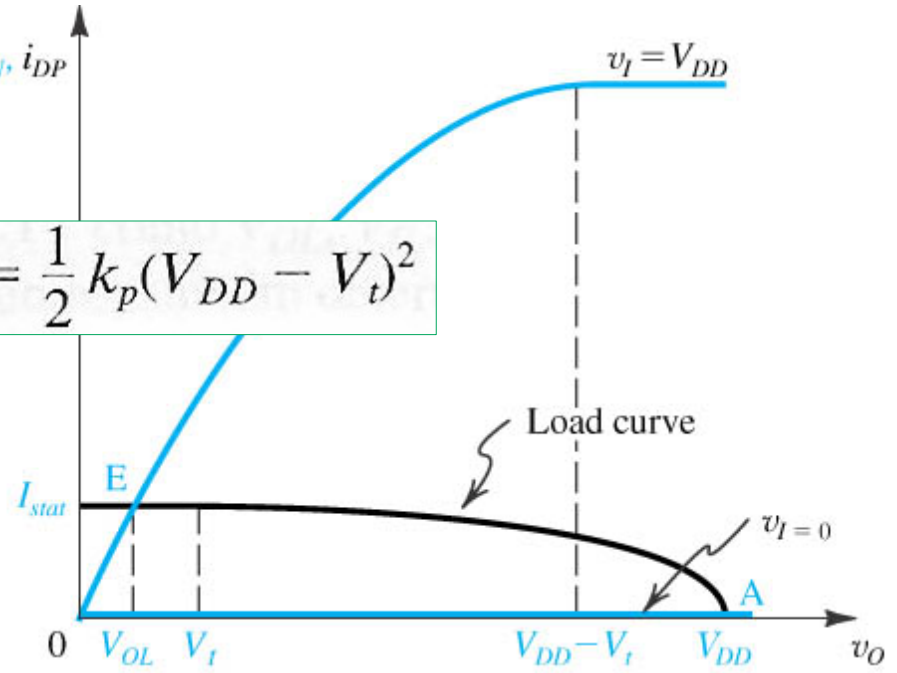
$$V_{IH} = V_t + \frac{2}{\sqrt{3r}}(V_{DD} - V_t)$$

$$v_I = V_{DD}$$

$$V_{OL} = (V_{DD} - V_t)\left[1 - \sqrt{1 - \frac{1}{r}}\right]$$





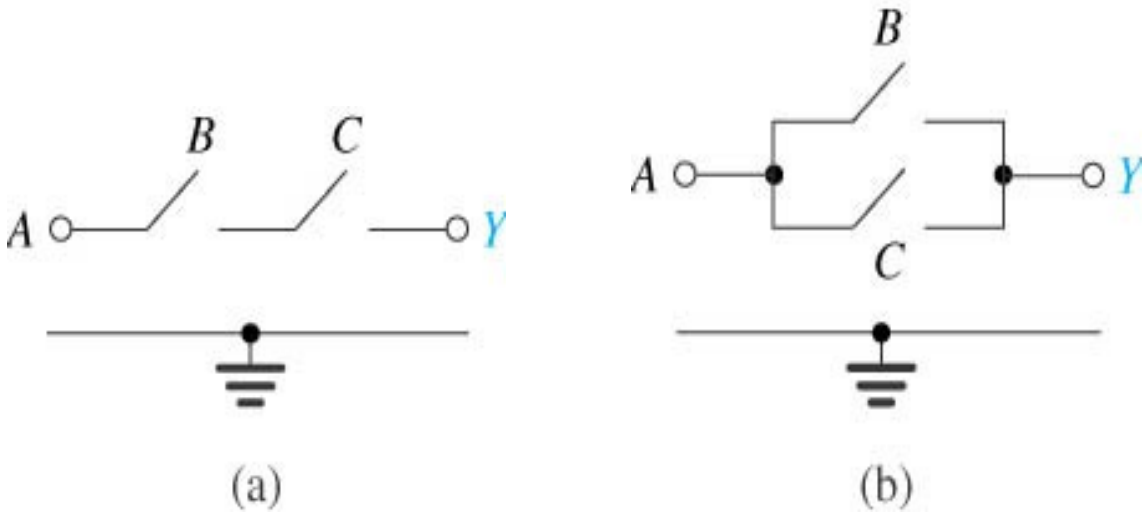


$$I_{\text{estat}} = \frac{1}{2} k_p (V_{DD} - V_t)^2$$

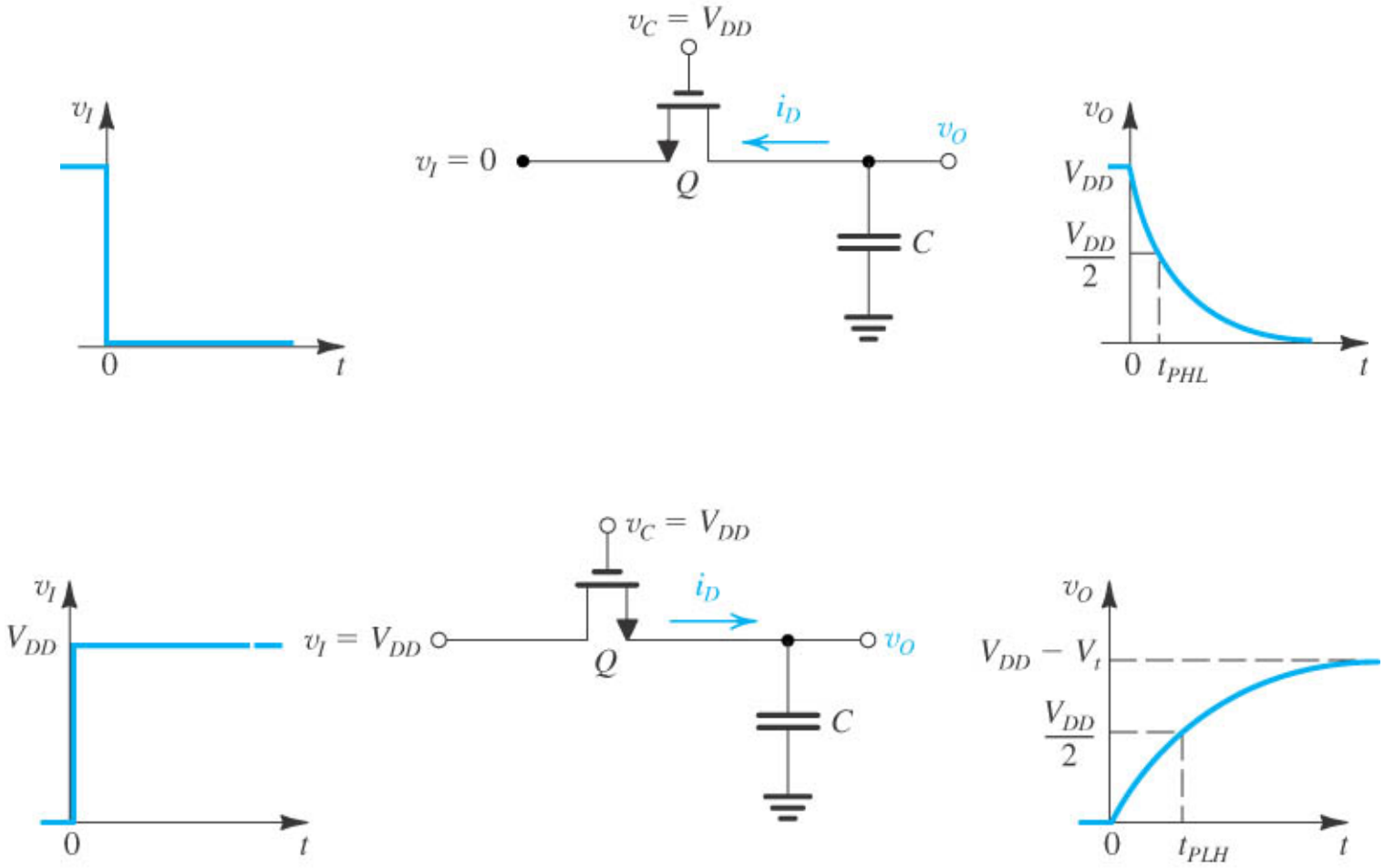
$$MR_H = (V_{DD} - V_t\left(1 - \frac{2}{\sqrt{3r}}\right)$$

$$MR_L = V_t - (V_{DD} - V_t)\left[1 - \sqrt{1 - \frac{1}{r} - \frac{1}{\sqrt{r(r+1)}}}\right]$$

Portas Lógicas com transistores de passagem

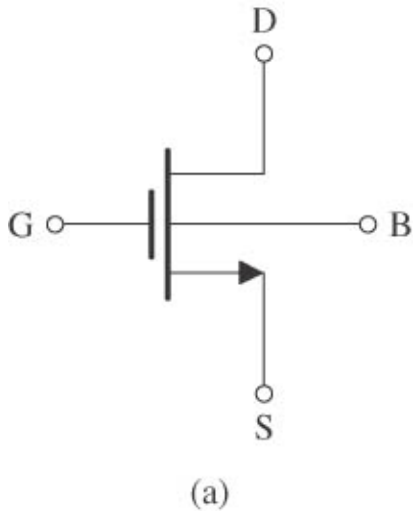


- **Figure 10.23** Conceptual pass-transistor logic gates. **(a)** Two switches, controlled by the input variables *B* and *C*, when connected in series in the path between the input node to which an input variable *A* is applied and the output node (with an implied load to ground) realize the function $Y = ABC$. **(b)** When the two switches are connected in parallel, the function realized is $Y = A(B + C)$.

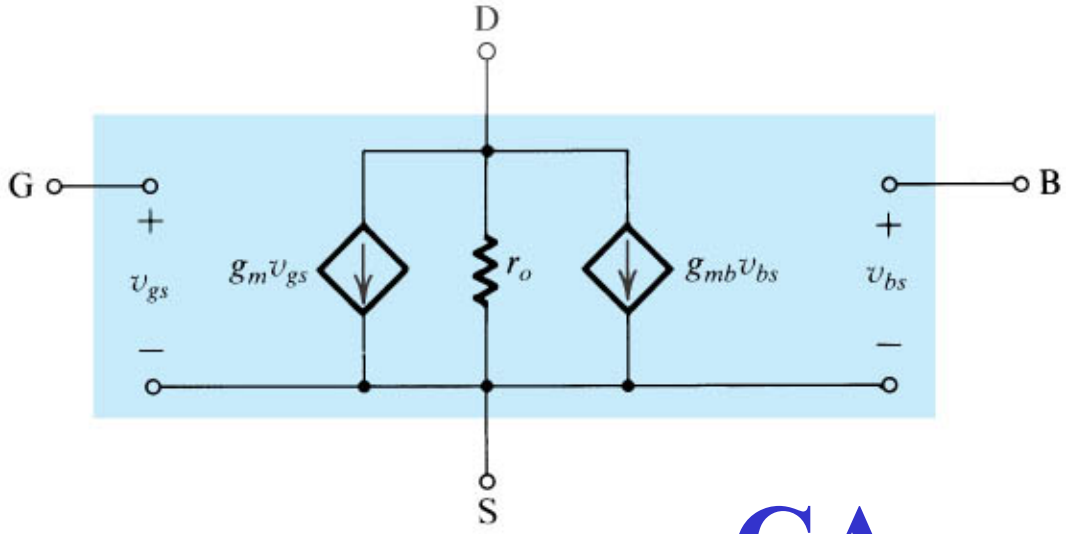


- **Figure 10.27 e 10.28 – Transistor NMOS como chave de passagem** .

Efeito de corpo



(a)



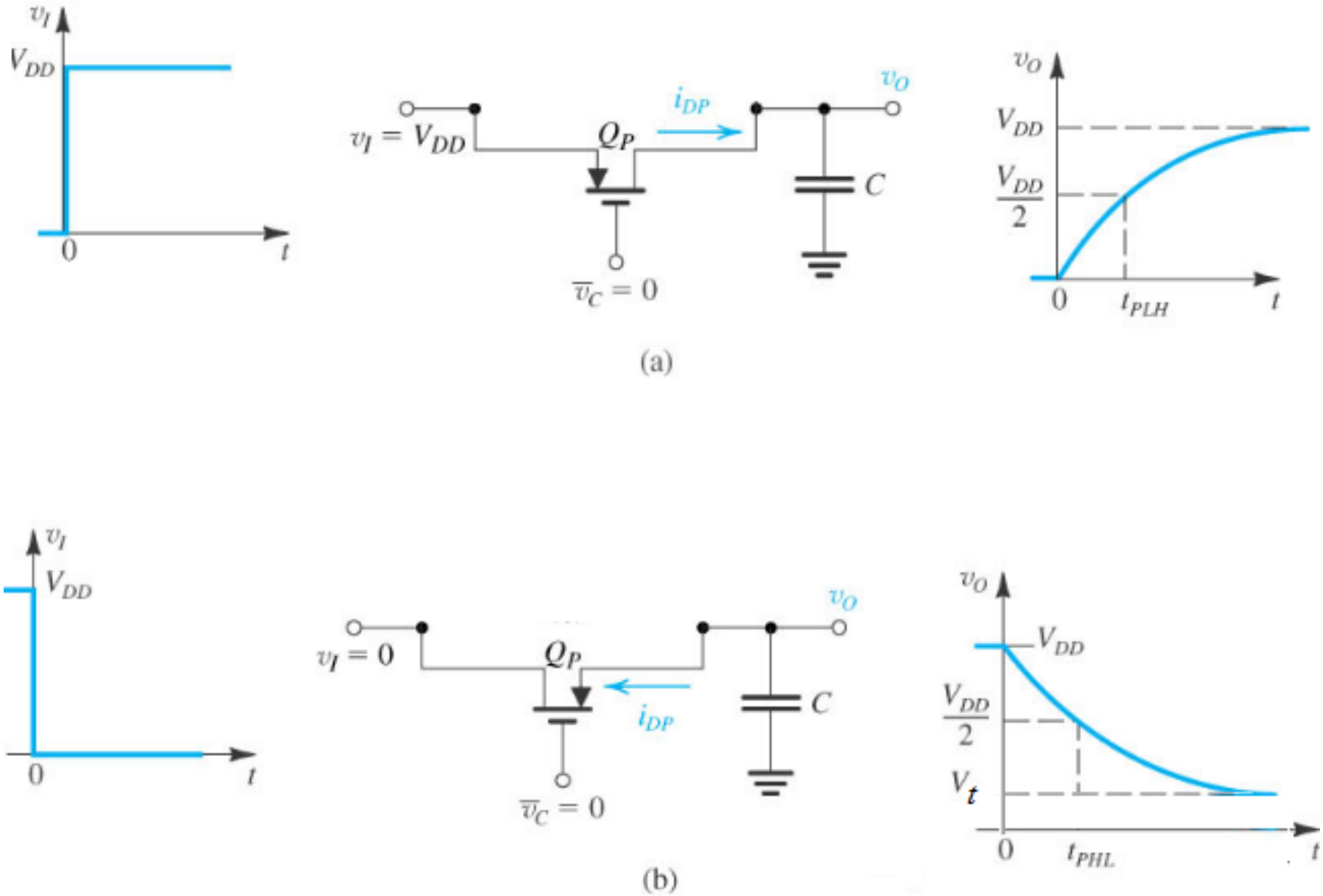
(b)

CA

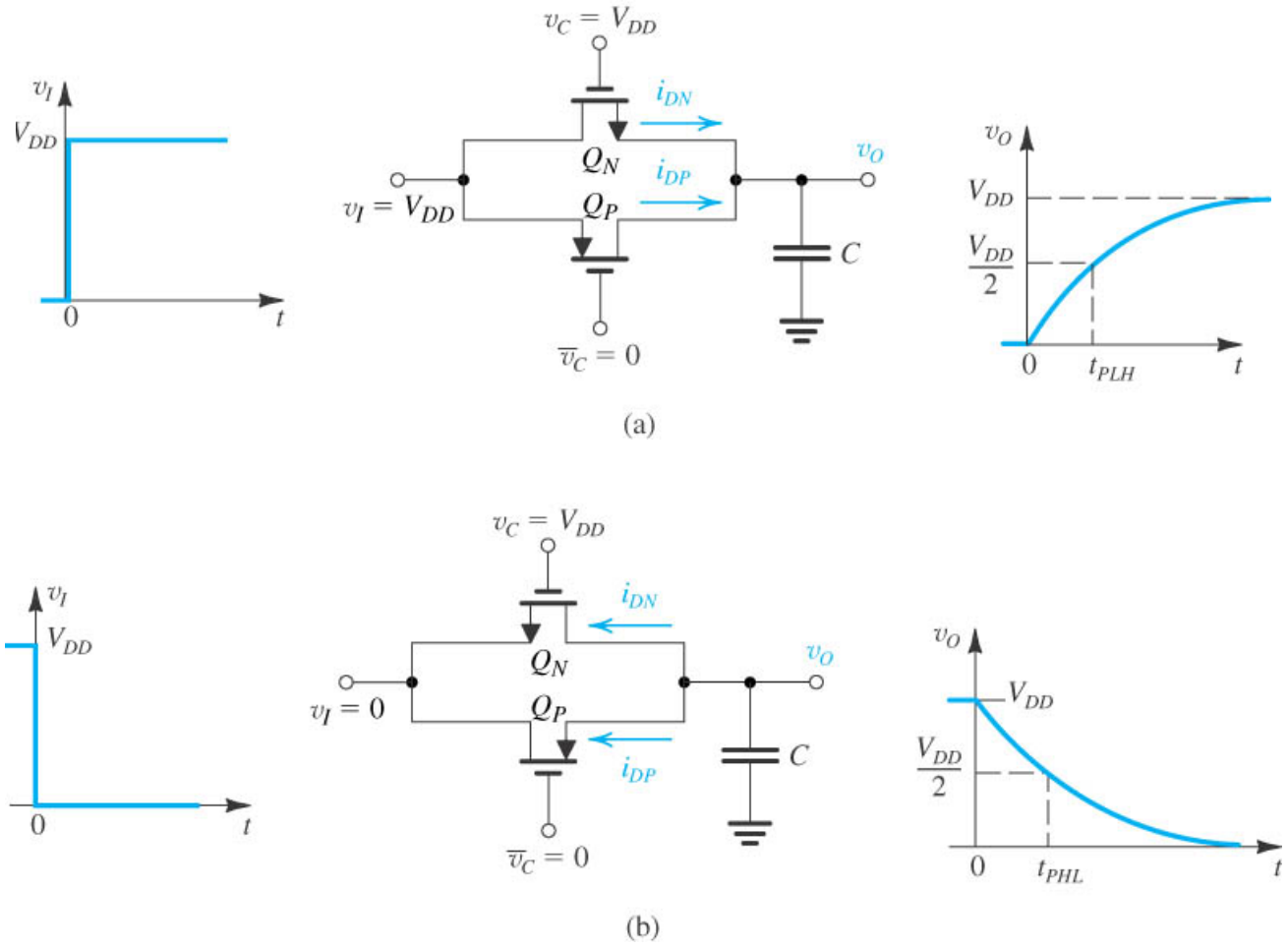
$$V_t = V_{t0} . + \gamma \left(\sqrt[2]{V_{SB} + 2 \cdot \phi_F} - \sqrt[2]{2 \cdot \phi_F} \right)$$

CC

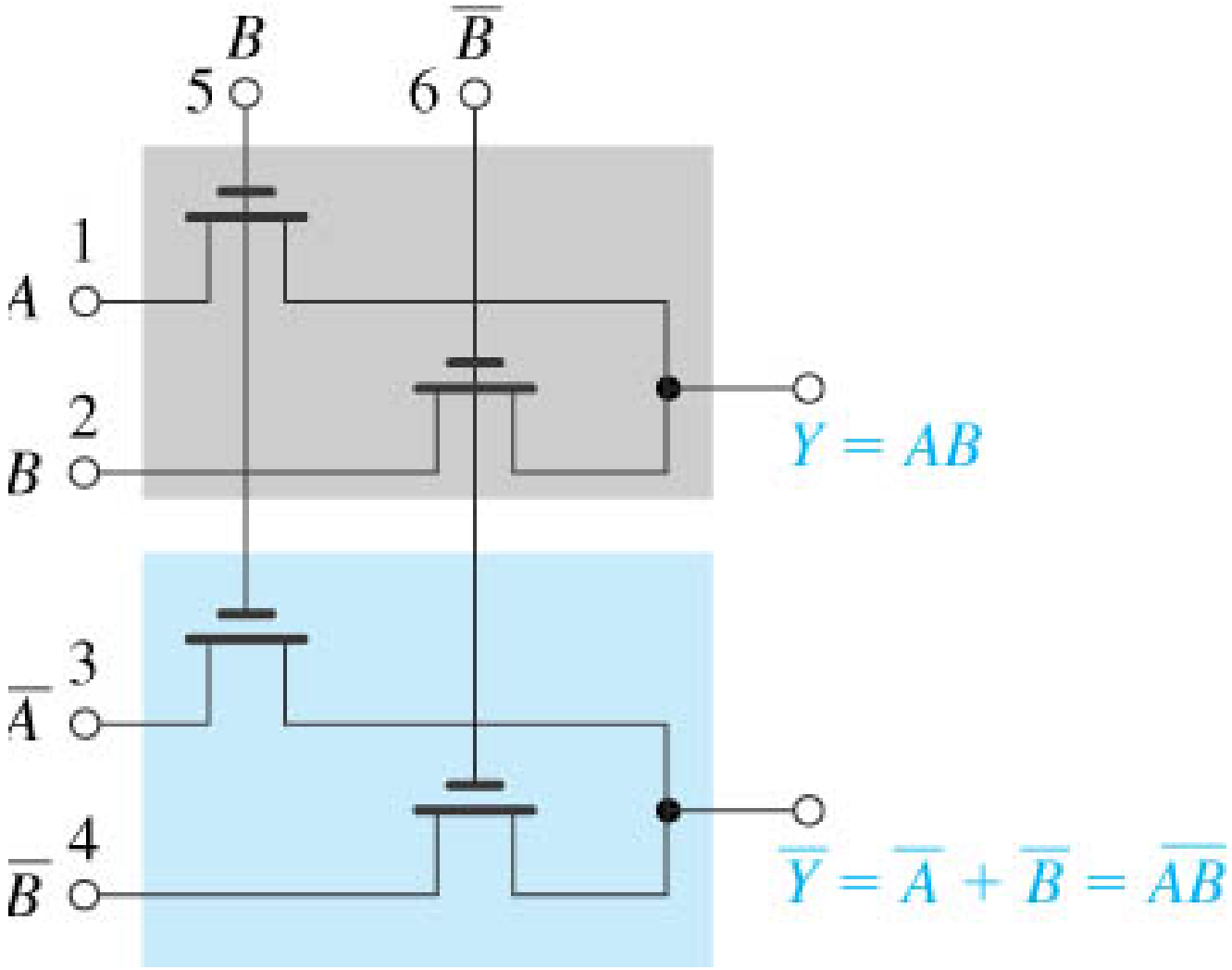
- **Figure 4.41** Small-signal equivalent-circuit model of a MOSFET in which the source is not connected to the body.



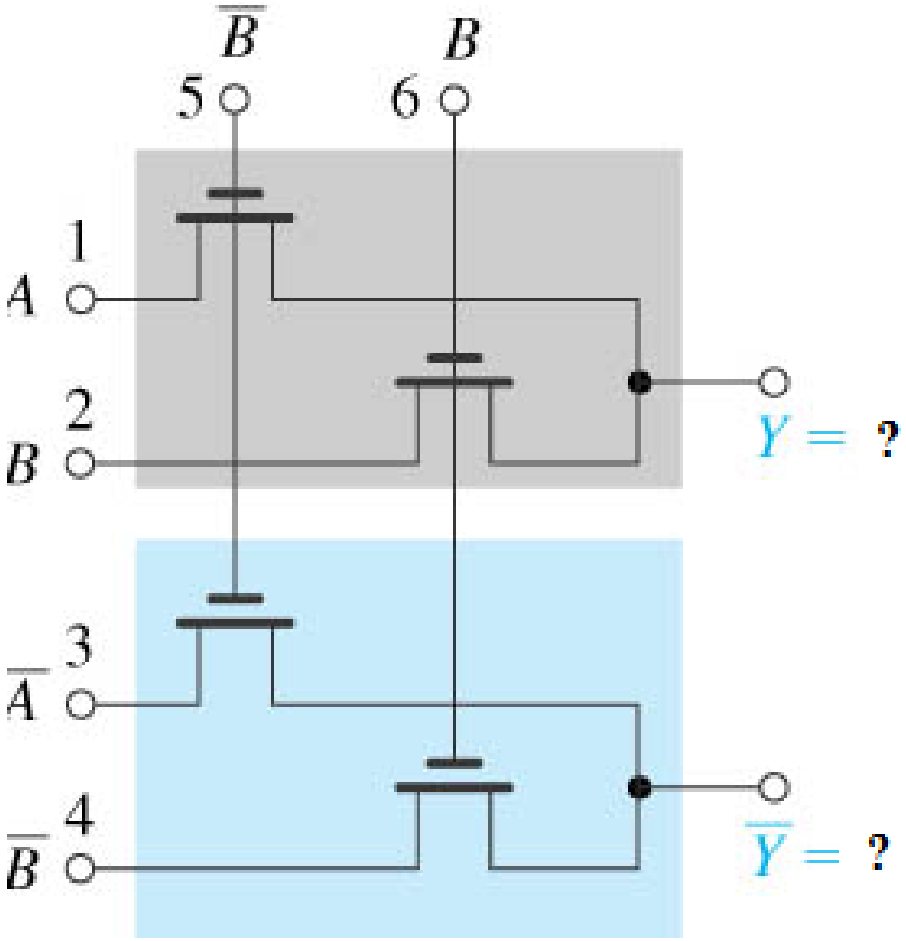
Transistor PMOS como chave de passagem .

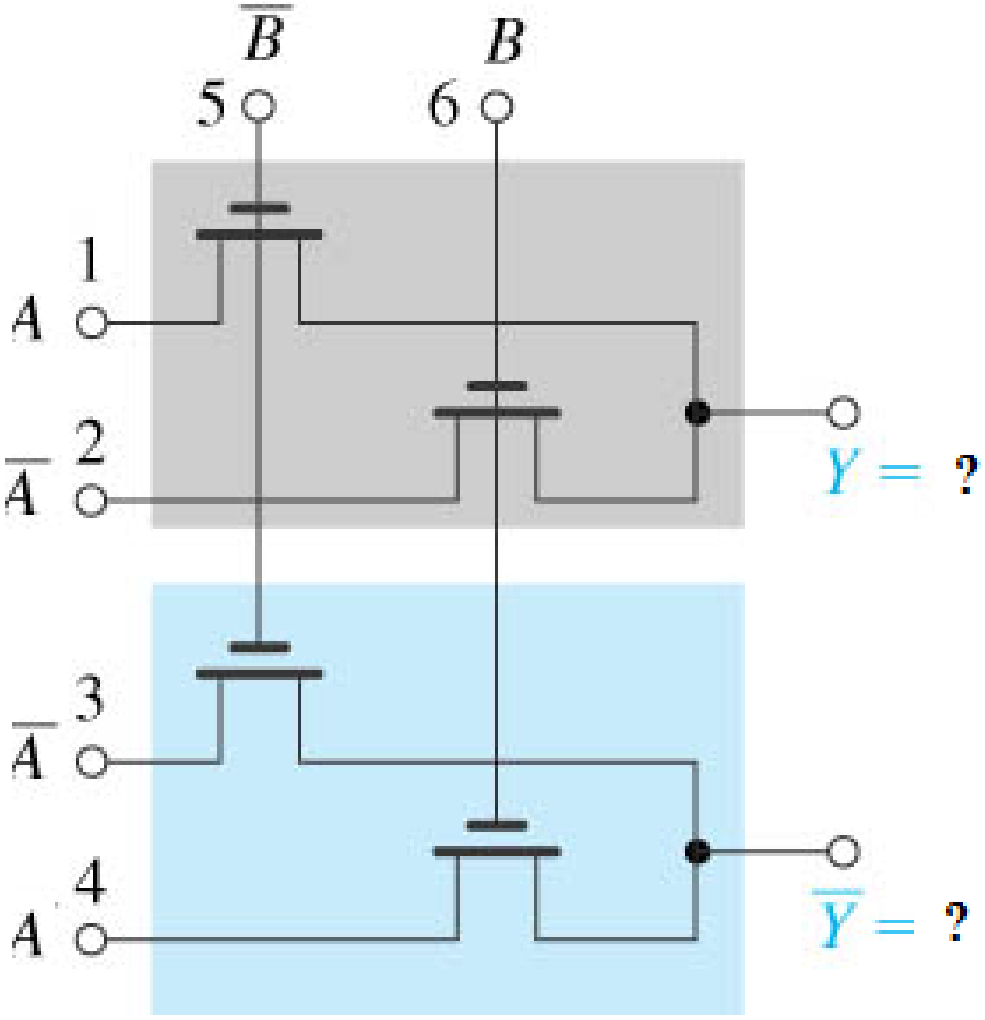


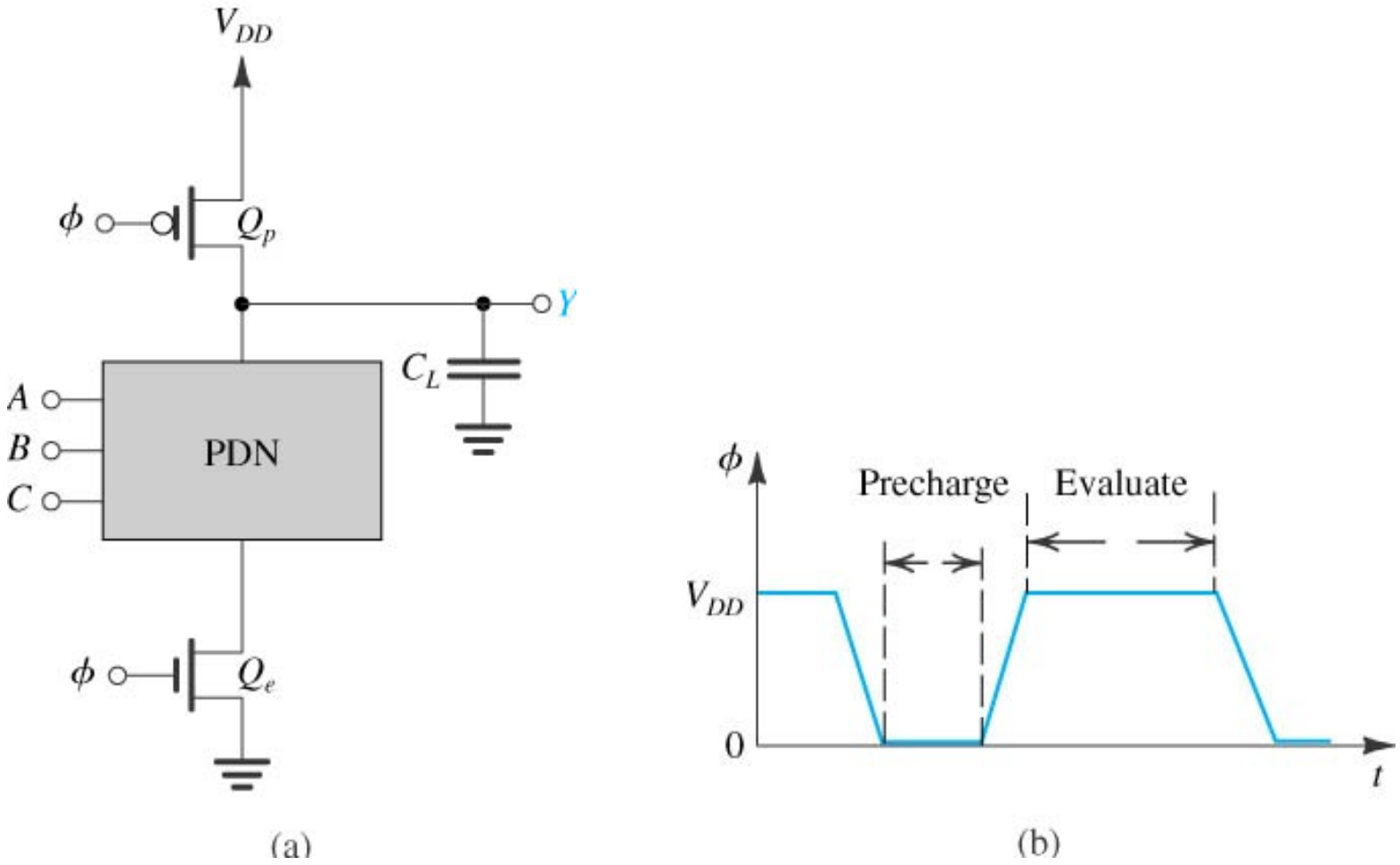
- **Figure 10.29** Operation of the transmission gate as a switch in PTL circuits with **(a)** v_I high and **(b)** v_I low.



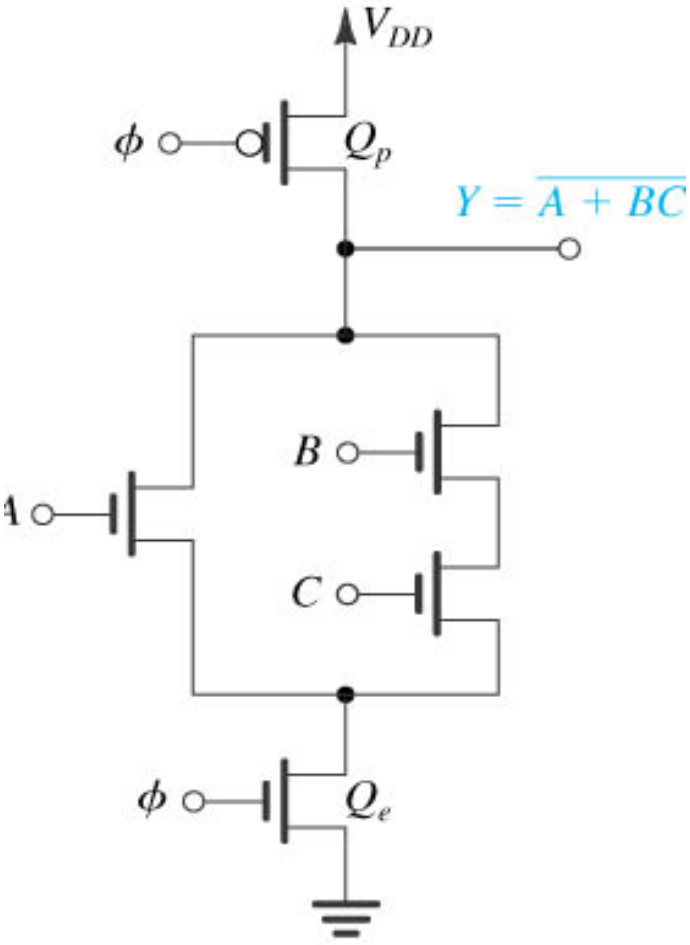
- **Figure 10.32** An example of a pass-transistor logic gate utilizing both the input variables and their complements. This type of circuit is therefore known as complementary pass-transistor logic or CPL. Note that both the output function and its complement are generated.


$\overline{B}$
5
B
6
1
A
2
B
$Y = ?$
3
$\overline{A}$
4
$\overline{B}$
$\overline{Y} = ?$

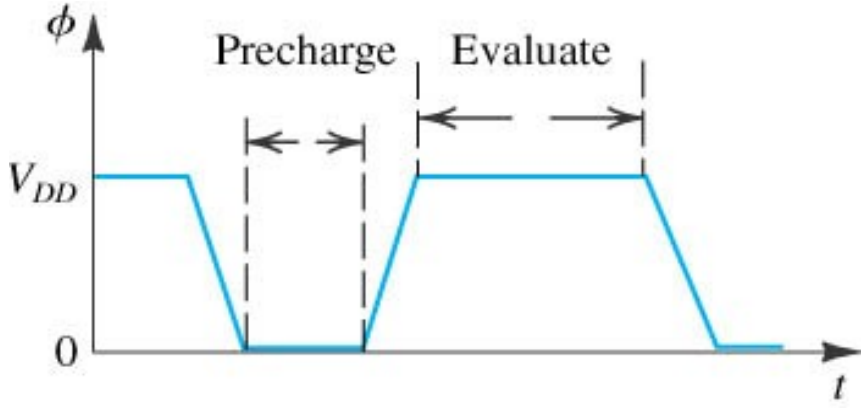

$\overline{B}$
B
5
6
1
A
2
$\overline{A}$
Y = ?
3
$\overline{A}$
4
A
$\overline{Y}$ = ?



- **Figure 10.33 (a)** Basic structure of dynamic-MOS logic circuits. **(b)** Waveform of the clock needed to operate the dynamic logic circuit. **(c)** An example circuit.

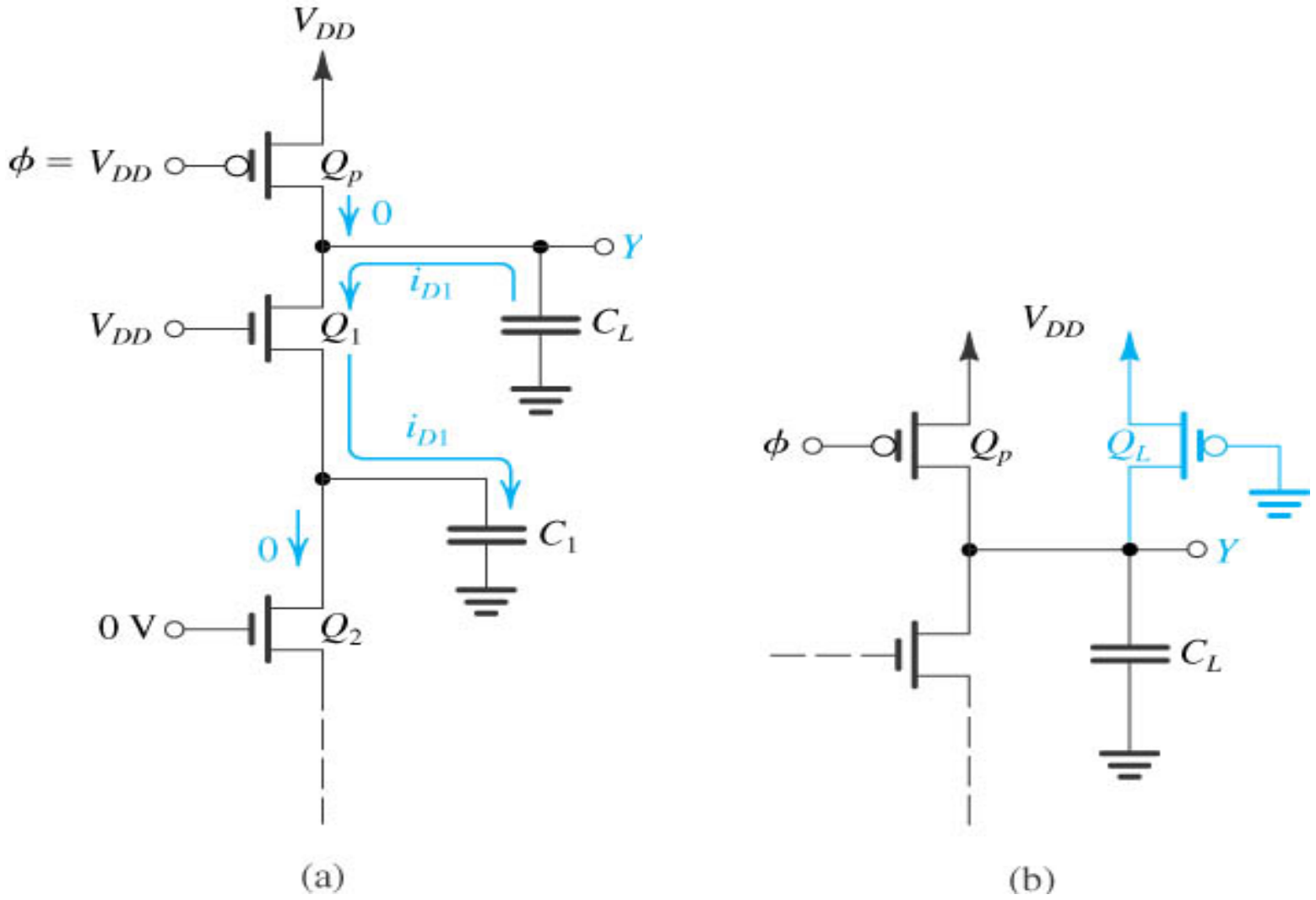


(c)

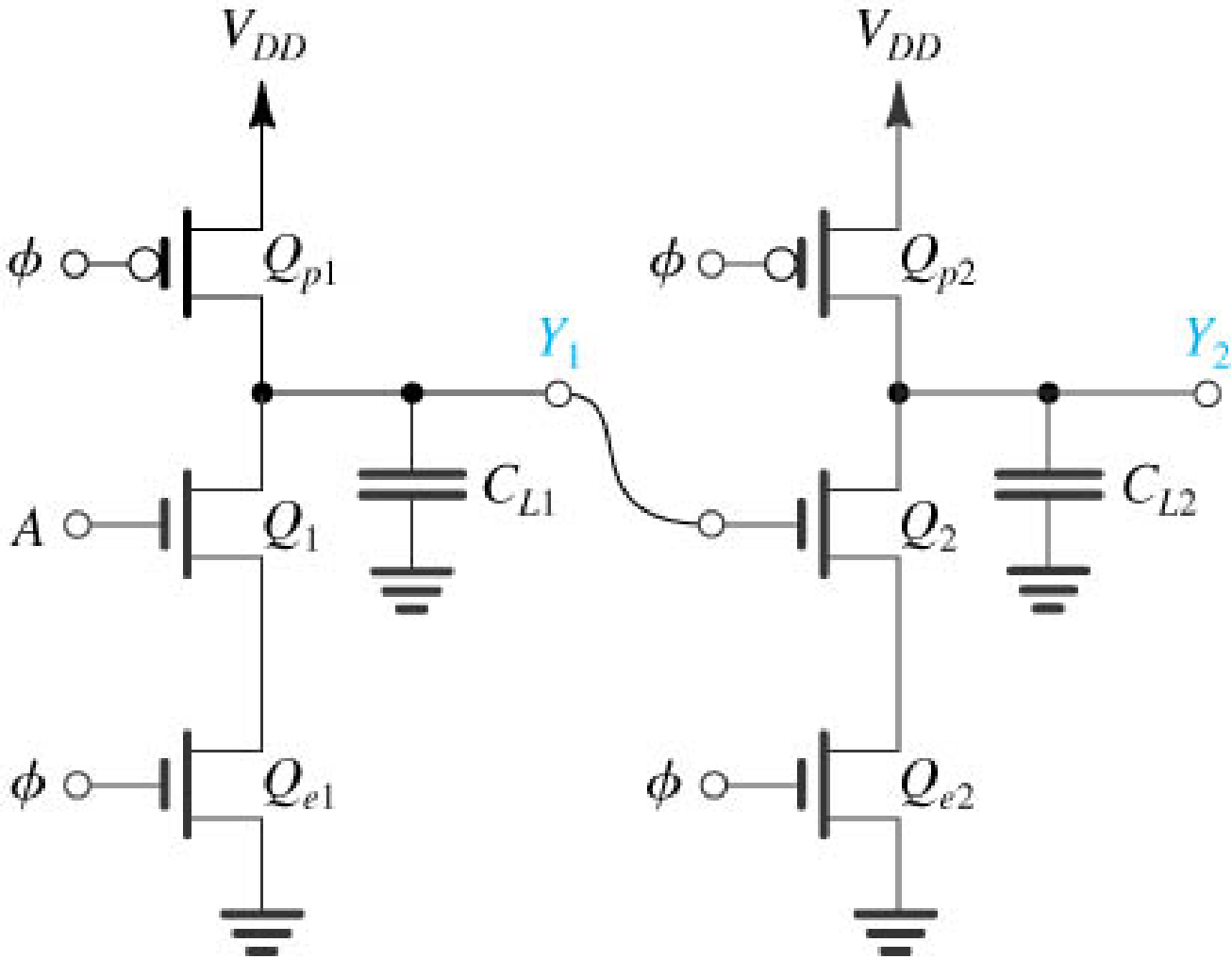


(b)

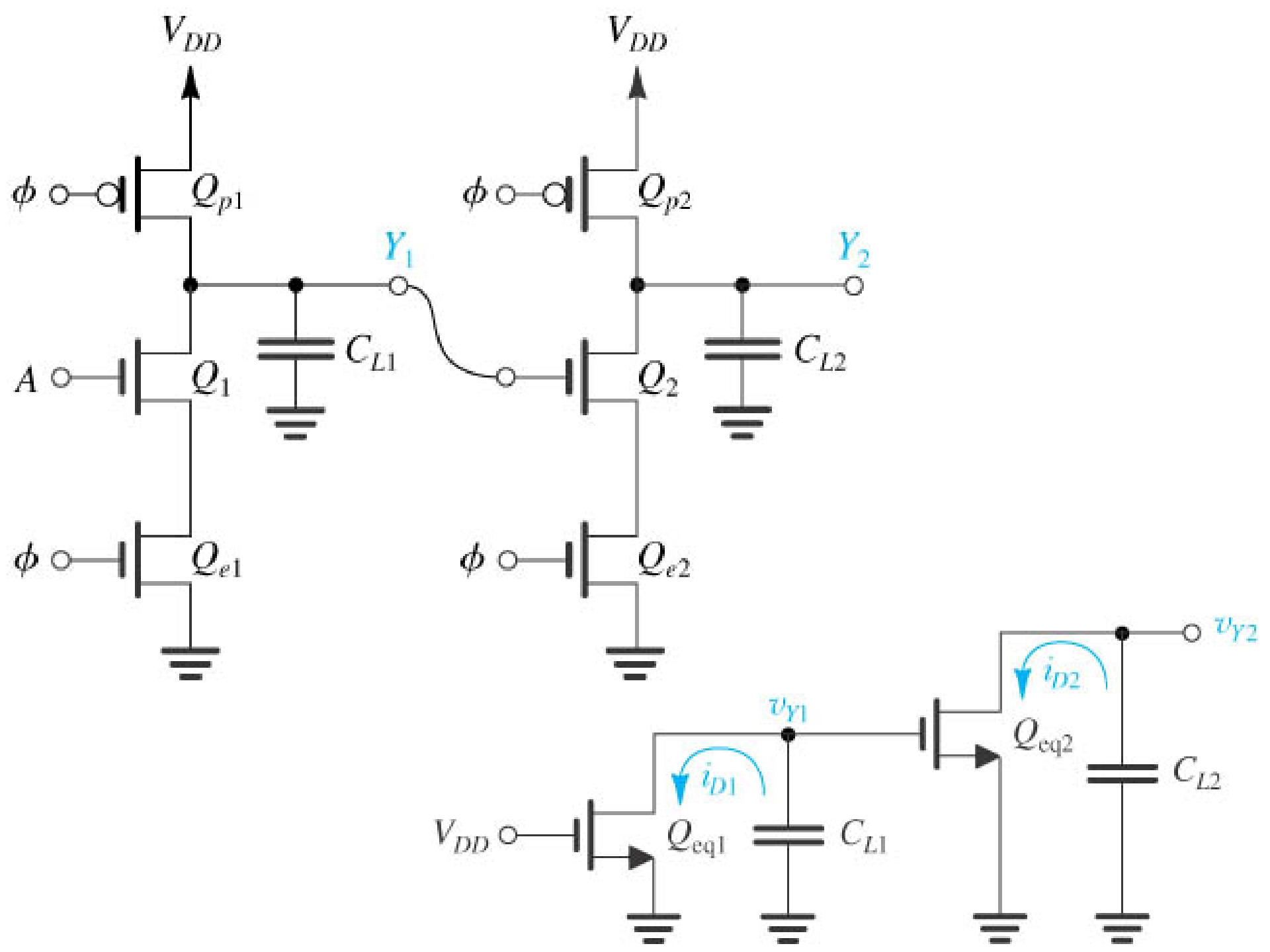
- **Figure 10.33 (a)** Basic structure of dynamic-MOS logic circuits. **(b)** Waveform of the clock needed to operate the dynamic logic circuit. **(c)** An example circuit.

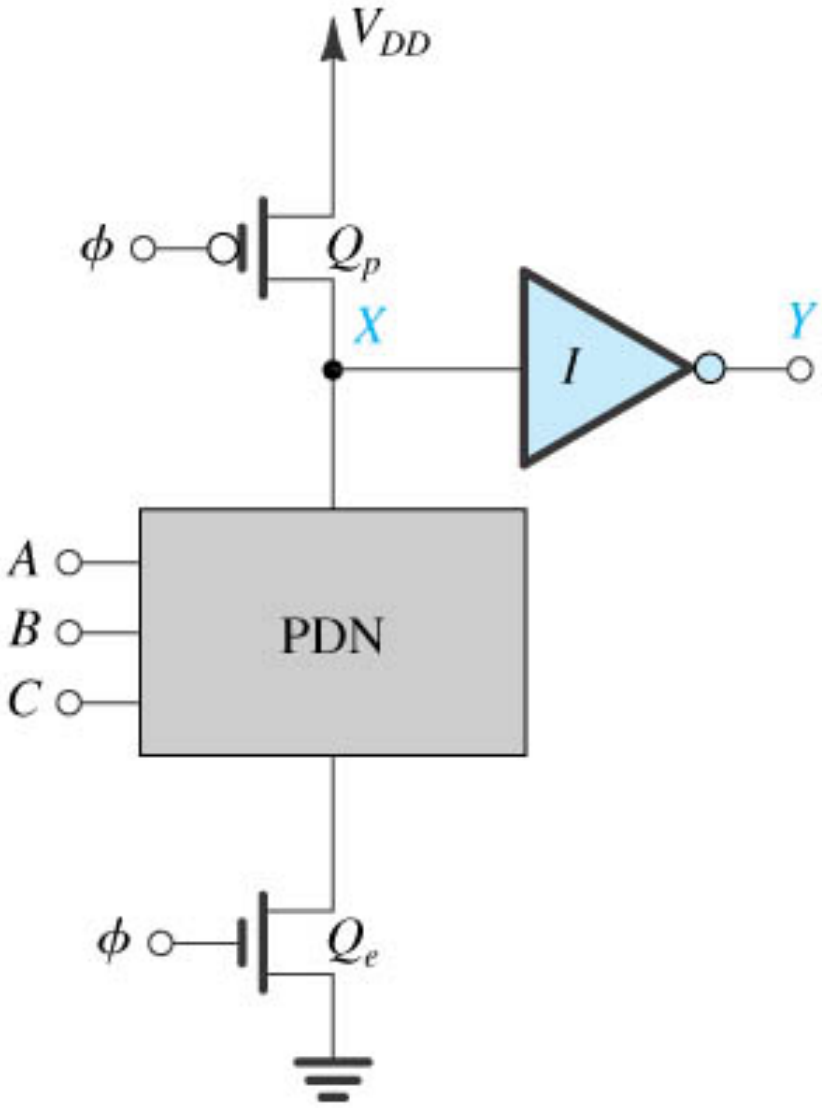


- **Figure 10.34 (a)** Charge sharing. **(b)** Adding a permanently turned-on transistor Q_L solves the charge-sharing problem at the expense of static power dissipation.

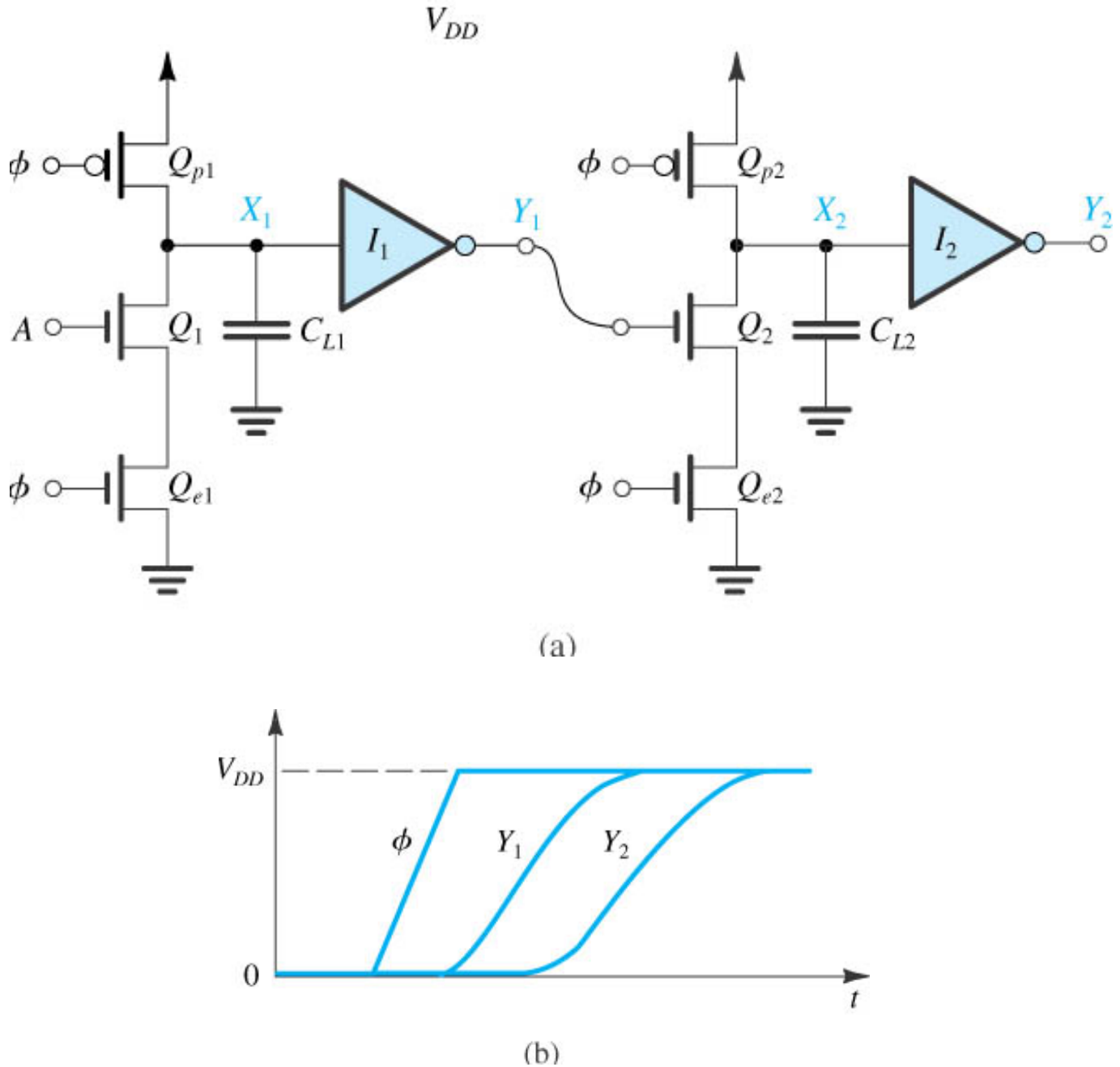


- **Figure 10.35** Two single-input dynamic logic gates connected in cascade. With the input *A* high, during the evaluation phase C_{L2} will partially discharge and the output at Y_2 will fall lower than V_{DD}, which can cause logic malfunction.


V_{DD}
V_{DD}
ϕ
Q_{p1}
ϕ
Q_{p2}
Y_1
Y_2
A
Q_1
C_{L1}
Q_2
C_{L2}
ϕ
Q_{e1}
ϕ
Q_{e2}
v_{Y2}
i_{D2}
v_{Y1}
Q_{eq2}
C_{L2}
i_{D1}
V_{DD}
Q_{eq1}
C_{L1}

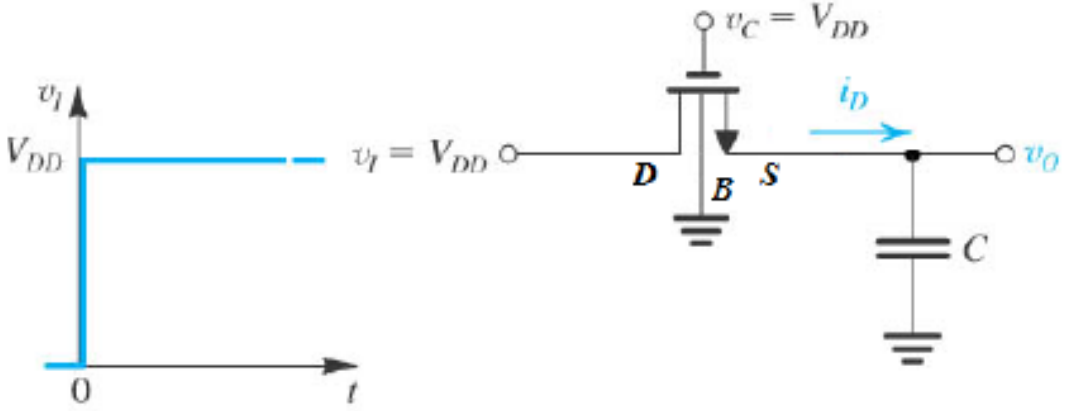


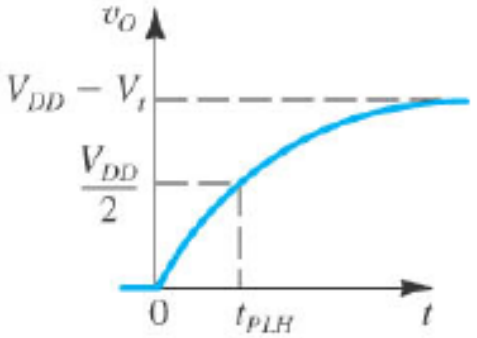
- **Figure 10.36** The Domino CMOS logic gate. The circuit consists of a dynamic-MOS logic gate with a static-CMOS inverter connected to the output. During evaluation, *Y* either will remain low (at 0 V) or will make one 0-to-1 transition (to V_{DD}).



- **Figure 10.37** **(a)** Two single-input domino CMOS logic gates connected in cascade. **(b)** Waveforms during the evaluation phase.

Considere o transistor NMOS habilitado como porta de passagem ($v_C = V_{DD}$). conforme indicado na figura a seguir. Sabendo-se que o substrato (B) está aterrado, determine o valor numérico da tensão de saída sobre o capacitor C após sua carga completa.





Dados:

$V_{DD} = 5\text{V}$

$k_n' = 200\mu\text{A/V}^2$

$V_{t0} = 1{,}0\ \text{V}$

$(\text{W/L})_n = 1$

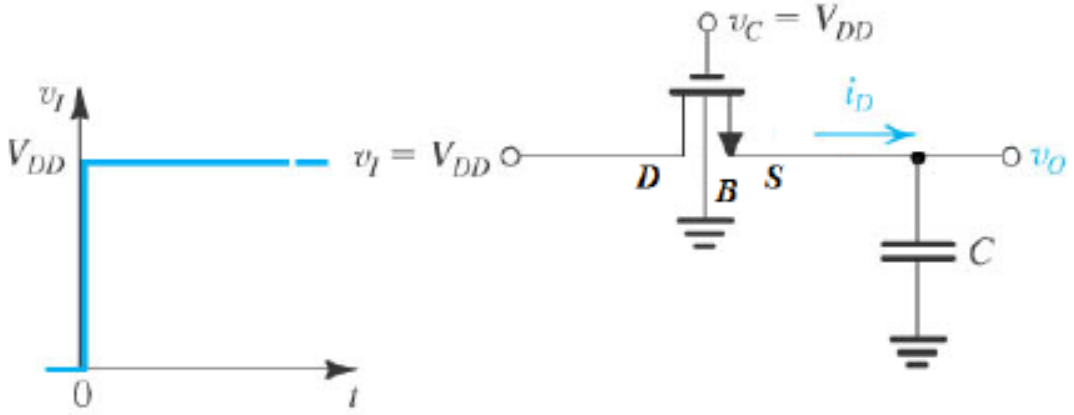
$\gamma = 0{,}5\ \text{V}^{1/2}$

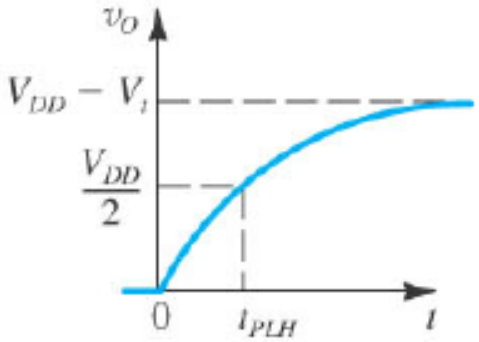
$2\phi_F = 0{,}6\text{V}$

FORMULARIO

$$V_t = V_{t0}. + \gamma\left(\sqrt[2]{V_{SB} + 2\cdot\phi_F} - \sqrt[2]{2\cdot\phi_F}\right)$$

Considere o transistor NMOS habilitado como porta de passagem ($v_C = V_{DD}$). conforme indicado na figura a seguir. Sabendo-se que o substrato (B) está aterrado, determine o valor numérico da tensão de saída sobre o capacitor C após sua carga completa.





Dados:

$V_{DD} = 5V$

$k_n' = 100\mu A/V^2$

$V_{t0} = 1{,}5\ V$

$(W/L)_n = 2$

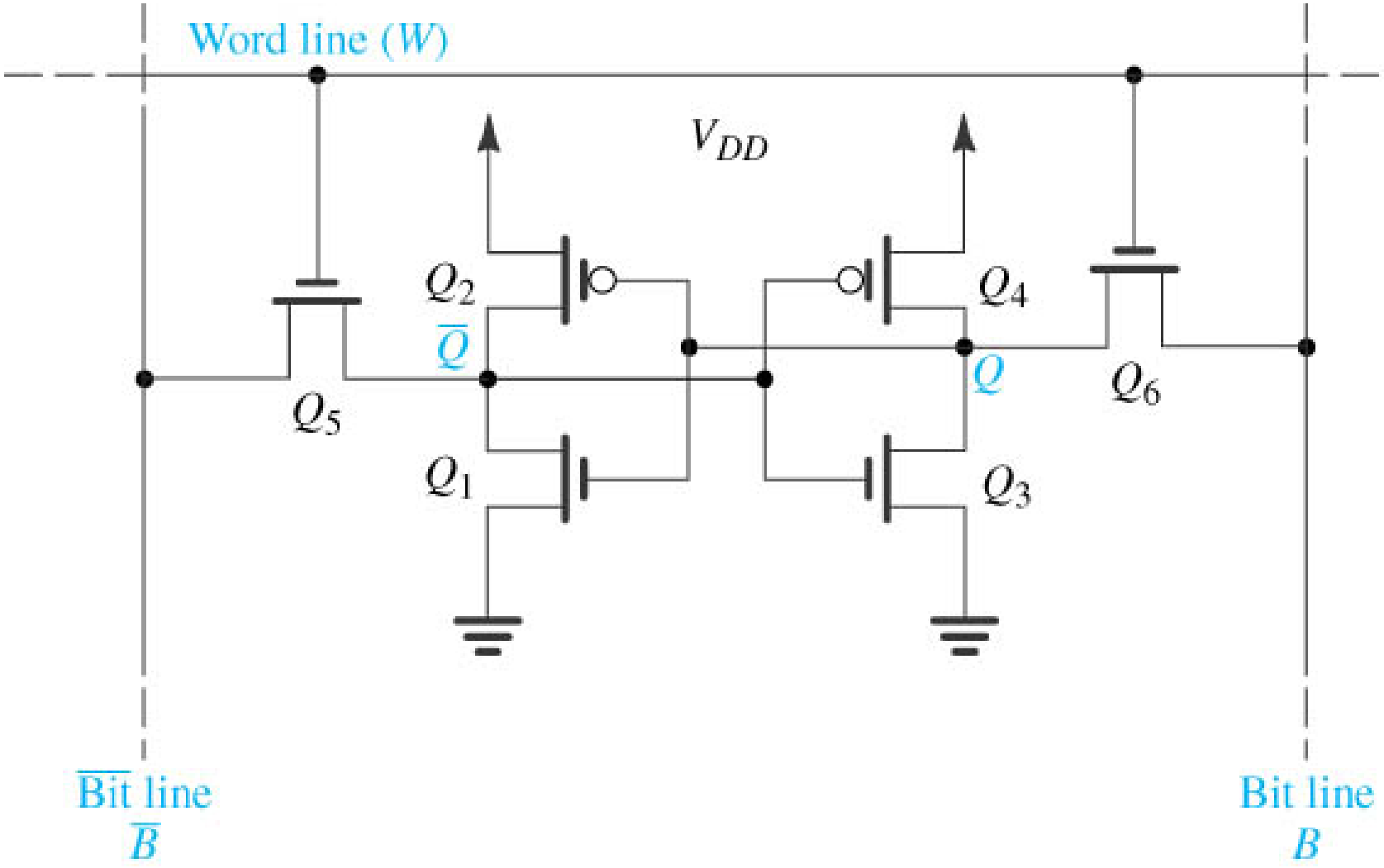
$\gamma = 0{,}3\ V^{1/2}$

$2\phi_F = 0{,}6V$

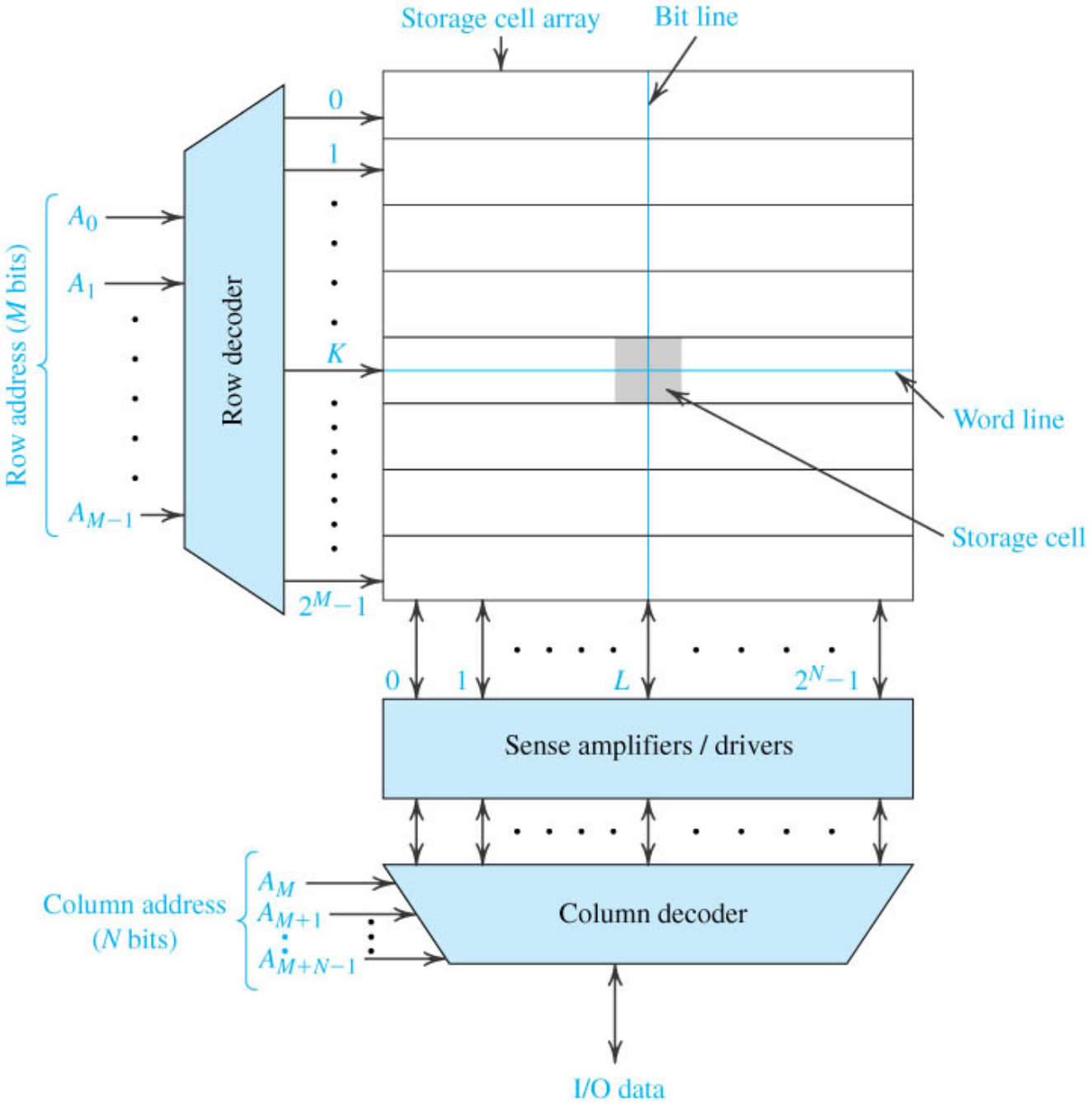
FORMULARIO

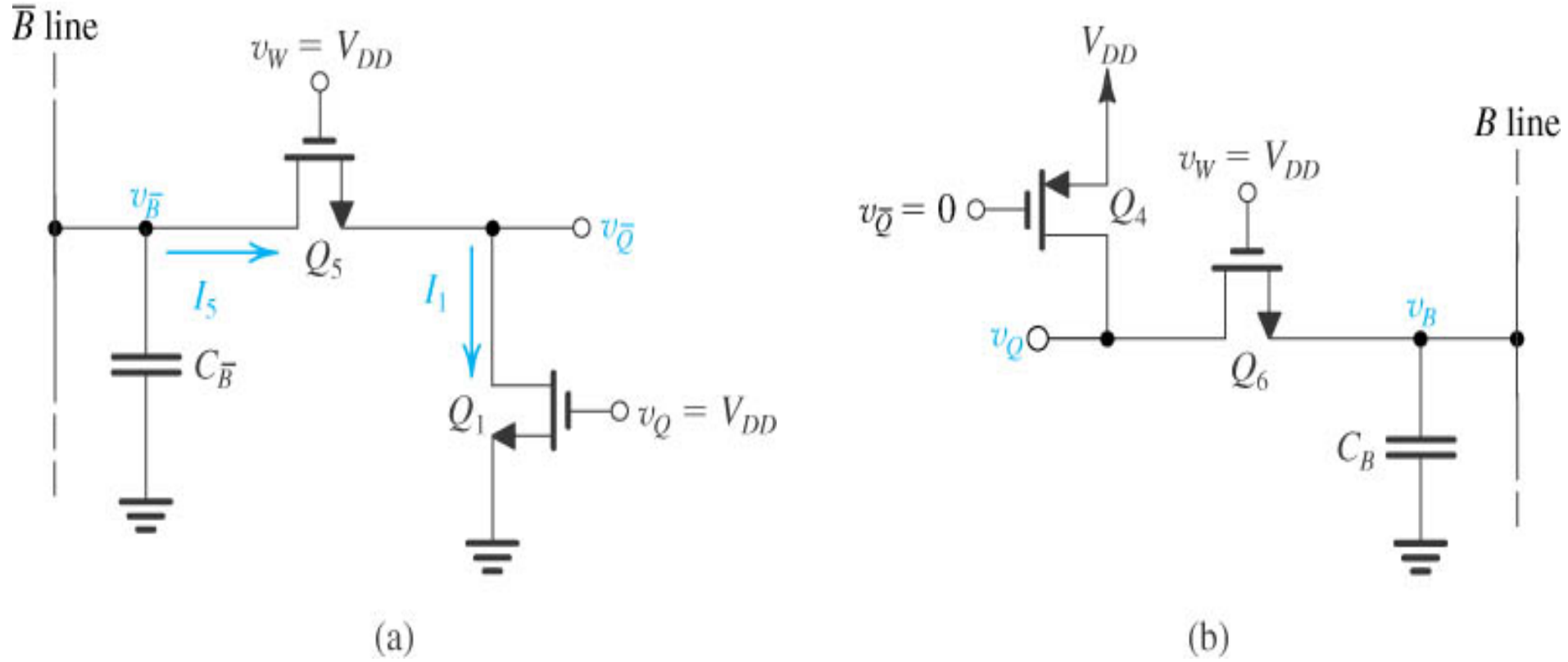
$$V_t = V_{t0}. + \gamma\left(\sqrt[2]{V_{SB} + 2\cdot\phi_F} - \sqrt[2]{2\cdot\phi_F}\right)$$

Célula de Memória SRAM CMOS

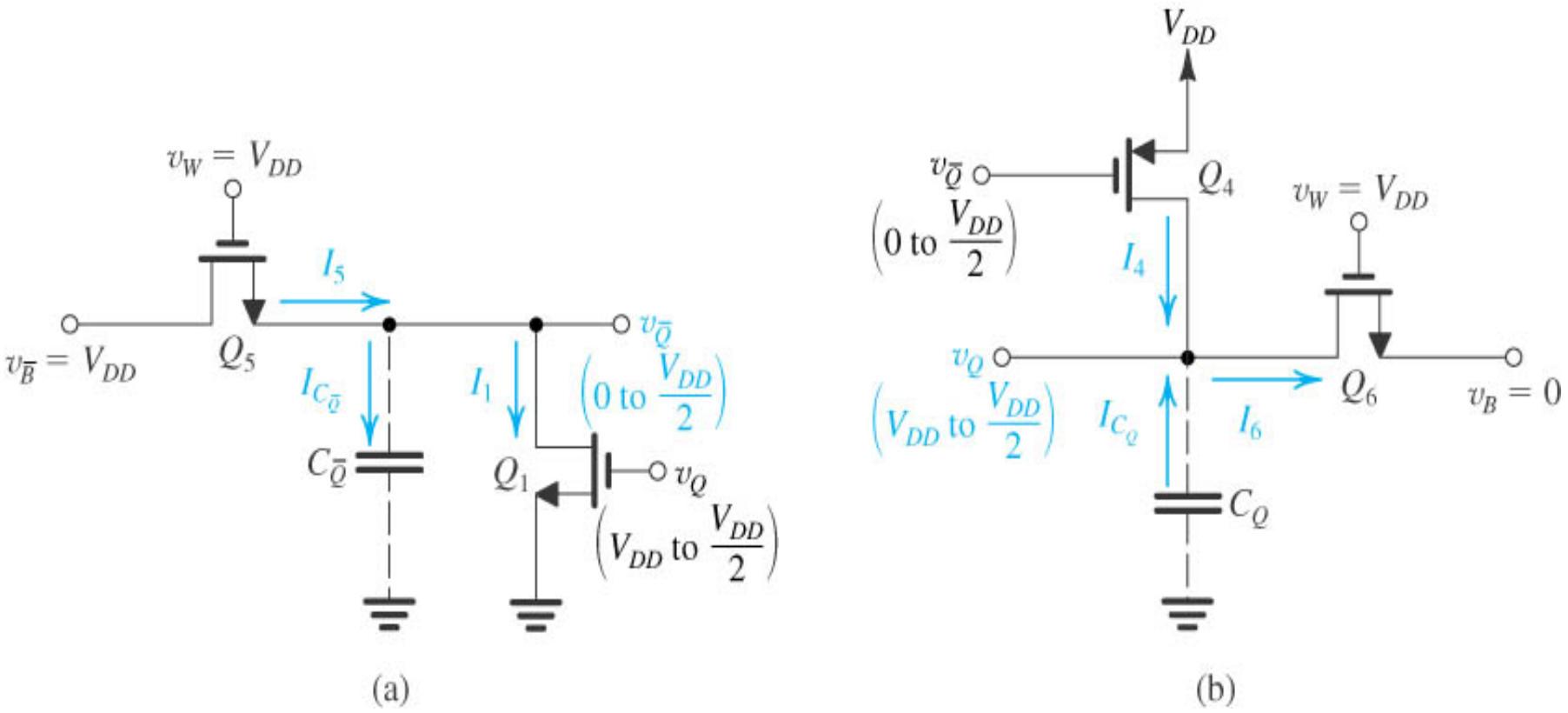


- A 2^{M+N}-bit memory chip organized as an array of 2^M rows $\times$ 2^N columns.





- **Figure 11.19** Relevant parts of the SRAM cell circuit during a read operation when the cell is storing a logic 1. Note that initially $v_{\overline{Q}} = V_{DD}$ and $v_Q = 0$. Also note that the B and $\overline{B}$ lines are usually precharged to a voltage of about $V_{DD}/2$. However, in Example 11.2, it is assumed for simplicity that the precharge voltage is V_{DD}.



- **Figure 11.20** Relevant parts of the SRAM circuit during a write operation. Initially, the SRAM has a stored 1 and a 0 is being written. These equivalent circuits apply before switching takes place. **(a)** The circuit is pulling node Q up toward $V_{DD}/2$. **(b)** The circuit is pulling node Q down toward $V_{DD}/2$.