PSI3024 – Eletrônica

Aulas 31 e 32

2023

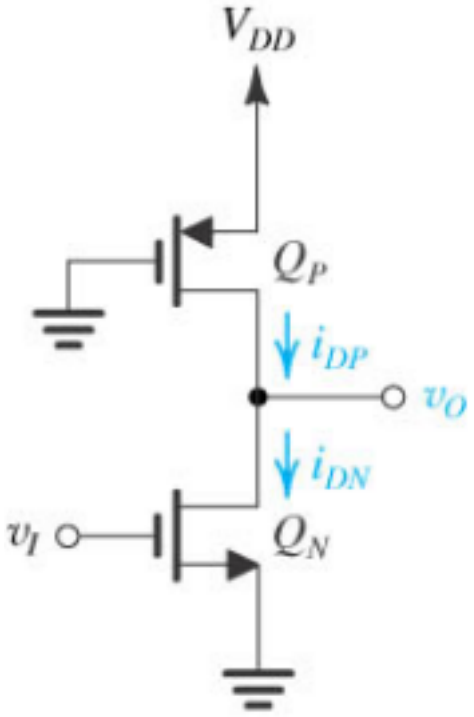
CIRCUITOS INVERSORES MOS

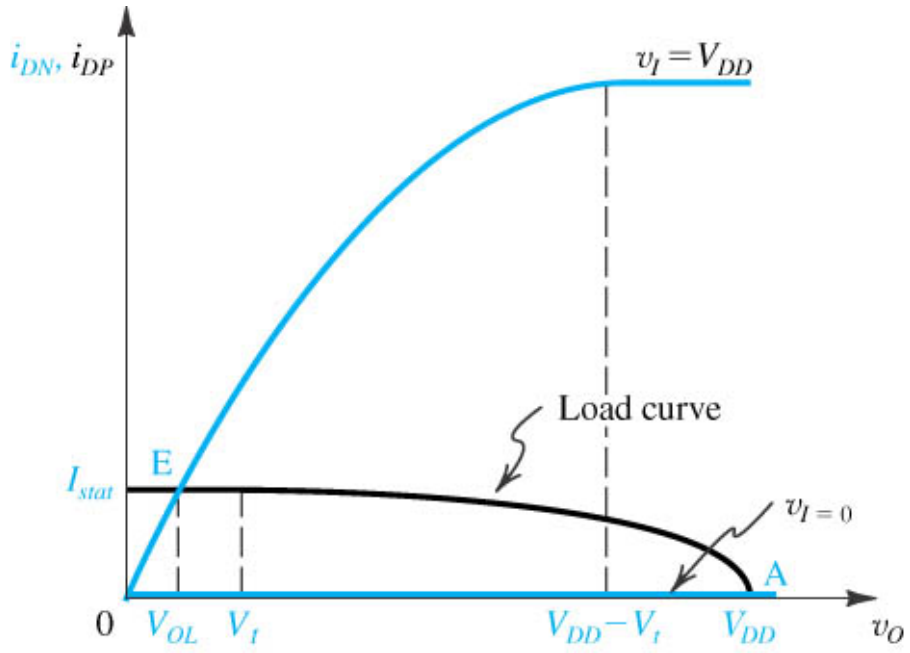
O circuito inversor é composto de dois dispositivos:
- um transistor de comando (por exemplo, nMOS)
- um elemento de carga.

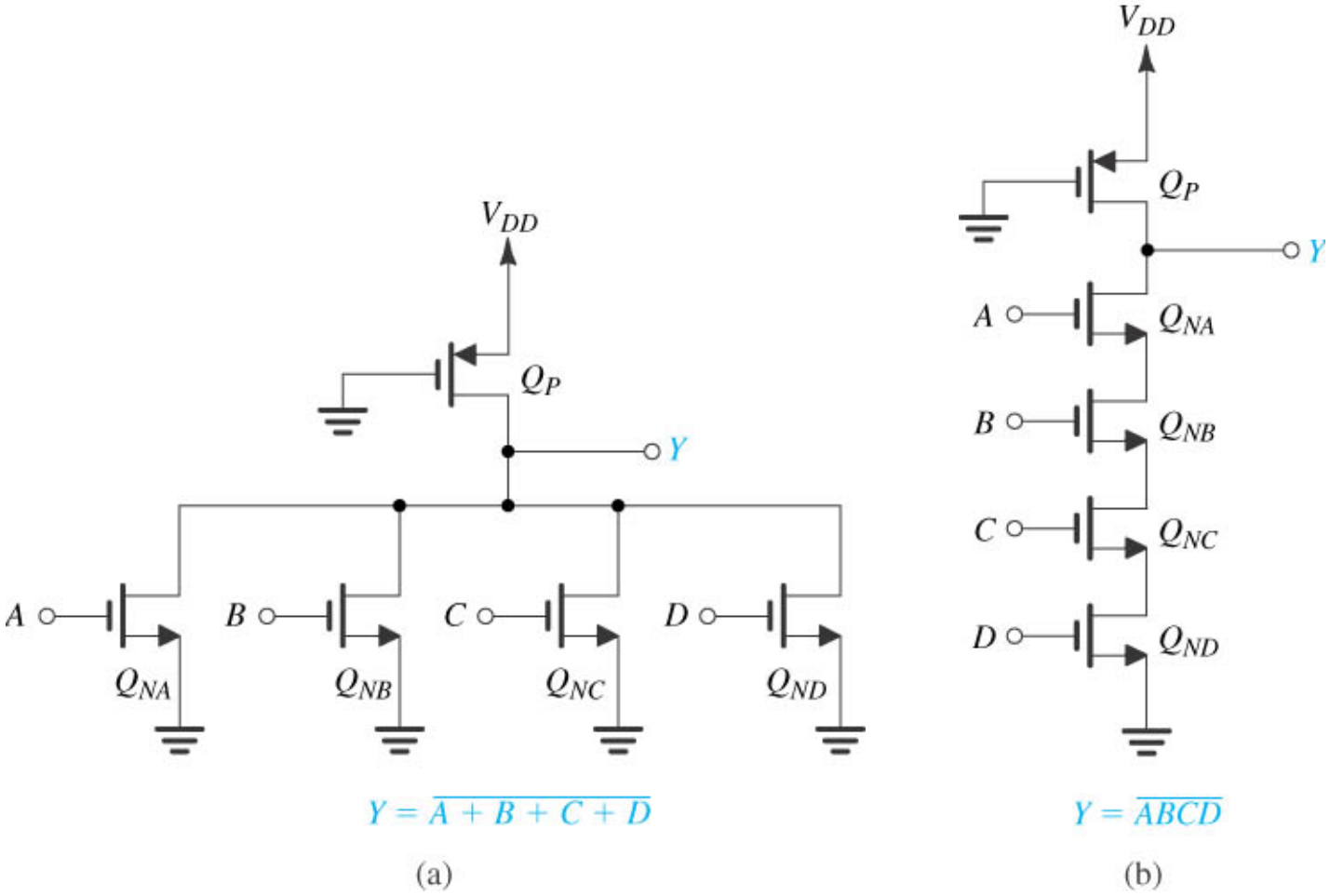
O elemento de carga pode ser do tipo:

a) resistiva
b) transistor de enriquecimento em triodo
c) transistor de enriquecimento em saturação
d) transistor de depleção
e) transistor tipo pMOS

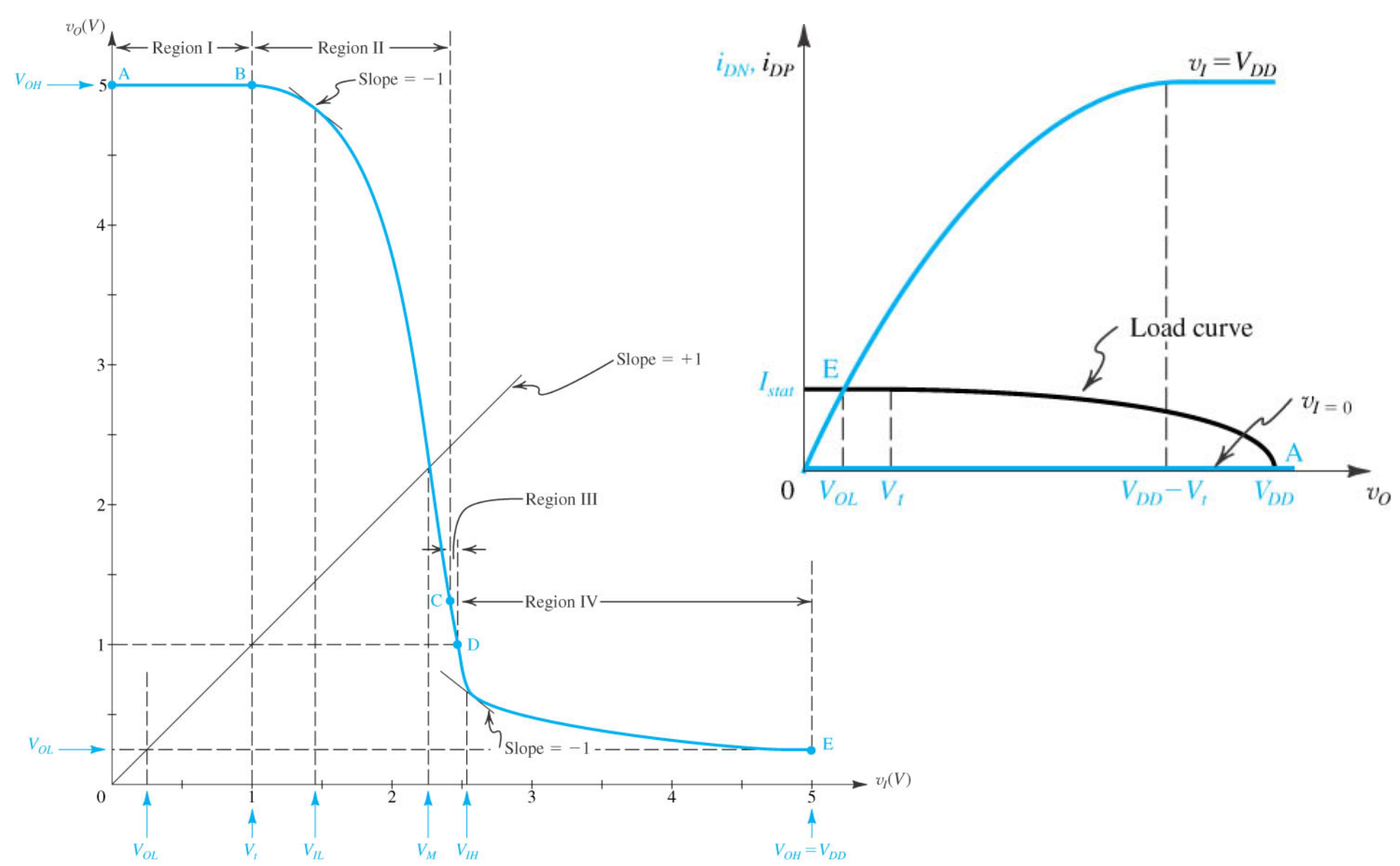
Inversor pseudo-NMOS







- **Figure 10.22** NOR and NAND gates of the pseudo-NMOS type.



- **Figure 10.21** VTC for the pseudo-NMOS inverter. This curve is plotted for V_{DD} = 5 V, $V_{tn} = -V_{tp}$ = 1 V, and r = 9.

Região II (segmento BC)

$$k_n = rk_p,$$

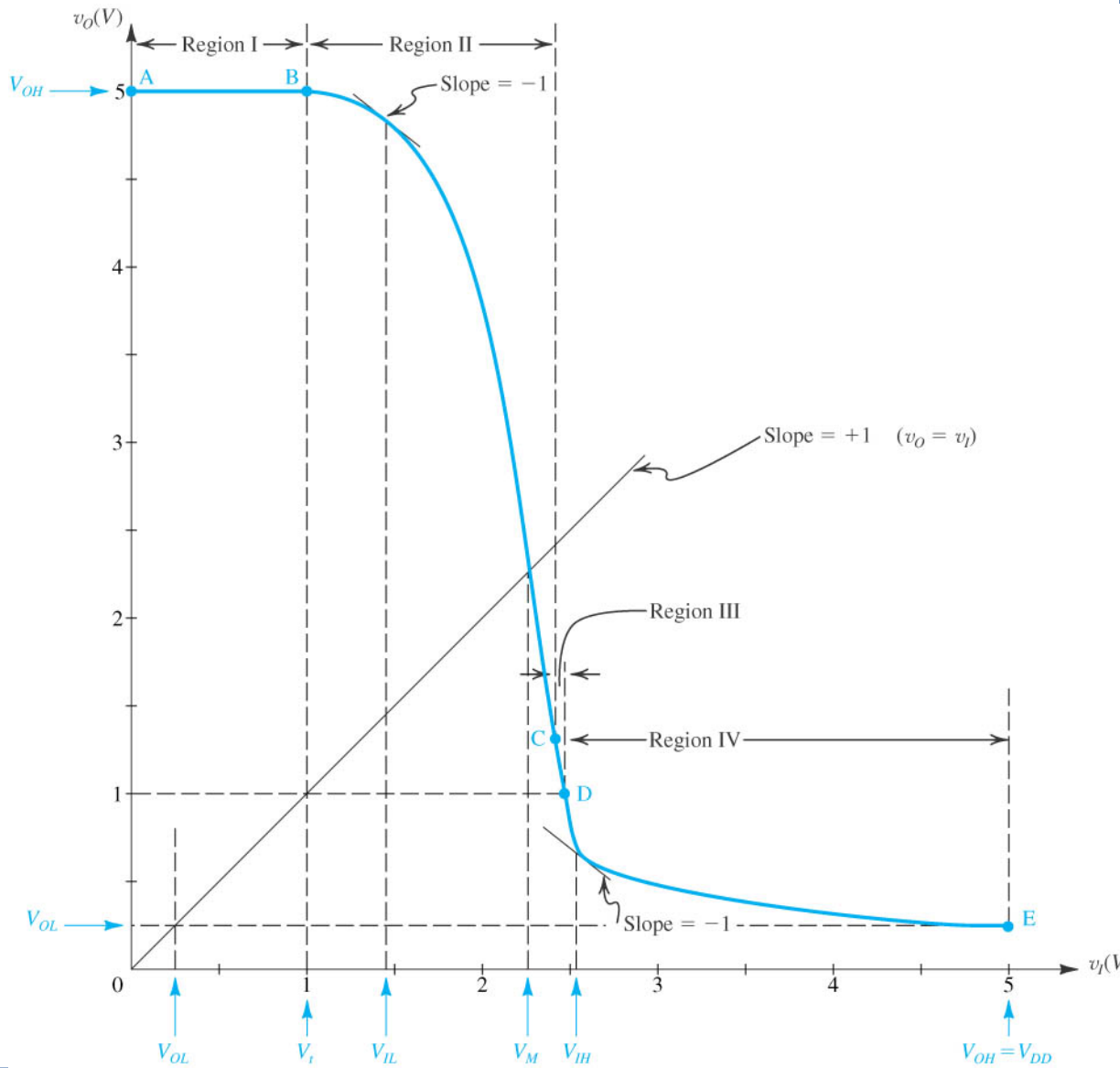
$$v_O = V_t + \sqrt{(V_{DD} - V_t)^2 - r(v_I - V_t)^2}$$

$$V_{IL} = V_t + \frac{V_{DD} - V_t}{\sqrt{r(r+1)}}$$

$$V_M = V_t + \frac{V_{DD} - V_t}{\sqrt{r+1}}$$

(ponto C)

$$v_O = v_I - V_t$$



Região IV (segmento DE)

$$v_O = (v_I - V_t) - \sqrt{(v_I - V_t)^2 - \frac{1}{r}(V_{DD} - V_t)^2}$$

$$k_n = rk_p$$

Região III (segmento CD)

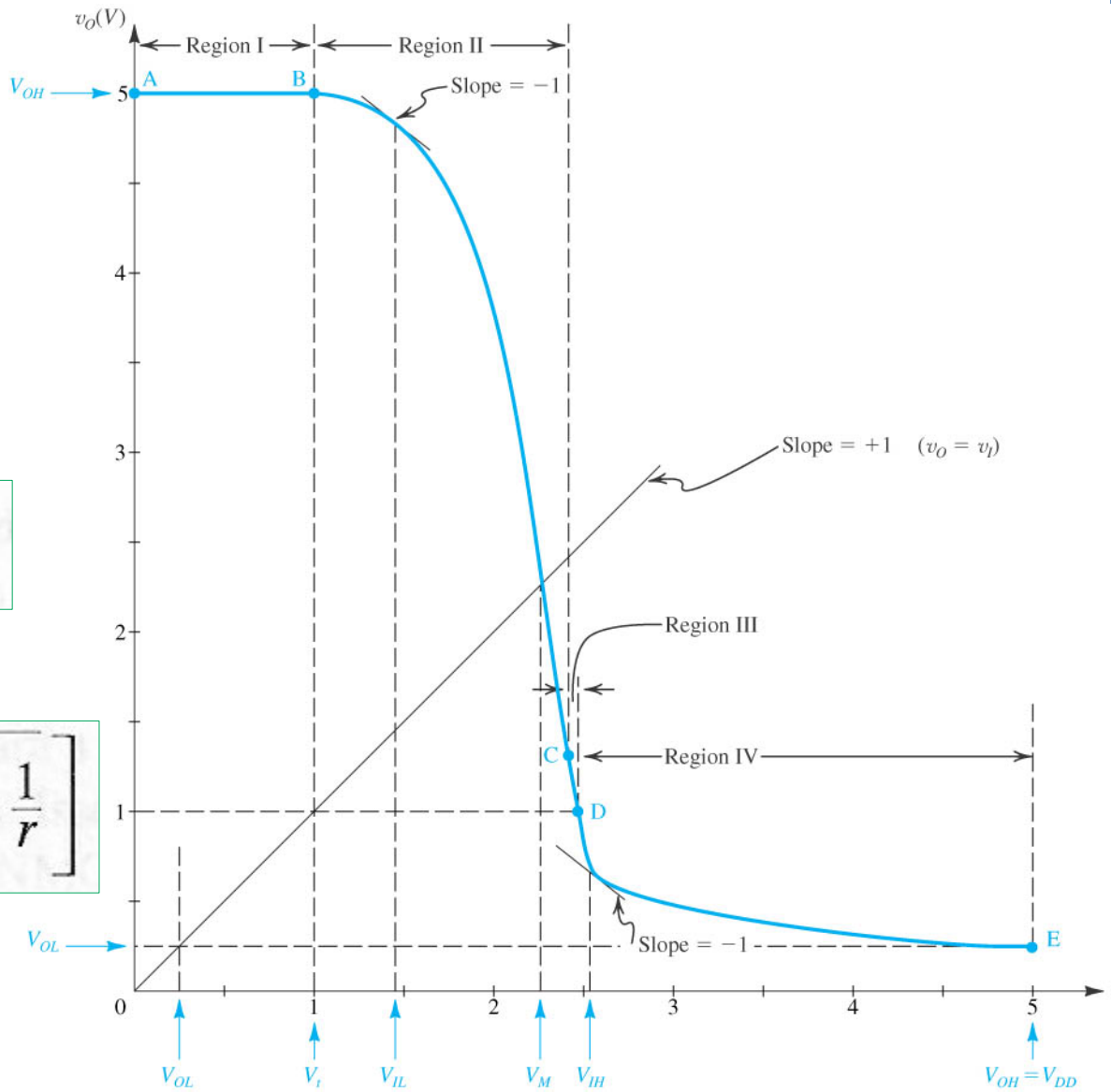
ponto D $v_O = V_t$.

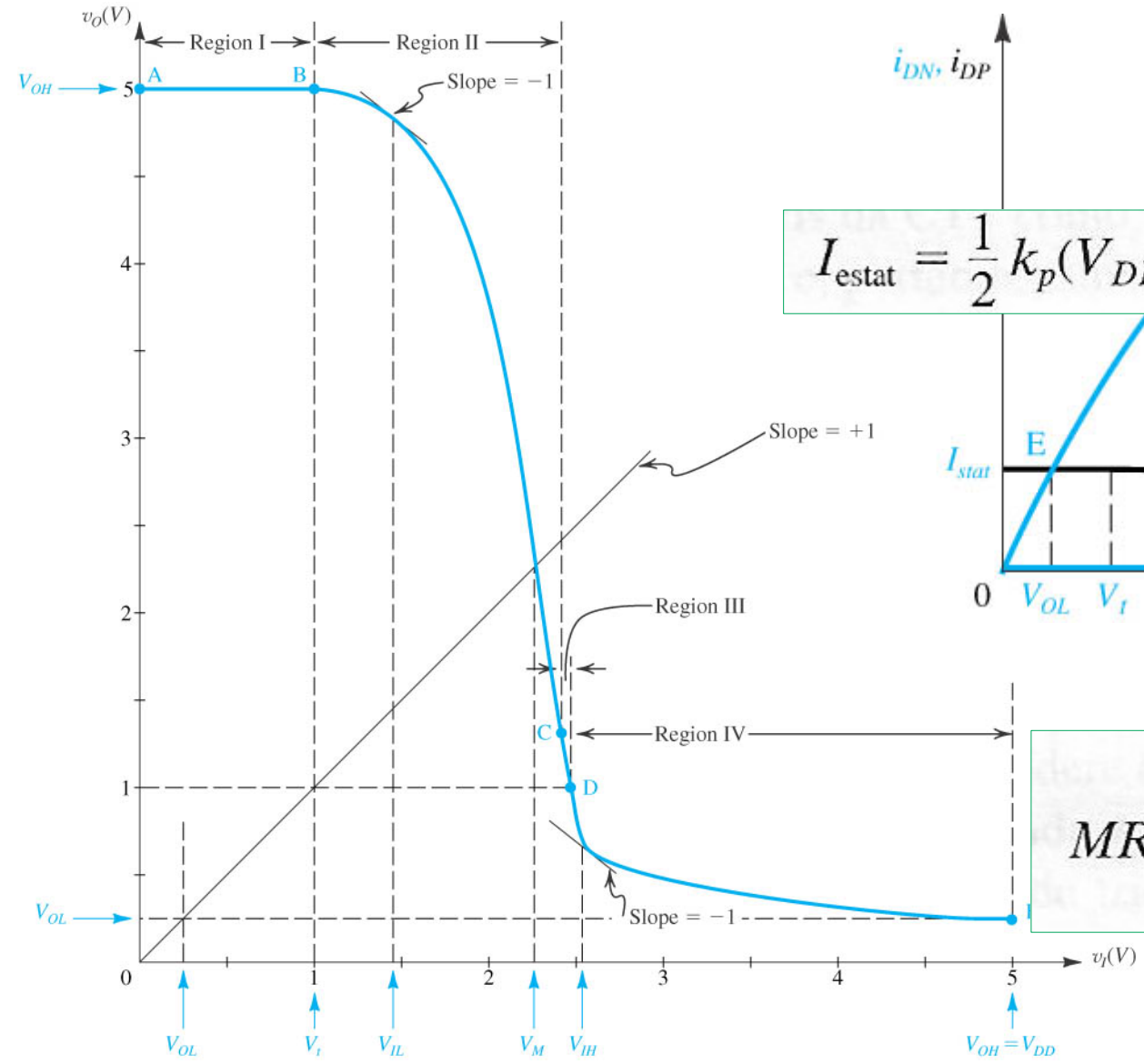
$$\partial v_O/\partial v_I = -1 \text{ e } v_1 = V_{IH},$$

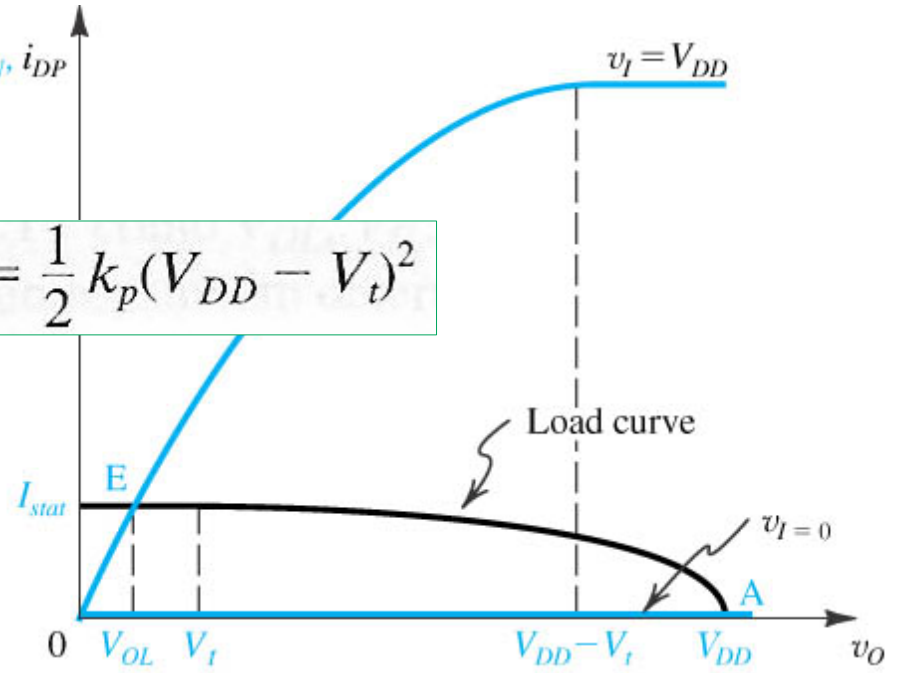
$$V_{IH} = V_t + \frac{2}{\sqrt{3r}}(V_{DD} - V_t)$$

$$v_I = V_{DD}$$

$$V_{OL} = (V_{DD} - V_t)\left[1 - \sqrt{1 - \frac{1}{r}}\right]$$







$$I_{\text{estat}} = \frac{1}{2} k_p (V_{DD} - V_t)^2$$

$$MR_H = (V_{DD} - V_t\left(1 - \frac{2}{\sqrt{3r}}\right)$$

$$MR_L = V_t - (V_{DD} - V_t)\left[1 - \sqrt{1 - \frac{1}{r} - \frac{1}{\sqrt{r(r+1)}}}\right]$$

EXEMPLO 10.3

Considere o inversor pseudo-NMOS fabricado na tecnologia CMOS especificada no Exemplo 10.1, ou seja, $\mu_n C_{ox} = 115\ \mu A/V^2$, $\mu_p C_{ox} = 30\ \mu A/V^2$, $V_{tn} = -V_{tp} = 0{,}4$ V e $V_{DD} = 2{,}5$ V. Seja a razão W/L de Q_N de (0,375 μm/0,25 μm) e $r = 9$. Obtenha:

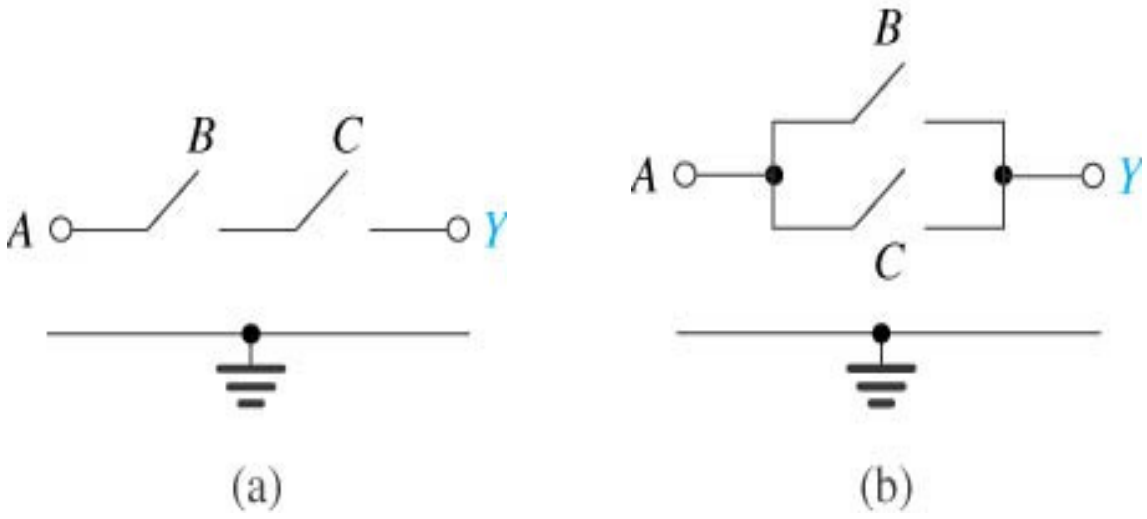
(a) V_{OH}, V_{OL}, V_{IL}, V_{IH}, V_M, MR_H e MR_L

(b) $(W/L)_p$

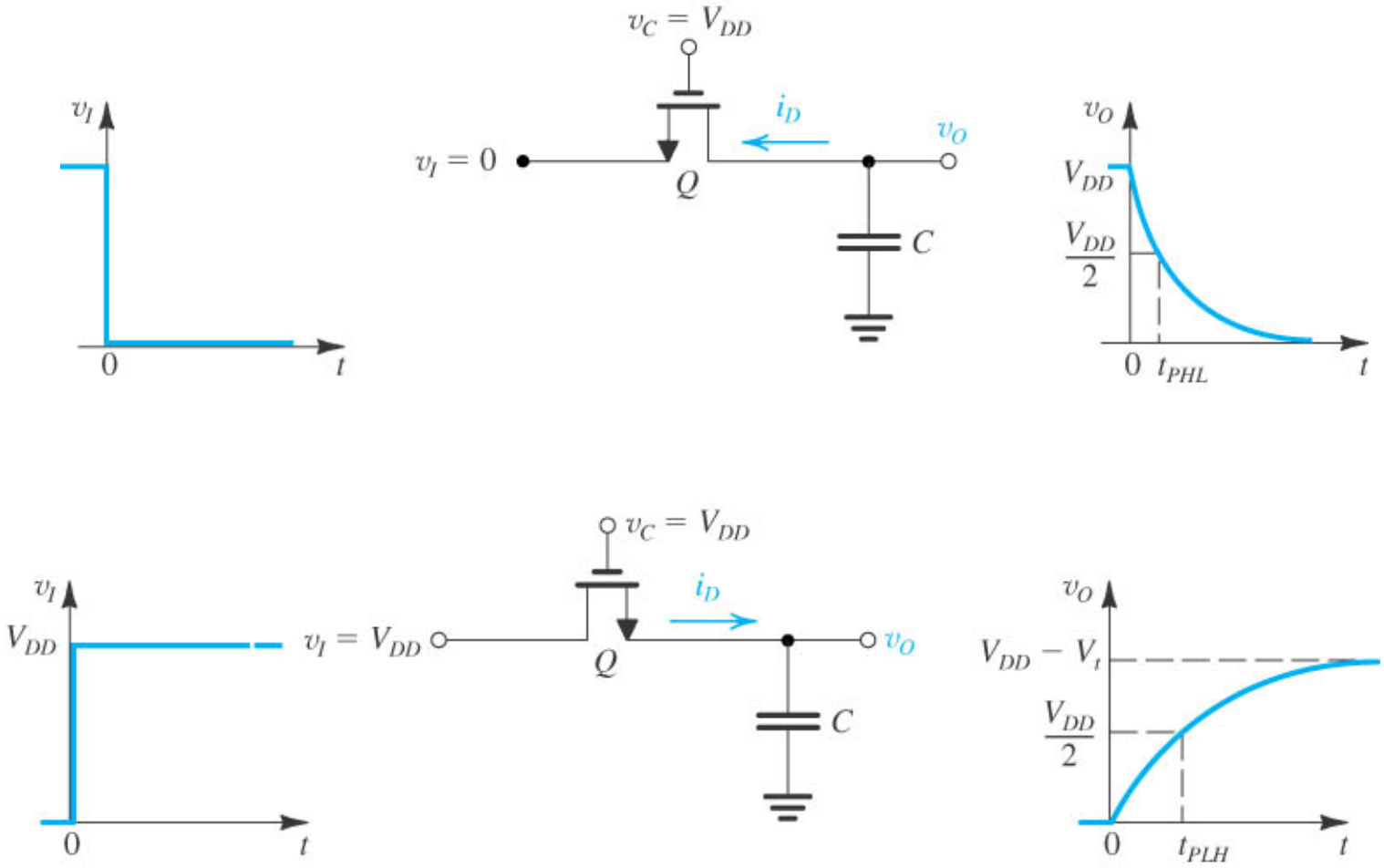
(c) I_{estat} e P_D

(d) t_{PLH}, t_{PHL} e t_P, supondo uma capacitância total na saída do inversor de 7 fF

Portas Lógicas com transistores de passagem

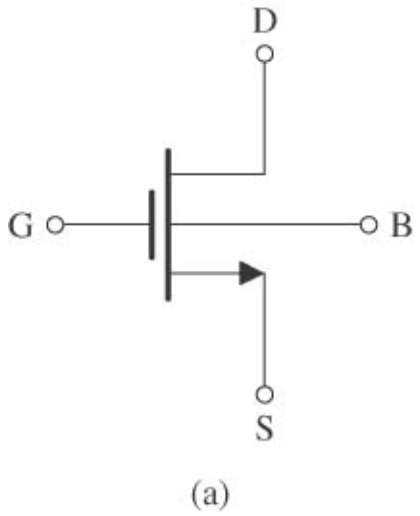


- **Figure 10.23** Conceptual pass-transistor logic gates. **(a)** Two switches, controlled by the input variables *B* and *C*, when connected in series in the path between the input node to which an input variable *A* is applied and the output node (with an implied load to ground) realize the function $Y = ABC$. **(b)** When the two switches are connected in parallel, the function realized is $Y = A(B + C)$.

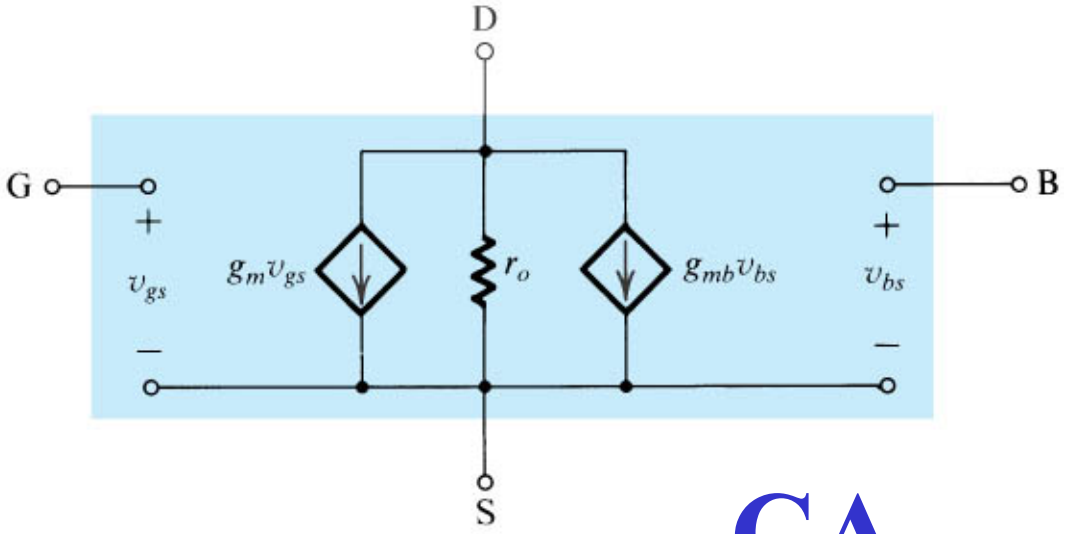


- **Figure 10.27 e 10.28 – Transistor NMOS como chave de passagem** .

Efeito de corpo



(a)



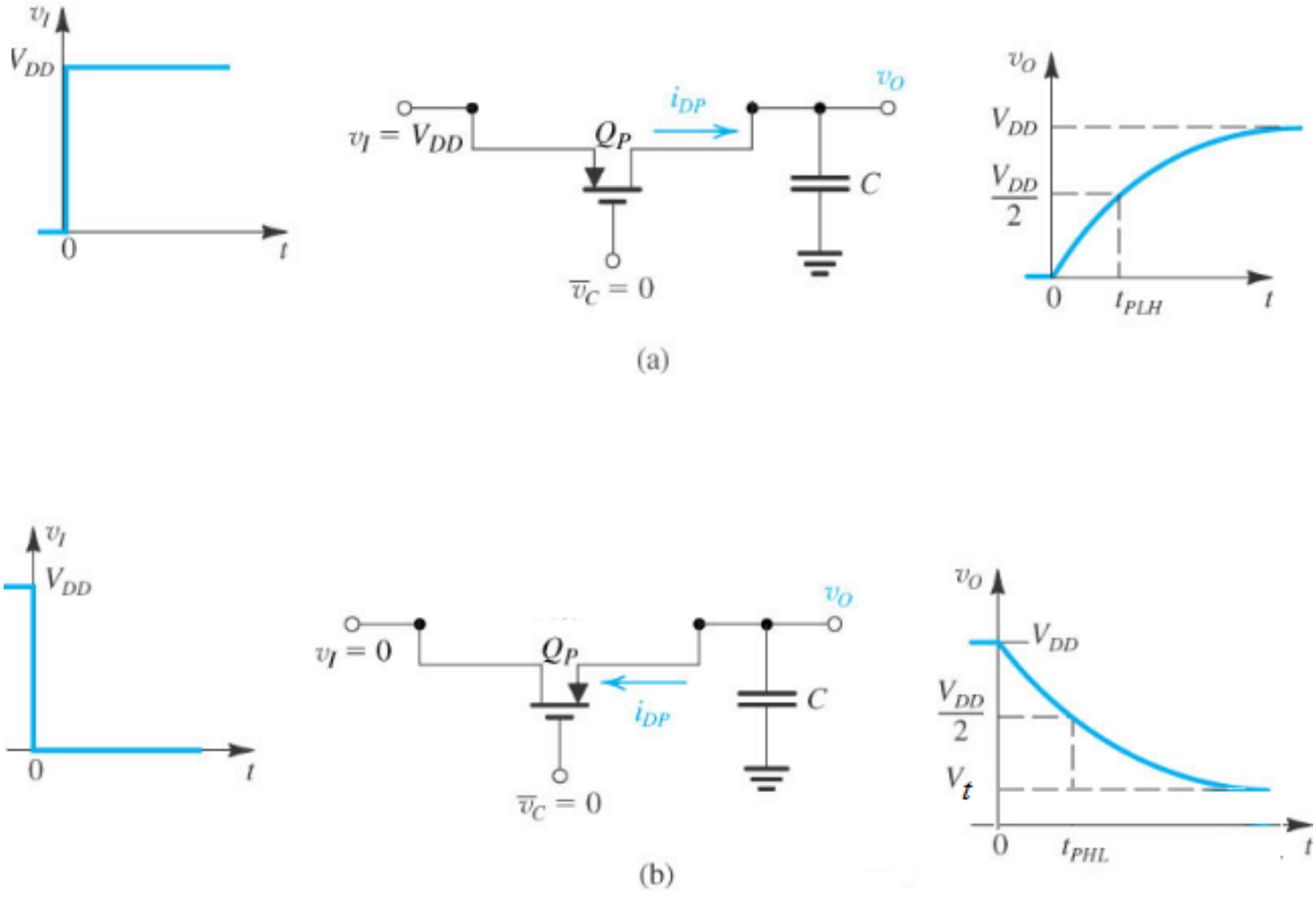
(b)

CA

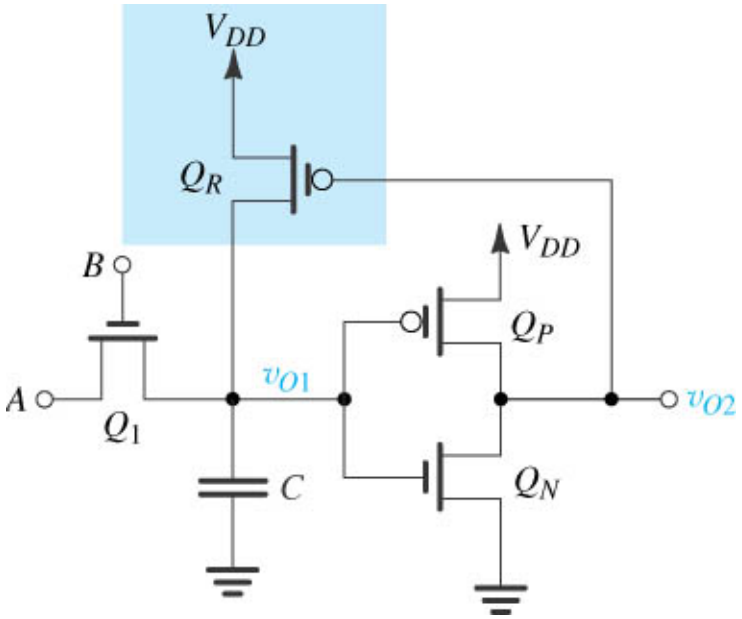
$$V_t = V_{t0}. + \gamma\left(\sqrt[2]{V_{SB}+2\cdot\phi_F} - \sqrt[2]{2\cdot\phi_F}\right)$$

CC

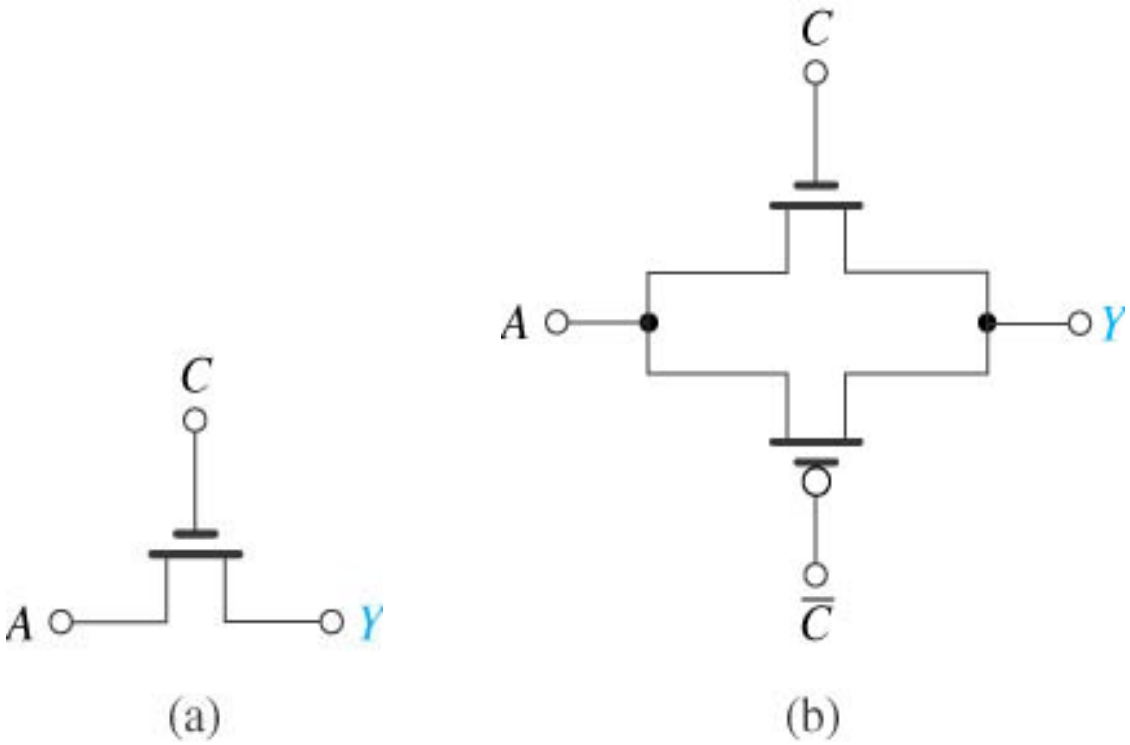
- **Figure 4.41** Small-signal equivalent-circuit model of a MOSFET in which the source is not connected to the body.



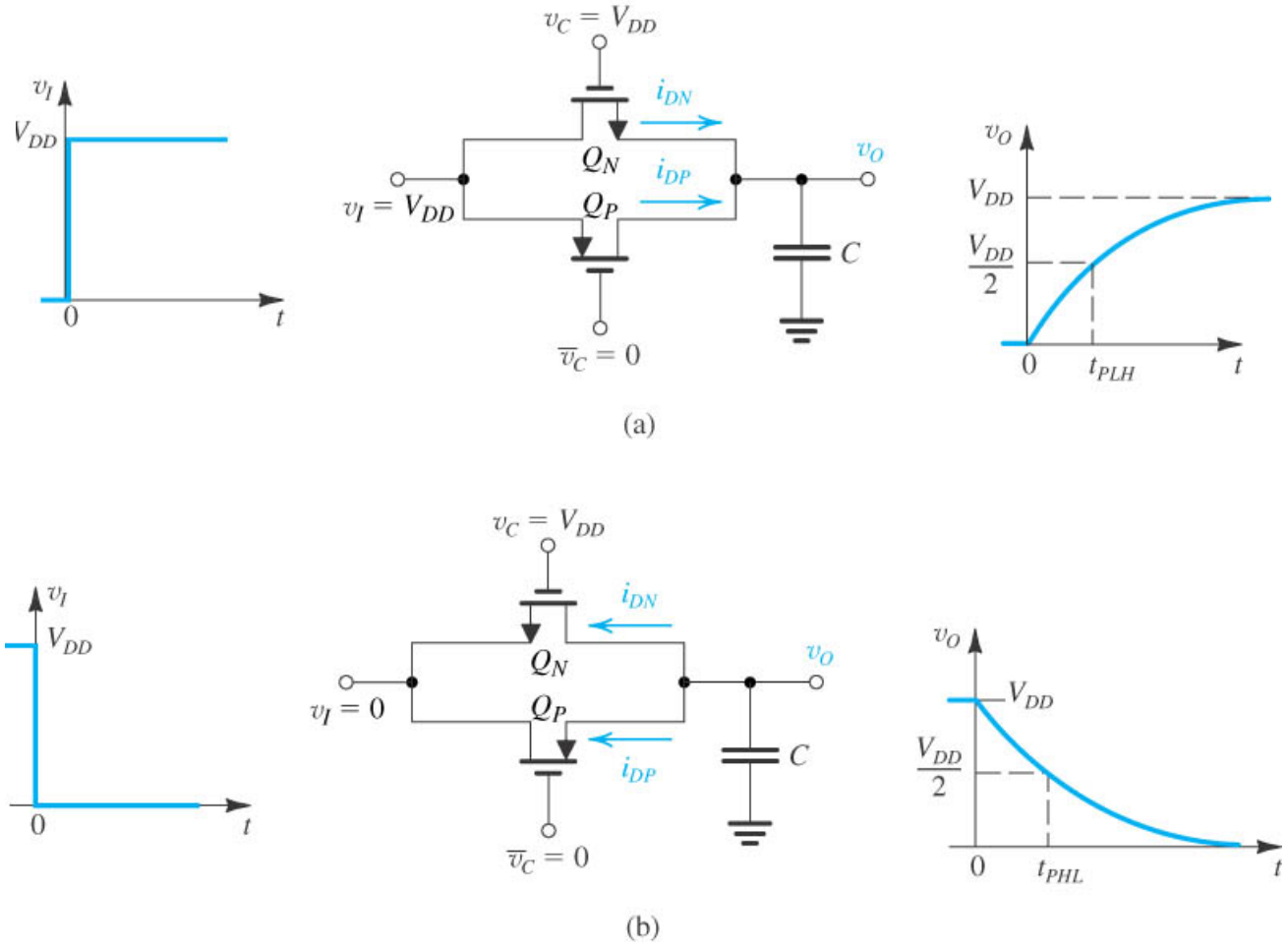
Transistor PMOS como chave de passagem .



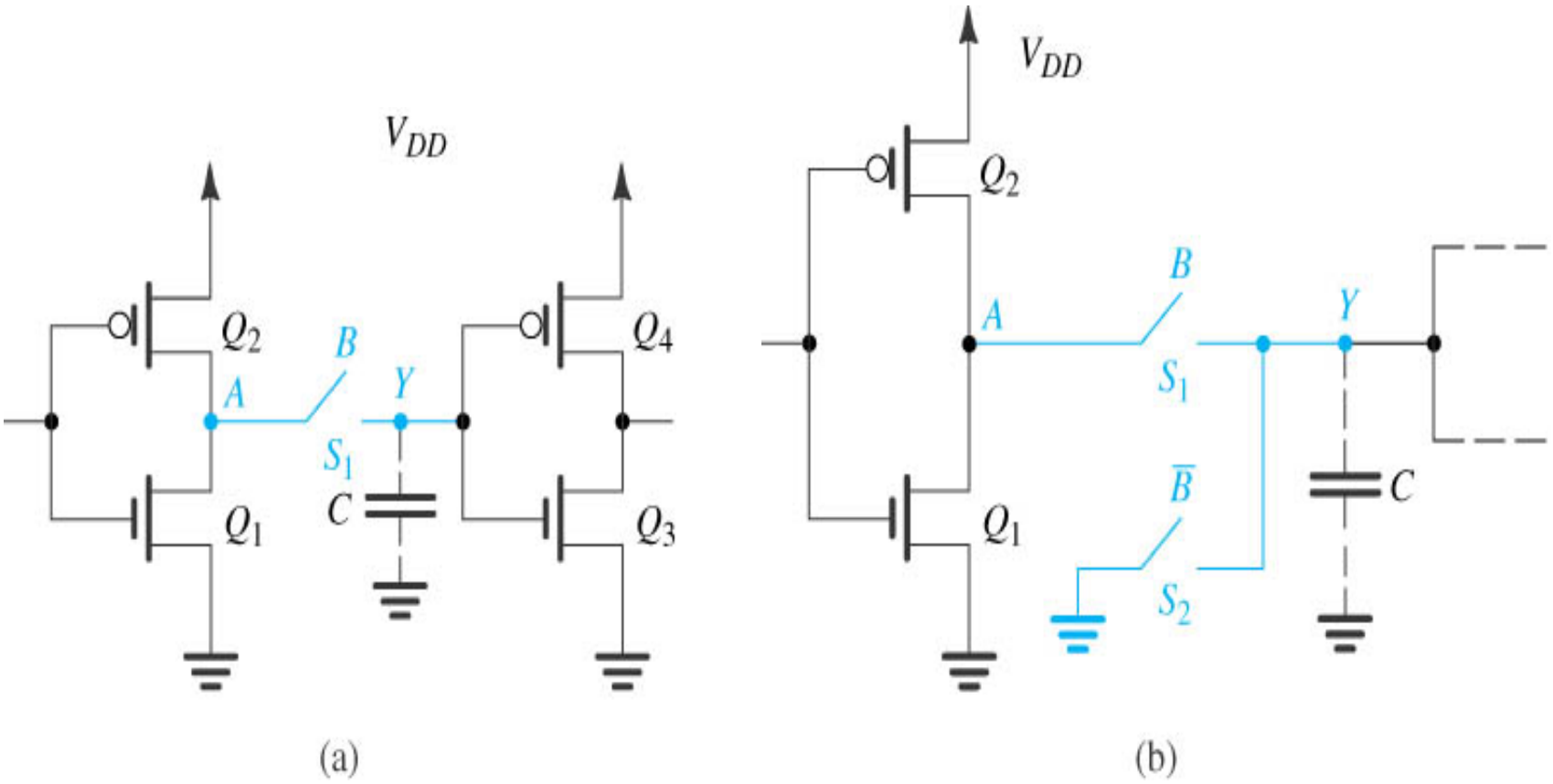
- **Figure 10.28** The use of transistor Q_R, connected in a feedback loop around the CMOS inverter, to restore the V_{OH} level, produced by Q_1, to V_{DD}.



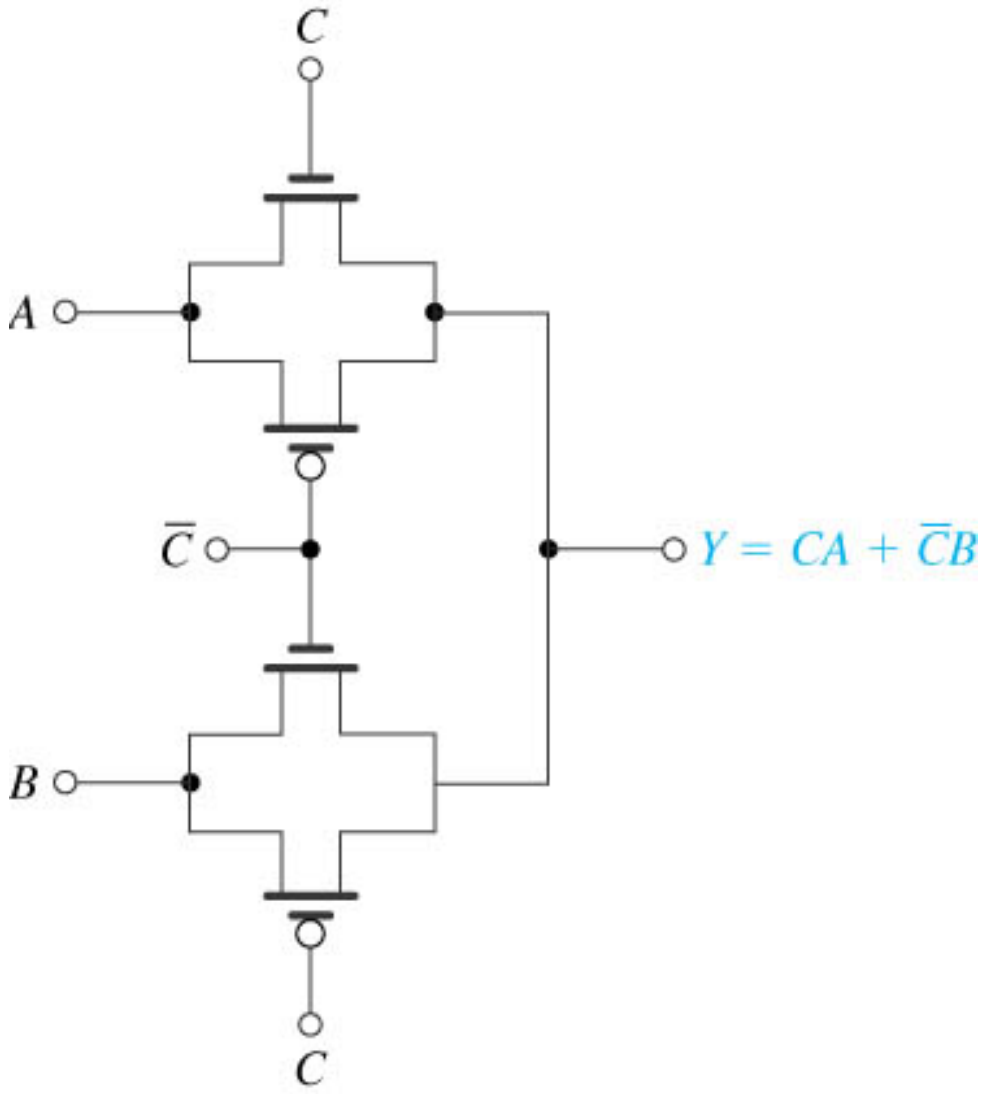
- **Figure 10.24** Two possible implementations of a voltage-controlled switch connecting nodes *A* and *Y*: **(a)** single NMOS transistor and **(b)** CMOS transmission gate.



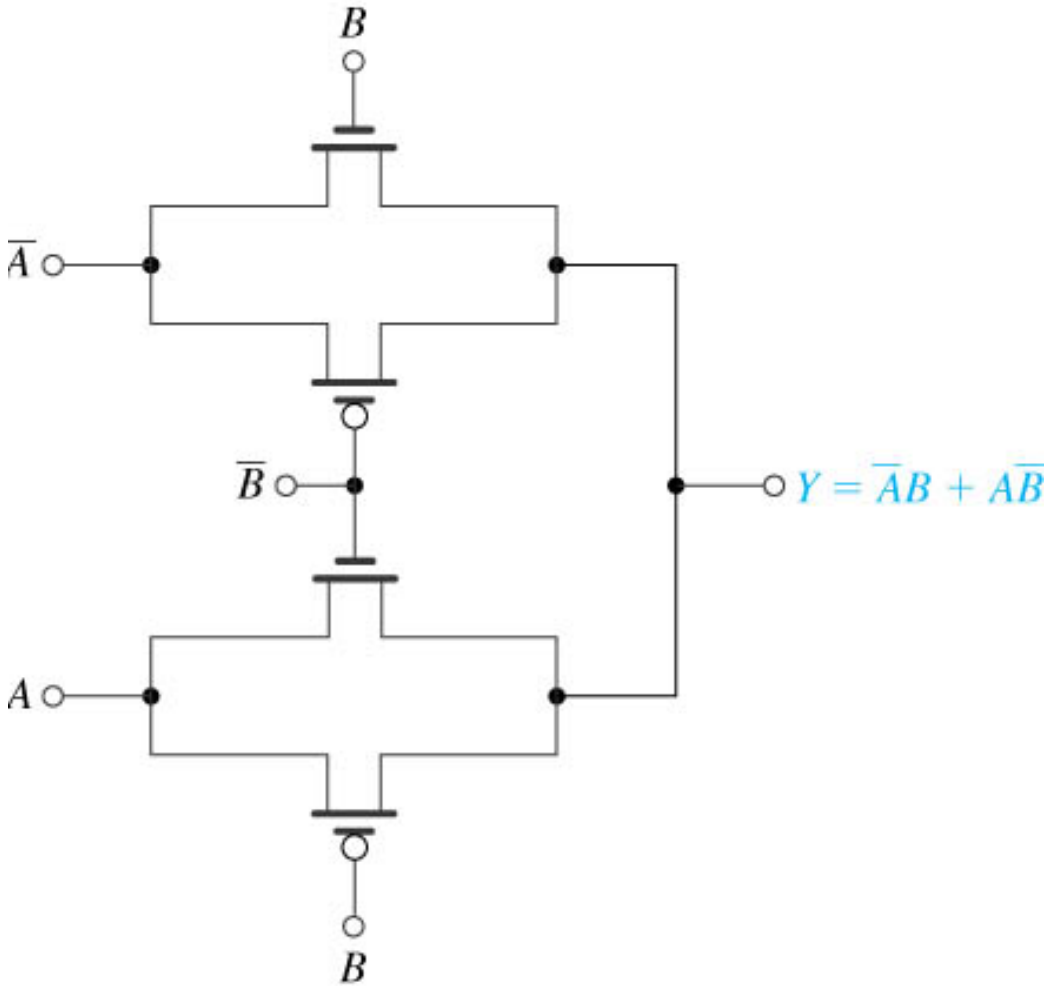
- **Figure 10.29** Operation of the transmission gate as a switch in PTL circuits with **(a)** v_I high and **(b)** v_I low.



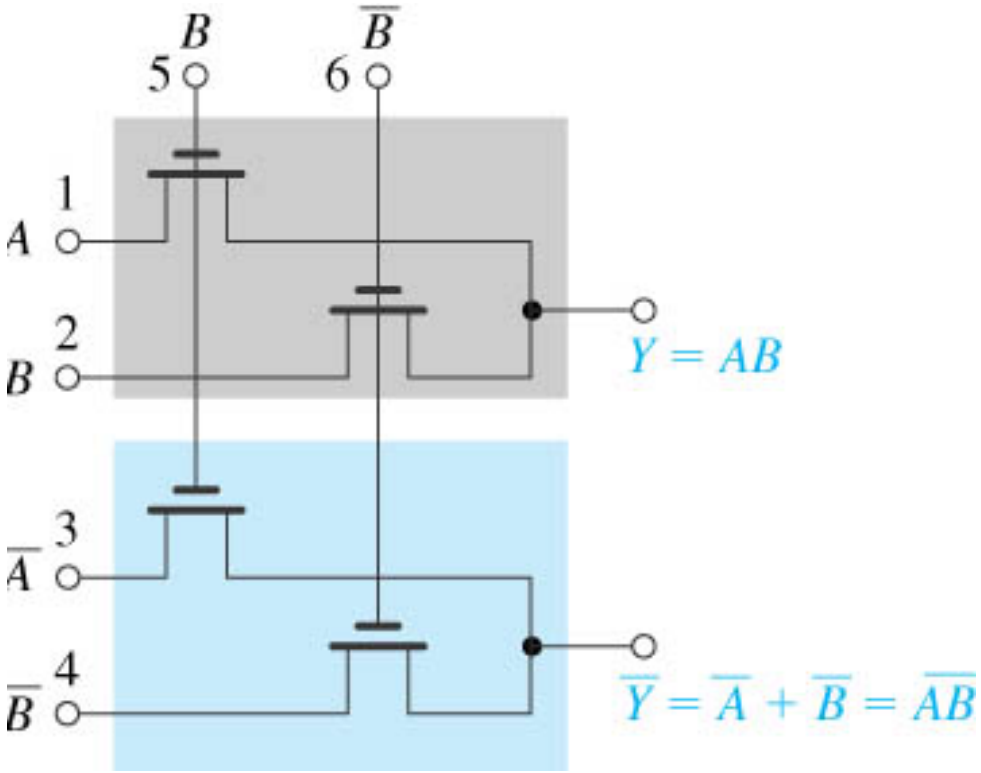
- **Figure 10.25** A basic design requirement of PTL circuits is that every node have, at all times, a low-resistance path to either ground or V_{DD}. Such a path does not exist in **(a)** when B is low and S_1 is open. It is provided in **(b)** through switch S_2.



- **Figure 10.30** Realization of a two-to-one multiplexer using pass-transistor logic.



- **Figure 10.31** Realization of the XOR function using pass-transistor logic.



- **Figure 10.32** An example of a pass-transistor logic gate utilizing both the input variables and their complements. This type of circuit is therefore known as complementary pass-transistor logic or CPL. Note that both the output function and its complement are generated.