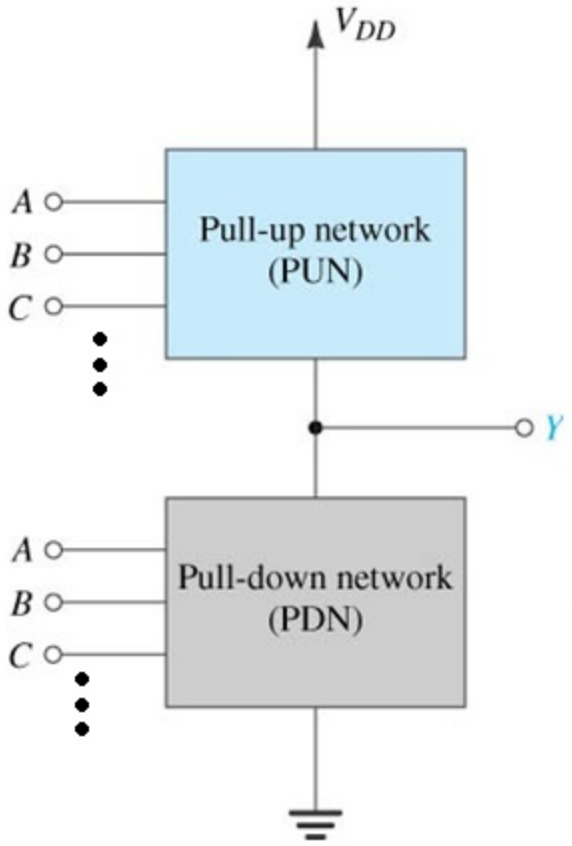
PSI3024 – Eletrônica

Aula 30

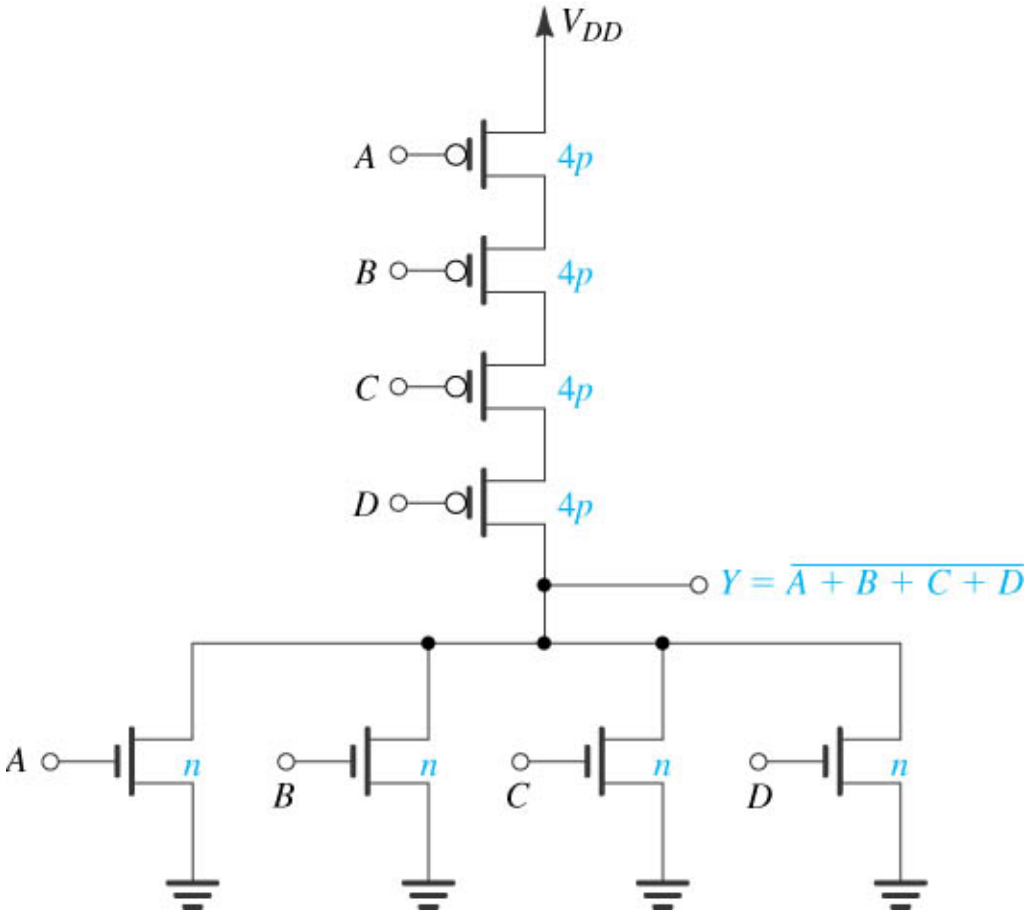
2023

Portas Lógicas: Implementação

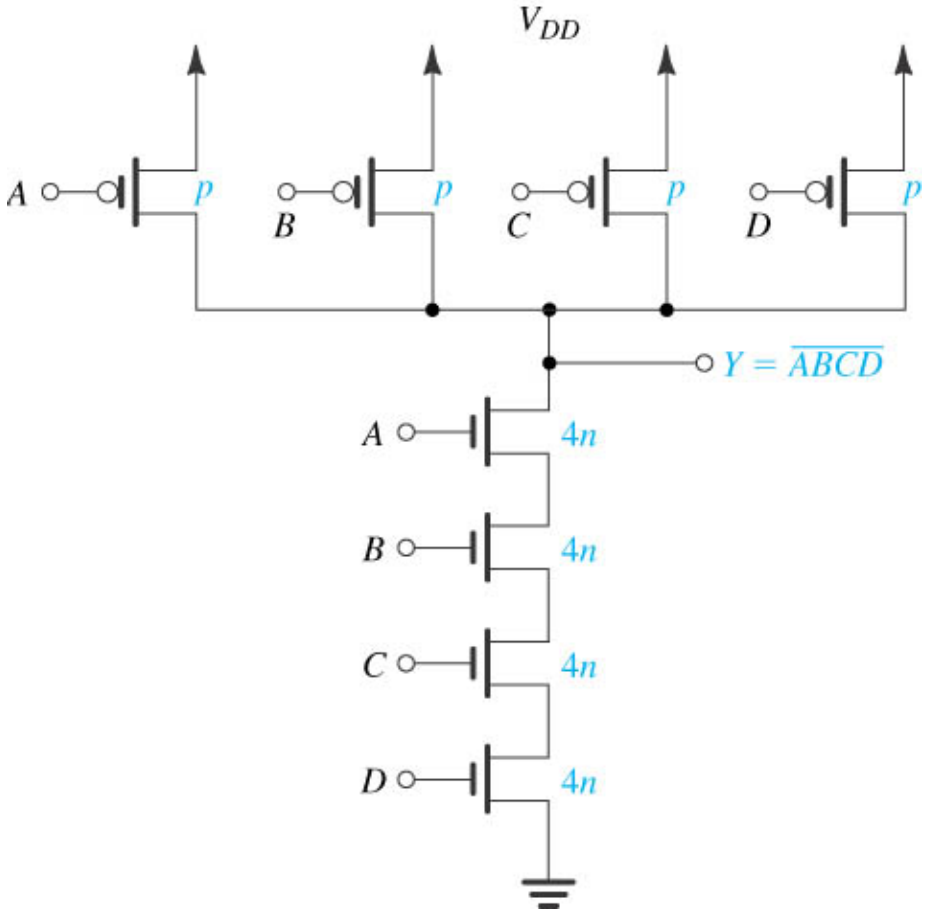


$$Y = \overline{A}$$

$$\overline{Y} = A$$

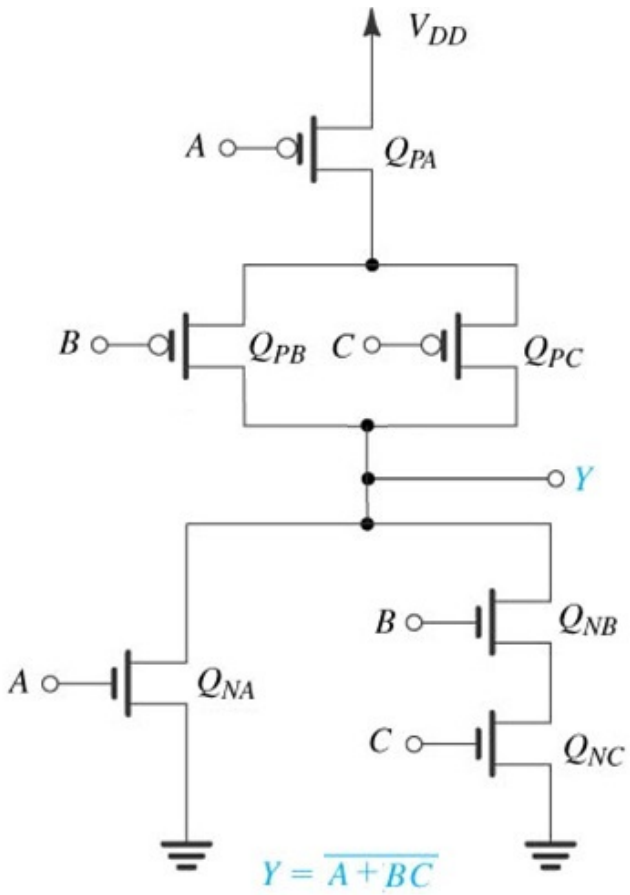


- **Figure 10.16** Proper transistor sizing for a four-input NOR gate. Note that *n* and *p* denote the (*W*/*L*) ratios of Q_N and Q_P, respectively, of the basic inverter.



- **Figure 10.17** Proper transistor sizing for a four-input NAND gate. Note that *n* and *p* denote the (*W*/*L*) ratios of Q_N and Q_P, respectively, of the basic inverter.

$$Y = \overline{A + B.C} = \overline{A}.\left(\overline{B} + \overline{C}\right), \qquad \overline{Y} = A + B.C$$



Rede Pull-up

$Y = \overline{A}(\overline{B} + \overline{C})$

Rede Pull-down

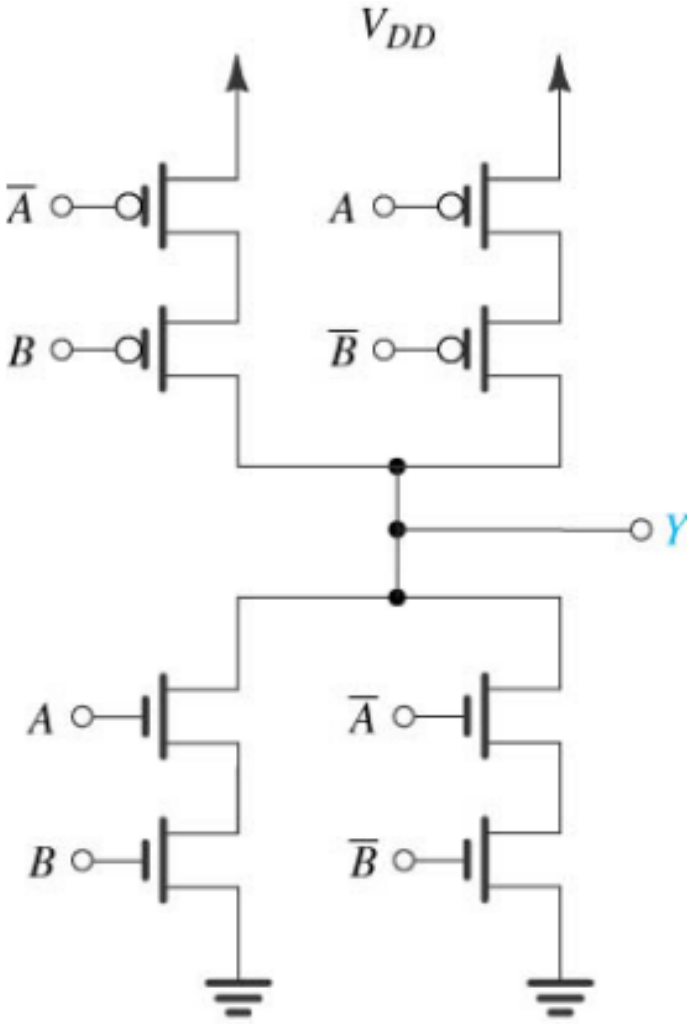
$\overline{Y} = A + BC$

Figura 6

Ou-Exclusivo

$$Y = A.\overline{B} + \overline{A}.B$$

$$\overline{Y} = A.B + \overline{A}.\overline{B}$$



- **Figure 10.15** Realization of the exclusive-OR (XOR) function: **(a)** The PUN synthesized directly from the expression in Eq. (10.25). **(b)** The complete XOR realization utilizing the PUN in (a) and a PDN that is synthesized directly from the expression in Eq. (10.26). Note that two inverters (not shown) are needed to generate the complemented variables. Also note that in this XOR realization, the PDN and the PUN are not dual networks; however, a realization based on dual networks is possible (see Problem 10.27).

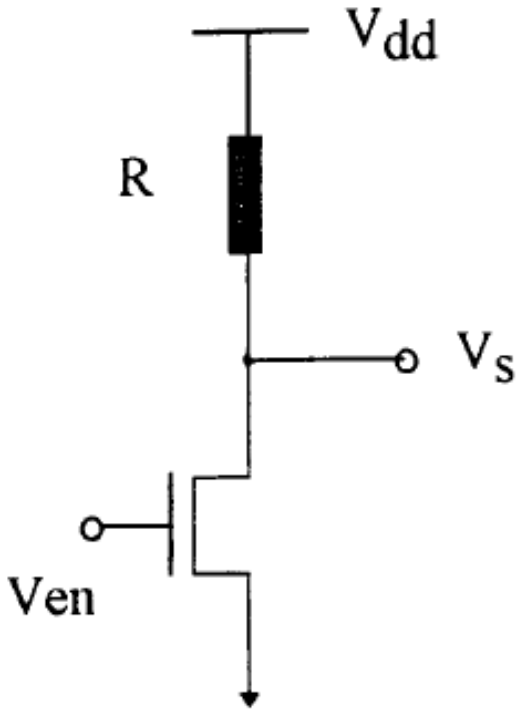
CIRCUITOS INVERSORES MOS

O circuito inversor é composto de dois dispositivos:
- um transistor de comando (por exemplo, nMOS)
- um elemento de carga.

O elemento de carga pode ser do tipo:

a) resistiva
b) transistor de enriquecimento em triodo
c) transistor de enriquecimento em saturação
d) transistor de depleção
e) transistor tipo pMOS

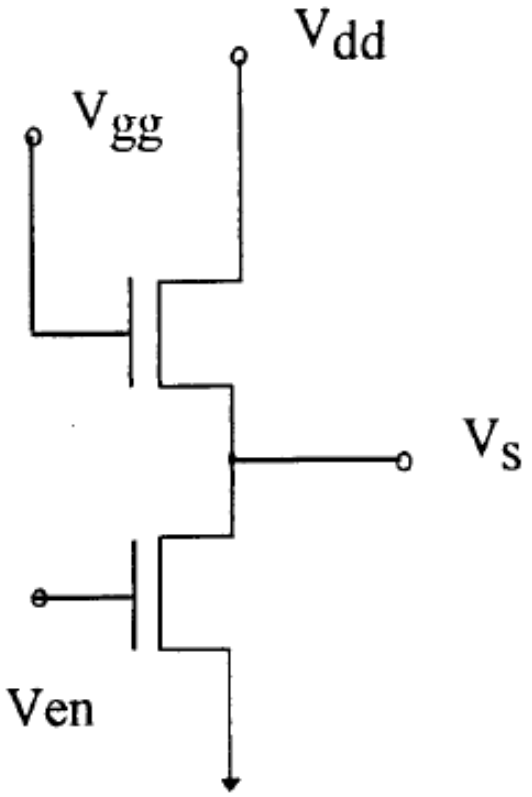
a) Carga resistiva



Ven	"0"	"1"
V_S(V)	~V_{dd}	~0,4V

Neste caso, Vs("0") depende do valor de R.

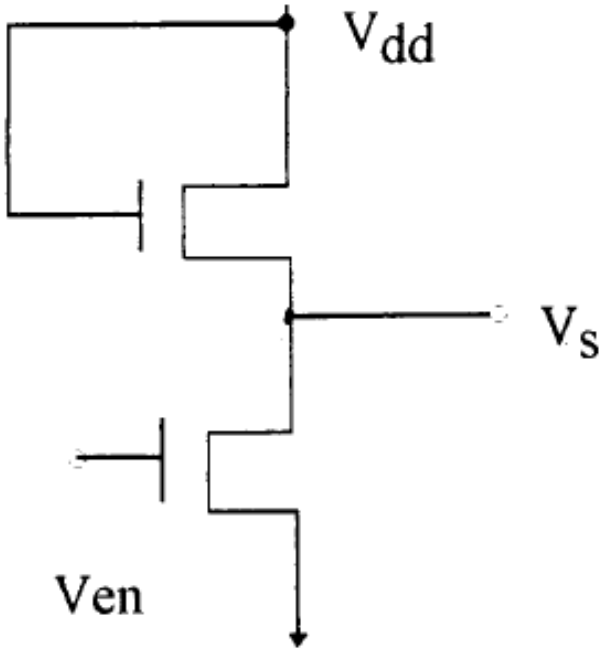
b) transistor de enriquecimento em triodo



Ven	"0"	"1"
$V_S(V)$	~V_{dd}	~0,4

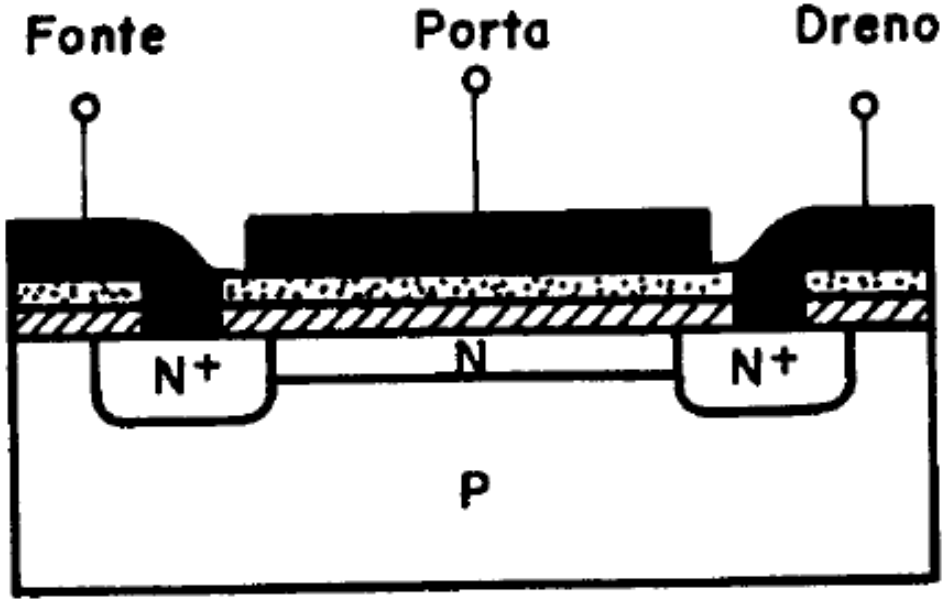
Obs: $V_{gg} > V_{dd} + V_t(V_s)$

c) transistor de enriquecimento em saturação



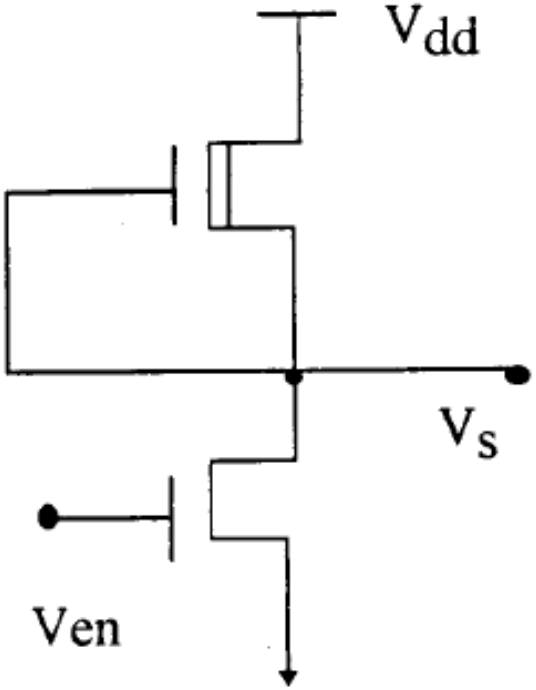
Ven	"0"	"1"
$V_S(V)$	$V_{dd} - V_t$	0,4

TRANSISTOR TIPO DEPLEÇÃO



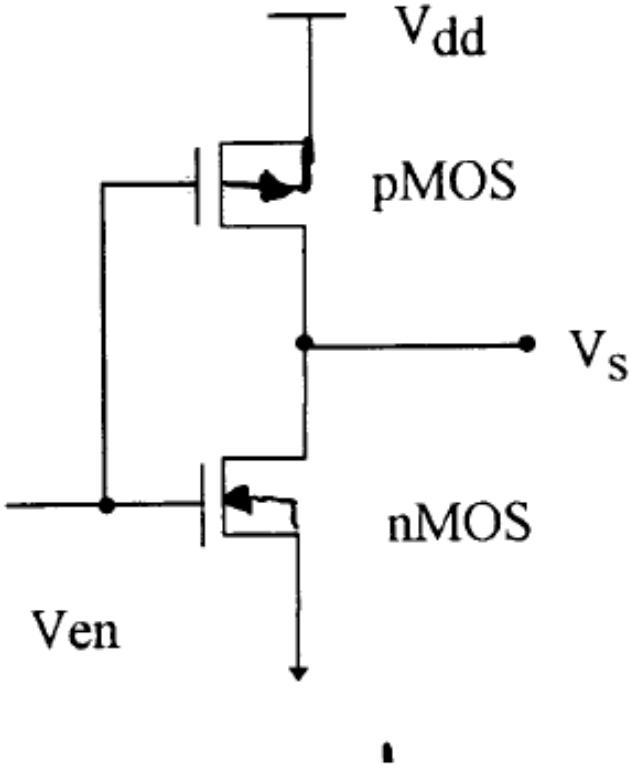
$$V_{TN} = +\frac{(2.q.N_A.\varepsilon_o.\varepsilon_s.2.\phi_F)^{1/2}}{C_{ox}} - \frac{Q_{ef}}{C_{ox}} - \frac{Q_{\mathrm{Im}}}{C_{ox}} + 2.\phi_F + \phi_{MS}$$

d) transistor de depleção



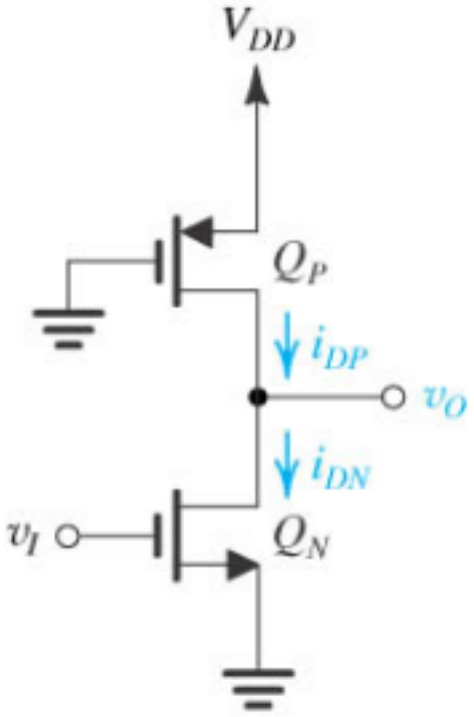
Ven	"0"	"1"
V_S	~V_{dd}	~0,4

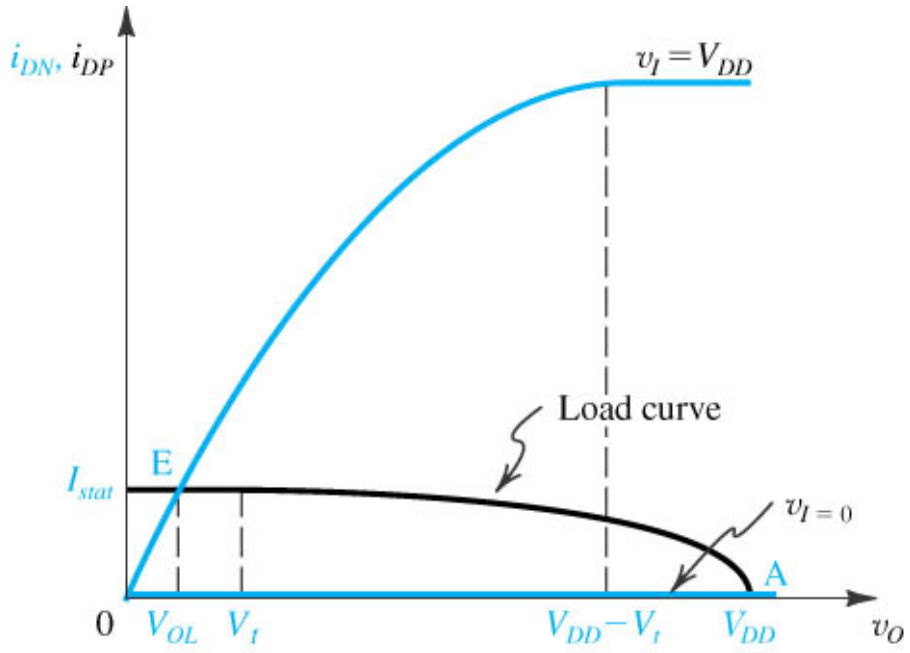
e) transistor tipo pMOS (inversor CMOS)

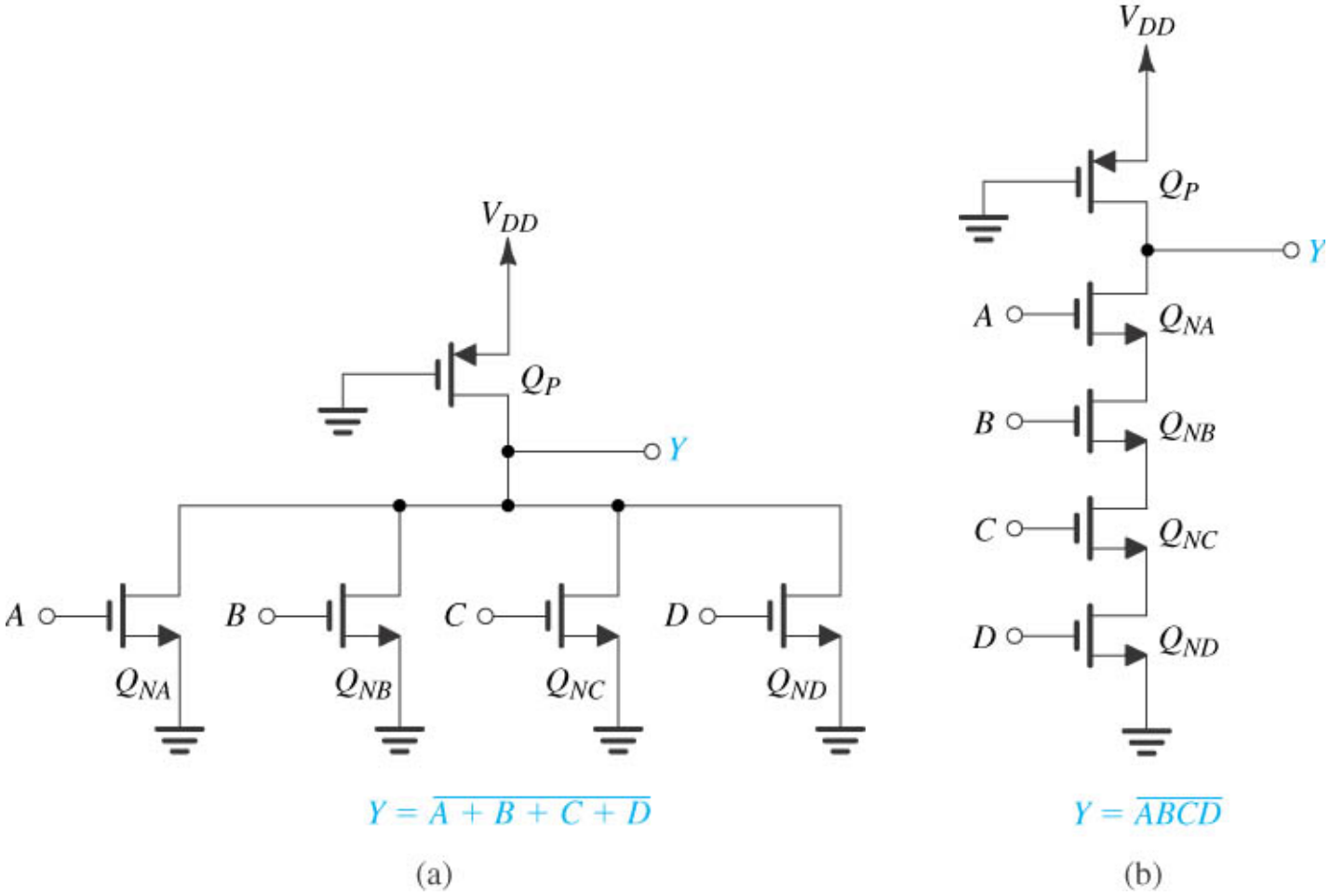


Ven	"0"	"1"
V_S(V)	V_{dd}	0

Inversor pseudo-NMOS







- **Figure 10.22** NOR and NAND gates of the pseudo-NMOS type.