# Growth, fabrication techniques for nanostructures

# Bulk crystal and heterostructure growth

Though technological methods and especially regimes of growing various types of crystals are generally different, they have a lot in common. Here we consider the common steps in growing pure materials using Si technology as an example.

Single-crystal growth

The following three steps are necessary to produce high-quality silicon crystals:
(i) production of metallurgical-grade silicon (impurity level $\approx 5 \times 10^{16}$ cm$^{-3}$);
(ii) improvement of the latter material up to electronic-grade silicon (the level of impu- rities is reduced to $\approx 5 \times 10^{13}$ cm$^{-3}$ or less); and
(iii) conversion to single-crystal Si ingots.

Metallurgical-grade silicon is typically produced via reaction of silicon dioxide ($SiO_2$) with C in the form of coke:

$$\mathbf{SiO_2 + 2C \rightarrow Si + 2CO}$$

which requires very high temperature ($\approx$1800 °C). Coke is a coal from which most of the gases have been removed. The silicon obtained at this step is not single-crystalline and is not pure enough for electronic applications, though it is good for some metallurgical applications such as the production of stainless steel.

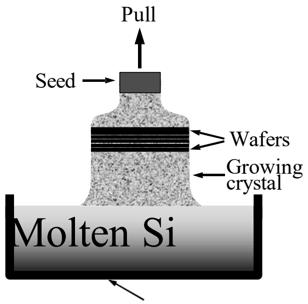
Further reductions in impurities can be achieved by carrying out the following reaction of the silicon with dry HCl:

$$Si + 3HCl \rightarrow HSiCl_3 + H_2.$$

The trichlorosilane $HSiCl_3$, which is typically in a liquid state with a boiling point of 32 °C. Simultaneously with $HSiCl_3$, other chlorides of impurities, such as $FeCl_3$, are formed. Since their boiling points are different, the simple fractional distillation technique can be applied: the mixture of $HSiCl_3$ and other impurity chlorides is heated and then condensed in a series of distillation towers at appropriate temperatures. By this technique $HSiCl_3$ is separated from impurities. The following reaction with $H_2$ then converts the trichlorosilane into highly pure electronic-grade silicon:

$$2HSiCl_3 + 2H_2 \rightarrow 2Si + 6HCl.$$

The pure Si obtained by this process is still polycrystalline. The final process, which converts polycrystalline silicon into single-crystal Si ingots, is based on the Czochralski method.




Czochralski method for the growth of bulk semiconductors.

In the Czochralski method, a seed Si crystal provides a template for growth. First, this seed crystal is lowered into the molten Si material. (The melting point of Si is 1412 °C.)

Then it is raised very slowly so that the molten material touching the seed crystallizes as the seed is withdrawn from the molten material. Rotation of the seed crystal, stabilization of the temperature field, and other tricks are used to grow highly homogeneous ingots.

Importantly, this technology facilitates doping in the course of crystal growth. Indeed, one can intentionally add precise quantities of impurities (dopants) into semiconductor melts to provide for regions of crystallization having the desired doping concentrations. This technique is used widely in growing silicon, germanium, and, with some modifications, compound semiconductors.

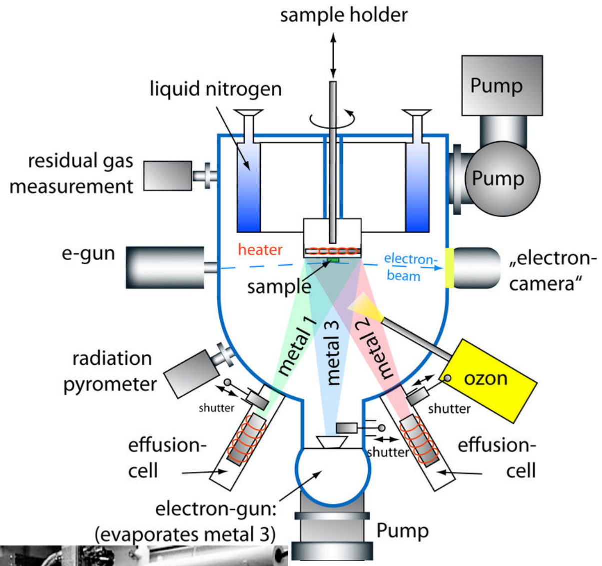
As the single-crystal ingot is grown, it is mechanically processed to obtain wafers of thicknesses of hundreds of micrometers,

# Epitaxial Growth

- Fabrication of a crystal layer upon a wafer of a compatible crystal makes it possible to obtain very well-controlled growth regimes and to produce high-quality crystals with the desired crystalline orientation at temperatures typically well below the melting point of the substrate.

- During the epitaxial growth, several methods of delivering the necessary atoms to the growing layer can be used. The most developed methods are *molecular-beam epitaxy* (MBE), *chemical-vapor deposition* (CVD), and *liquid-phase epitaxy* (LPE) ou PVD processes.

# Molecular-beam epitaxy

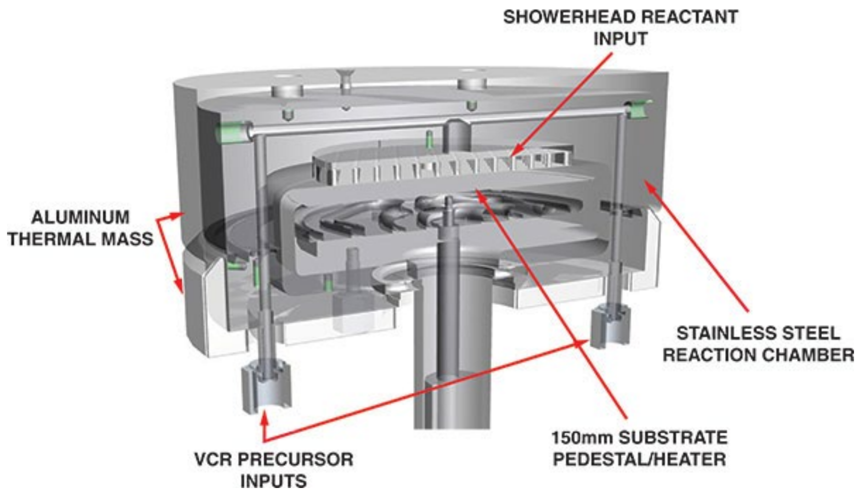


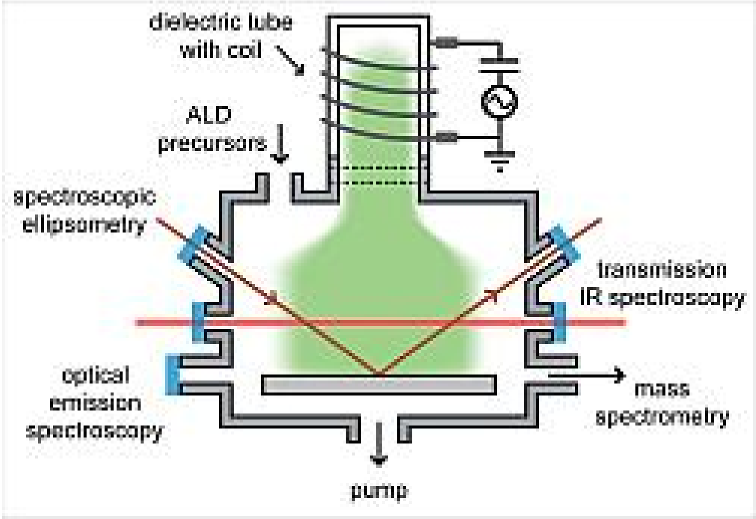


The MBE method can be realized in a high vacuum, where molecular or atomic beams deliver onto a substrate the necessary components for growing the desired crystalline layer. For example, suppose that we want to grow an AlGaAs layer on GaAs. Then, the substrate will be GaAs and the atomic beams are fluxes of the elements Al, Ga, and As, as well as beams of dopants (typically, Si is used for n-doping and Be for p-doping). Sources of the elements are contained in separately heated chambers. The evaporated elements form beams, which are separately and closely controlled, collimated, and directed onto the substrate surface. Typical flux densities in the beams are of $10^{14}$–$10^{16}$ atoms $cm^{-2}$ $s^{-1}$. The substrate is held at relatively low temperature (≈600 °C for GaAs), while densities of the components in the beams are large. This provides effective growth of the layer. A slow growth rate (≈1 monolayer per second), which is often referred to as layer-by-layer growth, results in the growth of a high-quality layer. By controlling shutters for each beam, one can produce abrupt changes in crystal compositions and doping concentrations on the scale of one monolayer.

# Atomic Layer Deposition

This epitaxial methods allows one to realize a low-temperature growth regime and to use high-purity chemicals for delivering the necessary atoms for growth of a crystalline layer. The layers can be grown onto a seed crystal or substrate from mixtures of chemical vapors containing both semiconductor elements and dopants. In ALD processes grown with thickness control of the order of one monolayer. Different types of doping – uniform doping, modulation doping, and delta-doping – are realized with high accuracy. Since in the chemical reactor the partial pressures of chemicals are much higher than the pressure in the molecular beams of the MBE method, the rate of crystal growth realized.



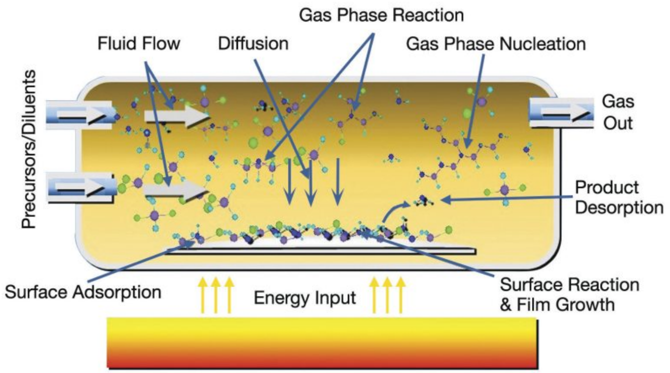



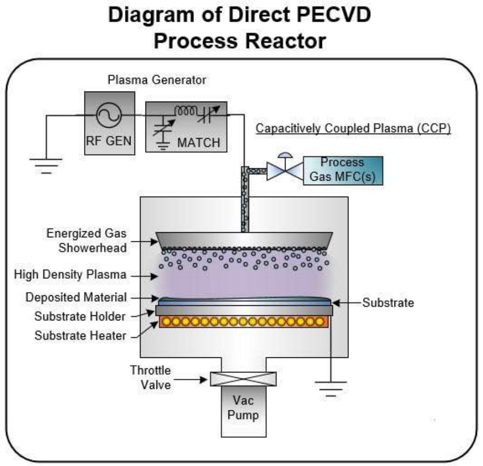
# Chemical-vapor deposition - CVD

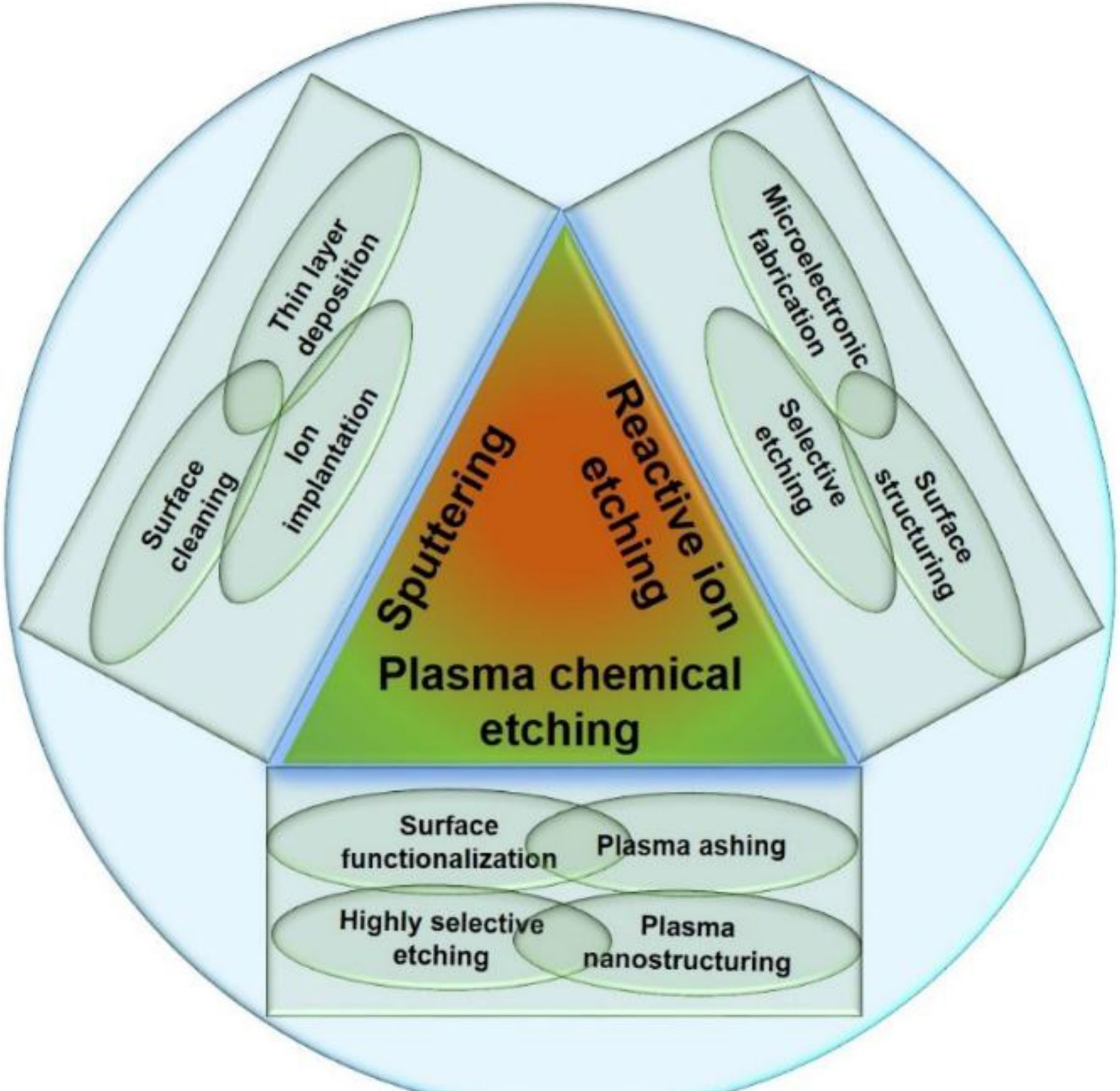
In the CVD method is higher than that of MBE. The former may be used in industrial production, while the latter is rather well suited for research laboratories The chemical-vapor deposition is conducted in a reaction chamber called a *reactor*. In the reactor, a typical pressure of chemicals is $\approx 10^4$ Pa and heating is achieved by power from a microwave radio-frequency source. In the case of growth of Si layers, several different gases containing Si atoms can be used. They include silicon tetrachloride ($SiCl_4$), silane ($SiH_4$), and dichlorosilane ($SiH_2Cl_2$). In the use of silicon tetrachloride, the following reaction with hydrogen occurs:

$$SiCl_4 + 2H_2 \rightarrow Si + 4HCl.$$

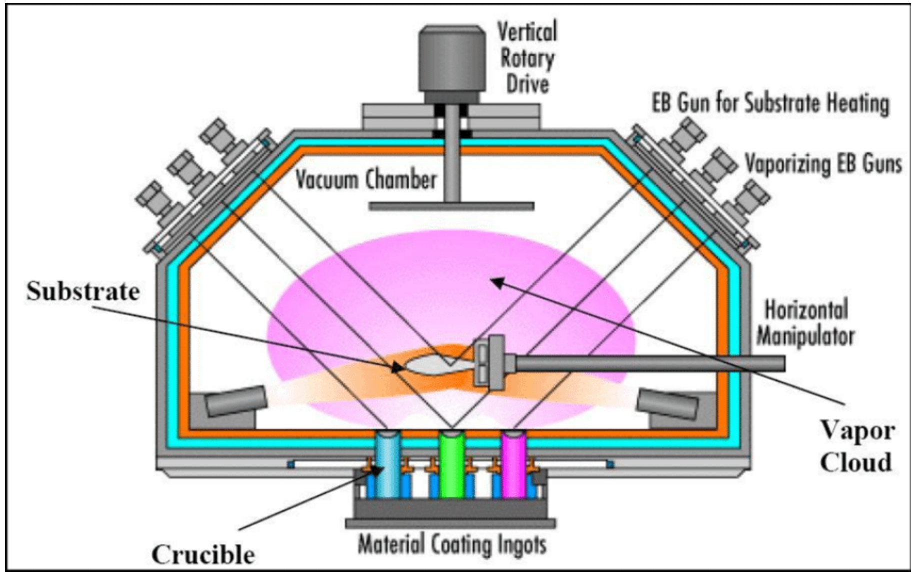
The reaction can be conducted at temperatures in the range of 1150–1250 °C. In the case of using silane and dichlorosilane, the reaction can be conducted at even lower temperatures (1000–1100 °C). These temperatures are well below the melting point of Si. Thus, these reactions release atoms of Si, and the relatively low-temperature regimes provide efficient crystal growth onto the seed.



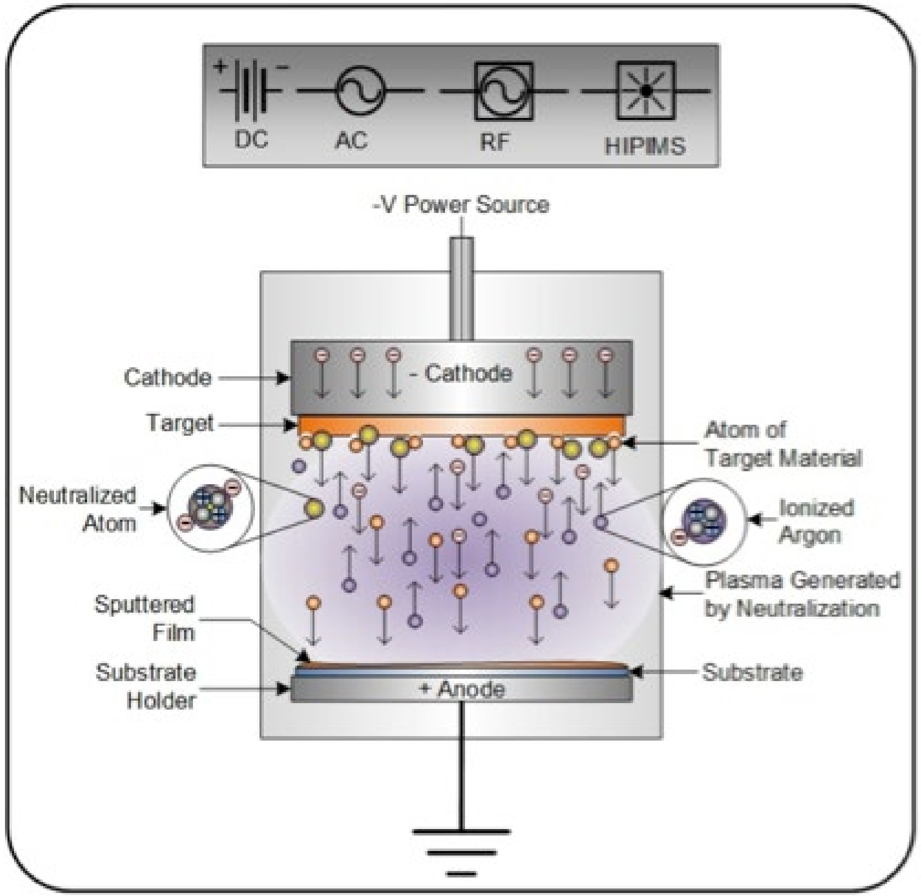




Thin layer deposition
Surface cleaning
Ion implantation
Sputtering
Reactive ion etching
Microelectronic fabrication
Selective etching
Surface structuring
Plasma chemical etching
Surface functionalization
Plasma ashing
Highly selective etching
Plasma nanostructuring

# Physical Vapor Deposition- PVD




Electron Beam -PVD




Sputtering

# Nanolithography

- Nanolithography is the branch of nanotechnology concerned with the study and application of the nanofabrication of nanometer-scale structures, meaning nanopatterning with at least one lateral dimension between the size of an individual atom and approximately 100 nm. The term nanolithography is derived from the Greek words “nanos”, meaning dwarf; “lithos”, meaning rock or stone; and “graphein” meaning to write. Therefore the literal translation is "tiny writing on stone", however nowadays one understands something different whenever this term is associated with nanotechnology. Nanolithography is used e.g. during the nano- fabrication of leading-edge semiconductor integrated circuits (nanocircuitry), for nanoelectromechanical systems (NEMS) or for almost any other fundamental application across various scientific disciplines in nanoresearch.

# Classification of lithographic techniques

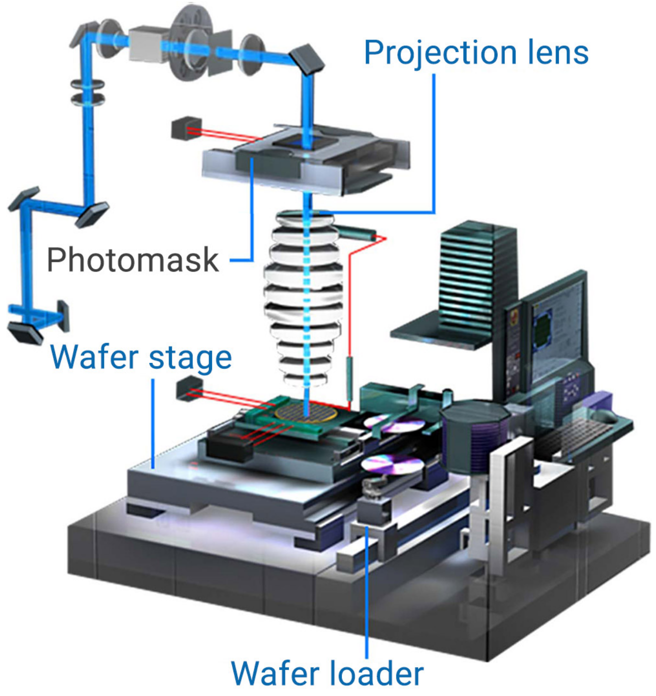
There are many techniques through which micro/nano patterning could be possible.

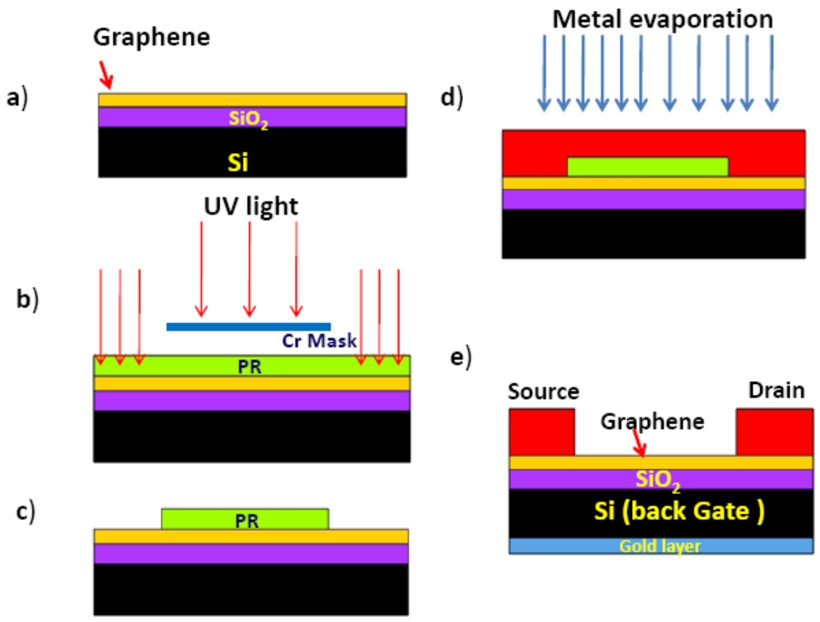
- Photolithography – an conventional and classical method
- Ion beam Lithography
- X-ray lithography
- Electron beam lithography
- Alternate Nanolithographic Techniques
  - Micro-contact printing
  - Nano-imprint lithography
  - Scanning Probe lithography

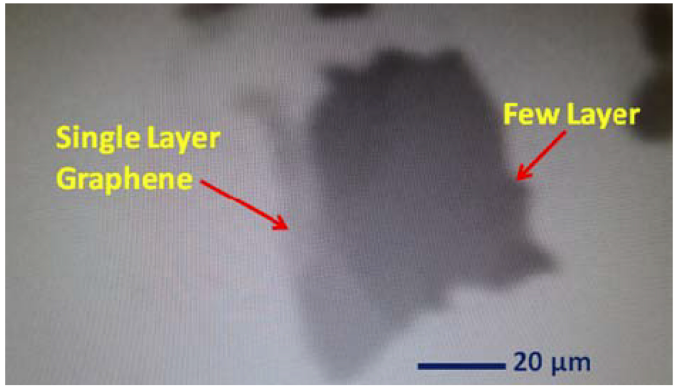
# Photolithography – A conventional and classical method (UV – Deep UV)

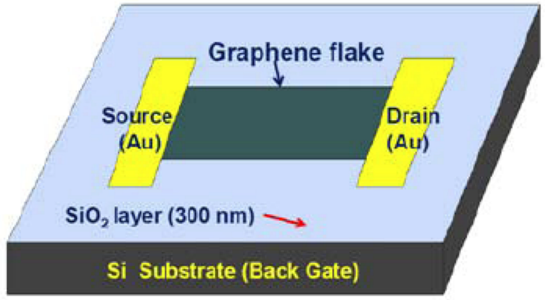
•Lithography consists of patterning substrate by employing the interaction of beams of photons or particles with materials. Photolithography is widely used in the integrated circuits (ICs) manufacturing. The process of IC manufacturing consists of a series of 10-20 steps or more, called mask layers where layers of materials coated with resists are patterned then transferred onto the material layer.

• A photolithography system consists of a light source, a mask, and an optical projection system. Photoresists are radiation sensitive materials that usually consist of a photo-sensitive compound, a polymeric backbone, and a solvent. Resists can be classified upon their solubility after exposure into: positive resists (solubility of exposed area increases) and negative resists (solubility of exposed area decreases).



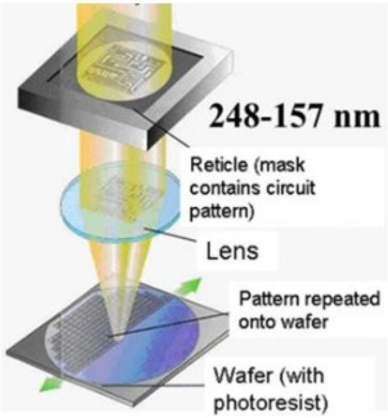



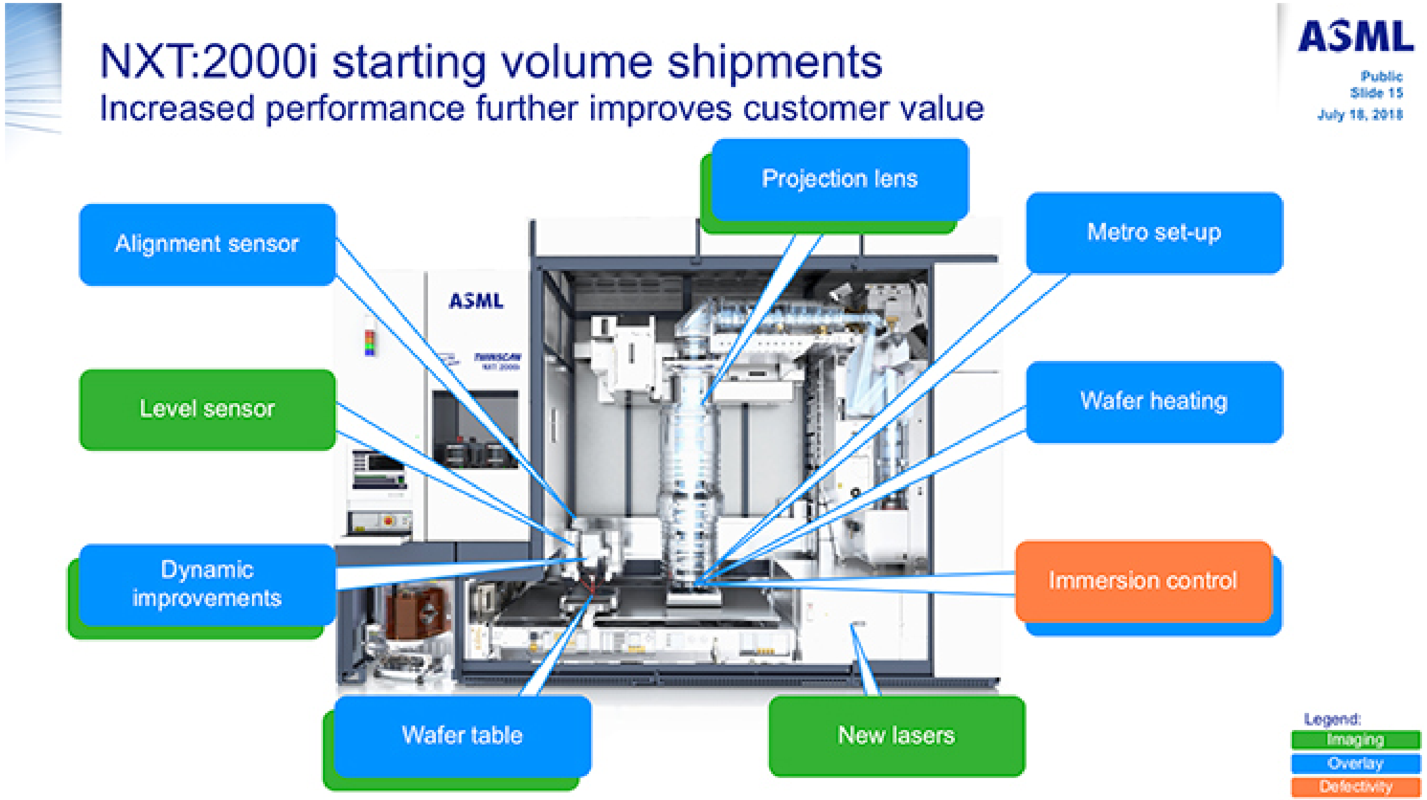

(a) (b)

Photolithographic process of electrode patterning on graphene. (a) Graphene flake on Si/$SiO_2$ substrate (b) Photoresist is spin-coated over the graphene flake and UV light illuminated through Cr mask. (c) the pattern after de- veloping process (d) gold (Au) evaporation through thermal evaporation technique (e) after lift-off process, the device with source and drain electrode structure with back-gate configuration. (Venugopal, 2011).


TR-SES-200 Vacuum UV-VIS spectrometer

- High Resolution Transmission and Reflection Evaluation system (110 nm ~ 900nm)
- Absolute method for Reflectance and Transmittance measurement
- Multiple Measurements at Any Angle without Sample Repositioning manually (Both Rotating and Tilting Sample Wheel, Rotating Detector)
- Solid Auto Sampler Wheel for Various Shape and Size



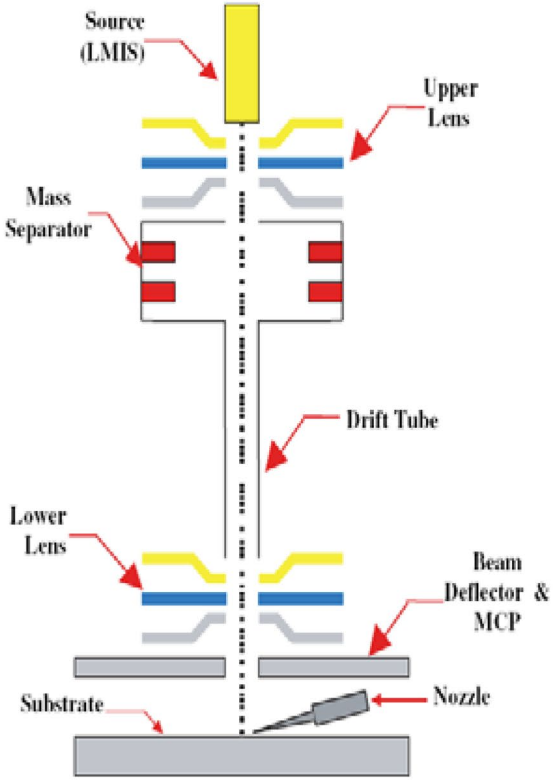



# Ion beam lithography

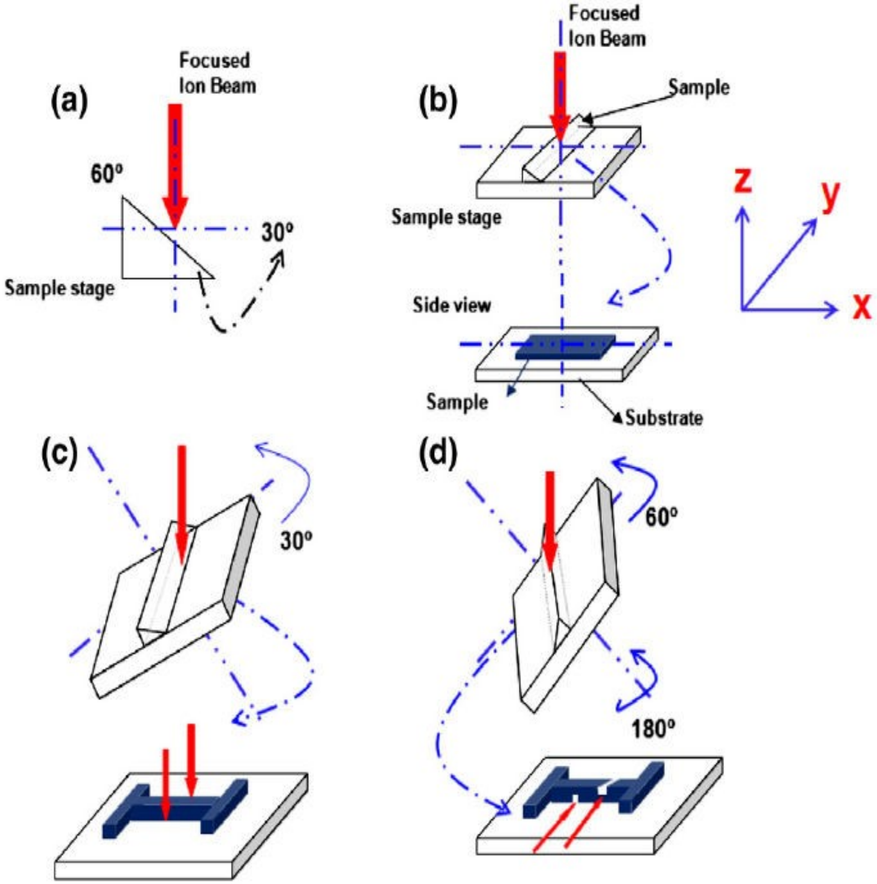
*Focused ion beam 3-D fabrication technique*

•Miniaturization is the central theme in modern fabrication technology. Many of the components used in modern products are becoming smaller and smaller. Here, the focused ion beam (FIB) direct milling technique will be discussed with the focus on fabricating devices at the micrometer to nano-scale level. Because of the very short wavelength and very large energy density, the FIB has the ability for direct fabrication of structures that have feature sizes at or below 1 $\mu$m. As a result, the FIB has recently become a popular candidate in making high- quality microdevices or high-precision microstructures

• The FIB has been a powerful tool in the semiconductor industry mainly for mask repairing, device modification, failure analysis and integrated circuit debugging. Two basic working modes, ion beam direct write and ion beam projection, have been developed for these applications. The ion beam direct write process, also known as FIB milling (FIBM), is the process of transferring patterns by direct impingement of the ion beam on the substrate. It is a large collection of microfabrication techniques that removes materials from a substrate and has been successfully used for fabricating various three-dimensional (3D) micro structures and devices from a wide range of materials. For the ion beam projection process, a collimated beam of ions passes through a stencil mask and the reduced image of the mask is projected onto the substrate underneath. The ion beam projection process is also known as focused ion beam lithography (FIBL) and can serve as an alternative to conventional optical lithography.



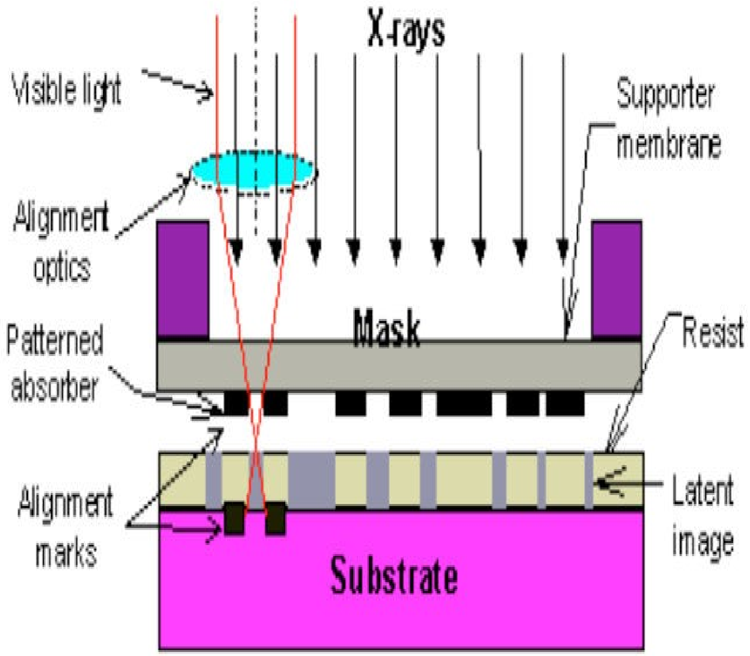
Source (LMIS)
Upper Lens
Mass Separator
Drift Tube
Lower Lens
Beam Deflector & MCP
Substrate
Nozzle

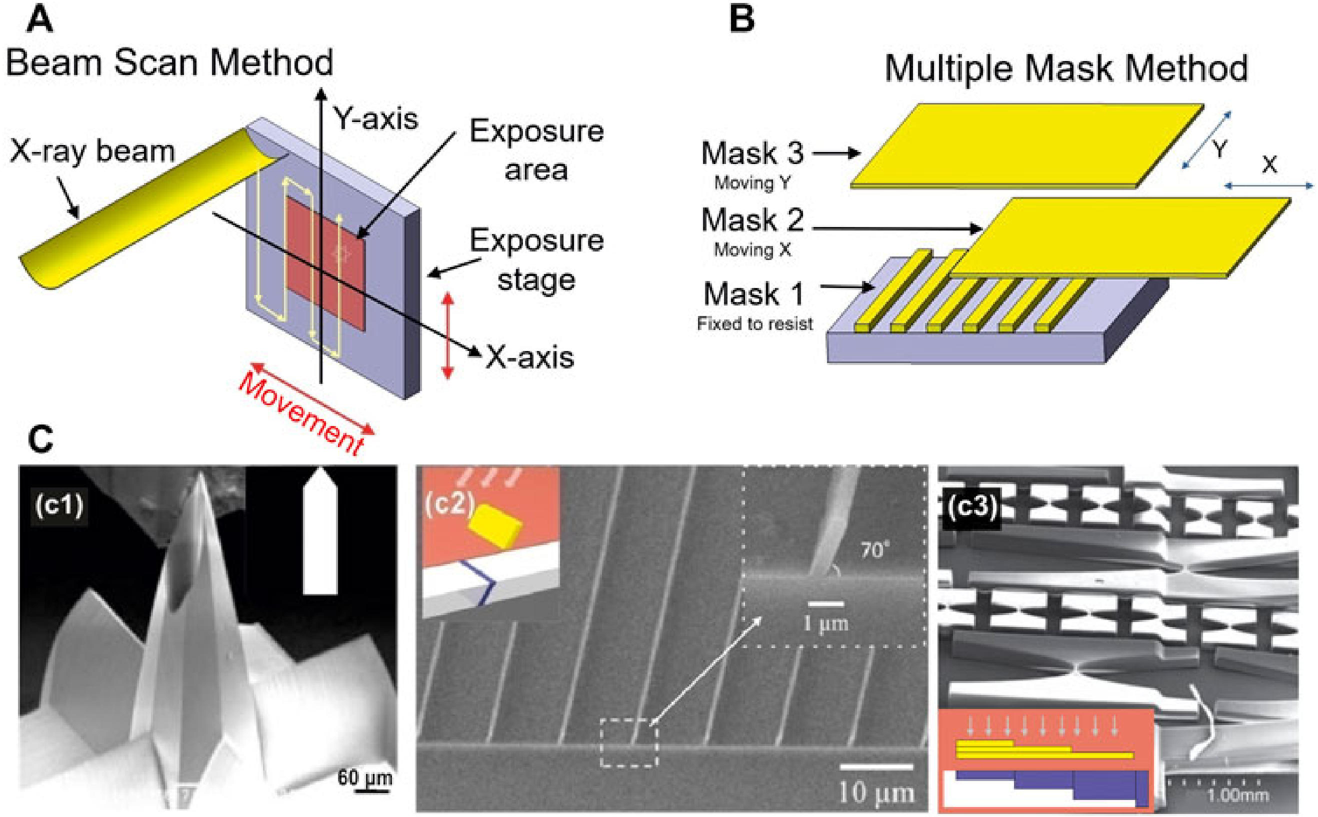



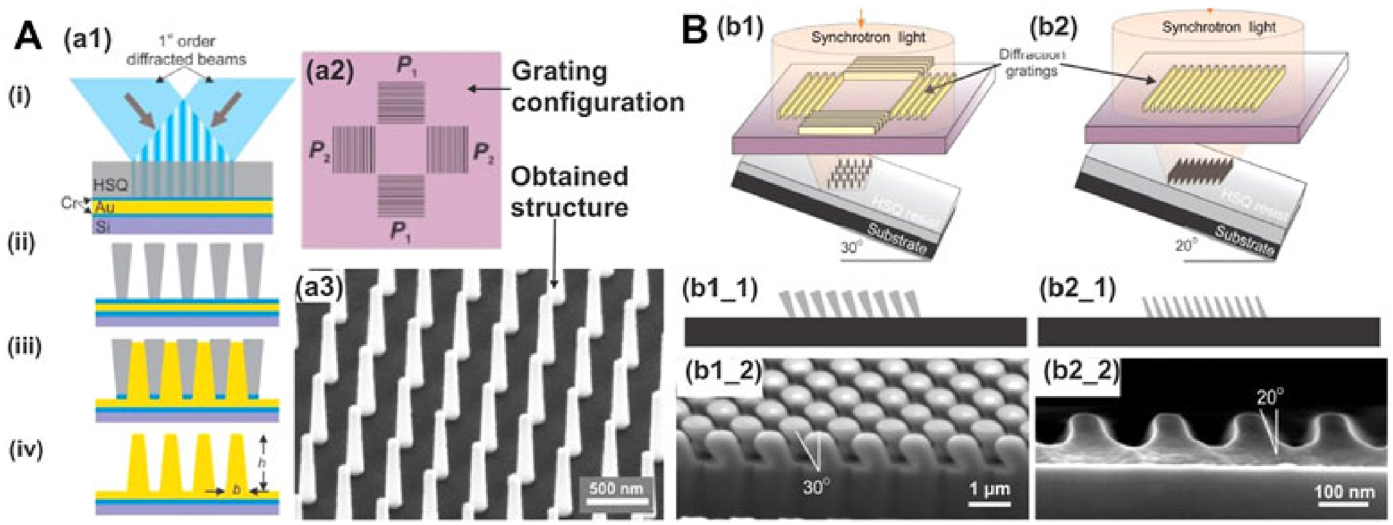
(a)
Focused Ion Beam
60°
30°
Sample stage
(b)
Focused Ion Beam
Sample
Sample stage
Side view
Sample
Substrate
z
y
x
(c)
30°
(d)
60°
180°

# X- ray lithography

- This lithography processes involve the category of nanolithographic techniques, through which transistors with smaller features can be patterned. It uses X-rays to transfer a geometric pattern from a mask to a light-sensitive chemical photoresist, or simply "resist," on the substrate. A series of chemical treatments then engraves the produced pattern into the material underneath the photoresist.
- **X-ray lithography** can be extended to an optical resolution of 15 nm by using the short wavelengths of 1 nm for the illumination. This is implemented by the proximity printing approach. The technique is developed to the extent of batch processing. The extension of the method relies on Near Field X-rays in Fresnel diffraction: a clear mask feature is "demagnified" by proximity to a wafer that is set near to a "Critical Condition". This Condition determines the mask-to-wafer Gap and depends on both the size of the clear mask feature and on the wavelength. The method is simple because it requires no lenses. This technique originated as a candidate for next-generation lithography for the semiconductor industry, with batches of microprocessors successfully produced. Having short wavelengths (below 1 nm), X-rays overcome the diffraction limits of optical lithography, allowing smaller feature sizes. If the X- ray source isn't collimated, as with a synchrotron radiation, elementary collimating mirrors or diffractive lenses are used in the place of the refractive lenses used in optics.

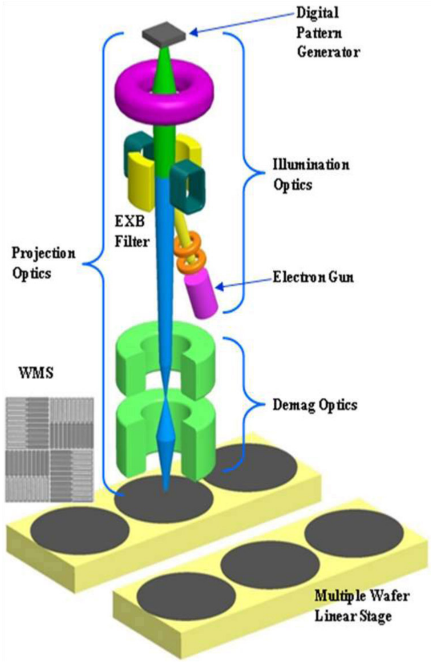

X-rays
Visible light
Supporter membrane
Alignment optics
Mask
Patterned absorber
Resist
Latent image
Alignment marks
Substrate

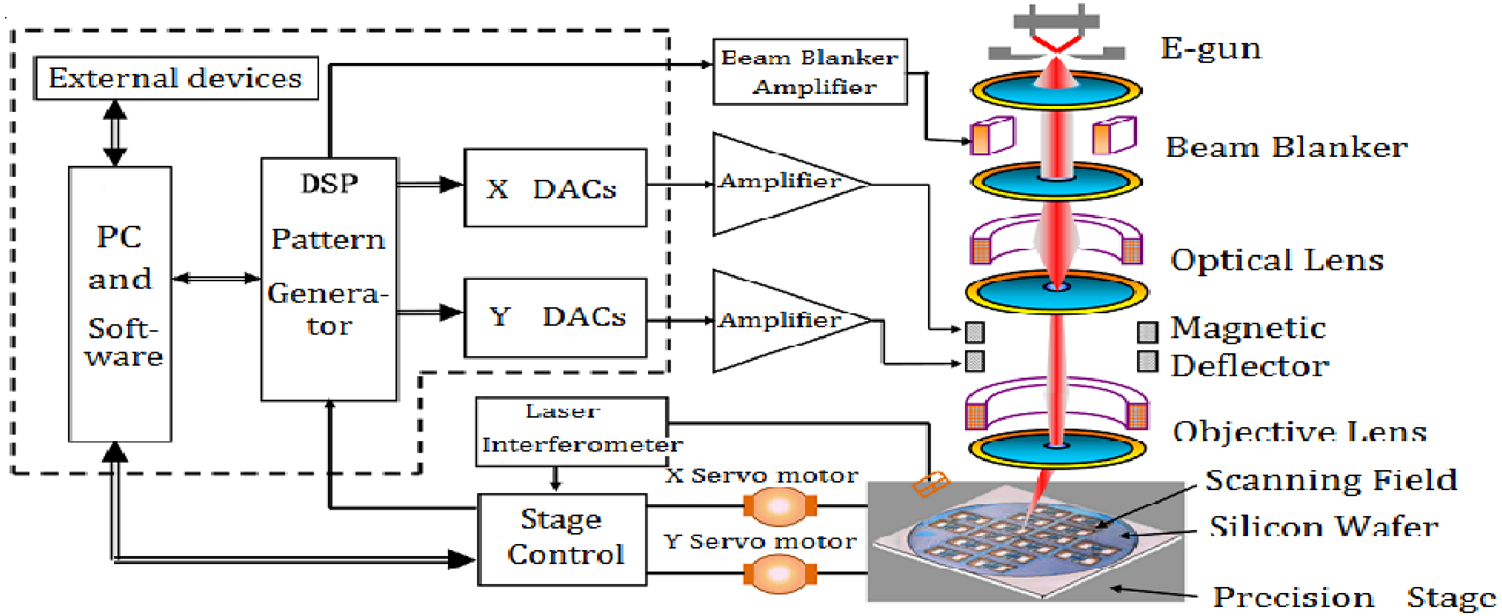

A
Beam Scan Method
X-ray beam
Y-axis
Exposure area
Exposure stage
X-axis
Movement
B
Multiple Mask Method
Mask 3
Moving Y
Mask 2
Moving X
Mask 1
Fixed to resist
Y
X
C
(c1)
60 µm
(c2)
70°
1 µm
10 µm
(c3)
1.00mm

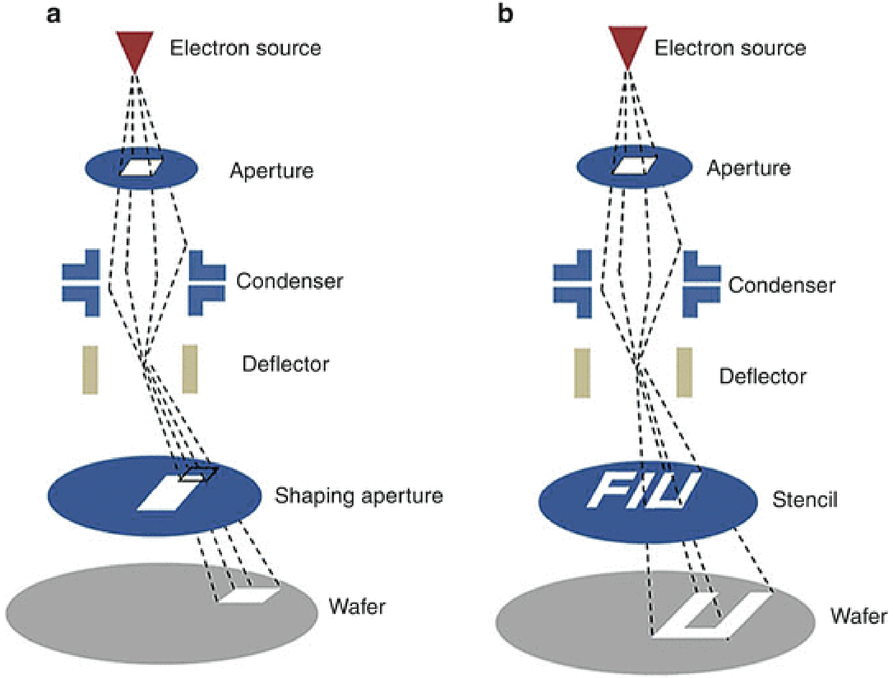

A
(a1)
1st order diffracted beams
(i)
HSQ
Cr
Au
Si
(ii)
(iii)
(iv)
h
b
(a2)
P1
P2
P2
P1
Grating configuration
Obtained structure
(a3)
500 nm
B
(b1)
Synchrotron light
Diffraction gratings
HSQ resist
Substrate
30°
(b2)
Synchrotron light
HSQ resist
Substrate
20°
(b1_1)
(b2_1)
(b1_2)
30°
1 µm
(b2_2)
20°
100 nm

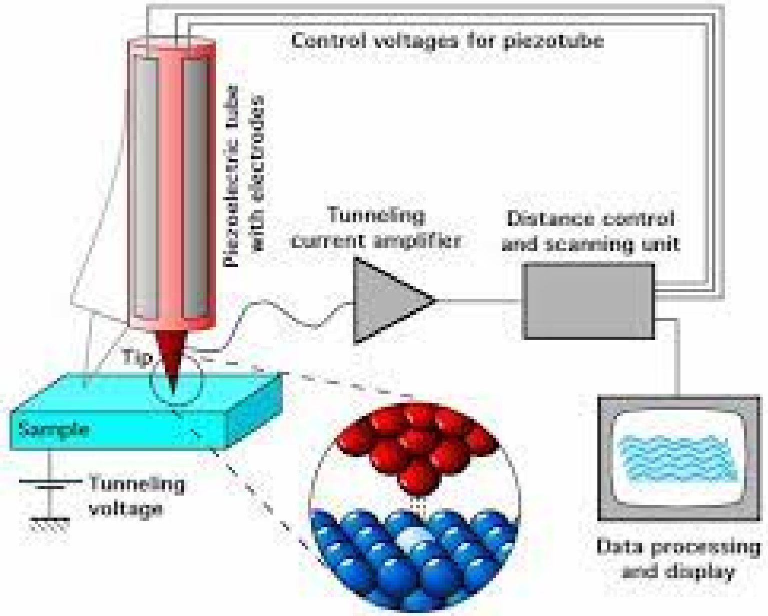
# E-beam lithography

- Electron Beam Lithography uses a tightly focussed beam of electrons scanned over the surface of a substrate. Typically, electron beam lithography with ultra high resolution (UHR) is used at the very beginning of a multiple technique and a multiple step process in a top down approach in order to transfer the nanostructure into the substrate or subsequently build up a device in a layer by layer fashion. For nanolithography with ultra high resolution down to sub10nm feature sizes, complete dedicated e-beam writer systems or converted scanning electron microscopes (SEM) can be used. With the help of a design editor and a pattern generator, the electron beam is guided over the substrate surface, which is covered with electron beam sensitive resist such as PMMA, in order to generate a resist mask which then can be further used for nanopattern transfer.


Digital
Pattern
Generator
Illumination
Optics
EXB
Filter
Projection
Optics
Electron Gun
WMS
Demag Optics
Multiple Wafer
Linear Stage


External devices
PC
and
Soft-
ware
DSP
Pattern
Genera-
tor
X DACs
Y DACs
Beam Blanker
Amplifier
Amplifier
Amplifier
Laser
Interferometer
X Servo motor
Y Servo motor
Stage
Control
E-gun
Beam Blanker
Optical Lens
Magnetic
Deflector
Objective Lens
Scanning Field
Silicon Wafer
Precision Stage

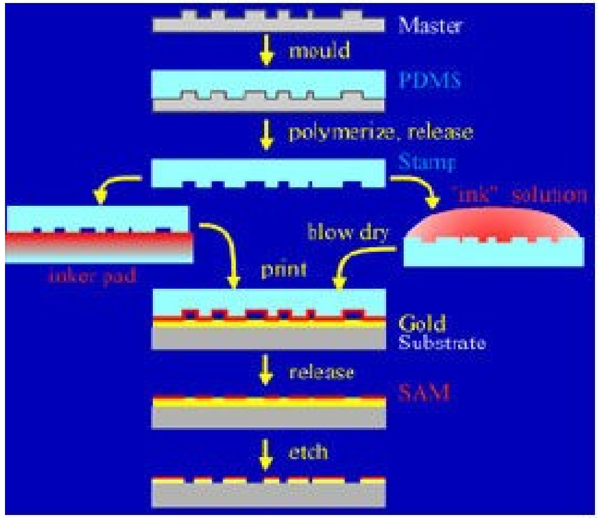

a
Electron source
Aperture
Condenser
Deflector
Shaping aperture
Wafer
b
Electron source
Aperture
Condenser
Deflector
Stencil
Wafer

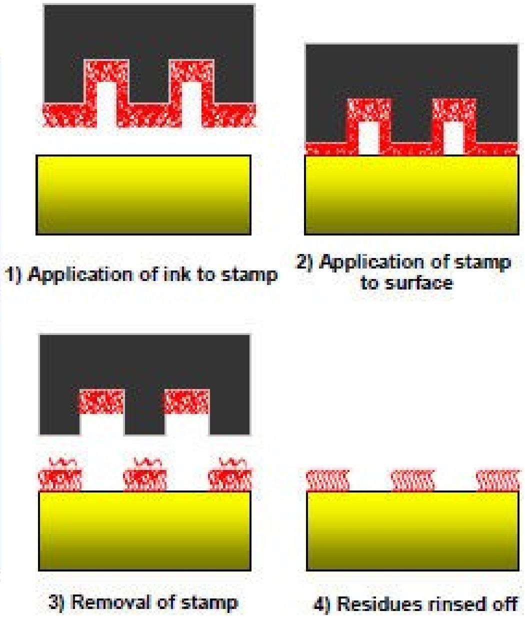

Control voltages for piezotube
Piezoelectric tube
with electrodes
Tunneling
current amplifier
Distance control
and scanning unit
Tip
Sample
Tunneling
voltage
Data processing
and display

# Alternate nanolithographic techniques

- *Micro-contact printing (soft lithography)*

- This is known as soft lithography that usually uses the relief patterns on a PDMS (poly-dimethylsiloxane) stamp in order to form patterns of self-assembled monolayers (SAMs) of ink on the surface of a substrate through conformal contact. This technique has wide range of application in cell biology, microelectronics, surface chemistry, micromachining, Patterning cells, patterning DNA and Patterning protein.

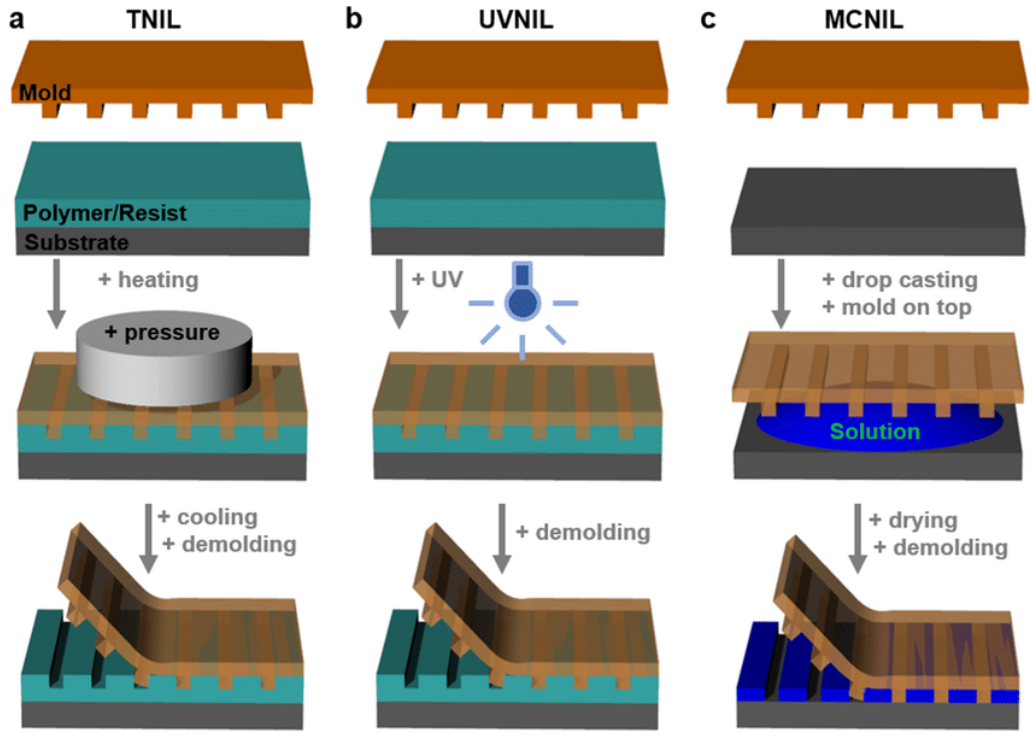


# Alternate nanolithographic techniques

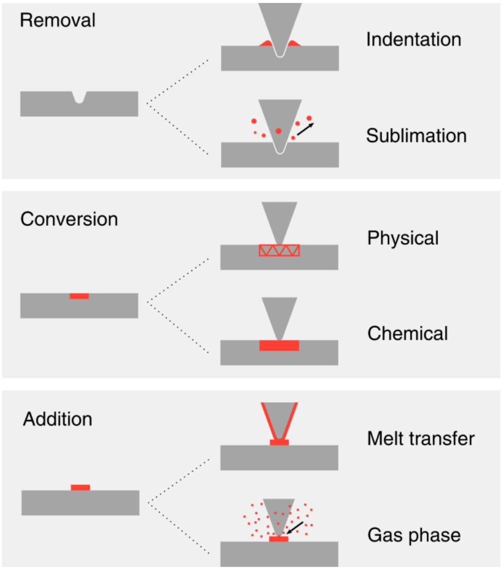
- *Nano-imprint lithography*

- Is an emerging process that can produce sub-10nm features. It is a simple process that uses a mould to emboss the resist with the required pattern. After embossing the resist, compressed resist material is removed using anisotropic etching and the substrate exposed. It can produce features at extremely small resolutions that cover a large area with a high throughput and relatively low cost, which is main advantage of this technique. It can be adapted to transfer all components needed to create a thin film transistor on a plastic substrate. It involves pressing and heating a thin film between a patterned template and a substrate. Upon heating, the patterned film adheres only to the substrate. This has high throughput and is relatively inexpensive compared to developing extreme deep UV lithography for commercial viability. It is also flexible enough to be used at chip level with several layers or at the wafer level when single layer is required. It can give resolutions lower than 10nm with high throughput at low cost. One of the current barriers to production at these resolutions is the development of mould. It can be used for fabricating nanoscale photo- detectors, silicon quantum-dot, quantum wire and ring transistors

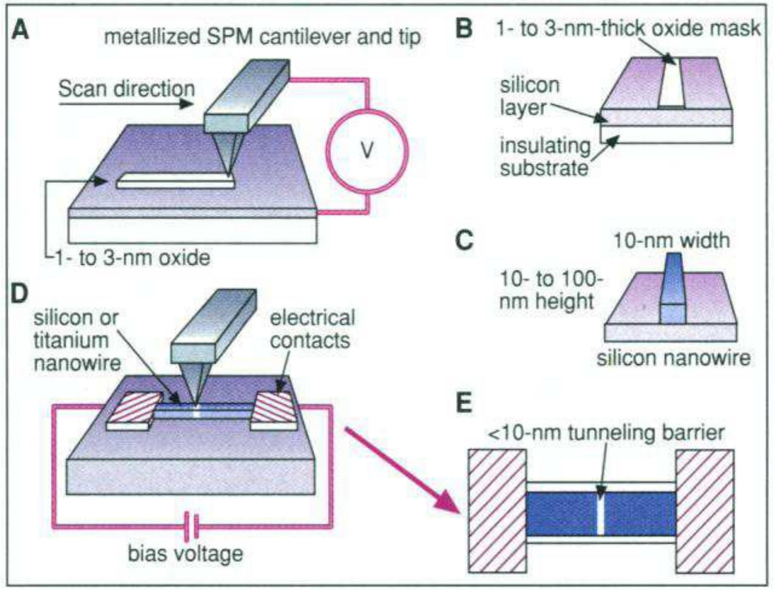


# Alternate nanolithographic techniques

- *Scanning Probe Lithography (SPL)*



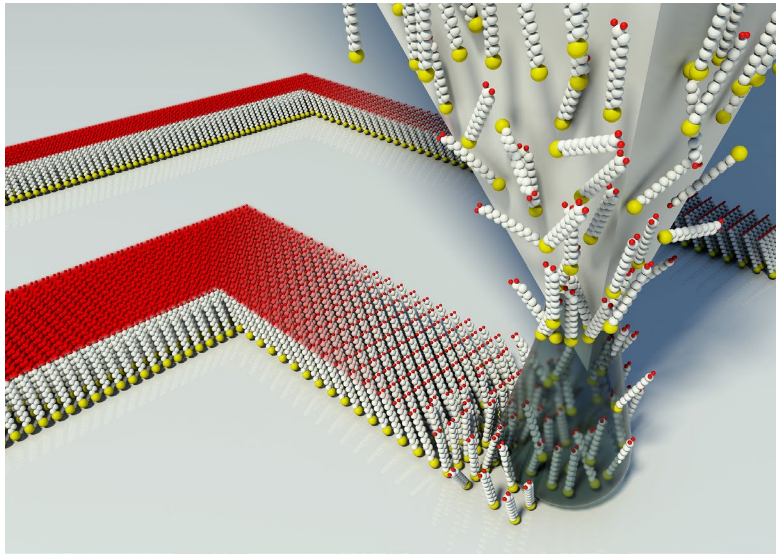

- SPL is an emerging area of research in which the scanning tunneling microscope (STM) or the atomic force microscope (AFM) is used to pattern nanometer-scale features. The patterning methods include mechanical pattering such as scratching or nano-indentation, or local heating with sharp tip (Dagata, 1995). When a voltage bias is applied between a sharp probe tip and a sample, an intense electric field is generated in the vicinity of the tip

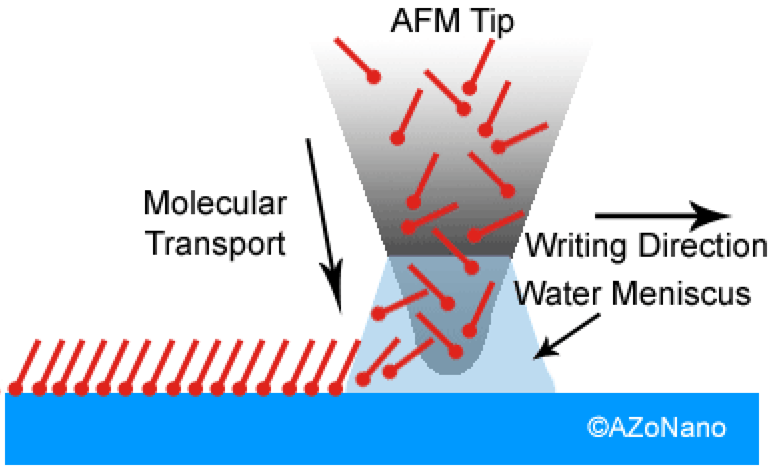


# Alternate nanolithographic techniques

- *Dip Pen Nanolithography (DPN)*

- Dip Pen Nanolithography (DPN) is known as a soft-lithography technique that uses an AFM scanning probe tip to draw nanostructures. In this process, a probe tip is coated with liquid ink, which then flows onto the surface to make patterns wherever the tip makes contact. This kind of direct write technique provides high-resolution patterning capabilities for a number of molecular and biomolecular "inks" on a variety of substrates. Substrates are the base material that the images are printed on. Some of the applications of the DPN technique include sol gel templates that are used to prepare nanotubes and nanowires, and protein nanoarrays to detect the amount of proteins in biological samples such as blood.

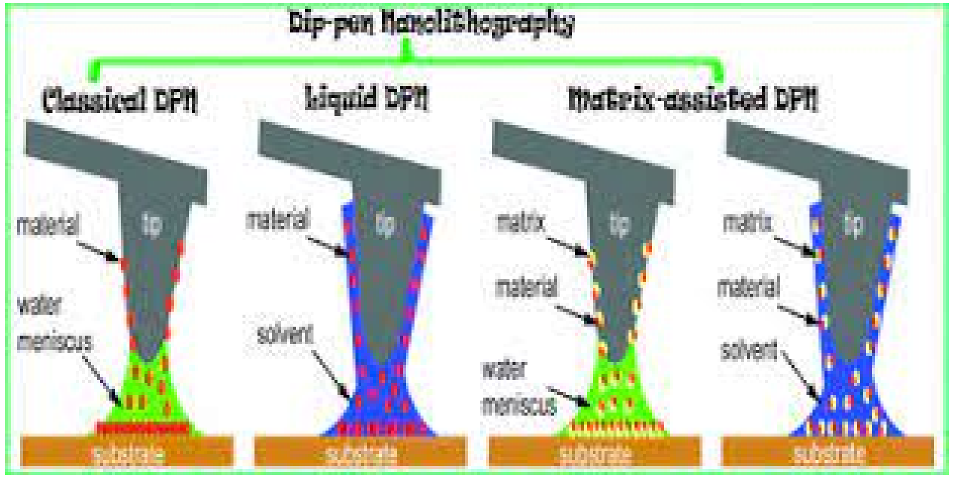




# Alternate nanolithographic techniques

- *Dip Pen Nanolithography (DPN)*

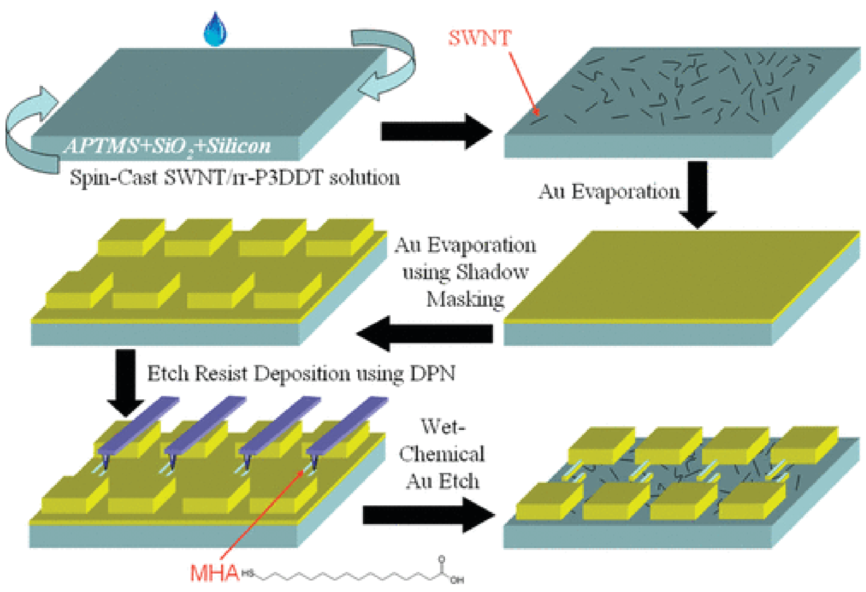
This process was first developed by Professor Chad Mirkin at Northwestern University Nanotechnology Institute for depositing thin organic films in patterns with feature sizes of around 10 nm ( about 20 times better than the best optical lithography). In DPN technology, the ink on a sharp object is transported to a paper substrate via capillary forces. The capillary transport of molecules from the AFM tip to the solid substrate is used in DPN to directly "write" pattern consisting of a relatively small collection of molecules in nanometer dimensions. An AFM tip is used to write alkanethiols with 30-nm line width resolution on a gold thin film in a manner analogous to that of a dip pen. Molecules are delivered from the AFM tip to a solid substrate of interest via capillary transport, making DPN a potentially useful tool for creating and functionalizing nanoscale devices

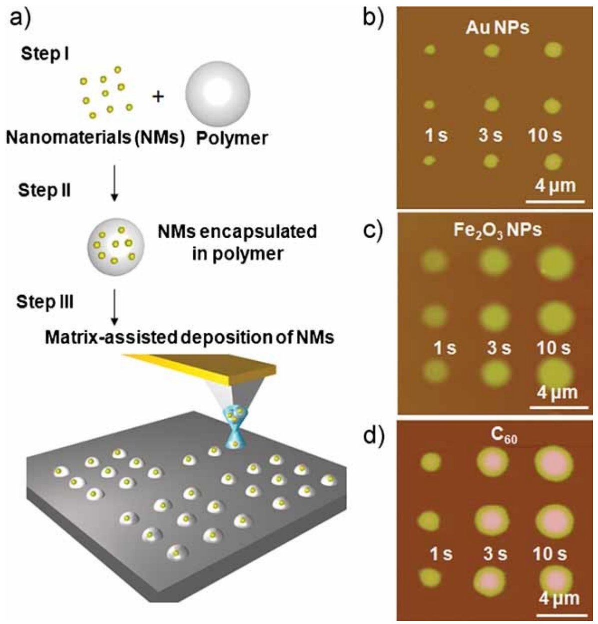


# Alternate nanolithographic techniques

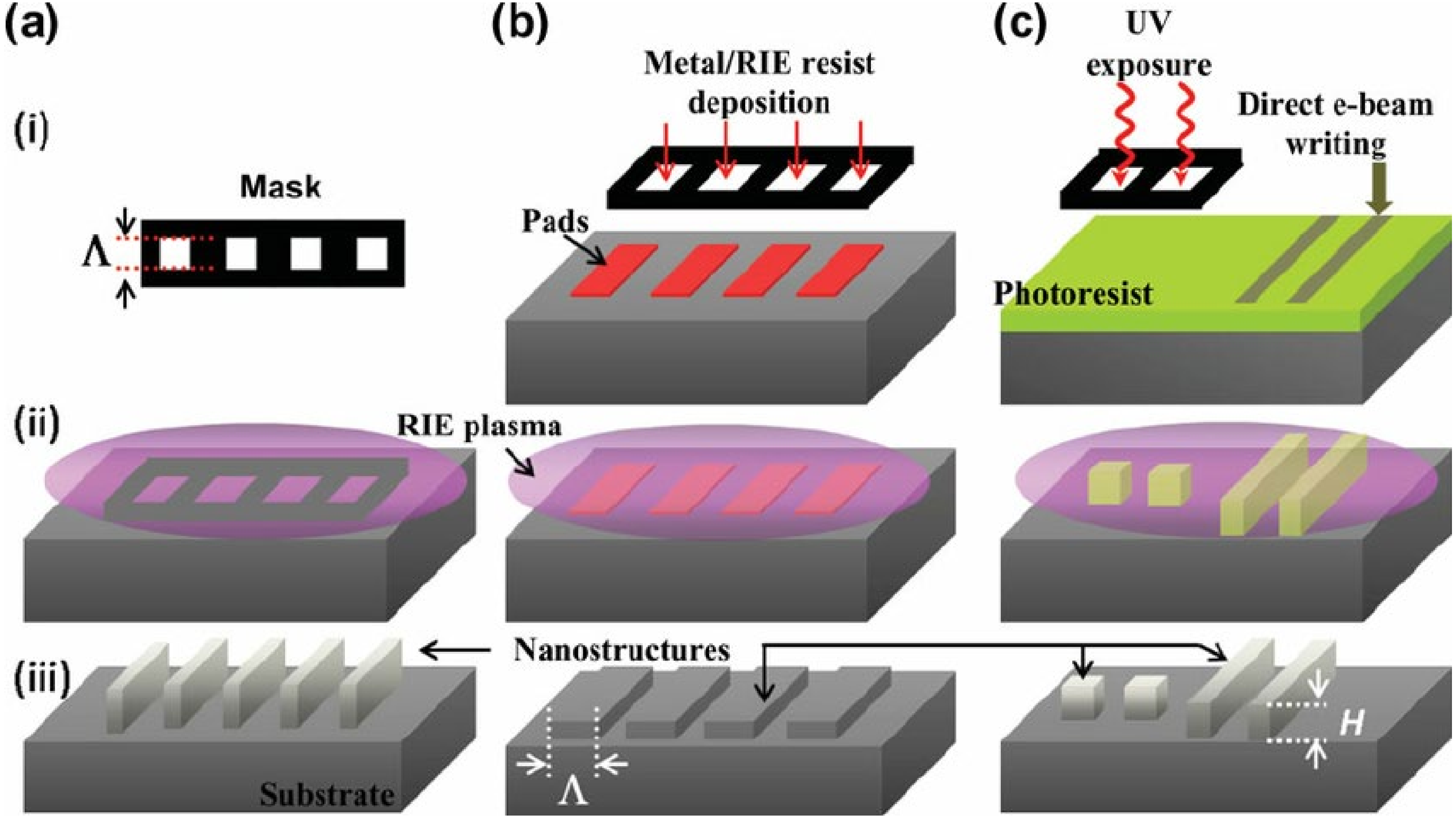
*DPN application on semiconductor surfaces*

Dip-Pen Nanolithography can not only apply to gold surface using alkyl or aryl thiols as inks, but also to semiconductor surfaces, such as silicon and gallium arsenide. Hexamethyldisilazane (HMDS) is used as the ink to pattern and modify (polarity) the surface of semiconductors. Lateral force microscopy (LFM) can be used to differentiate between oxidized semiconductor surfaces and patterned areas with the deposited monolayers of HMDS. The choice of the silazane ink is a critical component of the process since the traditional adsorbates such as trichlorosilanes are incompatible with the water meniscus and polymerize during ink deposition.

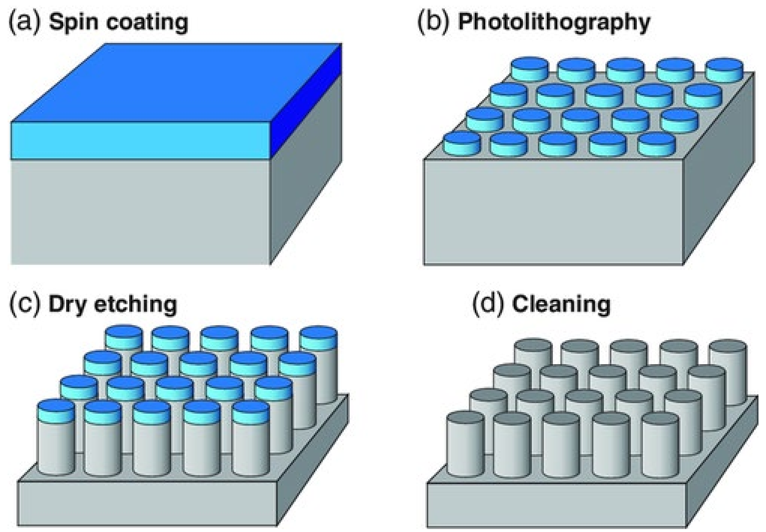


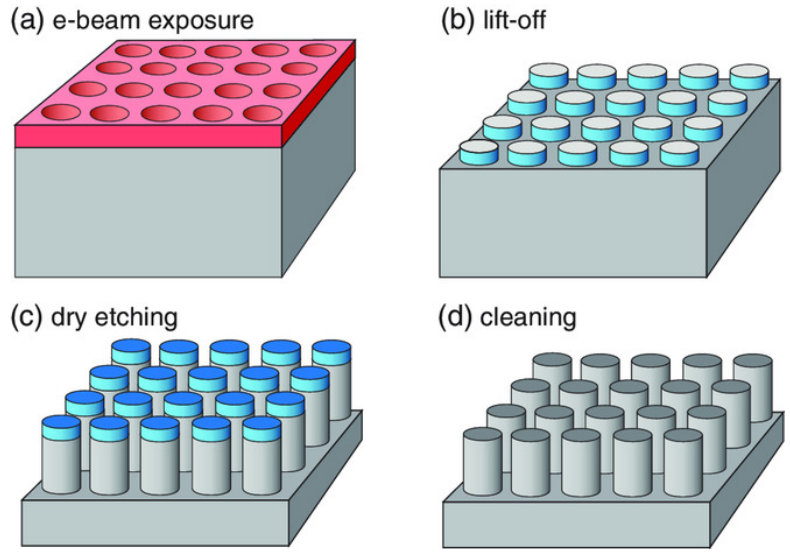



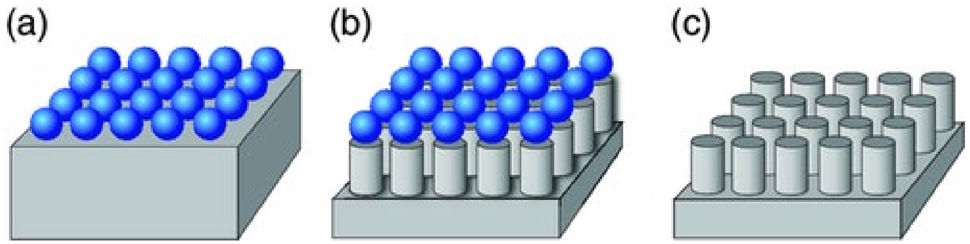
# Plasma Etching



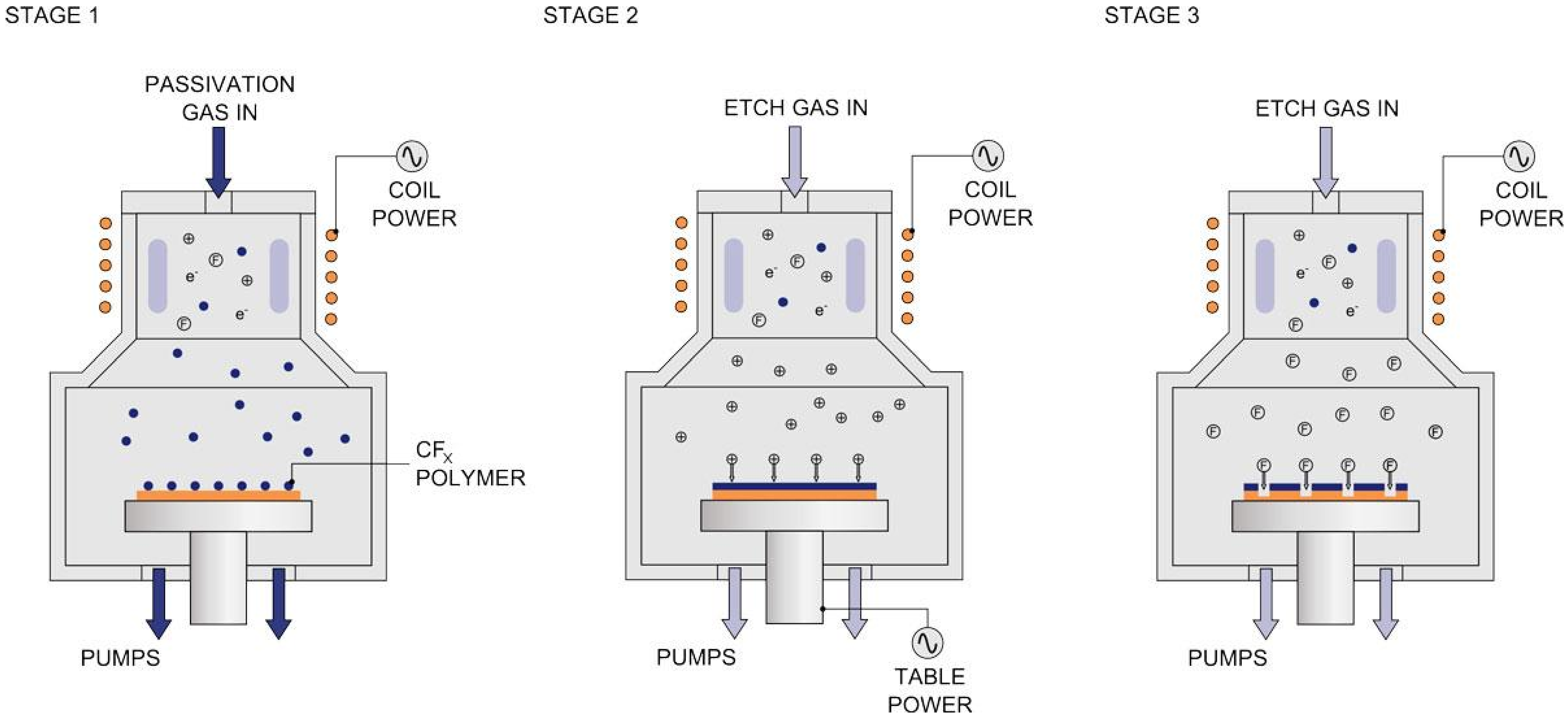
# Plasma Etching



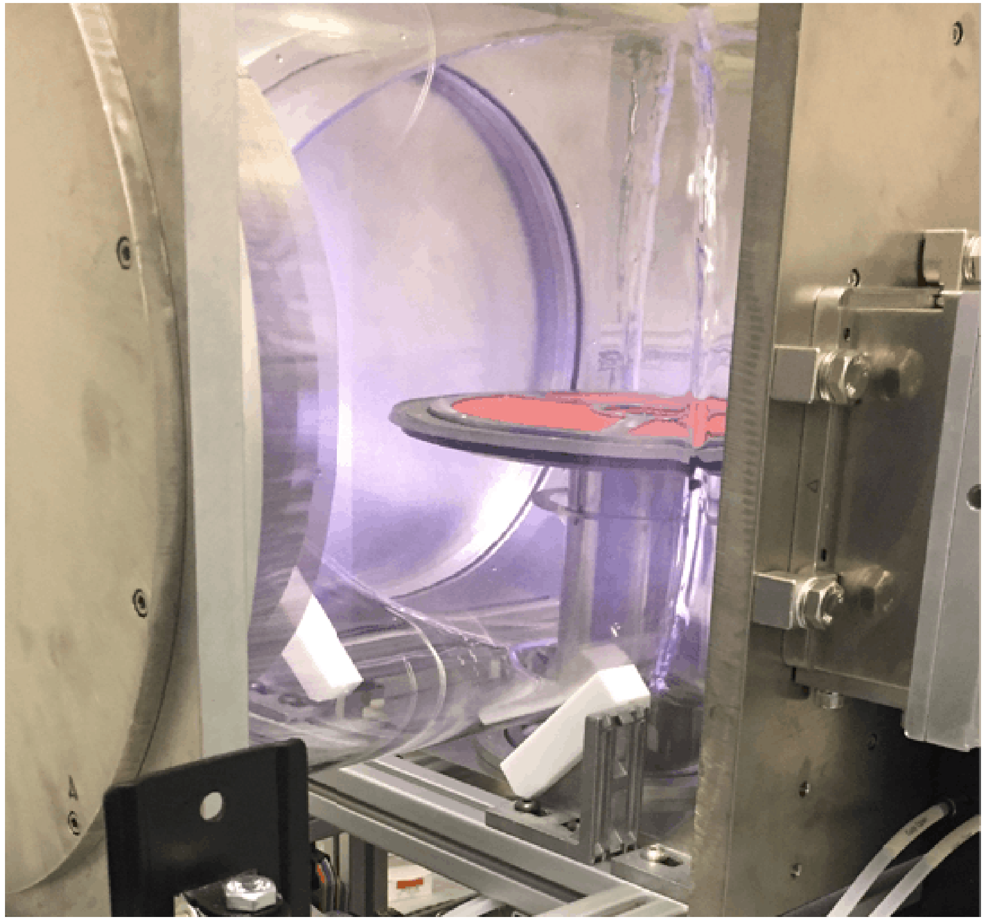



# Bosh Process



# Electron Enhanced Materials processing



- In this approach, each excited state reaction involves a material-specific energy threshold. Each wave of electrons interacts with the surface, providing exactly the right amount of energy necessary to drive the desired reaction. Due to a direct quantum excitation of bonds on the wafer surface, etching takes place one atomic layer at a time. The anisotropic etch that results is accomplished with a high etch rate, absence of any ion bombardment damage, and the elimination of any exposure of the wafer to elevated temperatures. Additional merits of our etching technology are that it yields atomically smooth surfaces, and it preserves the stoichiometry of the material.

# Electron Enhanced Materials processing