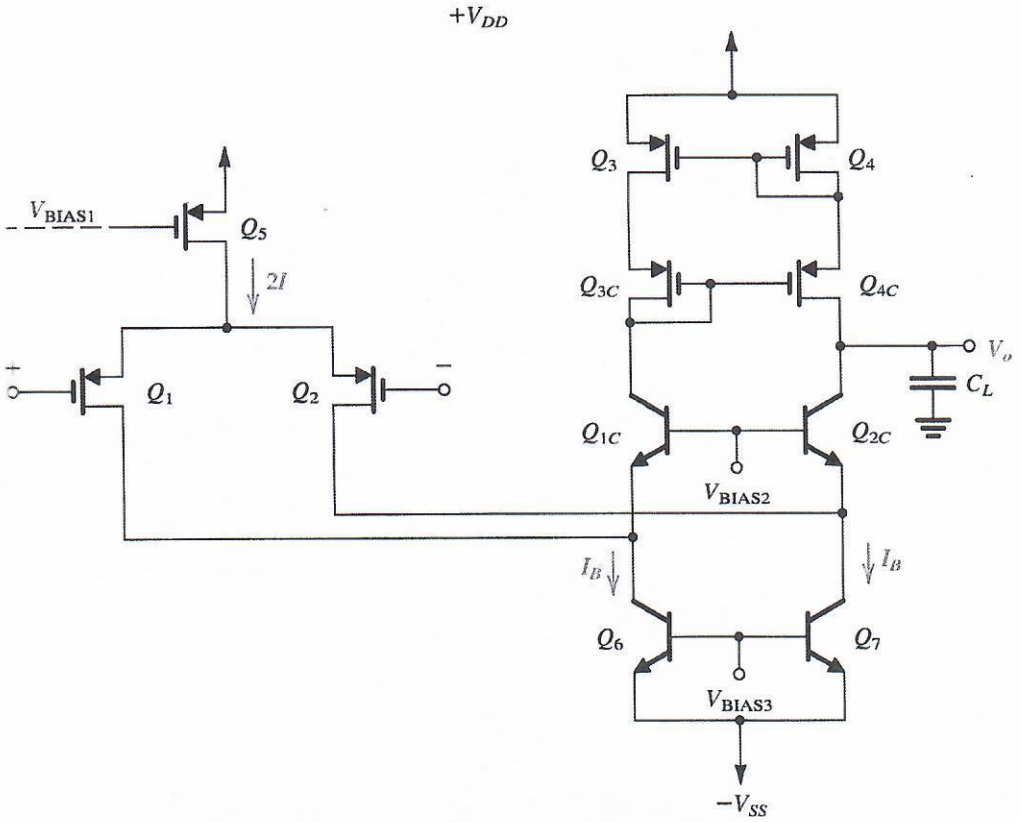

Fig. 10.27 A BiCMOS folded-cascode op amp. BJTs are employed to implement the common-base stage Q_{1C}, Q_{2C}. The high value of $g_{m1C} = g_{m2C}$ raises the frequency of the nondominant pole that results at the input of the common-base stage. Thus for a given value of C_L, $\omega_t = g_{m1}/C_L$ can be increased by operating the first stage at a higher g_m.

Digital Processing of Signals

Most physical signals, such as those obtained at transducer outputs, exist in analog form. Some of the processing required on these signals is most conveniently performed in an analog fashion. For instance, in instrumentation systems it is quite common to use a high-input-impedance, high-gain, high-CMRR differential amplifier right at the output of the transducer. This is usually followed by a filter whose object is to eliminate interference. However, further signal processing is usually required, which can range from simply obtaining a measurement of signal strength to performing some algebraic manipulations on this and related signals to obtain the value of a particular system parameter of interest, as is usually the case in systems intended to provide a complex control function. Another example of signal processing can be found in the common need for transmission of signals to a remote receiver.

All such forms of signal processing can be performed by analog means. In previous chapters we encountered circuits for implementing a number of such tasks. However, an attractive alternative exists: It is to convert, following some initial analog processing, the

signal from analog to digital form and then use economical, accurate, and convenient digital ICs to perform **digital signal processing.** Such processing can in its simplest form provide us with a measure of the signal strength as an easy-to-read number (consider, for example, the digital voltmeter). In more involved cases the digital signal processor can perform a variety of arithmetic and logic operations that implement a **filtering algorithm.** The resulting **digital filter** does many of the same tasks that an analog filter performs—namely, eliminate interference and noise. Yet another example of digital signal processing is found in digital communications systems, where signals are transmitted as a sequence of binary pulses, with the obvious advantage that corruption of the amplitudes of these pulses by noise is, to a large extent, of no consequence.

Once digital signal processing has been performed, we might be content to display the result in digital form, such as a printed list of numbers. Alternatively, we might require an analog output. Such is the case in a telecommunications system, where the usual output may be speech. If an analog output is desired, then obviously we need to convert the digital signal back to an analog form.

It is not our purpose here to study the techniques of digital signal processing. Rather, we shall examine the interface circuits between the analog and digital domains. Specifically, we shall study the basic techniques and circuits employed to convert an analog signal to digital form **(analog-to-digital or simply A/D conversion)** and those used to convert a digital signal to analog form **(digital-to-analog or simply D/A conversion).** Digital circuits are studied in Chapters 13 and 14.

Sampling of Analog Signals

The principle underlying digital signal processing is that of **sampling** the analog signal. Figure 10.28 illustrates in a conceptual form the process of obtaining samples of an analog signal. The switch shown closes periodically under the control of a periodic pulse signal (clock). The closure time of the switch, τ, is relatively short, and the samples obtained are stored (held) on the capacitor. The circuit of Fig. 10.28 is known as a **sample-and-hold (S/H) circuit.** As indicated, the S/H circuit consists of an analog switch that can be implemented by a MOSFET transmission gate (Section 5.10), a storage capacitor, and (not shown) a buffer amplifier.

Between the sampling intervals—that is, during the *hold* intervals—the voltage level on the capacitor represents the signal samples we are after. Each of these voltage levels is then fed to the input of an A/D converter, which provides an N-bit binary number proportional to the value of signal sample.

The fact that we can do our processing on a limited number of samples of an analog signal while ignoring the analog-signal details between samples is based on the sampling theorem [see Lathi (1965)].

Signal Quantization

Consider an analog signal whose values range from 0 to +10 V. Let us assume that we wish to convert this signal to digital form and that the required output is a 4-bit[2] signal.

[2] *Bit* stands for *b*inary dig*it*.

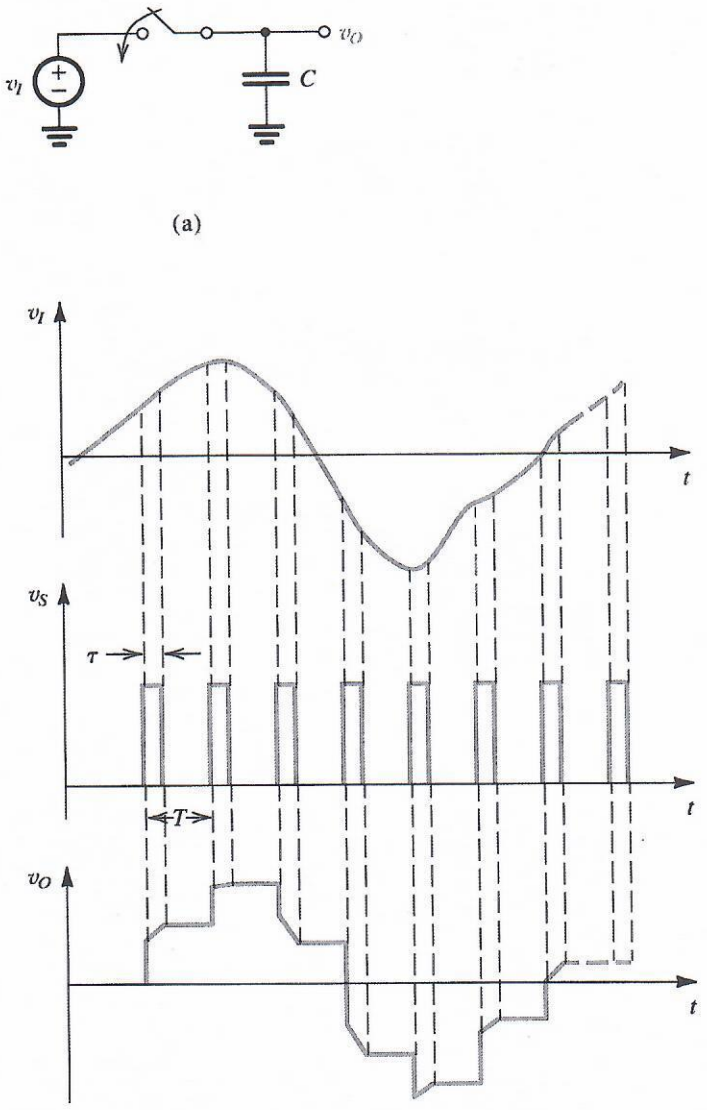

Fig. 10.28 Process of periodically sampling an analog signal. **(a)** Sample-and-hold (S/H) circuit. The switch closes τ seconds every period. **(b)** Input signal waveform. **(c)** Sampling signal (control signal for the switch). **(d)** Output signal (to be fed to A/D converter).

We know that a 4-bit binary number can represent 16 different values, 0 to 15; it follows that the *resolution* of our conversion will be 10 V/15 = $\frac{2}{3}$ V. Thus an analog signal of 0 V will be represented by 0000, $\frac{2}{3}$ V will be represented by 0001, 6 V will be represented by 1001, and 10 V will be represented by 1111.

All of the above sample numbers were multiples of the basic increment ($\frac{2}{3}$V). A question now arises regarding the conversion of numbers that fall between these succes-

sive incremental levels. For instance, consider the case of 6.2-V analog level. This falls between 18/3 and 20/3. However, since it is closer to 18/3 we treat it as if it were 6 V and *code* it as 1001. This process is called **quantization.** Obviously errors are inherent in this process; such errors are called quantization errors. Using more bits to represent (encode or code) an analog signal reduces quantization errors but requires more complex circuitry.

The A/D and D/A Converters as Functional Blocks

Figure 10.29 depicts the functional block representations of A/D and D/A converters. As indicated, the **A/D converter** (also called an ADC) accepts an analog sample v_A and produces an N-bit **digital word.** Conversely, the **D/A converter** (also called a DAC

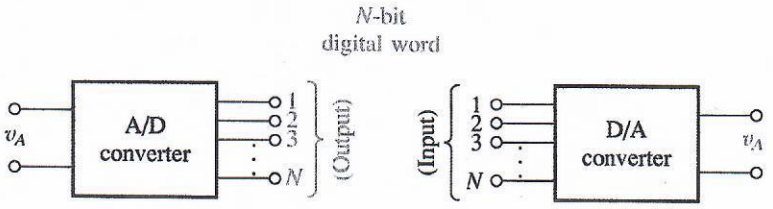

Fig. 10.29 The A/D and D/A converters as circuit blocks.

accepts an n-bit digital word and produces an analog sample. The output samples of the D/A converter are often fed to a sample-and-hold circuit. At the output of the S/H circuit a staircase waveform, such as that in Fig. 10.30, is obtained. The staircase waveform can then be smoothed by a low-pass filter, giving rise to the smooth curve shown in color in Fig. 10.30. In this way an analog output signal is reconstructed. Finally, note that the quantization error of an A/D converter is equivalent to $\pm\frac{1}{2}$ least significant bit (LSB).

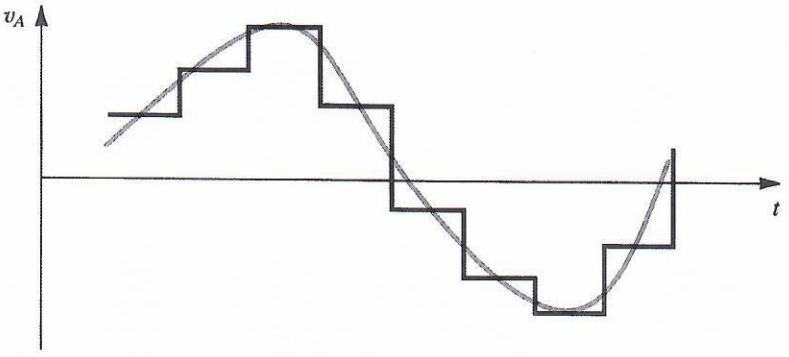

Fig. 10.30 The analog samples at the output of a D/A converter are usually fed to a sample-and-hold circuit to obtain the staircase waveform shown. This waveform can then be filtered to obtain the smooth waveform, shown in color. The time delay usually introduced by the filter is not shown.

50 μA, what value of C_C must be used? If devices with 1-V threshold are used, what gate-to-source bias voltage is used in the input stage? For a process for which $\mu_n C_{OX} = 20\ \mu A/V^2$, what W/L ratio applies for the input-stage devices?

**10.53 Consider a CMOS amplifier that is complementary to that in Fig. 10.23 in which each device is replaced by its complement of the same physical size with the supplies reversed. Use the overall conditions as specified in Example 10.2. For all devices evaluate I_D, g_m, and r_o. Find A_1, A_2, the dc open-loop gain, the input common-mode range, and the output voltage range. Neglect the effect of V_A on bias currents.

Section 10.8: Alternative Configurations for CMOS and BiCMOS Op Amps

D**10.54 Consider the cascoded input stage of Fig. 10.25. Let $2I = 25\ \mu A$, $\mu_p C_{OX} = 10\ \mu A/V^2$, $|V_t| = 1$ V, and W/L for Q_1, Q_2, Q_{1C}, and $Q_{2C} = 120/8$. By how much should V_{BIAS2} be set below the voltage at the common source connection of Q_1 and Q_2, so that Q_1, Q_2, Q_{1C}, and Q_{2C} are operating at the boundary of the saturation region? An arrangement that is usually used to generate V_{BIAS2} via creating a constant voltage difference between the sources of Q_1 and Q_2 and the gates of Q_{1C} and Q_{2C} is shown in Fig. P10.54. If I_{BIAS} is selected to be 5 μA, find the required W/L ratio for Q_B. Also, if W/L for Q_5 is 150/10 what must V_{BIAS1} be? Now draw the complete circuit and calculate V_{GS} for each of Q_3, Q_{3C}, Q_4, and Q_{4C} assuming that $\mu_n C_{OX} = 20\ \mu A/V^2$, W/L for each of Q_{3C} and $Q_4 = 60/8$. Find the input common-mode range.

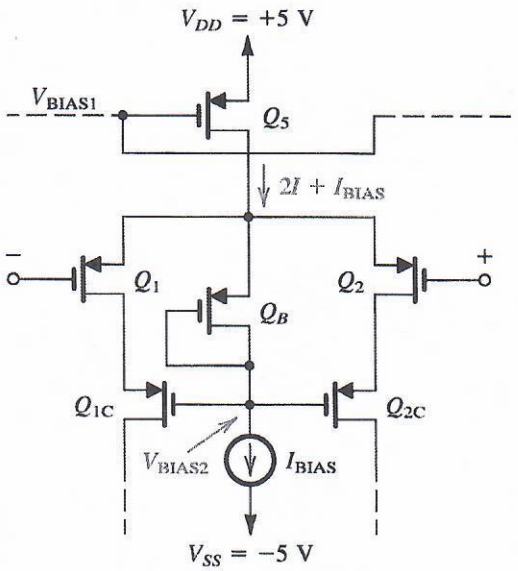

Fig. P10.54

10.55 Sketch the circuit that is complementary to that in Fig. 10.25, that is, one that uses an input n-channe differential pair.

10.56 Find the output resistance and the dc open-loop voltage gain of the folded cascode amplifier o Fig. 10.26 whose parameters are specified in Exercise 10.29. Assume $|V_A| = 25$ V for all devices.

D*10.57 Design the folded cascode circuit of Fig. 10.26 to obtain a dc open-loop voltage gain of 10,000 V/V and a unity-gain bandwidth of 1 MHz when the total capacitance at the output is 10 pF. Design for $I_B = 2I$, $(W/L)_1 = (W/L)_{4C} = 2(W/L)_{2C}$. Specify the required values of I and $(W/L)_1$. Let $\mu_n C_{OX} = 2\mu_p C_{OX} = 20\ \mu A/V^2$ and $|V_A| = 25$ V. (Hint: Use Eq. 10.62.)

D10.58 It is required to design the folded-cascode CMOS op-amp circuit of Fig. 10.26. The load capacitance C_L (including all parasitics) is 10 pF. The total capacitance at the input of each of the common-gate transistors Q_{1C} and Q_{2C} is $C_P = 1$ pF. Design for bias currents $2I = I_B = 100\ \mu A$ and $(W/L)_{1C} = (W/L)_{2C} = 10/10$. To obtain a sufficient phase margin the design should ensure that $f_t \le f_P/3$, where f_P is the frequency of the nondominant pole due to C_P. Specify the required W/L ratios for the input transistors to obtain the largest possible f_t. What is the value of f_t realized? Assume that $\mu_n C_{OX} = 2\ \mu_p C_{OX} = 20\ \mu A/V^2$.

D10.59 A folded-cascode BiCMOS amplifier having the topology of Fig. 10.27 is designed to operate at high frequencies. The bias currents are $2I = I_B = 400\ \mu A$, and the W/L ratio for the input stage transistors is 300/10. Find f_t for a load capacitance C_L (including all the output node parasitics) of 2 pF. To maintain an acceptable phase margin, the parasitic pole created at the input to the cascode transistors Q_{1C} and Q_{2C} must be at least three times higher in frequency than f_t. What is the largest parasitic capacitance C_P that can be tolerated? Assume $\mu_p C_{OX} = 10\ \mu A/V^2$.

Section 10.9: Data Converters—An Introduction

10.60 An analog signal in the range 0 to +10 V is to be digitized with a quantization error of less than 1%

full scale. What is the number of bits required? What is the resolution of the conversion? If the range is to be extended to ±10 V with the same requirement, what is the number of bits required? For an extension to a range of 0 to +15 V, how many bits are required to provide the same resolution? What is the corresponding resolution and quantization error?

*10.61 Consider Fig. 10.30. On the staircase output of the S/H circuit sketch the output of a simple low-pass RC circuit with a time constant that is (a) one-third of the sampling interval; (b) equal to the sampling interval.

Section 10.10: D/A Converter Circuits

*10.62 Consider the DAC circuit of Fig. 10.31 for the cases $N = 2$, 4, and 8. What is the tolerance, expressed as $\pm x\%$, to which the resistors should be selected so as to limit the resulting output error to the equivalent of $\pm\frac{1}{2}$ LSB?

10.63 The BJTs in the circuit of Fig. P10.63 have their base–emitter junction areas scaled in the ratios indicated. Find I_1 to I_4 in terms of I.

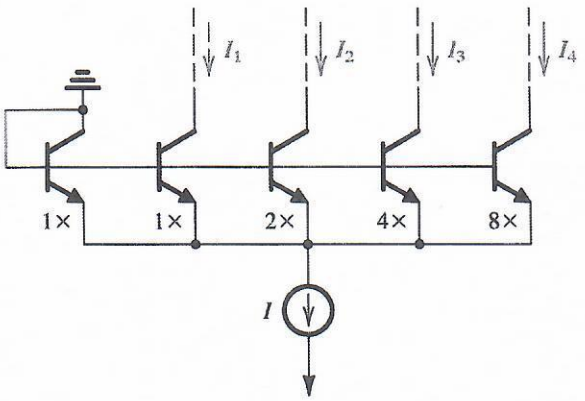

Fig. P10.63

10.64 A problem encountered in the DAC circuit of Fig. 10.33 is the large spread in transistor EBJ areas required when N is large. As an alternative arrangement consider using the circuit in Fig. 10.33 for 4 bits only. Then, feed the current in the collector of the terminating transistor Q_t to the circuit of Fig. P10.63 (in place of the current source I), thus producing currents for 4 more bits. In this way an 8-bit DAC can be implemented with a maximum spread in areas of 8. What is the total area of emitters needed in terms of the smallest device? Contrast this with the usual 8-bit circuit. Give the complete circuit of the converter thus realized.

D*10.65 The circuit in Fig. 10.31 can be used to multiply an analog signal by a digital one by feeding the analog signal to the V_{ref} terminal. In this case the D/A converter is called a **multiplying DAC** or MDAC. Given an input sine-wave signal of 0.1 sin ωt volts, use the circuit of Fig. 10.31 together with an additional op amp to obtain $v_O = 10D \sin \omega t$ where D is the digital word given by Eq. (10.67) and $N = 4$. How many discrete sine-wave amplitudes are available at the output? What is the smallest? What is the largest? To what digital input does a 10-V peak-to-peak output correspond?

10.66 What is the input resistance seen by V_{ref} in the circuit of Fig. 10.32?

Section 10.11: A/D Converter Circuits

10.67 A 12-bit dual-slope ADC of the type illustrated in 10.36 utilizes a 1-MHz clock and has $V_{ref} = 10$ V. Its analog input voltage is in the range 0 to −10 V. The fixed interval T_1 is the time taken for the counter to accumulate a count of 2^N. What is the time required to convert an input voltage equal to the full-scale value? If the peak voltage reached at the output of the integrator is 10 V, what is the integrator time constant? If through aging R increases by 2% and C decreases by 1%, what does V_{peak} become? Does the conversion accuracy change?

10.68 The design of a 4-bit flash ADC as shown in 10.37 is being considered. How many comparators are required? For an input signal in the range of 0 to +10 V, what are the reference voltages needed? Show how they can be generated using a 10-V reference and several 1-kΩ resistors (how many?). If a comparison is possible in 50 ns and the associated logic requires 35 ns, what is the maximum possible conversion rate? Indicate the digital code you expect at the output of the comparators and at the output of the logic for an input of (a) 0 V, (b) +5.1 V, and (c) +10 V.