Evolução de Microeletrônica, Regras de Escalamento e Limites

Evolução de Microeletrônica, Regras de Escalamento e Limites

1. Introdução
2. História e Evolução Microeletrônica
3. Materiais Usados em CI’s de Si.
4. ITRS e Tendências.
5. Regras de Escalamento.
6. Limites de Escalamento e Dispositivos pós CMOS
7. Conclusões

1. Introdução

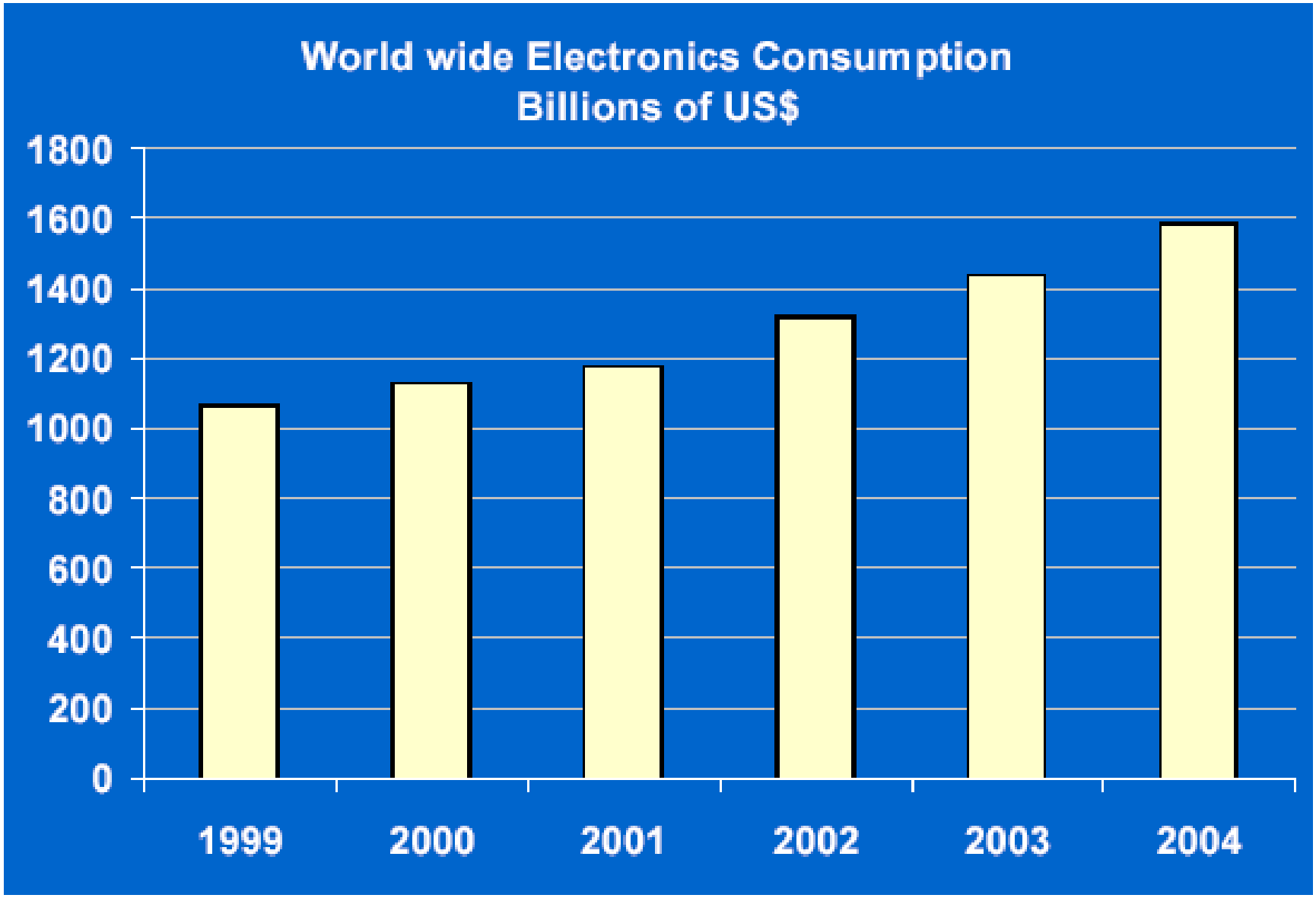
- História longa num período curto
- Alguns fatos marcantes:

  1947 - Descobrimento Transistor

  1959 - Processo Planar para CI´s

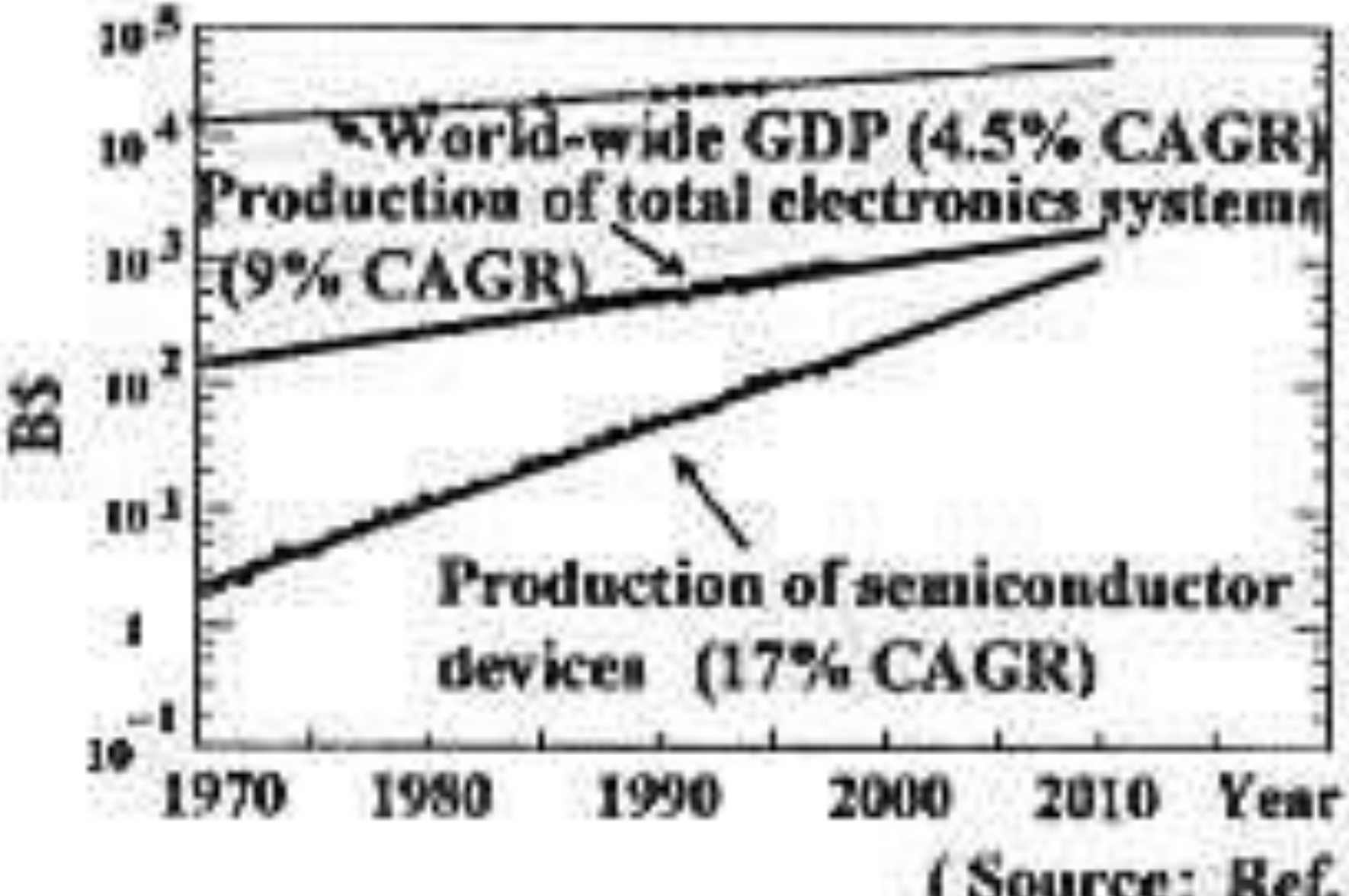
  1962 - Primeiros CI´s Comerciais
- Idade do transistor = 56 anos
- Idade de CI’s Comerciais = 42 anos.

- Crescimento incomparável na evolução tecnológica e no mercado: 16% anual
- Mercado global de eletrônica é > US$ 1 trilhão, maior do mundo !!!
- Revolução econômica e social – baseada na tecnologia da informação: Internet, i-mode, Bluetooth, telefone celular, navegação e carro inteligente, realidade virtual, jogos eletrônicos, etc
- Foi possível graças ao progresso em tecnologia de semicondutores e CI’s.
- Estamos na “Idade do Silício”.



Reed Electronics Group

In-Stat MDR



(Source: Ref. 1)

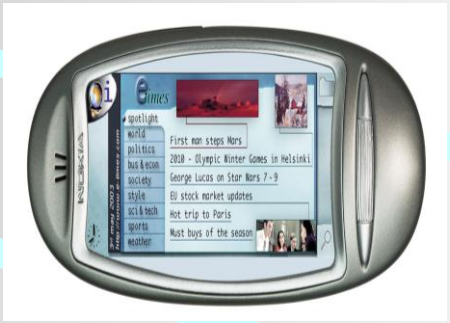
Fig.3 Trend of Semicoaductor Production

Towards ambient intelligence

10 1 chips/device

PC | Personal assistants | Ambient intelligence

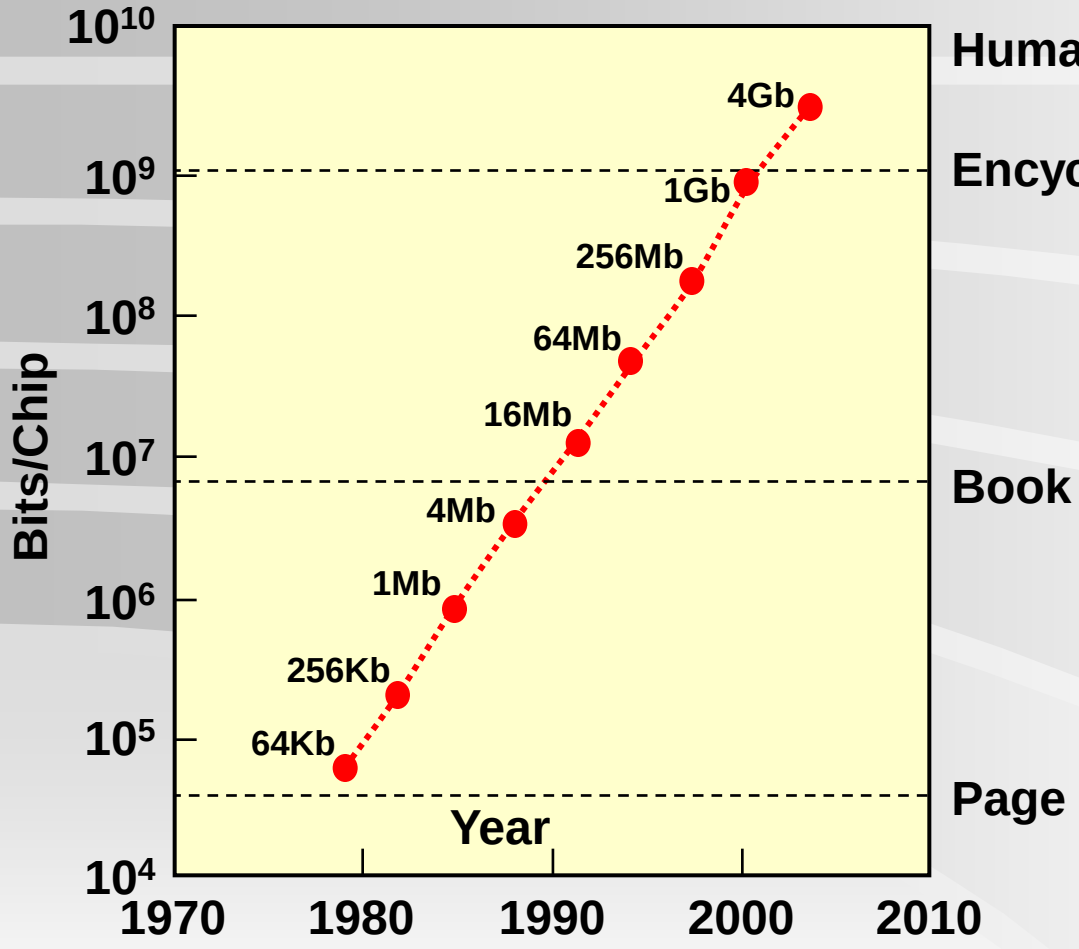
1 >100 # devices/person



Computing power | Personalized devices | Accessing the smart environment

1990 1995 2000 2005 2010 2015

Information Storage Capacity of Silicon Chips

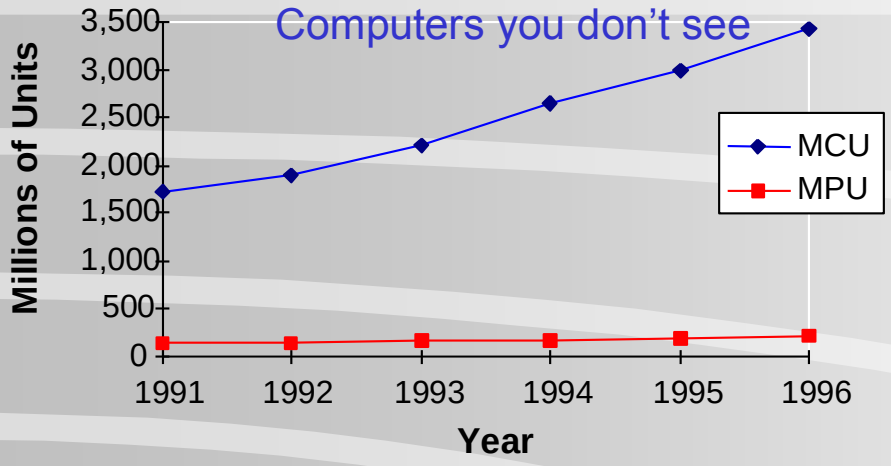


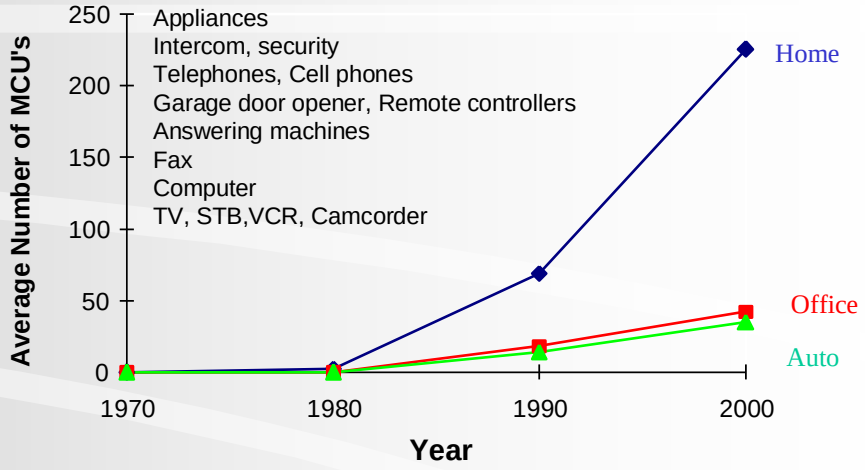
(from M. Green)

Ano	Dens.	Ref.
1970	1 kb	
2000	512 Mb	
2030	10^{13} b	1 cérebro
	10^{15} b	Biblioteca do congresso
	10^{20} b	Cultura humana
2075	10^{23} b	Todos os cérebros

(Garner et al, livro MEMS+ AVS2003)

Where Are the Transistors?





Source: ICE "Status 1996"

- Microprocessors and Microcontrollers are ubiquitous in our lives

  (onipresente)

(from M. Green)

CI’s oferecem:

muitas funções
alta velocidade de operação

Com:

- baixo custo
- baixo consumo de potência
- tamanho reduzido
- massa reduzida e alta confiabilidade.

Microfabricação desenvolveu-se para Microeletrônica (disp. discretos e CI´s),

- Hoje apresenta novas aplicações:
  - optoeletrônica
  - fotônica
  - microssensores e atuadores
  - micromecânica
  - estruturas para biologia
  - montagem de módulos de CI´s
- Atualmente: $\Rightarrow$ Nanofabricação, Nanoeletrônica.

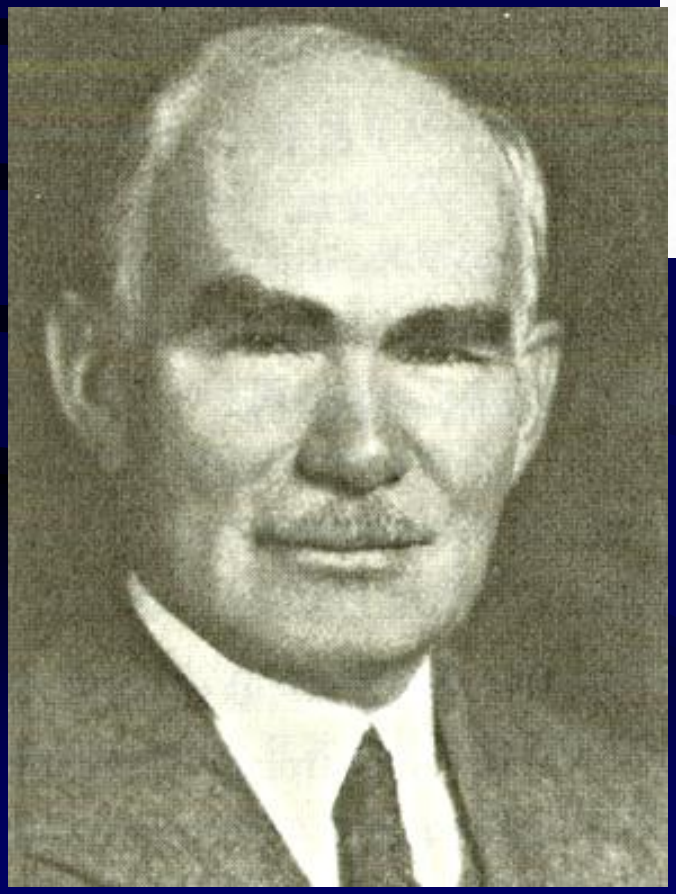
Evolução de Microeletrônica, Regras de Escalamento e Limites

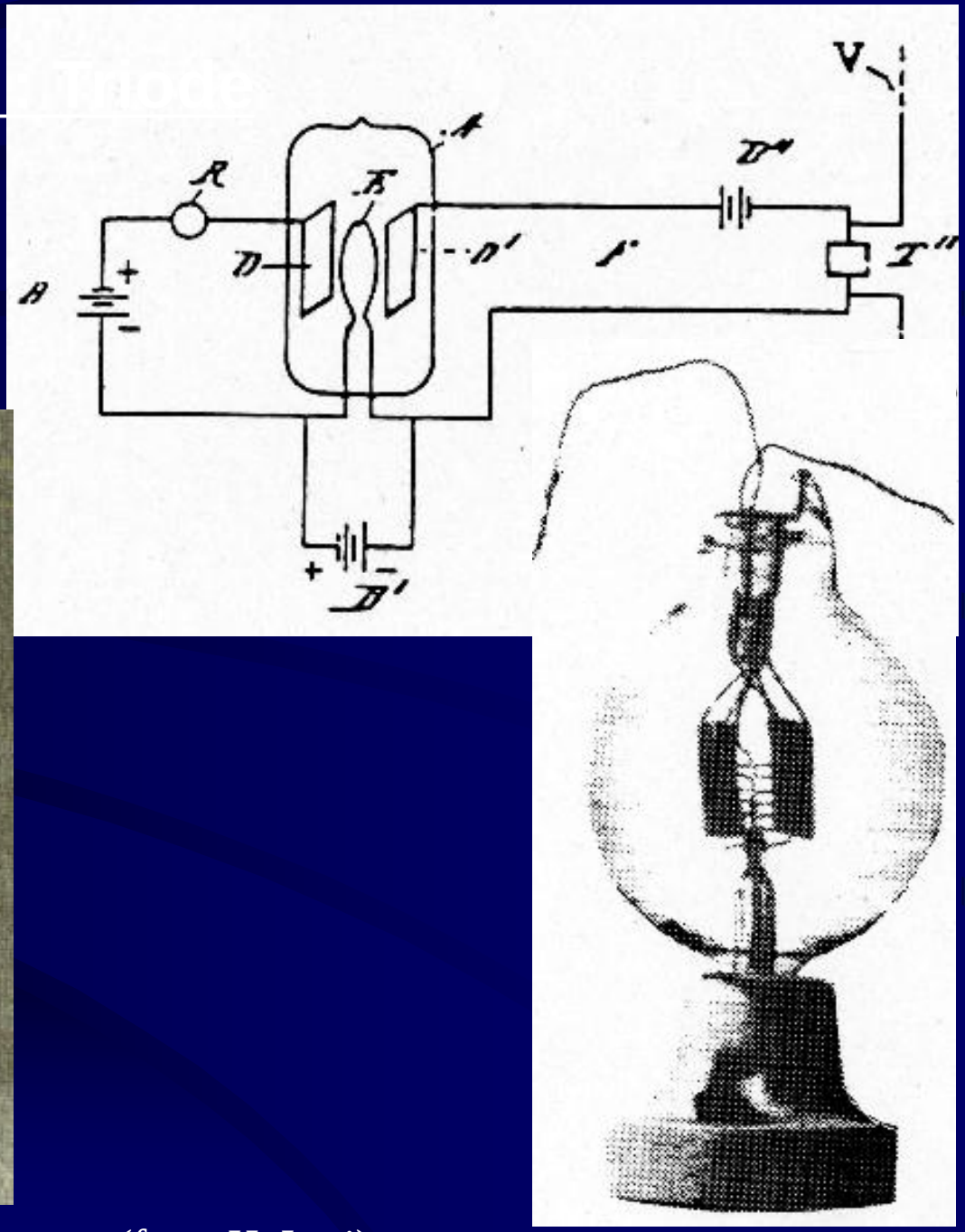
2. História e Evolução da Microeletrônica

- Século 19
  - falta de conhecimento teórico
  - 1874: retificador de PdS - F. Braun

1906: Vacuum Tube

Lee De Forest





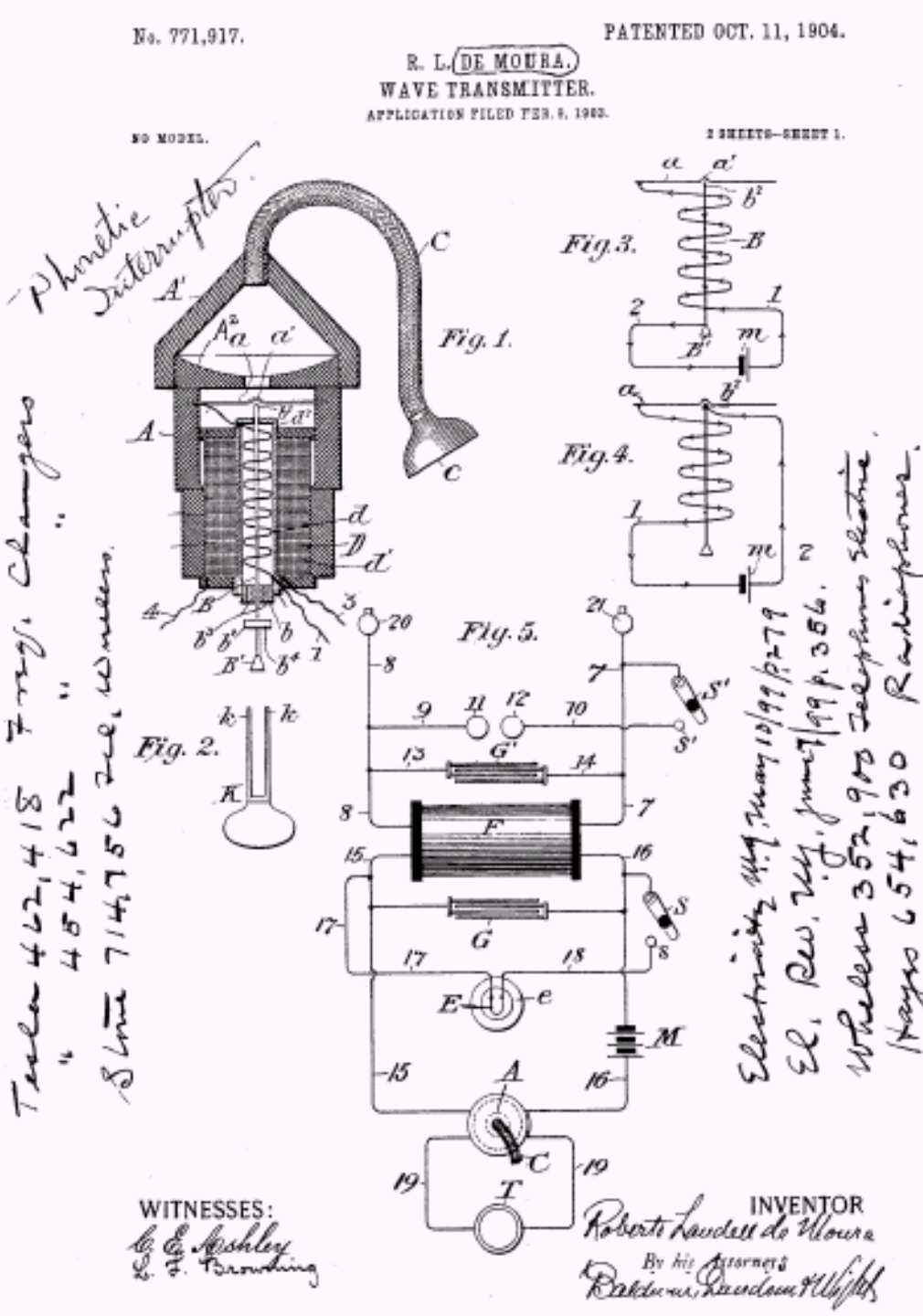
(from H. Iwai)

Pe. Roberto Landell de Moura

- Transmissor de ondas eletromagnéticas (luz ou RF), modulado por som.
- Aplicações: telégrafo e telefone sem fio.
- Dispositivos: Interruptor fonético, lâmpada transmissor de 3 terminais, receptor de Se.

- Patentes no USA:
  - #775,337: “Wireless Telephone”, filed Oct.4, 1901, approved Nov.22, 1904
  - #775,846: “Wireless Telegraph”, filed Oct.4, 1901, approved Nov.22, 1904
  - #771,917: “Wave-Transmitter”, filed Feb.9, 1903, approved Oct.11, 1904.
- *Pe. Landell de Moura permaneceu no USA, de 1901 a 1904, para conseguir as patentes.*

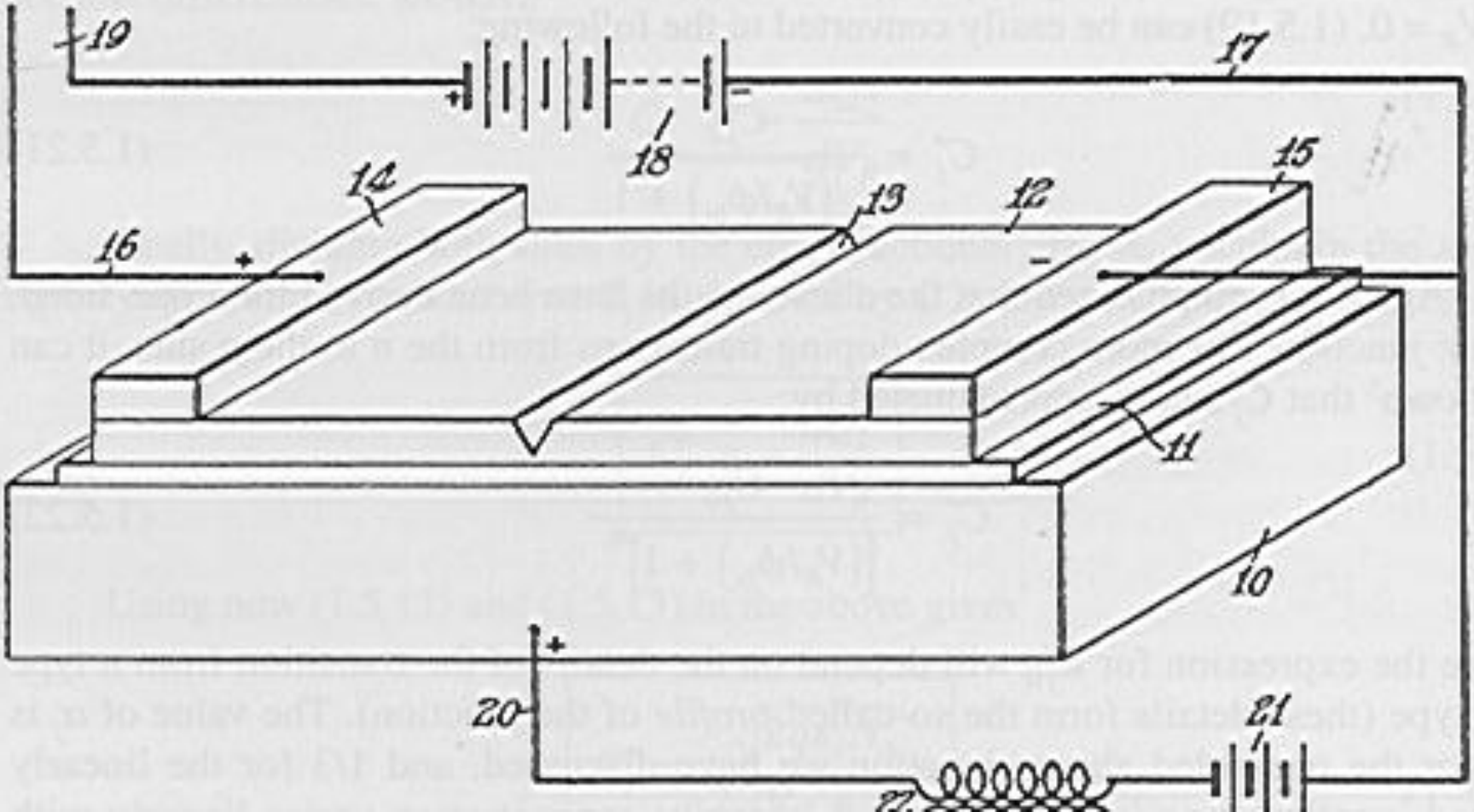
- Princípios:
  - modular a emissão de uma lâmpada (de arco) ou outro dispositivo de emissão.
  - Modulação sonora por diafragma ligado a chaves liga/desliga, que chaveia a corrente pelo emissor.
  - Receptor: um resistor de Selênio.
- Item E = lâmpada de arco
- Laboratório em Campinas, a partir de 1892.
- Demonstração de transmissão entre Av. Paulista e morro de Santana, 8km, em 1894.
- Em 1905 solicitou 2 navios ao presidente Rodrigues Alves para demonstrar sua comunicação entre os mesmos a qualquer distância. Os assessores o consideraram louco!
- Marconi: 1º experimento simples em 1895 e 1º radiograma em 1900.



- Início do século 20:
  - teoria de mecânica quântica, Schrödinger, etc
  - patente de transitor FET, 1928, Lilienfeld, sem sucesso experimental (estados de superfície)

Lilienfeld, “um homem muito à frente do seu tempo”!

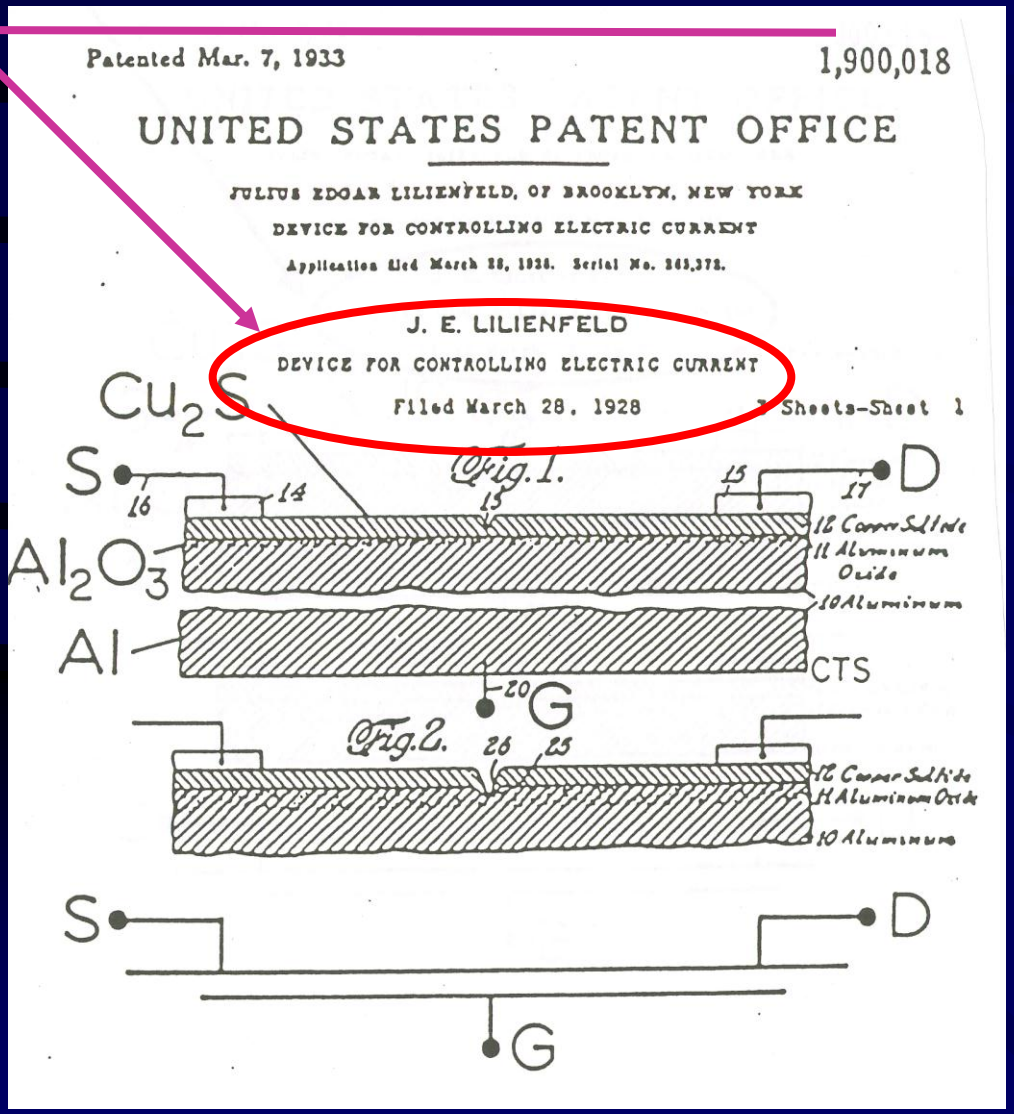
The body interface to the oxide is often called the *surface*.



J. E. LILIENFELD

DEVICES FOR CONTROLLED ELECTRIC CURRENT

Filed March 28, 1928



Patented Mar. 7, 1933 1,900,018

UNITED STATES PATENT OFFICE

JULIUS EDGAR LILIENFELD, OF BROOKLYN, NEW YORK

DEVICE FOR CONTROLLING ELECTRIC CURRENT

Application filed March 28, 1928. Serial No. 263,378.

J. E. LILIENFELD

DEVICE FOR CONTROLLING ELECTRIC CURRENT

Filed March 28, 1928 2 Sheets-Sheet 1

Cu_2S

S 16 14 13 15 17 D

12 Copper Sulfide

11 Aluminum Oxide

Al_2O_3

10 Aluminum

Al

CTS

20 G

Fig. 1.

Fig. 2. 26 25

12 Copper Sulfide

11 Aluminum Oxide

10 Aluminum

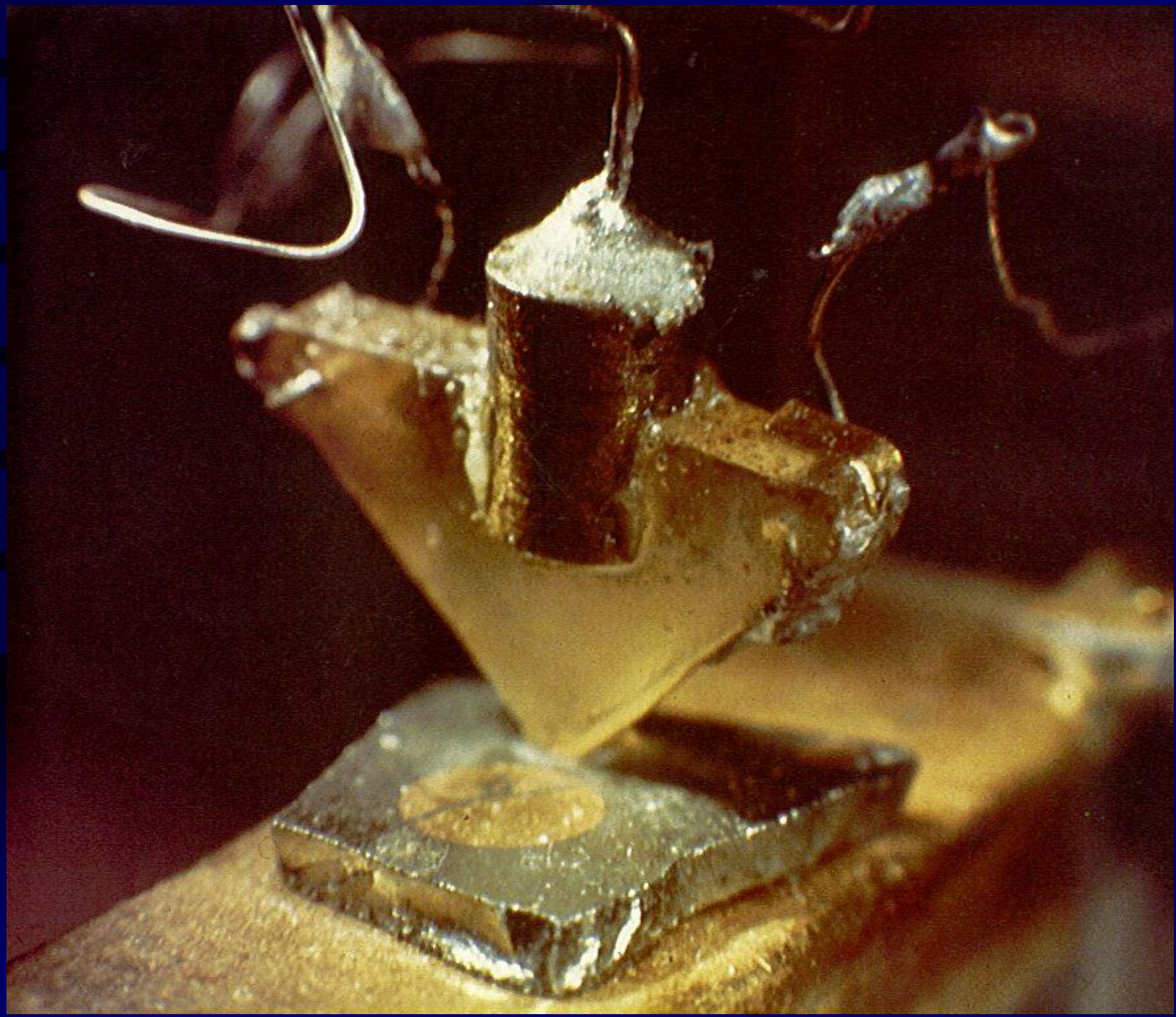
S D

G

J.E.LILIENFELD

(from H. Iwai)

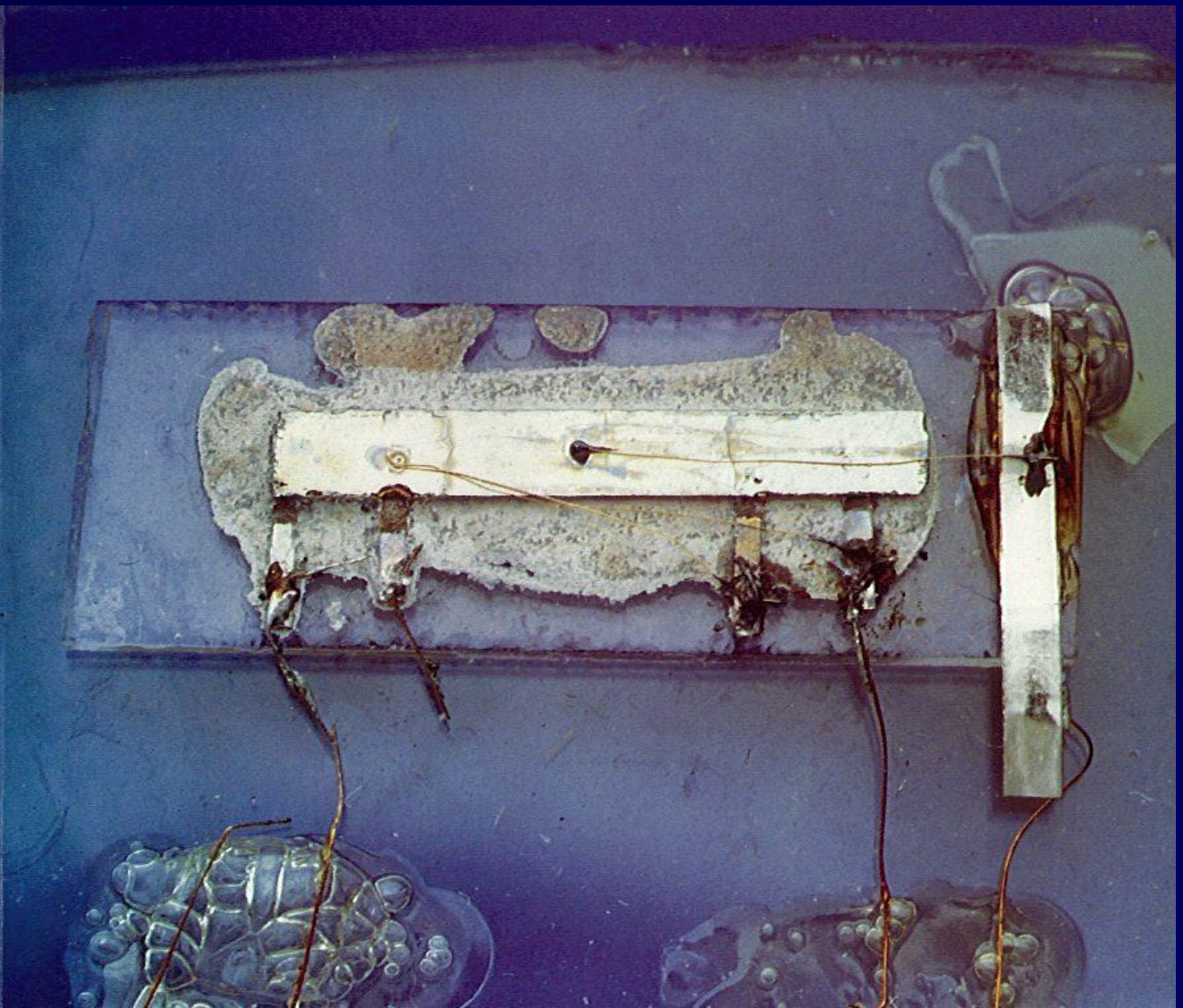
- 1936 - Grupo de estado sólido na Bell Labs
- 1940 - R. Ohi, identifica Si tipo p e tipo n
- 1940 - 1945, desfeito o grupo da Bell Labs
- 1946 - Novo grupo na Bell - W. Shockley
- 1947/Dez., Bardeen e Brattain descobrem o efeito transistor bipolar



J. Bardeen, W. Brattain, W. Shockley

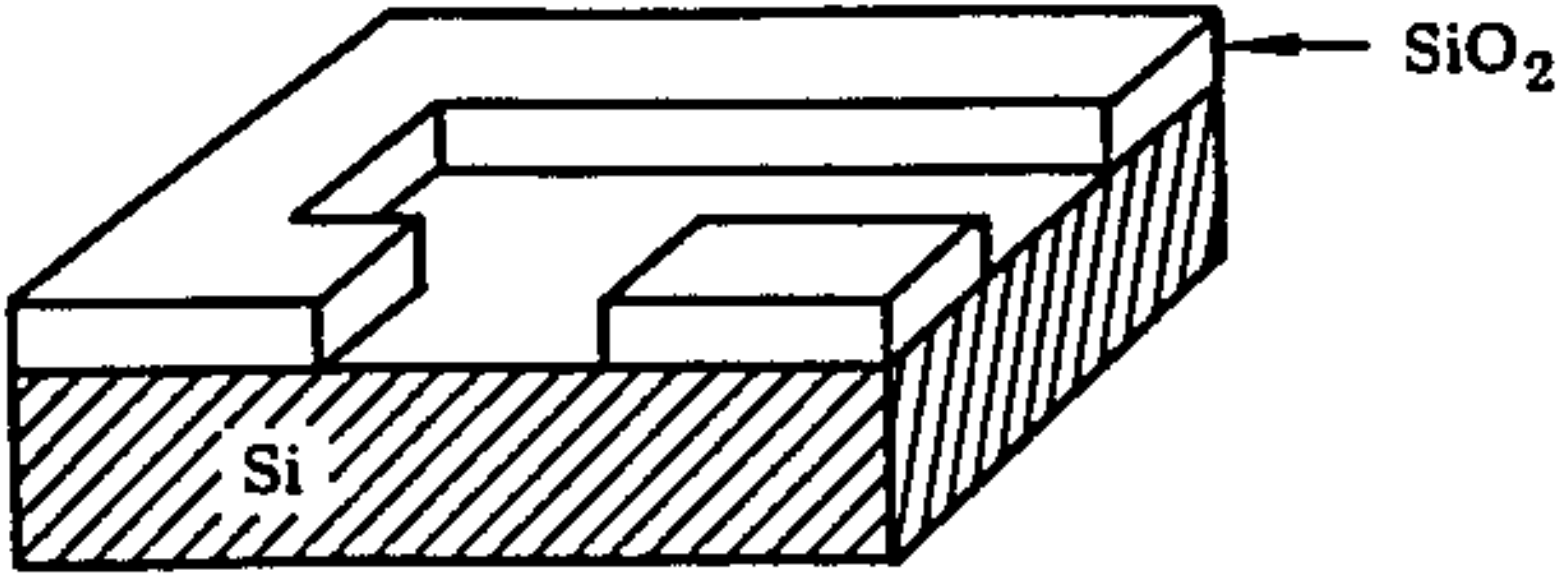
- 1948 - 1950: Shockley - teoria BJT
- 1952: Bell Labs licencia a patente para outras empresas: Texas, Sony, etc.
- 1956: prêmio Nobel de Física
- 1955: Shockley deixa a Bell e cria empresa Shockley Semicond., no Silicon Valey.
- 1957: R. Noyce, G. Moore e outros, deixam a Shockley Semicond., criam Fairchild.
- 1968: Noyce, Moore, Grove, criam Intel.
- Multiplicam-se as empresas no Vale do Si.

- 1958: J. Kilby, Texas Inst., patente de CI, usando processo rudimentar:



Processo Planar

- 1958 - J. Hoerni, Fairchild, processo planar:
  - Superf. Si oxidado + fotogravação, abertura de janelas para difusão, vários no mesmo plano.



(e) Remove resist--pattern transferred to SiO_2

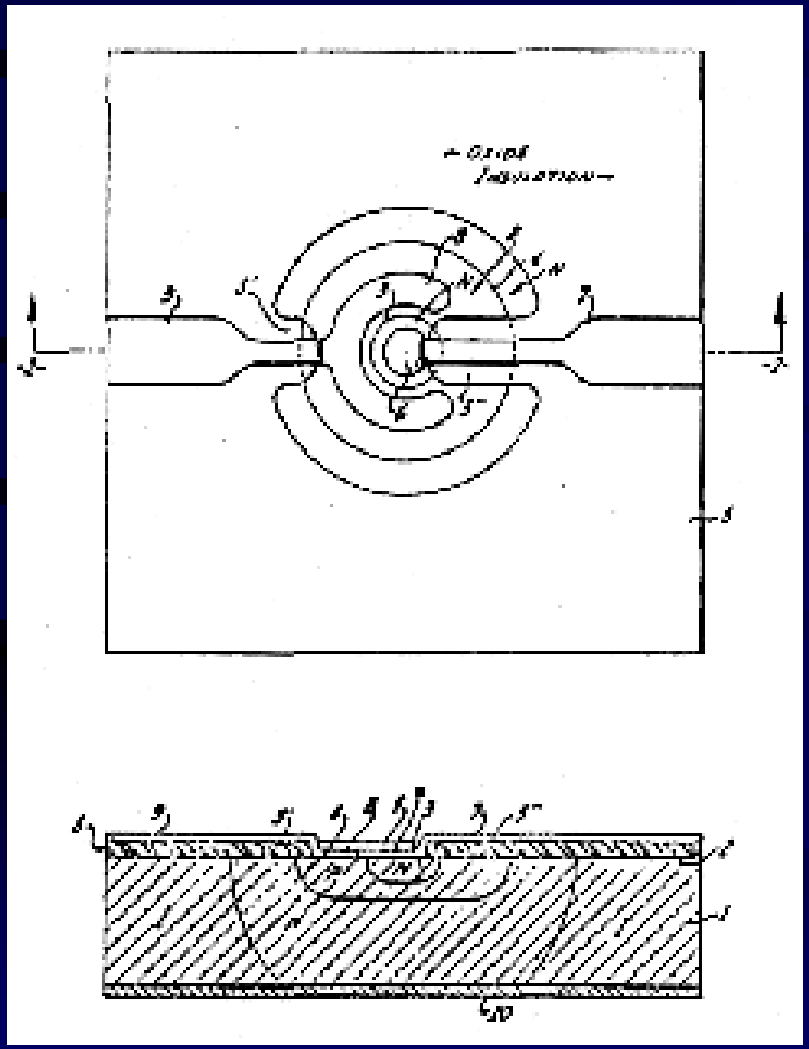
Nature Has Endowed the Silicon Microelectronics Industry with A Wonderful Material: SiO_2

Native to Silicon

- Low Interfacial Defect Density
- Melting Point = 1713°C
- Energy Gap = 9 eV
- Resistivity = 10^{15} Ω-cm
- Dielectric Strength ~ 1 x 10^{7} V/cm
- Dielectric Constant = 3.9

(from M. Green)

1959: 1º Circuito Integrado Planar

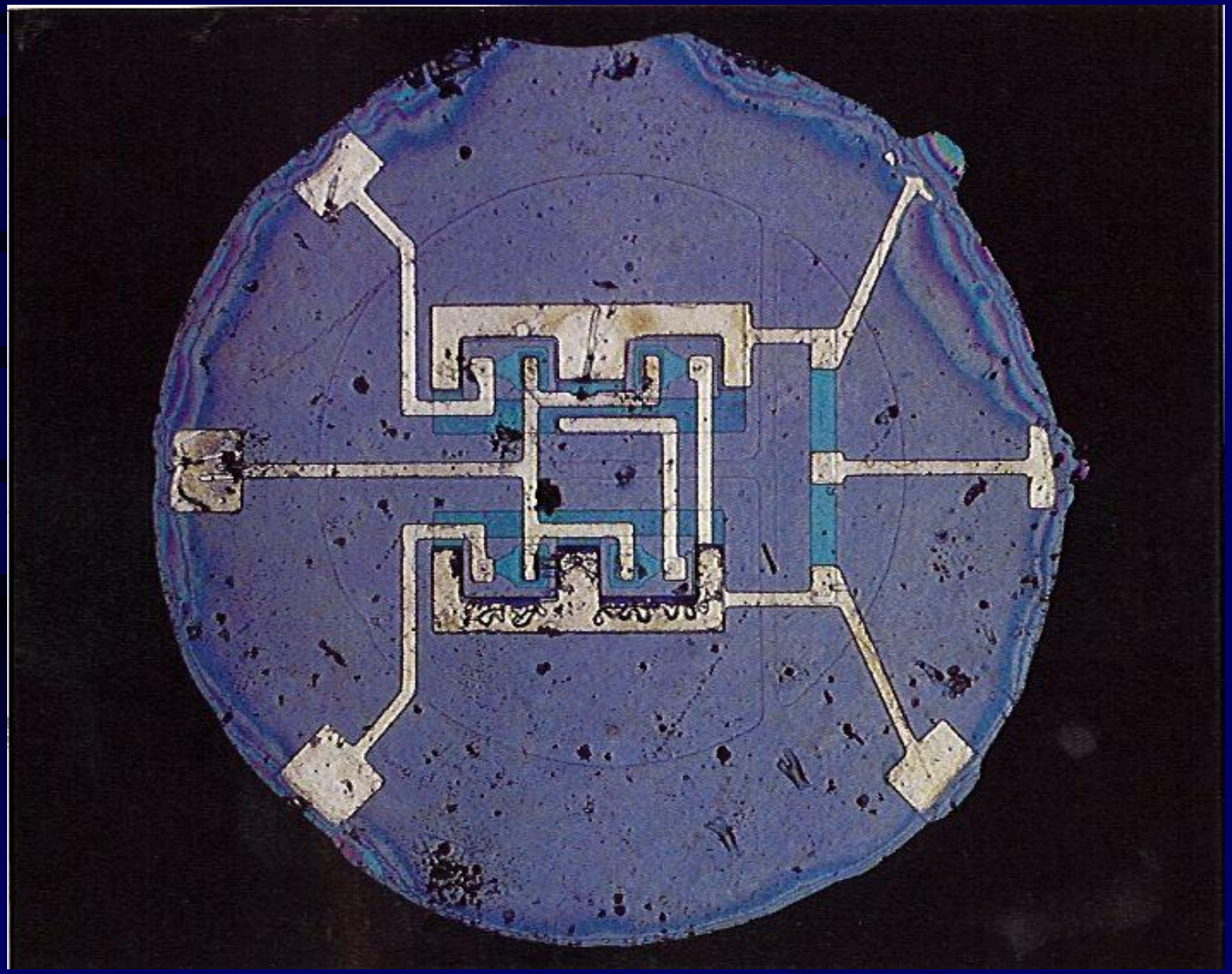


Robert N. Noyce

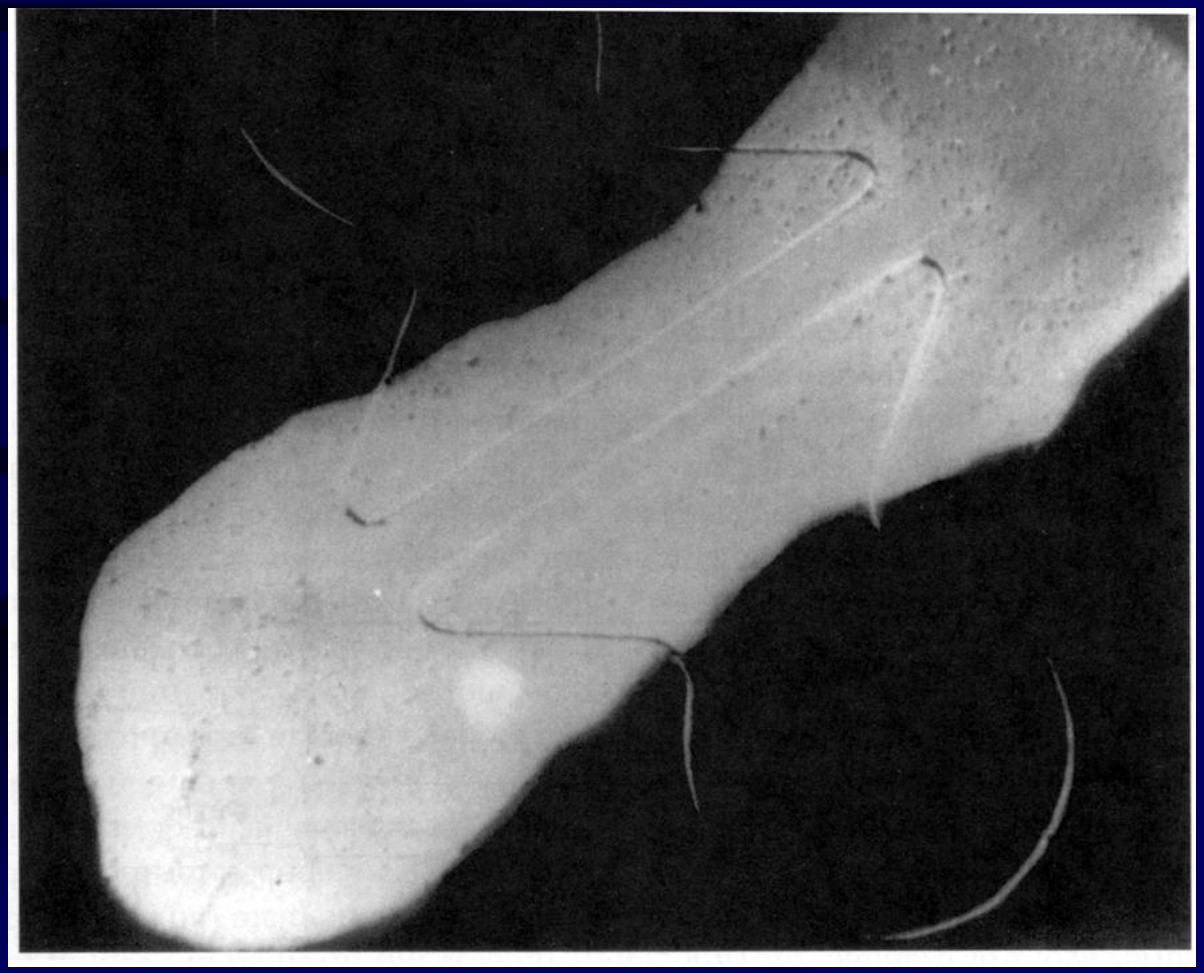
(from H. Iwai)

- 1959 - R. Noyce, Fairchild, processo planar para CI´s. O princípio é usado até hoje, com incorporação de forte evolução.
- 1962 - início da comercialização de CI´s.

Primeiro CI, 1961 - Fairchild



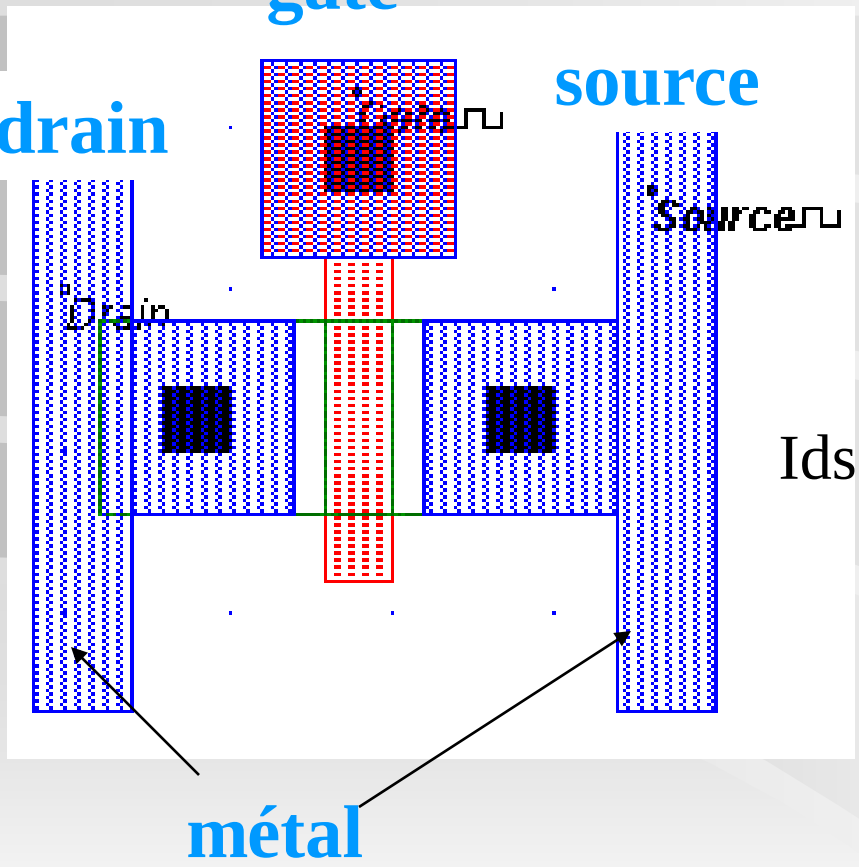
1960: Primeiro MOSFET, por D. Kahng and M. Atalla

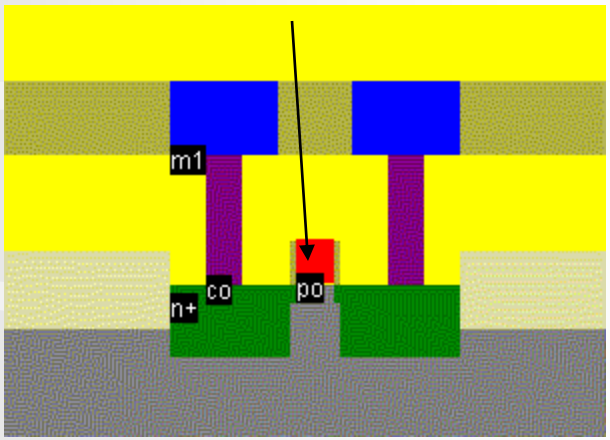


(from H. Iwai)

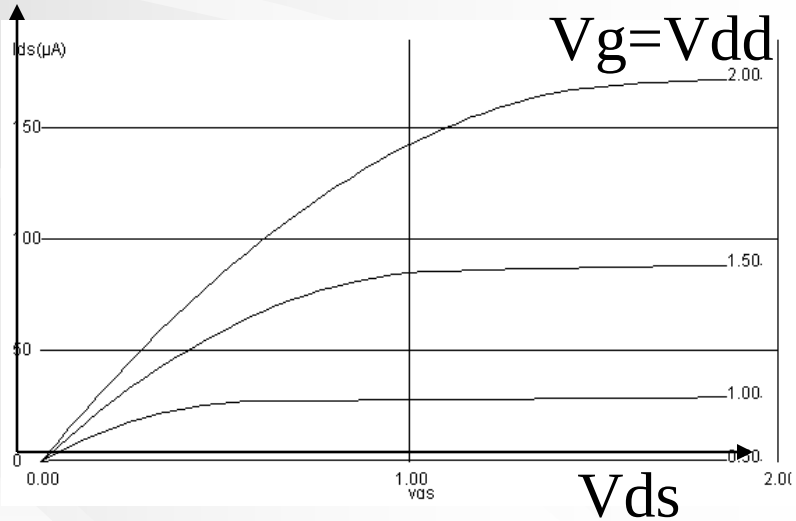
- 1960 - D. Kahng e M. Atalla, Bell Labs, transistor MOS.
- Persistem problemas de estabilidade, cargas no sistema SiO_2/Si
- 1963 - F. Wanlass, Fairchild, CMOS
- Outros grandes avanços na tecnologia MOS
  - uso de porta de Si policristalino (1966)
  - uso de I/I para ajuste de V_T

MOSFET

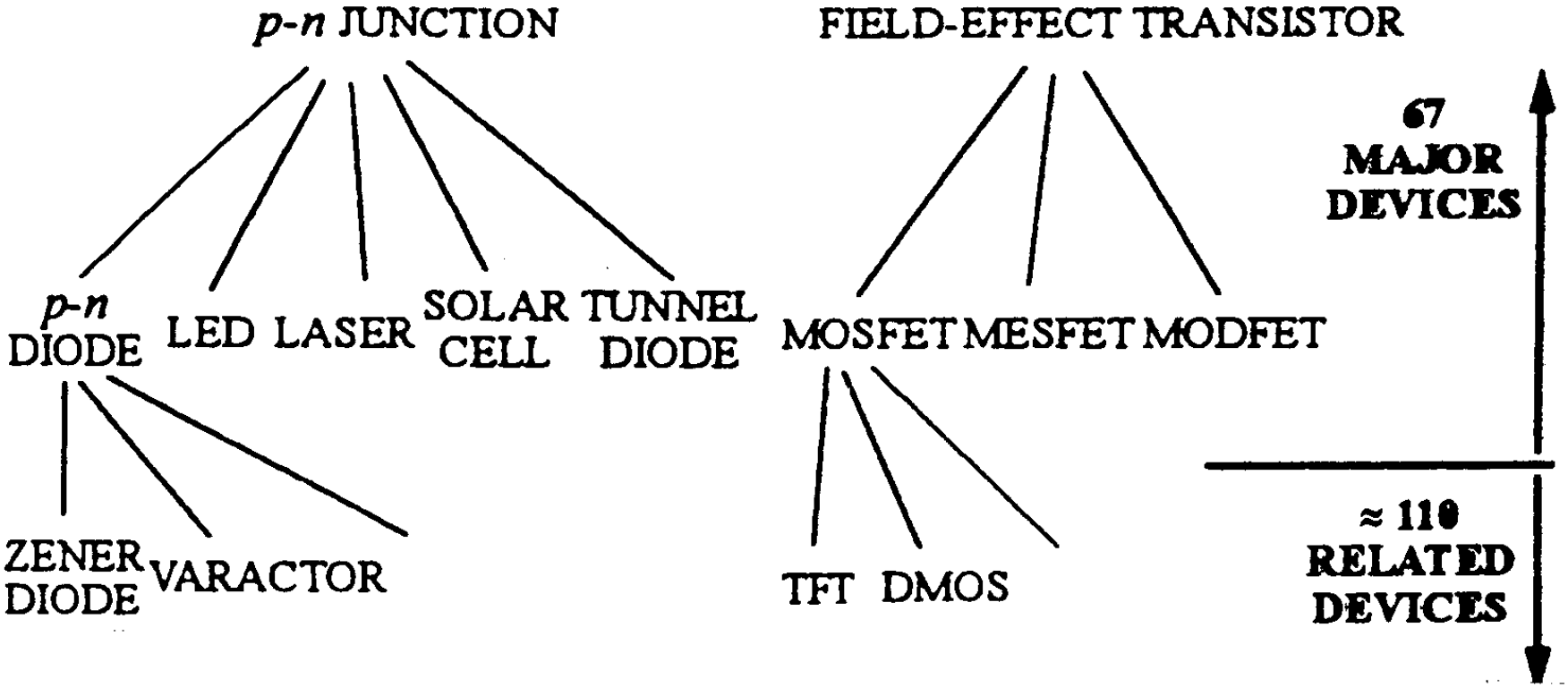

gate
drain
source
métal


g
m1
co
po
n+

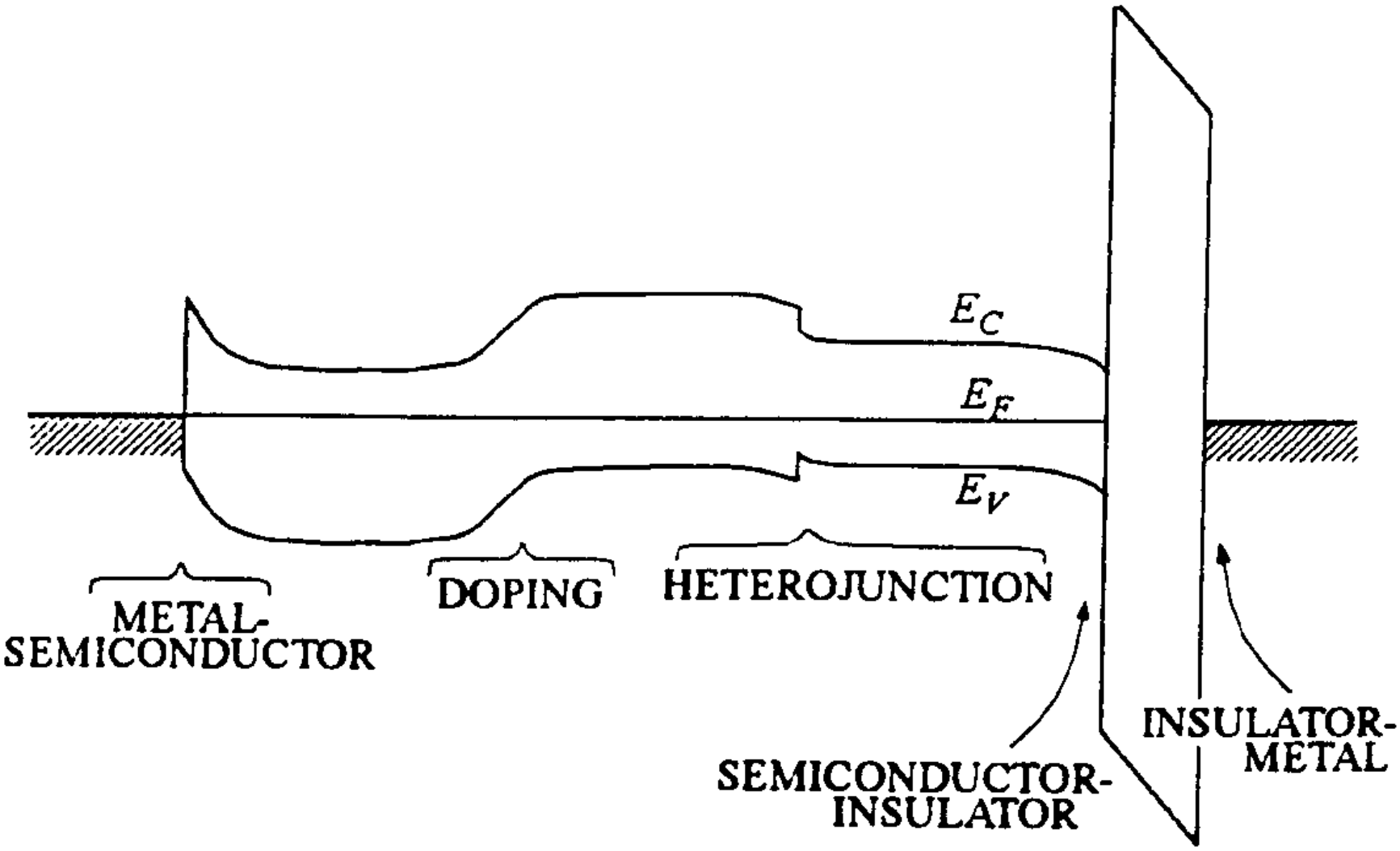
Ids


Vg=Vdd
Ids(µA)
2.00
50
00
1.50
50
1.00
0.00
1.00
vds
Vds

- Segundo K. Ng (IEEE Trans.E.D.Oct. 1996):



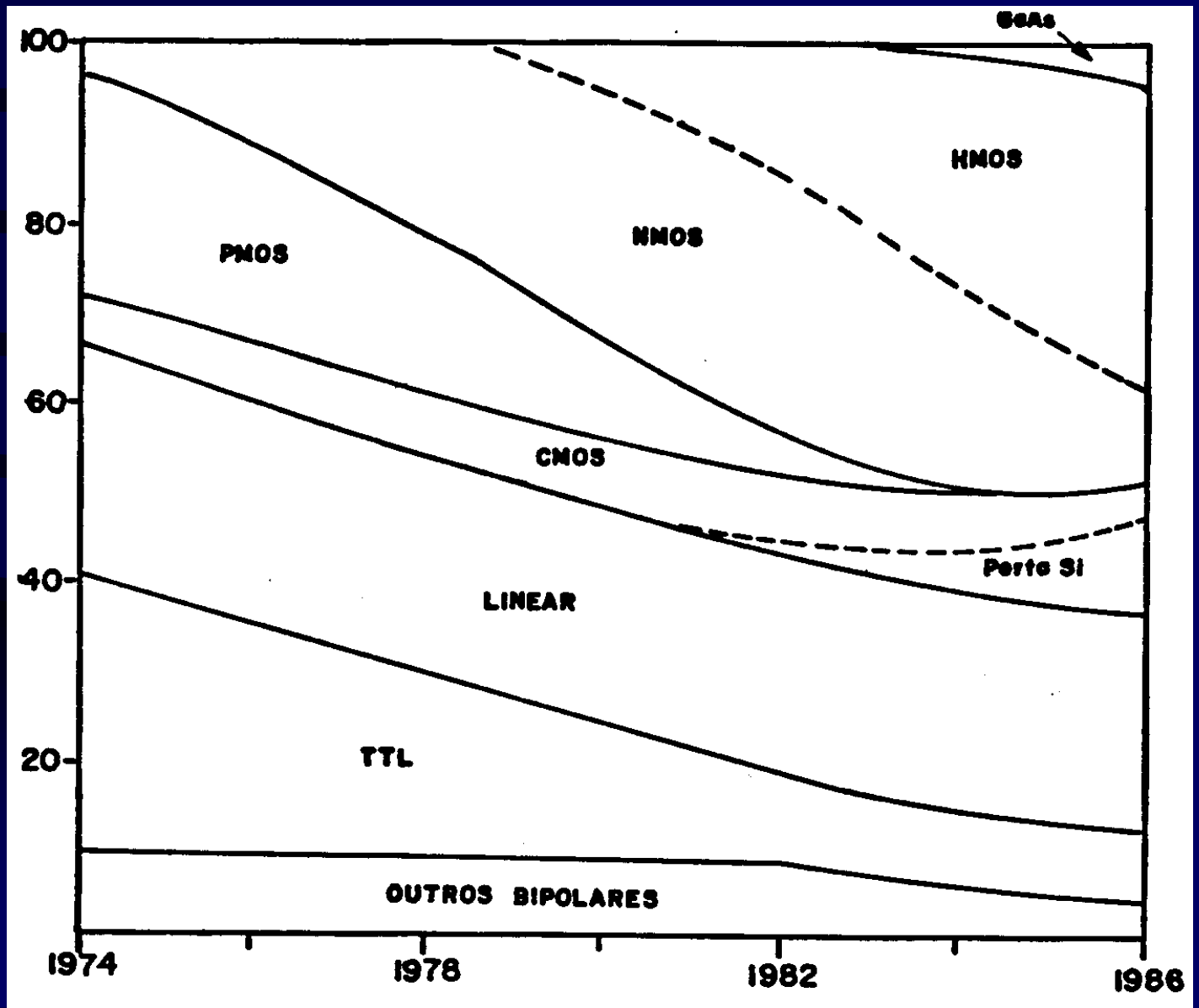
- Desenvolvimento de dispositivos é baseado:
  - a) Blocos construtivos:

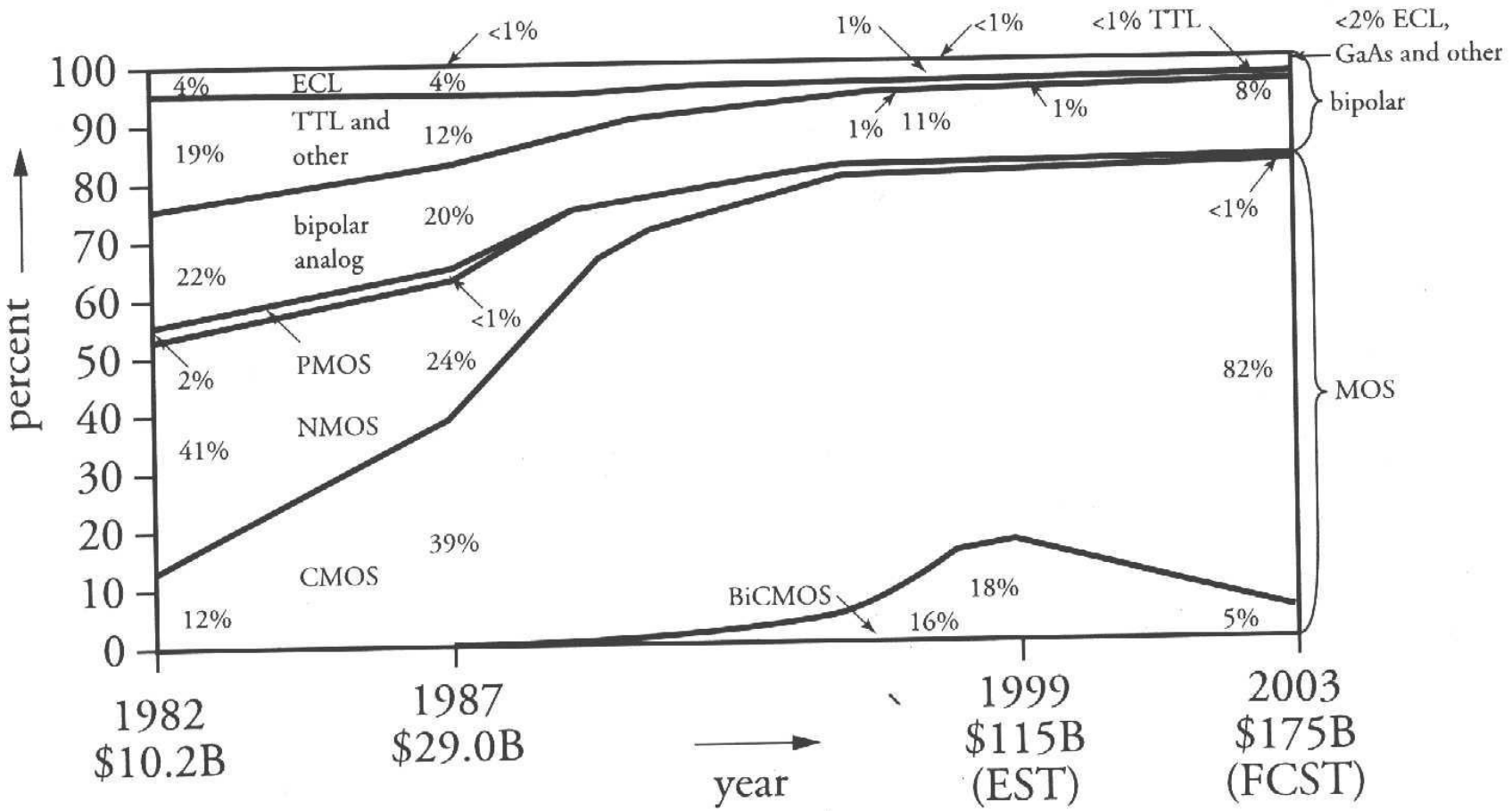


– b) mecanismos de transporte

– Deriva	resistores, transistores FET
– Difusão	junção pn, BJT
– Emissão termiônica	barr. Schottky,
– Tunelamento	diodo túnel, cont. ôhmico
– Recombinação	LED, Laser, diodo p-i-n
– Geração	célula solar, fotodiodo
– Avalanche	IMPATT, ZENER, APD

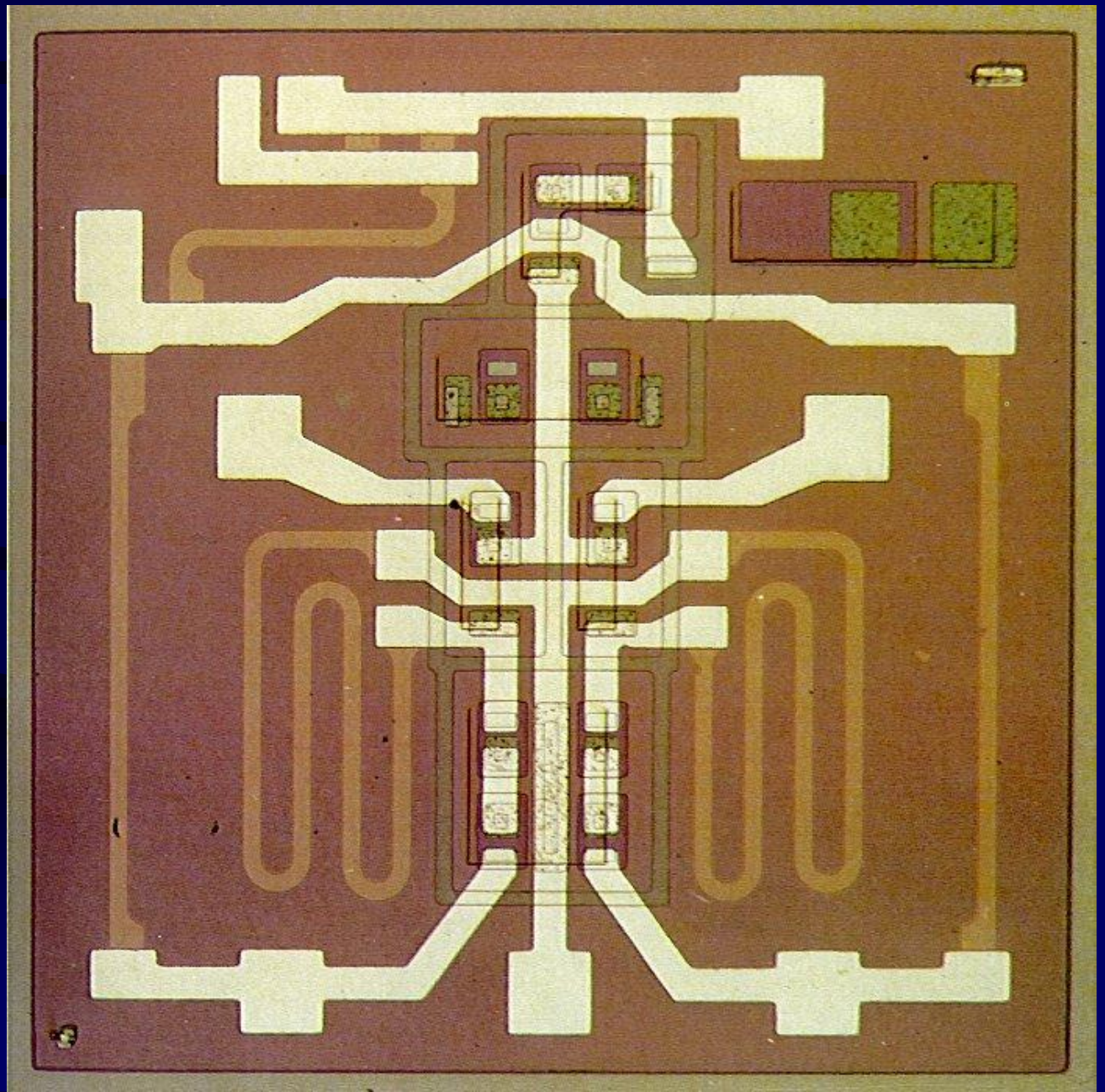
Tecnologias dominantes p/ CI: BJT, MOS
Atualmente, > 85 % é CMOS



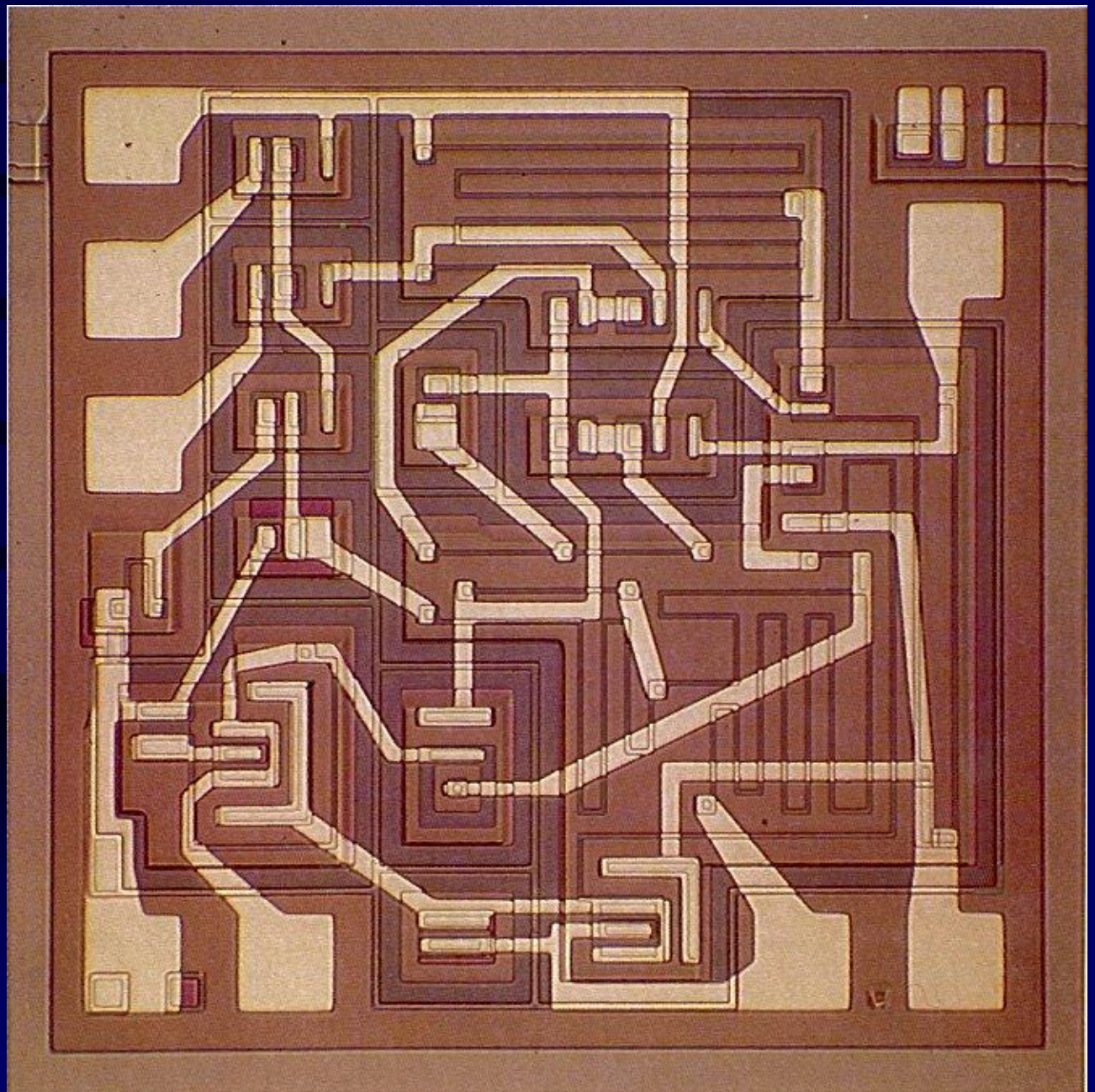


ICE, in Deep-Submicron CMOS ICs, H. Veendrick

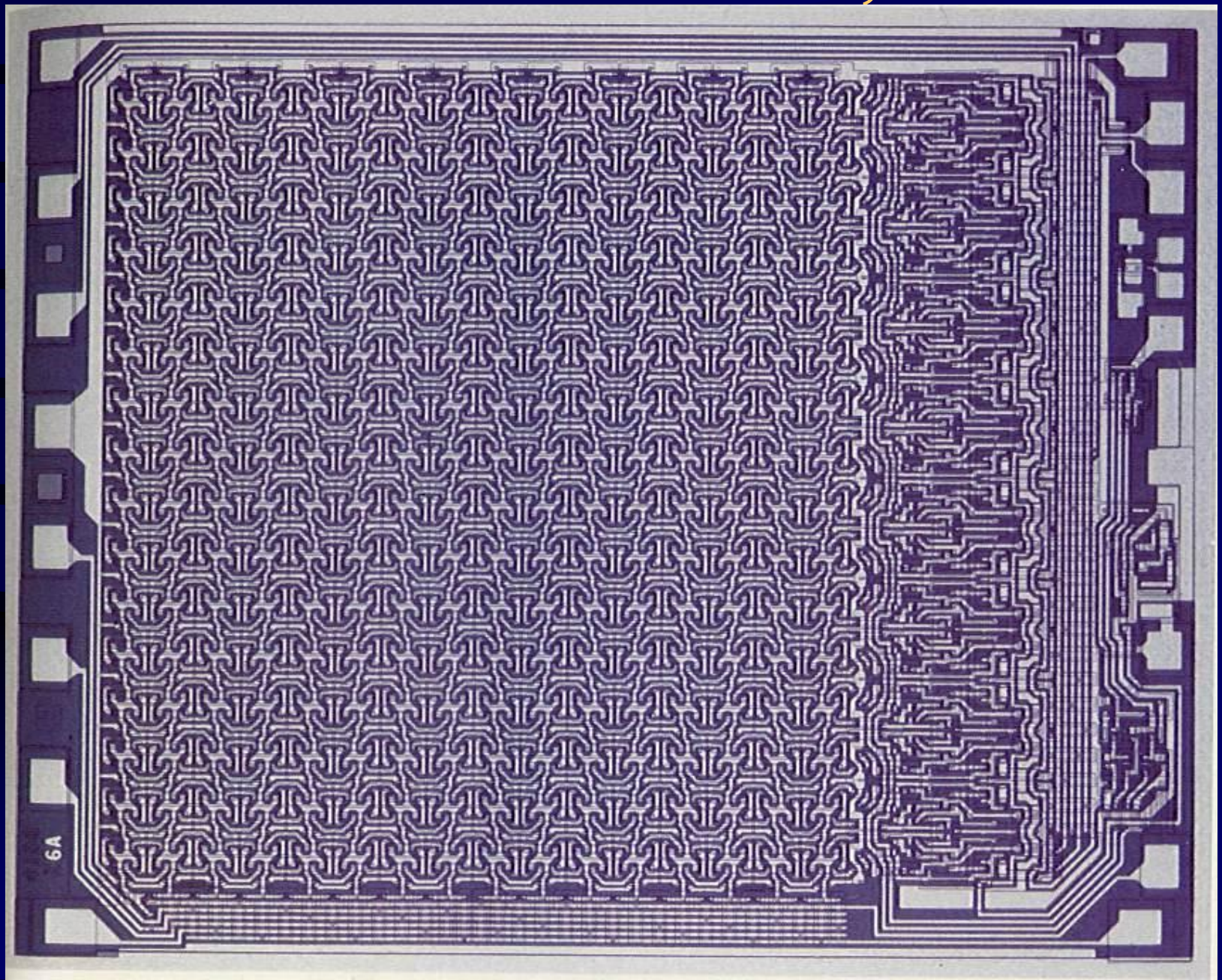
1964 - Op-Amp μA702, Fairchild



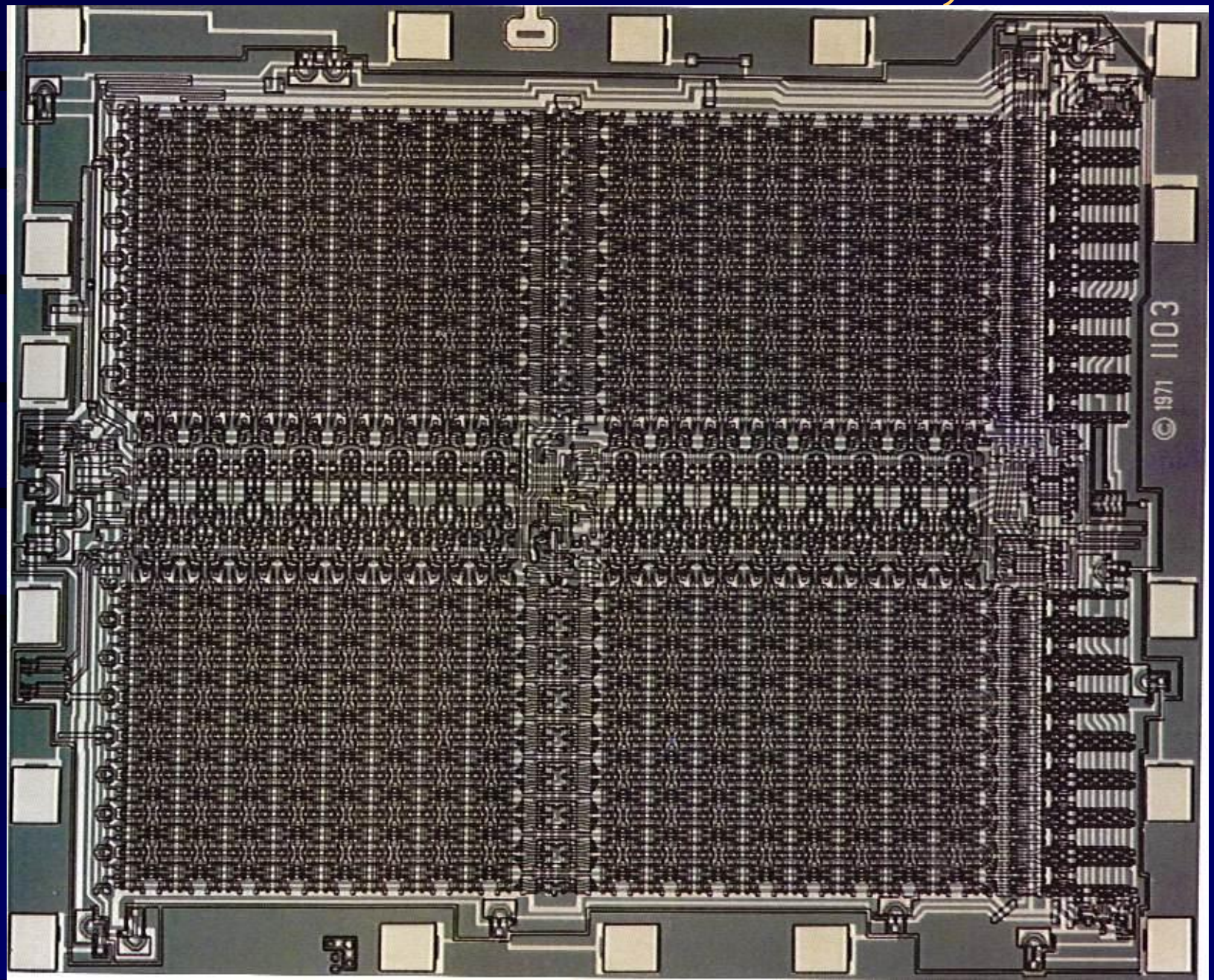
1965 - Op-Amp μA709, Fairchild



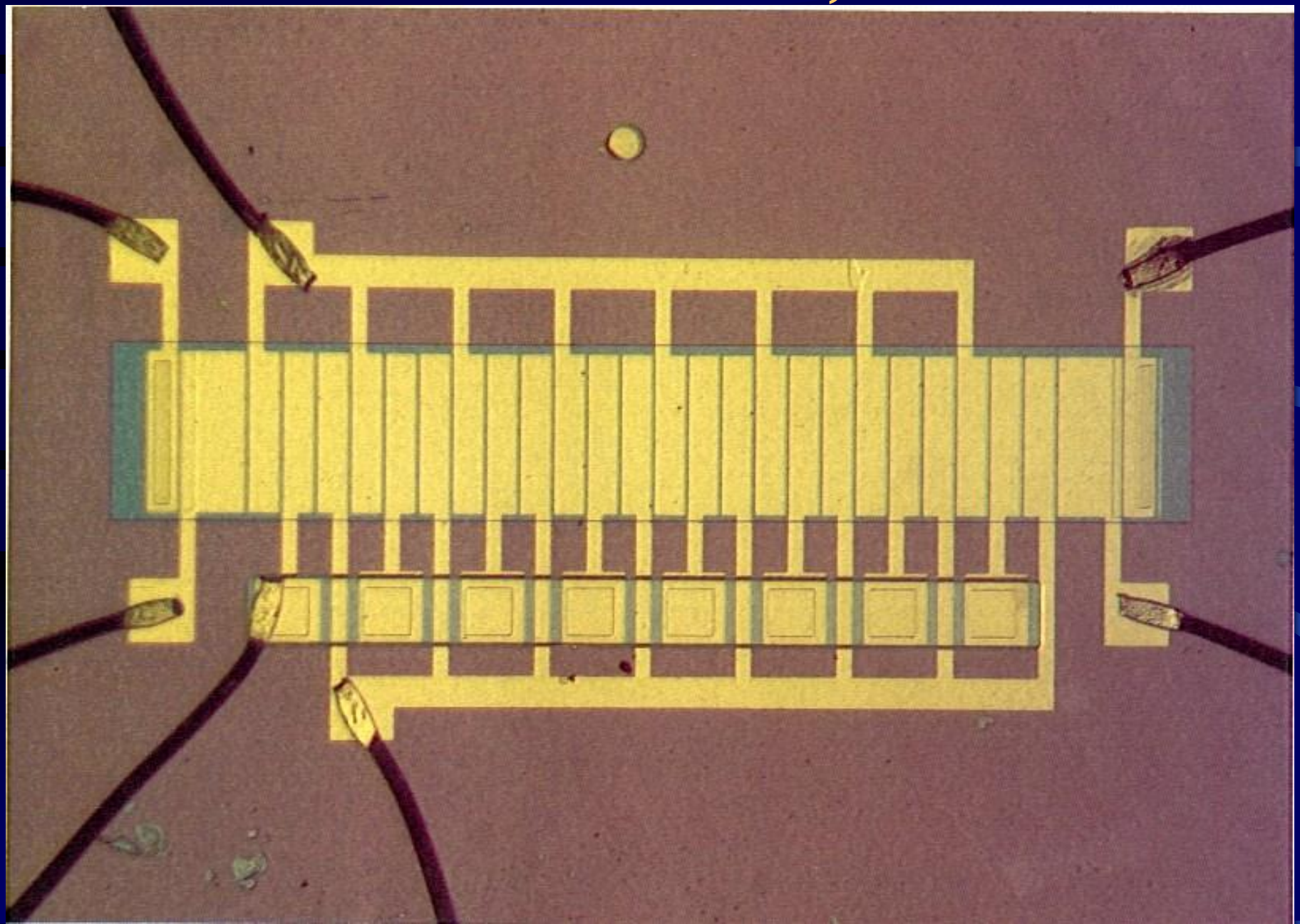
1970 - SRAM 256 Bit, Fairchild



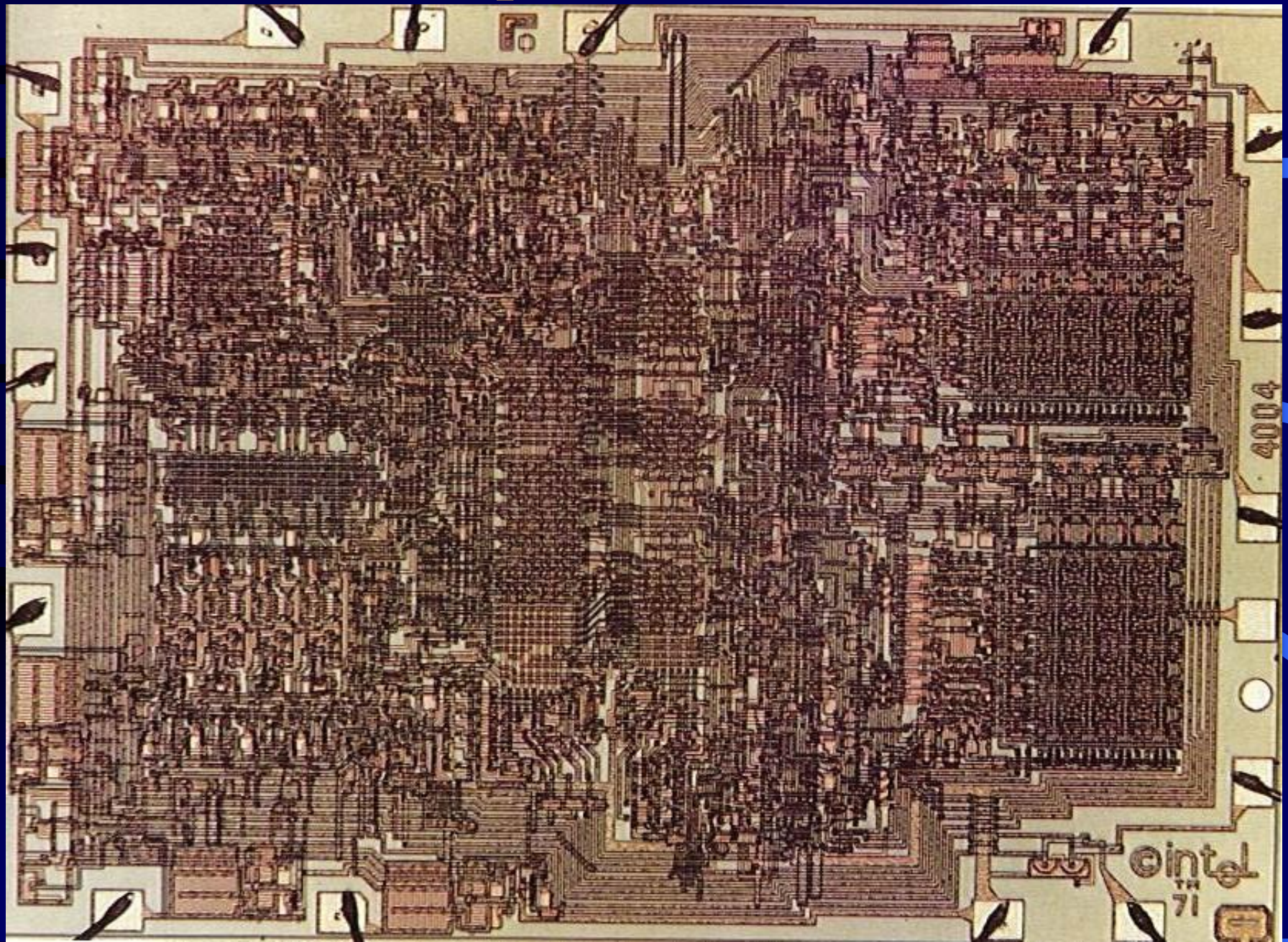
1970 - 1024 Bit DRAM, Intel



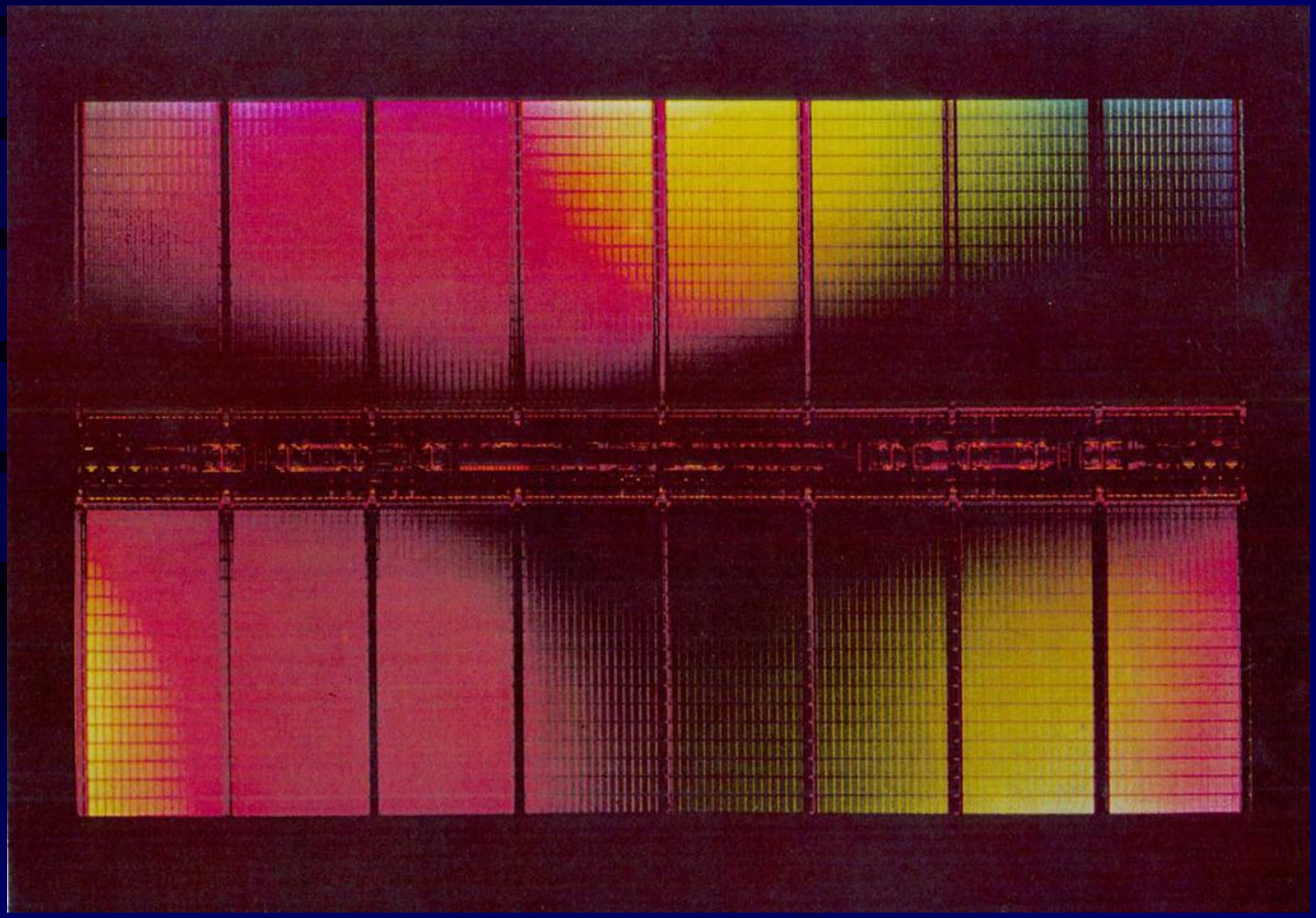
1970 - CCD 8 Bit, Bell Labs



1971 - Microprocessador 4004, Intel

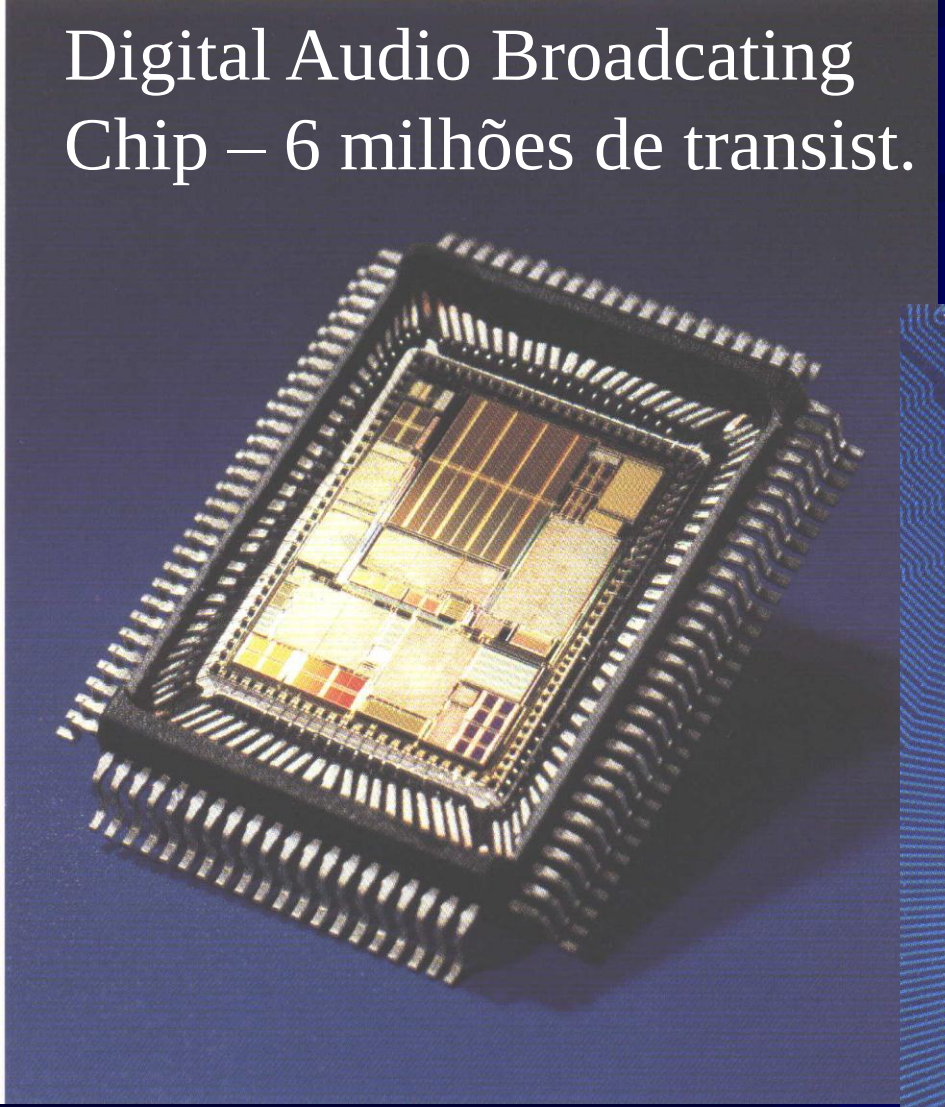


2001 - 256Mbit DRAM (TOSHIBA)

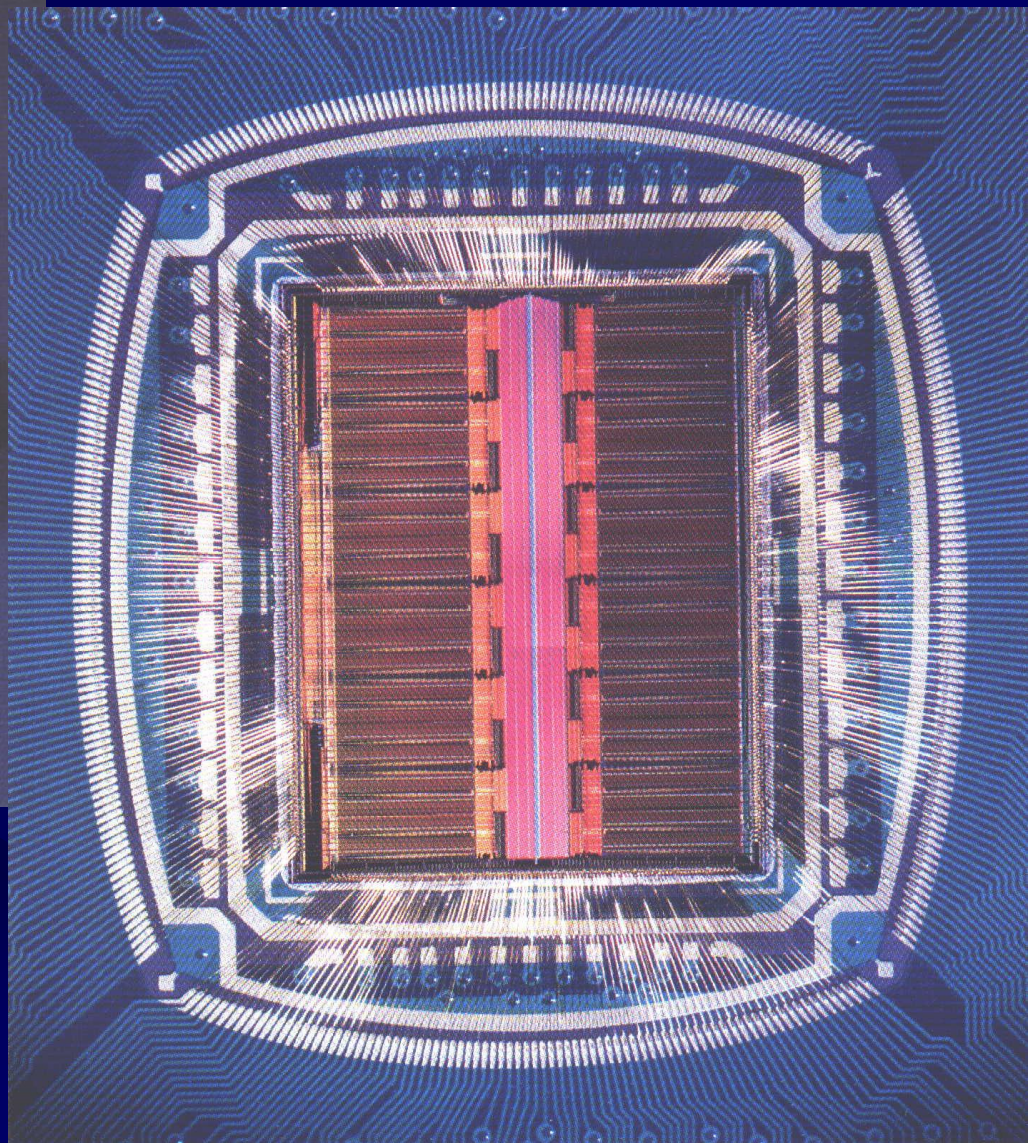


(from H. Iwai)

Digital Audio Broadcating Chip – 6 milhões de transist.



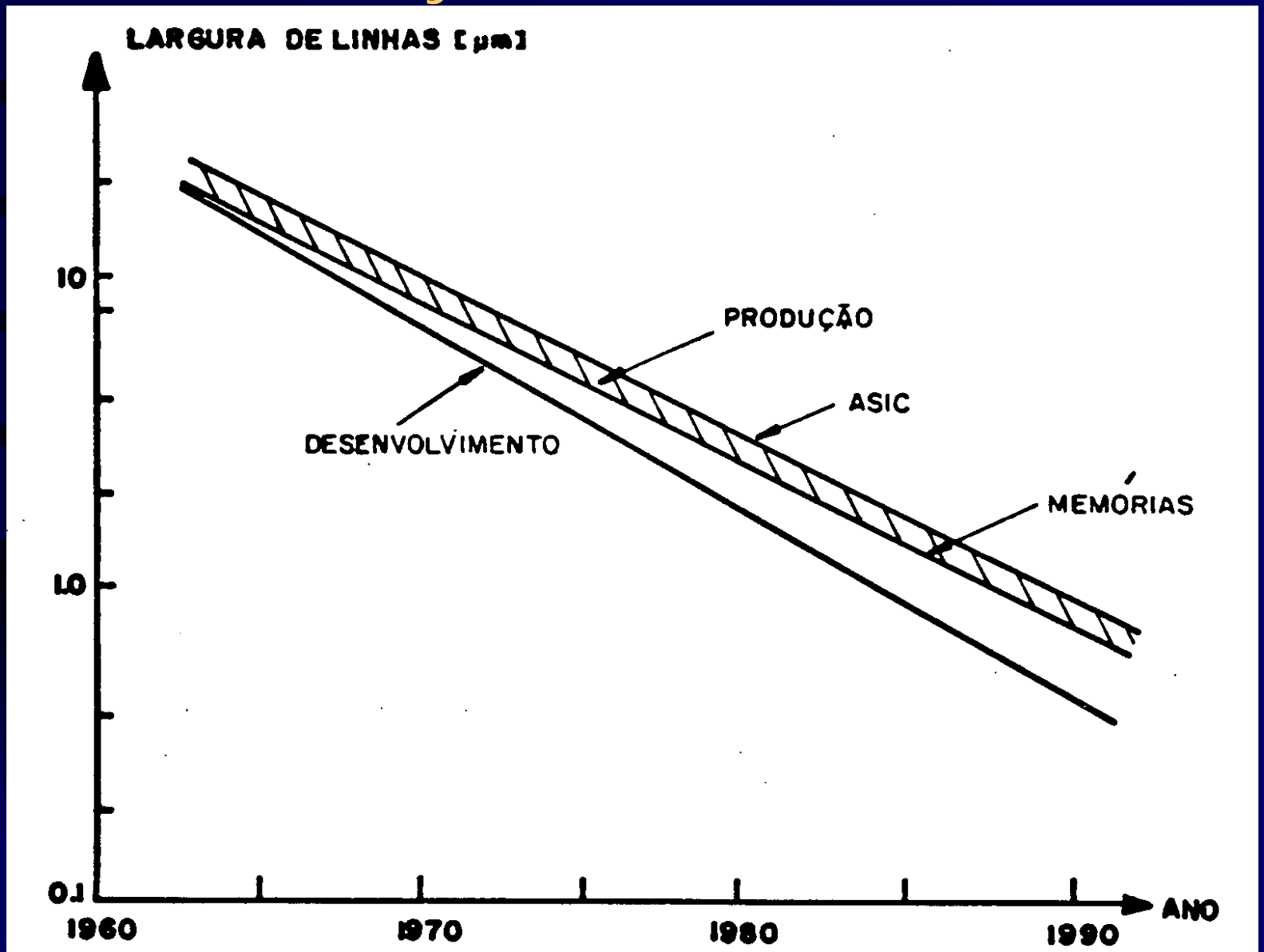
Complex Programmable Logic Device – 9 milhões de transistores.



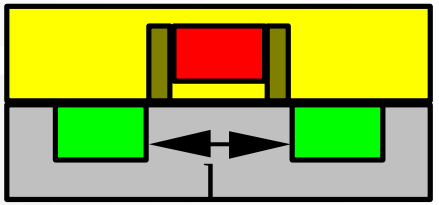
Philips, in Deep-Submicron CMOS ICs, H. Veendrick

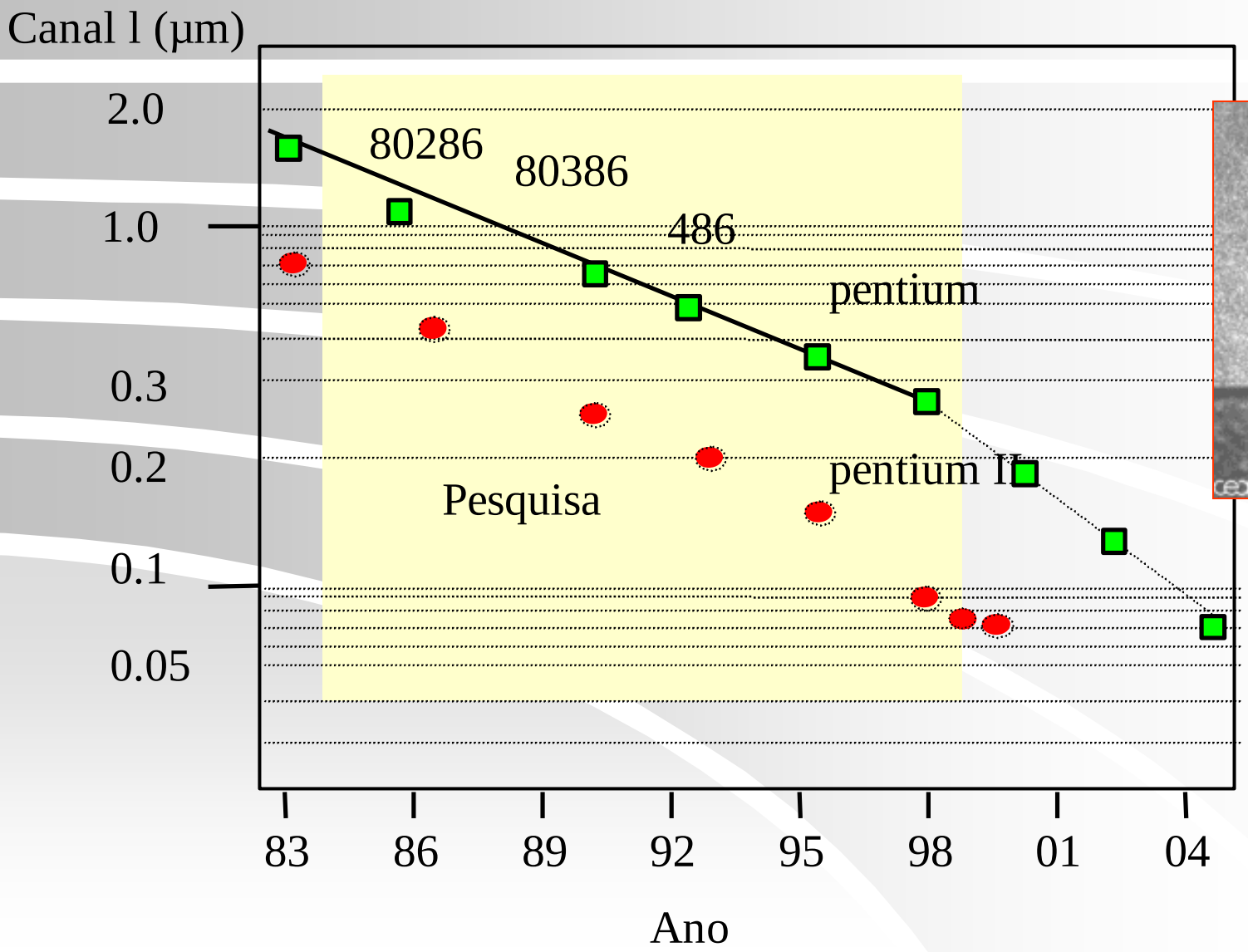
Evoluções Tecnológicas:

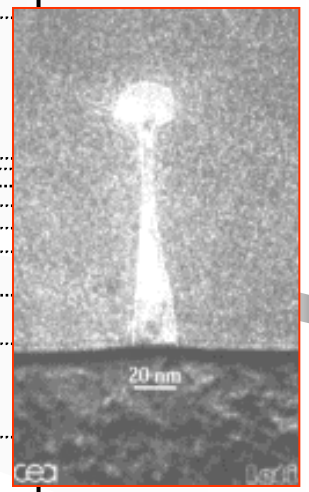
- Redução nas dimensões



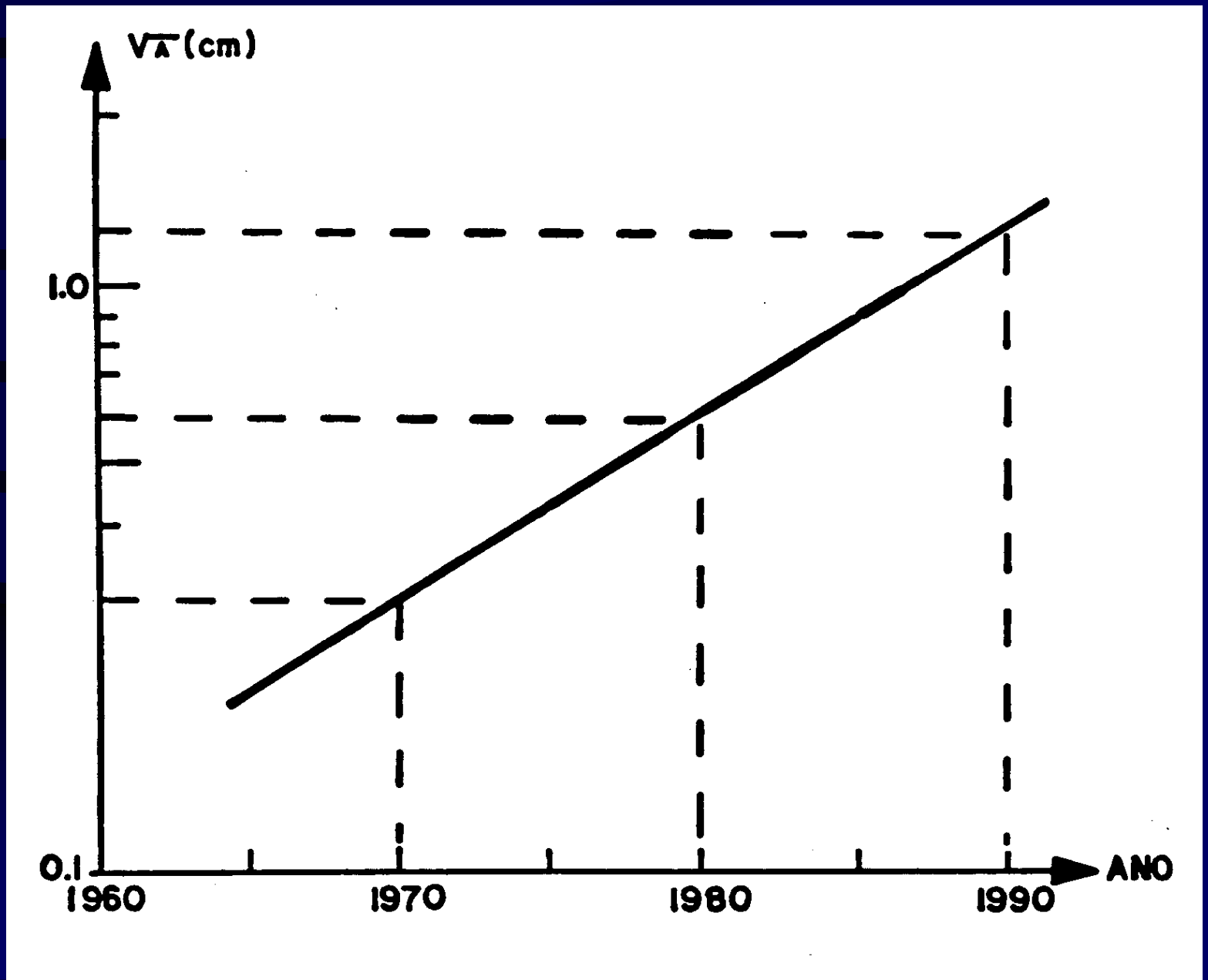
1. Roadmap



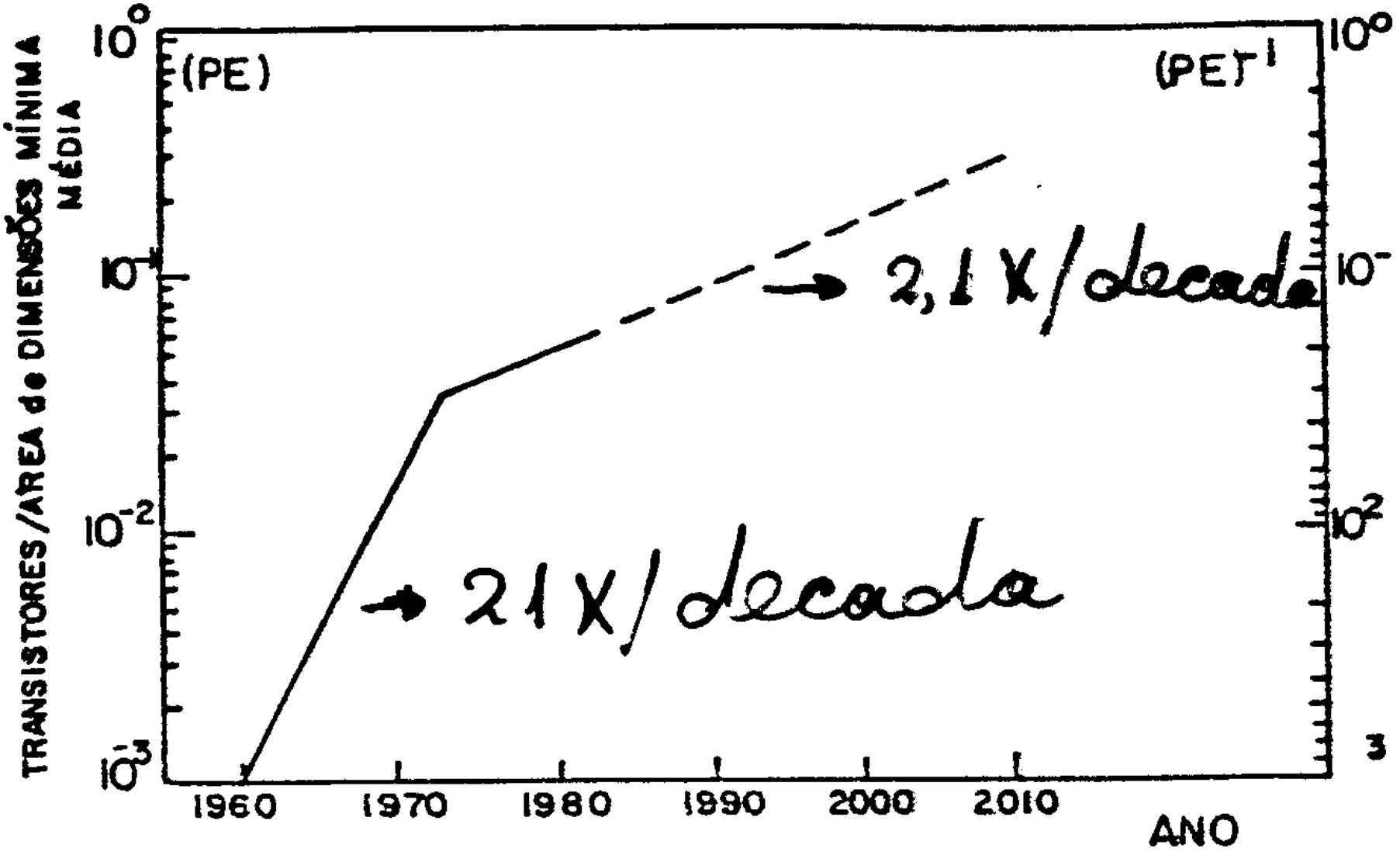

Canal l (µm)
2.0
1.0
0.3
0.2
0.1
0.05
80286
80386
486
pentium
pentium II
Pesquisa
83
86
89
92
95
98
01
04
Ano


20 nm

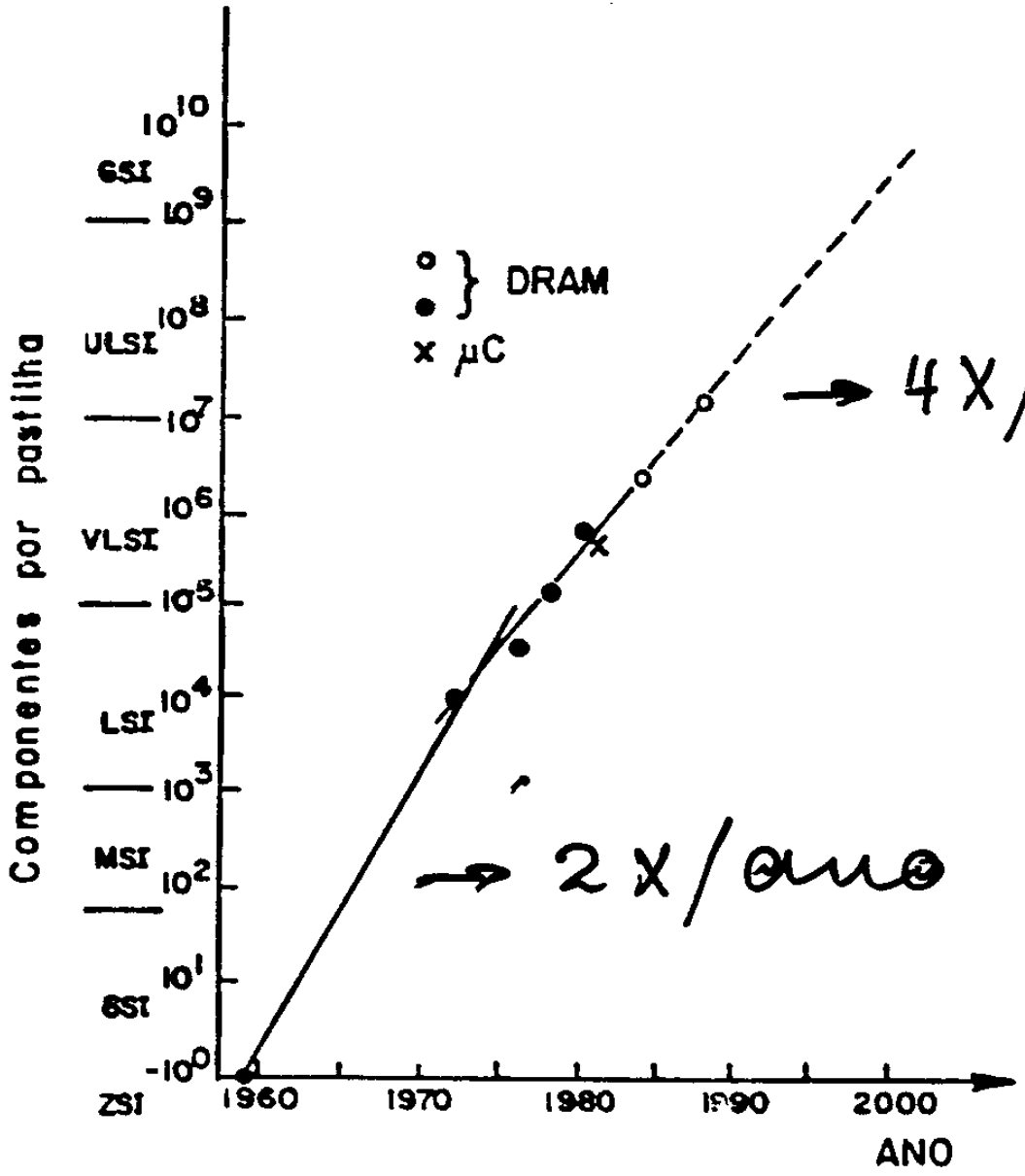
Área de chip



Eficiência de Empacotamento – Inovação

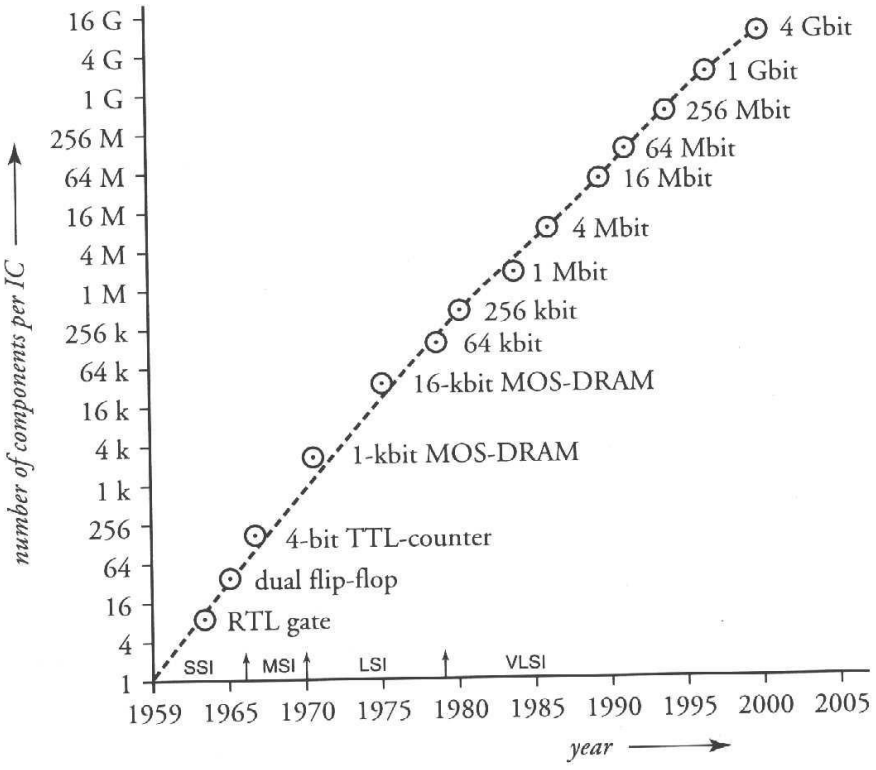


Número dispositivos por chip - Lei Moore

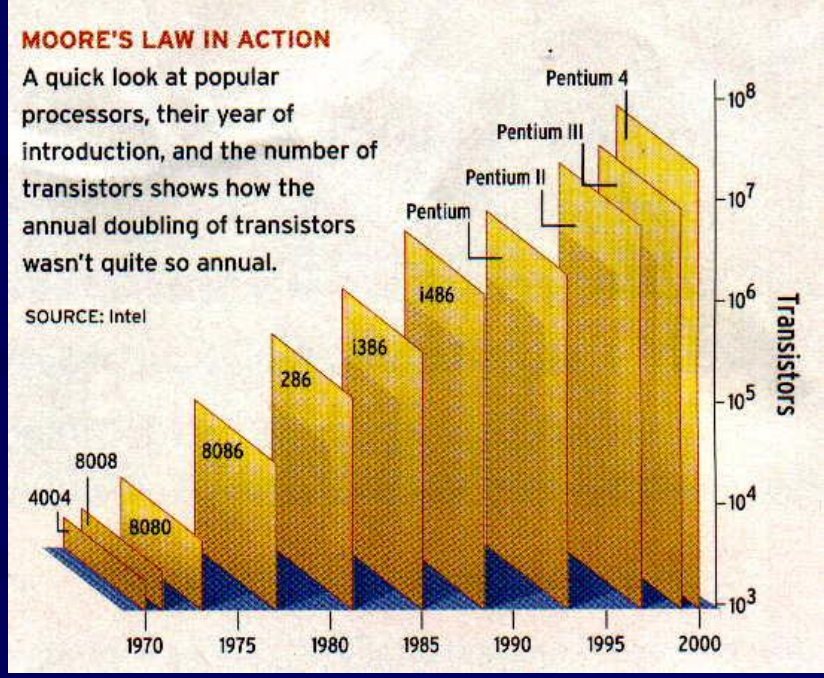


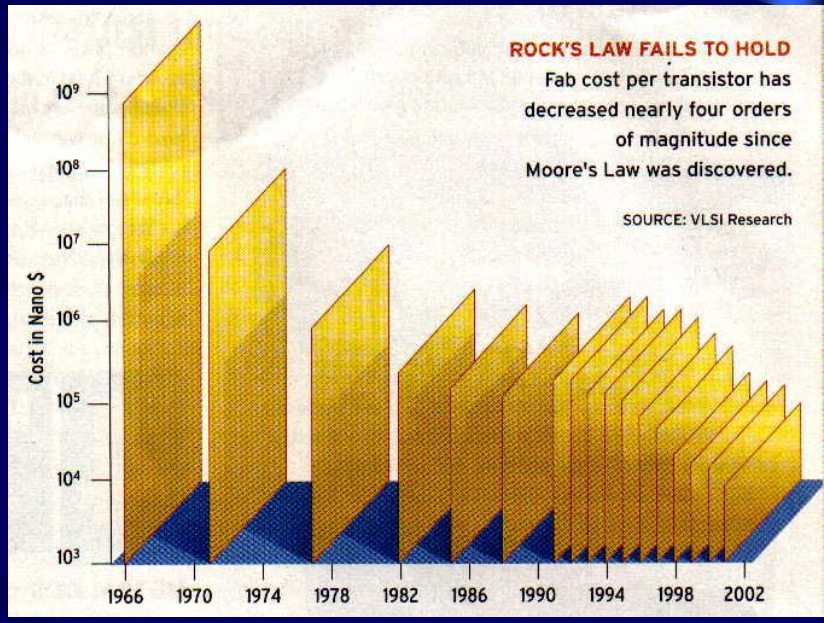
Apresentada em abril, 1965.
Preríodo - taxa:
<1965 - 2x/12 meses
<1975 – 2x/17 meses
<1985 – 2x/22 meses
<1995 – 2x/32 meses
<2003 – 2x/24 meses

Média>1970 – 2x/24 meses
(Intel considera:
média – 2x/18 meses)



(Deep-Submicron CMOS ICs, H. Veendrick)





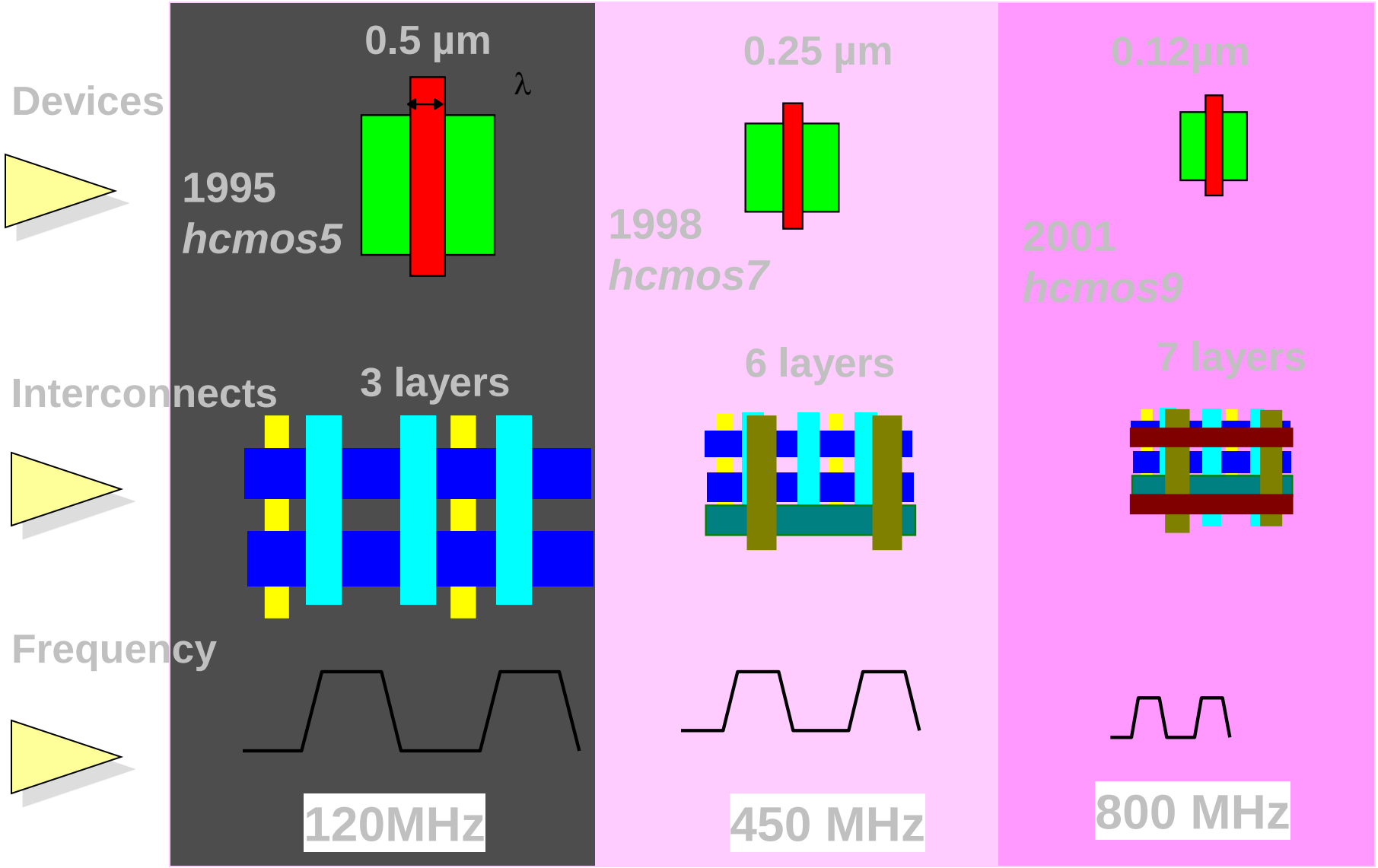
(IEEE Spectrum, Dec. 2003, p.32-33)

1. Roadmap

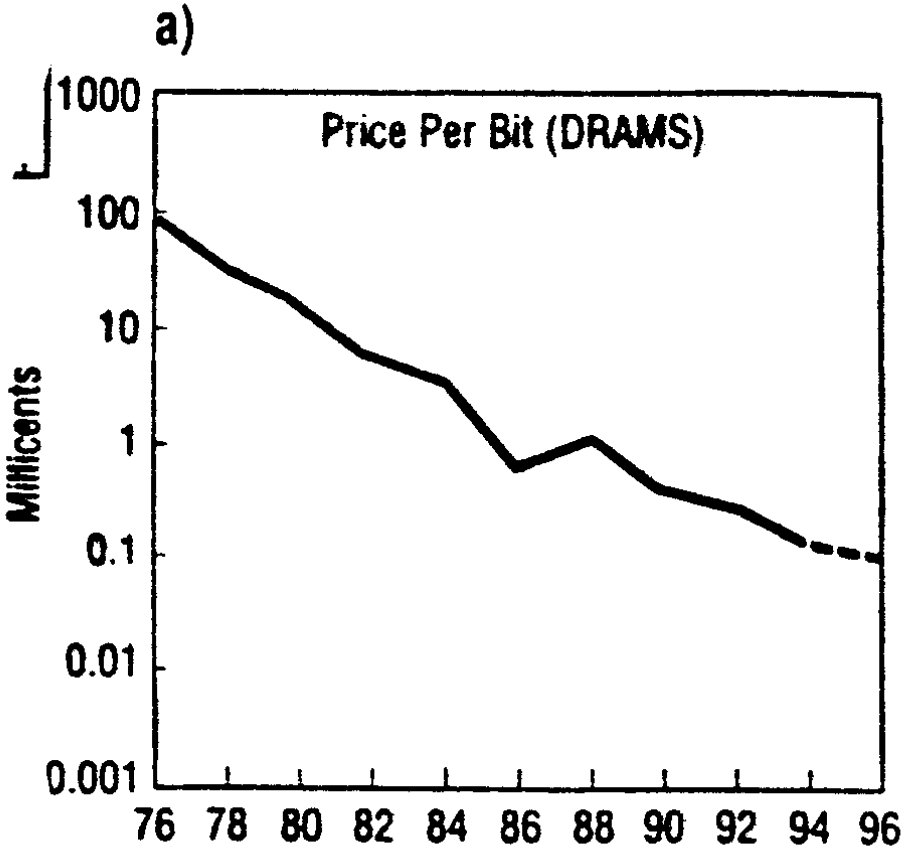
Devices

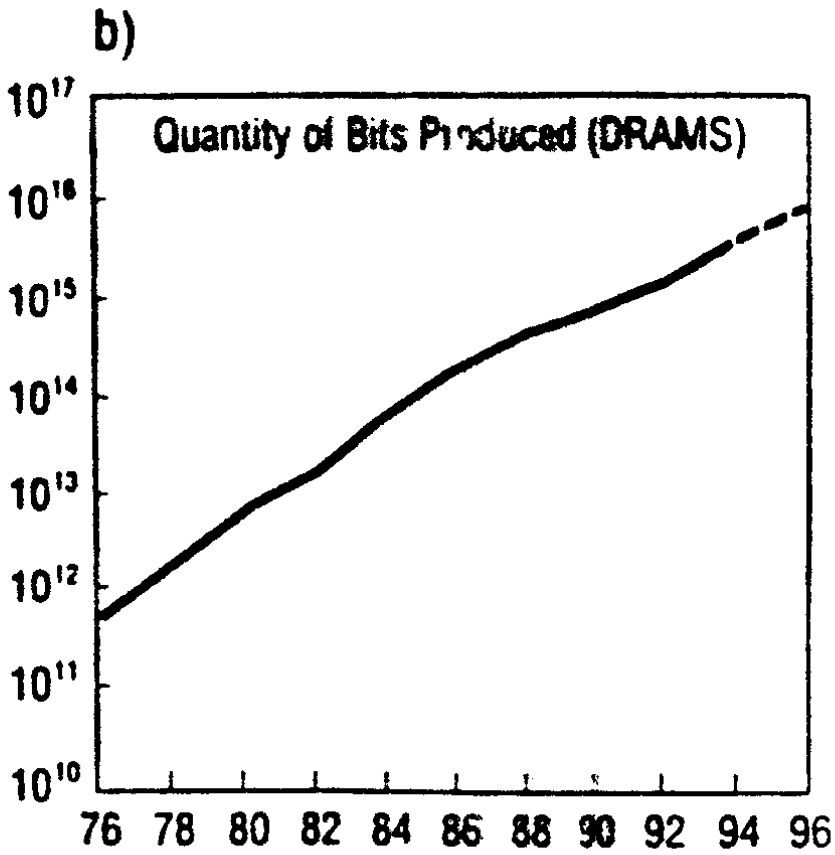
Interconnects

Frequency



- Redução de custo e aumento do no. de bits





- 10^{17} bits ~ 10 x no. grãos ~ no. formigas

Downsizing of the components

1910	1950	1960	1970	2000
Vacuum Tube	Transistor	IC	LSI	ULSI
10 cm	cm	mm	10 μm	100 nm

Downsizing:

Capacitance reduction → Power reduction
Speed increase

High integration → Function increase

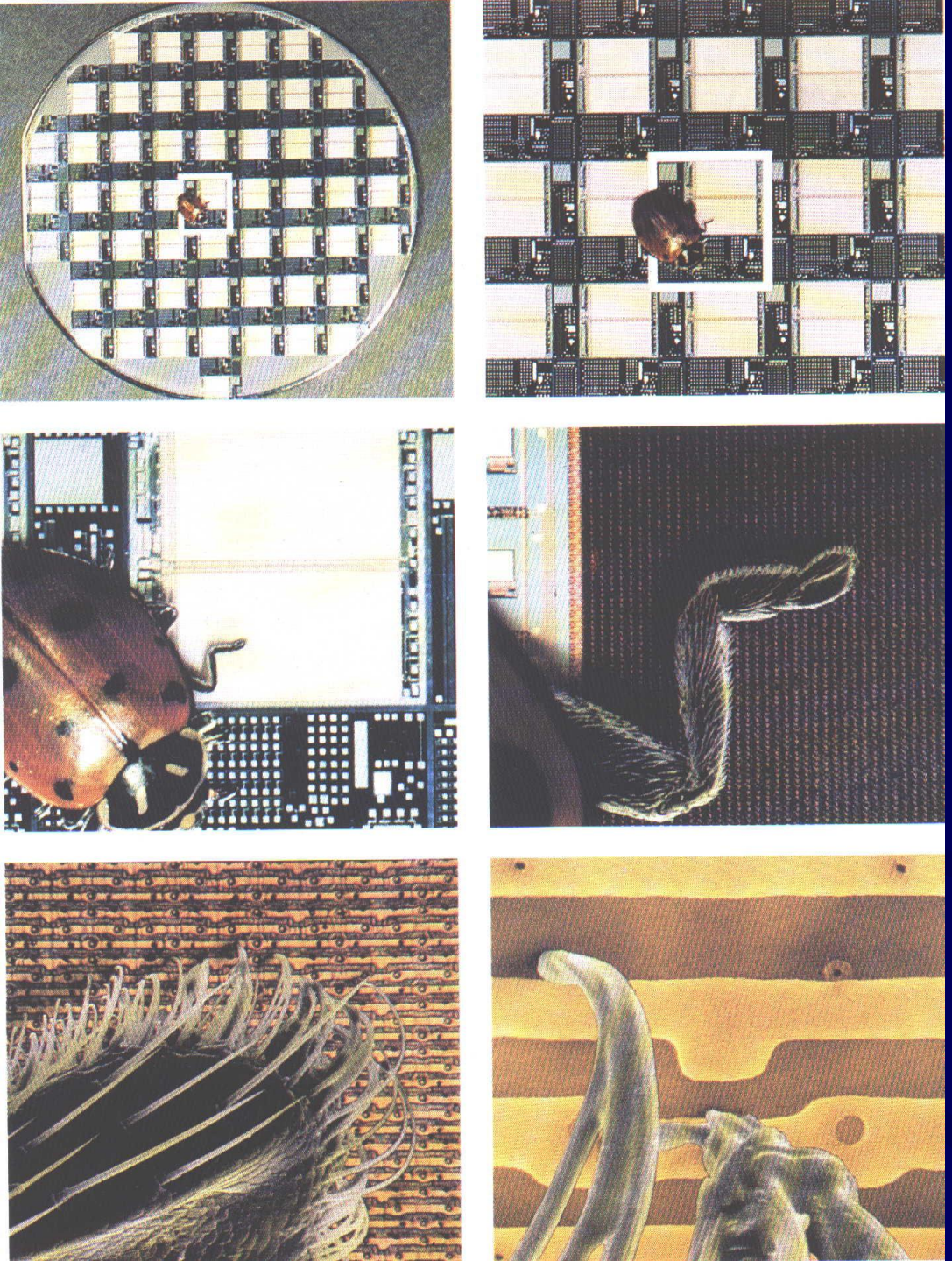
→ Cost reduction per function or speed

(from H. Iwai)

Past and current status of advanced LSI products

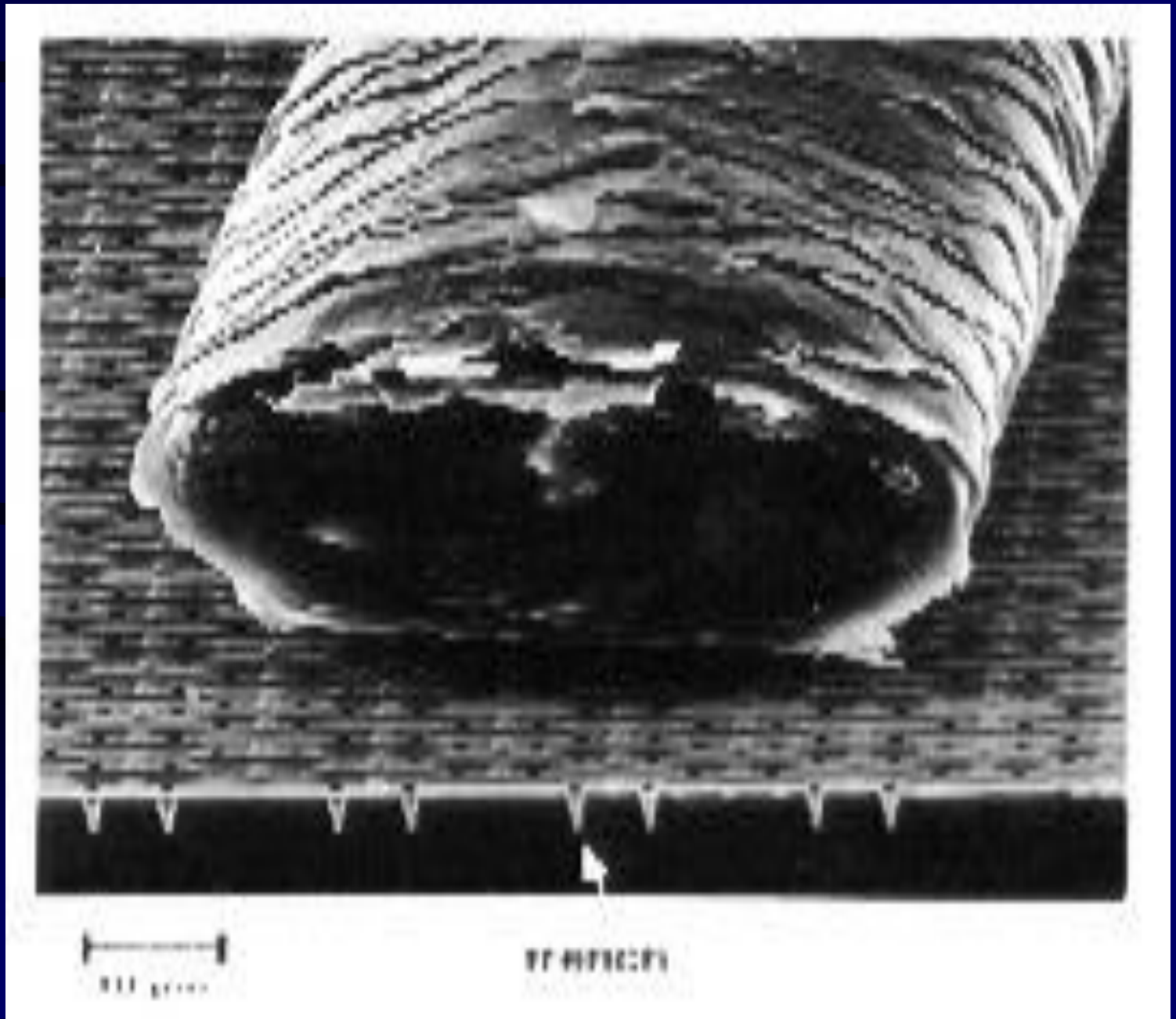
Year	Min/ Lg(μm)	ratio	DRAM	ratio	MPU	ratio
1970/72	10	1	1K	1	750K	1
2001	0.1	1/100	256M	256,000	2.0G	2,667

(from H. Iwai)



TI, Koning&Hartman,
in Deep-Submicron
CMOS ICs, H. Veendrick

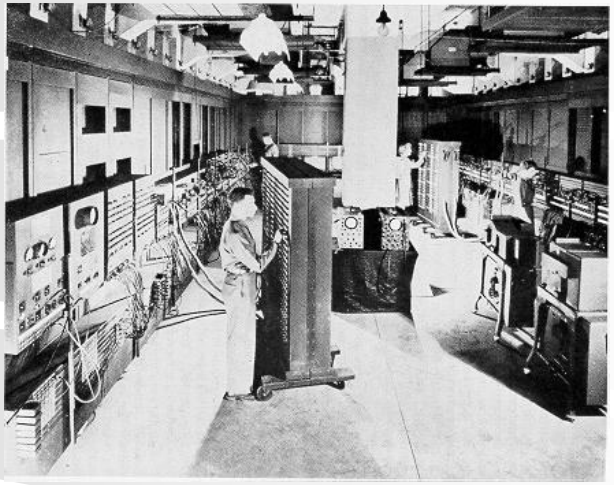
Outras Comparações:



Dados de algumas gerações:

	Eniac (1945)	X	68.040 (1990)	X	Pentium IV (2001)
dispositivos	18k	10^2	1.2M	$2x10^3$	42 M
Volume	200 m^3	10^{-8}	2 cm^3		146 mm^2 (L=0.13µm)
Velocid.	150 IPS	10^5	20 MIPS		2.2 GHz
Consumo	10 kW	10^{-4}	1W		(V_{DD}=1.5V)
Custo	$ 1 M	10^{-3}	$ 1 k		
Confiabilid.	horas	10^3	anos		

The Computer, Then and Now



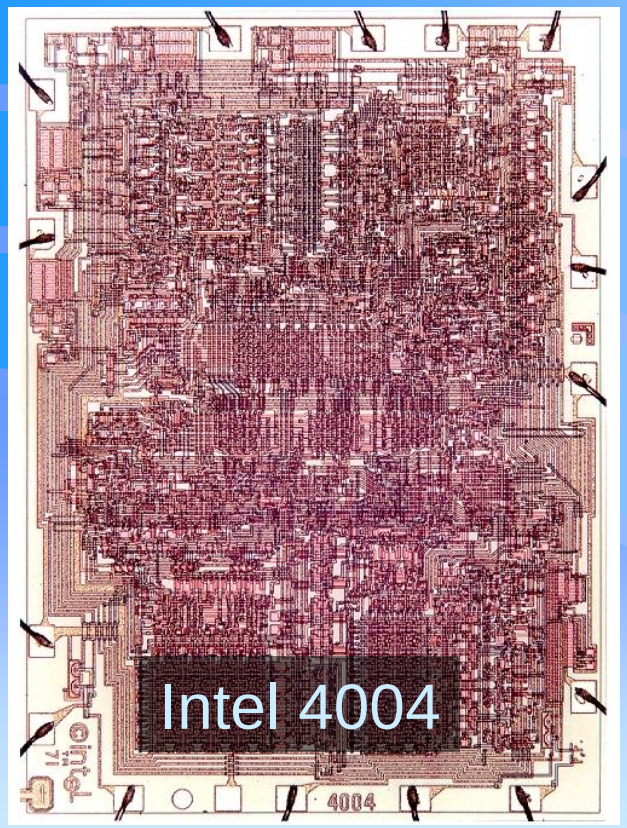
Laptop (2001)		ENIAC (1946)
$2000	~10^{-3}	>$1,000,000
500,000,000 additions/sec	105	5,000 additions/sec
2 kg	~10^{-4}	30,000 kg
< 45 W	~10^{-4}	174,000 W
300,000,000 transistors	~10^{4}	17,468 Tubes

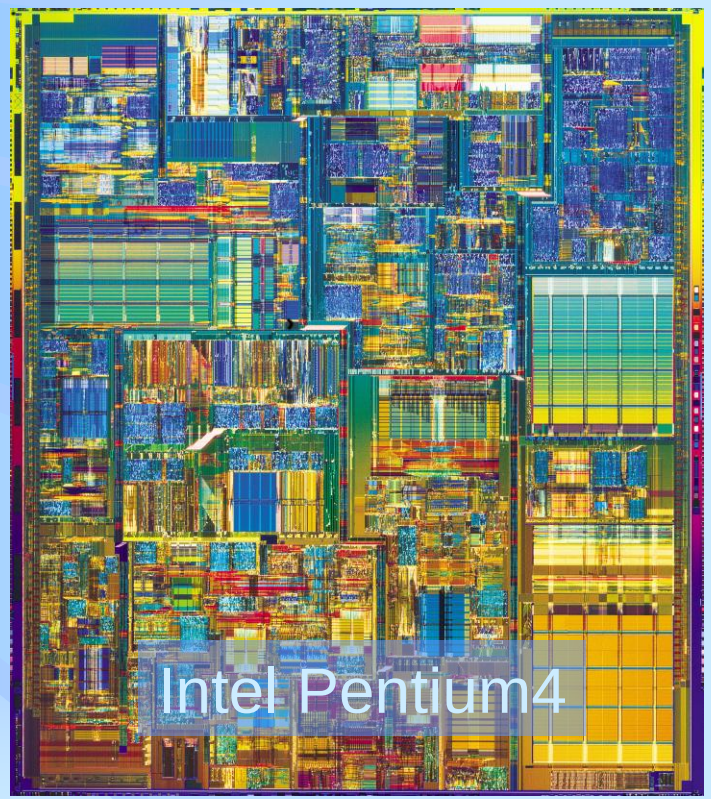
(from M. Green)

Year	1971	2001
Transistors	2,300	42,000,000
Speed (kHz)	108	2,000,000
CD (µm)	10.00	0.13

x 18,000
x 18,000
/ 6000

!!





Aplicando as mesmas escalas ao carro:

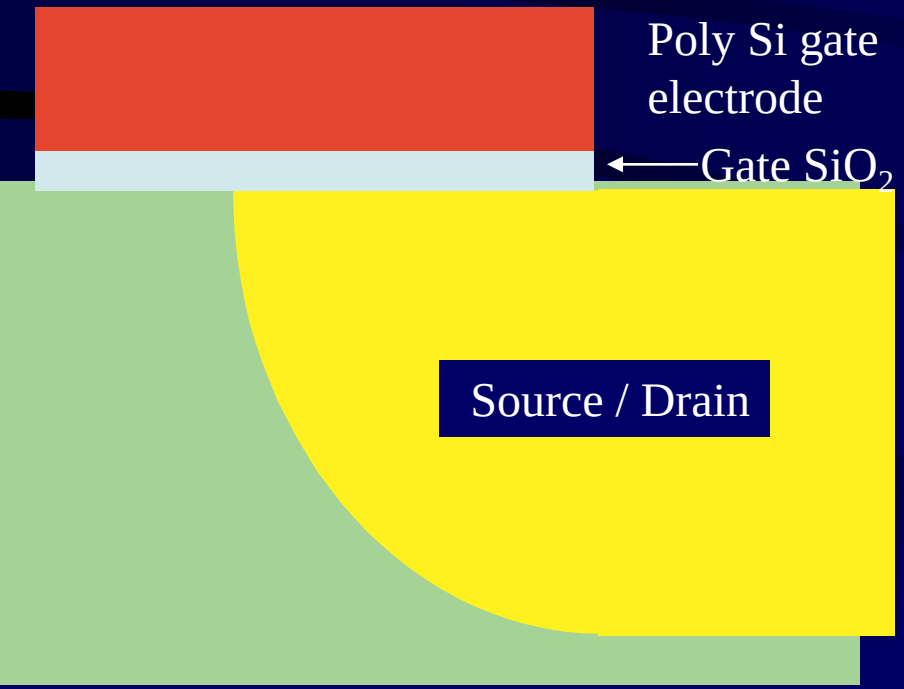
	Padrão	X	Analogia
Velocidade	110 km/h	10^{5}	3000 km/h
Consumo	10 km/l	10^{-4}	10000 km/l
Custo	$ 20 k	10^{-3}	$ 20
Confiabilidade	1 ano	10^{3}	1000 anos
Peso	1 t	10^{-8}	10 mg

Evolução de Microeletrônica, Regras de Escalamento e Limites

3. Materiais Usados em CI's de Si

6 μm NMOS LSI in 1974

magnification

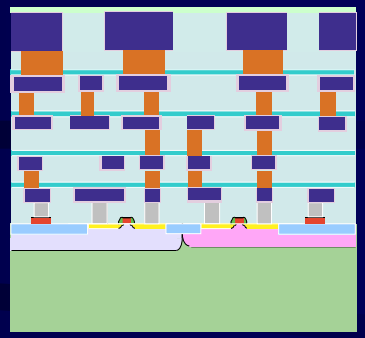


Layers	Materials
Si substrate	Si, SiO_2
Field oxide	BPSG
Gate oxide	PSG
Poly Si gate electrode	Al
Source/Drain diffusion	Atoms
Interlayer dielectrics	Si, O, Al, P, B
Aluminum interconnects	
Passivation	(H, N, Cl)

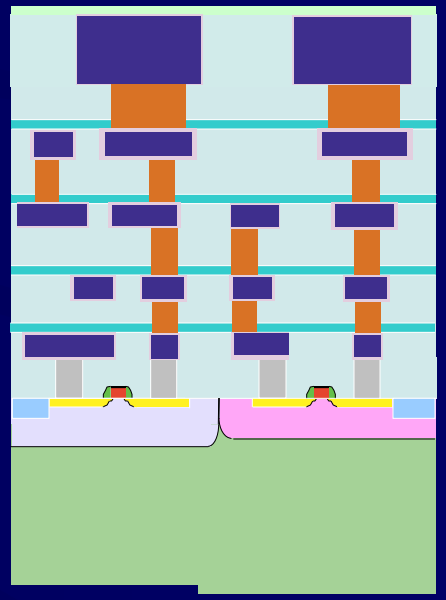
(from H. Iwai)

0.1 μm CMOS LSI in 2001

Large number of layers,
Many kinds of
materials and atoms



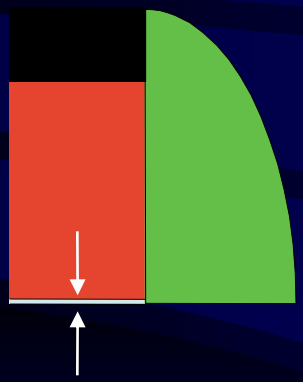
magnification



W via plug

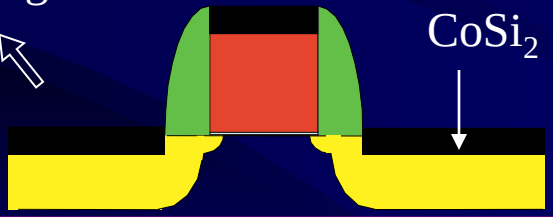
Low k ILD

W contact plug



Ultra-thin gate SiO_2

magnification



$CoSi_2$

magnification

(from H. Iwai)

At 130 nm node: ~ 20 materials

At 65 nm node: ~ 34 materials (SOI, SiGe, ultalow-k, HfO_2, SiON, ALD barrier and seed layers, etc) – S.I. Vol.26, no.12, p.36 (Nov.03).

Efeitos sobre a Capacitância de Porta

- Classicamente: $Q_c = C_{ox}\left(V_{GS} - V_T\right)$ $\quad C_{ox} = \dfrac{\varepsilon_{ox}}{t_{ox}}$
- Correções:

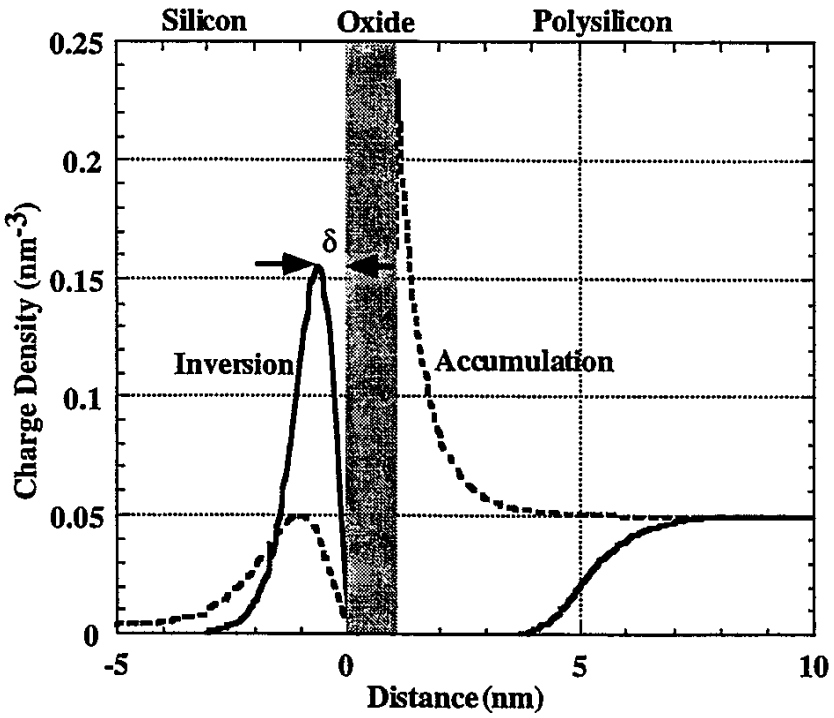
  efeito da espessura do canal

  depleção da porta de Si-poli

$$\frac{1}{C_{ef}} = \frac{1}{C_{ox}} + \frac{1}{C_c} + \frac{1}{C_{poli}}$$

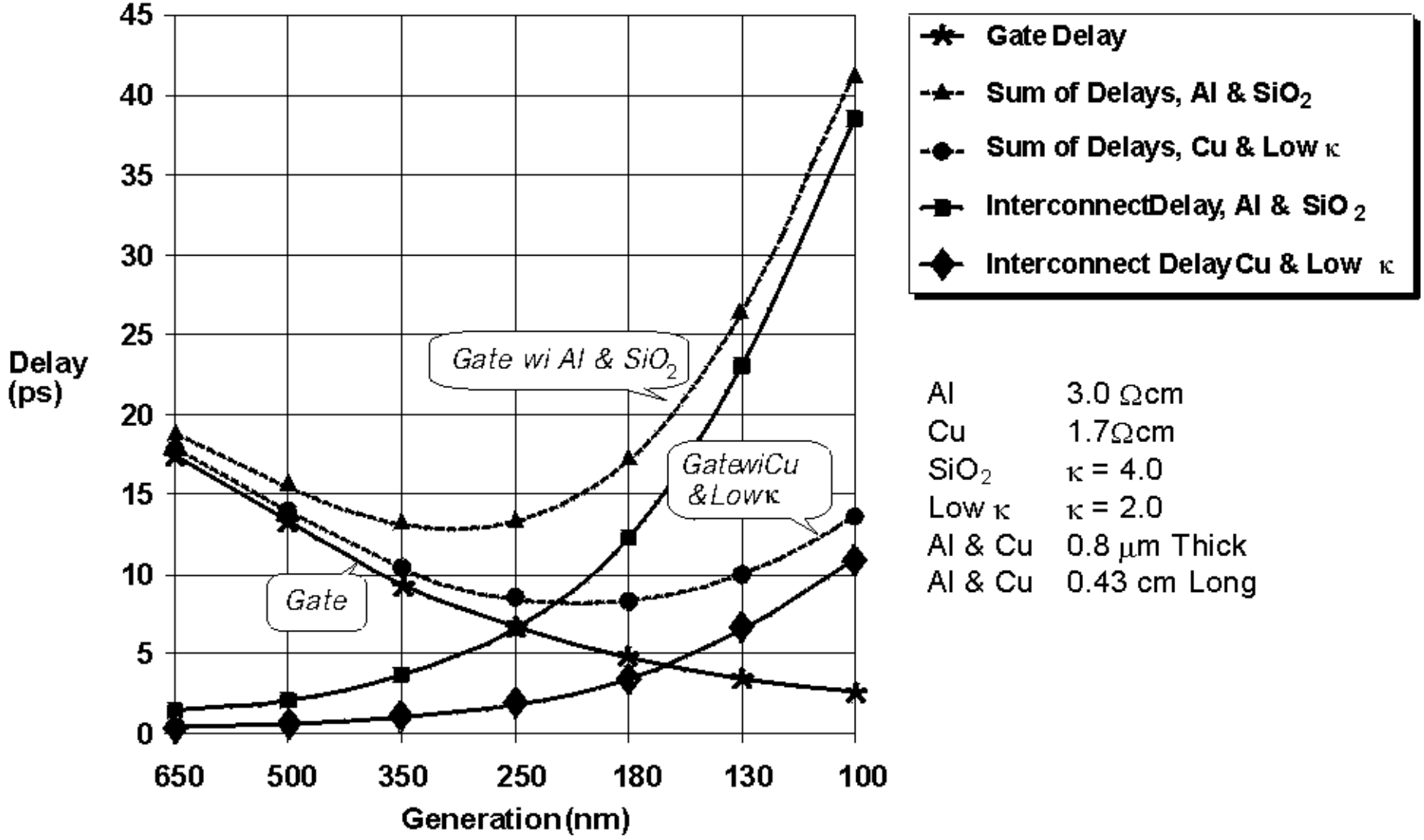
$$C_c = \frac{\varepsilon_{Si}}{t_c} \qquad C_{poli} = \frac{\varepsilon_{Si}}{t_{depl}}$$

Usar porta de metal!

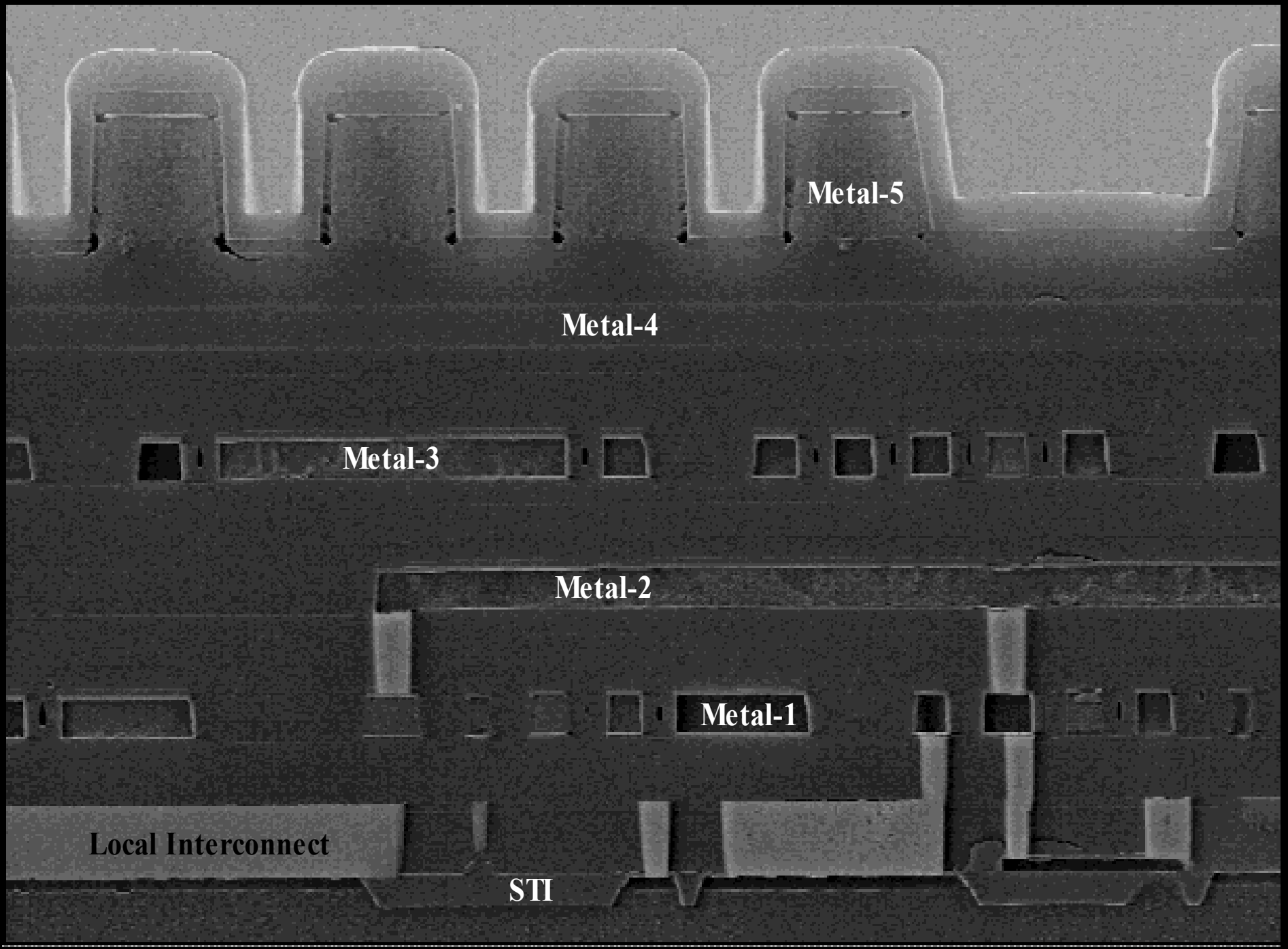


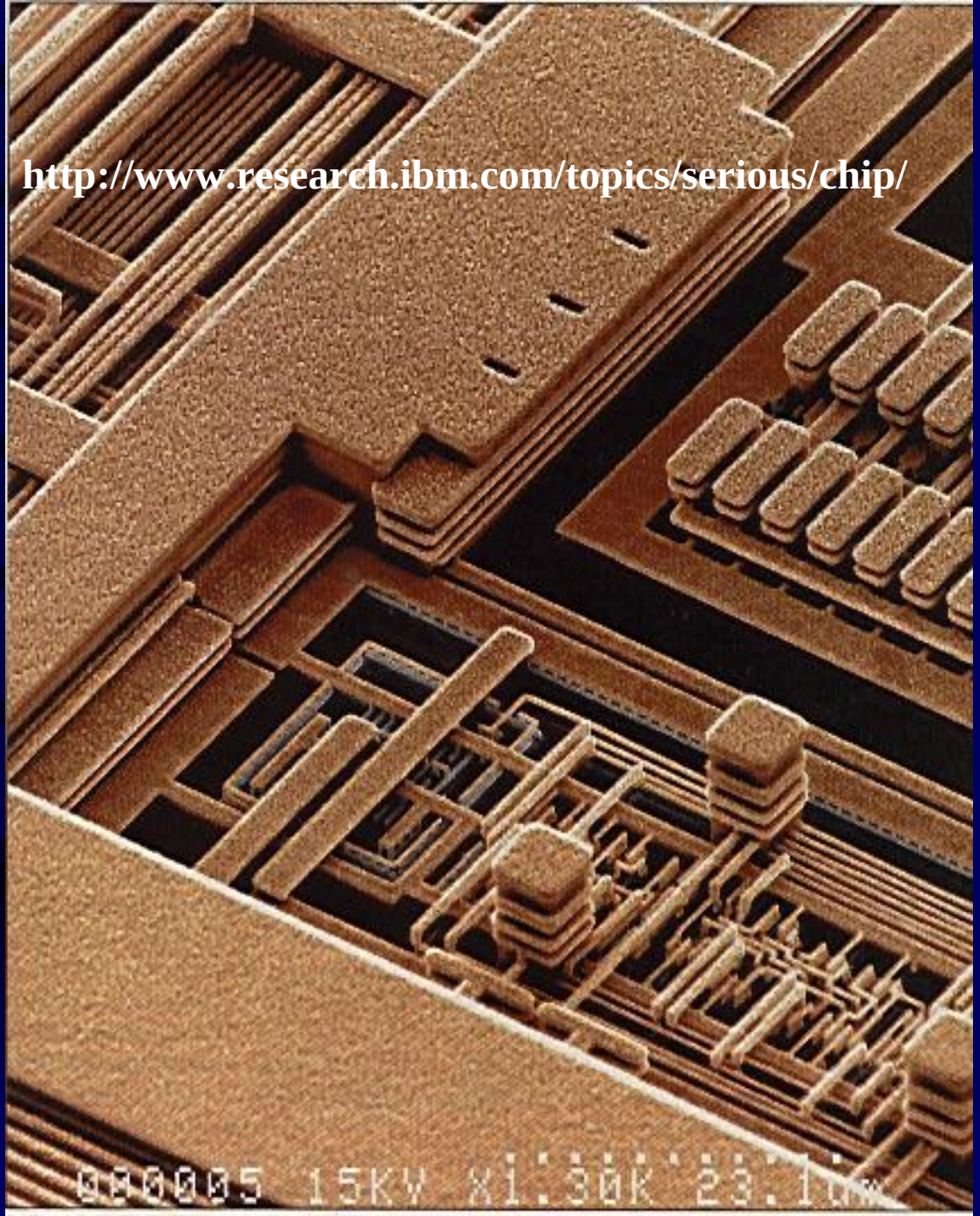
- Tunelamento pelo óxido: usar dielétrico de alto k!

Simulações de atraso de porta e de linhas



Al	3.0 Ωcm
Cu	1.7Ωcm
SiO_2	κ = 4.0
Low κ	κ = 2.0
Al & Cu	0.8 μm Thick
Al & Cu	0.43 cm Long


Metal-5
Metal-4
Metal-3
Metal-2
Metal-1
Local Interconnect
STI



[1] IBM Corp.'s new CMOS 7S process for manufacturing ICs uses copper for its six levels of

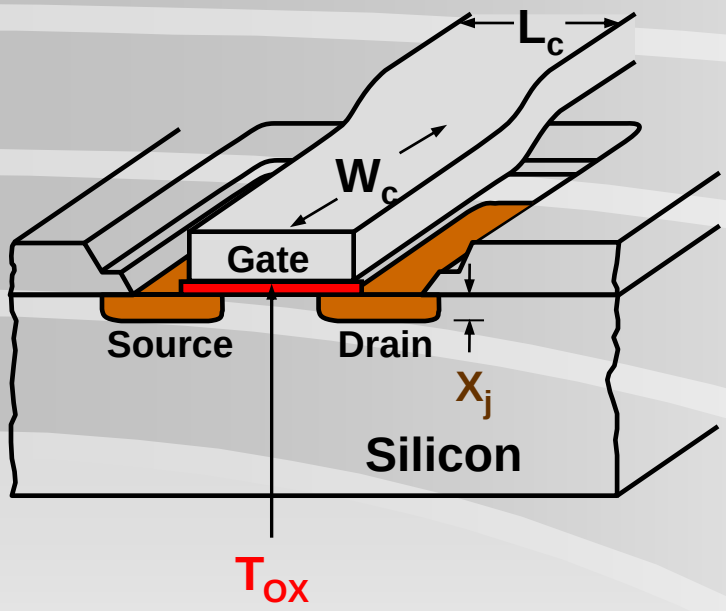
Evolução de Microeletrônica, Regras de Escalamento e Limites

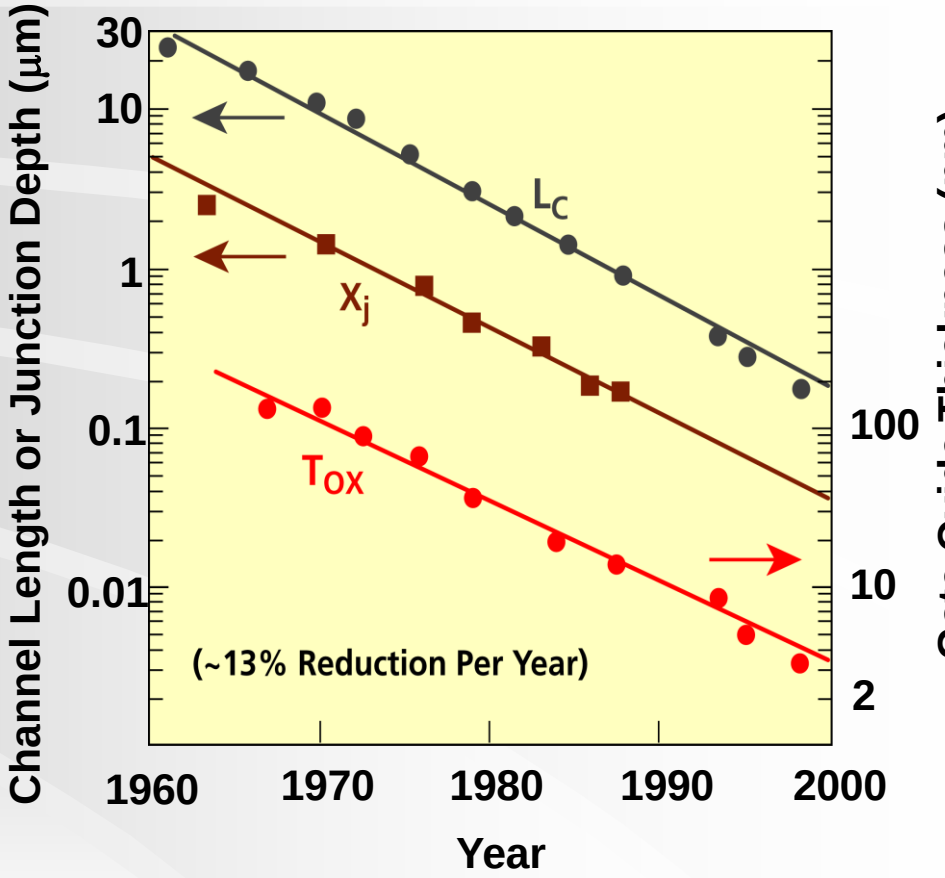
4. ITRS (International Technology Roadmap of Semiconductors) e Tendências

Previsão: Roadmap SIA 1997

Dado \ Ano	1997	1999	2001	2003	2006	2009	2012
$L_{MIN.}$(nm)	250	180	150	130	100	70	50
DRAM (bits)	256M	1G	-	4G	16G	64G	256G
Área chip DRAM (mm^2)	280	400	480	560	790	1120	1580
Diâmetro / lâmina (mm)	200	300	300	300	300	450	450
Níveis de metal (lógica)	6	6-7	7	7	7-8	8-9	9
Compr. metal (lógica) (m)	820	1480	2160	2840	5140	10000	24000
V_{DD}(V)	2.5	1.8	1.5	1.5	1.2	0.9	0.6
V_T(V)	0.45	0.40	0.35	0.30	0.25	0.20	0.15
F_{MAX} de relógio (MHz)	750	1250	1500	2100	3500	6000	10000
Número máscaras	22	23	23	24	25	26	28
Espess. Óxido	6.5	5.0	4.5	4.0	3.5	2.7	2.0
Defeitos (m^{-2})***	2080	1455	1310	1040	735	520	370
Custo/bit DRAM inicial (μc)	120	60	30	15	5.3	1.9	0.66

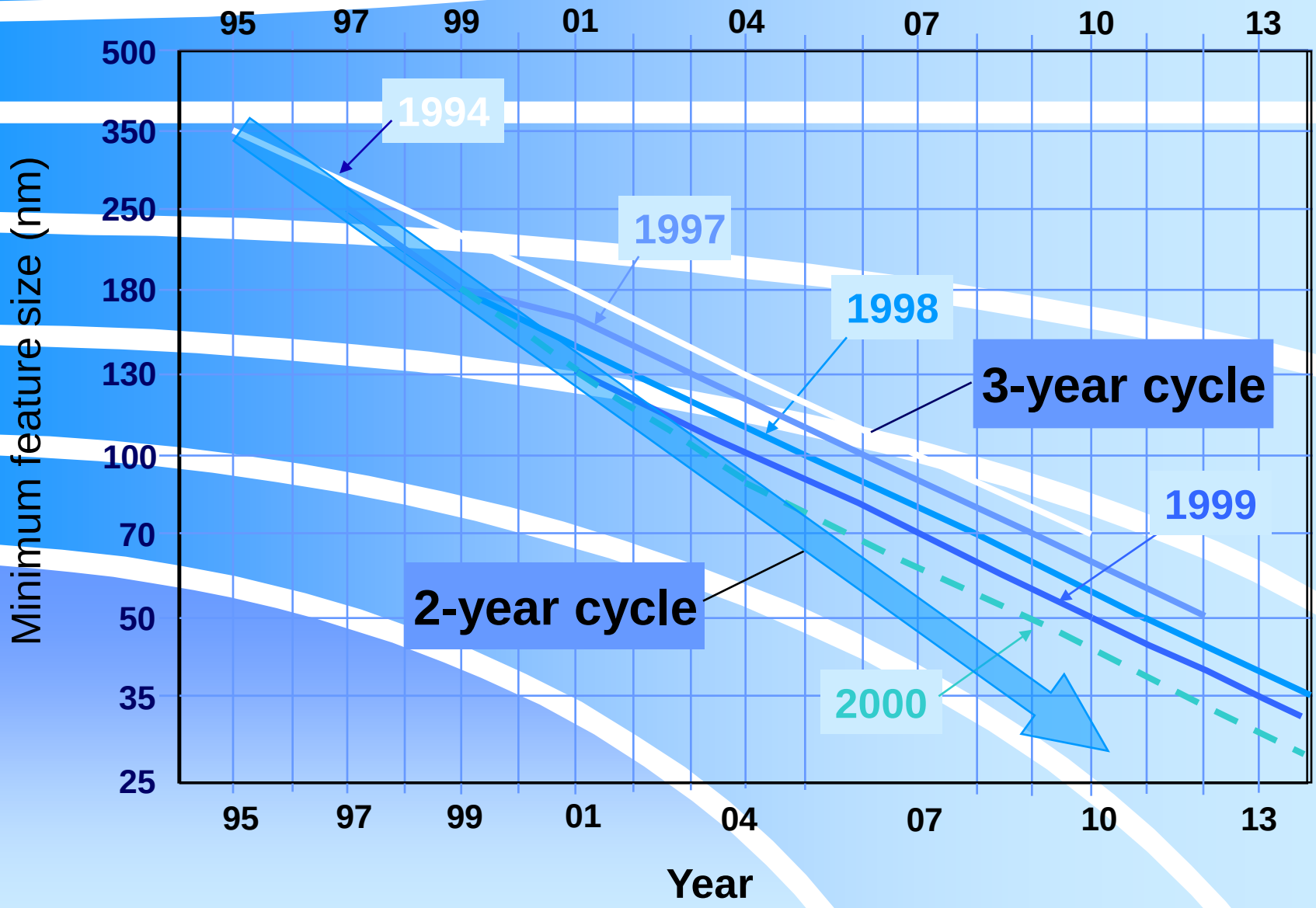
Scaling of MOSFET Dimensions





(from M. Green)

Acceleration ITRS roadmap

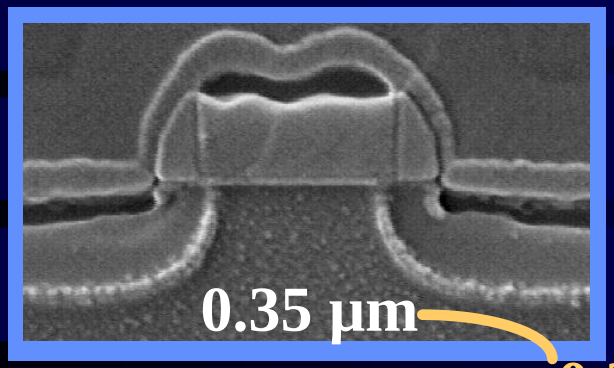


ITRS2001 – dimensões em nm

Ano	04	07	10	13	16	19	22	25
Nó tecnológico	90	65	45	32	22	15	10	7
Printed Gate	53	35	25	18	13	9	6	4
Physical Gate	37	25	18	13	9	6	4	3

- Quais as forças propulsoras para tal evolução?
  - Maior densidade integração ⇒ economia
  - Menor consumo de energia ⇒ desempenho
  - Maior velocidade de operação ⇒ desempenho
  - Menor no. de chips / sistema ⇒ economia
- Uma nova geração / 2 a 3 anos:
  - 2x densidade de circuitos lógicos
  - Aumento de 40% em desempenho
  - 4x capacidade de memórias

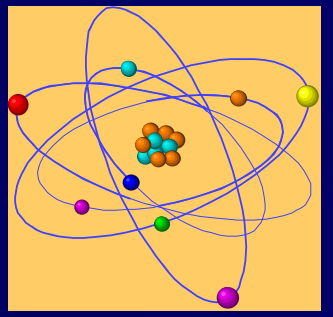
Ultra-Large-Scale To Giga-Scale Integration



0.25 µm

0.18 µm

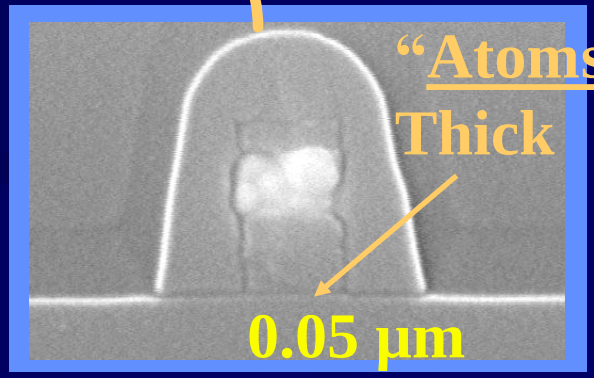
0.13 µm



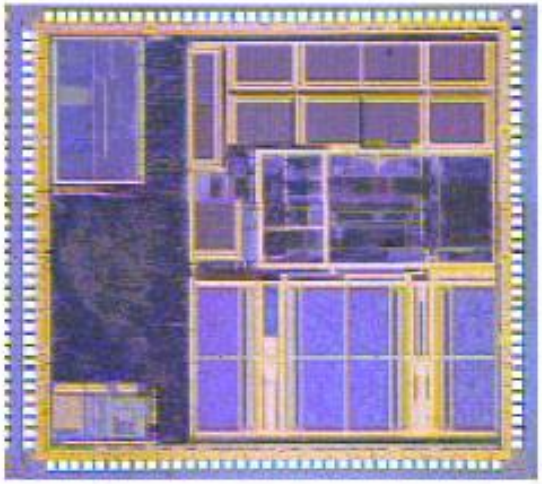
Higher Density

Higher Performance
More Functionality

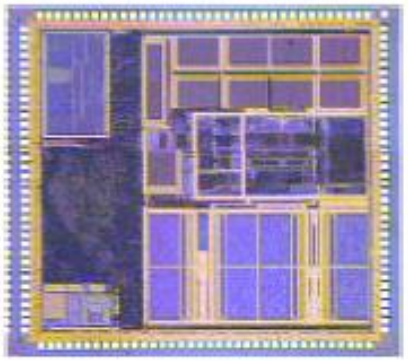
Lower Cost
per Function



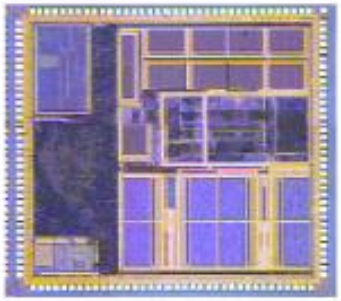
Scaling → "Technology Entitlement"



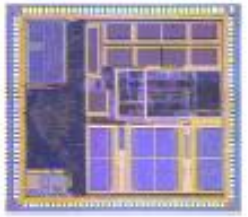
500-nm
80.7 mm^2



350-nm
46.6 mm^2



250-nm
19.2 mm^2



180-nm
10.7 mm^2

Die Per Wafer:

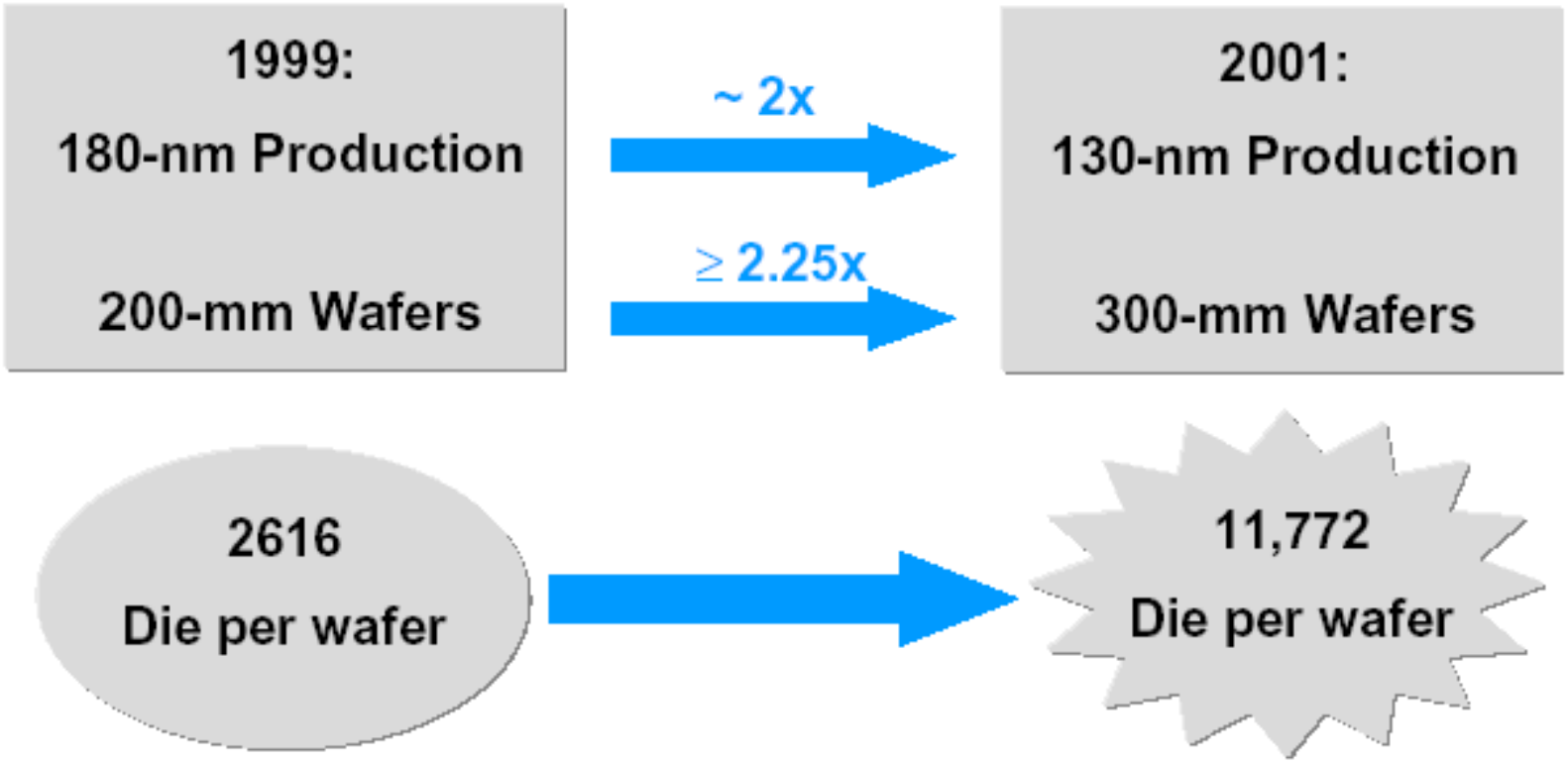
310 → 558 → 1435 → 2616

8.4x increase in DPW

RRD

Texas Instruments

CMOS Scaling × Wafer Scaling = Still More Die per Wafer !

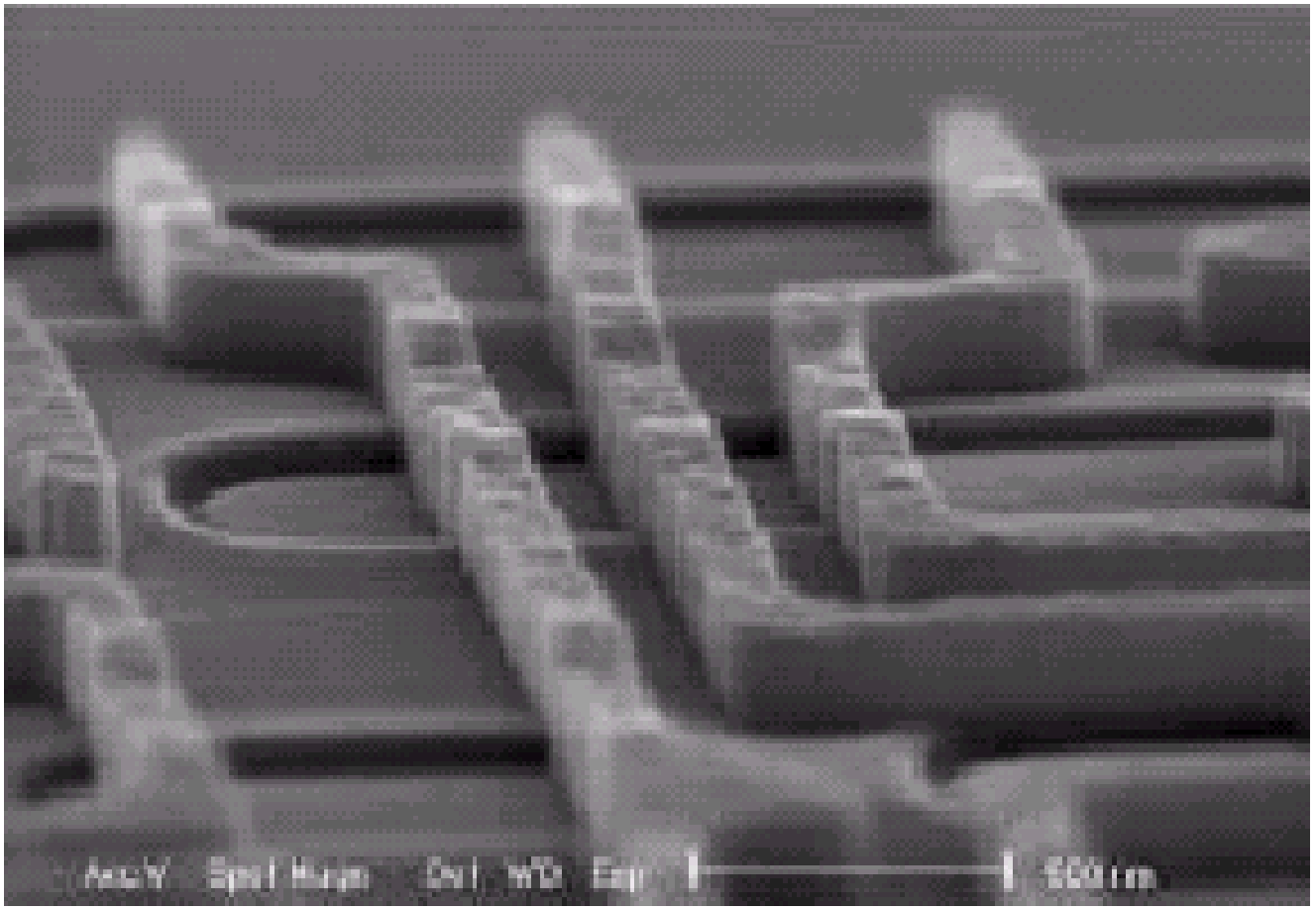


Another 4.5x increase in DPW
from CMOS scaling plus 300-mm
in only 2 years

RRD

Texas Instruments

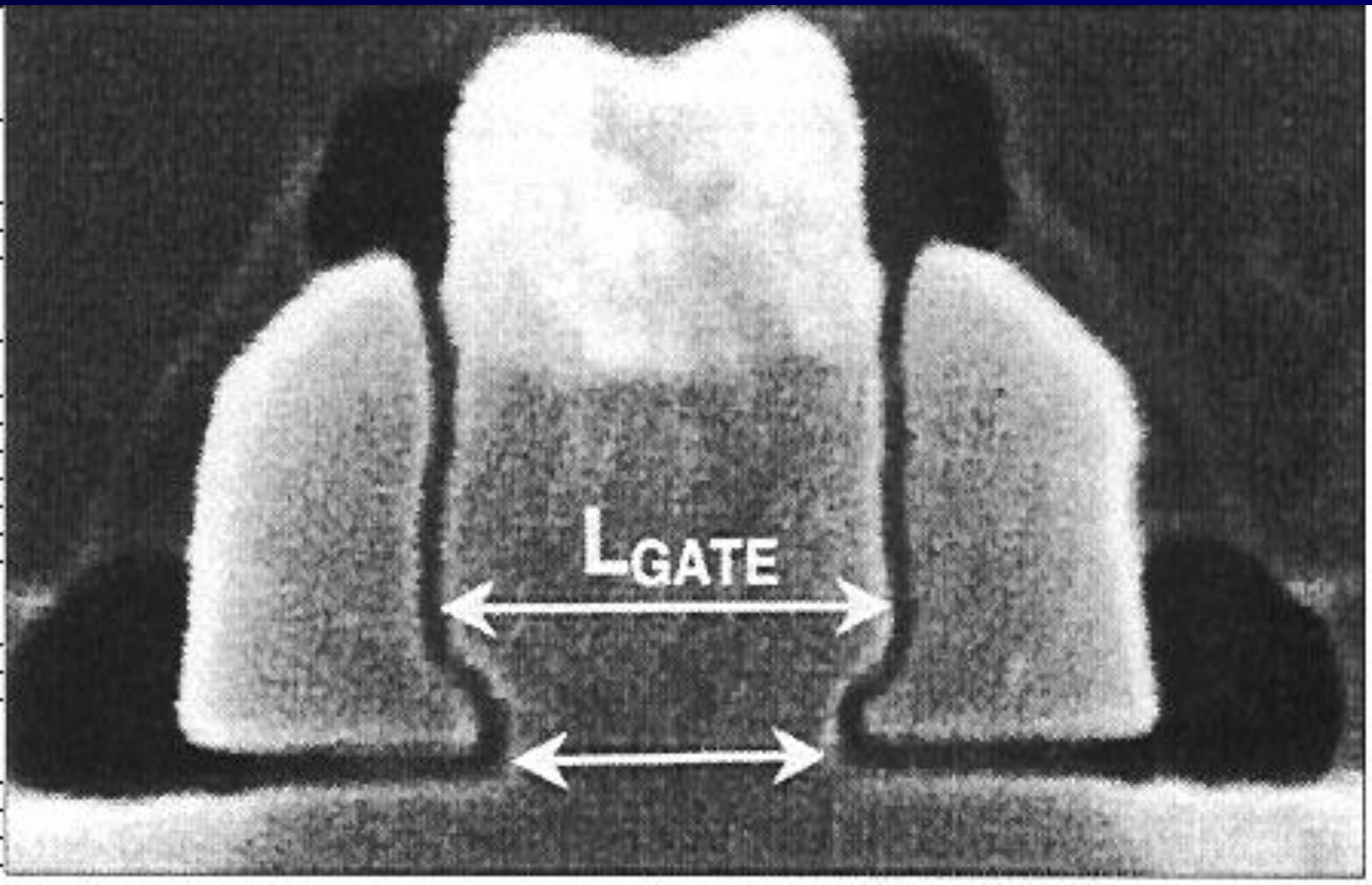
193 nm patterning

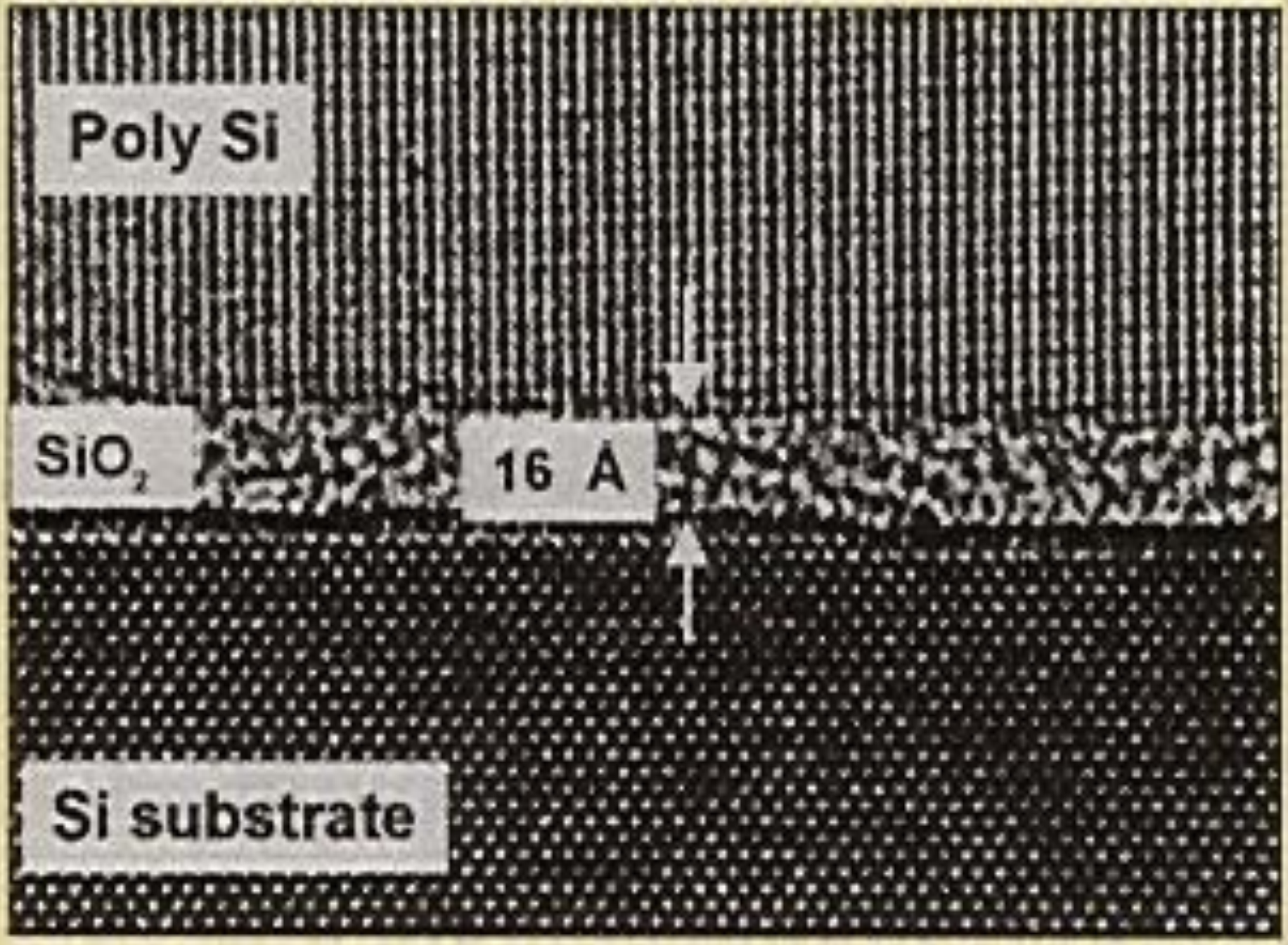


0.13 μm lines and spaces on STI after gate etch printed with binary 193 nm lithography

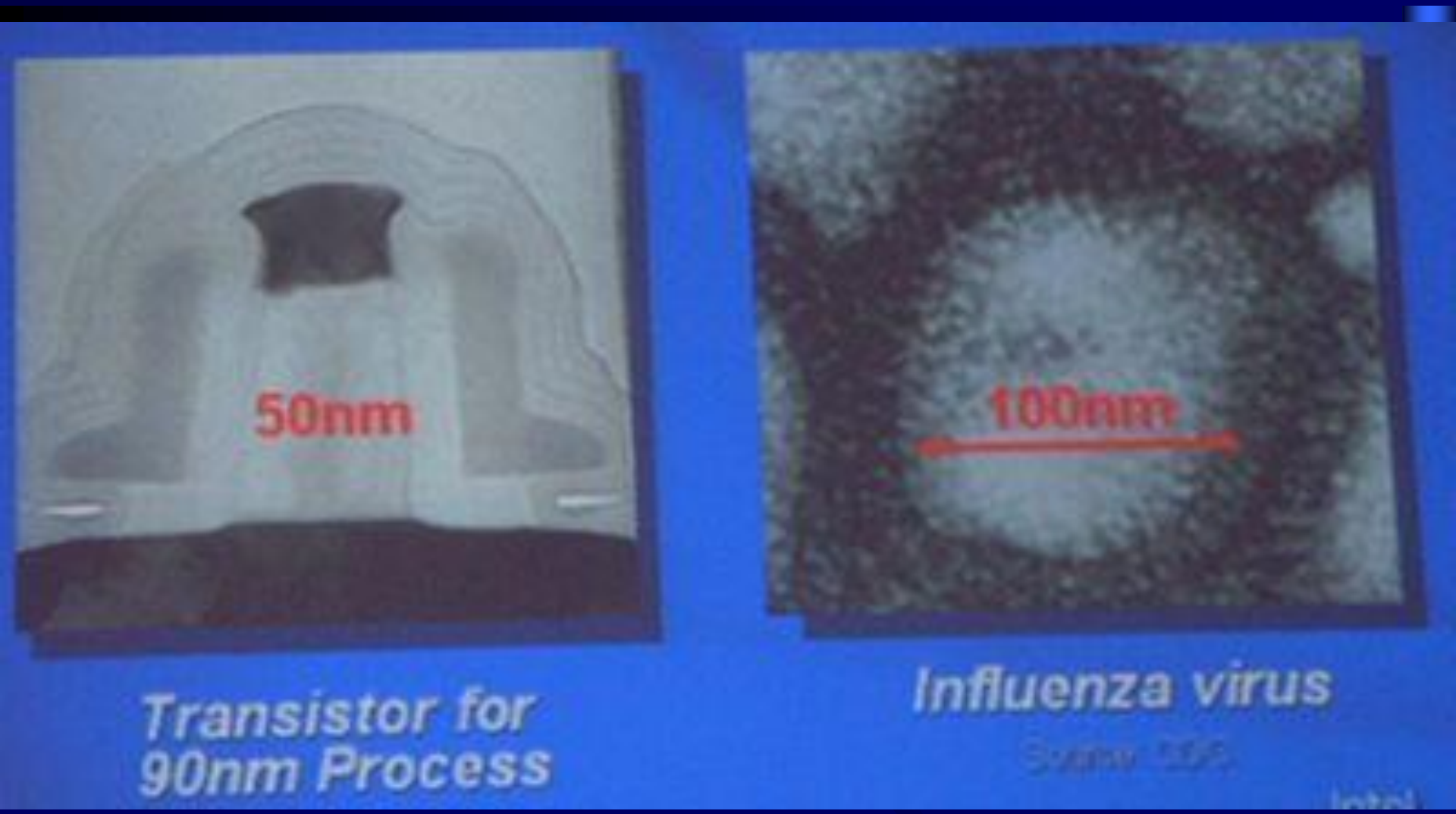
(from G. Badenes, IMEC, 2000)

L = 100 nm

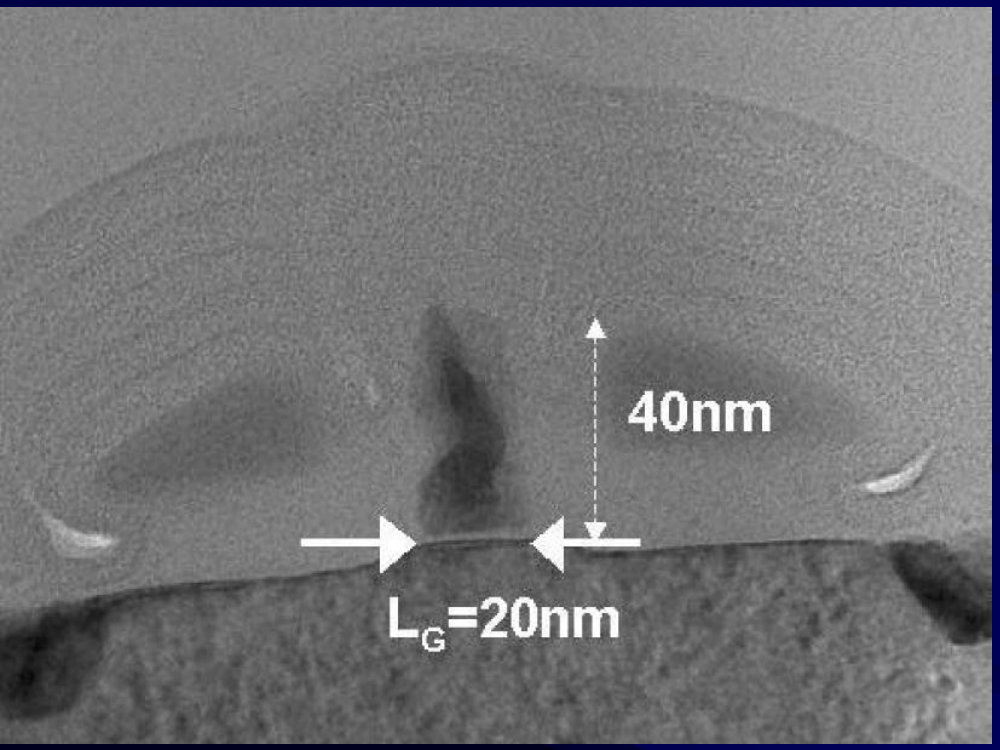


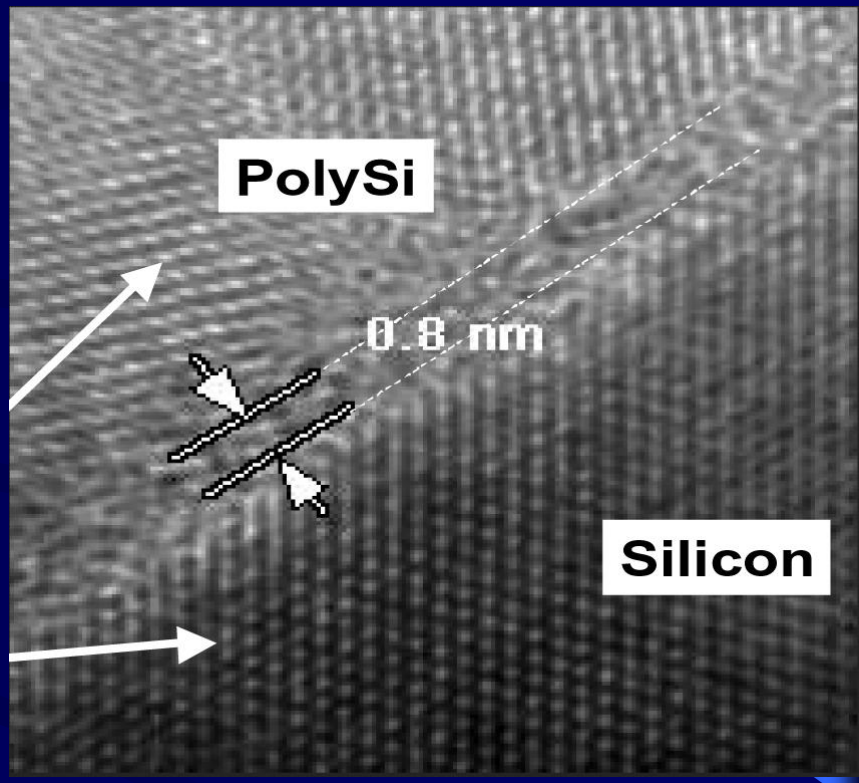

Poly Si
SiO2
16 Å
Si substrate

Transistor processo Intel 90 nm vs. Virus de Grípe.



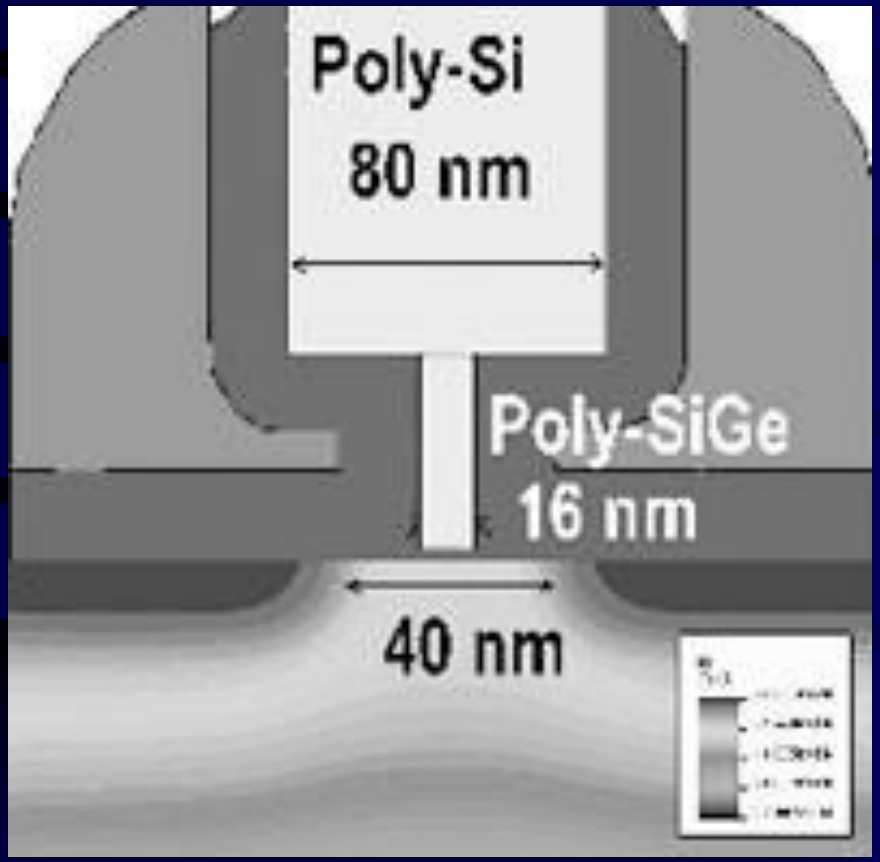
20 nm Gate Length Transistor

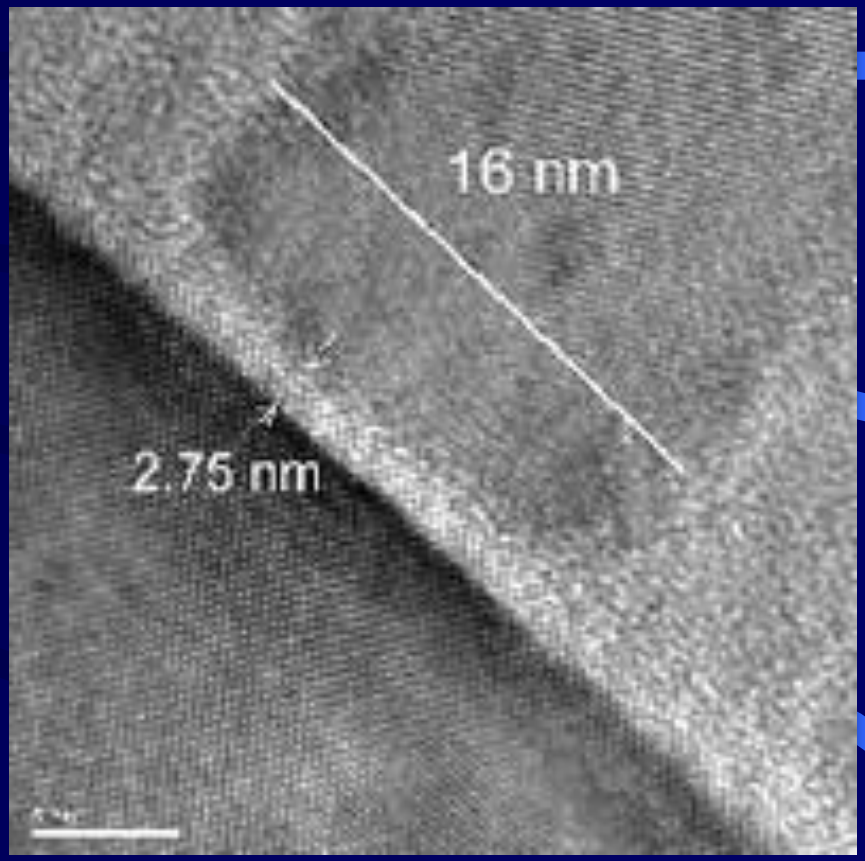




R. Chau, Proc. Silicon Nanoelectronics Workshop, pp. 2 - 3 (2001)
http://www.intel.com/research/silicon/micron.htm

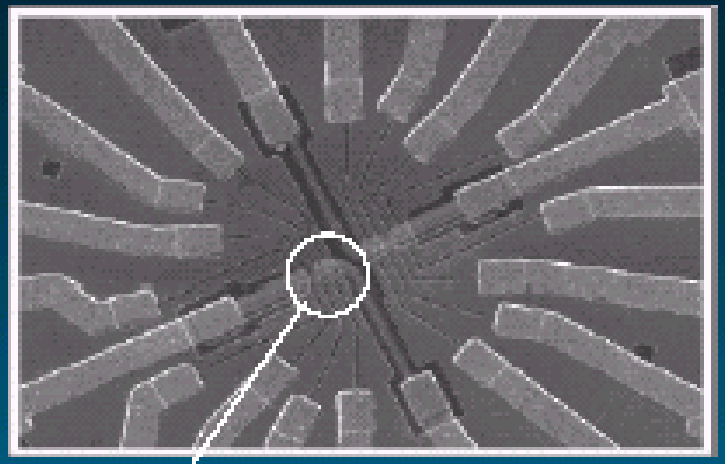
16 nm Gate Length Transistor

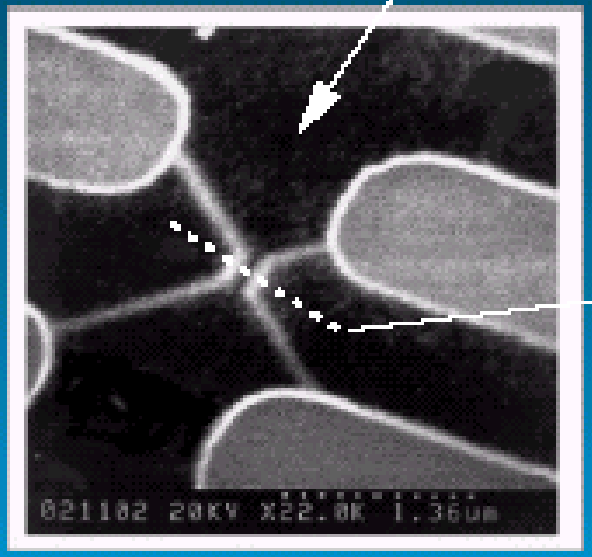




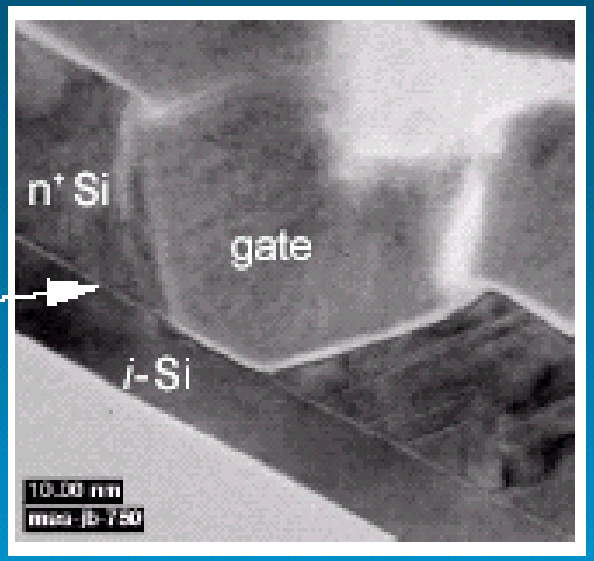
STMicroelectronics, Semiconductor International de Nov/2001.

IBM – 10 nm MOSFET



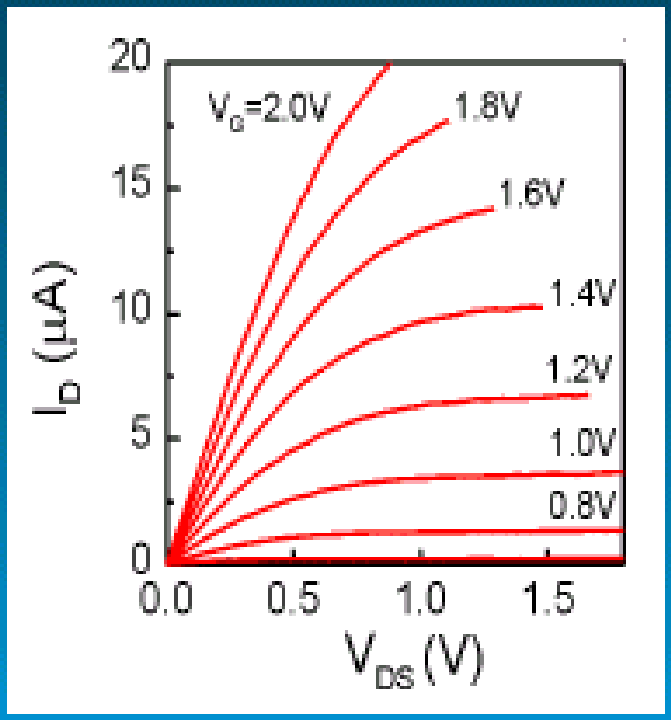


SEM Image
Top View of a MOSFET



TEM Image
Cross Section of a V-Groove

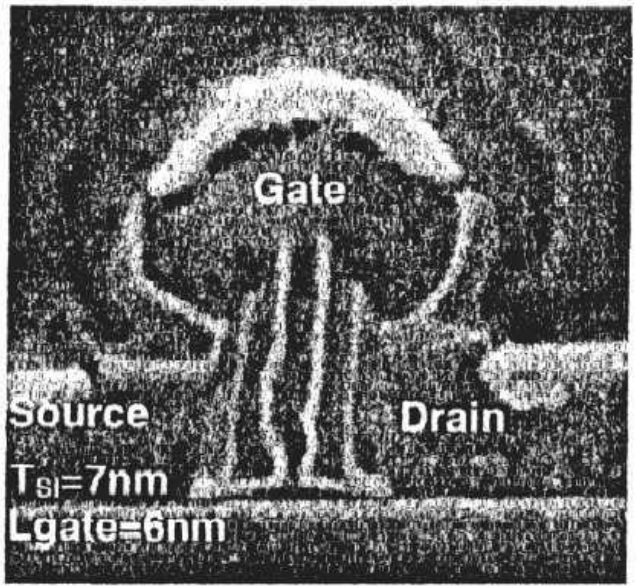
I_D-V_{DS} Characteristics



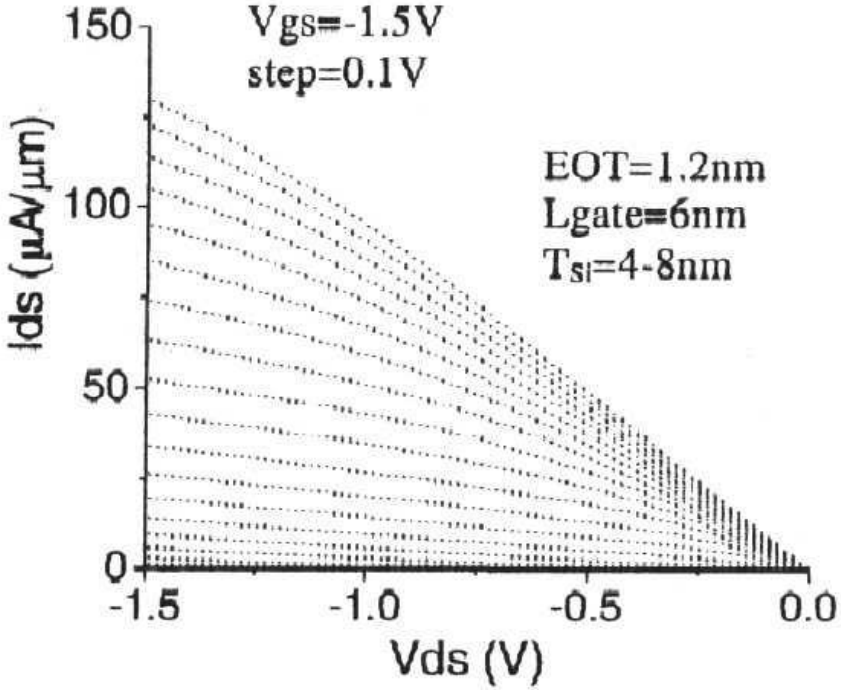
ITRS2001 – dimensões em nm

Ano	04	07	10	13	16	19	22	25
Nó tecnológico	90	65	45	32	22	15	10	7
Printed Gate	53	35	25	18	13	9	6	4
Physical Gate	37	25	18	13	9	6	4	3

Transistor pMOS, L = 6 nm, (IBM-2004)



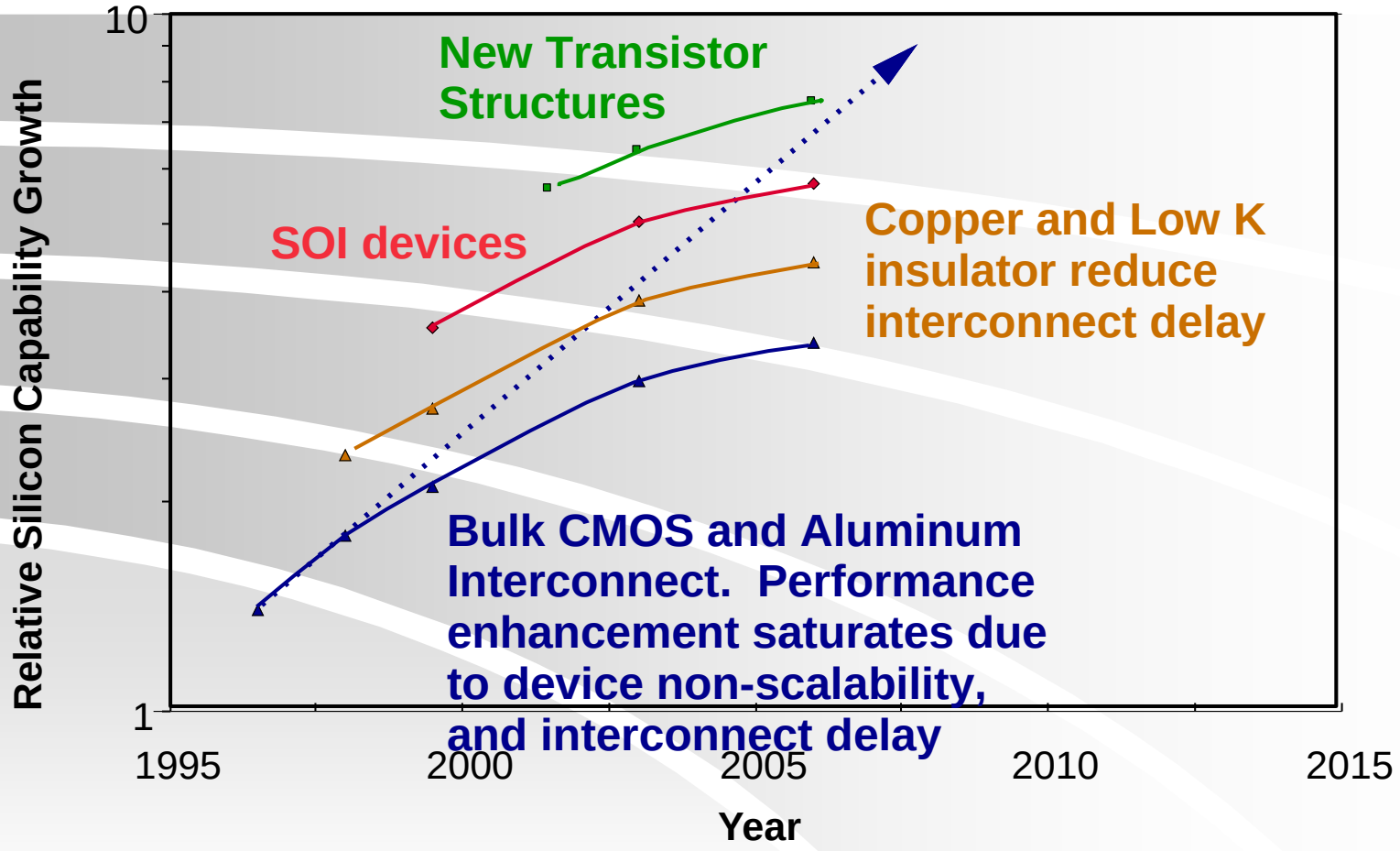
(a)



(b)

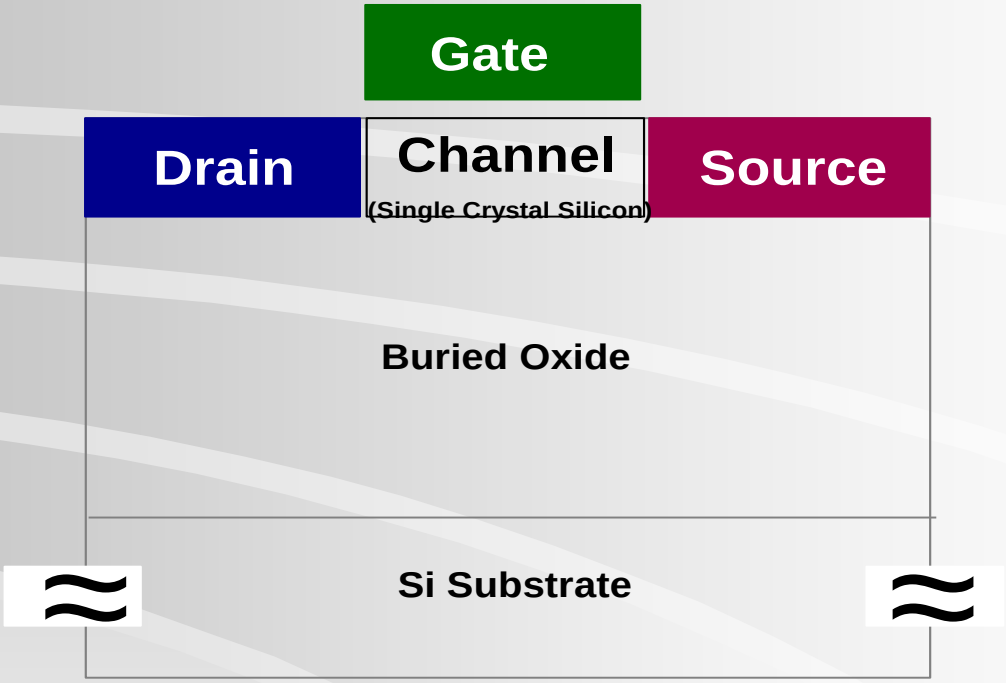
CMOS Circuit Performance Trends

Challenges and Solutions

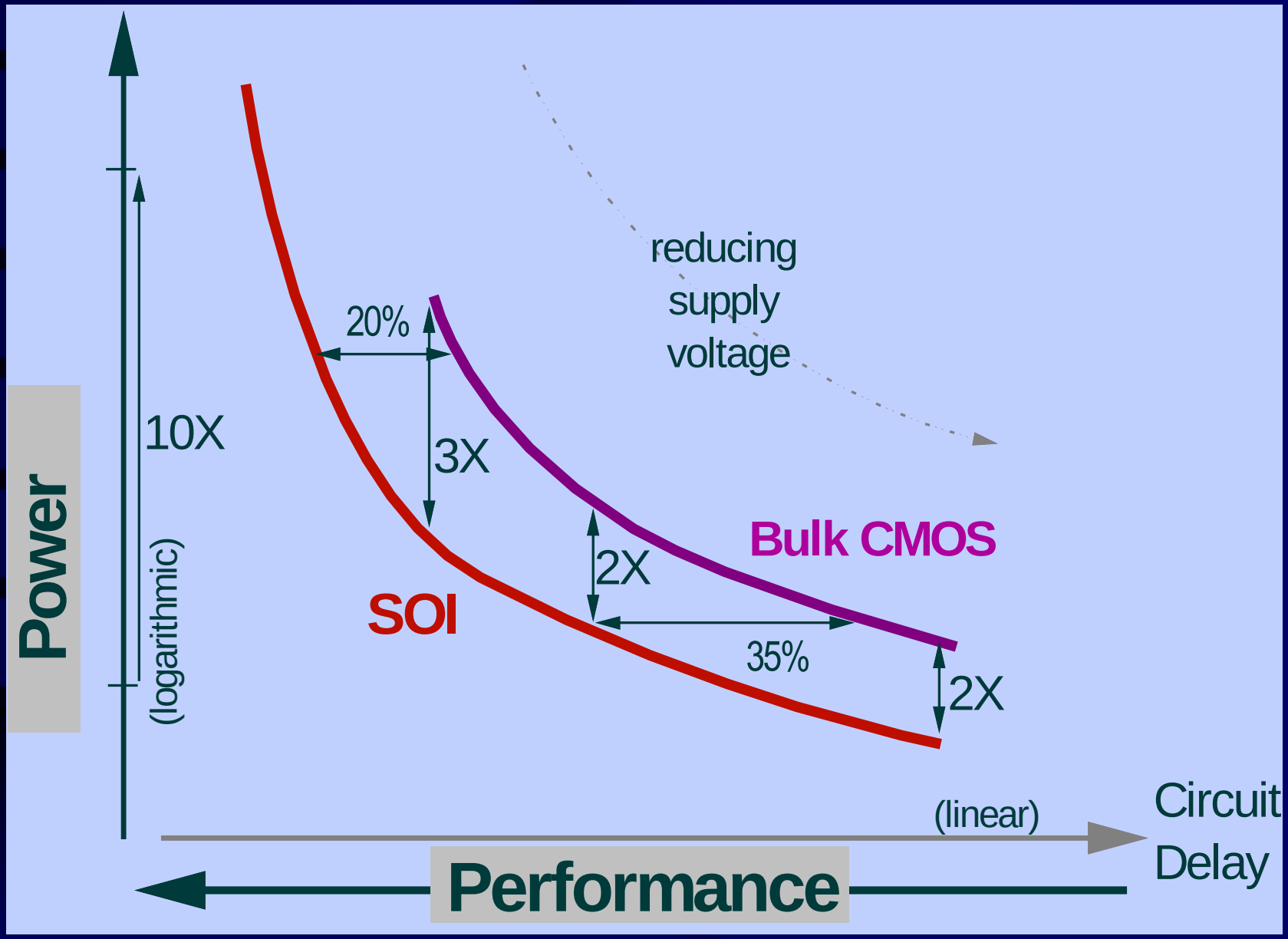


B. Davari, VLSI Circuits Symposium, Kyoto, Japan, May 1999

Silicon-on-Oxide (SOI) Field Effect Transistor (FET)

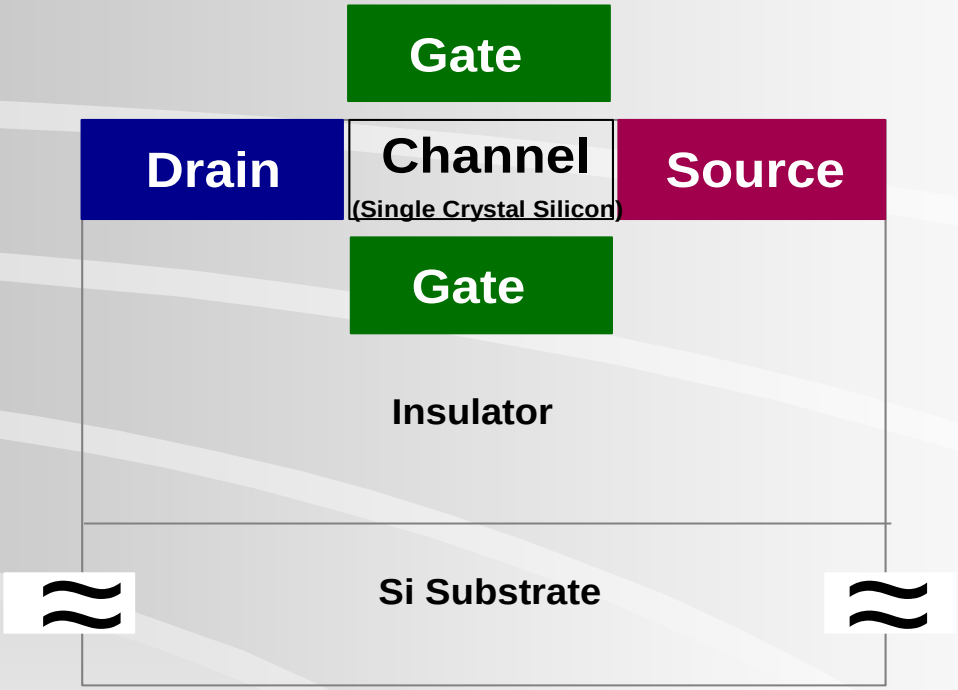


Source: CMOS Scaling into the Nanometer Regime; Yuan Taur, et. al; Proceedings of the IEEE
Vol. 85, No. 4, April 1997.

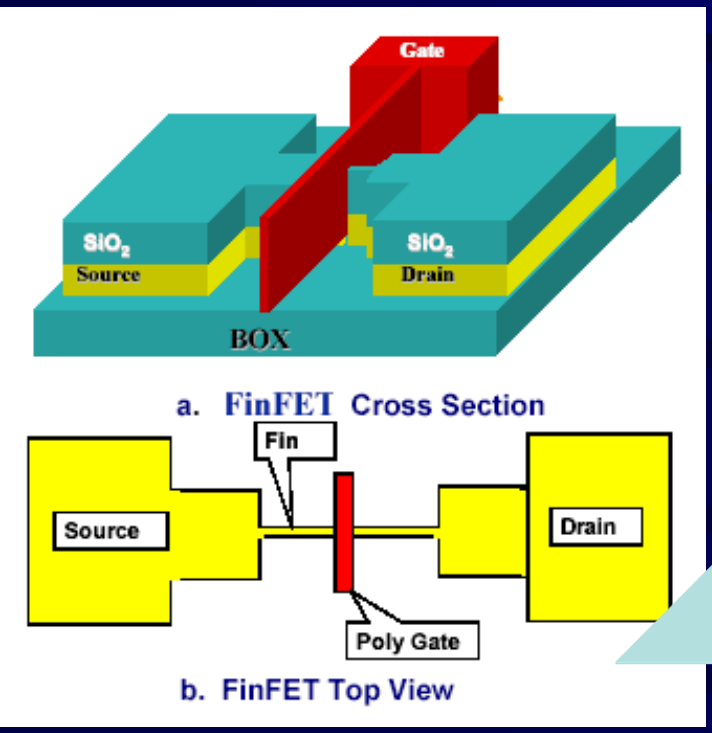


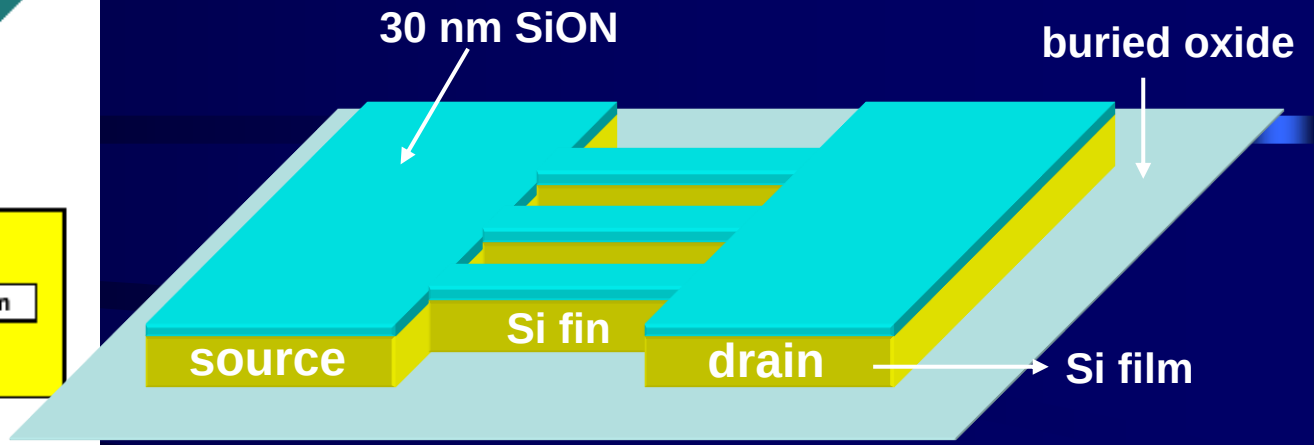
D.K. Sadana, Proc. ULSI Process Integration II, ECS Spring Meeting, Washington , March 2001.

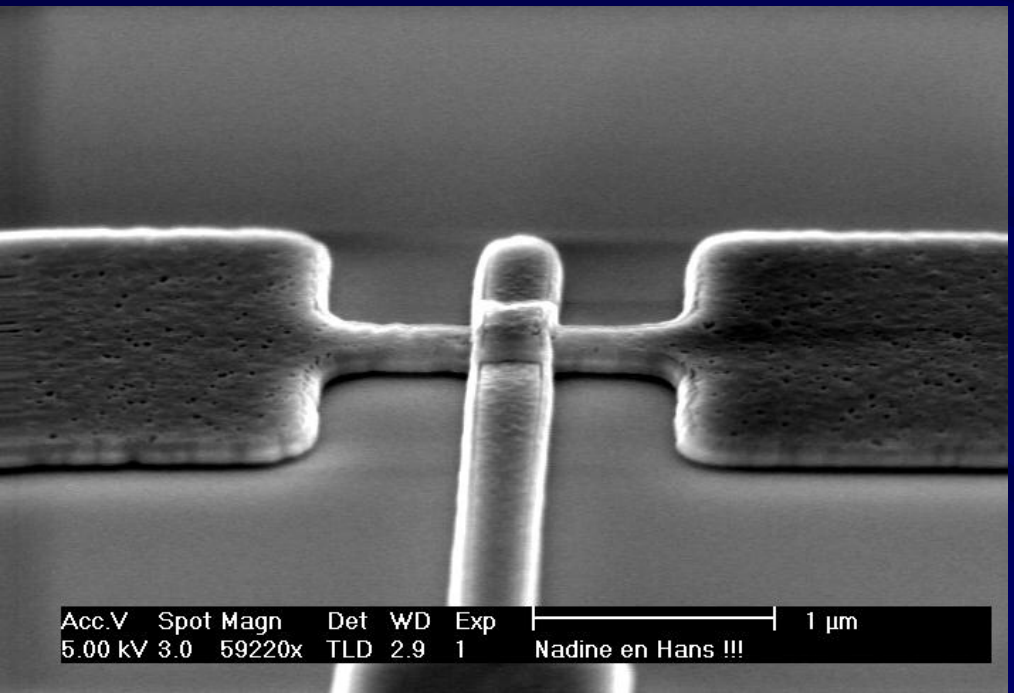
New Structure: Double Gate FET

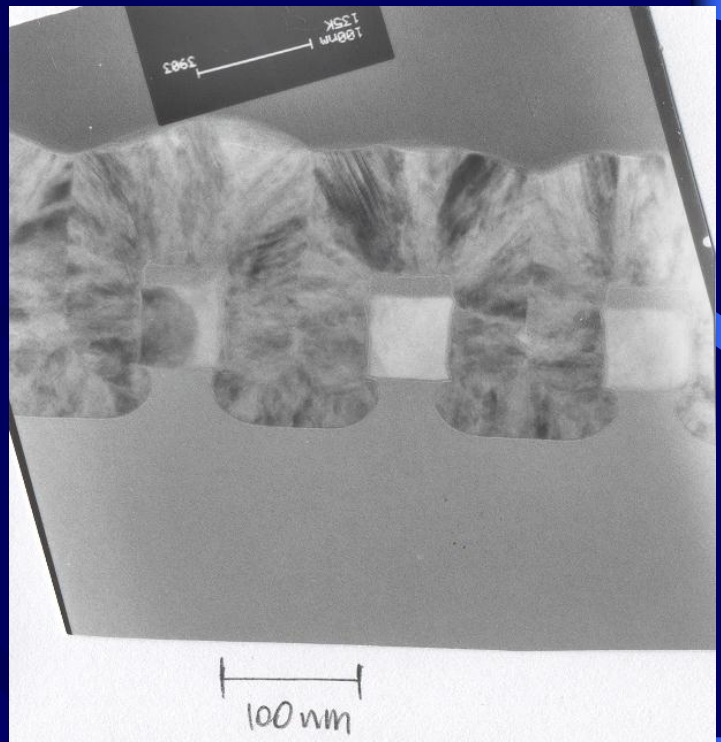


FinFET

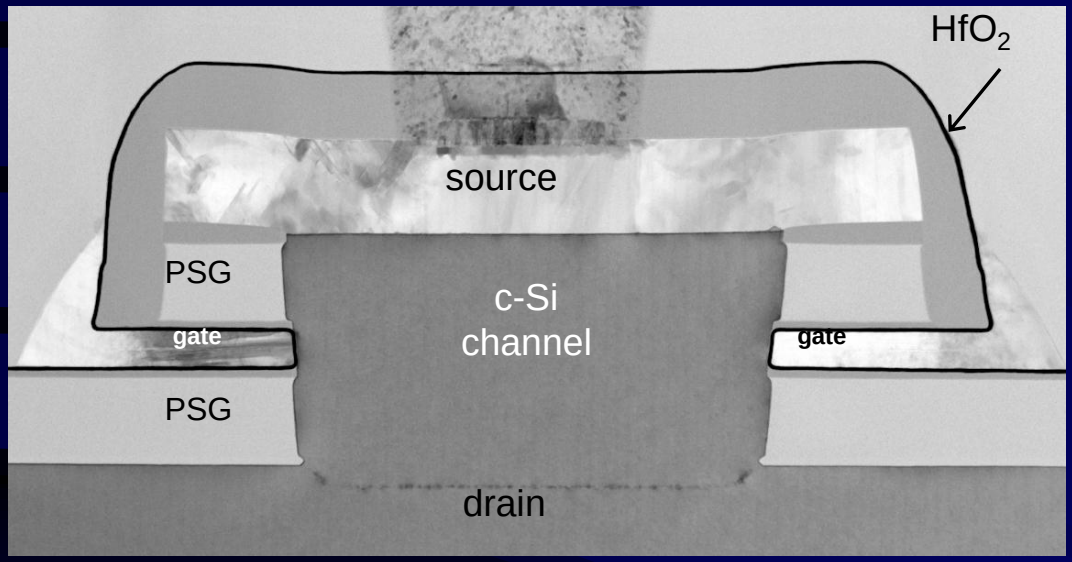

Gate
SiO2
Source
SiO2
Drain
BOX
a. FinFET Cross Section
Fin
Source
Drain
Poly Gate
b. FinFET Top View

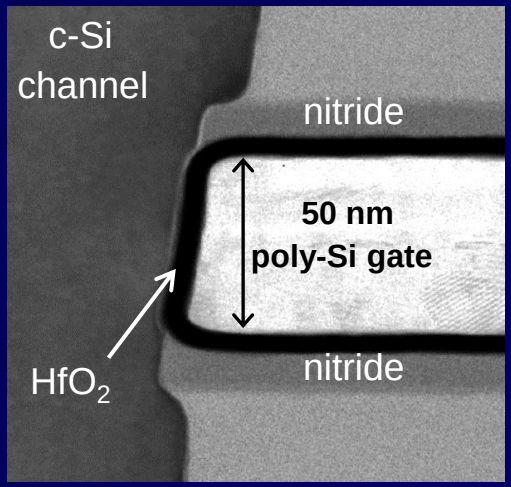

30 nm SiON
buried oxide
Si fin
source
drain
Si film

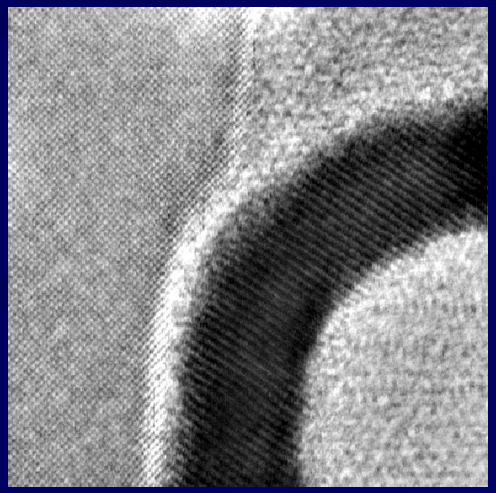

Acc.V Spot Magn Det WD Exp
5.00 kV 3.0 59220x TLD 2.9 1
1 µm
Nadine en Hans !!!


100 nm

HfO_2 Gate Dielectric on Vertical Transistor

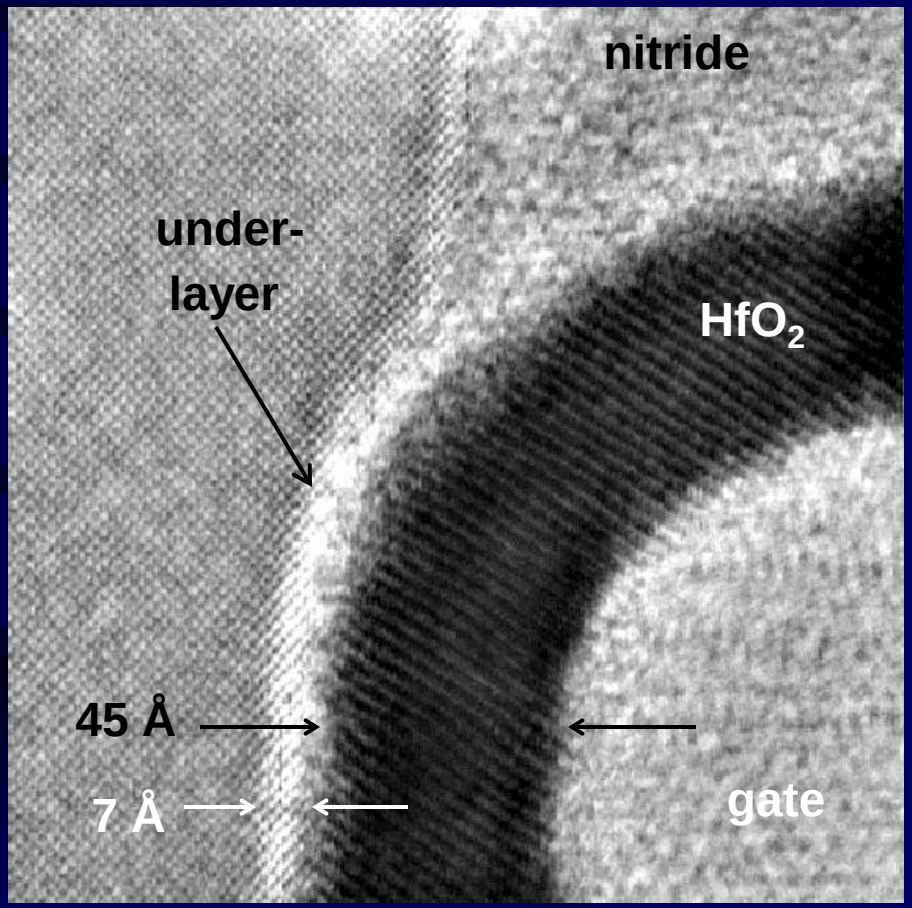






(from M. Green)

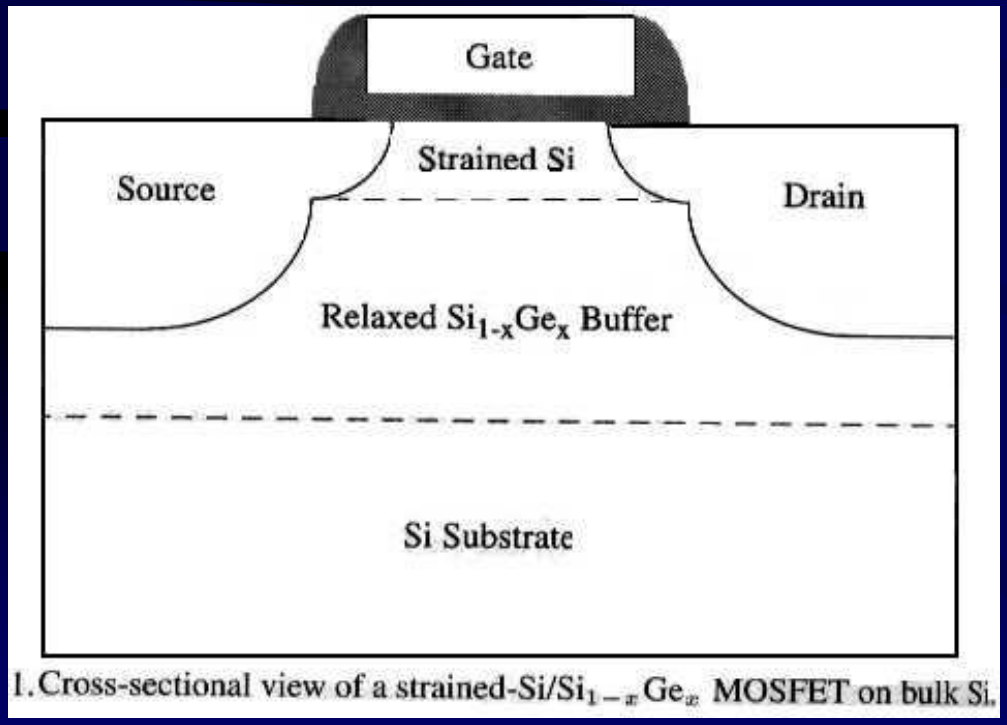
VRG: Atomic Resolution Image of HfO_2 Gate Dielectric



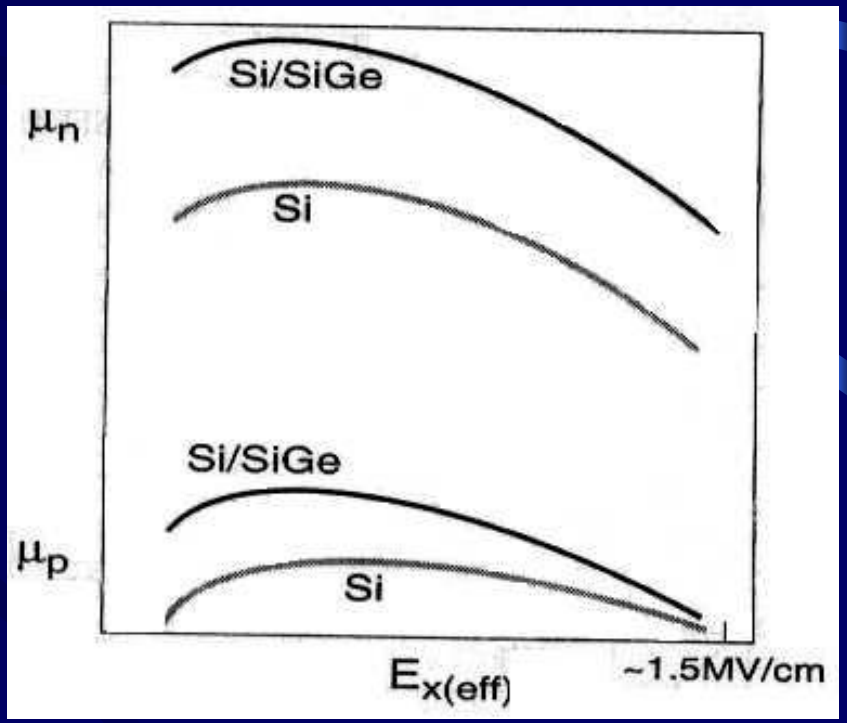
(from M. Green)

Canal de SiGe ou Si tensionado

- Modificação da estrutura de bandas E - k
- Maior mobilidade
- Maior vel. de saturação

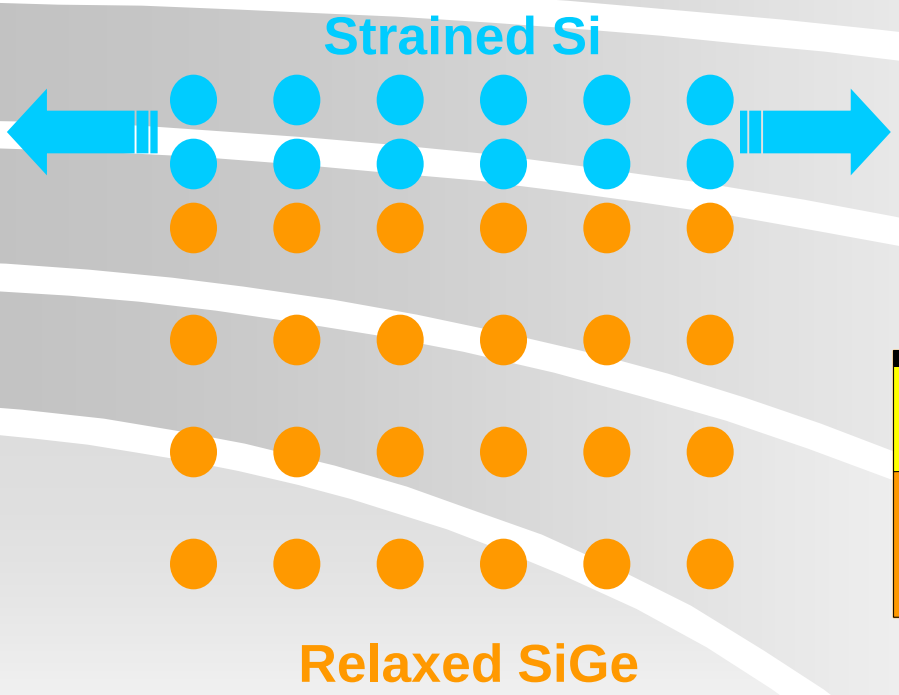


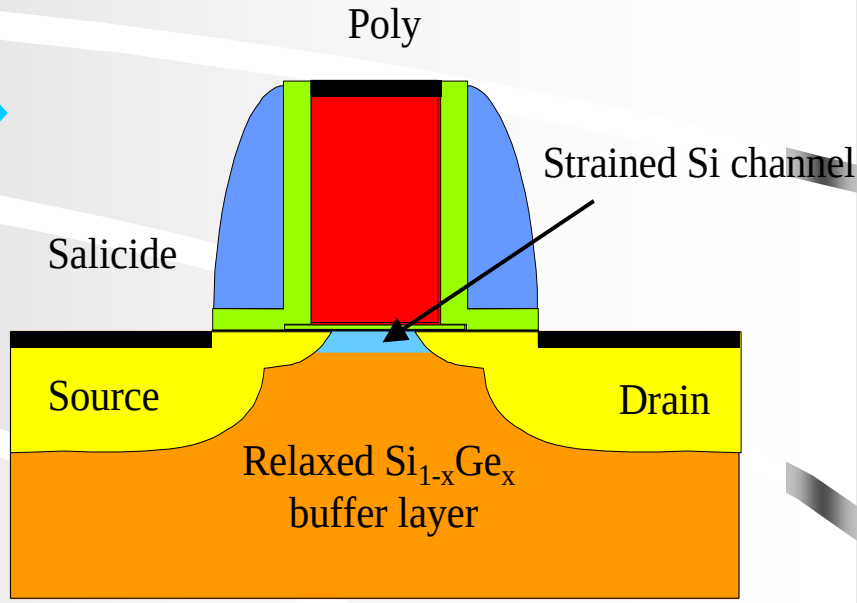
1. Cross-sectional view of a strained-Si/$Si_{1-x}Ge_x$ MOSFET on bulk Si.



Strained Si

- Device architecture:





Quais são as maiores barreiras futuras?

- Custo de produção (litografia, outros)
- Saturação na velocidade de operação (propagação de sinal e de relógio / linhas).
- Uniformidade, rendimento e confiabilidade
- Consumo de potência
- Efeitos de canal curto, tunelamento, resistências parasitárias (S/D).

- Limite prático?

Evolução de Microeletrônica, Regras de Escalamento e Limites

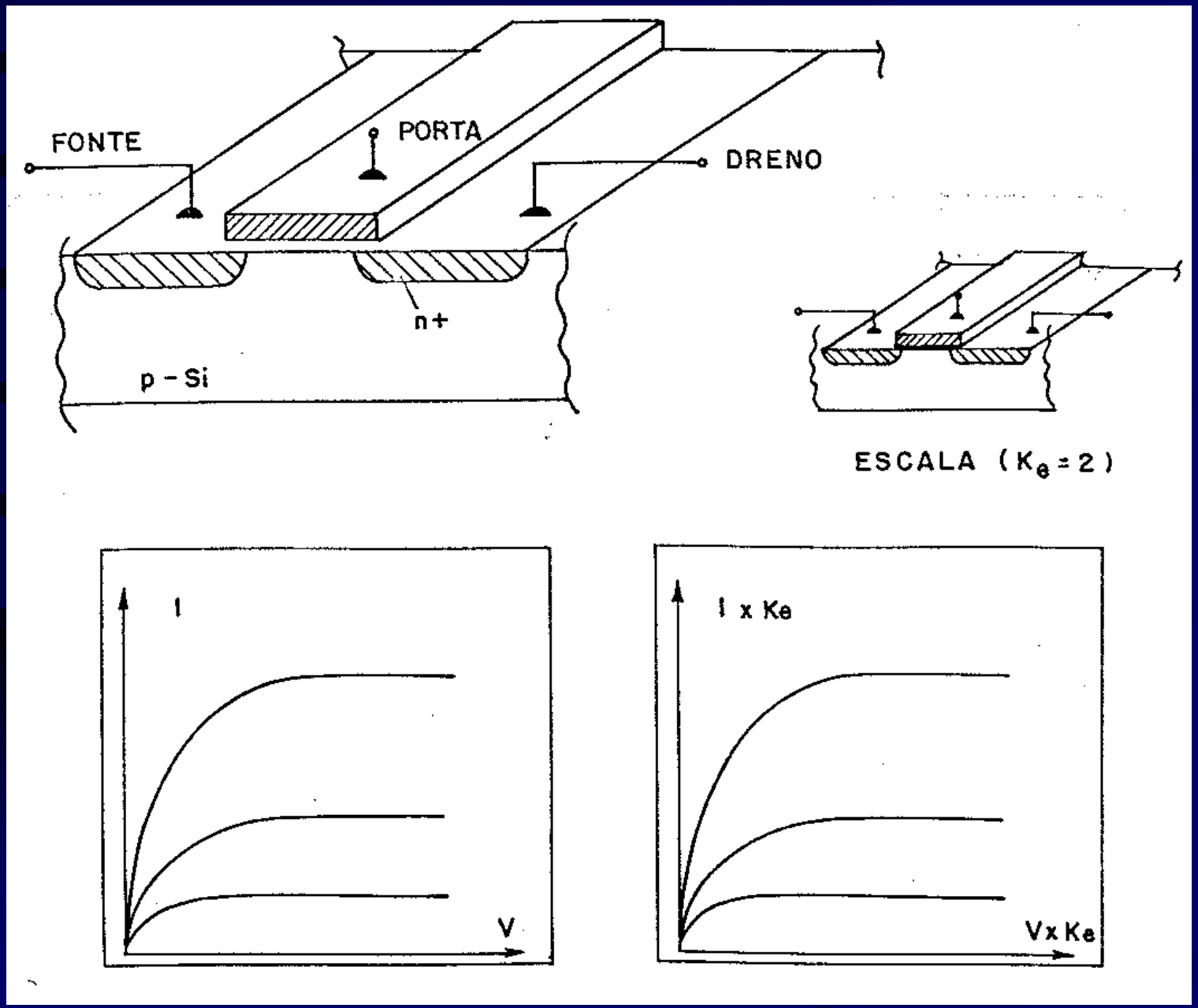
5. Regras de Escalamento

- Perguntas:
  - Como reduzir (escalar) dimensões ?
  - Quais as limitações dos dispositivos escalados?
  - Quais os limites de escalamento?

Leis de Escalamento

Parâmetro	Fator de escala
Dimensões: L, W, t_{ox}, x_J	k_d
N dopagem	k_N
Tensões	k_V

Leis de Escalamento – cont.

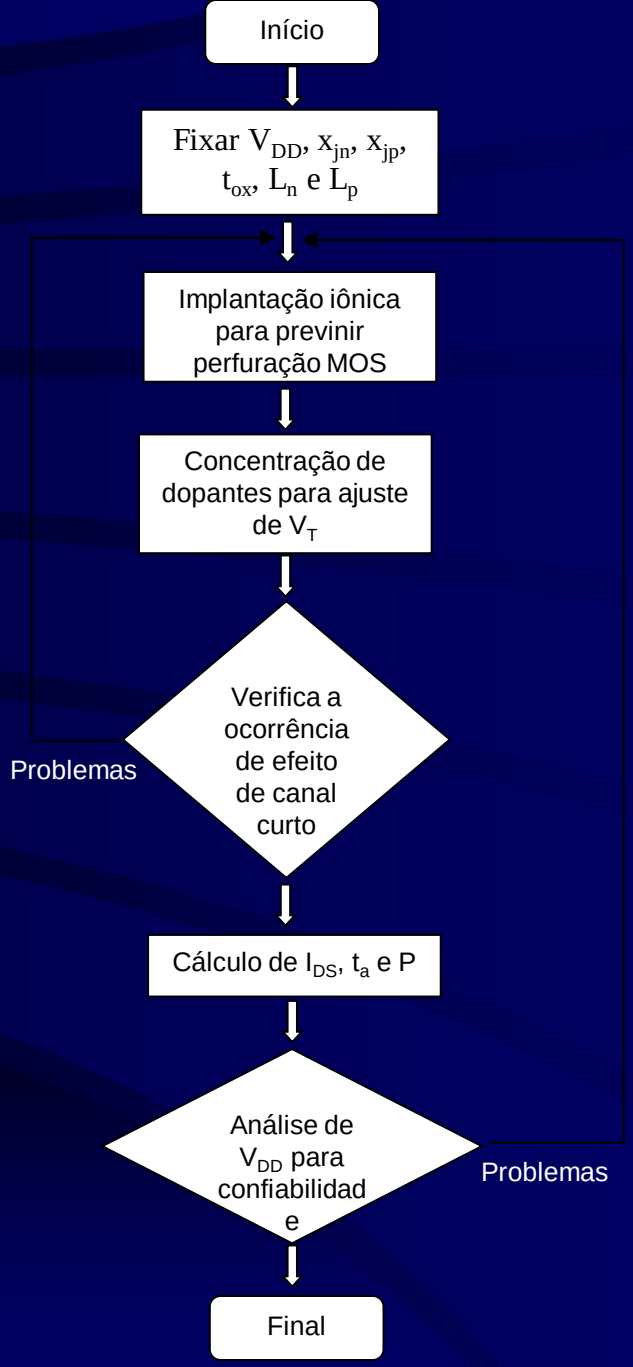


Leis de Escalamento – Tipos de Leis

Parâmetro	EC	VC	VQC	Geral
W, L, x_J	1/k	1/k	1/k	$1/k_d$
t_{OX}	1/k	$1/\sqrt{k}$	1/k	$1/k_d$
N	k	k	k	k_d^2/k_v
V_{DD}	1/k	1	$1/\sqrt{k}$	$1/ k_v$
I_{DS}	1/k	$\sqrt{k}$	1	k_d/k_v^2
C	1/k	$1/k^{3/2}$	1/k	$1/k_d$
t_a	1/k	$1/k^2$	$1/k^{3/2}$	k_d/k_v^2
P	$1/k^2$	$\sqrt{k}$	$1/\sqrt{k}$	k_d/k_v^3
$P.t_a$	$1/k^3$	$1/k^{3/2}$	$1/k^2$	$1/k_d^2k_v$
P/A	1	$k^{5/2}$	$k^{3/2}$	k_d^3/k_v^3

Leis de Escalamento – Procedimento Prático

- Por simulações de:
  - Processos (SUPREM)
  - Dispositivos (PISCES)
- Ajustar os parâmetros para ótimo desempenho, com análise de:
  - Tensão de limiar, V_T
  - Efeito de canal curto (V_T x L e V_{DD})
  - Perfuração MOS (punchthrough)
  - Corrente de corte, I_{off}
  - Tempo de atraso, t_a
  - Potência, P
  - Corrente de porta e substrato p/ confiabilidade

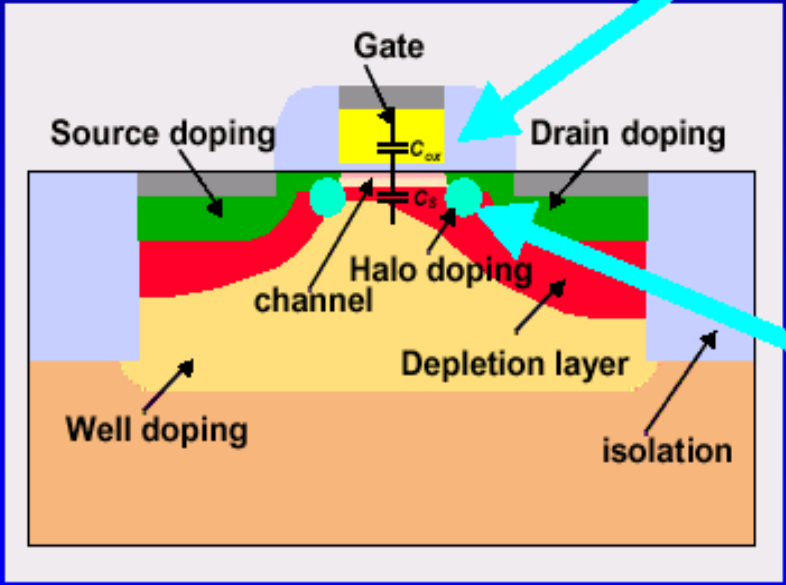

Início
Fixar V_{DD}, x_{jn}, x_{jp}, t_{ox}, L_n e L_p
Implantação iônica para previnir perfuração MOS
Concentração de dopantes para ajuste de V_T
Verifica a ocorrência de efeito de canal curto
Problemas
Cálculo de I_{DS}, t_a e P
Análise de V_{DD} para confiabilidade
Problemas
Final

Limitações

- Limitações de transistores de pequenas dimensões:
  - Efeitos de canal curto, ΔV_T x L e ΔV_T x V_{DS}
  - Perfuração MOS
  - Resistências parasitárias
  - Capacitância de inversão
  - Corrente de tunelamento de porta
  - Redução de mobilidade
  - Injeção de portadores quentes
  - Rupturas
  - Efeitos de canal estreito, ΔV_T x W

Threshold voltage:

- kT/q (subthreshold slope)
- V_{DD} - V_T decreases



Gate:

- tunneling
- inversion layer
- polySi gate depletion, activation, dopant penetration

Tunneling:

- drain to body
- source to drain

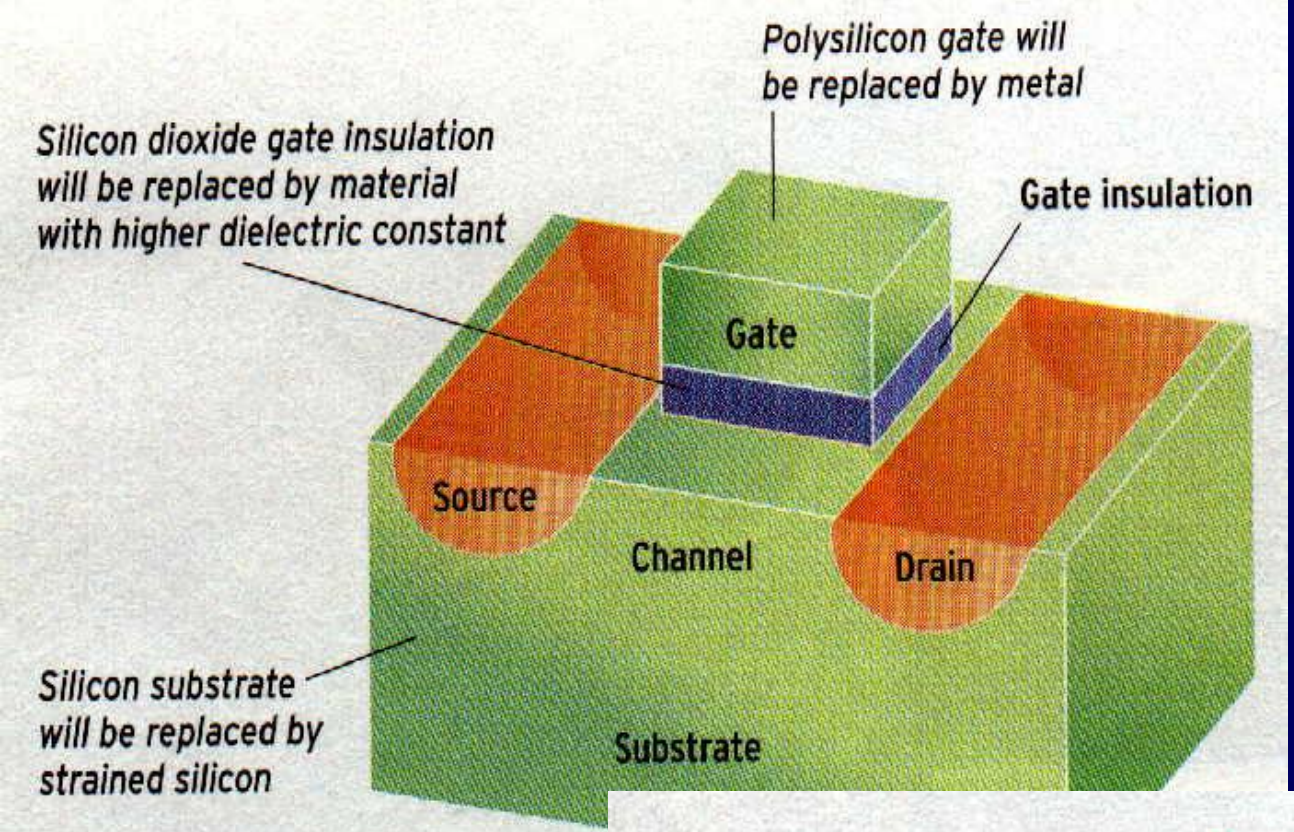
Dopant profile control:

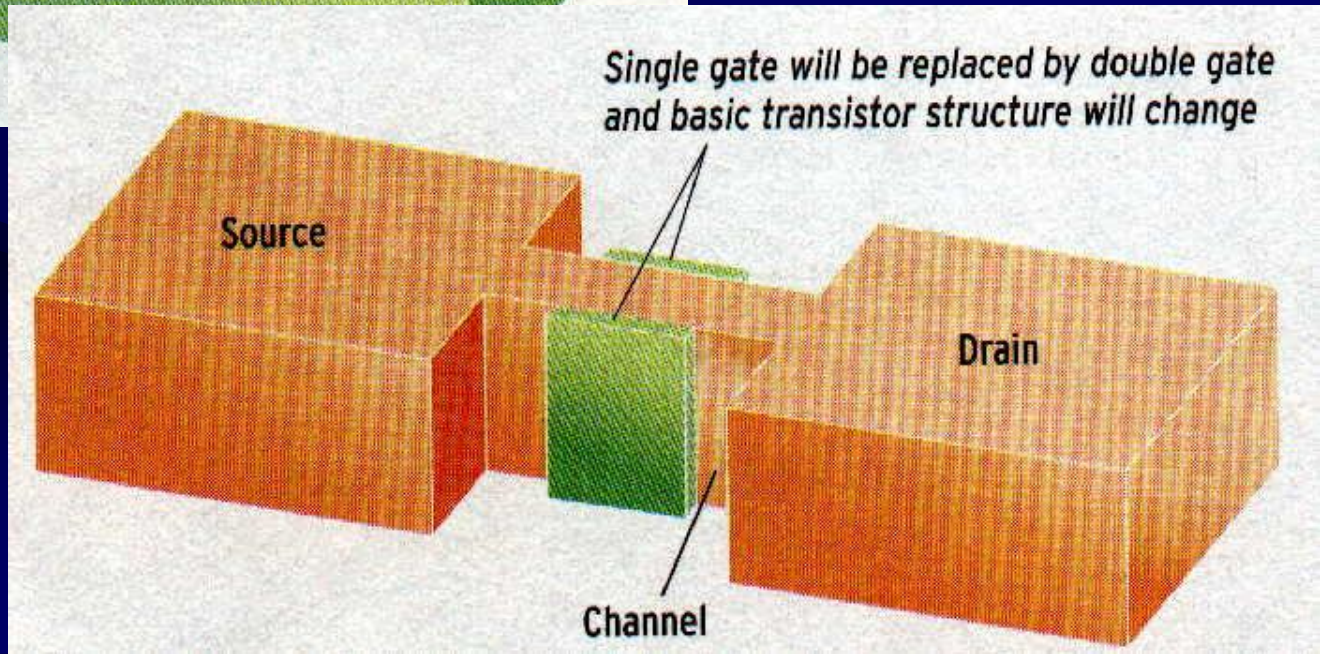
- transient enhanced diffusion
- ion implantation
- RTA ramp rate limitation
- discrete, random dopant placement

High electric fields:

- mobility degradation
- reliability

Resumo


Polysilicon gate will be replaced by metal
Silicon dioxide gate insulation will be replaced by material with higher dielectric constant
Gate insulation
Gate
Source
Channel
Drain
Silicon substrate will be replaced by strained silicon
Substrate


Single gate will be replaced by double gate and basic transistor structure will change
Source
Drain
Channel

Efeitos das limitações e “guias de estrada”

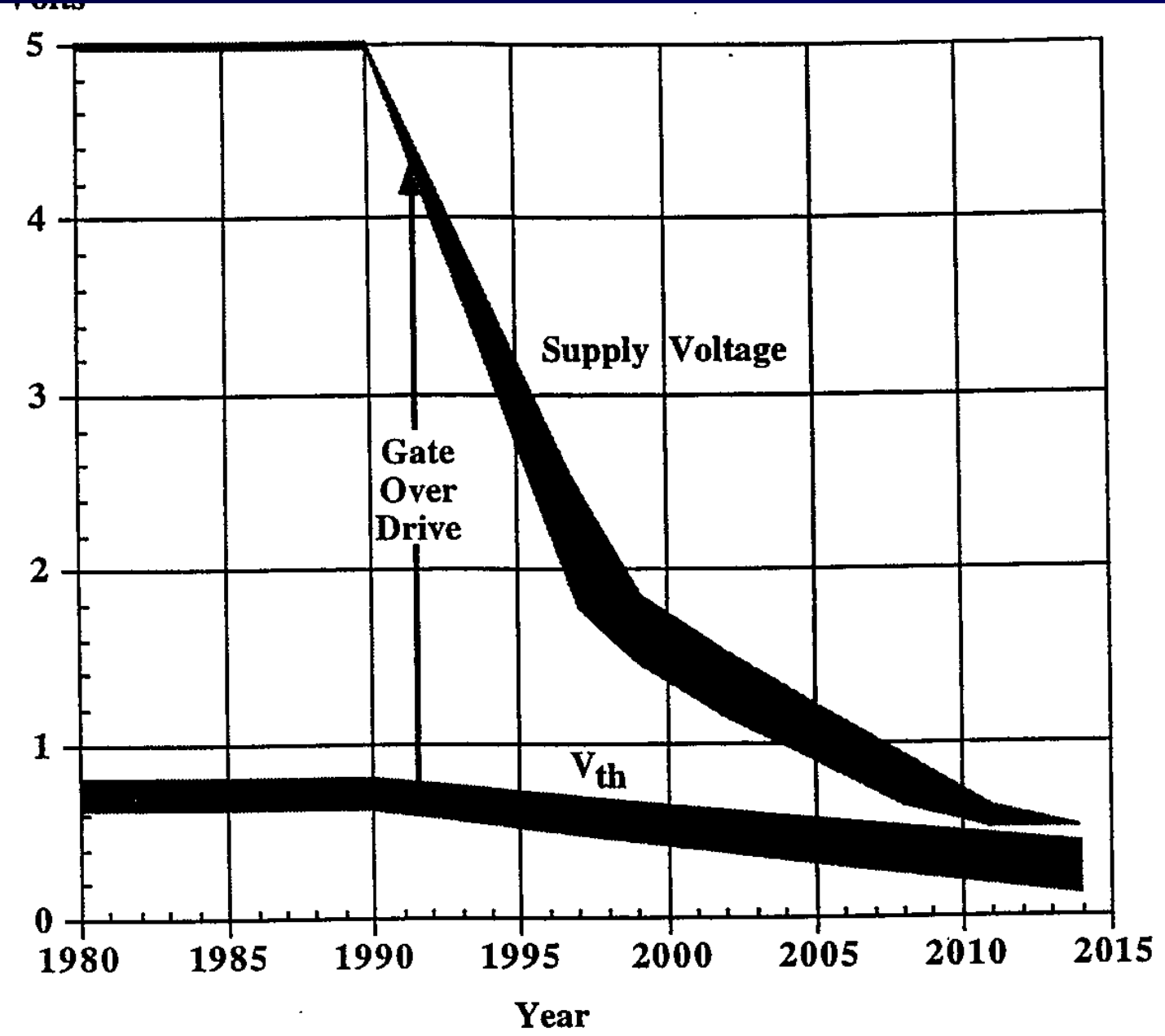
- As limitações:

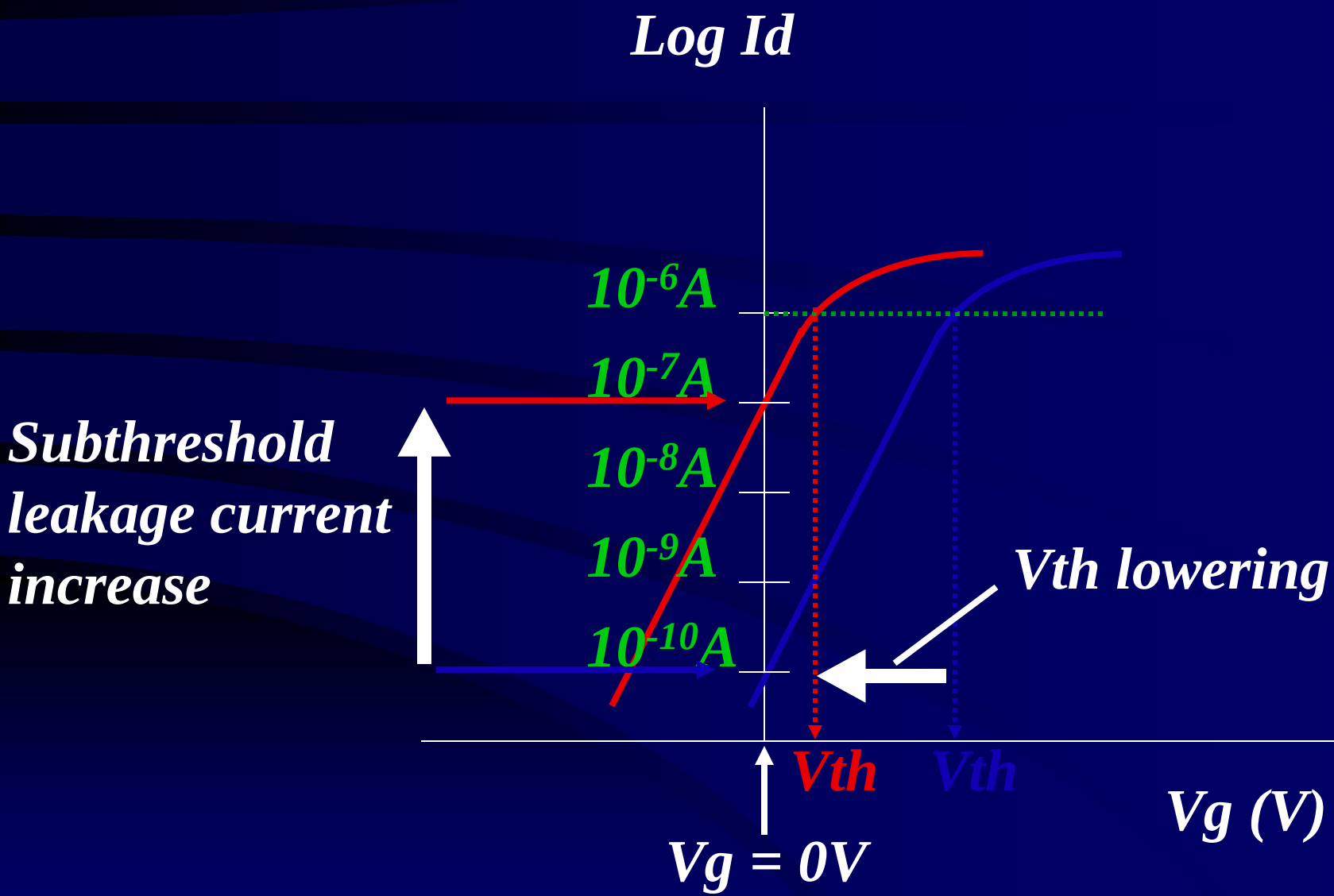
  a) afetam o desempenho elétrico dos dispositivos

  – b) determinam as condições limites de operação

  c) determinam condições de contorno para o projeto da estrutura física dos transistores e do processo de fabricação.

Redução de V_{DD} e V_T:




Log Id
10-6A
10-7A
10-8A
10-9A
10-10A
Subthreshold leakage current increase
Vth lowering
Vth
Vth
Vg (V)
Vg = 0V

An example of Real Scaling

	1972	2001	Ratio	Limiting factor
Gate length	6 μm	0.1 μm	1/60	
Gate oxide	100 nm	2 nm	1/50	Gate leakage TDDB
Junction depth	700 nm	35 nm	1/20	Resistance
Supply voltage	5 V	1.2 V	**1/4**	**Vth, Power**
Threshold voltage	0.8 V	0.3 V	**1/2.6**	**Subthreshold leakage**
Electric field (Vd/tox)	0.5 $MVcm^{-1}$	6 $MVcm^{-1}$	**30**	**TDDB**

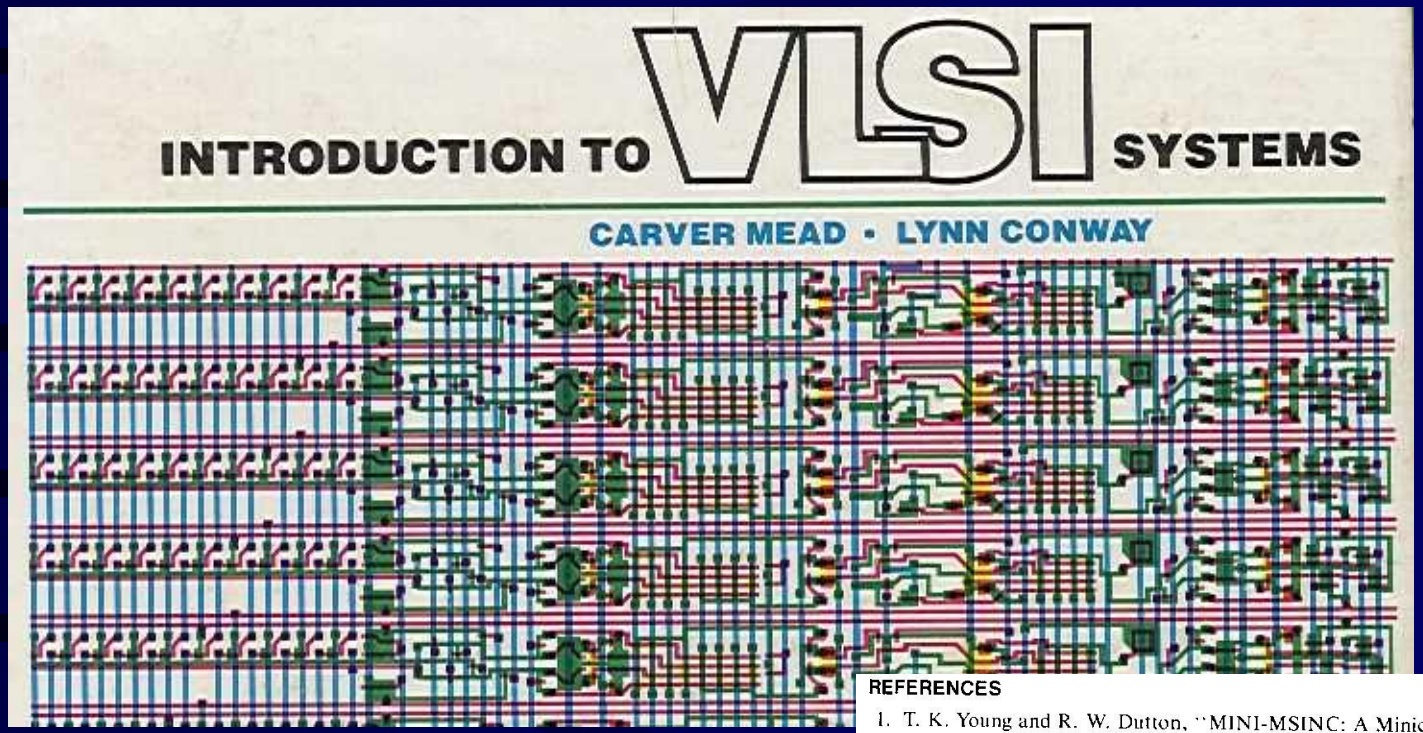
(from H. Iwai)

Evolução de Microeletrônica, Regras de Escalamento e Limites

6. Limites de Escalamento e Dispositivos pós CMOS

Qual é o limite Prático para CMOS?

(1980)



approximately five volts and minimum channel lengths of approximately six microns. Therefore, the kind of scaling we have envisioned here will take us to devices with approximately one-half micron channel lengths and current densities approximately ten times what they are today. Power per unit area will remain constant over that range. Smaller devices might be built but must be used without lowering the voltage any further. Consequently the power per unit area will increase. Finally, there appears to be a fundamental limit[10] of approximately one-quarter micron channel length, where certain physical effects such as the tunneling through the gate oxide and fluctuations in the positions of impurities in the depletion layers begin to make the devices of smaller dimension unworkable.

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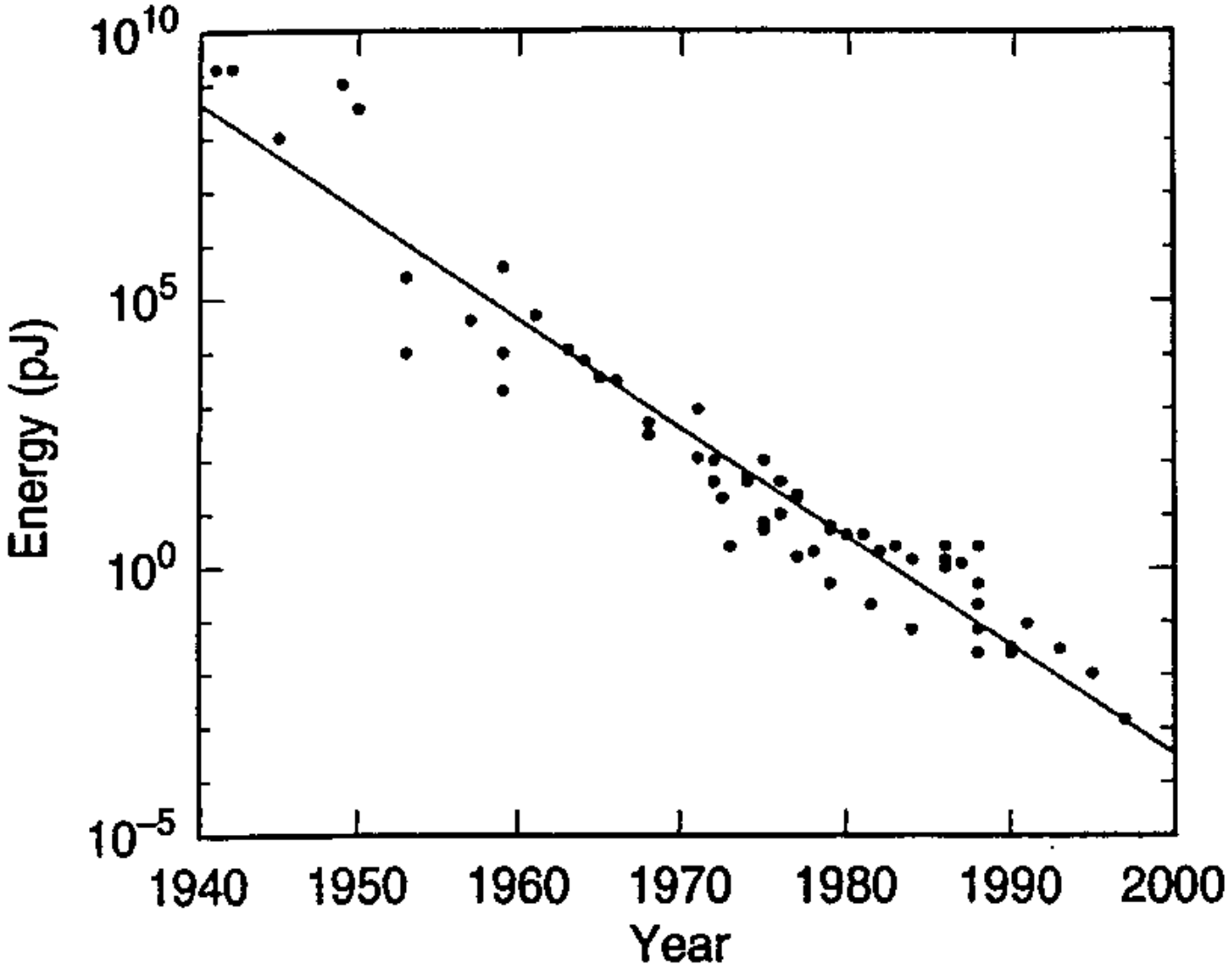
1. T. K. Young and R. W. Dutton, "MINI-MSINC: A Minicomputer Simulator for MOS Circuits with Modular Built-in Model," Stanford Electronics Laboratories, Technical Report No. 5013-1, March 1976.
2. L. Nagel and D. Pederson, "Simulation Program with Integrated Circuit Emphasis (SPICE)," 16th Midwest Symposium on Circuit Theory, Waterloo, Ontario, April 12, 1973.
3. W. M. Penney and L. Lau, eds., *MOS Integrated Circuits*, Princeton, N.J.: Van Nostrand, 1972, pp. 60–85.
4. R. C. Jaeger, "Comments on 'An Optimized Output Stage for MOS Integrated Circuits'," *IEEE J. Solid-State Circuits*, June 1975, pp. 185–186.
5. T. Kilburn; D. B. G. Edwards; and D. Aspinall, "A Parallel Arithmetic Unit Using a Saturated Transistor Fast-Carry Circuit," *Proc. IEE*, Pt. B, vol. 107, November 1960, pp. 573–584.
6. Staff of the Computation Lab, "Description of a Relay Calculator," Annals of the Harvard Computation Lab, vol. 24, Harvard University Press, 1949.
7. T. J. Chaney and C. E. Molnar, "Anomalous Behavior of Synchronizer and Arbiter Circuits," *IEEE Transactions on Computers*, April 1973, pp. 421–422.
8. C. H. Séquin and M. F. Tompsett, *Charge Transfer Devices*, New York: Academic Press, 1975.
9. F. H. Gaensslen; V. L. Rideout; E. J. Walker; and J. J. Walker, "Very Small MOSFETs for Low-Temperature Operation," *IEEE Transactions on Electron Devices*, March 1977.
10. B. Hoeneisen, and C. A. Mead, "Fundamental Limitations in Micro-electronics–1. MOS Technology," *Solid-State Electronics*, vol. 15, 1972, pp. 819–829.

Qual é o limite Prático para CMOS?

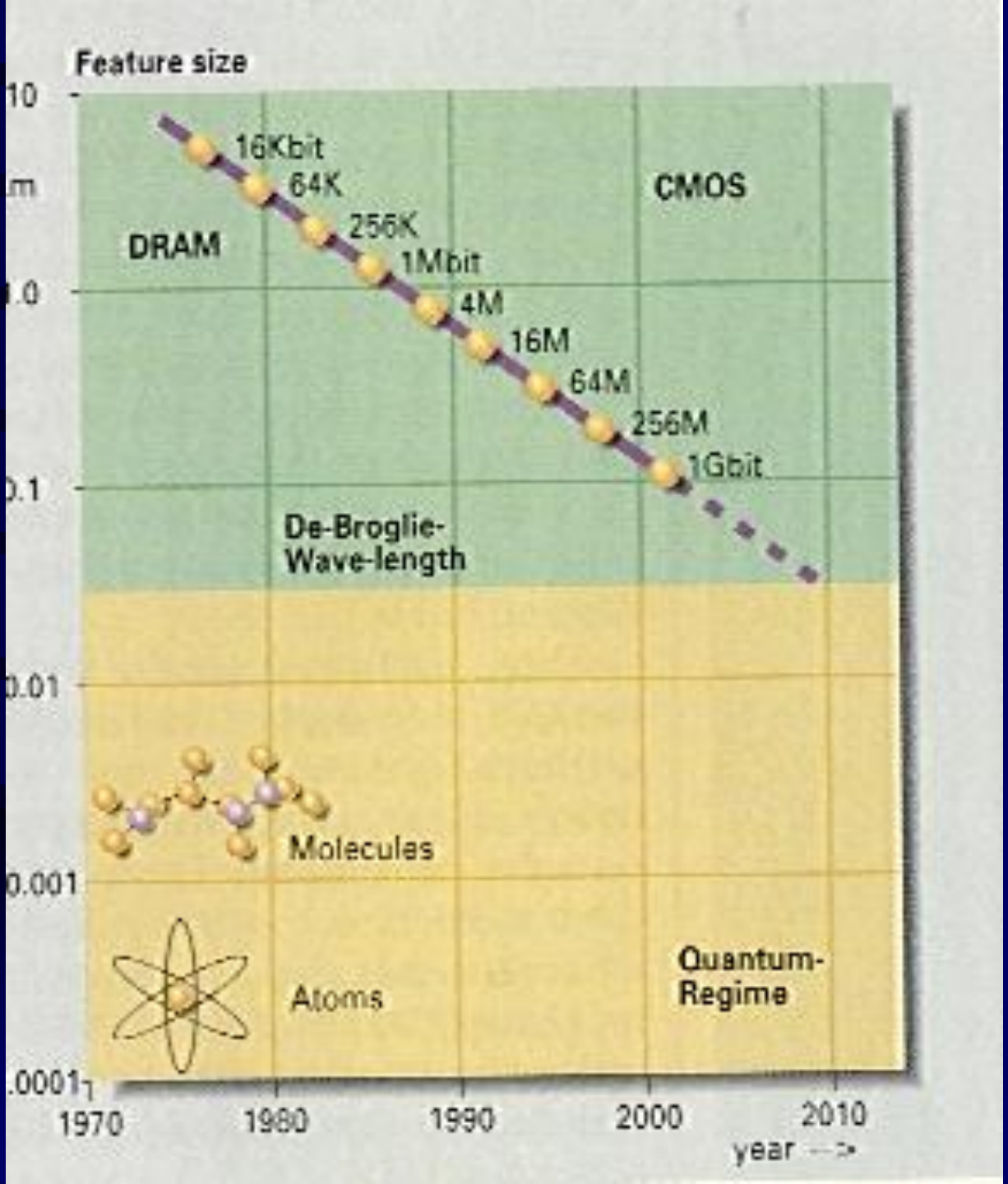
- 25 nm (H. Iwai, IEEE, JSSC, Mar. 99)
  Quando? Entre 2020 e 2030 $\Rightarrow$ 10^{10} a 10^{12} tr./chip
  $\Rightarrow$ permite produtos não visualizáveis hoje.
- Vários fatores apontam 10 nm de comprimento de porta ser um limite prático para o escalamento de CMOS. Como fatores limitantes apontam:
  - tunelamento pelo dielétrico de porta;
  - impossibilidade de escalar a tensão de alimentação, devido a questões de ruído térmico e de *bandbap;*
  - impactos de tolerância e margens do número de átomos dopantes no dispositivo [Melliar-Smith and Helms].
- Transistores com L de 16 e 15 nm já foram demonstrados [Boeuf et al e Yu et al, respectivamente, IEDM2001]
- Uma regra: $L \sim 45 \cdot t_{ox}$

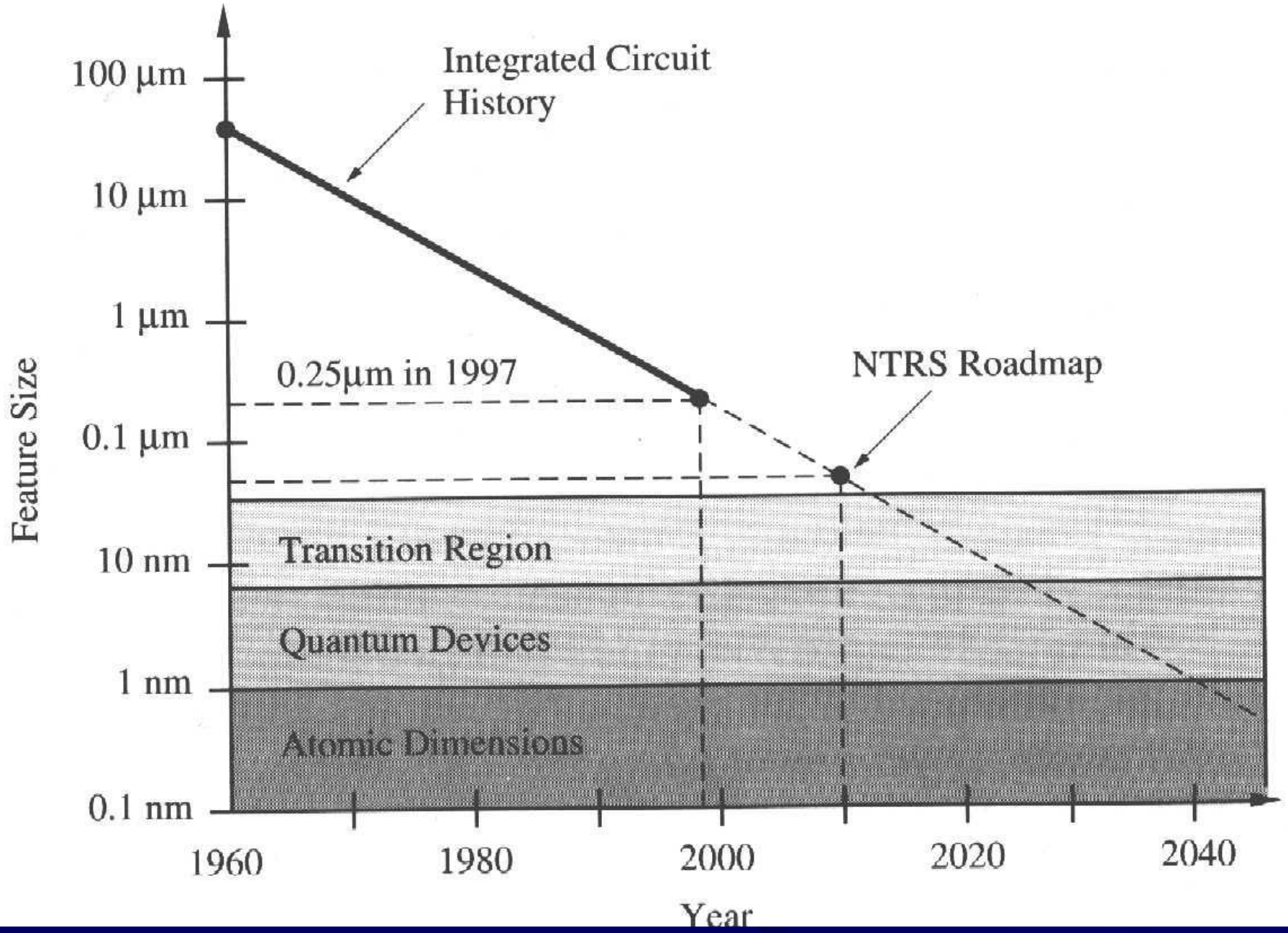
Limites de Escalamento



Limites de Escalamento

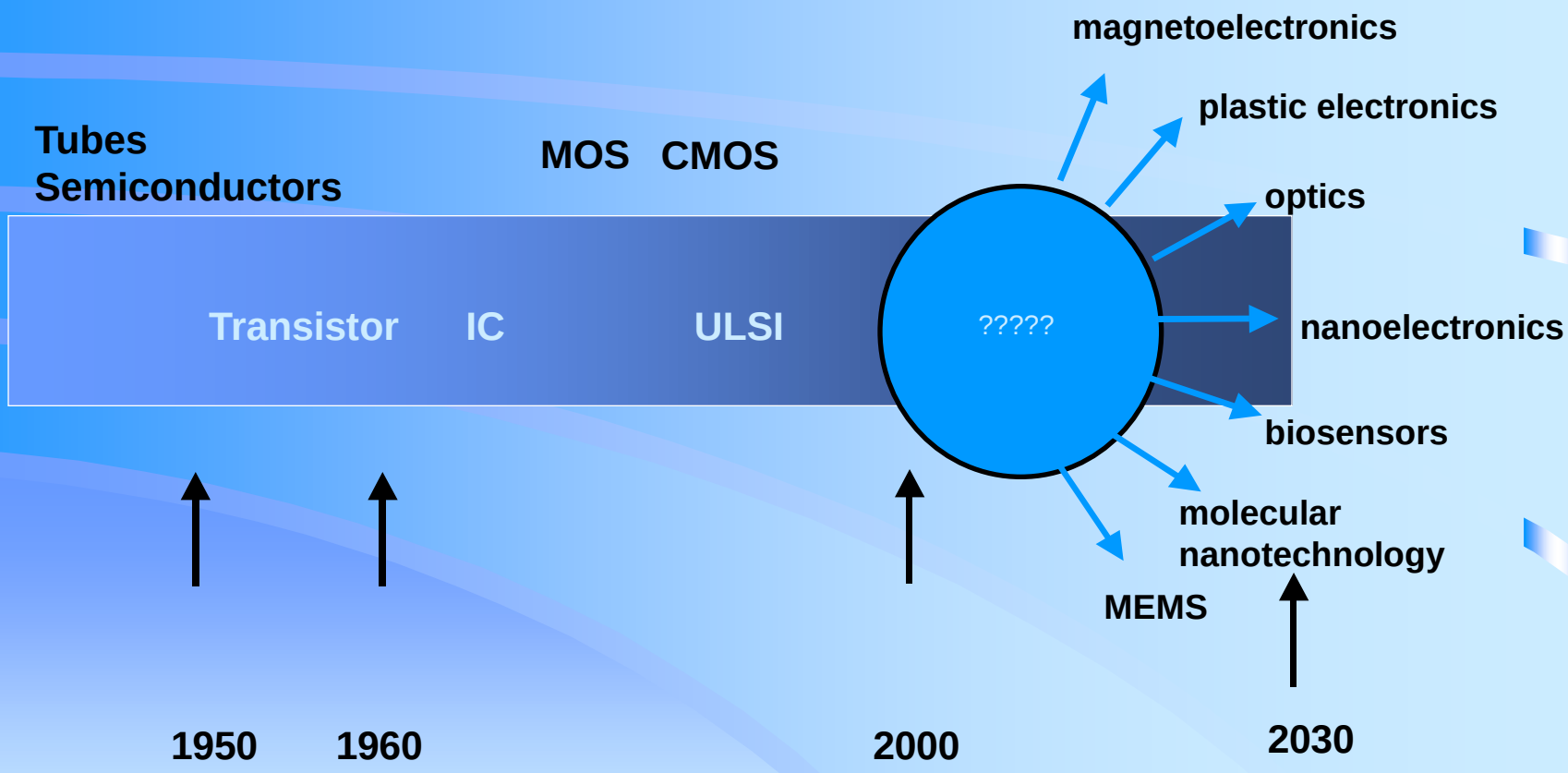
- Considerar:
  - 1. Limites fundamentais
  - 2. Limites do material
  - 3. Limites do dispositivo
  - 4. Limites do circuito
  - 5. Limites do sistema


Feature size
10
m
1.0
0.1
0.01
0.001
.0001
16Kbit
64K
256K
1Mbit
4M
16M
64M
256M
1Gbit
DRAM
CMOS
De-Broglie-
Wave-length
Molecules
Atoms
Quantum-
Regime
1970
1980
1990
2000
2010
year



(Plummer et al)

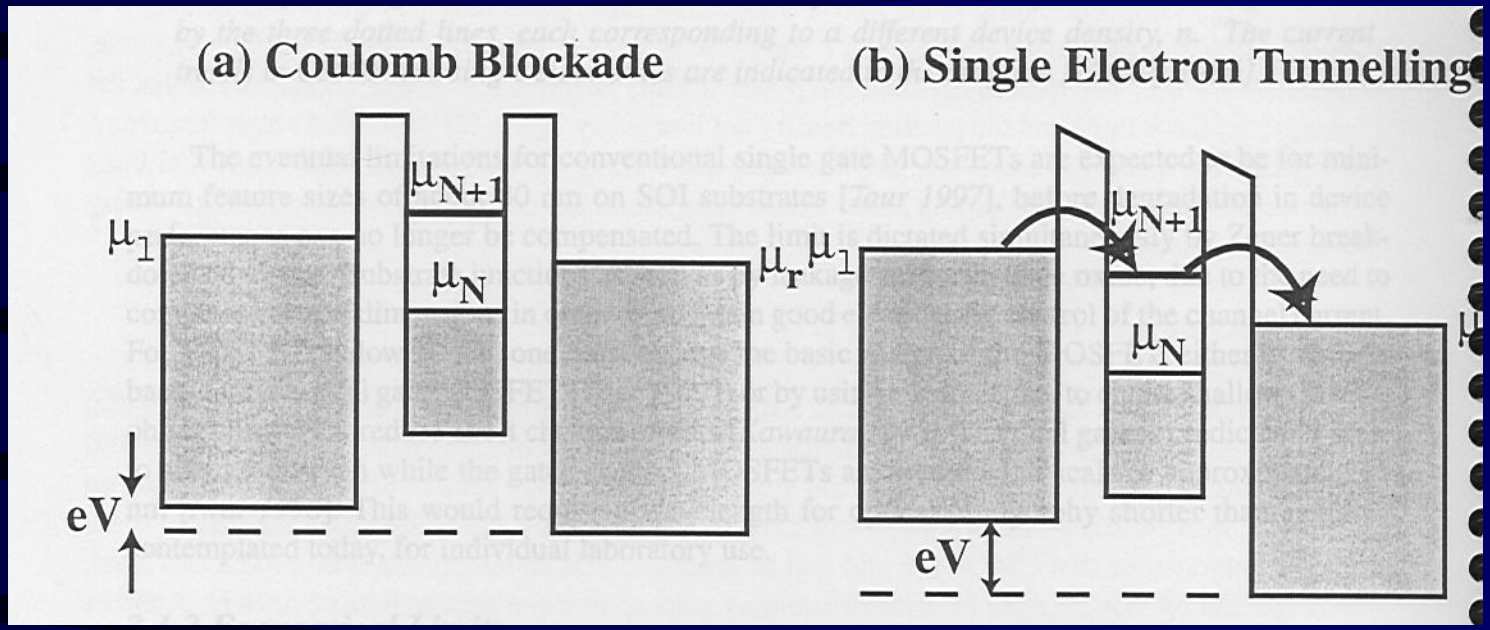
CMOS technologies and the future



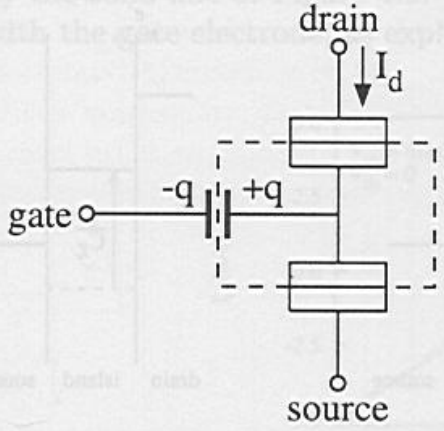
Após Limite de Escalamento CMOS?

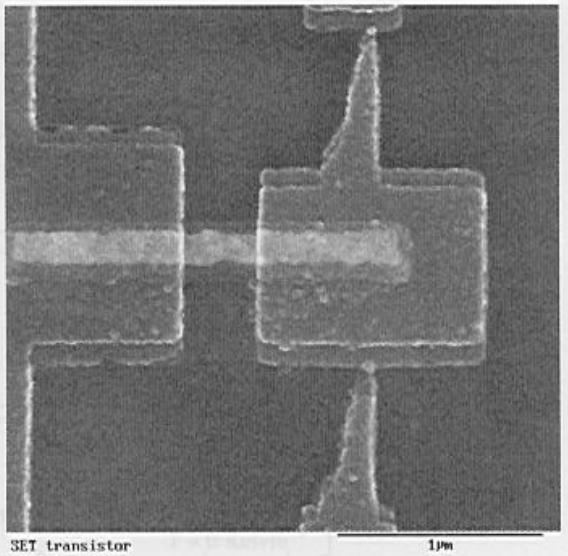
- Novos Conceitos de Dispositivos e Circuitos:
  - a) dispositivos de bloqueio Coulombiano, entre outros dispositivos de um único elétron;
  - b) Dispositivos de tunelamento ressonantes (RTD)
  - c) estruturas de nano-tubos de carbono
  - d) transistor molecular
  - e) dispositivos quânticos, onde se controla o estado do elétron de um átomo = spintrônica.

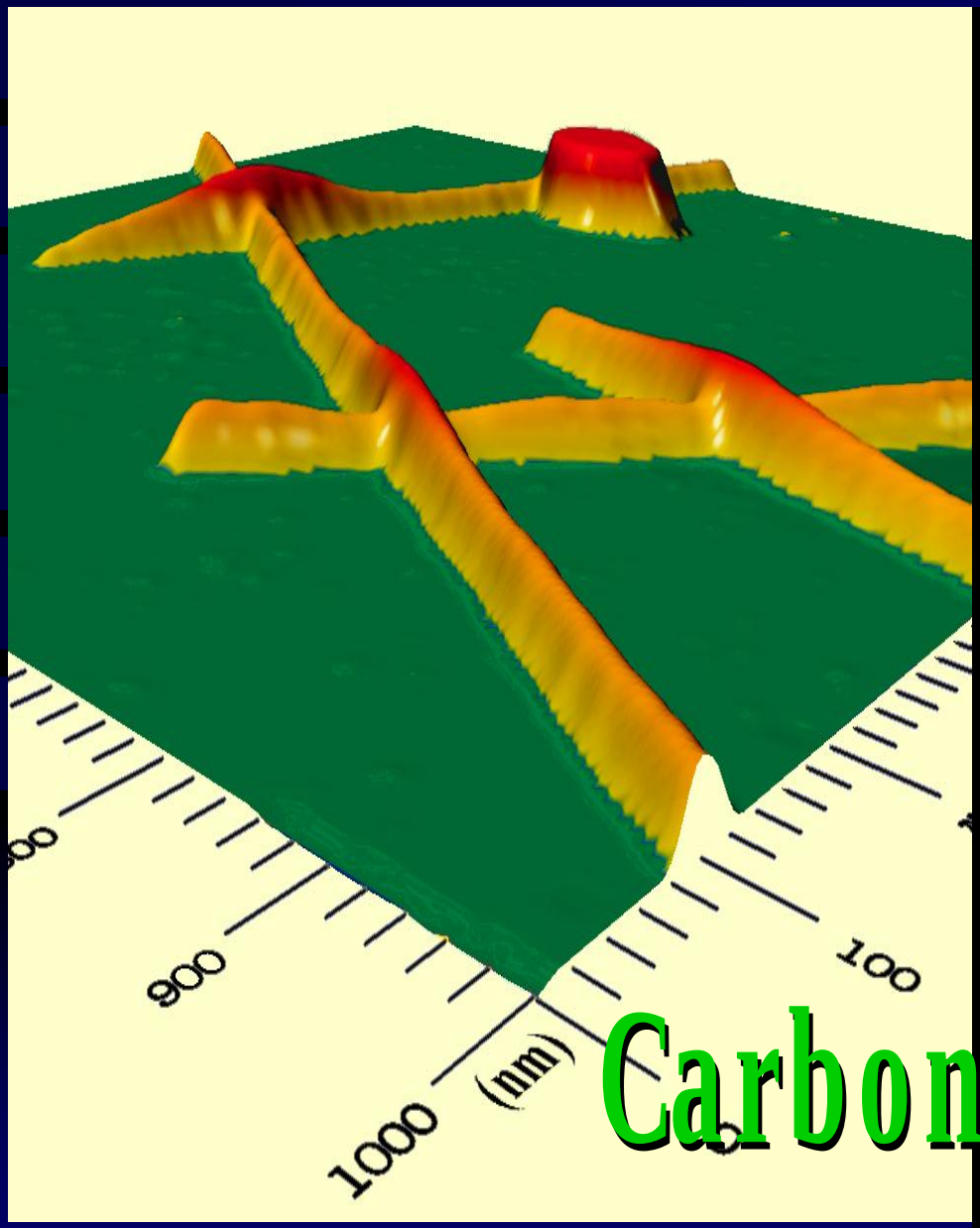
Single Electron Tunneling Device - SET

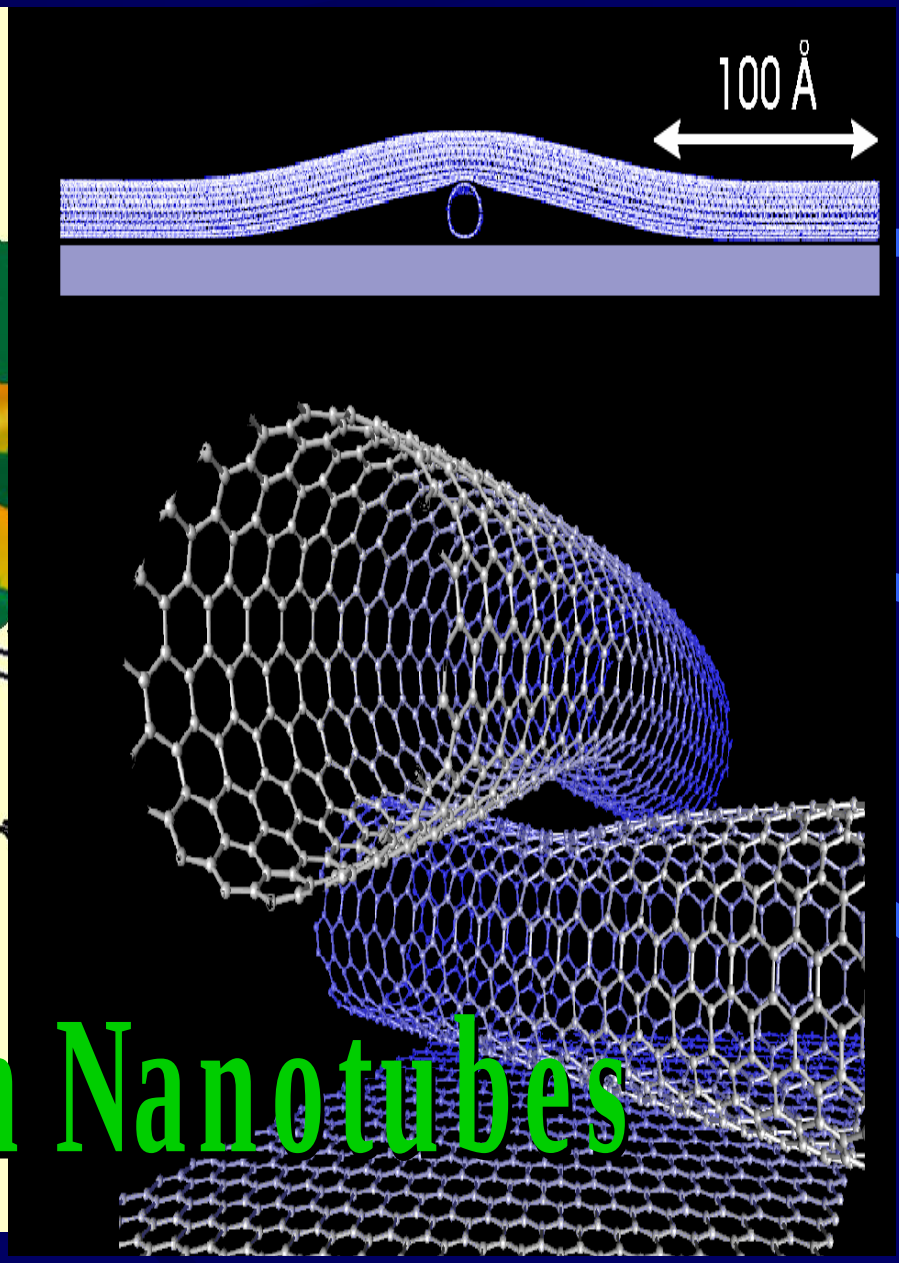


$$\Delta V = \frac{e}{C_\Sigma}$$





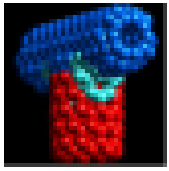




Carbon Nanotubes

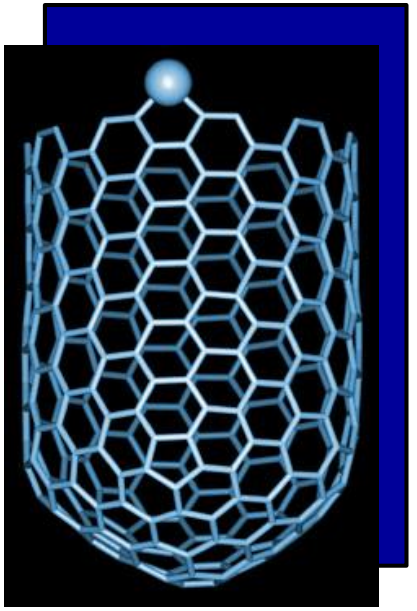
Ames Research Center

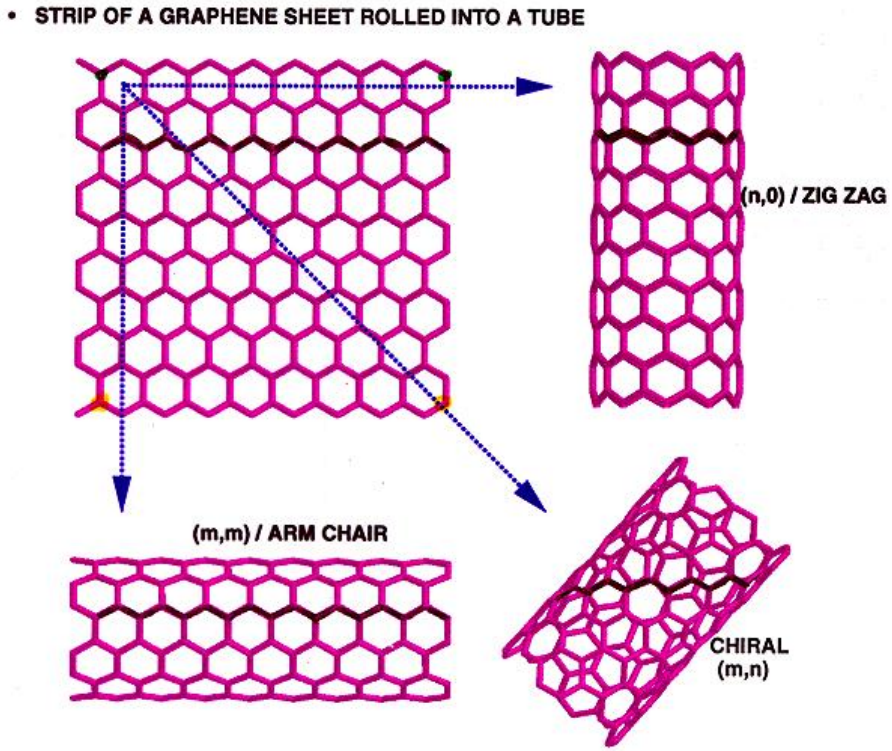
Carbon Nanotube



CNT is a tubular form of carbon with diameter as small as 1 nm.
Length: few nm to microns.

CNT is configurationally equivalent to a two dimensional graphene sheet rolled into a tube.





CNT exhibits extraordinary mechanical properties: Young's modulus over 1 Tera Pascal, as stiff as diamond, and tensile strength ~ 200 GPa.

CNT can be metallic or semiconducting, depending on chirality.

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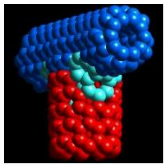
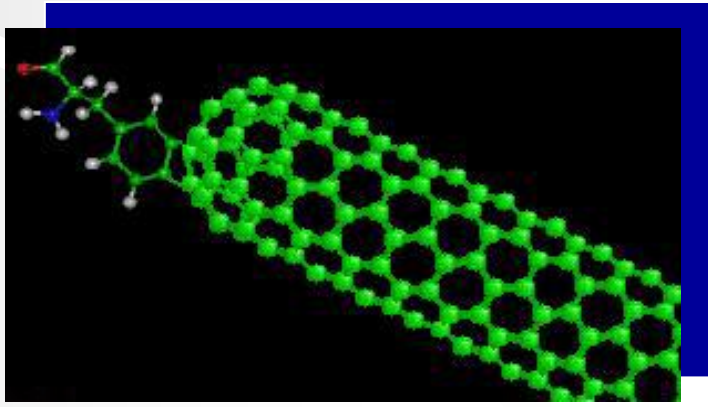
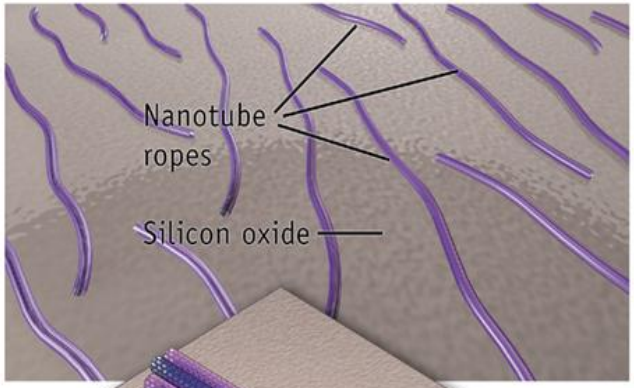
CNT Properties (cont.)



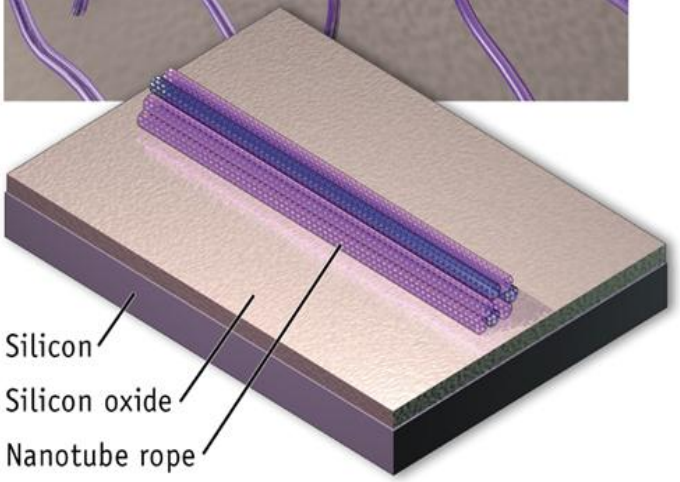
- Electrical conductivity six orders of magnitude higher than copper
- Can be metallic or semiconducting depending on chirality
  - 'tunable' bandgap
  - electronic properties can be tailored through application of external magnetic field, application of mechanical deformation…
- Very high current carrying capacity
- Excellent field emitter; high aspect ratio and small tip radius of curvature are ideal for field emission
- Can be functionalized

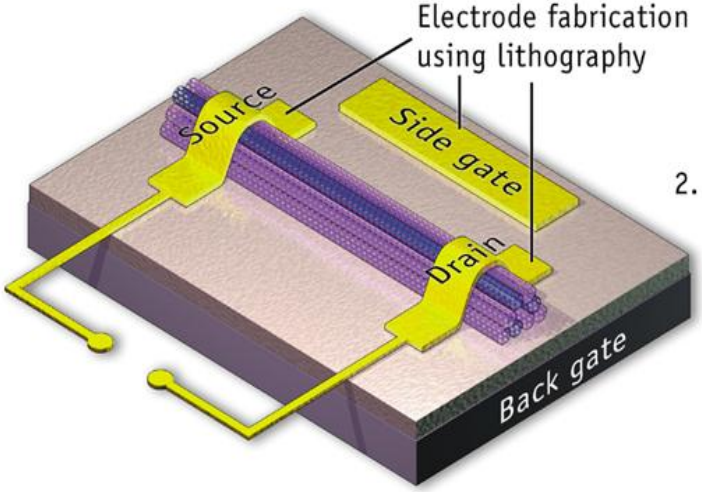


New Breakthrough Transistor Technology From IBM: Carbon Nanotubes - Constructive Deconstruction



1. Ropes of Nanotubes: The scientists deposit the ropes of metallic and semiconducting tubes onto a silicon wafer.





2. A mask is projected onto the tubes and the semiconducting tubes are switched off, insulating them from electricity.

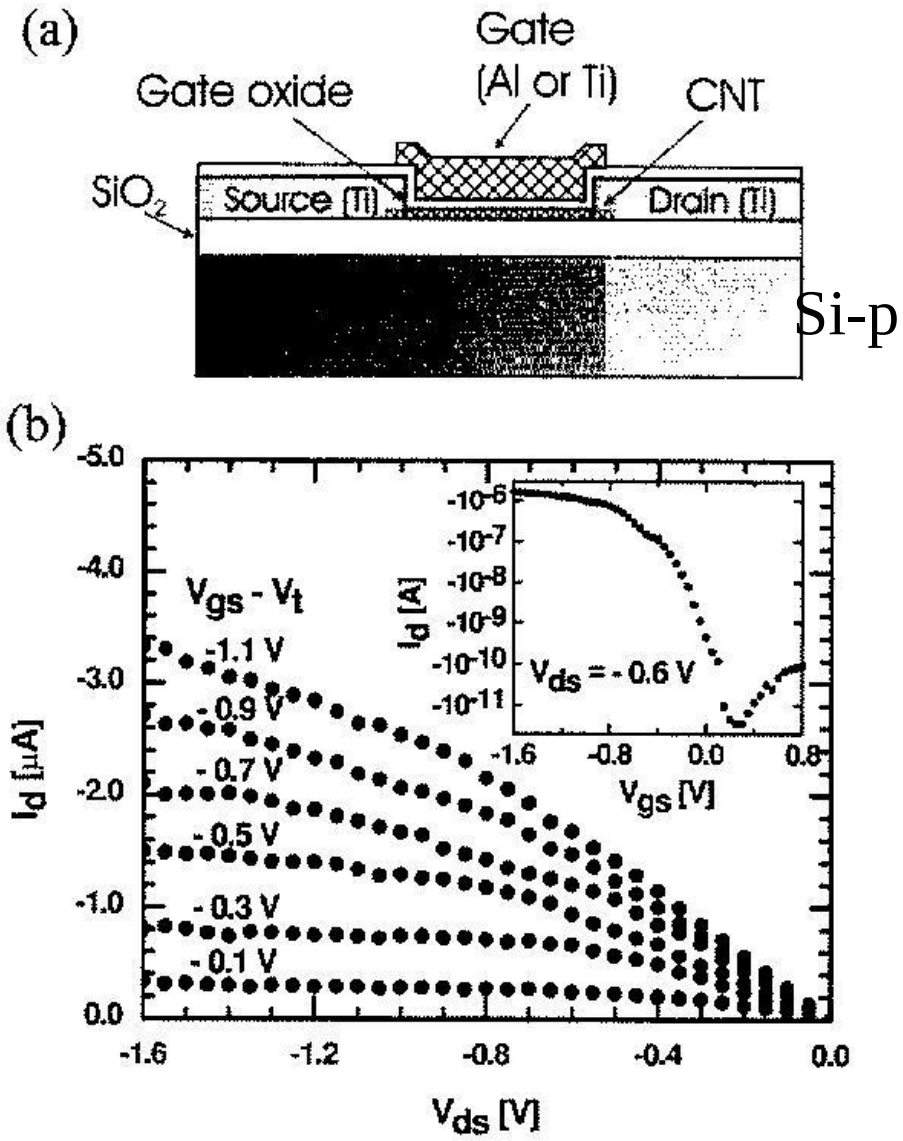
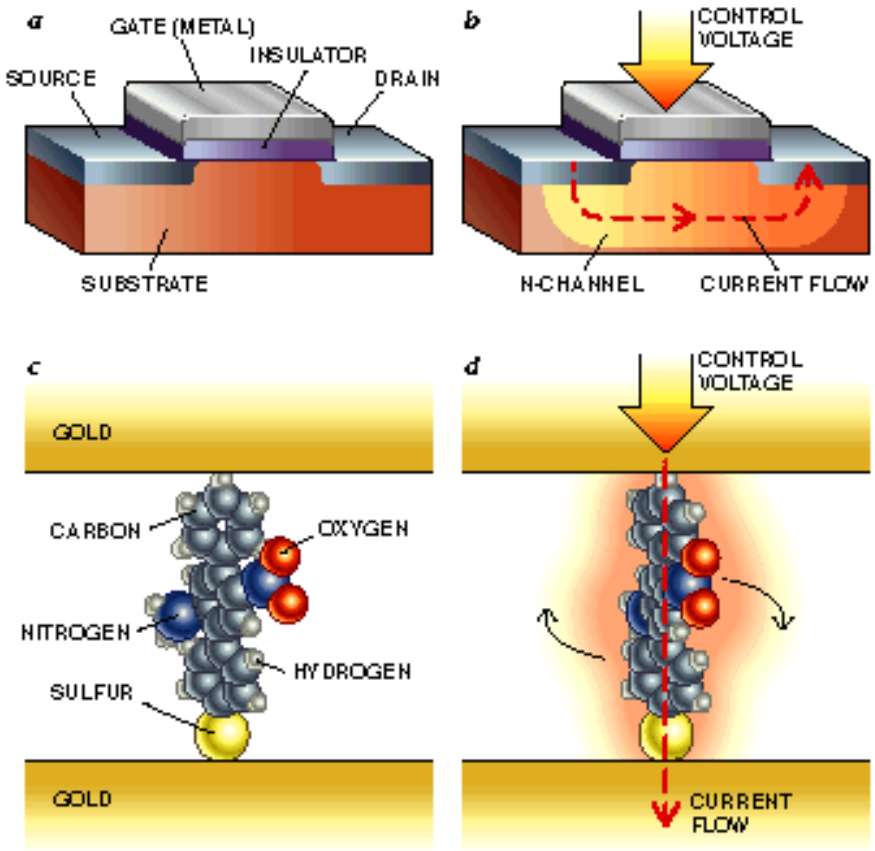


FIG. 1. (a) Schematic cross section of top gate CNFET showing the gate and source and drain electrodes. (b) Output characteristic of a top gate *p*-type CNFET with a Ti gate and a gate oxide thickness of 15 nm. The gate voltage values range from −0.1 to −1.1 V above the threshold voltage which is −0.5 V. Inset: Transfer characteristic of the CNFET for V_{ds} = −0.6 V.

A.P.L, 20/May/2002, p.3817.

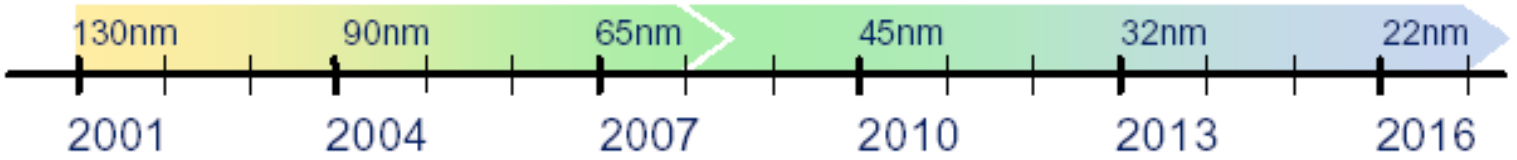
Transistor Molecular



CONVENTIONAL MICROTRANSISTOR (a) has three terminals, known as the source, gate and drain. A positive voltage applied to the gate draws electrons to the insulator (b), enabling current to flow from the source to the drain. A molecule based on three benzene rings (c) was also used to switch an electric current. The center ring had asymmetric fragments, enabling it to be twisted by an electrical field (d). With a specific voltage applied, the electrical field twisted the molecule and permitted current to flow.

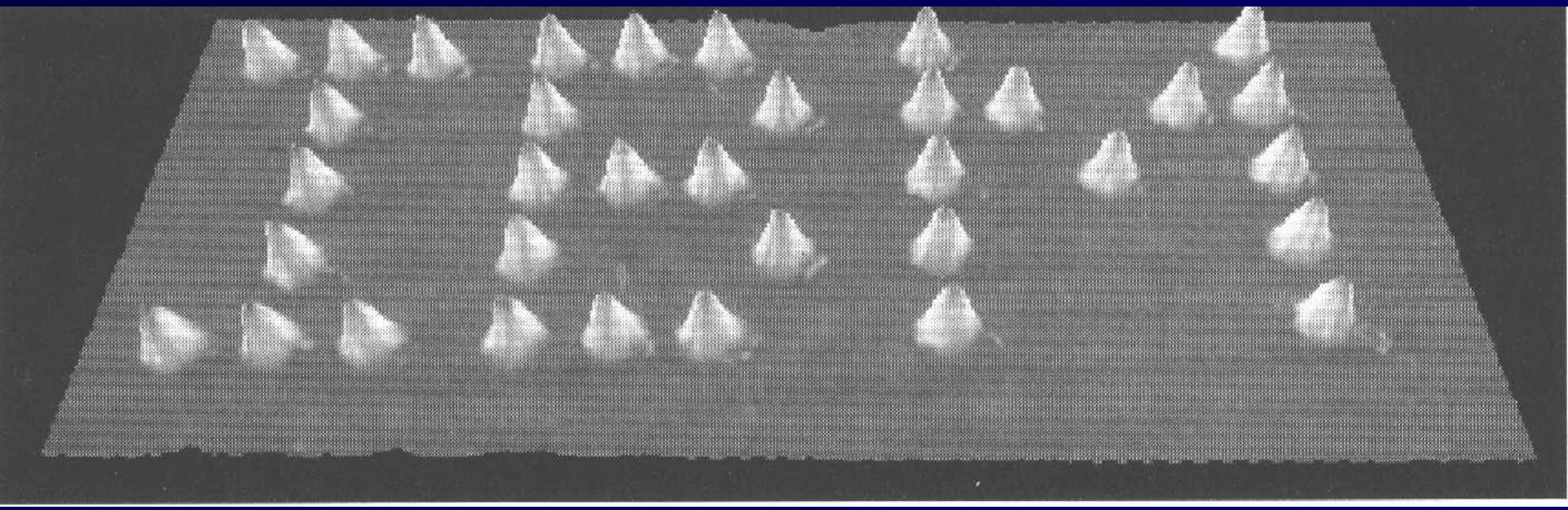
Tecnologias Emergentes

Digital	**Ultra thin CMOS-SOI** **Band engineering: SiGe, strained Si...** **Vertical Transistor** **FinFET** **Double Gate Transistor**
Memory	**Magnetic RAM: Spin Valve** **Magnetic tunnel junction** **Phase change memory (OUM)** **Nano Floating Gate memory** **Single electron memory** **Molecular memory**
Emerging Devices	**Resonant Tunneling Diode FET** **Single electron transistor** **Rapid single quantum flux** **Quantum cellular automata** **Nanotube devices** **Molecular devices**



Já é possível manipulação individual de átomos. Ex.: Xe sobre cristal de Ni (espaço ente átomos ~ 1 nm)

Eigler & Schweizer, Nature 1990.



7. Conclusões

1) Evolução muito rápida

2) Área multidisciplinar. Importância da formação básica

3) Enorme importância econômica

4) É primordial a soma de esforços. Não há espaço para ilhas isoladas, dada a complexidade e multidisciplinaridade.