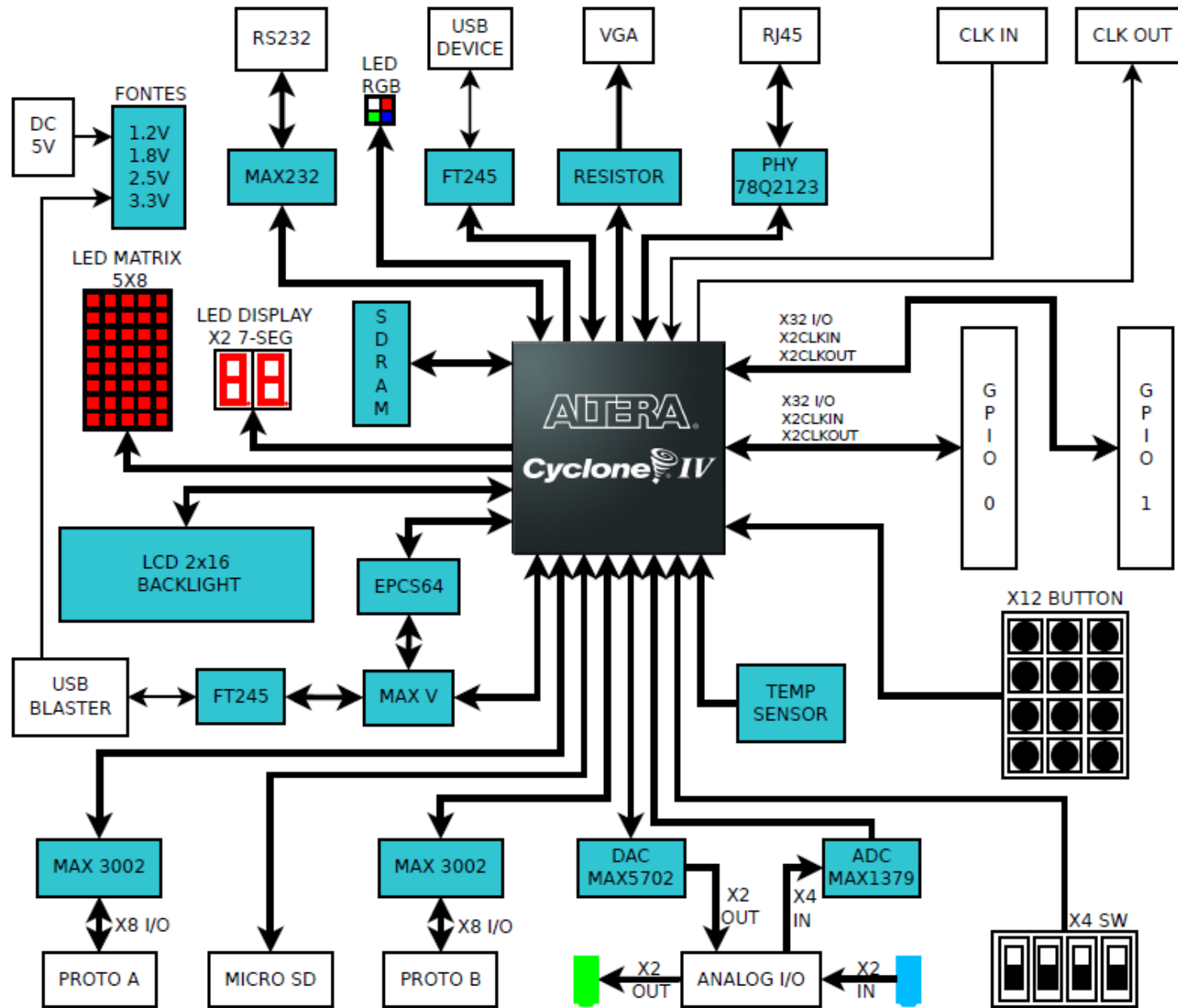


Kit de Desenvolvimento - MercurioIV



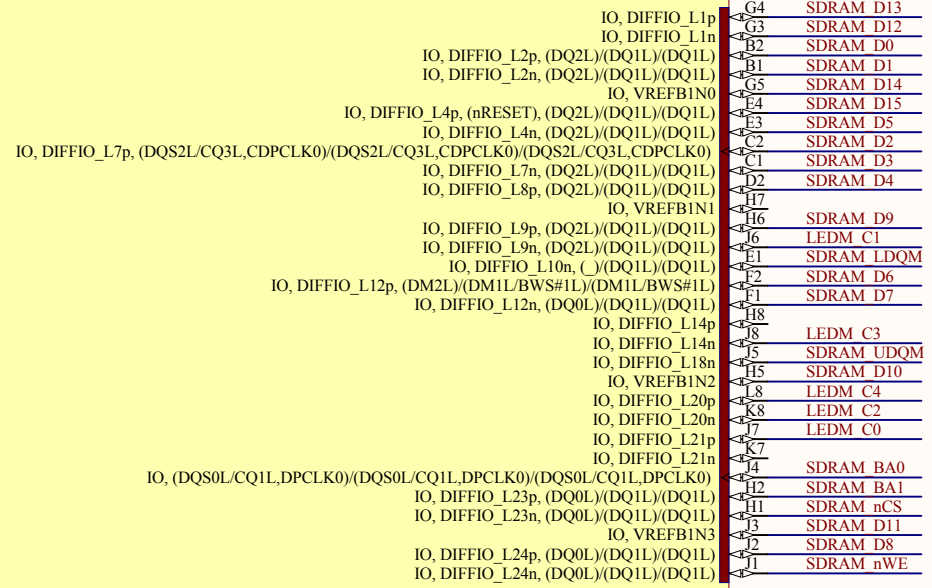
DESCRIÇÃO	FOLHA
Diagrama de Blocos e Sumário	1
FPGA I/O Bancos 1, 2, 3, 4, 5, 6, 7 e 8	2 ~ 9
FPGA Configuração e Clock	10
FPGA Alimentação e Desacoplamento	11
GPIO, PROTO IO, Clock Externo	12
Display LCD e LED, Matriz LED, RGB LED	13
Chaves e Botões	14
SDRAM	15
Porta Ethernet	16
Porta Serial e VGA	17
Porta USB Device e Sdcard	18
Conversor ADC, DAC e Sensor de Temperatura	19
Reguladores de Tensão 1.2V, 1.8V, 2.5V e 3.3V	20
ALTERA USB Blaster	21

LEDm C[4..0]	LEDm C[4..0]
SDRAM BA[1..0]	SDRAM BA[1..0]
SDRAM D[15..0]	SDRAM D[15..0]
SDRAM LDQM	SDRAM LDQM
SDRAM UDQM	SDRAM UDQM
SDRAM nCS	SDRAM nCS
SDRAM nWE	SDRAM nWE

U10A

BANK 1

EP4CE30F23C7



A

A

B


B

C

C

D

D

		Copyright (c) 2011 - DHW Eng. & Rep.	
Title			
Mercurio IV			
Size	Document Number	Rev	
A4	FPGA - BANK 1	2.1	
Date:	20/09/2013	Sheet	2 of 21

DISP0 D[7..0]	DISP0 D[7..0]
DISP1 D[7..0]	DISP1 D[7..0]
LCD D4	LCD D4
LCD D6	LCD D6
PROTO A3	PROTO A3
SDRAM A[12..0]	SDRAM A[12..0]
SDRAM CKE	SDRAM CKE
SDRAM nCAS	SDRAM nCAS
SDRAM nRAS	SDRAM nRAS

U10B

BANK 2

EP4CE30F23C7

IO, DIFFIO_L26p, (DQ0L)/(DQ1L)/(DQ1L)	L6 SDRAM A12
IO, DIFFIO_L26n, (DQ0L)/(DQ1L)/(DQ1L)	M6 DISP1 D4
IO, DIFFIO_L27p, (DQ0L)/(DQ1L)/(DQ1L)	M2 SDRAM A9
IO, DIFFIO_L27n, (DQ0L)/(DQ1L)/(DQ1L)	M1 SDRAM nCAS
IO, DIFFIO_L28p, (DM0L)/(DM1L/BWS#1L)/(DM1L/BWS#1L)	M4 SDRAM A7
IO, DIFFIO_L28n, (DQ1L)/(DQ3L)/(DQ1L)	M3 SDRAM A11
IO, DIFFIO_L29p, (DQ1L)/(DQ3L)/(DQ1L)	M2 SDRAM nRAS
IO, DIFFIO_L29n, (DQ1L)/(DQ3L)/(DQ1L)	N1 SDRAM A8
IO, DIFFIO_L30n	L7
IO, VREFB2N0	M5 SDRAM CKE
IO, DIFFIO_L32p, (DQ1L)/(DQ3L)/(DQ1L)	L2 SDRAM A0
IO, DIFFIO_L32n, (DQ1L)/(DQ3L)/(DQ1L)	P1 SDRAM A10
IO, DIFFIO_L33p, (DQ1L)/(DQ3L)/(DQ1L)	R2 SDRAM A3
IO, DIFFIO_L33n, (DQ1L)/(DQ3L)/(DQ1L)	R1 SDRAM A1
IO, (DQ1L)/(DQ3L)/(DQ1L)	N5 SDRAM A6
IO, DIFFIO_L34p, (DQS1L/CQ1L#,DPCLK1)/(DQS1L/CQ1L#,DPCLK1)/(DQS1L/CQ1L#,DPCLK1)	P4 SDRAM A4
IO, DIFFIO_L34n, (DQ1L)/(DQ3L)/(DQ1L)	P3 SDRAM A2
IO, DIFFIO_L35p, (DM1L/BWS#1L)/(DM3L/BWS#3L)/(DM1L/BWS#1L)	U2 DISP0 D2
IO, DIFFIO_L35n, (DQ3L)/(DQ3L)/(DQ1L)	U1 DISP0 D3
IO, DIFFIO_L38p, (DQ3L)/(DQ3L)/(DQ1L)	V2 DISP0 D0
IO, DIFFIO_L38n, (DQ3L)/(DQ3L)/(DQ1L)	V1 DISP0 D1
IO, VREFB2N1	P5 SDRAM A5
IO, DIFFIO_L41p, (DQ3L)/(DQ3L)/(DQ1L)	N6 DISP1 D6
IO, DIFFIO_L41n	M7
IO, DIFFIO_L42p	M8
IO, DIFFIO_L42n	N8
IO, DIFFIO_L44p, (DQ3L)/(DQ3L)/(DQ1L)	W2 DISP0 D6
IO, DIFFIO_L44n, (DQ3L)/(DQ3L)/(DQ1L)	W1 DISP0 D7
IO, DIFFIO_L45p, (DQ3L)/(DQ3L)/(DQ1L)	V2 DISP0 D4
IO, DIFFIO_L45n, (DQ3L)/(DQ3L)/(DQ1L)	V1 DISP0 D5
IO, VREFB2N2	T3 DISP1 D2
IO, DIFFIO_L49p	N7 DISP1 D5
IO, DIFFIO_L49n	P7
IO, DIFFIO_L50n, (DQ3L)/(DQ3L)/(DQ1L)	AA1 PROTO A3
IO, RUP1	V4 LCD D4
IO, RDN1	V3 LCD D6
IO, DIFFIO_L52p	P6 DISP1 D7
IO, (DM3L/BWS#3L)/(DM3L/BWS#3L)/(DM1L/BWS#1L)	T5 DISP1 D1
IO, (DQS3L/CQ3L#,CDPCLK1)/(DQS3L/CQ3L#,CDPCLK1)/(DQS3L/CQ3L#,CDPCLK1)	T4 DISP1 D3
IO, VREFB2N3	R5 DISP1 D0
IO	R6
IO, DIFFIO_L53p	R7
IO, DIFFIO_L53n	P7

A

A

B


B

C

C

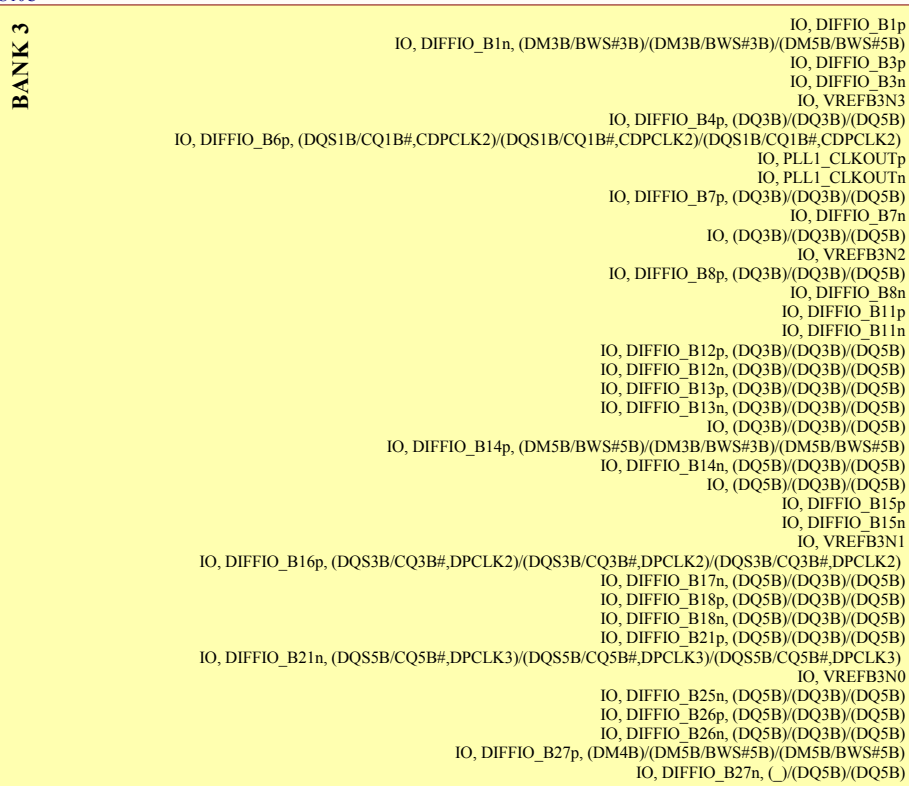
D

D

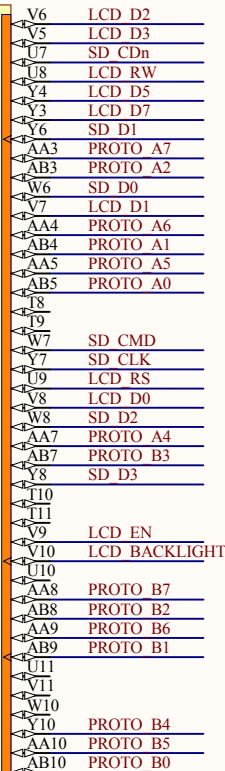
		Copyright (c) 2011 - DHW Eng. & Rep.
Title		
Mercurio IV		
Size	Document Number	Rev
A4	FPGA - BANK 2	2.1
Date:	20/09/2013	Sheet 3 of 21


LCD BACKLIGHT	LCD BACKLIGHT
LCD D5	LCD D5
LCD D7	LCD D7
LCD D[3..0]	LCD D[3..0]
LCD EN	LCD EN
LCD RS	LCD RS
LCD RW	LCD RW
PROTO_A[2..0]	PROTO_A[2..0]
PROTO_A[7..4]	PROTO_A[7..4]
PROTO_B[7..0]	PROTO_B[7..0]
SD CDn	SD CDn
SD CLK	SD CLK
SD CMD	SD CMD
SD D[3..0]	SD D[3..0]

U10C



EP4CE30F23C7



 Engenharia Representação		Copyright (c) 2011 - DHW Eng. & Rep.	
Title Mercurio IV			
Size A4	Document Number FPGA - BANK 3	Rev 2.1	
Date: 20/09/2013	Sheet 4	of 4	Rev 21


ADC CNVST	ADC CNVST
ADC CSn	ADC CSn
ADC DOUT[2..1]	ADC DOUT[2..1]
ADC REFSEL	ADC REFSEL
ADC SCLK	ADC SCLK
ADC SD	ADC SD
ADC SEL	ADC SEL
ADC UB	ADC UB
DAC CLR	DAC CLR
DAC CSn	DAC CSn
DAC DIN	DAC DIN
DAC SCLK	DAC SCLK
GPIO1 D29	GPIO1 D29
GPIO1 D31	GPIO1 D31
I2C OVERTEMPn	I2C OVERTEMPn
KEY3	KEY3
KEY[7..6]	KEY[7..6]
KEY[11..9]	KEY[11..9]

U10D

BANK 4

EP4CE30F23C7

IO, DIFFIO_B28p, (DQ4B)/(DQ5B)/(DQ5B)	AA13
IO, DIFFIO_B28n, (DQ4B)/(DQ5B)/(DQ5B)	AB13
IO, DIFFIO_B29p, (DQ4B)/(DQ5B)/(DQ5B)	AA14 DAC SCLK
IO, DIFFIO_B29n, (DQ4B)/(DQ5B)/(DQ5B)	AB14 DAC DIN
IO, VREFB4N3	V12
IO, DIFFIO_B32p, (DQ4B)/(DQ5B)/(DQ5B)	W13
IO, DIFFIO_B32n, (DQ4B)/(DQ5B)/(DQ5B)	V13
IO, DIFFIO_B33p, (DQ4B)/(DQ5B)/(DQ5B)	AA15 DAC CLR
IO, DIFFIO_B33n, (DQ4B)/(DQ5B)/(DQ5B)	AB15 DAC CSn
IO, DIFFIO_B34p, (DQ4B)/(DQ5B)/(DQ5B)	U12
IO, DIFFIO_B35p, (DM2B)/(DM5B/BWS#5B)/(DM5B/BWS#5B)	AA16 ADC SD
IO, DIFFIO_B35n, (DQ2B)/(DQ5B)/(DQ5B)	AB16 ADC SEL
IO, DIFFIO_B36p	T12
IO, DIFFIO_B36n	T13
IO, (DQS2B/CQ3B,DPCLK5)/(DQS2B/CQ3B,DPCLK5)	V13
IO, VREFB4N2	W14
IO, DIFFIO_B38n	U13
IO, DIFFIO_B39p, (DQ2B)/(DQ5B)/(DQ5B)	V14
IO, DIFFIO_B39n	U14
IO, DIFFIO_B40p	U15
IO, DIFFIO_B40n, (DQ2B)/(DQ5B)/(DQ5B)	V15 KEY6
IO, DIFFIO_B41n, (DQ2B)/(DQ5B)/(DQ5B)	W15 KEY9
IO, DIFFIO_B42p	T14
IO, DIFFIO_B42n, (DQ2B)/(DQ5B)/(DQ5B)	T15
IO, (DQ2B)/(DQ5B)/(DQ5B)	AB18 ADC CNVST
IO, DIFFIO_B43p	AA17 ADC CSn
IO, DIFFIO_B43n	AB17 ADC REFSEL
IO, VREFB4N1	AA18 ADC SCLK
IO, RUP2	AA19 ADC DOUT2
IO, RDN2	AB19 ADC DOUT1
IO, DIFFIO_B48p, (DQ2B)/(DQ5B)/(DQ5B)	V17 KEY7
IO, DIFFIO_B48n, (DQS0B/CQ1B,CDPCLK3)/(DQS0B/CQ1B,CDPCLK3)	Y17 KEY11
IO, DIFFIO_B49p, (DQ5B)/(DQ5B)	AA20 I2C OVERTEMPn
IO, DIFFIO_B49n, (DQ2B)/(DQ5B)/(DQ5B)	AB20 ADC UB
IO, VREFB4N0	V16
IO, DIFFIO_B50p	U16 KEY3
IO, DIFFIO_B50n	U17 KEY10
IO, PLL4_CLKOUTp	T16 GPIO1 D31
IO, PLL4_CLKOUTn	R16 GPIO1 D29
IO, DIFFIO_B52p	R14
IO, DIFFIO_B52n	R15

		Copyright (c) 2011 - DHW Eng. & Rep.
Title		
Mercurio IV		
Size	Document Number	Rev
A4	FPGA - BANK 4	2.1
Date:	20/09/2013	Sheet 5 of 21

GPIO0_CLKOUT1	GPIO0_CLKOUT1
GPIO0_D15	GPIO0_D15
GPIO0_D[20..17]	GPIO0_D[20..17]
GPIO0_D[31..22]	GPIO0_D[31..22]
GPIO1_D30	GPIO1_D30
GPIO1_D[28..24]	GPIO1_D[28..24]
I2C_SCL	I2C_SCL
I2C_SDA	I2C_SDA
KEY8	KEY8
KEY[2..0]	KEY[2..0]
KEY[5..4]	KEY[5..4]
SW[3..0]	SW[3..0]


U10E

BANK 5

EP4CE30F23C7

IO, DIFFIO_R56p, (DM3R/BWS#3R)/(DM3R/BWS#3R)/(DM1R/BWS#1R)
 IO, RUP3
 IO, RDN3
 IO, (DQS3R/CQ3R#,CDPCLK4)/(DQS3R/CQ3R#,CDPCLK4)/(DQS3R/CQ3R#,CDPCLK4)
 IO, VREFB5N3
 IO, DIFFIO_R51n, (DQ3R)/(DQ3R)/(DQ1R)
 IO, DIFFIO_R51p
 IO, DIFFIO_R50n, (DQ3R)/(DQ3R)/(DQ1R)
 IO, DIFFIO_R50p
 IO, DIFFIO_R49n, (DQ3R)/(DQ3R)/(DQ1R)
 IO, DIFFIO_R49p, (DQ3R)/(DQ3R)/(DQ1R)
 IO, DIFFIO_R46n
 IO, DIFFIO_R46p
 IO, VREFB5N2
 IO
 IO, DIFFIO_R45n, (DQ3R)/(DQ3R)/(DQ1R)
 IO, DIFFIO_R45p, (DQ3R)/(DQ3R)/(DQ1R)
 IO, DIFFIO_R44n, (DQ3R)/(DQ3R)/(DQ1R)
 IO, DIFFIO_R43n, (DQ3R)/(DQ3R)/(DQ1R)
 IO, DIFFIO_R43p, (DQ3R)/(DQ3R)/(DQ1R)
 IO, DIFFIO_R42n
 IO, DIFFIO_R42p, (DM1R/BWS#1R)/(DM3R/BWS#3R)/(DM1R/BWS#1R)
 IO, DIFFIO_R40p
 IO, DIFFIO_R39n, (DQ1R)/(DQ3R)/(DQ1R)
 IO, DIFFIO_R39p, (DQ1R)/(DQ3R)/(DQ1R)
 IO, VREFB5N1
 IO, DIFFIO_R38n, (DQ1R)/(DQ3R)/(DQ1R)
 IO, DIFFIO_R38p, (DQ1R)/(DQ3R)/(DQ1R)
 IO, DIFFIO_R36n, (DQ1R)/(DQ3R)/(DQ1R)
 IO, DIFFIO_R36p
 IO, DIFFIO_R33n
 IO, DIFFIO_R33p, (DQS1R/CQ1R#,DPCLK6)/(DQS1R/CQ1R#,DPCLK6)/(DQS1R/CQ1R#,DPCLK6)
 IO, DIFFIO_R32n, (DEV_OE)
 IO, DIFFIO_R32p, (DEV_CLRn)
 IO, DIFFIO_R31n, (DQ1R)/(DQ3R)/(DQ1R)
 IO, DIFFIO_R31p, (DQ1R)/(DQ3R)/(DQ1R)
 IO, DIFFIO_R30n, (DQ1R)/(DQ3R)/(DQ1R)
 IO, DIFFIO_R30p, (DQ1R)/(DQ3R)/(DQ1R)
 IO, VREFB5N0

AA21	I2C_SCL
T17	GPIO1_D30
T18	GPIO0_D31
W20	KEY4
W19	KEY8
Y22	SW3
Y21	I2C_SDA
U20	KEY1
U19	
W22	SW1
W21	SW2
P15	
P16	
R17	GPIO1_D27
P17	GPIO1_D25
V22	KEY0
V21	SW0
R20	GPIO1_D28
U22	KEY2
U21	KEY5
R18	GPIO0_D30
R19	GPIO0_D27
N16	
R22	GPIO0_D28
R21	GPIO0_D29
P20	GPIO1_D26
P22	GPIO0_D24
P21	GPIO0_D25
N20	GPIO0_D22
N19	GPIO0_D23
N17	
N18	GPIO0_D26
N22	GPIO0_D18
N21	GPIO0_D19
M22	GPIO0_CLKOUT1
M21	GPIO0_D15
M20	GPIO0_D20
M19	GPIO0_D17
M16	GPIO1_D24

		Copyright (c) 2011 - DHW Eng. & Rep.	
Title Mercurio IV			
Size A4	Document Number FPGA - BANK 5	Rev 2.1	
Date: 20/09/2013	Sheet 6	of 21	


ETH COL	ETH COL
ETH CRS	ETH CRS
ETH RXCLK	ETH RXCLK
ETH RXER	ETH RXER
ETH TXCLK	ETH TXCLK
ETH TXD[3..0]	ETH TXD[3..0]
ETH TXEN	ETH TXEN
ETH TXER	ETH TXER
GPIO0_CLKOUT0	GPIO0_CLKOUT0
GPIO0_D1	GPIO0_D1
GPIO0_D16	GPIO0_D16
GPIO0_D21	GPIO0_D21
GPIO0_D[14..3]	GPIO0_D[14..3]
GPIO1_D15	GPIO1_D15
GPIO1_D15	GPIO1_D15
GPIO1_D23	GPIO1_D23
GPIO1_D[21..17]	GPIO1_D[21..17]

U10F

BANK 6

EP4CE30F23C7

IO, DIFFIO_R27n, (INIT_DONE)	L22	GPIO0_D12
IO, DIFFIO_R27p, (CRC_ERROR)	L21	GPIO0_D13
IO, VREFB6N3	K19	GPIO0_D16
IO, DIFFIO_R24n, (nCEO)	K22	
IO, DIFFIO_R24p, (CLKUSR)	K21	GPIO0_D9
IO, DIFFIO_R23n, (DQS0R/CQ1R,DPCLK7)/(DQS0R/CQ1R,DPCLK7)	F22	GPIO0_D5
IO, DIFFIO_R23p, (DM0R)/(DM1R/BWS#1R)/(DM1R/BWS#1R)	F21	GPIO0_D8
IO, DIFFIO_R22n, (DQ0R)/(DQ1R)/(DQ1R)	H22	GPIO0_D1
IO, DIFFIO_R22p, (DQ0R)/(DQ1R)/(DQ1R)	H21	GPIO0_D4
IO, DIFFIO_R20n	K17	GPIO0_D21
IO, DIFFIO_R20p, (DQ0R)/(DQ1R)/(DQ1R)	K18	GPIO0_CLKOUT0
IO, VREFB6N2	F18	GPIO0_D14
IO, DIFFIO_R18n, (DQ0R)/(DQ1R)/(DQ1R)	F22	ETH_COL
IO, DIFFIO_R18p, (DQ0R)/(DQ1R)/(DQ1R)	F21	ETH_CRS
IO, DIFFIO_R13n, (DQ0R)/(DQ1R)/(DQ1R)	H20	GPIO0_D10
IO, DIFFIO_R13p, (DQ0R)/(DQ1R)/(DQ1R)	H19	GPIO0_D7
IO, DIFFIO_R12n, (nWE), (DQ0R)/(DQ1R)/(DQ1R)	F22	ETH_TXD3
IO, DIFFIO_R12p, (nOE), (DQ0R)/(DQ1R)/(DQ1R)	F21	ETH_TXD2
IO, VREFB6N1	H18	GPIO0_D11
IO, DIFFIO_R10n	F17	GPIO1_D23
IO, DIFFIO_R10p	H16	GPIO1_D21
IO, DIFFIO_R9n, (DM2R)/(DM1R/BWS#1R)/(DM1R/BWS#1R)	D22	ETH_TXD1
IO, DIFFIO_R9p, (DQ1R)/(DQ1R)	D21	ETH_TXD0
IO, DIFFIO_R8n, (nAVD), (DQ2R)/(DQ1R)/(DQ1R)	F20	GPIO0_D6
IO, DIFFIO_R8p, (DQ2R)/(DQ1R)/(DQ1R)	F19	GPIO0_D3
IO, DIFFIO_R7n, (PADD23), (DQ2R)/(DQ1R)/(DQ1R)	G18	GPIO1_D18
IO, DIFFIO_R7p	H17	GPIO1_D20
IO, DIFFIO_R6n, (DQ2R)/(DQ1R)/(DQ1R)	C22	ETH_TXEN
IO, DIFFIO_R6p, (DQ2R)/(DQ1R)/(DQ1R)	C21	ETH_TXCLK
IO, DIFFIO_R5n, (PADD22), (DQ2R)/(DQ1R)/(DQ1R)	B22	ETH_TXER
IO, DIFFIO_R5p, (PADD21), (DQ2R)/(DQ1R)/(DQ1R)	B21	ETH_RXER
IO, DIFFIO_R4n, (PADD20), (DQS2R/CQ3R,CDPCLK5)/(DQS2R/CQ3R,CDPCLK5)	C20	ETH_RXCLK
IO, VREFB6N0	D20	GPIO1_D15
IO, DIFFIO_R2n, (DQ2R)/(DQ1R)/(DQ1R)	F17	GPIO1_D17
IO, DIFFIO_R2p	G17	GPIO1_D19

 Engenharia Representação		Copyright (c) 2011 - DHW Eng. & Rep.
Title Mercurio IV		
Size A4	Document Number FPGA - BANK 6	Rev 2.1
Date: 20/09/2013	Sheet 7 of 21	


ETH MDC	ETH MDC
ETH MDIO	ETH MDIO
ETH RXDV	ETH RXDV
ETH RXD[3..0]	ETH RXD[3..0]
GPIO0 D0	GPIO0 D0
GPIO0 D2	GPIO0 D2
GPIO1 CLKOUT[1..0]	GPIO1 CLKOUT[1..0]
GPIO1 D16	GPIO1 D16
GPIO1 D16	GPIO1 D22
GPIO1 D22	GPIO1 D[14..0]
GPIO1 D[14..0]	VGA B[3..0]
VGA B[3..0]	VGA G[3..0]
VGA G[3..0]	VGA HS
VGA HS	VGA VS
VGA VS	

U10G

BANK 7

EP4CE30F23C7

IO, DIFFIO_T51n	F16	GPIO0 D2
IO, DIFFIO_T51p, (DQ2T)/(DQ5T)/(DQ5T)	F16	GPIO0 D0
IO, DIFFIO_T50n, (DQ2T)/(DQ5T)/(DQ5T)	F15	GPIO1 CLKOUT0
IO, DIFFIO_T50p	G16	GPIO1 D22
IO, DIFFIO_T49n	G15	GPIO1 D16
IO, DIFFIO_T49p, (DQS0T/CQ1T,CDPCLK6)/(DQS0T/CQ1T,CDPCLK6)/(DQS0T/CQ1T,CDPCLK6)	F14	GPIO1 D7
IO, DIFFIO_T48n	F15	
IO, DIFFIO_T48p	H14	
IO, VREFB7N0	D17	GPIO1 D13
IO, DIFFIO_T47n, (DQ2T)/(DQ5T)/(DQ5T)	C19	GPIO1 D14
IO, DIFFIO_T47p, (DQ2T)/(DQ5T)/(DQ5T)	D19	GPIO1 CLKOUT1
IO, PLL2_CLKOUTn	A20	ETH RXD0
IO, PLL2_CLKOUTp	B20	ETH RXDV
IO, DIFFIO_T46p, (DQ2T)/(DQ5T)/(DQ5T)	C17	GPIO1 D12
IO, RUP4	B19	ETH RXD1
IO, RDN4	A19	ETH RXD2
IO, DIFFIO_T45n, (DQ2T)/(DQ5T)/(DQ5T)	A18	ETH MDC
IO, DIFFIO_T45p, (PADD0)	B18	ETH RXD3
IO, VREFB7N1	D15	GPIO1 D10
IO, DIFFIO_T44n, (DQ2T)/(DQ5T)/(DQ5T)	F15	GPIO1 D11
IO, DIFFIO_T44p	G14	
IO, DIFFIO_T42n	G13	GPIO1 D6
IO, DIFFIO_T41n, (PADD1), (DQ2T)/(DQ5T)/(DQ5T)	A17	VGA VS
IO, DIFFIO_T41p, (PADD2), (DQ2T)/(DQ5T)/(DQ5T)	B17	ETH MDIO
IO, DIFFIO_T40n, (DM2T)/(DM5T/BWS#5T)/(DM5T/BWS#5T)	A16	VGA B3
IO, DIFFIO_T40p, (DQ4T)/(DQ5T)/(DQ5T)	B16	VGA HS
IO, VREFB7N2	C15	GPIO1 D9
IO, DIFFIO_T38n, (PADD3), (DQ4T)/(DQ5T)/(DQ5T)	E14	GPIO1 D8
IO, DIFFIO_T38p, (PADD4), (DQS2T/CQ3T,DPCLK8)/(DQS2T/CQ3T,DPCLK8)/(DQS2T/CQ3T,DPCLK8)	F13	GPIO1 D5
IO, DIFFIO_T36n, (PADD5), (DQ4T)/(DQ5T)/(DQ5T)	A15	VGA B1
IO, DIFFIO_T36p, (PADD6), (DQ4T)/(DQ5T)/(DQ5T)	B15	VGA B2
IO, DIFFIO_T35n, (PADD7)	C13	VGA G0
IO, DIFFIO_T35p, (PADD8), (DQ4T)/(DQ5T)/(DQ5T)	D13	GPIO1 D3
IO, VREFB7N3	F13	GPIO1 D4
IO, DIFFIO_T31n, (PADD9), (DQ4T)/(DQ5T)/(DQ5T)	A14	VGA G3
IO, DIFFIO_T31p, (PADD10), (DQ4T)/(DQ5T)/(DQ5T)	B14	VGA B0
IO, DIFFIO_T29n, (PADD11), (DQ4T)/(DQ5T)/(DQ5T)	A13	VGA G1
IO, DIFFIO_T29p, (PADD12), (DQS4T/CQ5T,DPCLK9)/(DQS4T/CQ5T,DPCLK9)/(DQS4T/CQ5T,DPCLK9)	B13	VGA G2
IO, DIFFIO_T28p, (DQ2T)/(DQ5T)/(DQ5T)	F12	GPIO1 D2
IO, DIFFIO_T27n, (PADD13)	F11	GPIO1 D0
IO, DIFFIO_T27p, (PADD14), (DM4T)/(DM5T/BWS#5T)/(DM5T/BWS#5T)	F11	GPIO1 D1

		Copyright (c) 2011 - DHW Eng. & Rep.
Title <h2 style="text-align: center;">Mercurio IV</h2>		
Size	Document Number	Rev
A4	FPGA - BANK 7	2.1
Date:	20/09/2013	Sheet 8 of 21

ETH_RSTn	ETH_RSTn
LEDM_R[7..0]	LEDM_R[7..0]
LED_B	LED_B
LED_G	LED_G
LED_R	LED_R
SDRAM_CLK	SDRAM_CLK
SMA_CLKOUT	SMA_CLKOUT
UART_CTS	UART_CTS
UART_RTS	UART_RTS
UART_RXD	UART_RXD
UART_TXD	UART_TXD
USB_D[7..0]	USB_D[7..0]
USB_PWRENn	USB_PWRENn
USB_RD	USB_RD
USB_RXFn	USB_RXFn
USB_TXEn	USB_TXEn
USB_WR	USB_WR
VGA_R[3..0]	VGA_R[3..0]


U10H

BANK 8

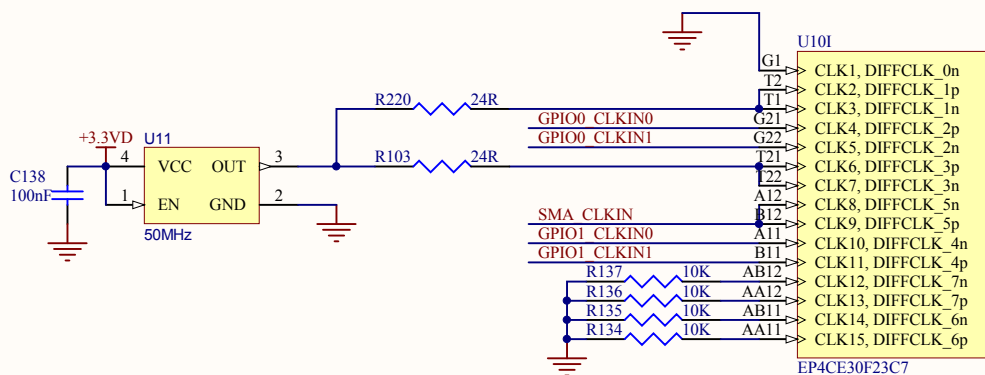
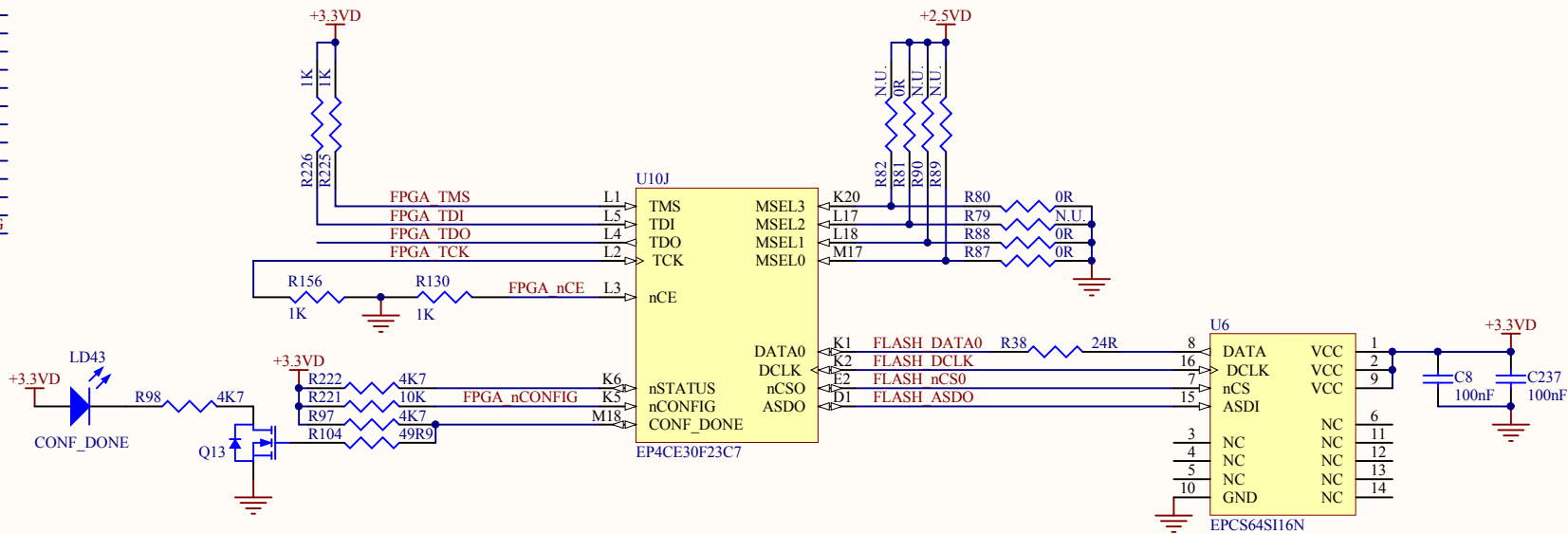
IO, DIFFIO_T26n, (DQ5T)/(DQ3T)/(DQ5T)
 IO, DIFFIO_T26p
 IO, DIFFIO_T25n, (DQ5T)/(DQ3T)/(DQ5T)
 IO, DIFFIO_T25p, (PADD15)
 IO, DIFFIO_T24n, (PADD16), (DQ5T)/(DQ3T)/(DQ5T)
 IO, DIFFIO_T24p, (PADD17), (DQS5T/CQ5T#,DPCLK10)/(DQS5T/CQ5T#,DPCLK10)/(DQS5T/CQ5T#,DPCLK10)
 IO, VREFB8N0
 IO, DIFFIO_T22n
 IO, DIFFIO_T20n, (DATA2), (DQ5T)/(DQ3T)/(DQ5T)
 IO, DIFFIO_T20p, (DATA3), (DQ5T)/(DQ3T)/(DQ5T)
 IO, DIFFIO_T19n, (PADD18), (DQ5T)/(DQ3T)/(DQ5T)
 IO, DIFFIO_T19p, (DATA4), (DQ5T)/(DQ3T)/(DQ5T)
 IO, DIFFIO_T18n, (PADD19), (DQ5T)/(DQ3T)/(DQ5T)
 IO, DIFFIO_T18p, (DATA15), (DQ5T)/(DQ3T)/(DQ5T)
 IO, VREFB8N1
 IO, DIFFIO_T16n, (DATA14), (DQS3T/CQ3T#,DPCLK11)/(DQS3T/CQ3T#,DPCLK11)/(DQS3T/CQ3T#,DPCLK11)
 IO, DIFFIO_T16p, (DATA13), (DM5T/BWS#5T)/(DM3T/BWS#3T)/(DM5T/BWS#5T)
 IO, DIFFIO_T14n
 IO, DIFFIO_T14p
 IO, DIFFIO_T11p, (DATA5), (DQ3T)/(DQ3T)/(DQ5T)
 IO, VREFB8N2
 IO, DIFFIO_T8n
 IO, DIFFIO_T8p, (DATA6), (DQ3T)/(DQ3T)/(DQ5T)
 IO, DIFFIO_T7n, (DATA7), (DQ3T)/(DQ3T)/(DQ5T)
 IO, DIFFIO_T7p
 IO, DIFFIO_T6n, (DQ3T)/(DQ3T)/(DQ5T)
 IO, DIFFIO_T6p, (DATA8), (DQ3T)/(DQ3T)/(DQ5T)
 IO, DIFFIO_T5n, (DATA9), (DQ3T)/(DQ3T)/(DQ5T)
 IO, DIFFIO_T5p
 IO, DIFFIO_T4n, (DATA10), (DQ3T)/(DQ3T)/(DQ5T)
 IO, DIFFIO_T4p, (DATA11), (DQ3T)/(DQ3T)/(DQ5T)
 IO, VREFB8N3
 IO
 IO, DIFFIO_T3n, (DQ3T)/(DQ3T)/(DQ5T)
 IO, DIFFIO_T3p, (DATA12), (DQS1T/CQ1T#,CDPCLK7)/(DQS1T/CQ1T#,CDPCLK7)/(DQS1T/CQ1T#,CDPCLK7)
 IO, DIFFIO_T1n, (DM3T/BWS#3T)/(DM3T/BWS#3T)/(DM5T/BWS#5T)
 IO, DIFFIO_T1p
 IO
 IO, PLL3_CLKOUTn
 IO, PLL3_CLKOUTp
 IO


D10
 F10
 A10 VGA_R2
 B10 VGA_R3
 A9 VGA_R0
 B9 USB_WR
 C10 VGA_R1
 G11 ETH_RSTn
 A8 USB_RD
 B8 USB_PWRENn
 A7 USB_D3
 B7 USB_D6
 A6 USB_D5
 B6 USB_D7
 F9 LEDM_R2
 C8 LEDM_R1
 C7 UART_CTS
 H11 LEDM_R7
 H10
 A5 USB_D1
 B5 USB_D2
 G10
 F10 LEDM_R0
 C6 UART_RTS
 D7 LED_R
 A4 USB_D4
 B4 USB_D0
 F8 LEDM_R5
 G8 LEDM_R6
 A3 USB_RXFn
 B3 USB_TXEn
 D6 LED_G
 E7 LED_B
 C3 UART_RXD
 C4 UART_TXD
 F7
 G7
 F9 LEDM_R4
 E6 SMA_CLKOUT
 E5 SDRAM_CLK
 G9 LEDM_R3

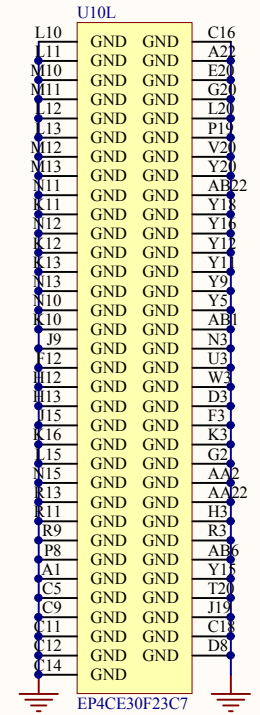
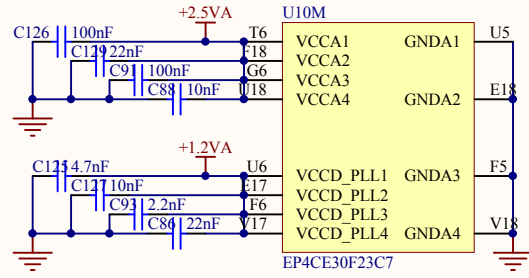
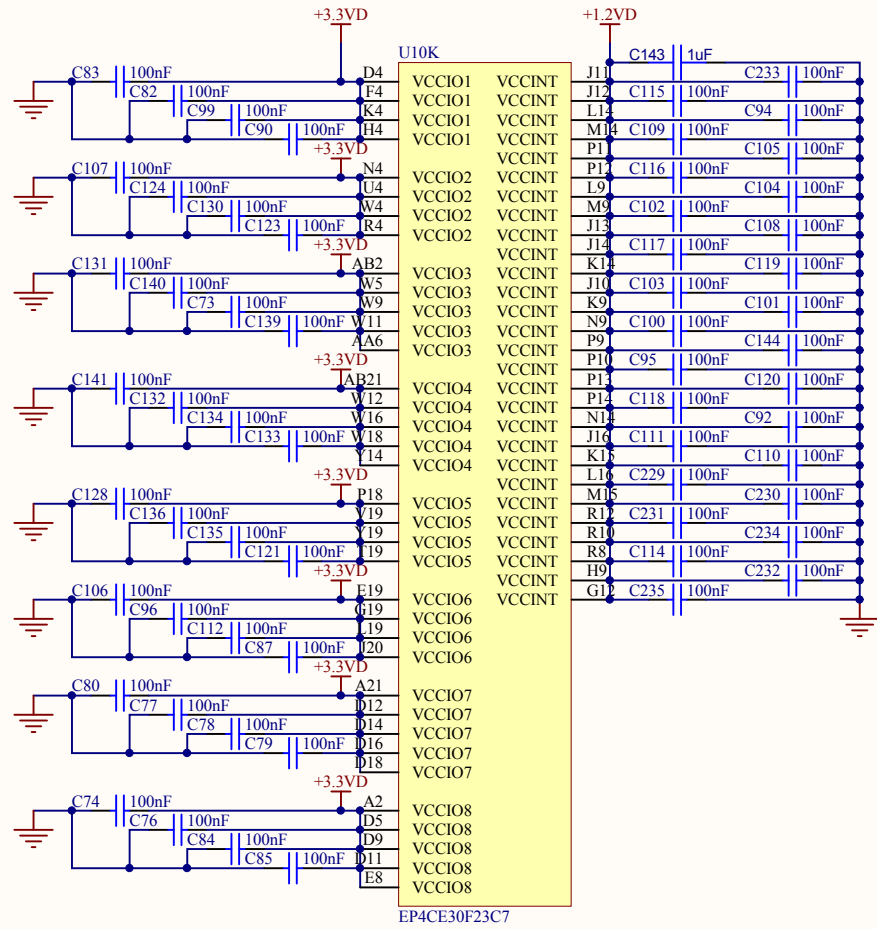
EP4CE30F23C7

 Engenharia Representação		Copyright (c) 2011 - DHW Eng. & Rep.
Title Mercurio IV		
Size A4	Document Number FPGA - BANK 8	Rev 2.1
Date: 20/09/2013	Sheet 9	of 21

GPIO0_CLKIN0	GPIO0_CLKIN0
GPIO0_CLKIN1	GPIO0_CLKIN1
GPIO1_CLKIN0	GPIO1_CLKIN0
GPIO1_CLKIN1	GPIO1_CLKIN1
SMA_CLKIN	SMA_CLKIN
FPGA_TCK	FPGA_TCK
FPGA_TDI	FPGA_TDI
FPGA_TDO	FPGA_TDO
FPGA_TMS	FPGA_TMS
FLASH_ASDO	FLASH_ASDO
FLASH_DATA0	FLASH_DATA0
FLASH_DCLK	FLASH_DCLK
FLASH_nCS0	FLASH_nCS0
FPGA_nCE	FPGA_nCE
FPGA_nCONFIG	FPGA_nCONFIG



 Engenharia 1 Representação		Copyright (c) 2011 - DHW Eng. & Rep.	
Mercurio IV			
Size	Document Number	Rev	
A4	FPGA CONFIG - CLOCK - FLASH	2.1	
Date:	20/09/2013	Sheet	10 of 21

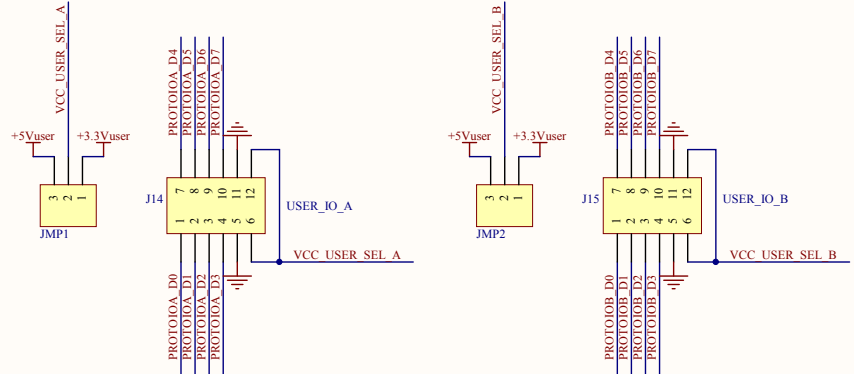
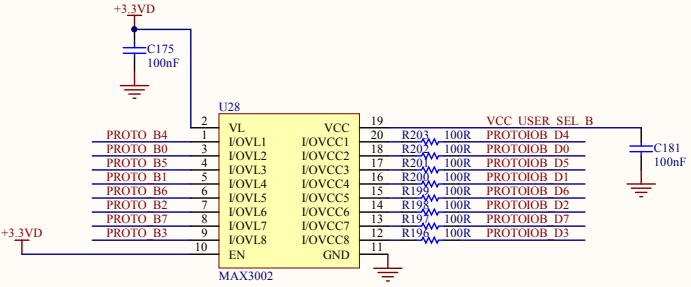
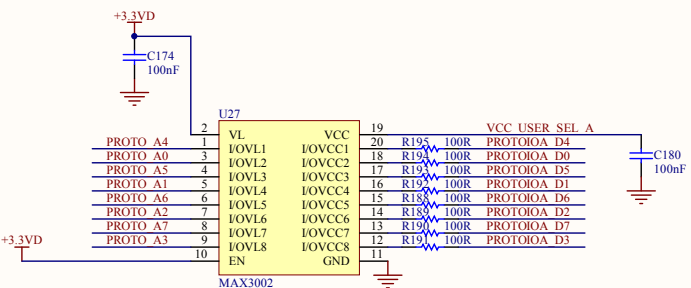
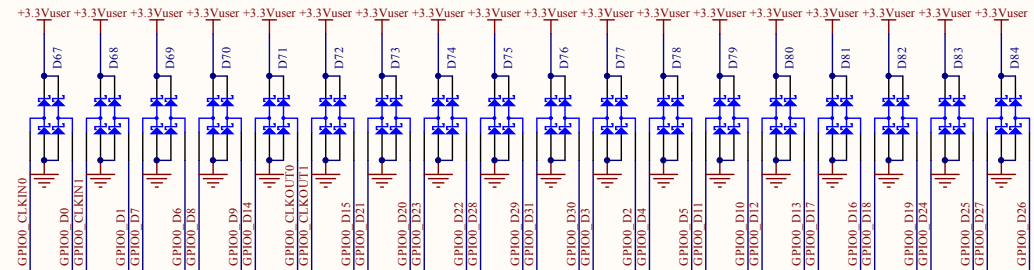
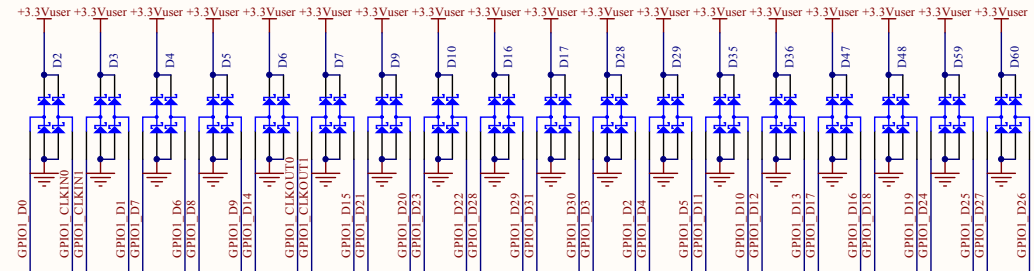
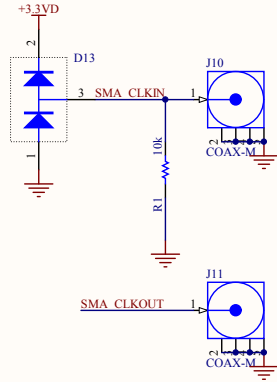
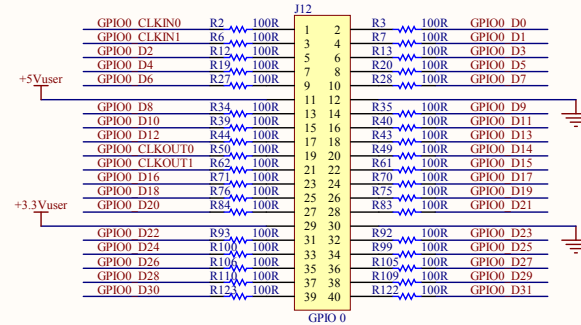
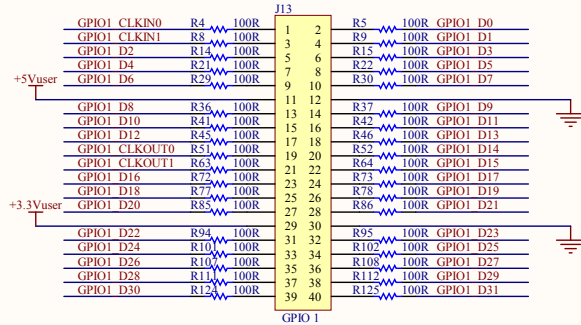


dhw Engenharia e Representação
Copyright (c) 2011 - DHW Eng. & Rep.

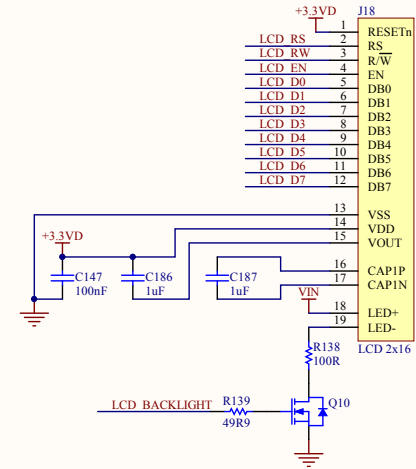
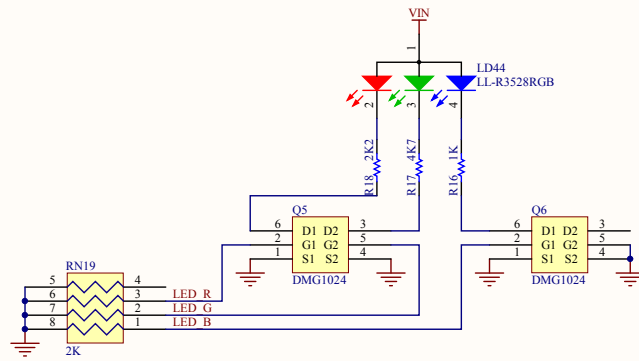
Title: **Mercurio IV**

Size: A4	Document Number: FPGA POWER	Rev: 2.1
Date: 20/09/2013	Sheet: 11 of 21	

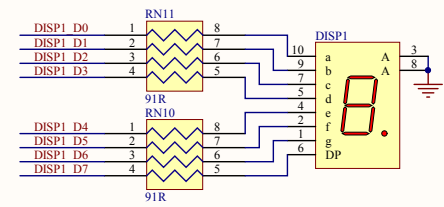
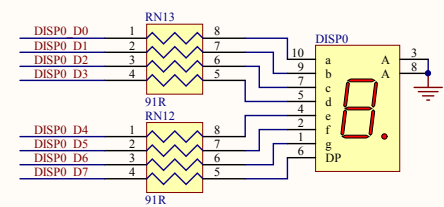
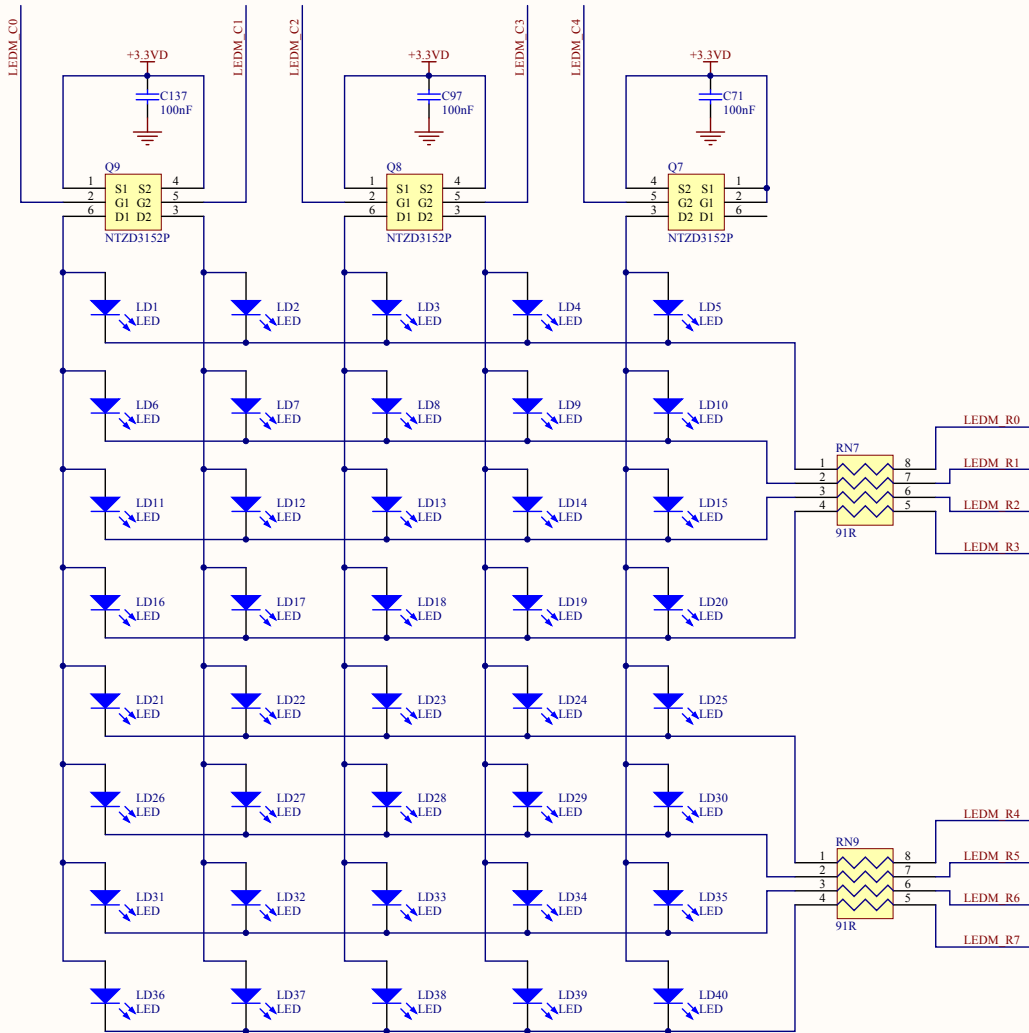
GPIO0_CLKIN[1..0]	GPIO0_CLKIN[1..0]
GPIO0_CLKOUT[1..0]	GPIO0_CLKOUT[1..0]
GPIO0_D[31..0]	GPIO0_D[31..0]
GPIO1_CLKIN[1..0]	GPIO1_CLKIN[1..0]
GPIO1_CLKOUT[1..0]	GPIO1_CLKOUT[1..0]
GPIO1_D[31..0]	GPIO1_D[31..0]
PROTO_A[0..7]	PROTO_A[0..7]
PROTO_B[0..7]	PROTO_B[0..7]
SMA_CLKIN	SMA_CLKIN
SMA_CLKOUT	SMA_CLKOUT



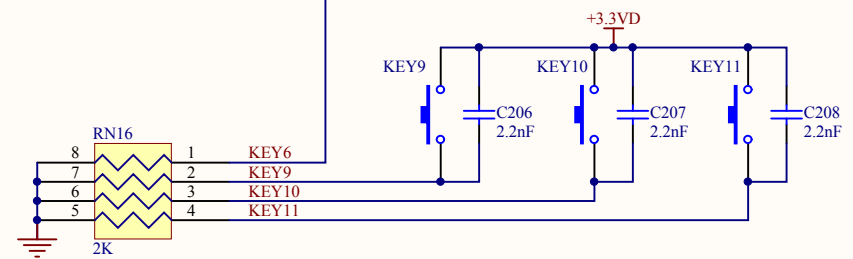
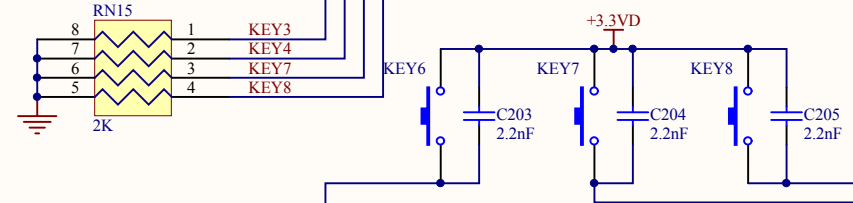
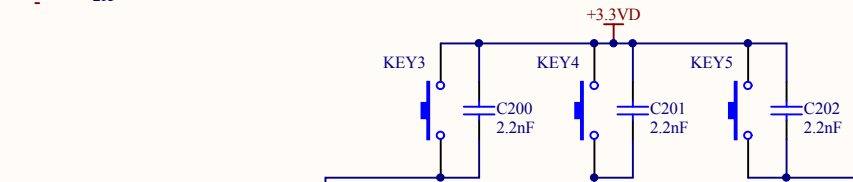
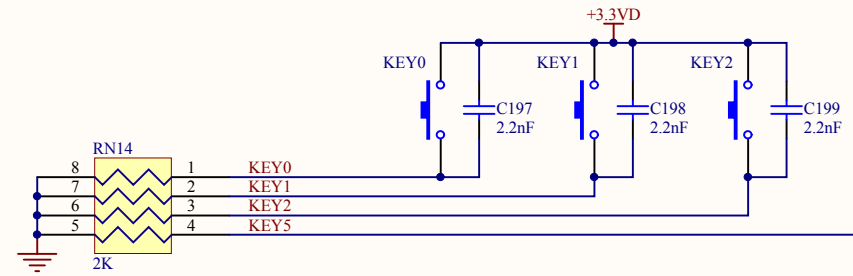
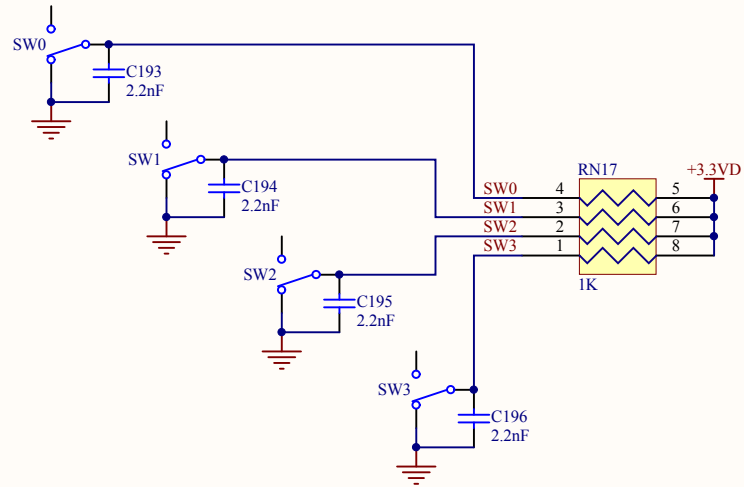
DISP0 D[0..7]	DISP0 D[0..7]
DISP1 D[0..7]	DISP1 D[0..7]
LCD BACKLIGHT	LCD BACKLIGHT
LCD D[0..7]	LCD D[0..7]
LCD EN	LCD EN
LCD RS	LCD RS
LCD RW	LCD RW
LEDM C[0..4]	LEDM C[0..4]
LEDM R[0..7]	LEDM R[0..7]
LED B	LED B
LED G	LED G
LED R	LED R




+3.3VD	J18
LCD RS	RESETn
LCD RW	RS
LCD EN	R/W
LCD D0	EN
LCD D1	DB0
LCD D2	DB1
LCD D3	DB2
LCD D4	DB3
LCD D5	DB4
LCD D6	DB5
LCD D7	DB6
	DB7
	VSS
	VDD
	VOUT
	CAP1P
	CAP1N
	VIN
	LED+
	LED-
	LCD 2x16

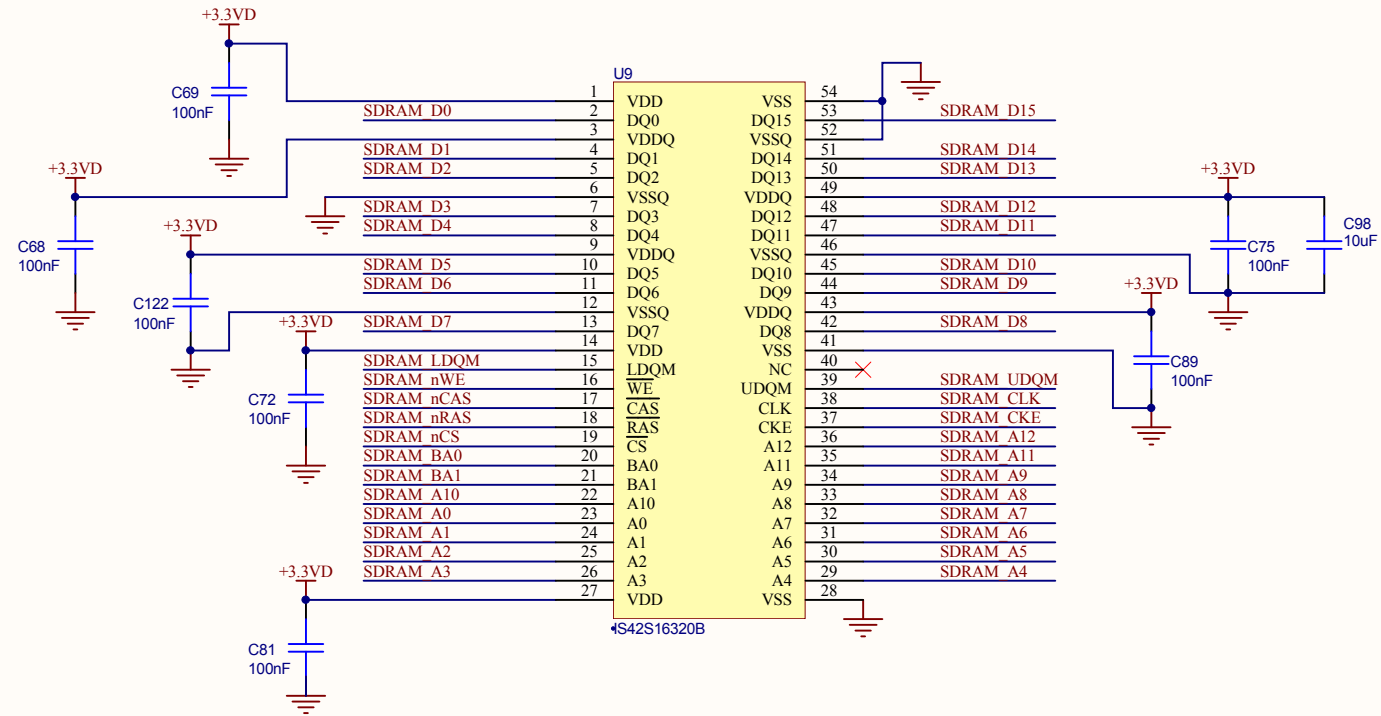
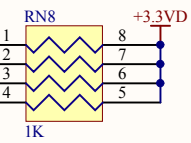


KEY[0..11] KEY[0..11]
 SW[0..3] SW[0..3]



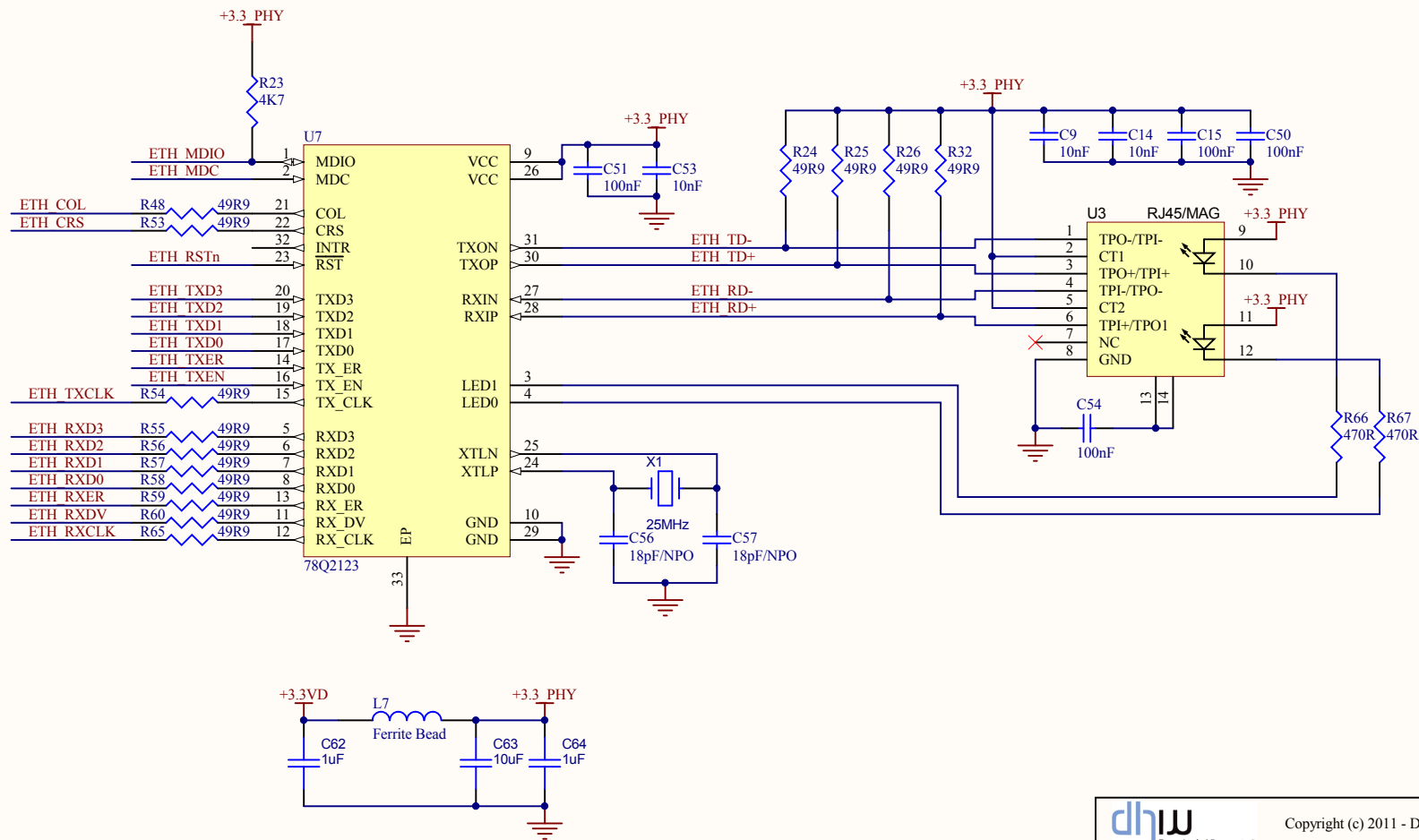
 Engenharia Representação		Copyright (c) 2011 - DHW Eng. & Rep.
MercurioIV		
Size	Document Number	Rev
A4	KEY - SWITCH	2.1
Date:	20/09/2013	Sheet 14 of 21

SDRAM A[0..12]	SDRAM A[0..12]
SDRAM BA[0..1]	SDRAM BA[0..1]
SDRAM CKE	SDRAM CKE
SDRAM CLK	SDRAM CLK
SDRAM D[0..15]	SDRAM D[0..15]
SDRAM LDQM	SDRAM LDQM
SDRAM UDQM	SDRAM UDQM
SDRAM nCS	SDRAM nCS
SDRAM nRAS	SDRAM nRAS
SDRAM nCAS	SDRAM nCAS
SDRAM nWE	SDRAM nWE



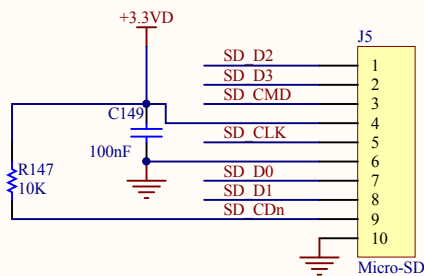
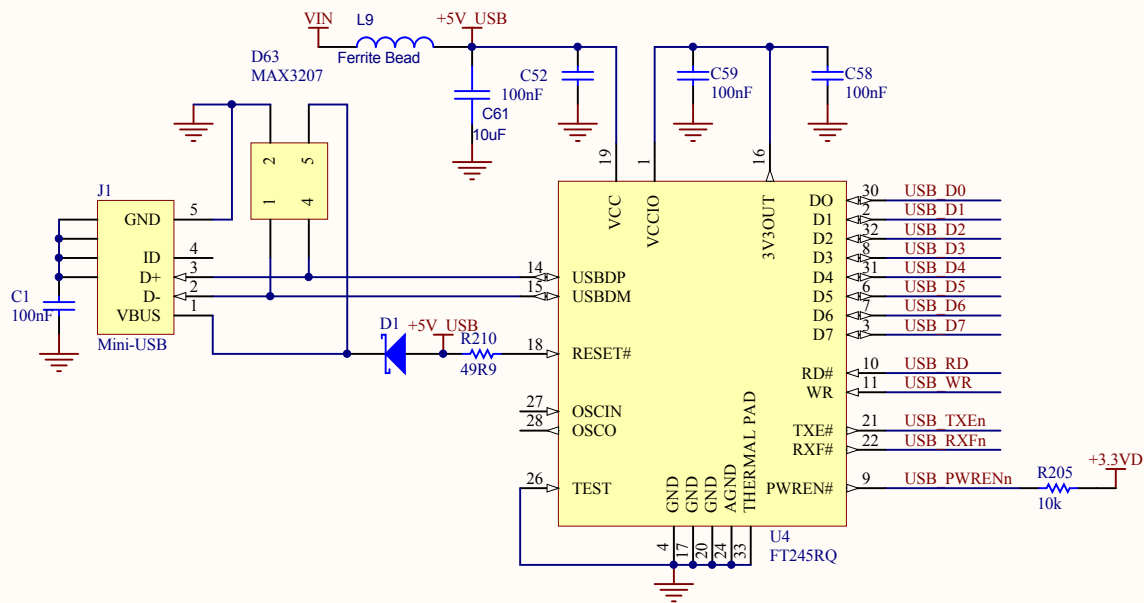
dhw Engenharia Representação		Copyright (c) 2011 - DHW Eng. & Rep.
Title Mercurio IV		
Size A4	Document Number SDRAM	Rev 2.1
Date: 20/09/2013	Sheet 15	of 21

ETH RXD[3..0]	ETH RXD[3..0]
ETH TXD[3..0]	ETH TXD[3..0]
ETH MDIO	ETH MDIO
ETH MDC	ETH MDC
ETH COL	ETH COL
ETH CRS	ETH CRS
ETH RSTn	ETH RSTn
ETH TXER	ETH TXER
ETH TXEN	ETH TXEN
ETH TXCLK	ETH TXCLK
ETH RXER	ETH RXER
ETH RXDV	ETH RXDV
ETH RXCLK	ETH RXCLK



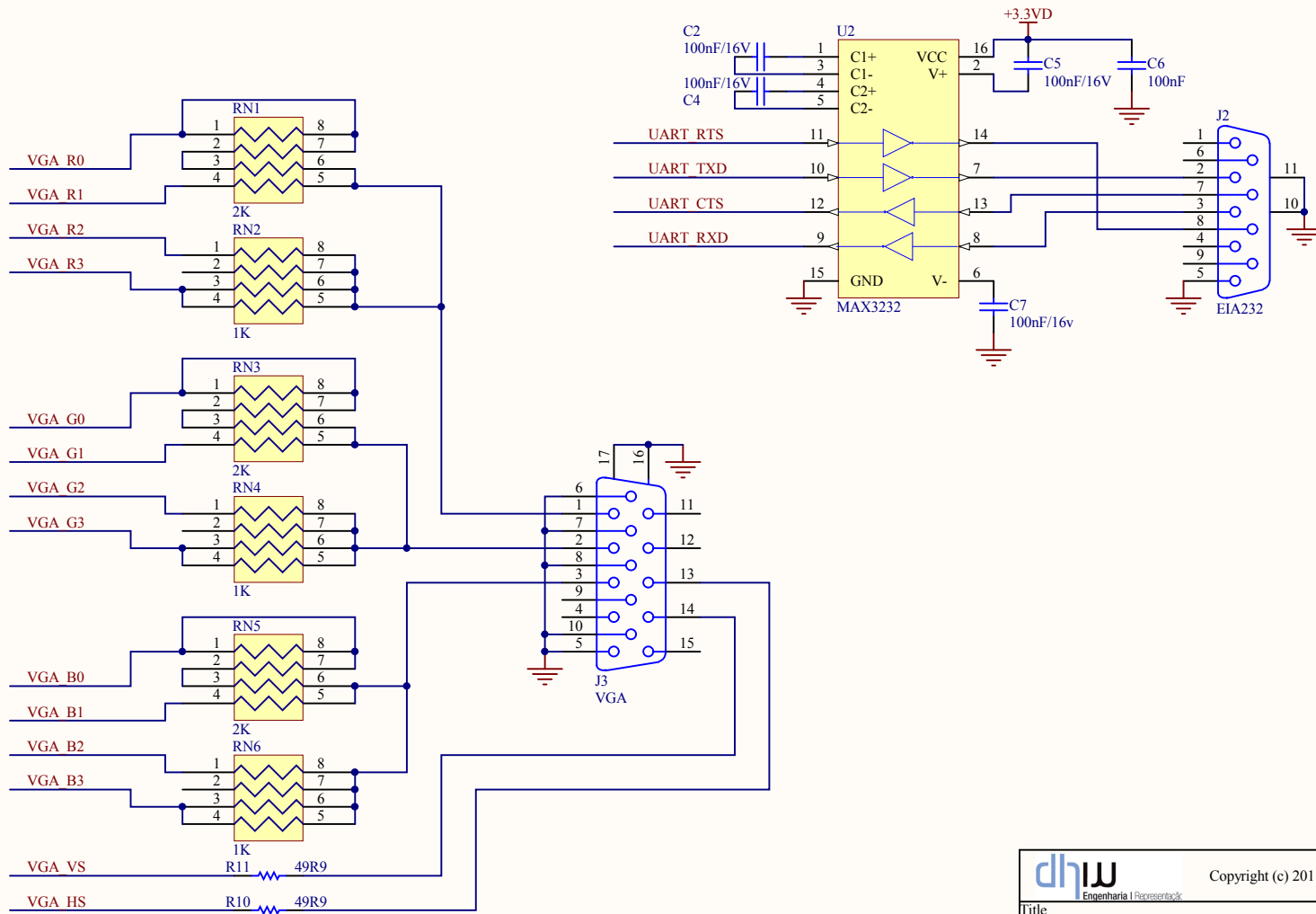
dhw Engenharia Representação		Copyright (c) 2011 - DHW Eng. & Rep.
Mercurio IV		
Size A4	Document Number ETHERNET	Rev 2.1
Date: 20/09/2013	Sheet 16	of 21

SD CDn	SD CDn
SD CLK	SD CLK
SD CMD	SD CMD
SD D[0..3]	SD D[0..3]
SD D[0..7]	SD D[0..7]
USB PWRENn	USB PWRENn
USB RD	USB RD
USB RXFn	USB RXFn
USB TXEn	USB TXEn
USB WR	USB WR



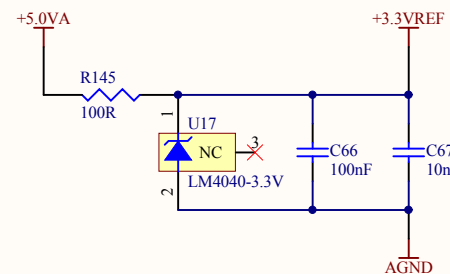
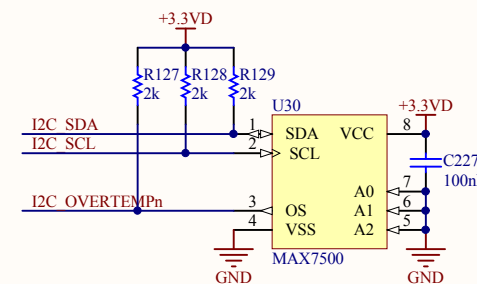
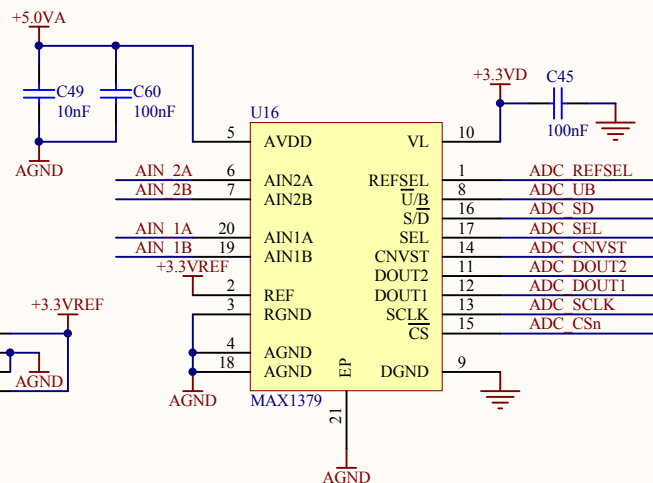
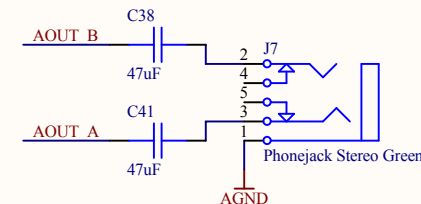
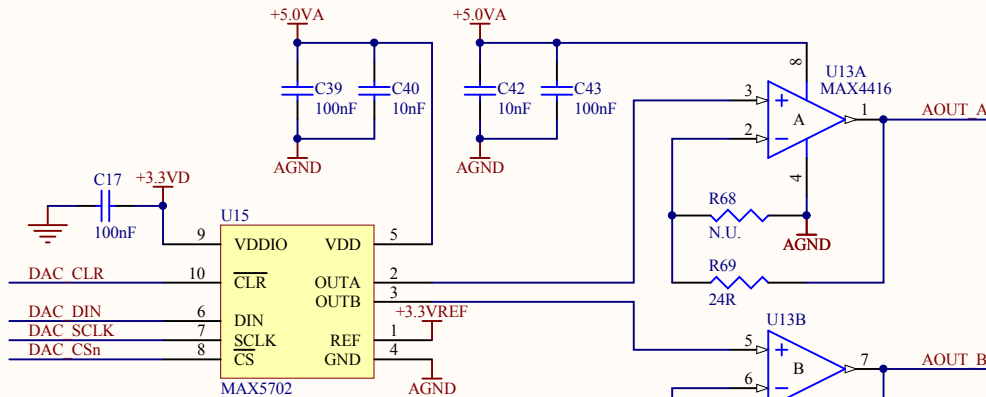
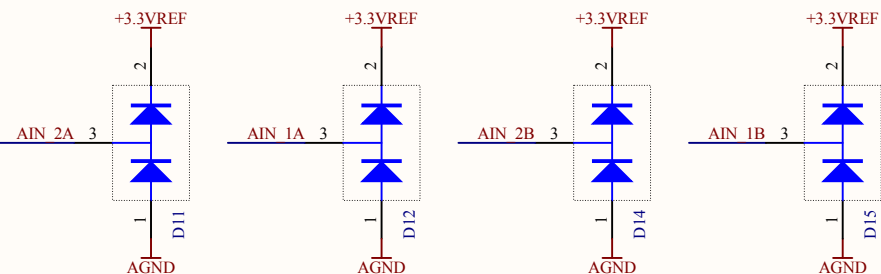
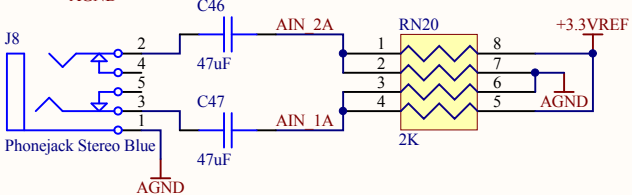
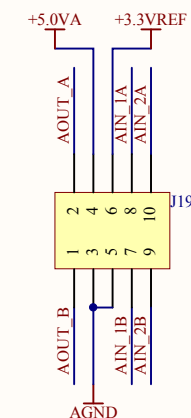
dhw Engenharia Representação		Copyright (c) 2011 - DHW Eng. & Rep.
Mercurio IV		
Size A4	Document Number USB - SDCard	Rev 2.1
Date: 20/09/2013	Sheet 17	of 21


UART CTS	UART CTS
UART RTS	UART RTS
UART RXD	UART RXD
UART TXD	UART TXD
VGA B[0..3]	VGA B[0..3]
VGA G[0..3]	VGA G[0..3]
VGA HS	VGA HS
VGA R[0..3]	VGA R[0..3]
VGA VS	VGA VS

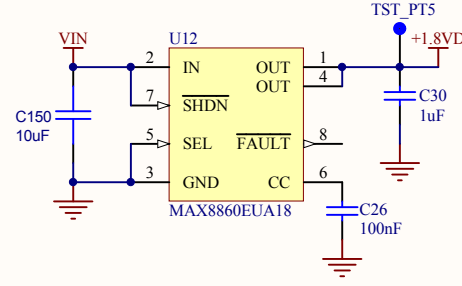
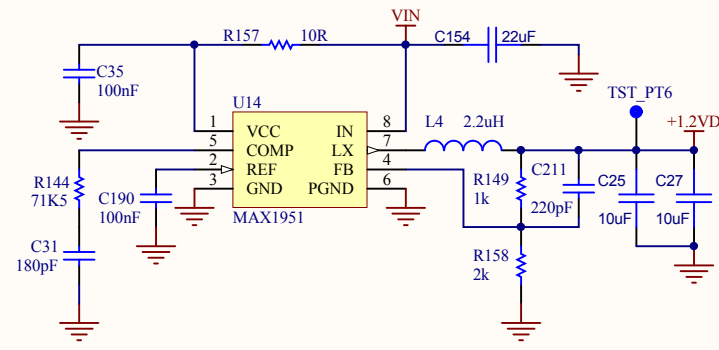
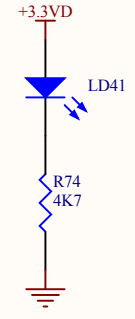
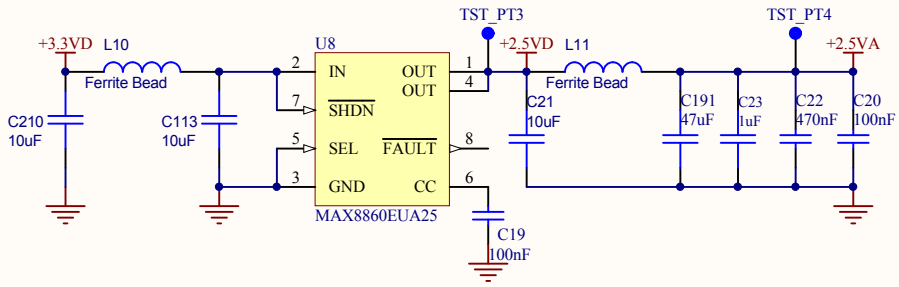
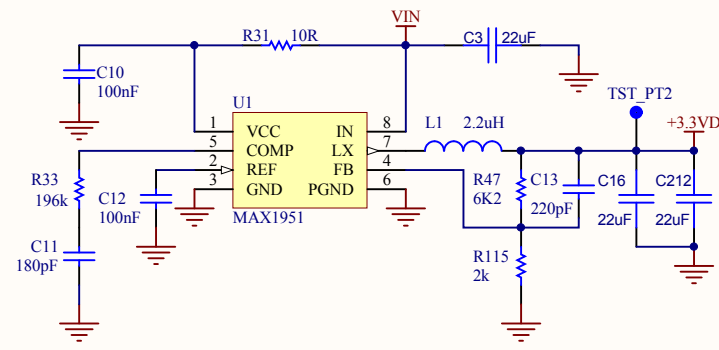
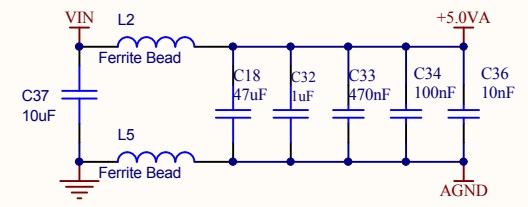
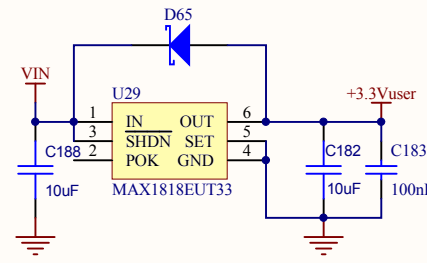
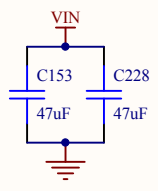
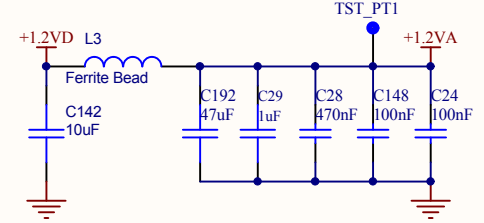
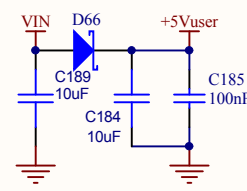
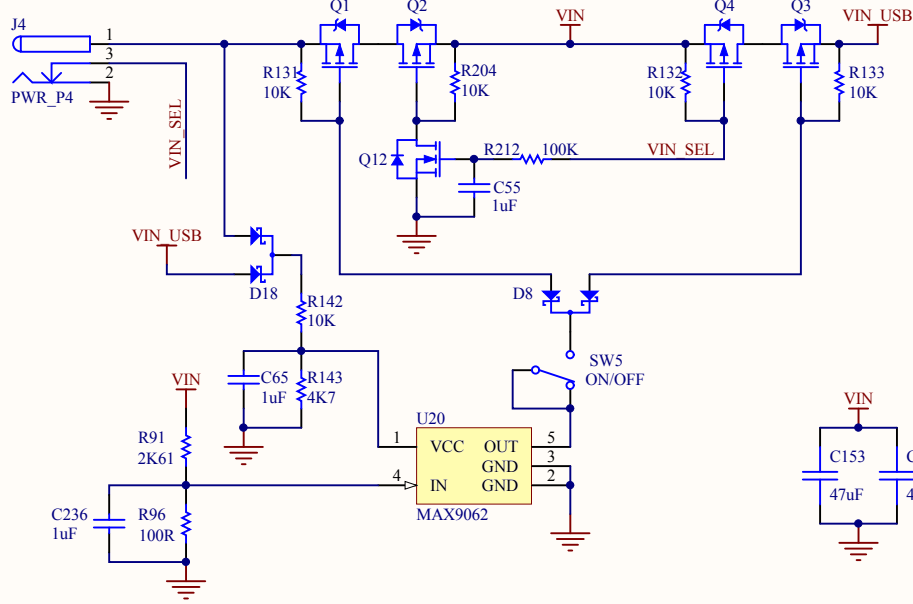



dhw Engenharia Representação		Copyright (c) 2011 - DHW Eng. & Rep.
Title Mercurio IV		
Size A4	Document Number VGA - SERIAL	Rev 2.1
Date: 20/09/2013	Sheet 18	of 21

ADC DOUT[2..1]	ADC DOUT[2..1]
ADC REFSEL	ADC REFSEL
ADC UB	ADC UB
ADC SD	ADC SD
ADC SEL	ADC SEL
ADC CNVST	ADC CNVST
ADC SCLK	ADC SCLK
ADC CSn	ADC CSn
DAC CLR	DAC CLR
DAC DIN	DAC DIN
DAC SCLK	DAC SCLK
DAC CSn	DAC CSn
I2C SCL	I2C SCL
I2C SDA	I2C SDA
I2C OVERTEMPn	I2C OVERTEMPn

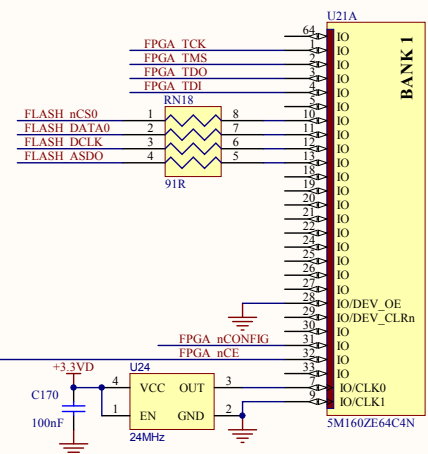
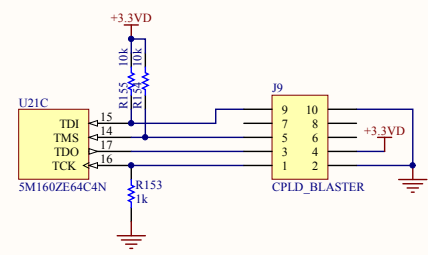
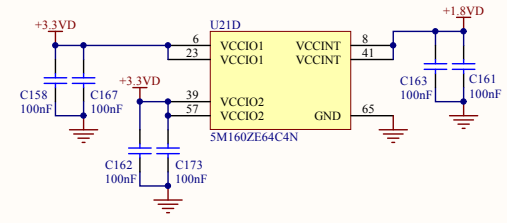
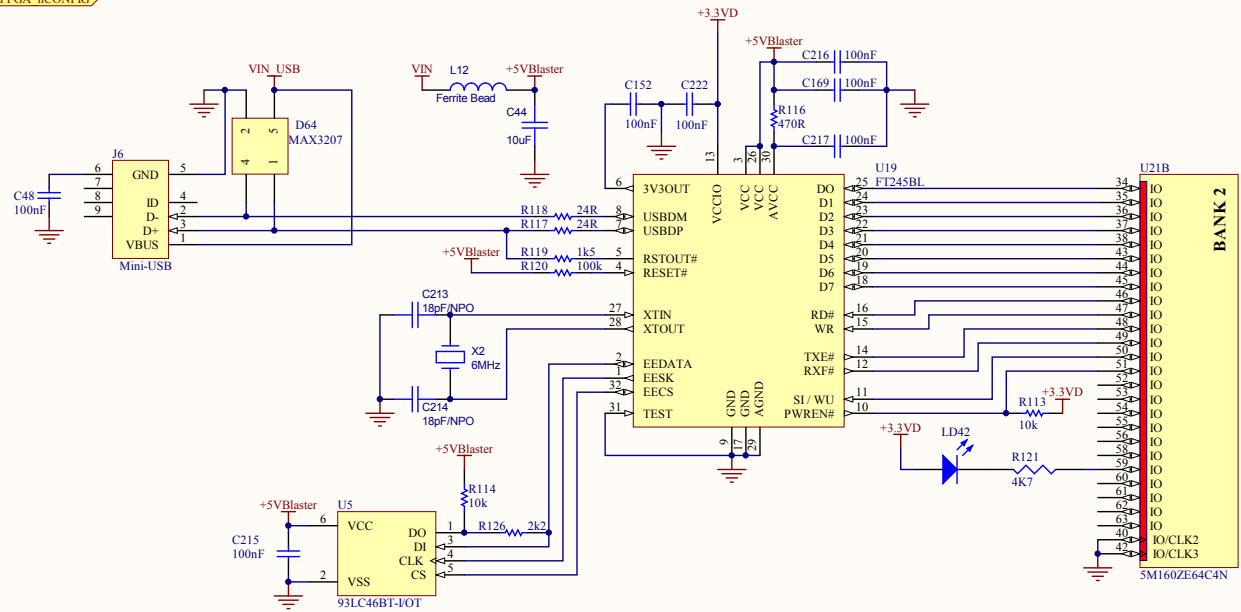


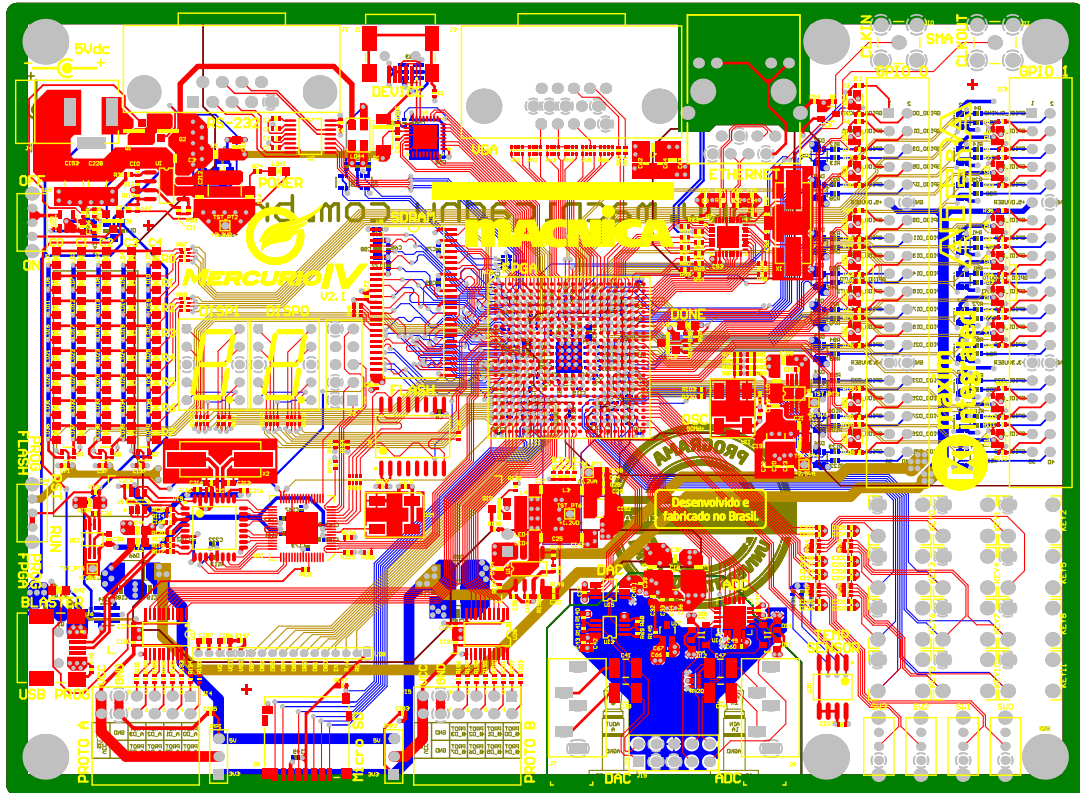
		Copyright (c) 2011 - DHW Eng. & Rep.
Title		
Mercurio IV		
Size	Document Number	Rev
A4	ADC - DAC - TEMP SENSOR	2.1
Date:	20/09/2013	Sheet 19 of 21



		Copyright (c) 2011 - DHW Eng. & Rep.
Mercurio IV		
Size	Document Number	Rev
A4	POWER SUPPLY	2.1
Date:	20/09/2013	Sheet 20 of 21

- FLASH ASDO
- FLASH DATA0
- FLASH DCLK
- FLASH nCS0
- FPGA TCK
- FPGA TDI
- FPGA TDO
- FPGA TMS
- FPGA nCE
- FPGA nCONFIG





PLACA: 6 LAYERS
 MASCARA DE SOLDA: BRANCA
 SIMBOLOGIA: PRETO
 MATERIAL: FR4 - 1.6mm
 ACABAMENTO: ENIG
 VIAS: COBERTAS COM MASCARA DE SOLDA

PCB STACKUP

0.7mil	L1	.GTL - SIGNAL 1
4.5 mil		
1.4mil	L2	.GP1 - GND
22 mil		
1.4mil	L3	.GP2 - PWR1
4.5 mil		
0.7mil	L4	.G1 - SIGNAL 2
22 mil		
1.4mil	L5	.GP3 - PWR2
4.5 mil		
0.7 mil	L6	.GBL - SIGNAL 3

- Dielectric constant 4.3

Top Silkscreen
 Bottom Silkscreen
 Top Layer - .GTL - SIGNAL 1
 Internal 1 - .GP1 - GND
 Internal 2 - .GP2 - PWR1
 Internal 3 - .G1 - SIGNAL 2
 Internal 4 - .GP3 - PWR2
 Bottom Layer - .GBL - SIGNAL 3