ROCHESTER INSTITUTE OF TECHNOLOGY
MICROELECTRONIC ENGINEERING

RIT's Sub-CMOS Process (Leff < 1.0 µm)

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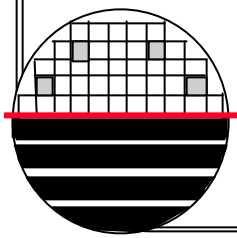
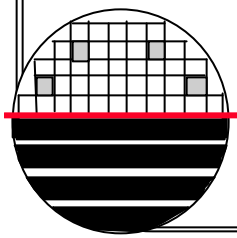


OUTLINE

Introduction
Process Comparison
- p-well CMOS
- Subμ CMOS
- Advanced CMOS

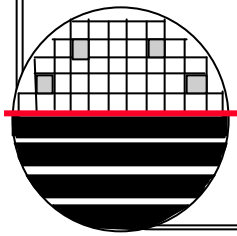
Subμ CMOS Process Details



INTRODUCTION

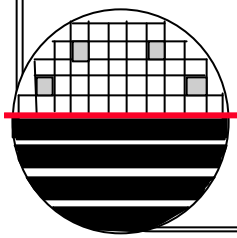
RIT has been CMOS processes since 1995. Today we run Subμ and Advanced CMOS for MicroE students to learn about new process technologies. We run SMFL CMOS to fabricate circuits for students in EE Analog IC design courses.

RIT p-well CMOS (1995)	λ = 4 μm	Lmin = 8 μm
RIT Subμ CMOS (2000)	λ = 0.5 μm	Lmin = 1.0 μm
RIT Advanced CMOS (2003)	λ = 0.25 μm	Lmin = 0.5 μm
SMFL CMOS (2004)	λ = 1.0 μm	Lmin = 2.0 μm



MAJOR CONSIDERATIONS

Substrate Doping
Well Formation and Channel Stop
Isolation Technology
Gate Oxide Thickness
Gate Doping
Threshold Voltages
Side Wall Spacers and Low Doped Drain
Drain/Source Junction Depth
Well Contacts
Silicides
Metal Technology



PROCESS COMPARISON

Built in Voltage: $\Psi_o = 0.55 + KT/q \quad \ln (N/ni)$

Width of Space Charge Layer, $Wsc = [(2\varepsilon/q) (\Psi_o + V_R) (1/N)]^{1/2}$

W on lightly doped side:

Maximum Electric Field: $E_o = - [(2q/\varepsilon) (\Psi_o + V_R) (N)^{1/2}$

Example:

Y_o **= 0.55 + 0.026 ln (3E16/1.45E10) = 0.928**

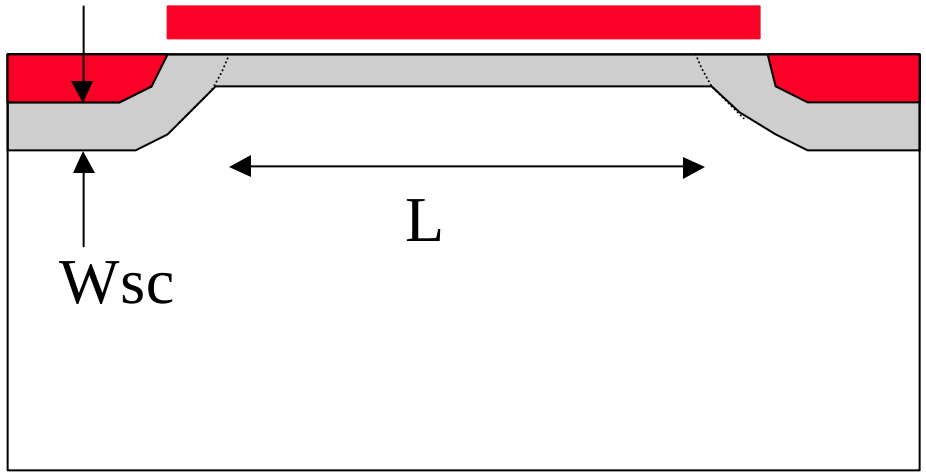
Wsc = [(2(11.7)(8.85E-14)**/1.6E-19) (0.928) (1/3E16)]$^{1/2}$**
= 0.20 µm

$\varepsilon = \varepsilon_o \varepsilon_r = 8.85E\text{-}12 \ (11.7)$ F/m
8.85E-14 (11.7) F/cm

RIT P-WELL CMOS

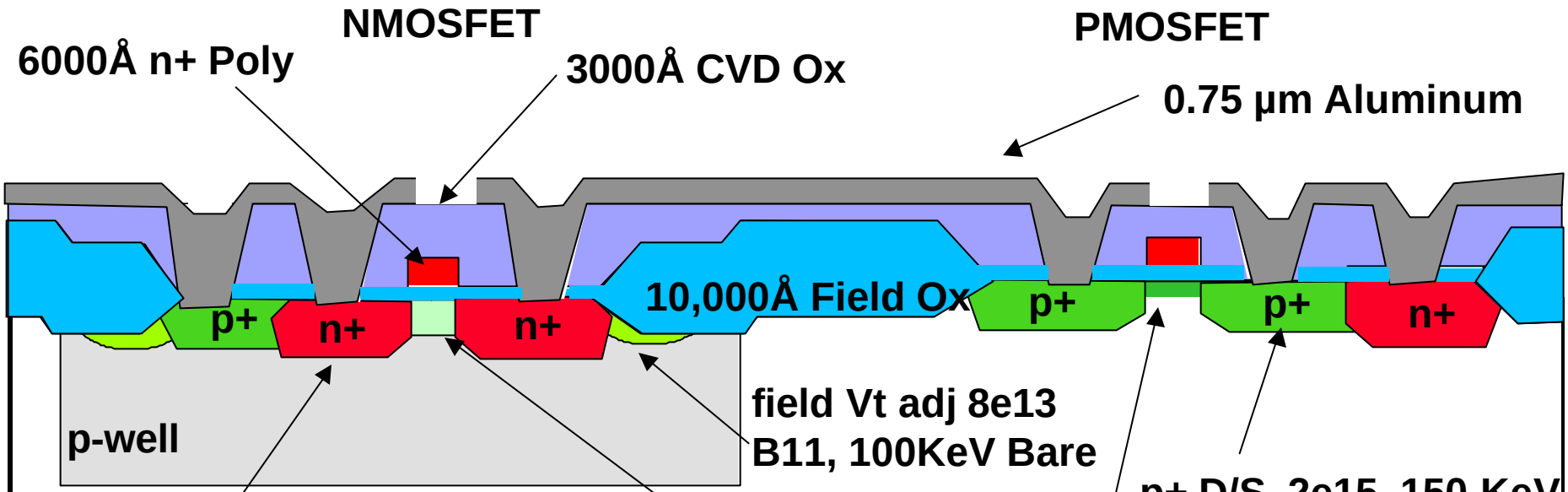
RIT p-well CMOS

100 mm wafers
Nsub = 1E15 cm-3
Npwell= 1E16 cm-3
Dose = 1.2E12 cm-2
Xjwell= 4.5µm
LOCOS
Field Ox = 11,000 Å
Xox = 500 Å
Lmin= 8 µm



Long Channel Behavior

RIT P-WELL CMOS



GCA 6700 g-LINE STEPPER

g-Line Stepper

λ = 436 nm

NA = 0.28

σ = 0.6

Resolution

0.6 λ / NA = ~1µm

20 x 20 mm Field Size

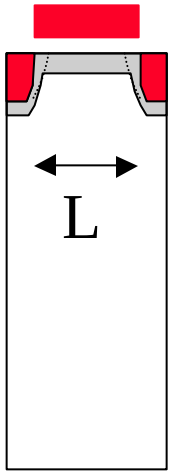
Depth of Focus

= $k_2 \lambda/(NA)^2$ = 3 µm

RIT SUBμ CMOS

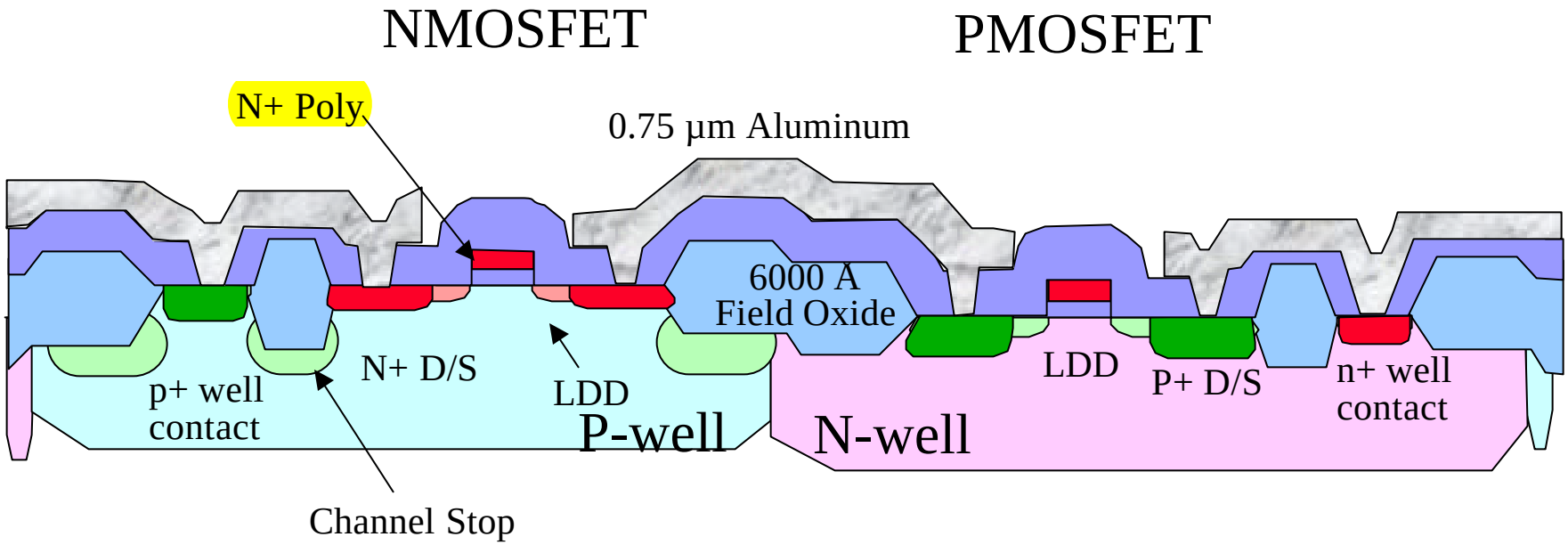
RIT Subμ CMOS

150 mm wafers
Nsub = 1E15 cm-3
Nn-well = 3E16 cm-3
Xj = 2.5 μm
Np-well = 1E16 cm-3
Xj = 3.0 μm
LOCOS
Field Ox = 6000 Å
Xox = 150 Å
Lmin= 1.0 μm
LDD/Side Wall Spacers



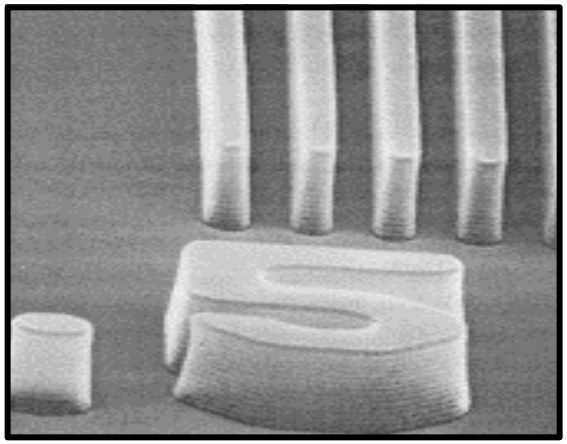
Long Channel Behavior

RIT SUBμ CMOS



N-type Substrate 10 ohm-cm

CANON FPA-2000 i1 STEPPER



i-Line Stepper $\lambda = 365$ nm

NA = 0.52, $\sigma = 0.6$

Resolution = $0.7\ \lambda$ / NA = ~0.5 µm

20 x 20 mm Field Size

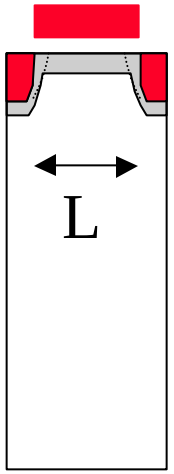
Depth of Focus = $k_2\ \lambda/(NA)^2$

= 0.8 µm

RIT ADVANCED CMOS

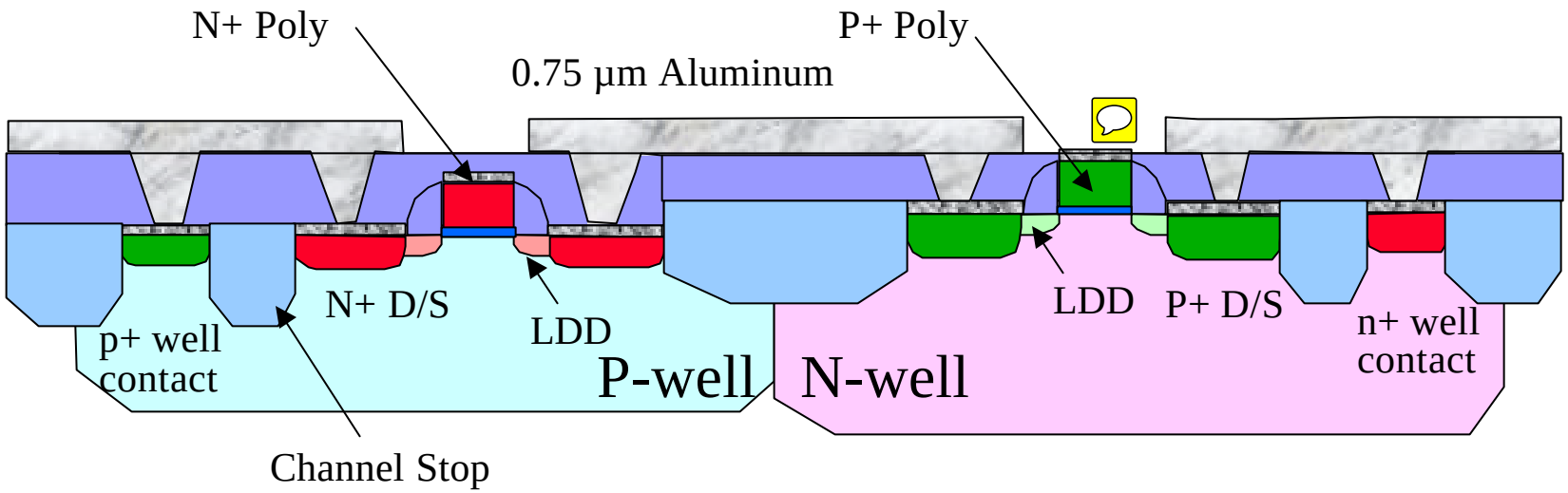
RIT Advanced CMOS

150 mm Wafers
Nsub = 1E15 cm-3
Nn-well = 2.5E16 cm-3
Xj = 2 µm
Np-well = 2.5E16 cm-3
Xj = 2.5 µm
Shallow Trench Isolation
Field Ox = 6000 Å
Dual Doped Gate n+ and p+
Xox = 100 Å
Lmin= 0.5 µm
LDD/Side Wall Spacers
Ti Silicide
Tungsten Plugs, CMP, Al Damascene



Long Channel Behavior

RIT ADVANCED CMOS



ASML 5500/90 STEPPER

KrF Excimer Laser Stepper

λ = 248 nm

NA = 0.52, σ = 0.6

Resolution = 0.7 λ / NA = ~0.3 µm

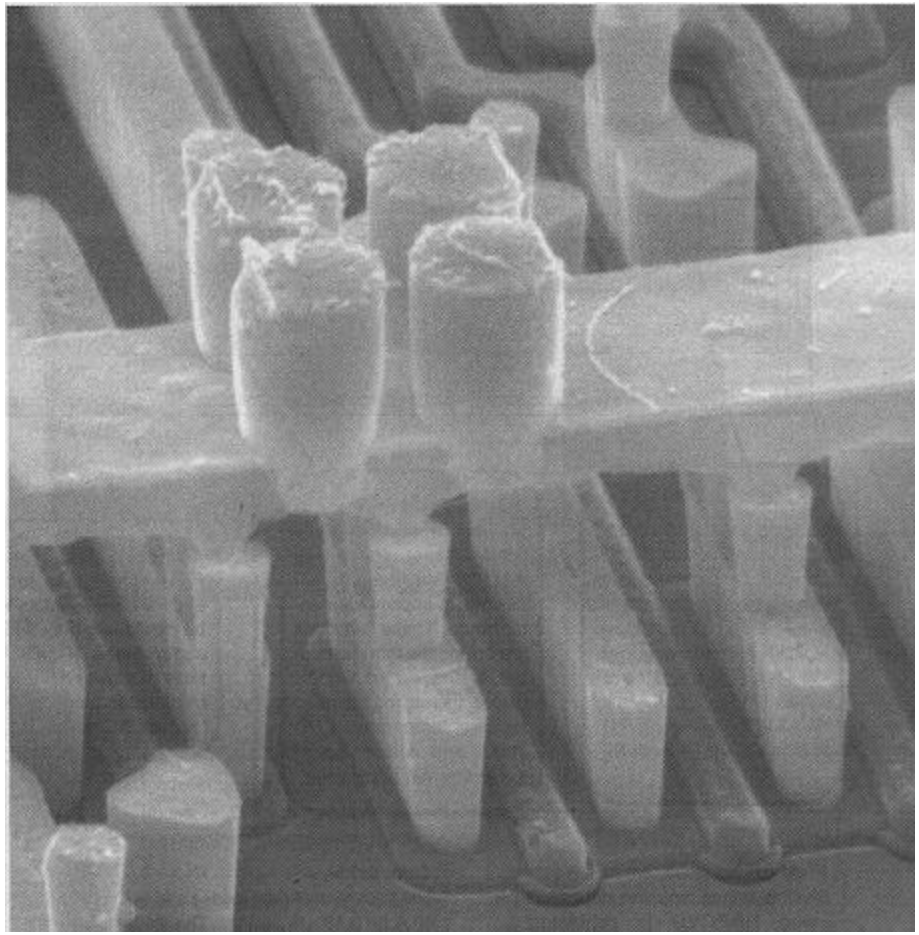
20 x 20 mm Field Size

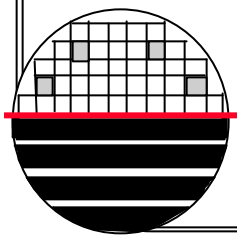
Depth of Focus = $k_2 \lambda/(NA)^2$

~ 0.64 µm

MULTI- LAYER ALUMINUM, W PLUGS, CMP, DAMASCENE OF LOCAL W INERCONNECT

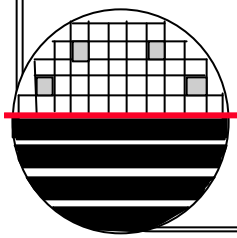
Multi-layer aluminum interconnect with tungsten plugs, CMP, and damascene of local tungsten interconnect.



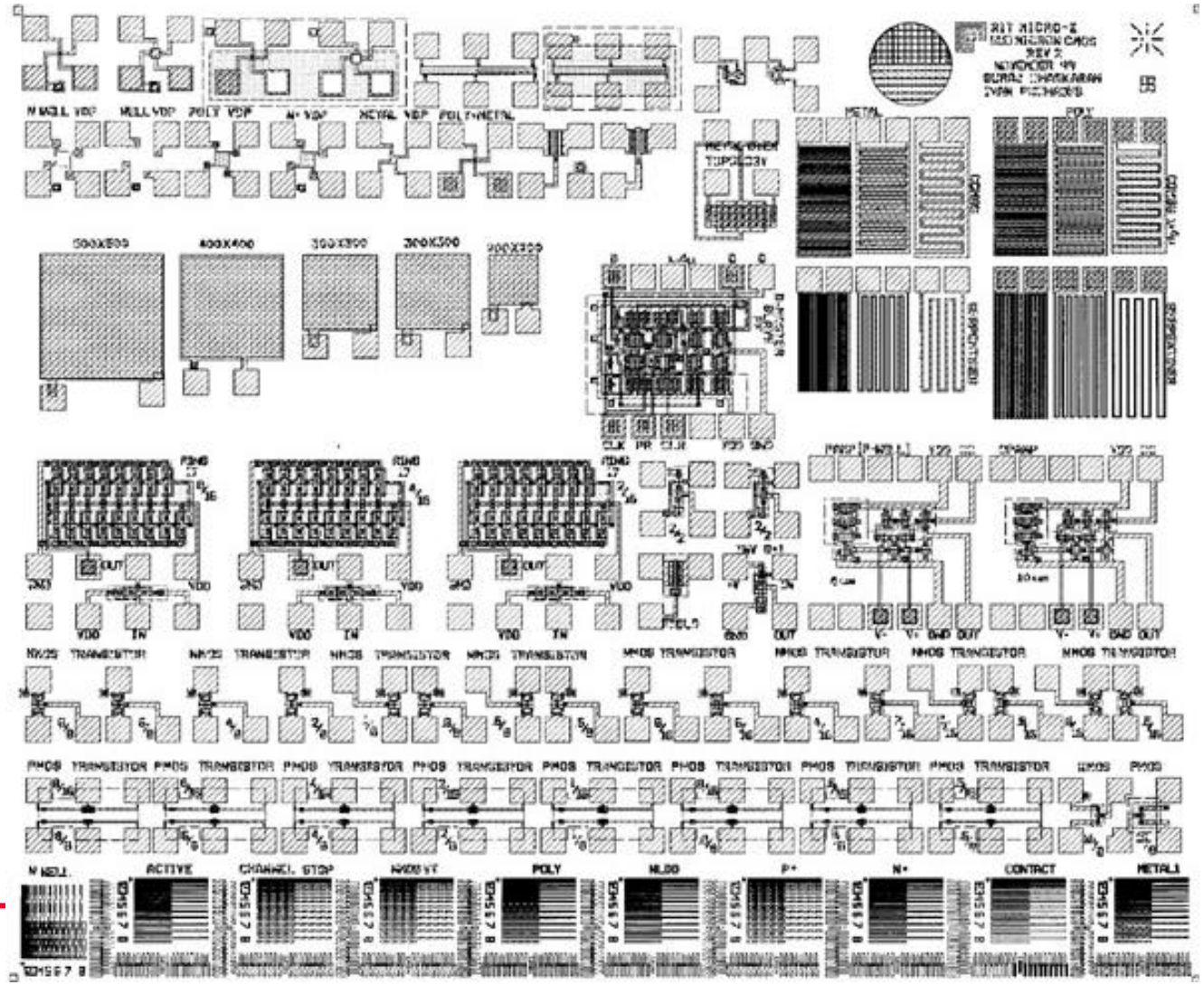


RIT SUBμ CMOS PROCESS

150 mm Wafers
LOCOS
n+ Poly Gates
LDD
11 Photo Layers (includes 1st Metal)

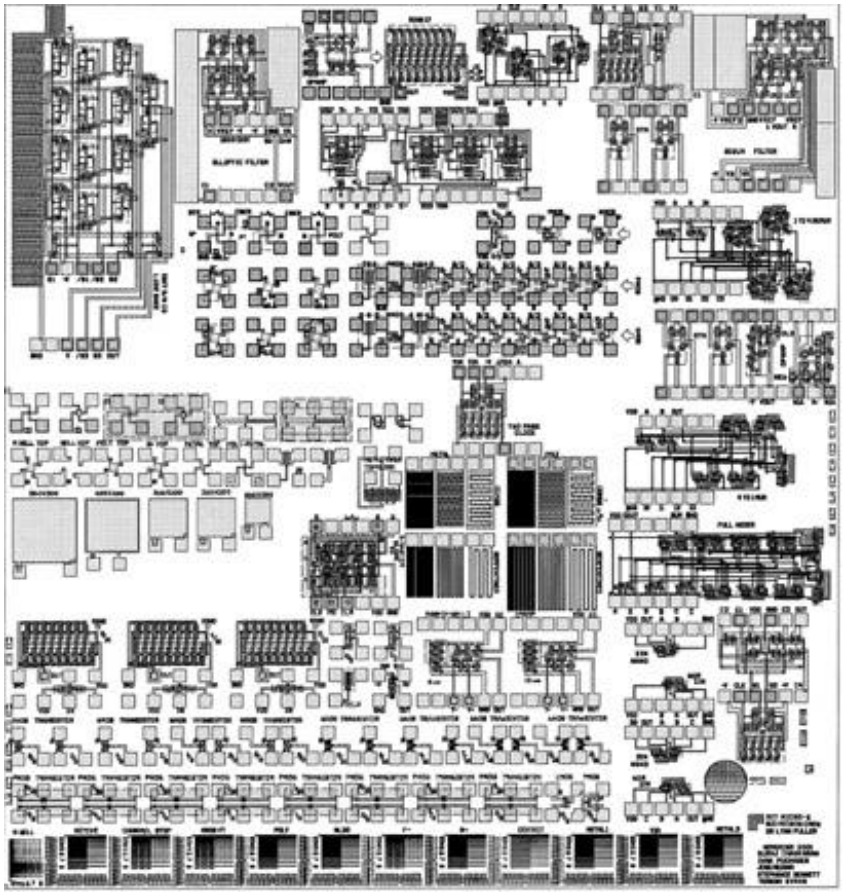


SUB MICRON CMOS TEST STRUCTURES



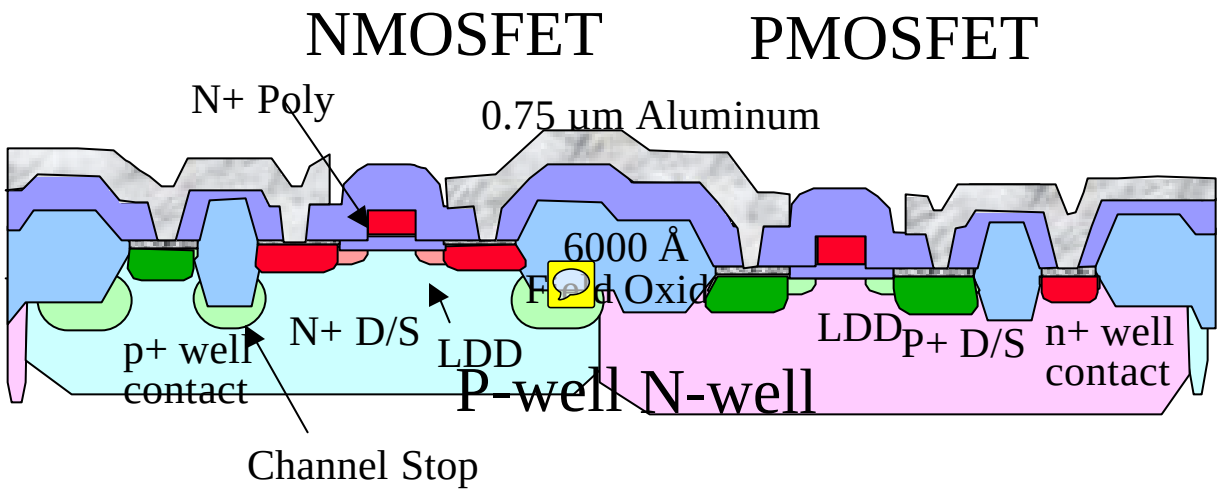
CMOS TEST CHIP FOR MANUFACTURING LABS

Layout of CMOS test chip for microelectronic engineering manufacturing courses. This chip has transistors down to 0.5 µm gate length, a variety of test structures, digital and analog circuit building blocks including A-to-D and D-to-A converters, operational amplifiers, transconductance amplifiers, and filters of various types.

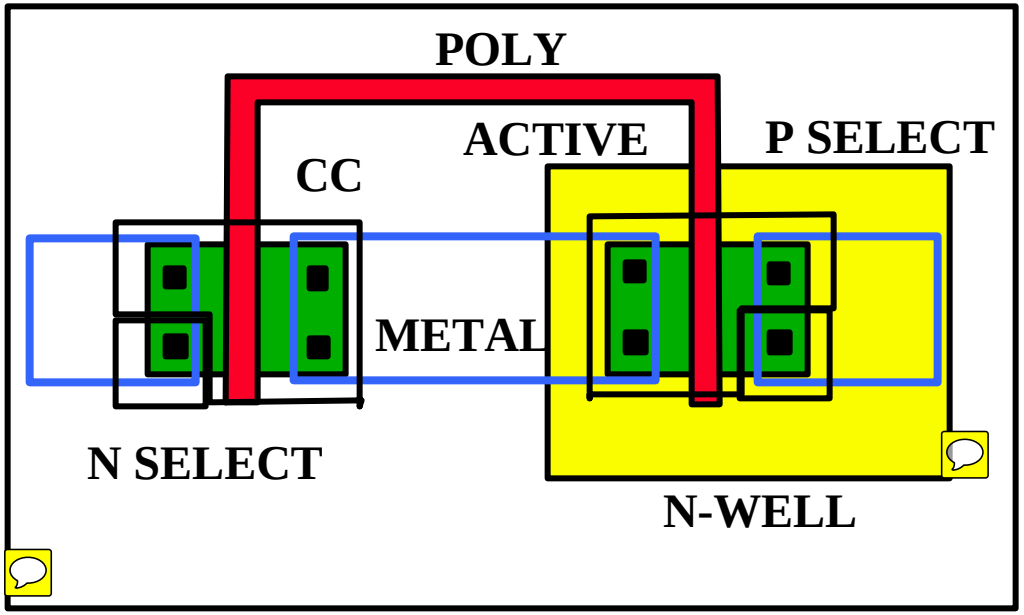


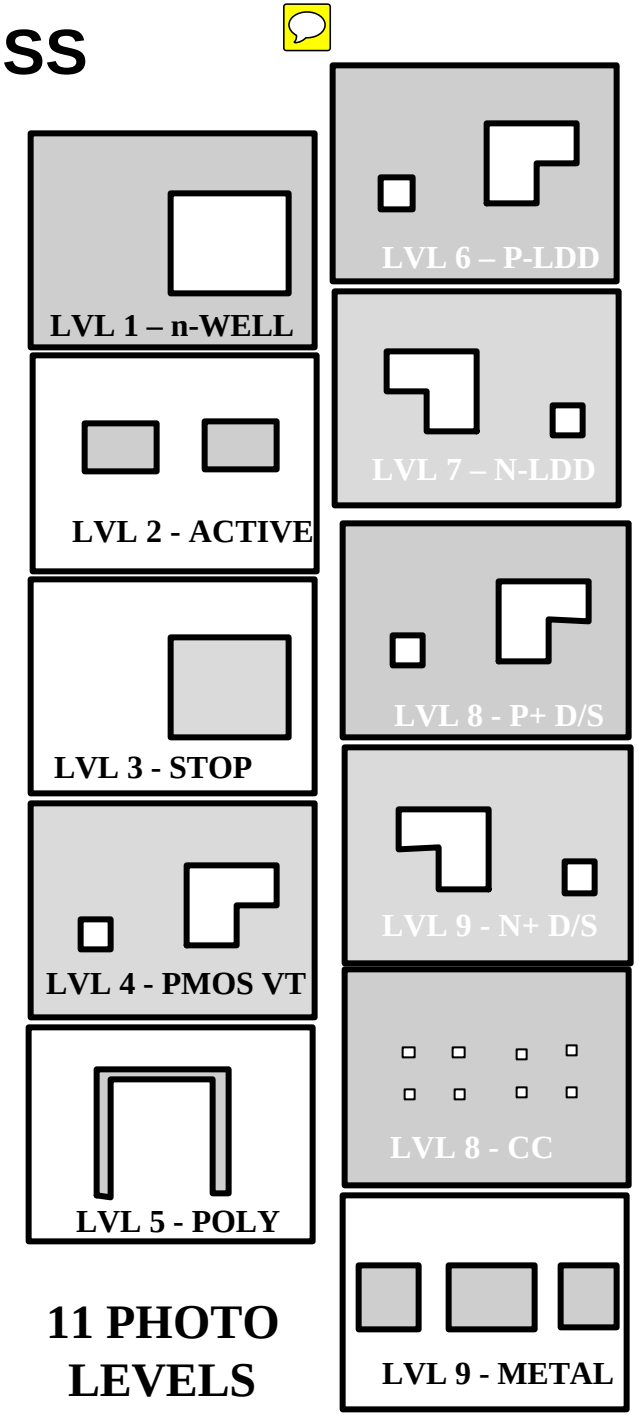
Dr. Lynn Fuller, Lisa Bonanno 2003

RIT SUB-CMOS PROCESS



N-type Substrate 10 ohm-cm





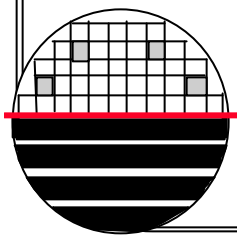
11 PHOTO LEVELS

SUB-CMOS 150 PROCESS

SUB-CMOS Versions 150

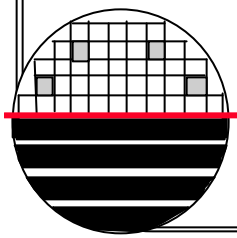
1. ID01
2. DE01
3. CL01
4. OX05--- pad oxide
5. CV02- 1500 Å
6. PH03 –1- n well
7. ET29
8. IM01 – n-well
9. ET07
10. CL01
11. OX04 – well oxide
12. ET19
13. IM01 – p-well
14. OX06 – well drive
15. ET06
16. CL01
17. OX05 – pad oxide
18. CV02 - 3500 Å
19. PH03 – 2 - Active
20. ET29
21. ET07
22. PH03 – 3 - p-well stop
23. IM01- stop
24. ET07
25. CL01
26. OX04 - field
27. ET19
28. ET06
29. OX04 - Kooi
30. PH03 – 4 - PMOS Vt Adjust
31. IM01 - Vt
32. ET07
33. ET06
34. CL01
35. OX06 - gate
36. CV01
37. DI04 - dope poly Si
38. ET06
39. DE01
40. PH03 – 5 – poly
41. ET08
42. ET07
43. PH03 – 6 - n-LDD
44. IM01
45. ET07
46. PH03 – 7 - p-LDD
47. IM01
48. ET07
49. CL01
50. CV03
51. OX08 -- LTO Densify Anneal
52. ET10
53. PH03 – 8 - N+D/S
54. IM01 – N+D/S
55. ET07
56. PH03 – 9 P+ D/S
57. IM01 – P+ D/S
58. ET07
59. CL01
60. OX08 – DS Anneal
61. CV03 – LTO
62. PH03 – 10 CC
63. ET10
64. ET07
65. CL01
66. ME01
67. PH03 -11- metal
68. ET05
69. ET07
70. SI01
71. TE01
72. TE02
73. TE03
74. TE04

3-20-03



STARTING WAFER

N-type or P-type Substrate 10 ohm-cm



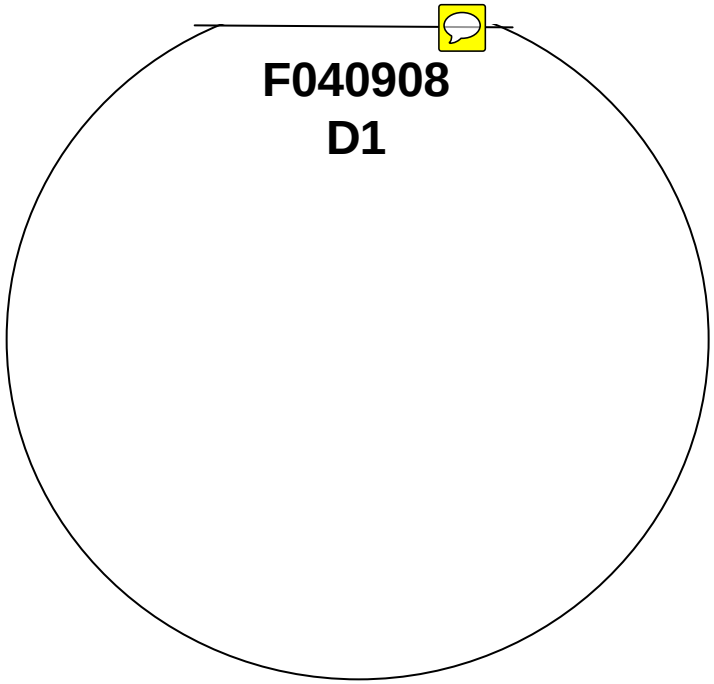
SCRIBE WAFERS WITH LOT AND WAFER NUMBER

Lot Numbers are: XYYMMDD
Where X is

R for Research
L for Laboratory
F for Student Factory
S for Scrap or Shipped

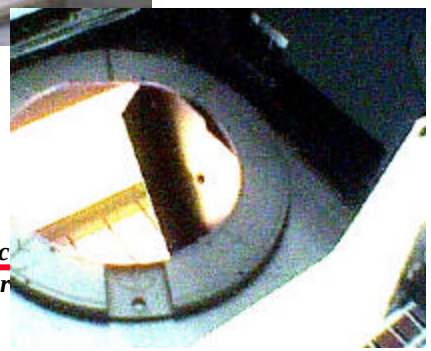
YY is year
MM is month
DD is day

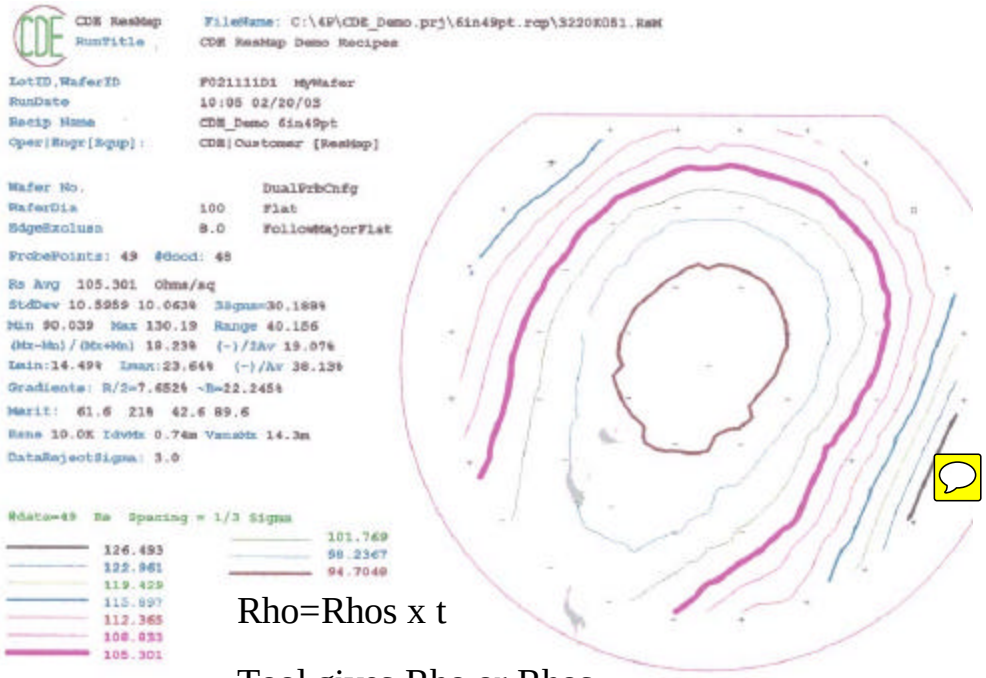
The wafer number is D1, D2, D3, etc. for device wafers or C1, C2, C3, etc. for control wafers, X1,X2 for extra wafers to replace broken D wafers



MEASURE WAFER RESISTIVITY

CDE Resistivity Mapper





Rho=Rhos x t

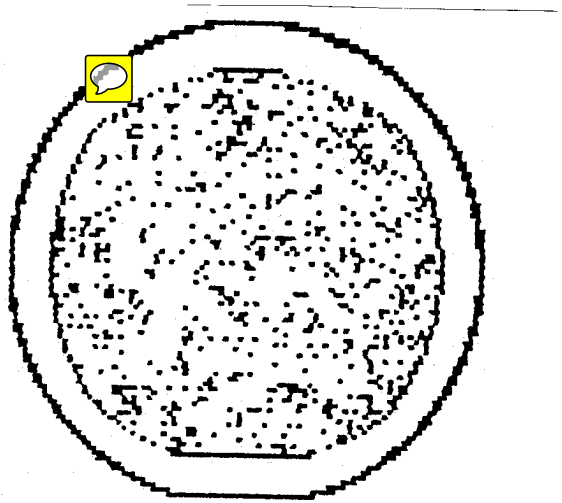
Tool gives Rho or Rhos depending on recipe used, automatically adjusts correction factors for wafer thickness

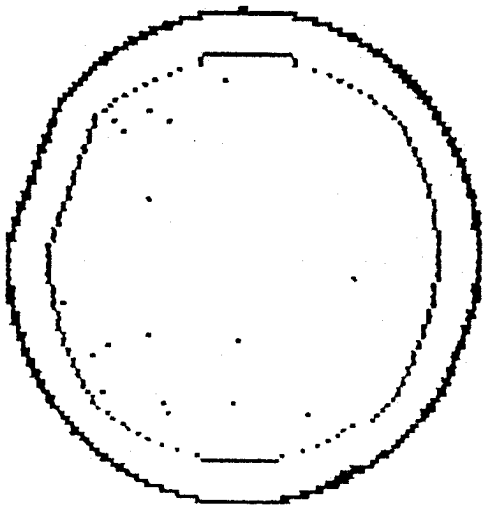
Record:
Average Resistivity on D1 only
Rho(ave) = ohm-cm

TENCORE SURF SCAN

Gives total surface particle count and count in 4 bins <0.5, 0.5 to 2.0, 2.0-10, >10. Bin boundary can be selected. Edge exclusion eliminated count from near the edge of the wafer.

EXAMPLE SURFACE PARTICLE COUNT DATA





Before Cleaning (75 mm)

Size Range (µm)	Count
0.2 - 0.5	104
0.5 - 2.0	562
2.0 - 10	19
>10	2

After Cleaning (75 mm)

Size Range (µm)	Count
0.2 - 0.5	10
0.5 - 2.0	4
2.0 - 10	3
>10	0

RCA CLEAN

APM

NH_4OH - 1part
H_2O_2 - 3parts
H_2O - 15parts
70 °C, 15 min.

DI water
rinse, 5 min.

H_20 - 50
HF - 1
60 sec.

DI water
rinse, 5 min.

HPM

HCL - 1part
H_2O_2 - 3parts
H_2O - 15parts
70 °C, 15 min.

DI water
rinse, 5 min.

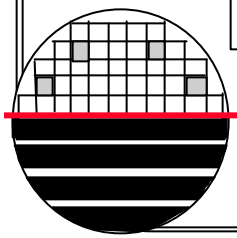
SPIN/RINSE
DRY

What does RCA stand for?

ANSWER

PLAY

Explain the Process



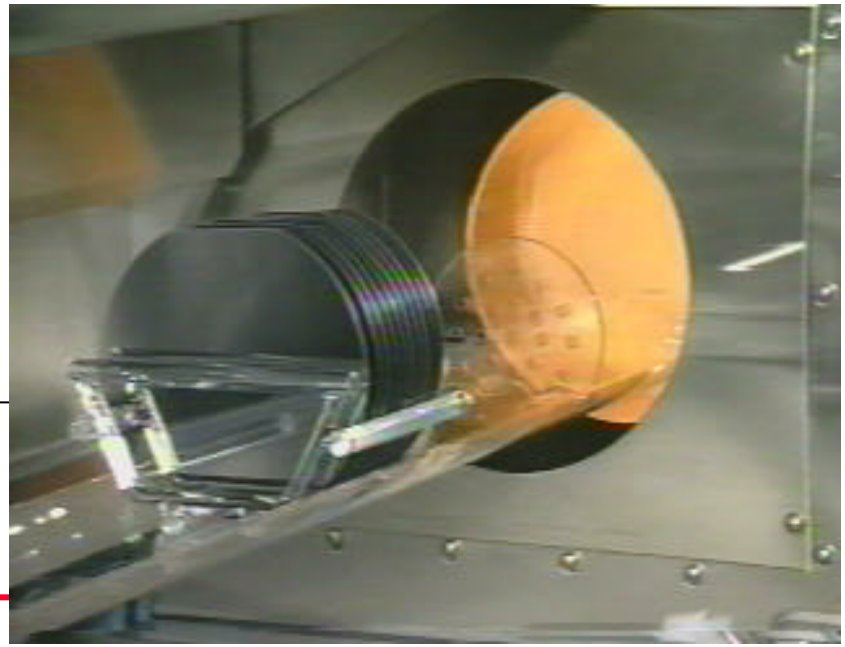
RCA CLEAN TOOLS

Megasonics Wet Bench
Spin/Rinse/Dry Tool (SRD)

PAD OXIDE GROWTH

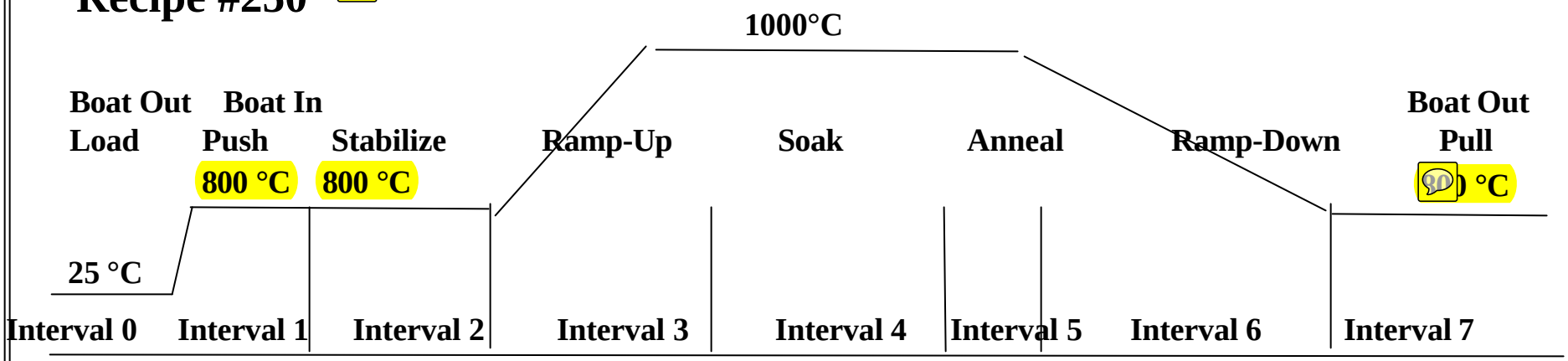
Pad Oxide, 500A
Bruce Furnace 04 Recipe 250

Substrate 10 ohm-cm



BRUCE FURNACE RECIPE 250 500Å DRY OXIDE

Recipe #250



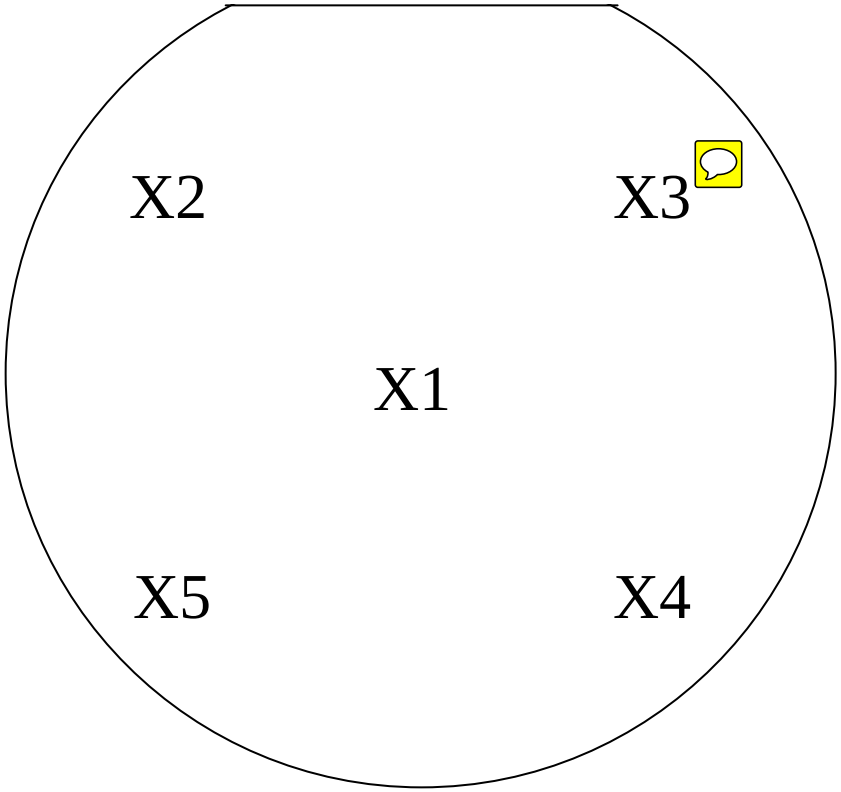
Any	12 min	15 min	20 min	40min	5min	40 min	12 min
0 lpm	10 lpm	10 lpm	5 lpm	10 lpm	15 lpm	10 lpm	5 lpm
none	N2	N2	O2	O2	N2	N2	N2

At the end of a run the furnace returns to Interval 0 which is set for boat out, 25 °C and no gas flow. The furnace waits in that state until someone aborts the current recipe or loads a new recipe.

MEASURE OXIDE THICKNESS

Record:
Color = TAN
Color Chart Thickness = 500 Å
Nanospec Thickness = Å

FACTORY THICKNESS MEASUREMENT LOCATIONS



DEPOSIT SILICON NITRIDE

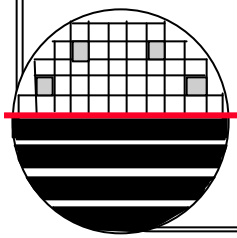
Nitride Target 1500A
LPCVD, 810C, Rate~43Å/min

Recipe FACTORY NITRIDE 810
Temp = 810°C
Pressure = 400 mTorr
DCS Flow = 60 sccm
Ammonia Flow = 150 sccm

Substrate 10 ohm-cm

LEVEL 1 PHOTO - N-WELL

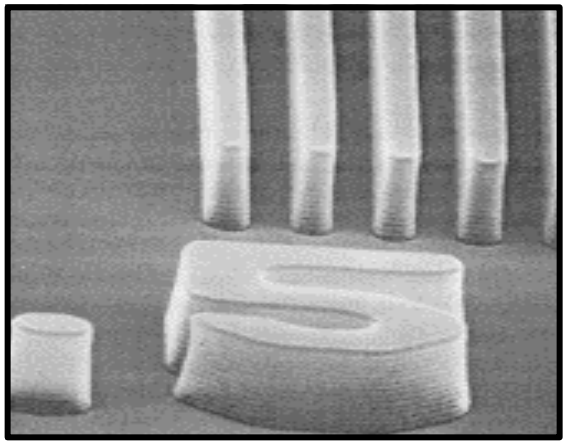
Substrate 10 ohm-cm



SSI COAT AND DEVELOP TRACK FOR 6” WAFERS

Use Recipe: Coat.rcp and Develop.rcp

CANON FPA-2000 i1 STEPPER



i-Line Stepper $\lambda = 365$ nm

NA = 0.52, $\sigma = 0.6$

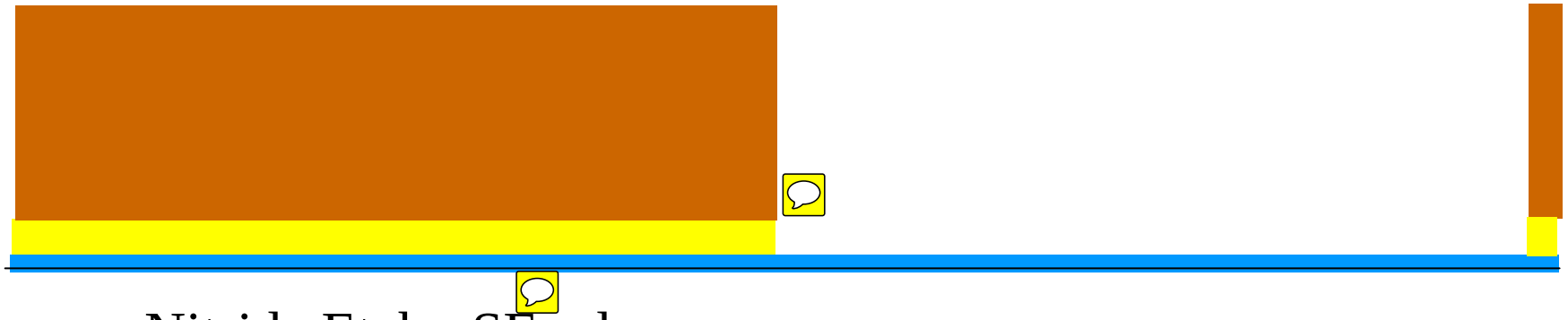
Resolution = $0.7\ \lambda$ / NA = ~0.5 µm

20 x 20 mm Field Size

Depth of Focus = $k_2\ \lambda/(NA)^2$

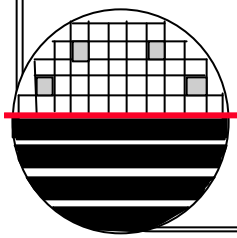
= 0.8 µm

PLASMA ETCH NITRIDE



Nitride Etch: SF_6 plasma

LAM 490 Etcher, Etch Rate ~1000 Å/min

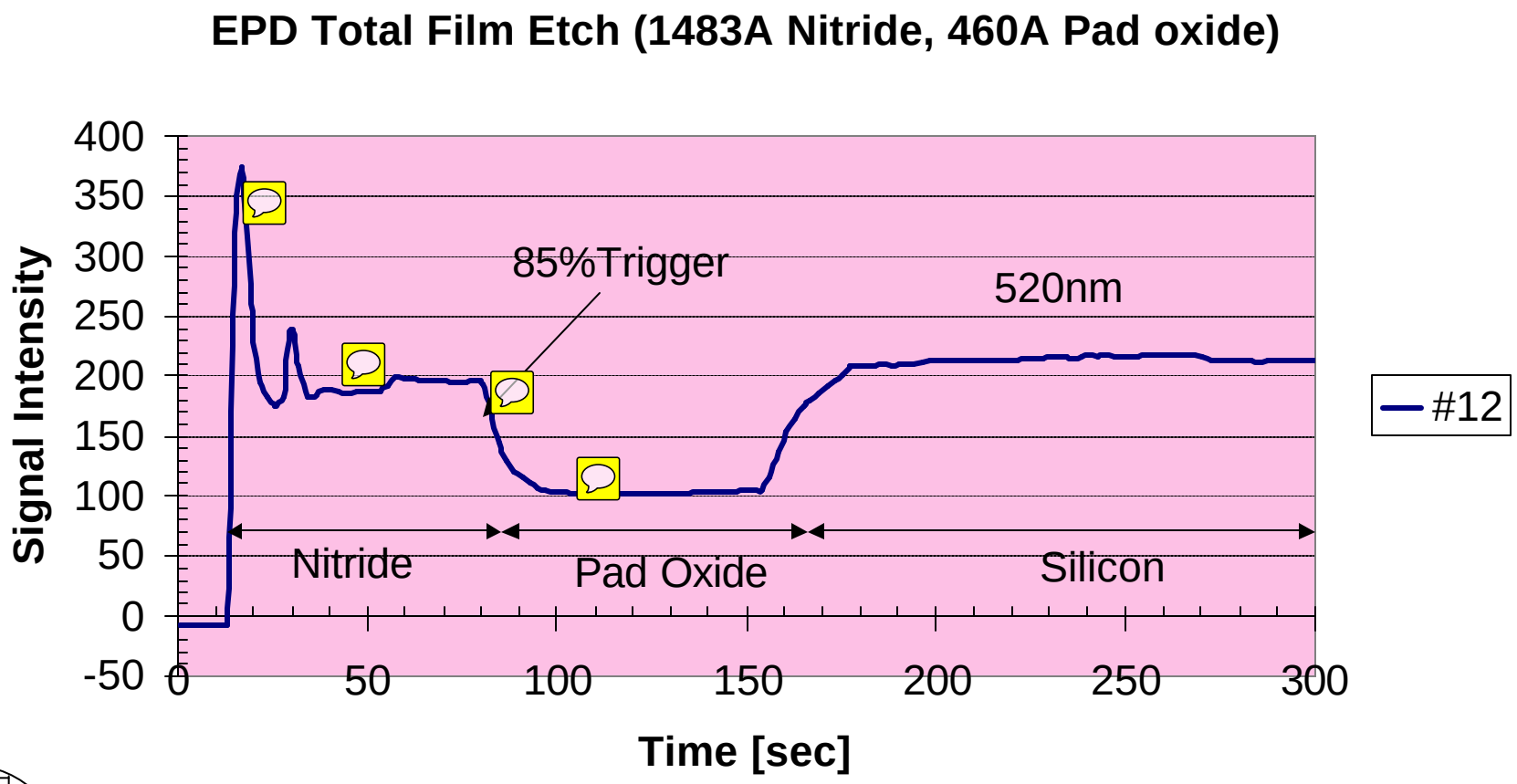


PLASMA ETCH TOOL

Lam 490 Etch Tool
Plasma Etch Nitride (~ 1500 Å/min)
SF6 flow = 200 sccm
Pressure= 260 mTorr
Power = 125 watts
Time=thickness/rate

Use end point detection capability
This system has filters at 520 nm and 470 nm. In any case the color of the plasma goes from pink/blue to white/blue once the nitride is removed.

LAM 490 END POINT



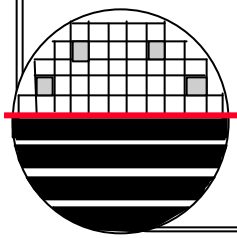
LAM 490 END POINT

Process: Step 1 – 260mTorr; 125W,
200sccm SF6,
Max Time = 2 min, Time Only

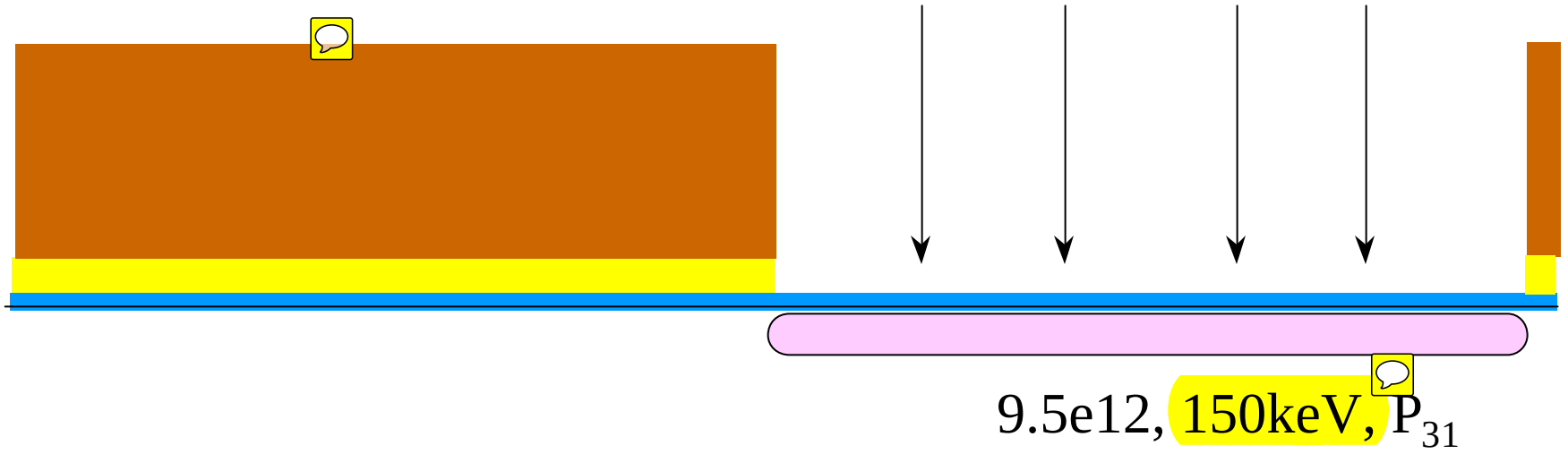
Process: Step 2 – 260mTorr; 125W,
200sccm SF6,
Max Time = 2min 20sec, Enpoint & Time

Process: Step 3 – 260mTorr; 125W,
200sccm SF6,
Overetch – 40%

Endpoint Parameters – Sampling A (ch12 @ 520nm)
Active during step 02
Delay 50sec before normalizing
Normalize for 10sec
Trigger at 85%



N-WELL IMPLANT



9.5e12, 150keV, P_{31}

Substrate 10 ohm-cm

IMPLANT MASKING THICKNESS CALCULATOR

Rochester Institute of Technology					Lance Barron		
Microelectronic Engineering					Dr. Lynn Fuller		
11/20/04							

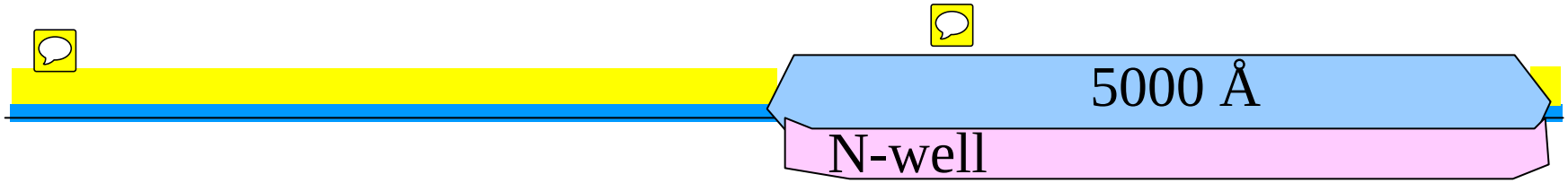
IMPLANT MASK CALCULATOR **Enter 1 - Yes 0 - No in white boxes**

DOPANT SPECIES		MASK TYPE		ENERGY	
B11	1	Resist	0	40	KeV
BF2	0	Poly	1		
P31	0	Oxide	0		
		Nitride	0		

Thickness to Mask >1E15/cm3 Surface Concentration 2961.954 Angstroms

VARIAN 350 D ION IMPLANTER (4" AND 6" WAFERS)

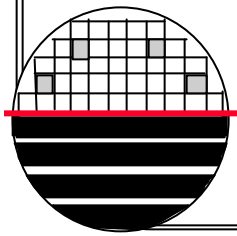
PHOTORESIST ASH, RCA CLEAN AND, N-WELL MASKING OXIDE GROWTH



Oxide, 5000A

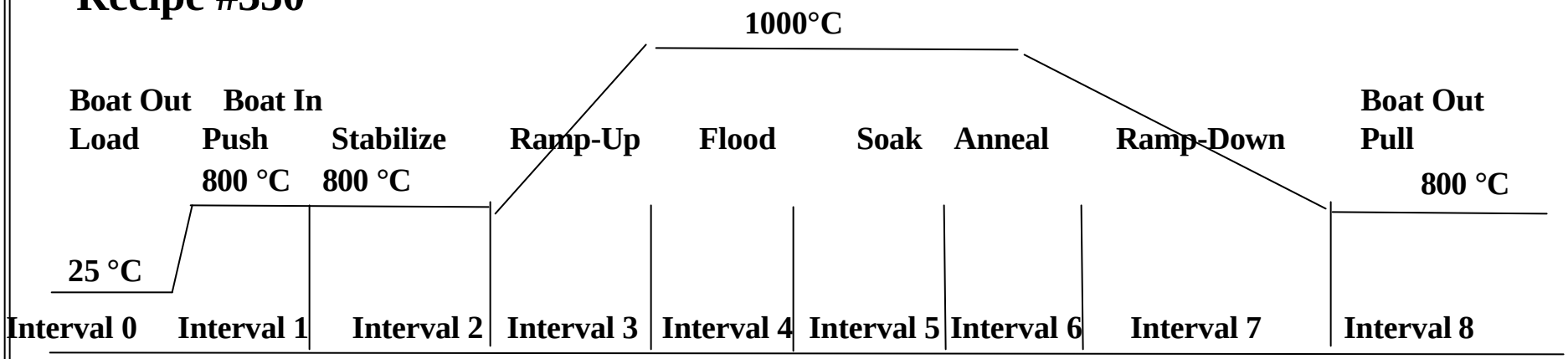
Bruce Furnace01 Recipe 350

Substrate 10 ohm-cm



BRUCE FURNACE RECIPE 350

Recipe #350

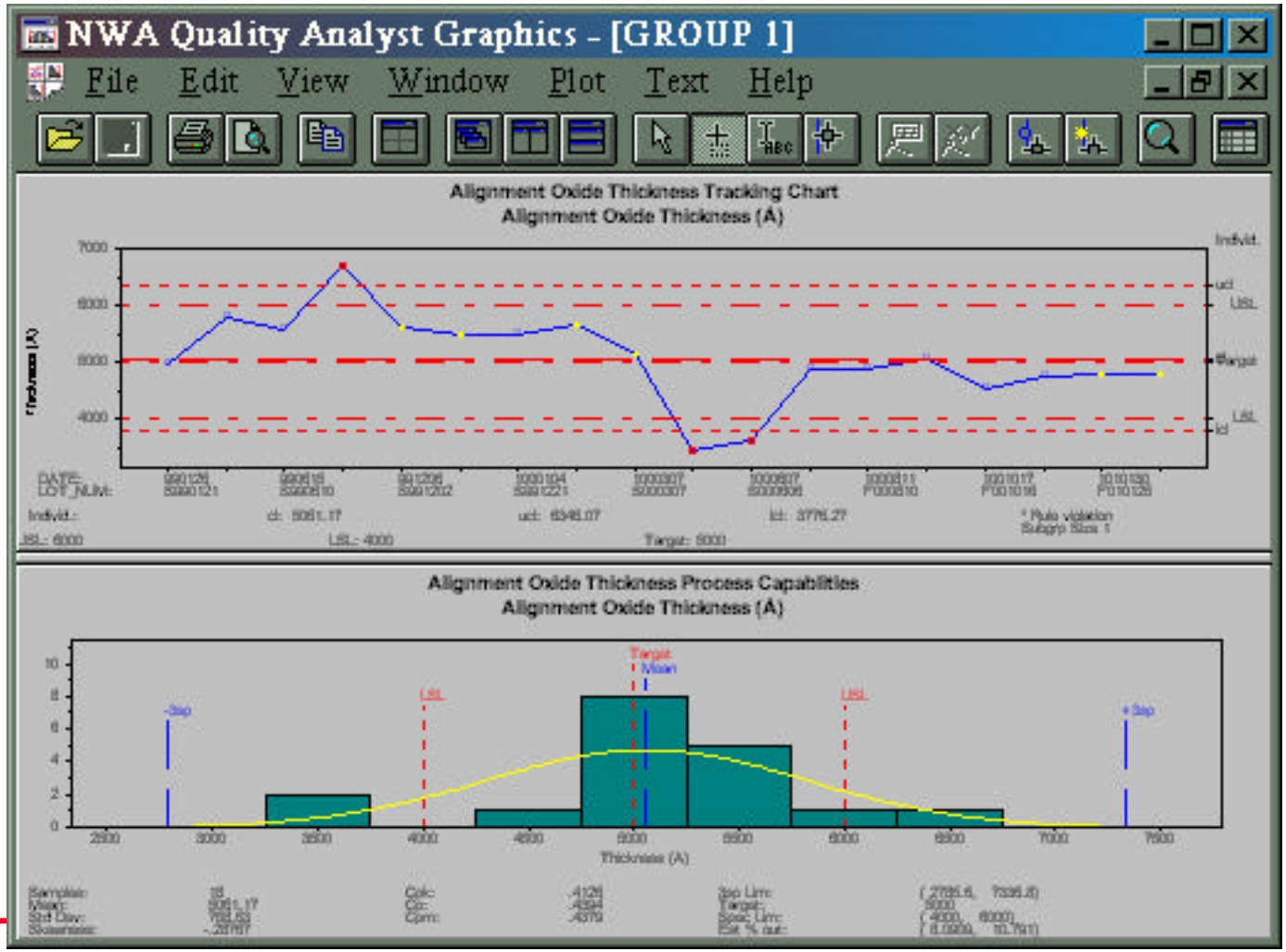


Any	12 min	15 min	20 min	5 min	100min	5 min	40 min	12 min
0 lpm	10 lpm	10 lpm	5 lpm	5 lpm	10 lpm	15 lpm	10 lpm	15 lpm
none	N2	N2	N2	O2	O2/H2	N2	N2	N2

At the end of a run the furnace returns to Interval 0 which is set for boat out, 25 °C and no gas flow. The furnace waits in that state until someone aborts the current recipe or loads a new recipe.

Wet Oxide Growth, Target 5000 Å

SPC CHARTS


NWA Quality Analyst Graphics - [GROUP 1]
File Edit View Window Plot Text Help
Alignment Oxide Thickness Tracking Chart
Alignment Oxide Thickness (A)
Alignment Oxide Thickness Process Capabilities
Alignment Oxide Thickness (A)
Thickness (A)

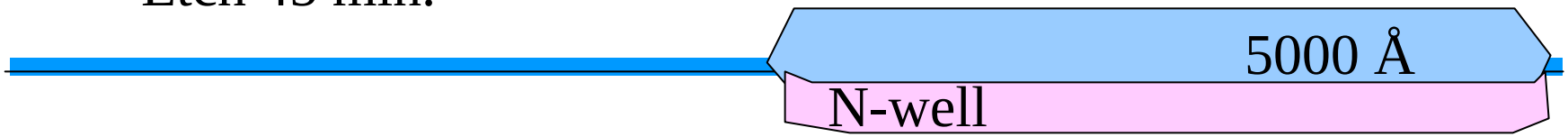
MEGASONIC RCA CLEAN, SRD & ASHER

RCA Clean Bench

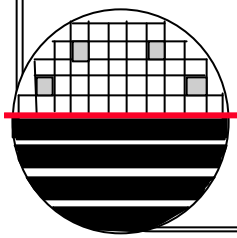
Branson Asher

WET ETCH NITRIDE

Hot Phosphoric Acid
Wet Nitride Etch.
Etch Rate ~50 Å/min
Etch 45 min.



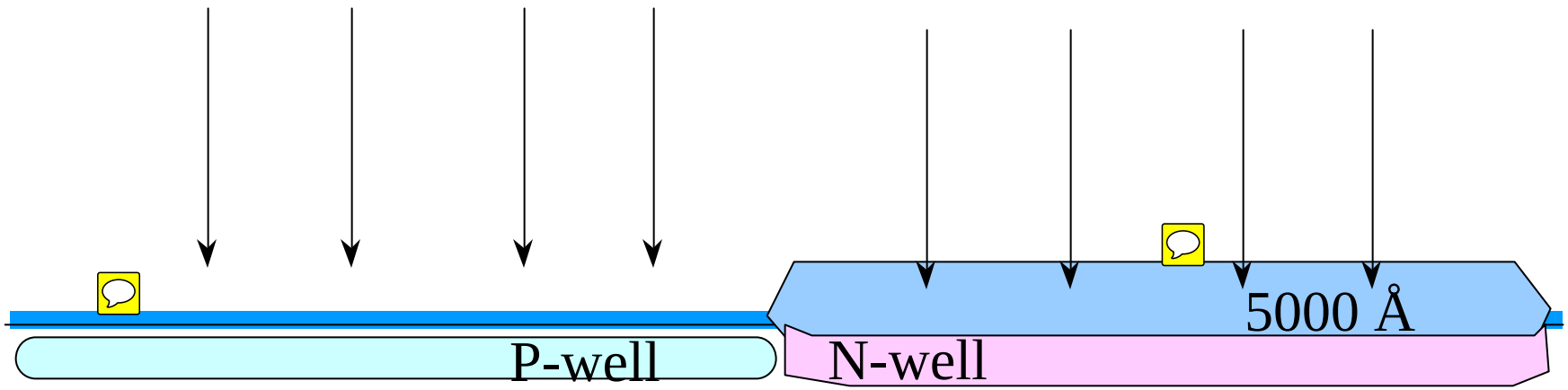
Substrate 10 ohm-cm



HOT PHOSPHORIC ACID ETCH BENCH

- Include D1-D3
- Warm up Hot Phos pot to 175º
- Use Teflon boat to place wafers in acid bath
  - 3500Å +/-500 → 90 minutes
  - 1500Å +/- 500 → 45 minutes
  - Etch rate of ~50 Å/min
- Rinse for 5 minutes in Cascade Rinse
- SRD wafers

IMPLANT P-WELL



2e13, 50keV, B_{11}

Substrate 10 ohm-cm

IMPLANT MASKING THICKNESS CALCULATOR

Rochester Institute of Technology					Lance Barron		
Microelectronic Engineering					Dr. Lynn Fuller		
11/20/04							

IMPLANT MASK CALCULATOR **Enter 1 - Yes 0 - No in white boxes**

DOPANT SPECIES

B11	1
BF2	0
P31	0

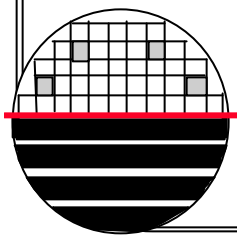
MASK TYPE

Resist	0
Poly	1
Oxide	0
Nitride	0

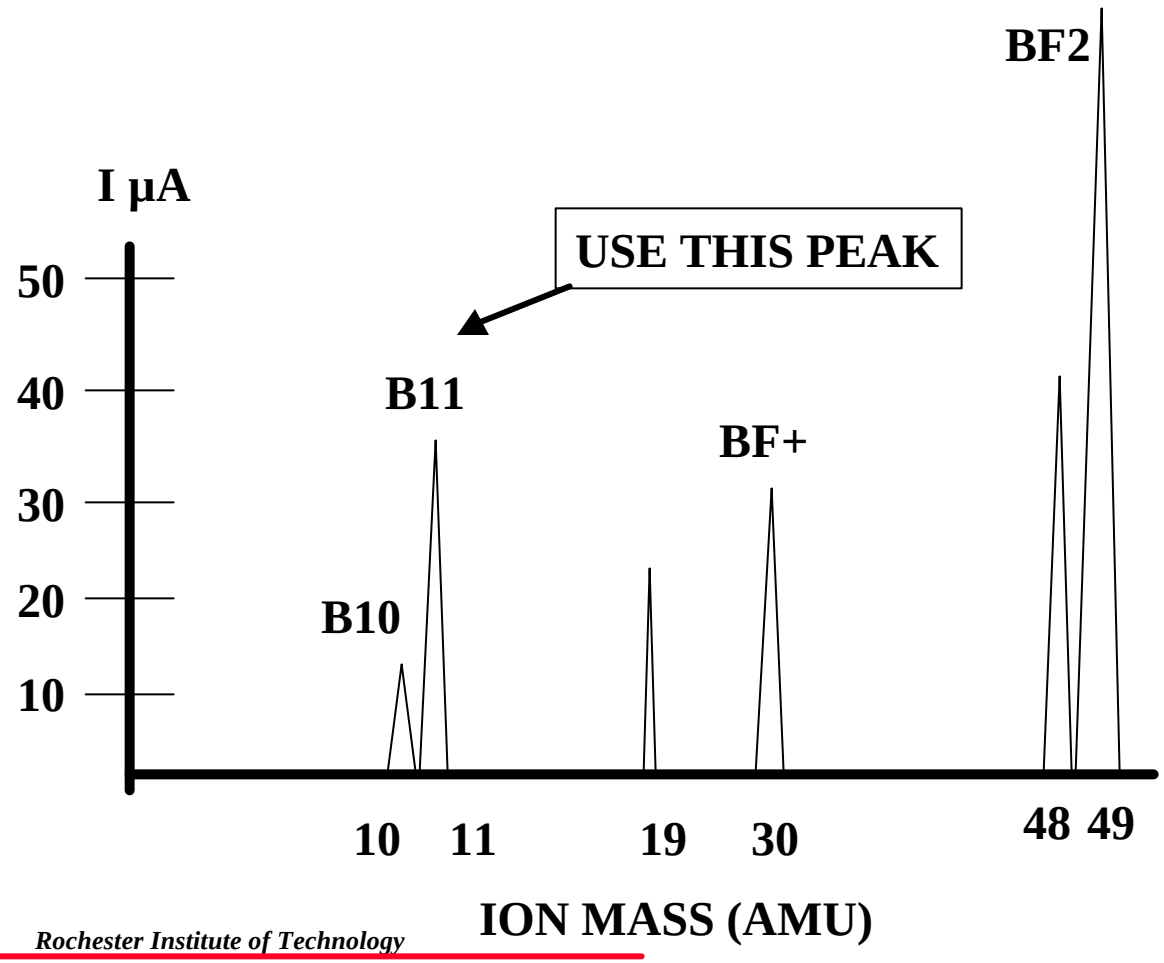
ENERGY

40 KeV

Thickness to Mask >1E15/cm3 Surface Concentration 2961.954 Angstroms

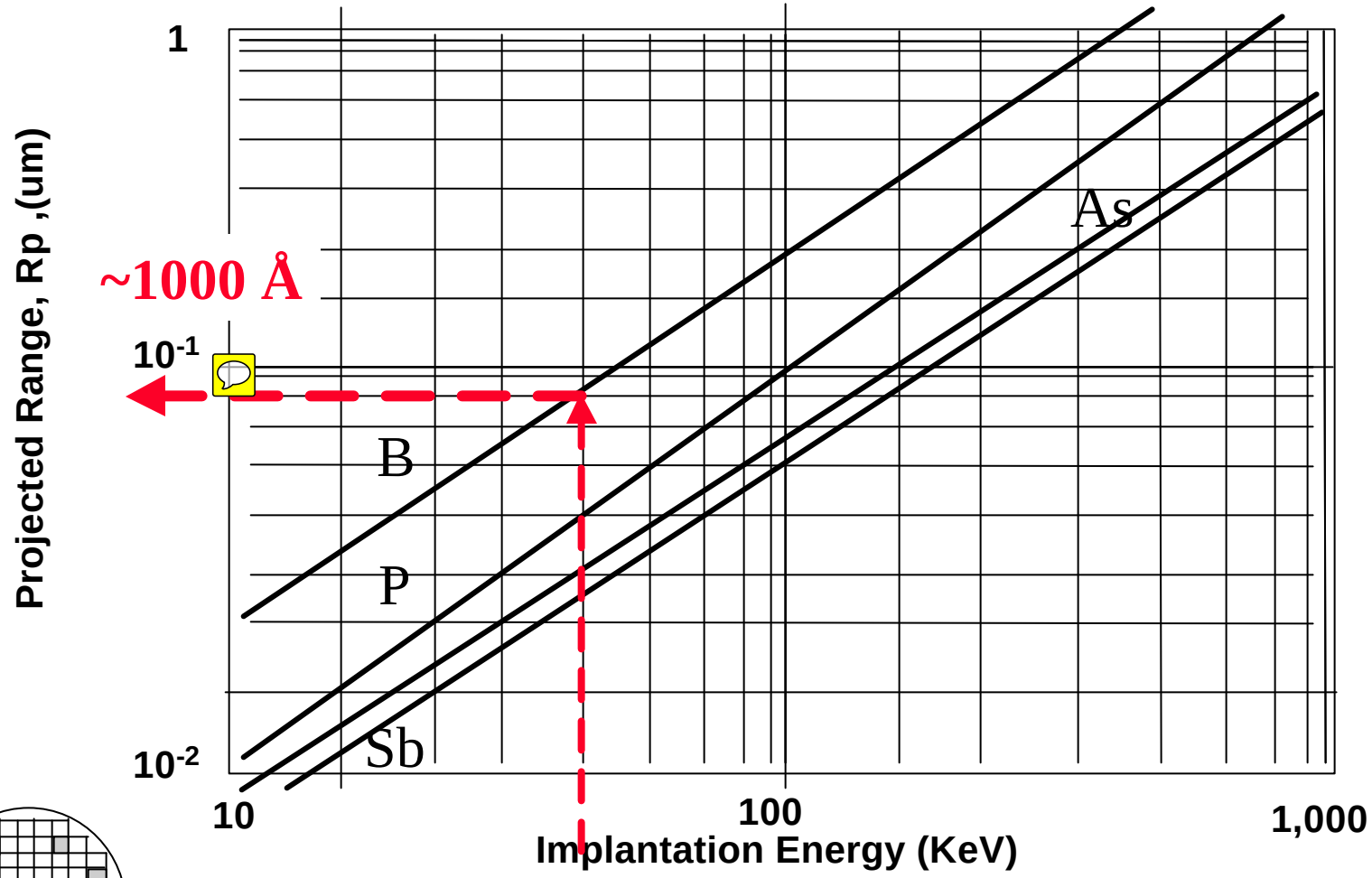


B_{11} IMPLANT FOR BORON THRESHOLD ADJUSTS, STOP, P-WELL



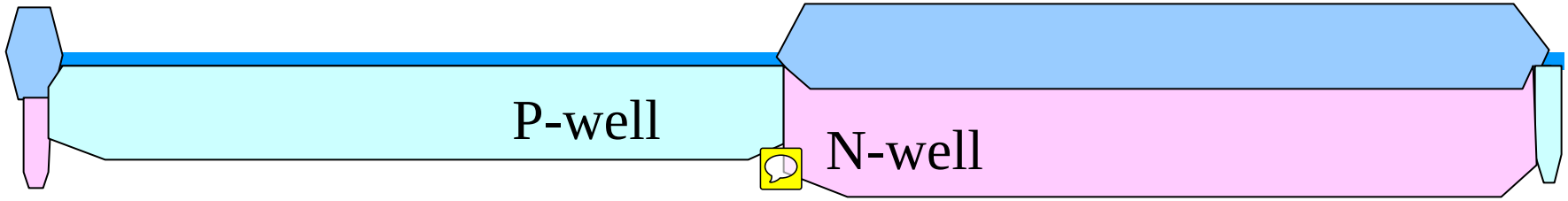
PLAY

ION IMPLANT RANGE CHART



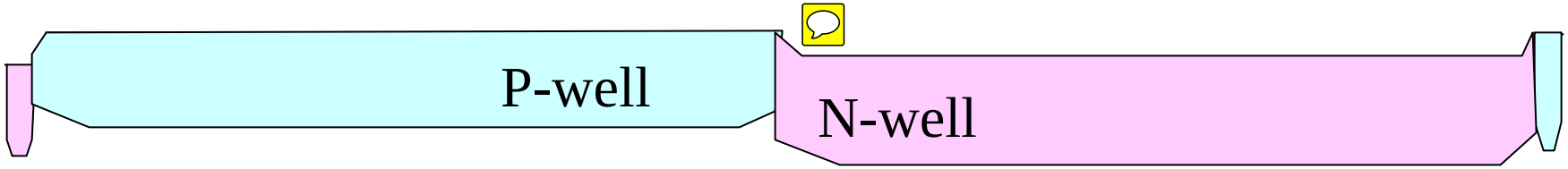
WELL DRIVE

1100 C, 8 Hours, N2



Substrate 10 ohm-cm

ETCH ALL OXIDE

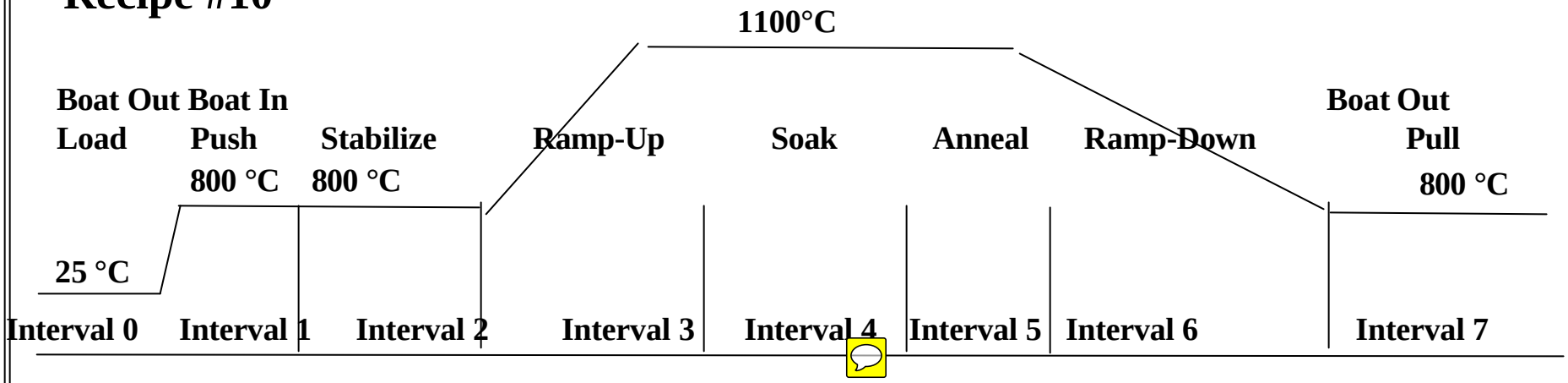


Substrate 10 ohm-cm

BRUCE FURNACE RECIPE 10 SUB-CMOS WELL DRIVE

Verified:12-8-04

Recipe #10



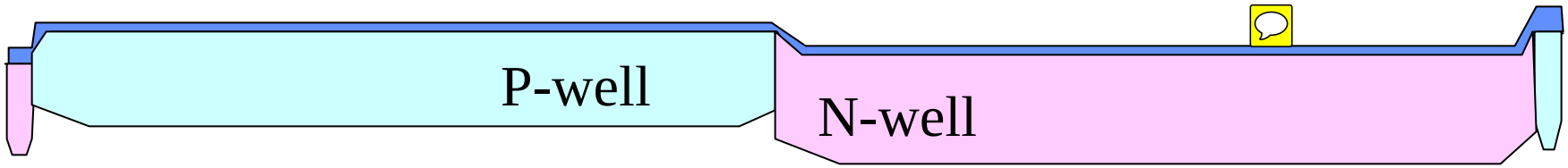
Any	12 min	15 min	30 min	600 min	5 min	60 min	12 min
0 lpm	10 lmp	10 lpm	10 lpm	10 lpm	10 lpm	10 lpm	5 lpm
none	N2	N2	N2	N2	N2	N2	N2

At the end of a run the furnace returns to Interval 0 which is set for boat out, 25 °C and no gas flow. The furnace waits in that state until someone aborts the current recipe or loads a new recipe.

Sub-CMOS Well Drive, No Oxide Growth, Tube 1

GROW PAD OXIDE

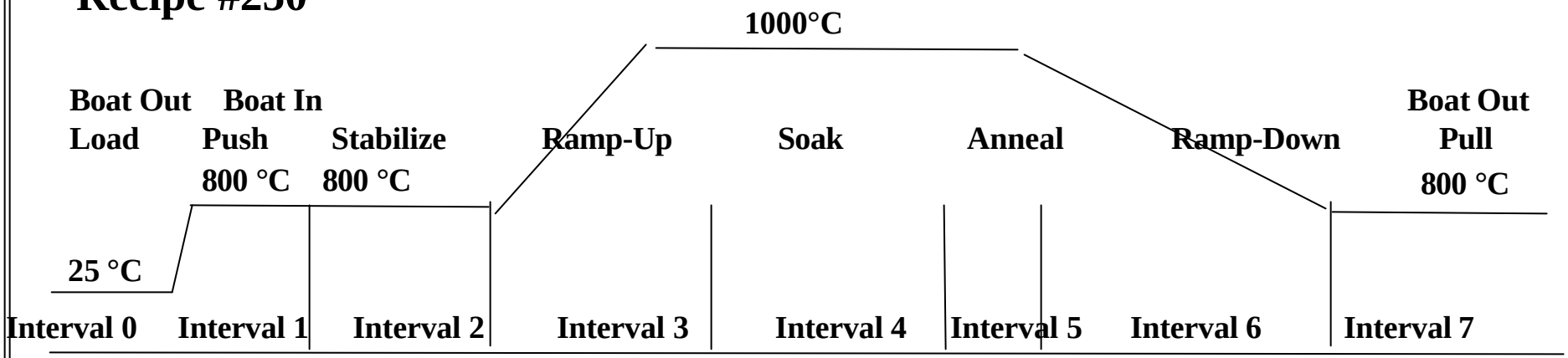
Pad Oxide, 500A
Bruce Furnace 01 Recipe 250



Substrate 10 ohm-cm

BRUCE FURNACE RECIPE 250 500Å DRY OXIDE

Recipe #250

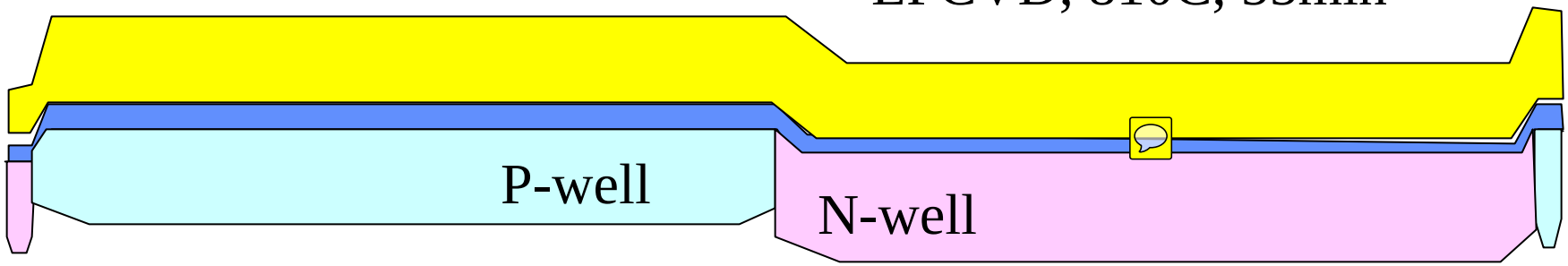


Any	12 min	15 min	20 min	40min	5min	40 min	12 min
0 lpm	10 lpm	10 lpm	5 lpm	10 lpm	15 lpm	10 lpm	5 lpm
none	N2	N2	O2	O2	N2	N2	N2

At the end of a run the furnace returns to Interval 0 which is set for boat out, 25 °C and no gas flow. The furnace waits in that state until someone aborts the current recipe or loads a new recipe.

DEPOSIT NITRIDE

Nitride, **3500A**
LPCVD, 810C, 55min



Substrate 10 ohm-cm

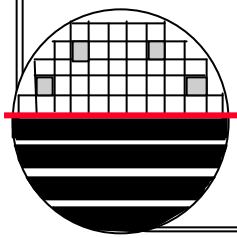
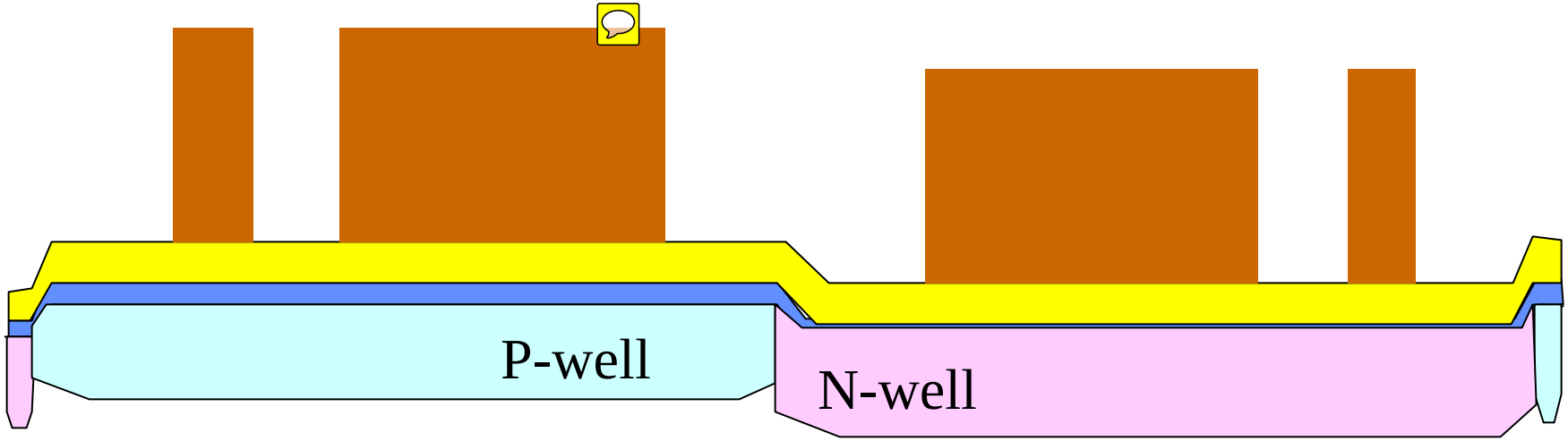
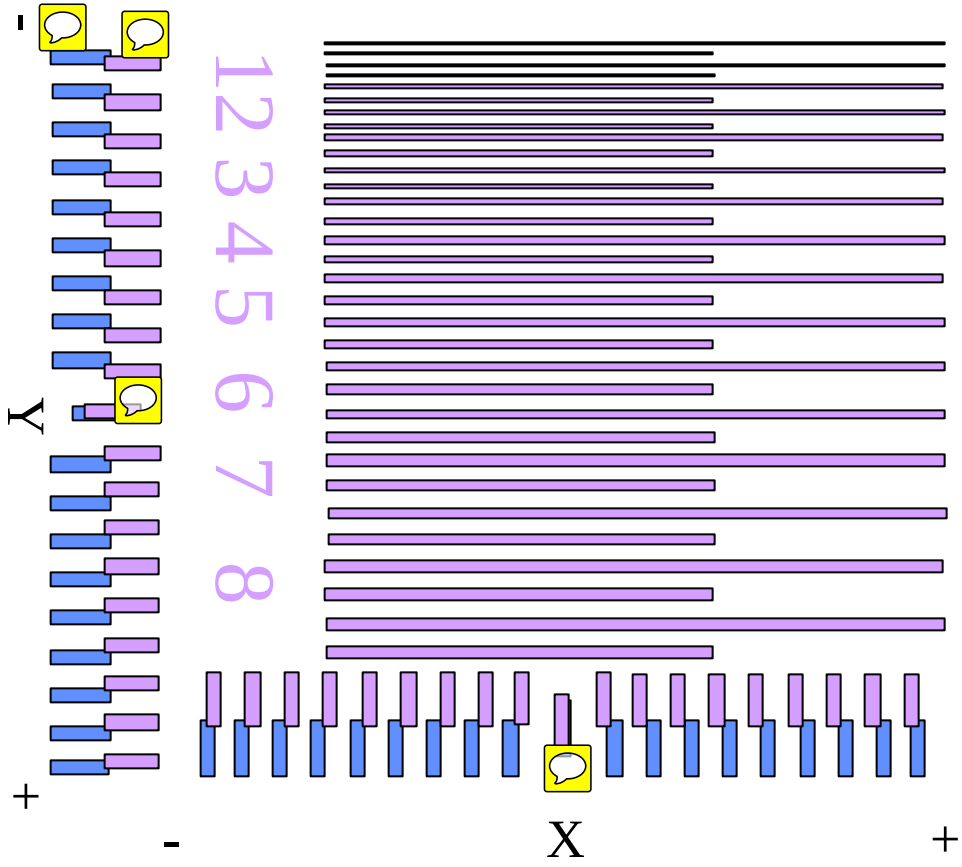


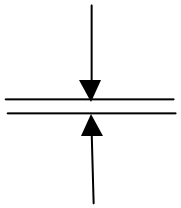
PHOTO 2 ACTIVE

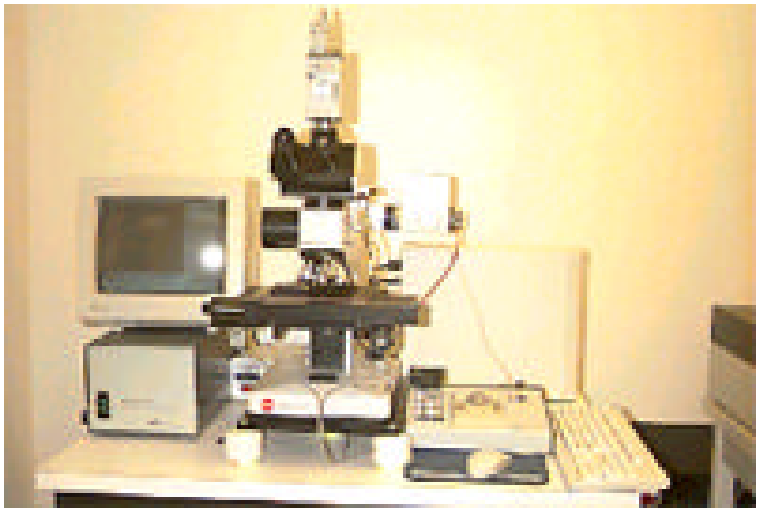


Substrate 10 ohm-cm

ALIGNMENT VERNIERS
CRITICAL DIMENSION (CD) STRUCTURES

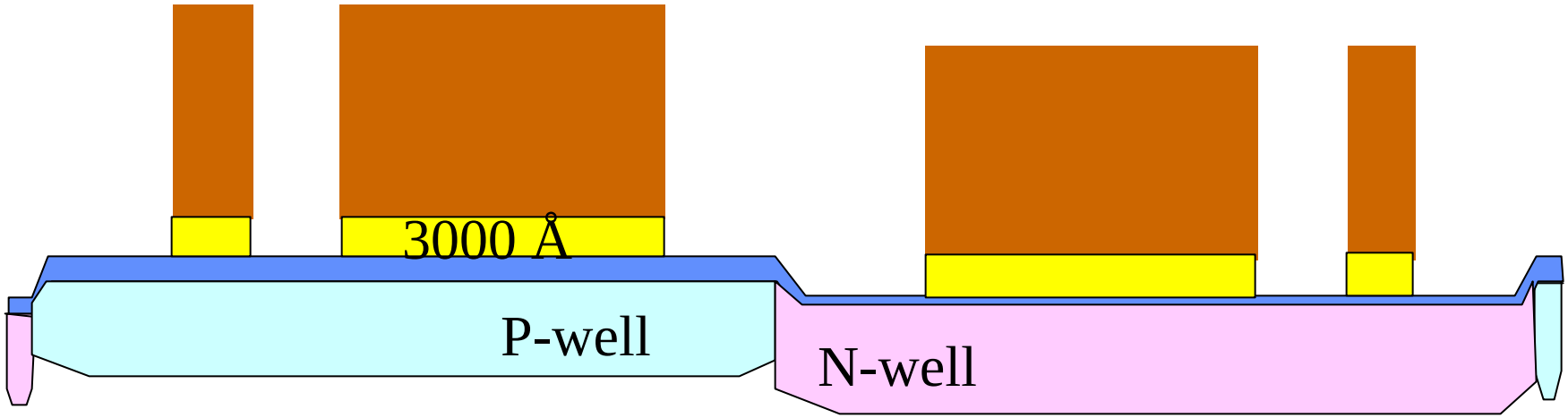






PLAY

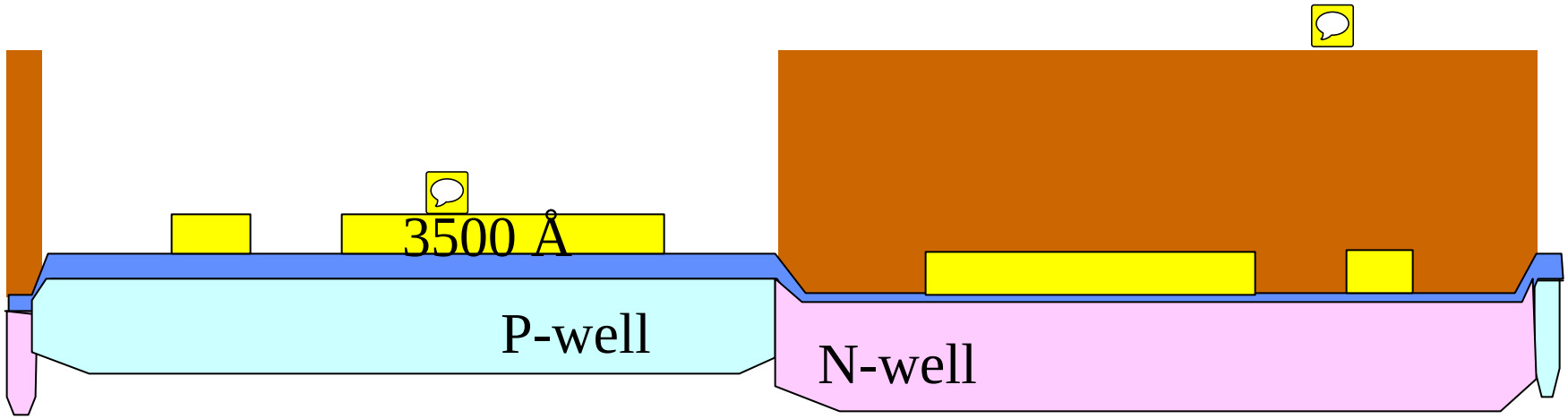
ETCH NITRIDE



Substrate 10 ohm-cm

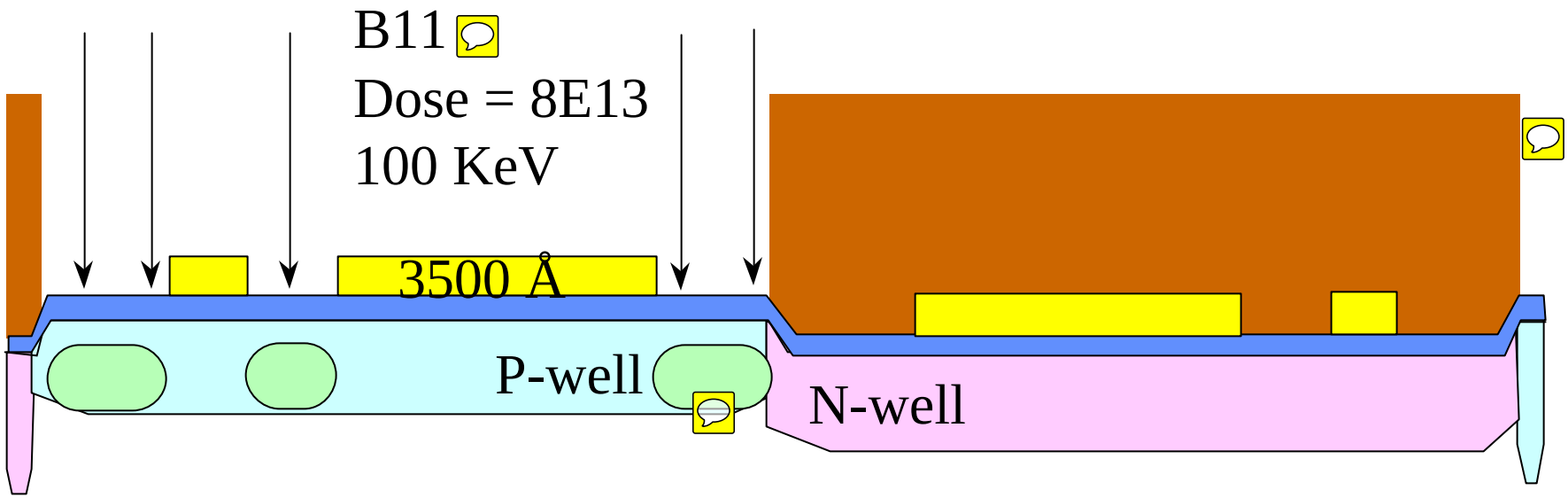
Nitride Etch: 200 sec, SF_6 plasma

PHOTO 3 CHANNEL STOP



N-type Substrate 10 ohm-cm

CHANNEL STOP IMPLANT



Substrate 10 ohm-cm

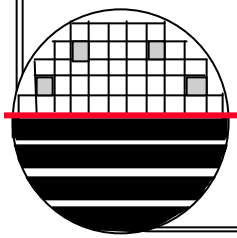
IMPLANT MASKING THICKNESS CALCULATOR

Rochester Institute of Technology					Lance Barron		
Microelectronic Engineering					Dr. Lynn Fuller		
11/20/04							

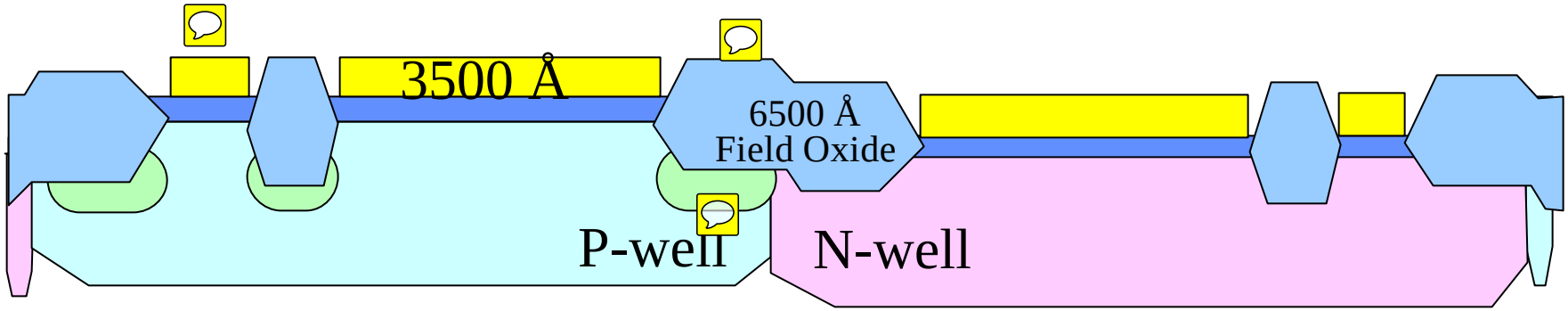
IMPLANT MASK CALCULATOR **Enter 1 - Yes 0 - No in white boxes**

DOPANT SPECIES		**MASK TYPE**		**ENERGY**	
B11	1	Resist	0	40	KeV
BF2	0	Poly	1		
P31	0	Oxide	0		
		Nitride	0		

Thickness to Mask >1E15/cm3 Surface Concentration 2961.954 Angstroms



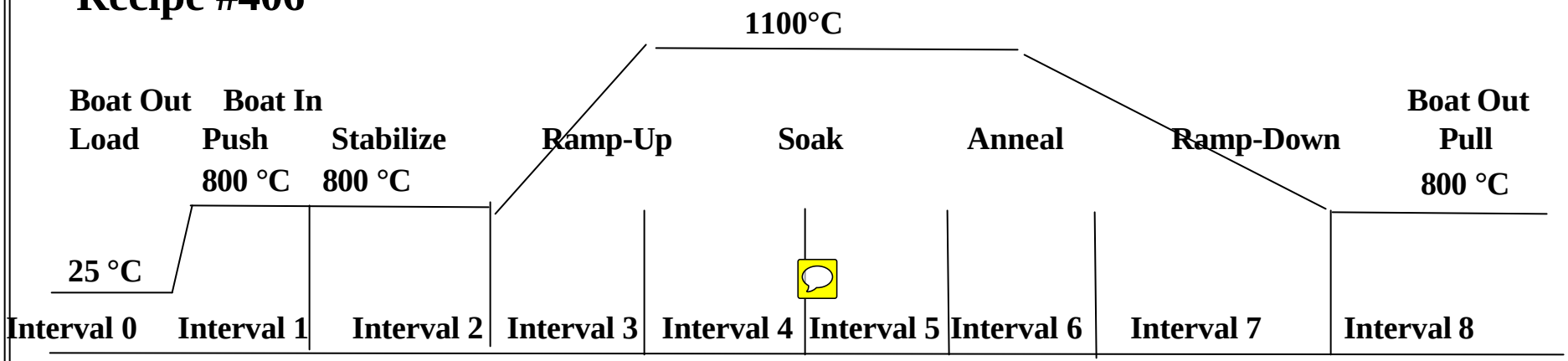
GROW FIELD OXIDE



N-type Substrate 10 ohm-cm

BRUCE FURNACE RECIPE 406 – WET OXIDE 6,500Å

Recipe #406

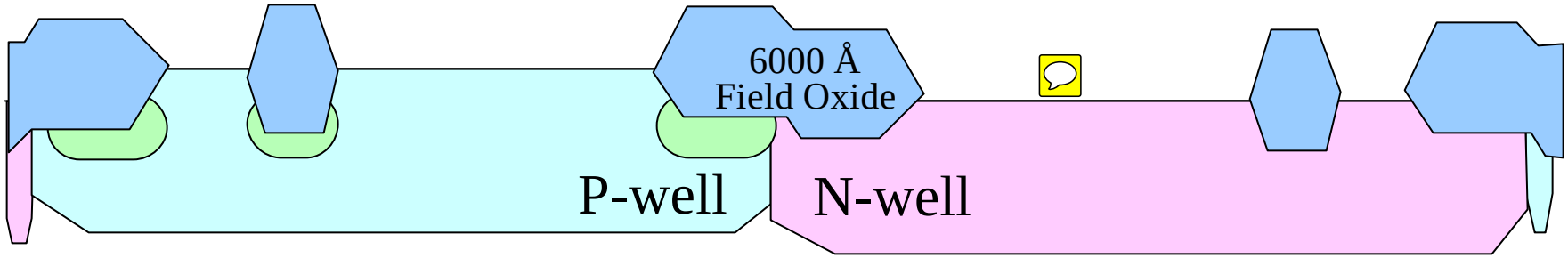


Any	12 min	15 min	30 min	5 min	65 min	5 min	60 min	12 min
0 lpm	10 lpm	10 lpm	5 lpm	5 lpm	10 lpm	15 lpm	10 lpm	15 lpm
none	N2	N2	N2	O2	O2/H2	N2	N2	N2

At the end of a run the furnace returns to Interval 0 which is set for boat out, 25 °C and no gas flow. The furnace waits in that state until someone aborts the current recipe or loads a new recipe.

Wet Oxide Growth, Target 6,500 Å

ETCH NITRIDE AND PAD OXIDE



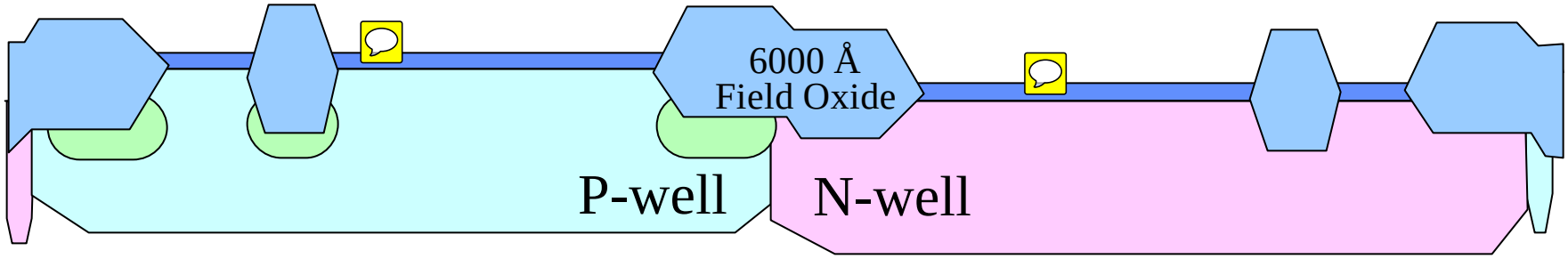
N-type Substrate 10 ohm-cm

HOT PHOSPHORIC ACID ETCH BENCH

- Include D1-D3
- Warm up Hot Phos pot to 175º
- Use Teflon boat to place wafers in acid bath
  - 3500Å +/-500 → 90 minutes
  - 1500Å +/- 500 → 45 minutes
  - Etch rate of ~50 Å/min
- Rinse for 5 minutes in Cascade Rinse
- SRD wafers

GROW SACRIFICIAL OXIDE (KOOI OXIDE)

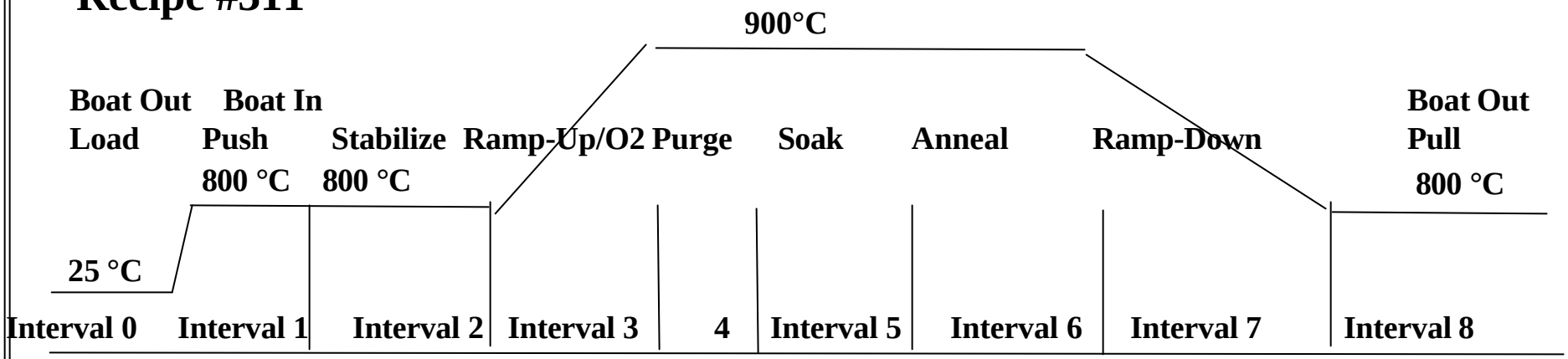
1000 Å Oxide, 900A, Wet O_2
Bruce Furnace01 Recipe 311:



N-type Substrate 10 ohm-cm

BRUCE FURNACE RECIPE 311 – WET OXIDE 1,000Å

Recipe #311

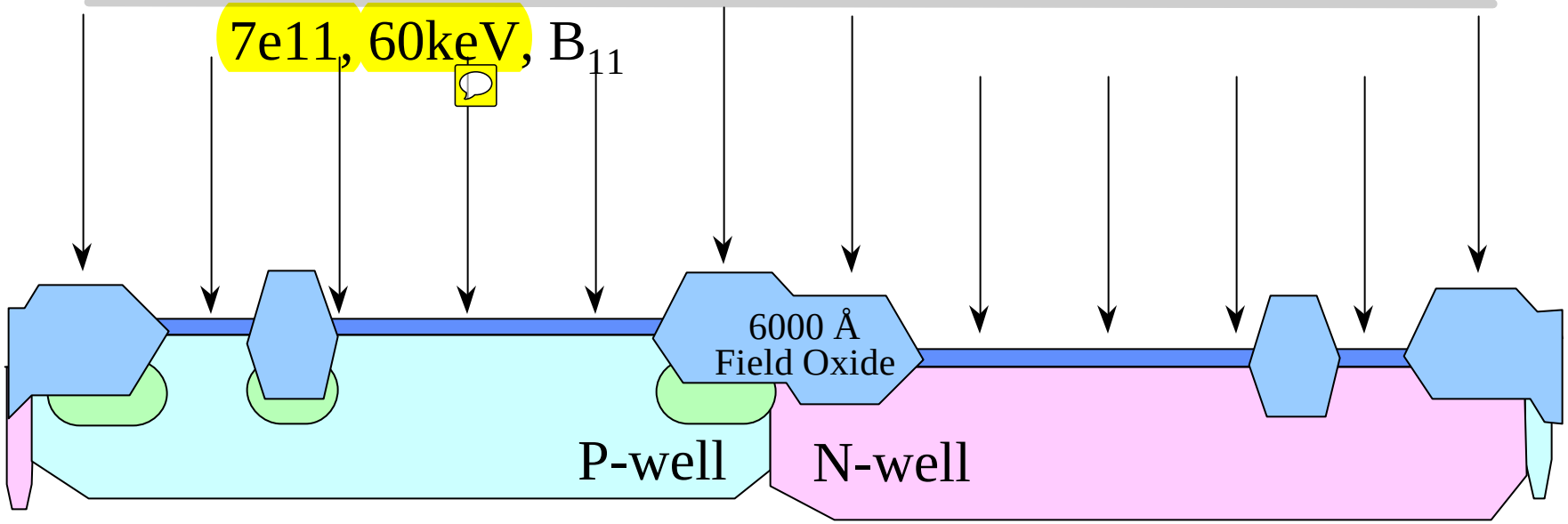


Any	12 min	15 min	10 min	5 min	40 min	5 min	15 min	15 min
0 lpm	15 lpm	15 lmp	10 lpm	10 lpm	10 lpm	15 lpm	10 lpm	15 lpm
none	N2	N2	O2	O2	O2/H2	N2	N2	N2

At the end of a run the furnace returns to Interval 0 which is set for boat out, 25 °C and no gas flow. The furnace waits in that state until someone aborts the current recipe or loads a new recipe.

Wet Oxide Growth, Target 1000 Å, Kooi

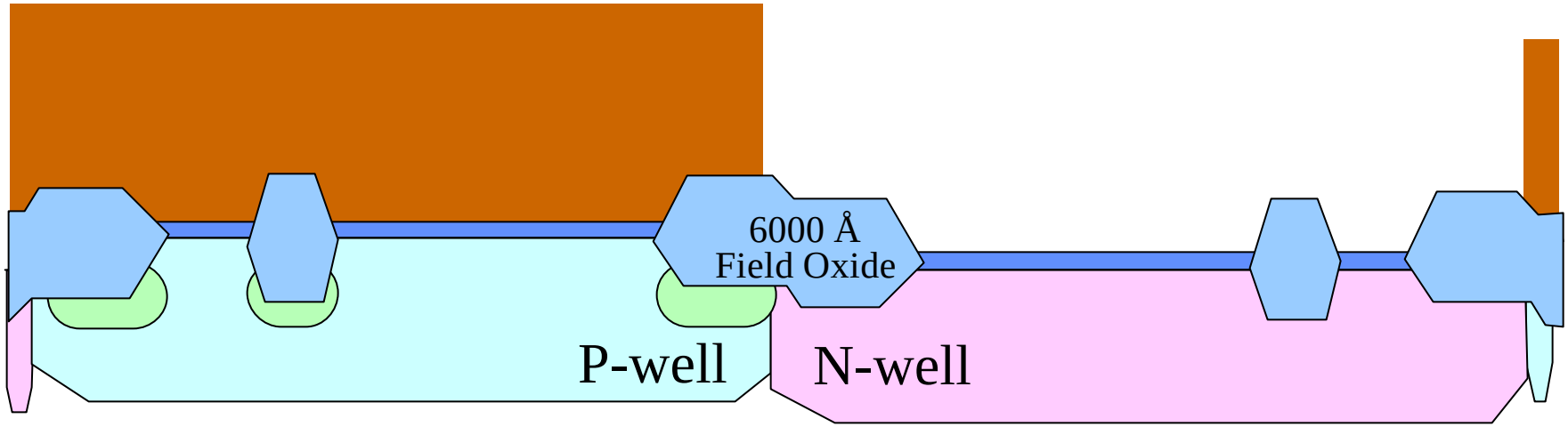
BLANKET PMOS & NMOS VT ADJUST IMPLANT



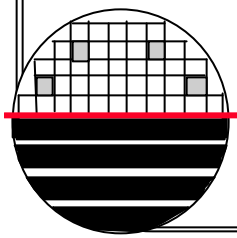
N-type Substrate 10 ohm-cm

Note: This implant may be omitted

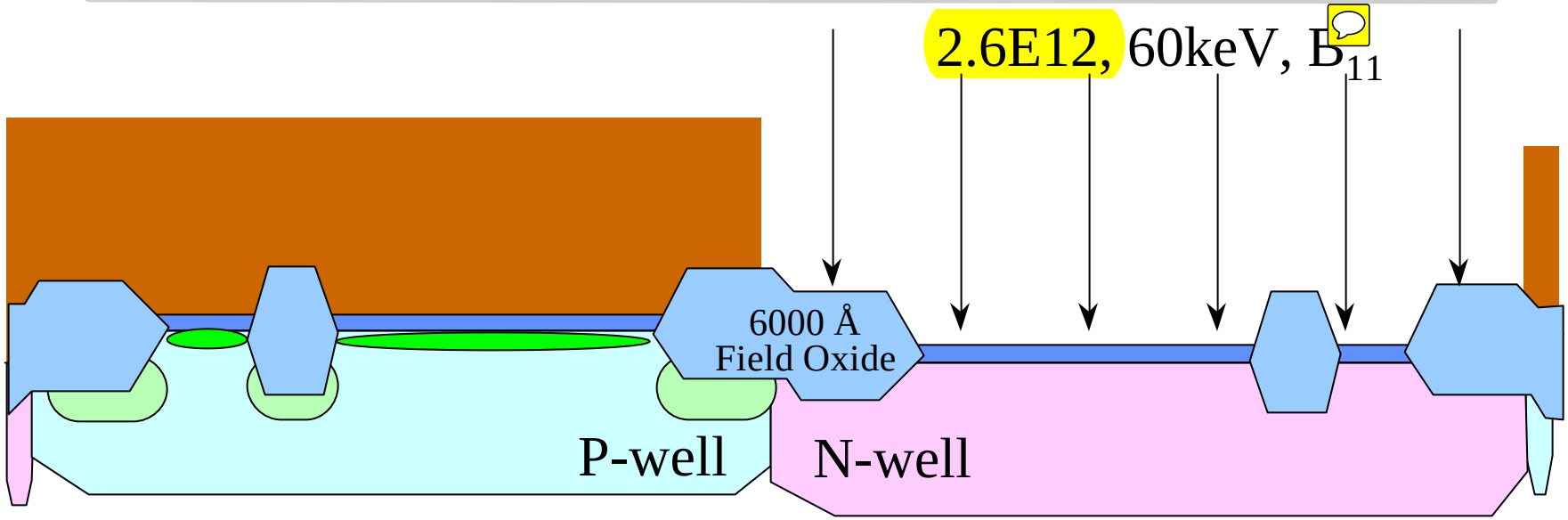
PHOTO 4 PMOS VT



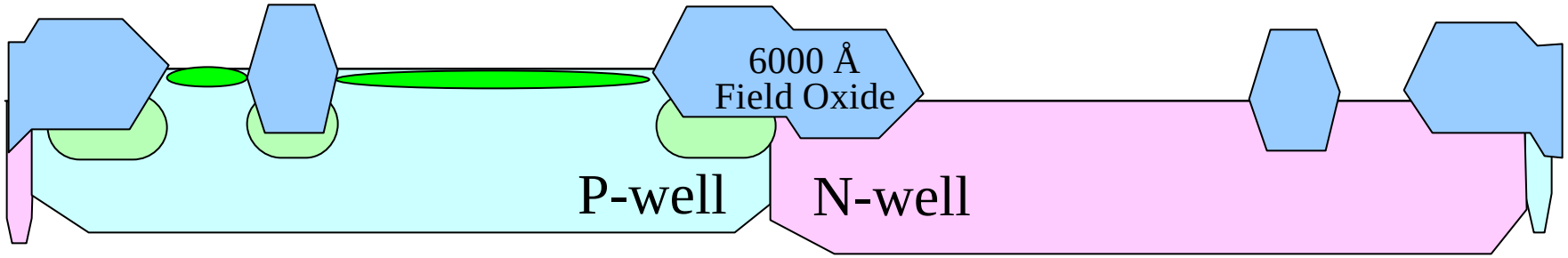
N-type Substrate 10 ohm-cm



PMOS VT IMPLANT



ASH RESIST, ETCH KOOI OXIDE, RCA CLEAN

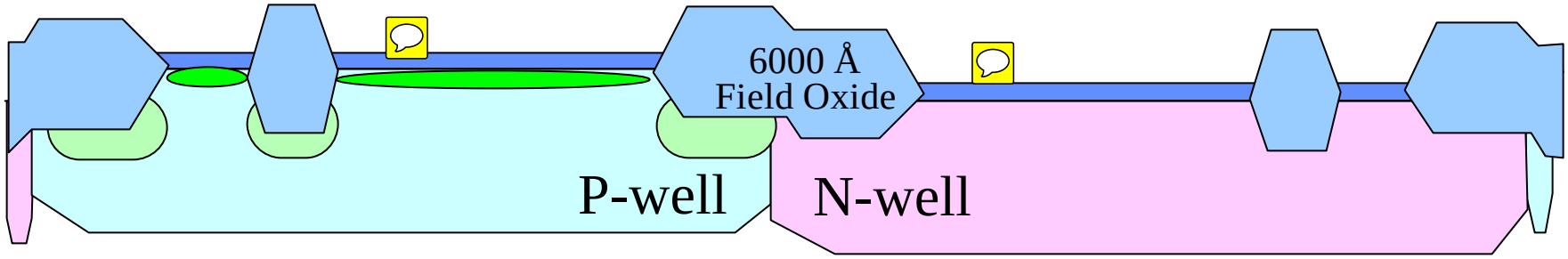


N-type Substrate 10 ohm-cm

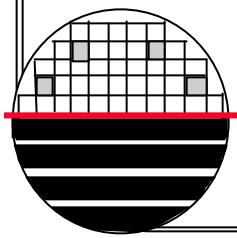
GROW GATE OXIDE

Oxide, 150A, Dry O_2

Bruce Furnace04 Recipe 215



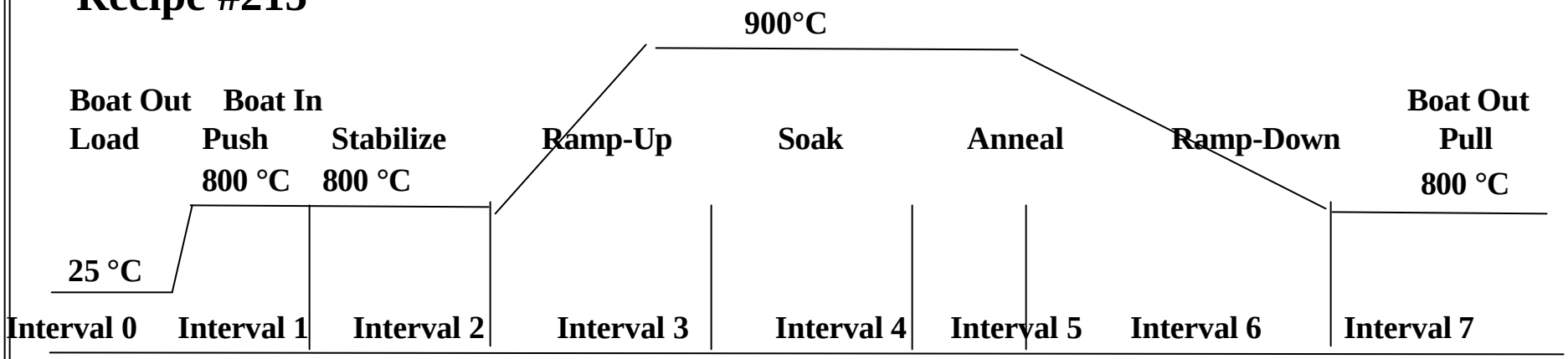
N-type Substrate 10 ohm-cm



BRUCE FURNACE RECIPE 215 – 150Å DRY OXIDE

Verified:2-24-04

Recipe #215



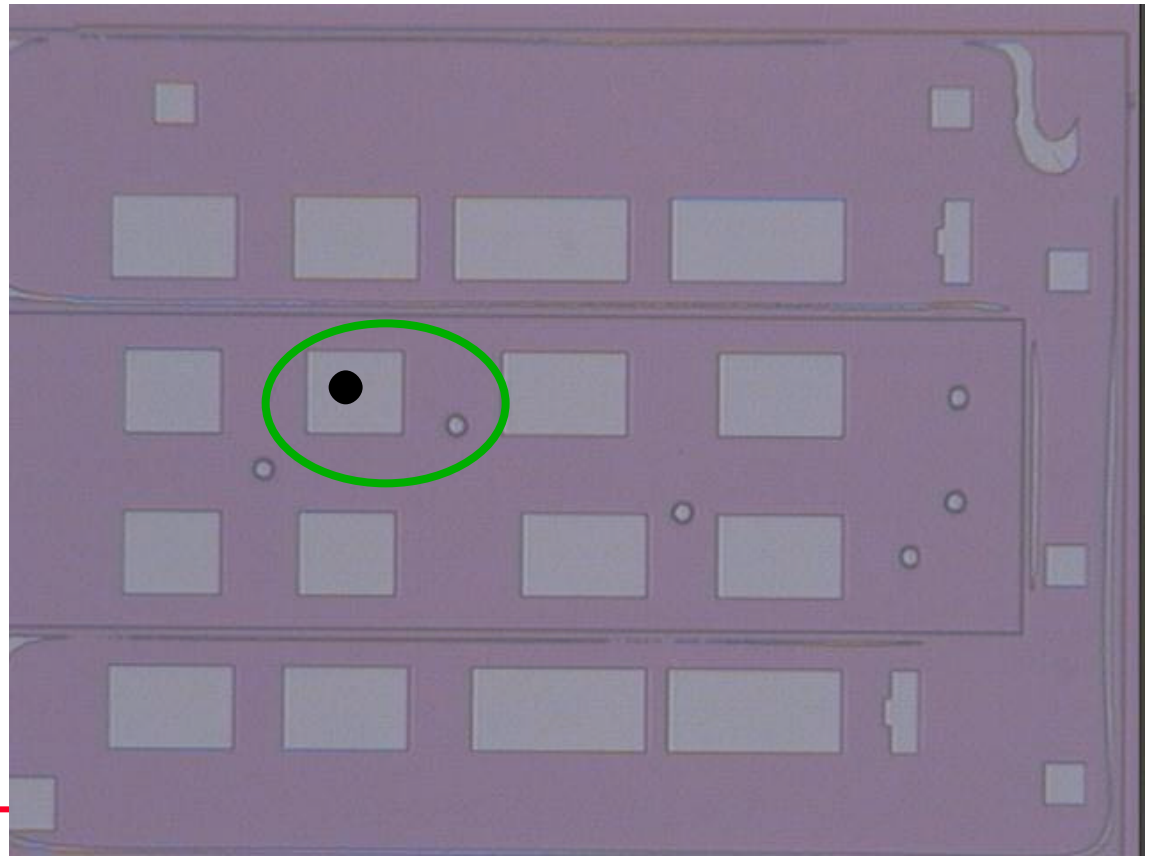
Any	12 min	15 min	10 min	45 min	5 min	20 min	15 min
0 lpm	10 lpm	10 lmp	5 lpm	10 lpm	15 lpm	10 lpm	5 lpm
none	N2	N2	O2	O2	N2	N2	N2

At the end of a run the furnace returns to Interval 0 which is set for boat out, 25 °C and no gas flow. The furnace waits in that state until someone aborts the current recipe or loads a new recipe.

Dry Oxide Growth, Target 150 Å

LOCATION FOR MEASUREMENT OF GATE OXIDE

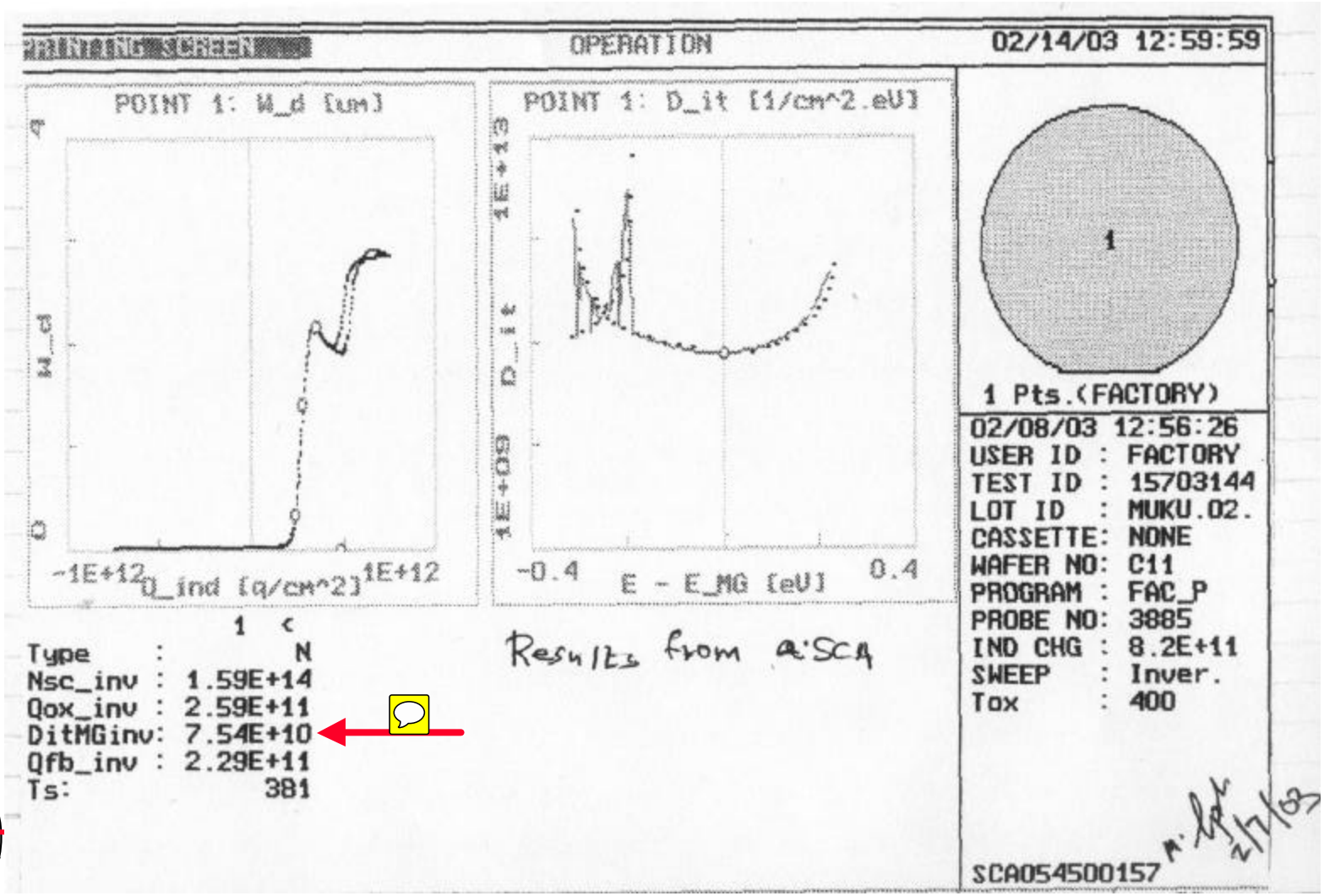
Measure gate oxide thickness (~150A) in any white active area



MEASURE C1 AND C2 ON SCA-2500

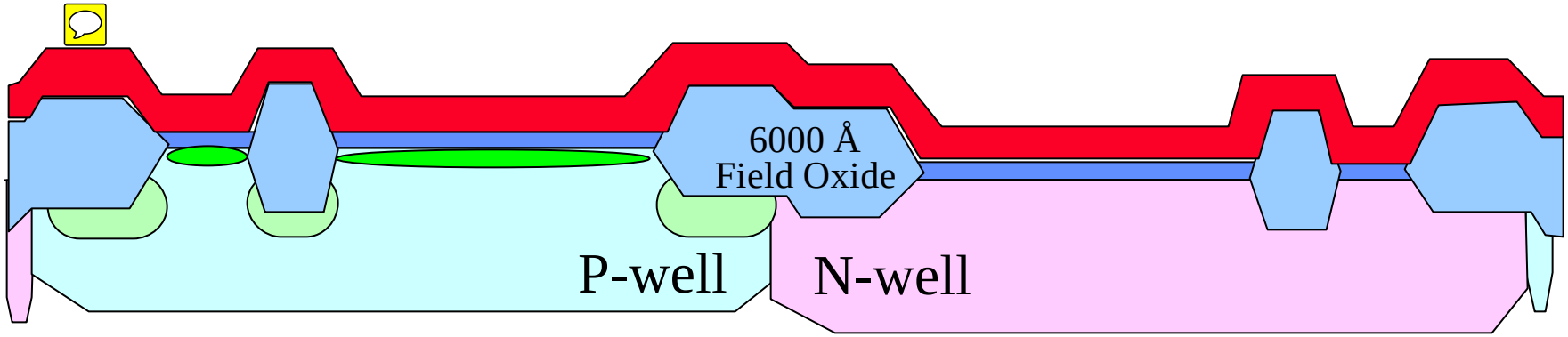
Login: FACTORY
Password: OPER
<F1> Operate
<F1> Test Center the wafer on the stage
Select (use arrow keys on the numeric pad (far right on the keyboard)
space bar, page up, etc)
PROGRAM = FAC-P or FAC-N
LOT ID = HAWAII
WAFER NO. = C1
TOX = 250 (from nanospec)
<F12> start test and wait for measurement
<Print Screen> print results
<F8> exit and log off
<ESC> can be used anytime, but wait for current test to be completed

SCA MEASUREMENT OF GATE OXIDE



LPCVD POLY

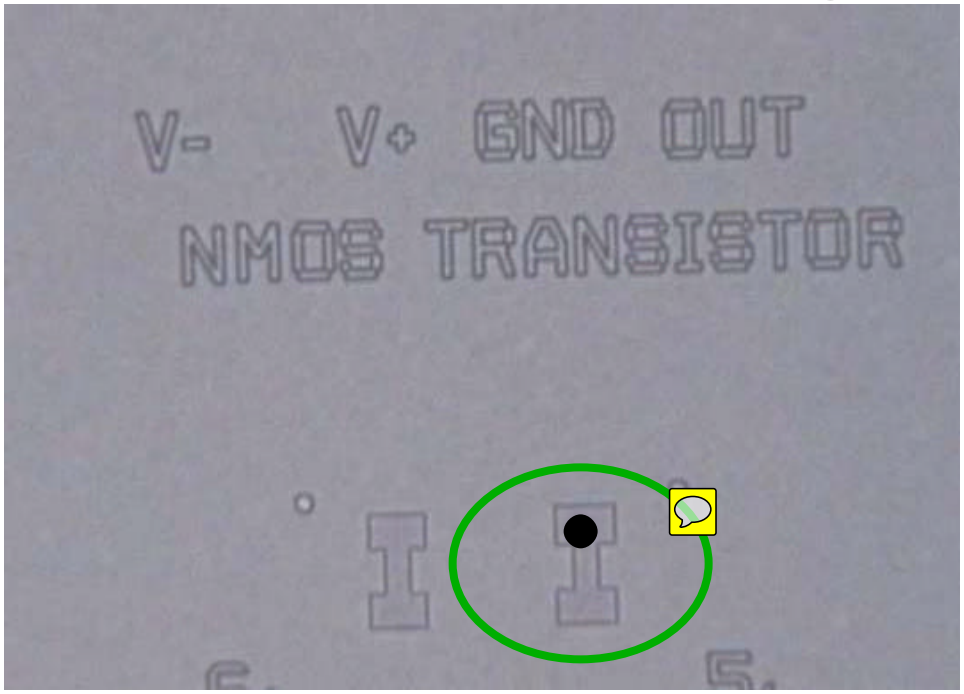
Polysilicon, 6000A
LPCVD, 610C, 78min



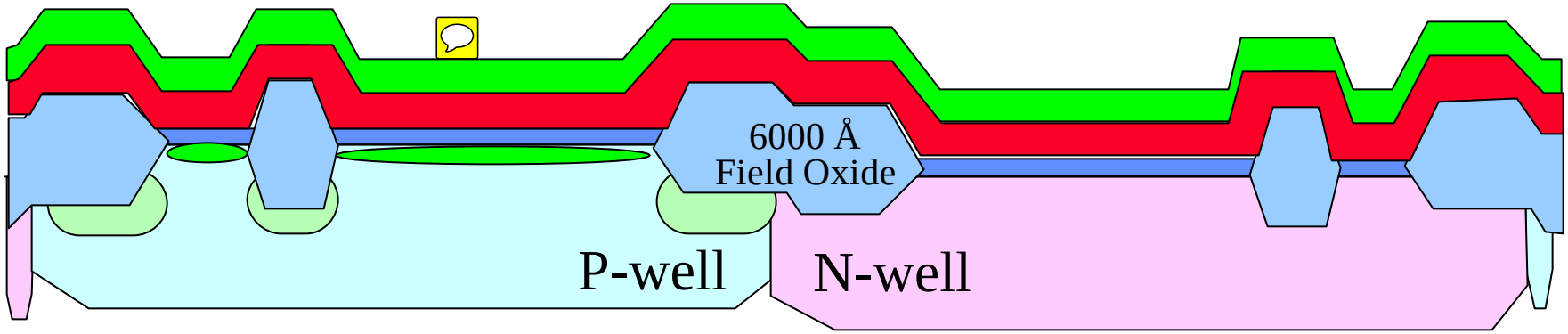
N-type Substrate 10 ohm-cm

LOCATION FOR POLY THICKNESS MEASUREMENT

Measure poly thickness within any active area using thin film stack #4 on nanospec at 40X magnification



POLYSILICON DOPING



Emulsitone N-250

3000rpm, 30sec

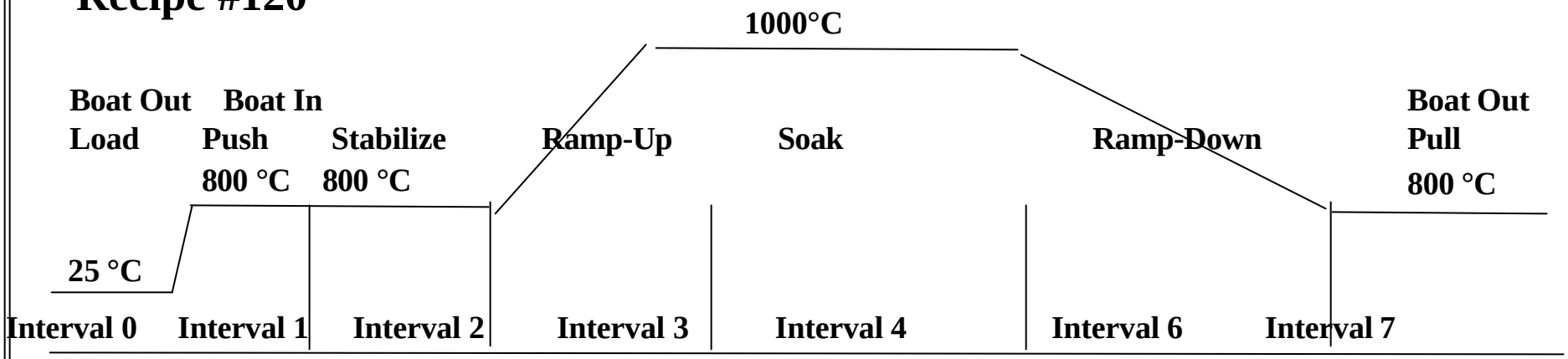
Bake, 200C, 15min

Use Bruce Furnace03
Recipe 120

BRUCE FURNACE RECIPE 120- N+ POLY DOPE

Verified:2-24-04

Recipe #120



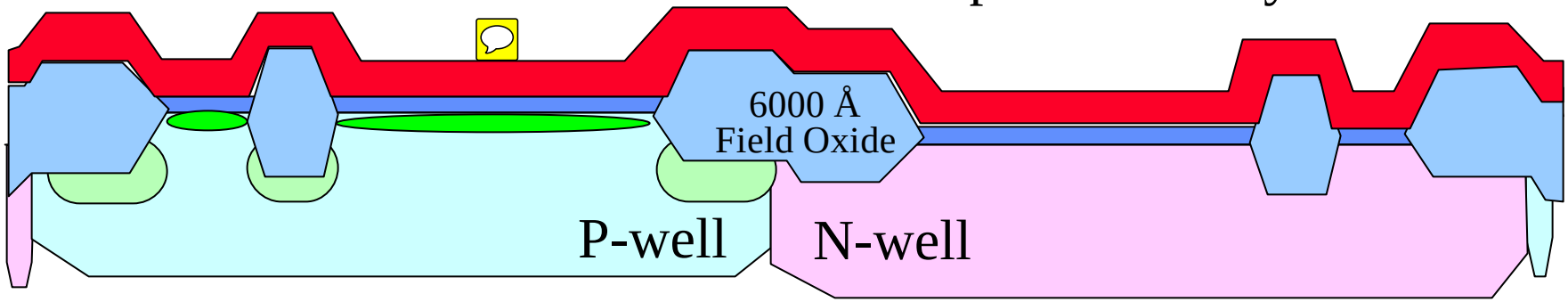
Any	12 min	15 min	20 min	15 min	40 min	15 min
0 lpm	10 lpm	10 lmp	5 lpm	10 lpm	10 lpm	5 lpm
none	N2	N2	N2	N2	N2	N2

At the end of a run the furnace returns to Interval 0 which is set for boat out, 25 °C and no gas flow. The furnace waits in that state until someone aborts the current recipe or loads a new recipe.

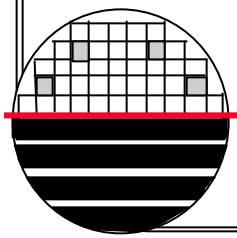
N+ Poly Doping, Thin Poly, < 1 µm, No Oxide Growth

ETCH SPIN ON GLASS

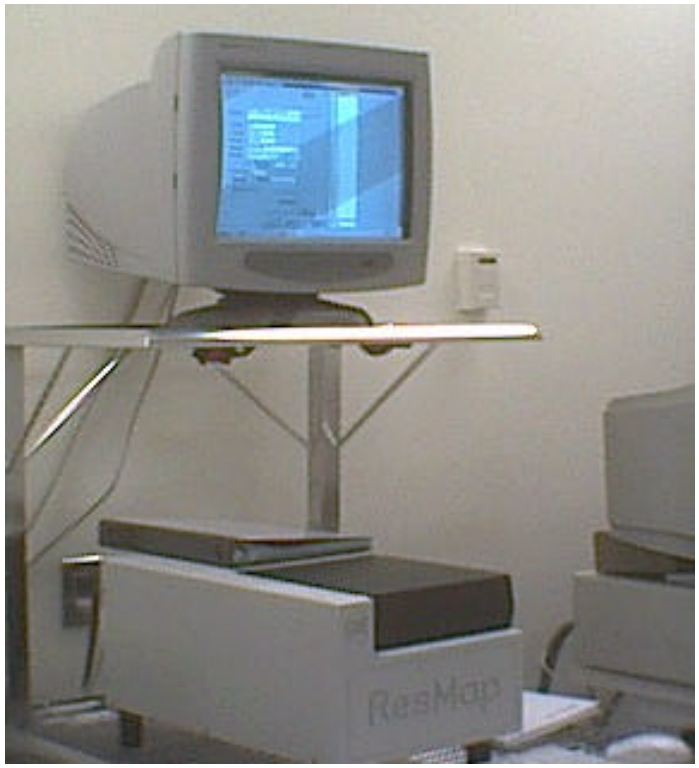
4 min BHF dip
5 min Rinse
Spin/Rinse/Dry



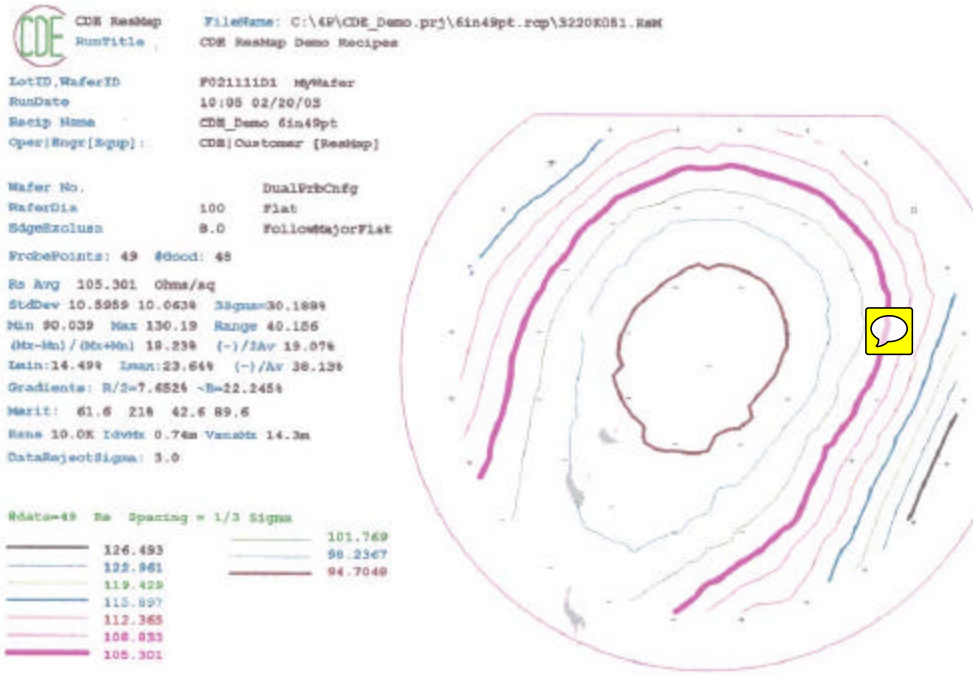
N-type Substrate 10 ohm-cm



MEASURE POLY SHEET RESISTANCE



CDE Resistivity Mapper



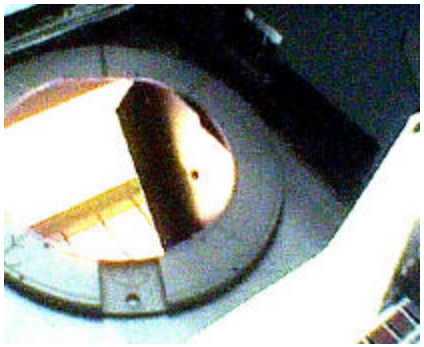
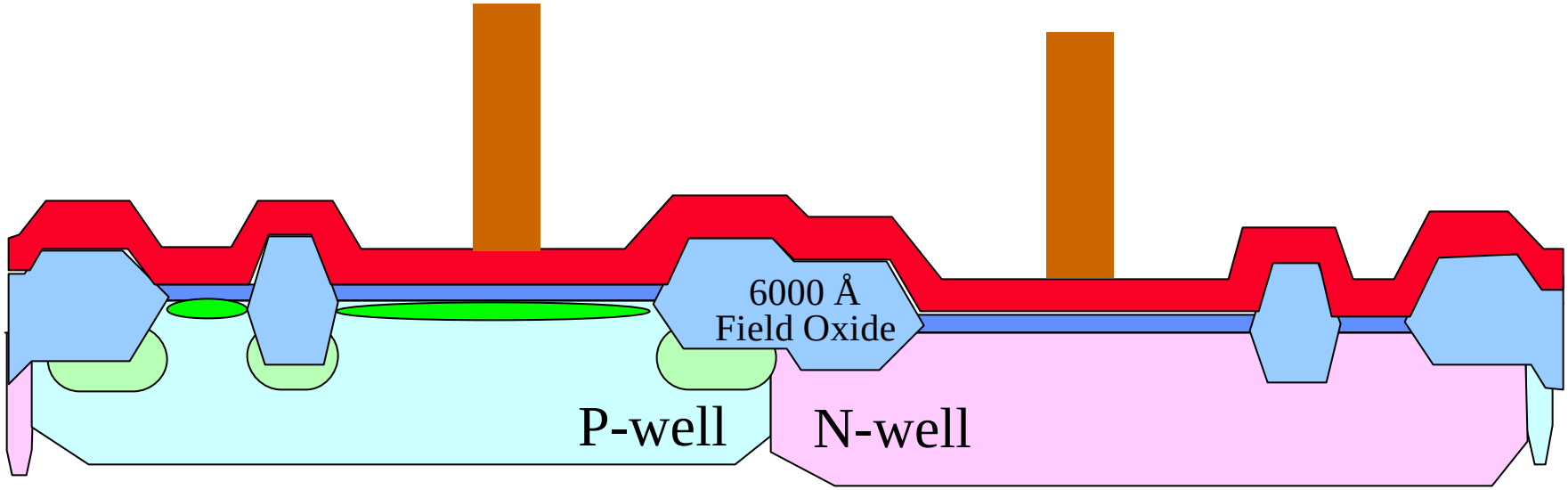
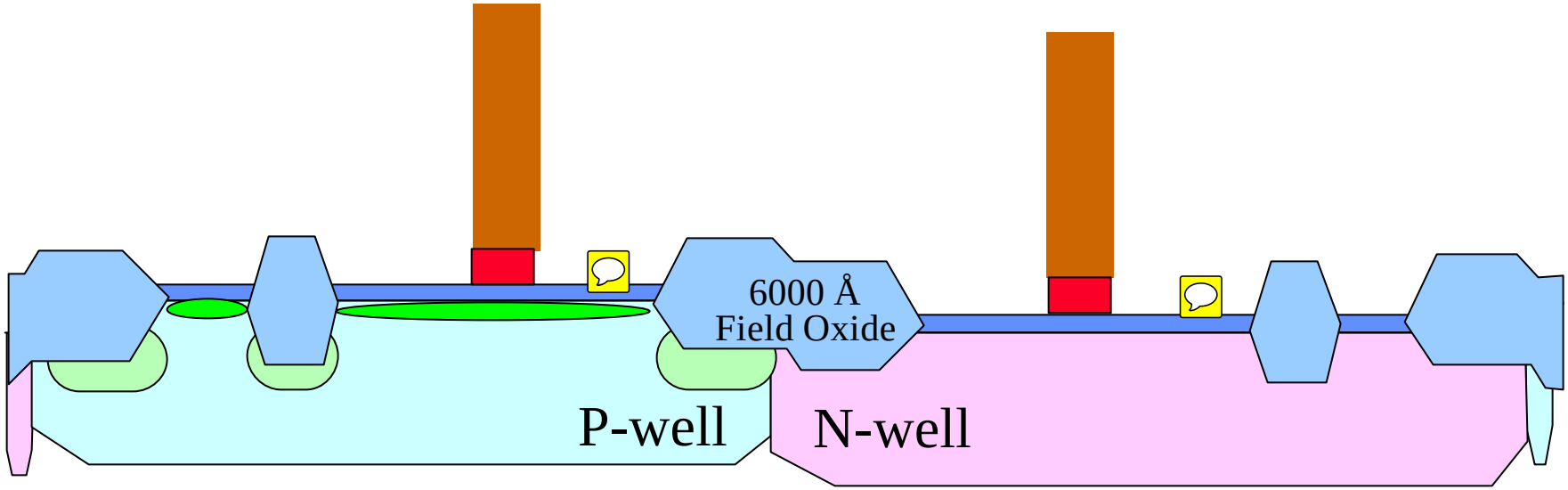


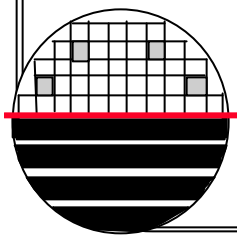
PHOTO 5 POLY GATE



N-type Substrate 10 ohm-cm

POLY ETCH





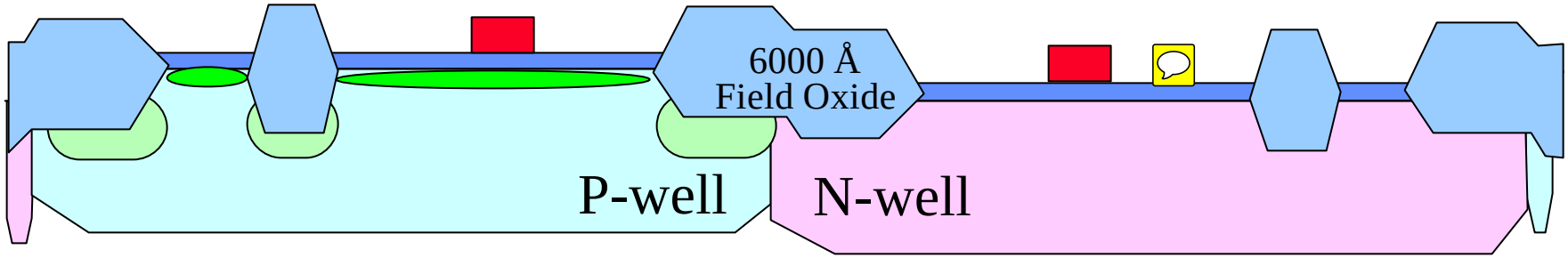
POLY ETCH WITH END POINT

Process: Step 1 – 325mTorr; 0 watts
Gap = 1.5 cm
140sccm SF6, 15 sccm O2
Max Time = 2 min.
Time Only

Process: Step 2 – 325mTorr; 100 watts,
Gap = 1.5 cm
140sccm SF6, 15 sccm O2
Max Time = 1 min. 15 sec
Time or Endpoint
Endpoint and Time
Sampling A (ch12 @ 520nm)
Active during step 02
Delay 15sec before normalizing
Normalize for 10sec
Trigger at 90%

Process: Step 3 – 325mTorr; 140W,
Gap = 1.5 cm
140sccm SF6, 15 sccm O2
Overetch – 10%

STRIP RESIST



Include D1-D3
Strip Photresist in Branson Asher

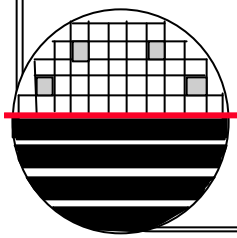
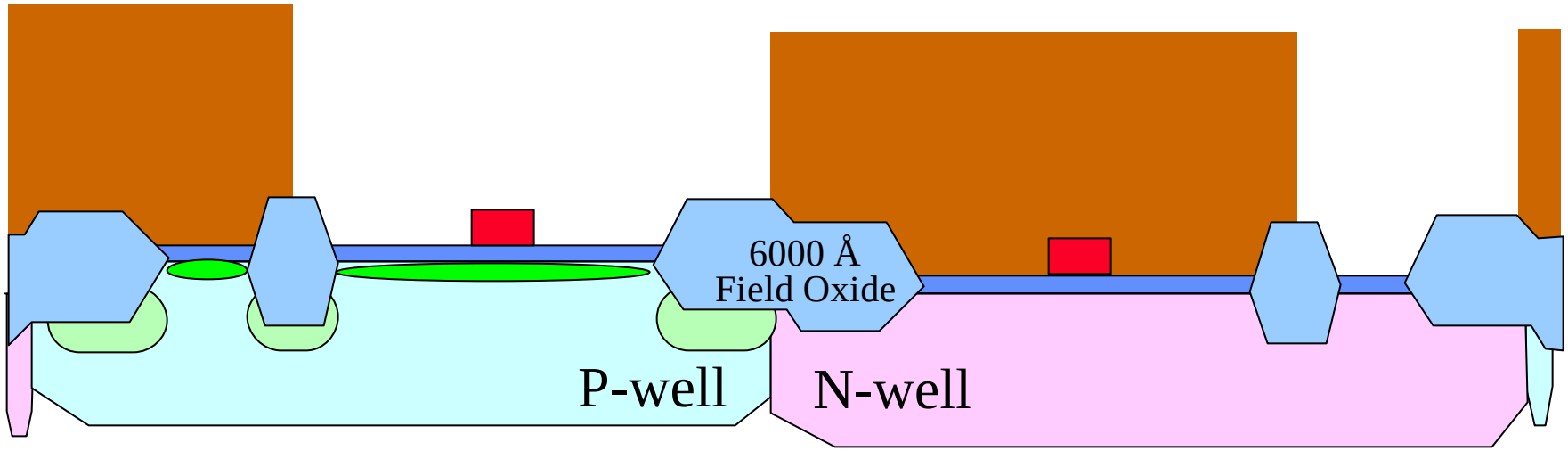


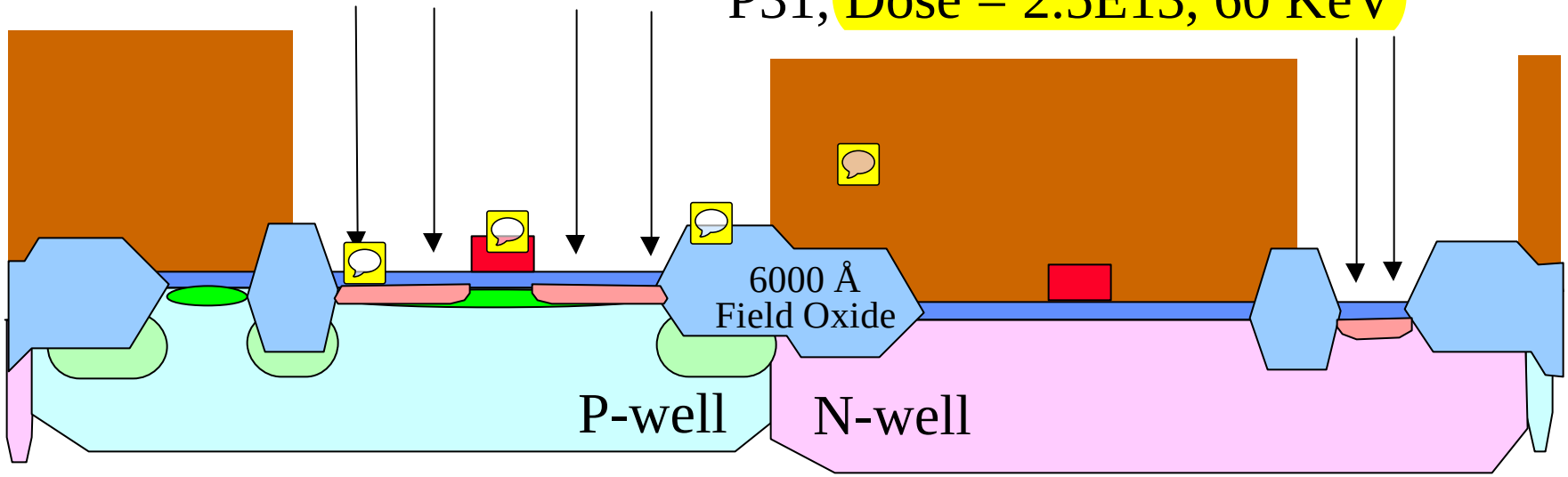
PHOTO 6 LDD N-TYPE IMPLANT



N-type Substrate 10 ohm-cm

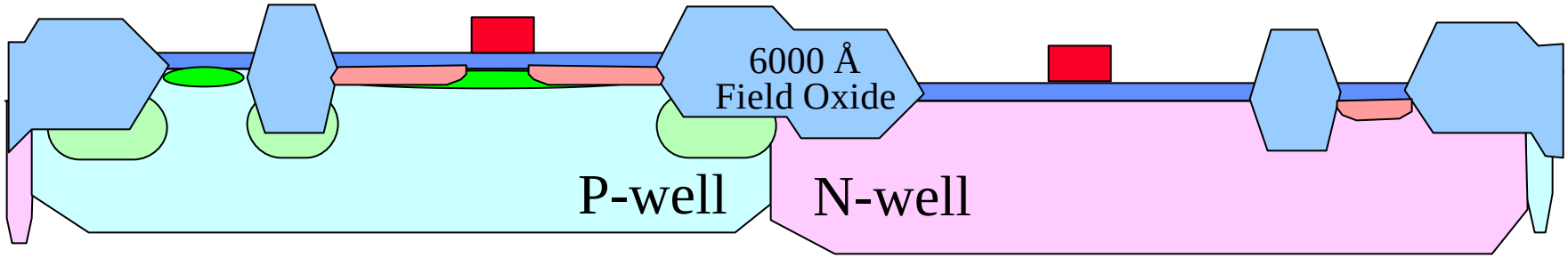
IMPLANT LDD

P31, Dose = 2.5E13, 60 KeV



N-type Substrate 10 ohm-cm

STRIP RESIST



Include D1-D3
Strip Photresist in Branson Asher

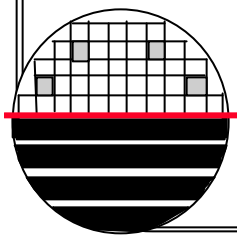
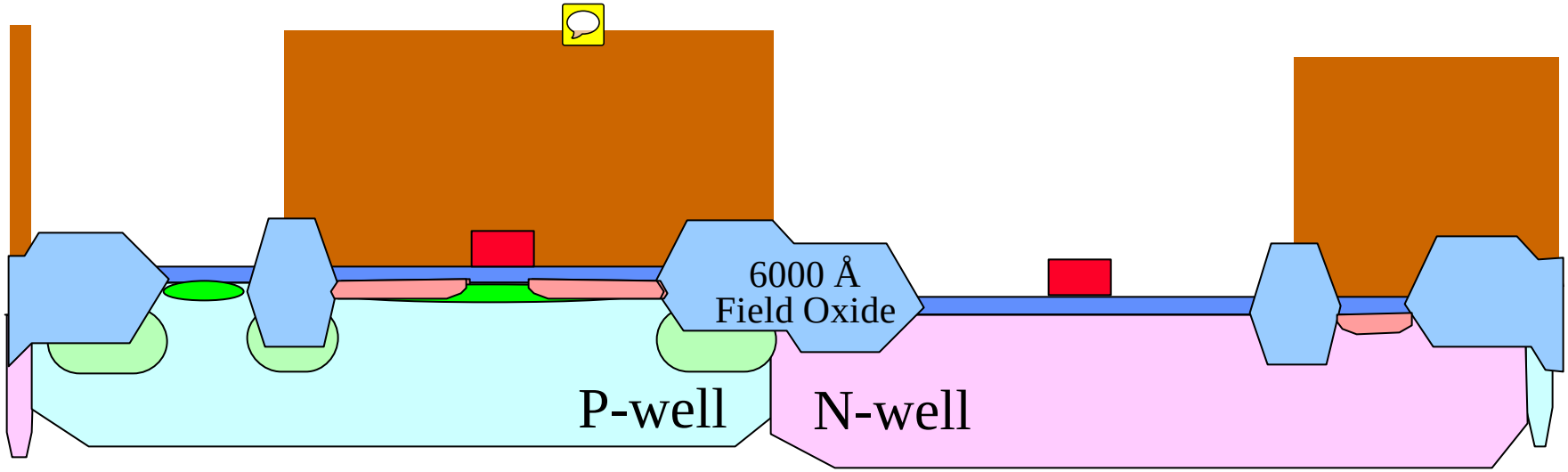


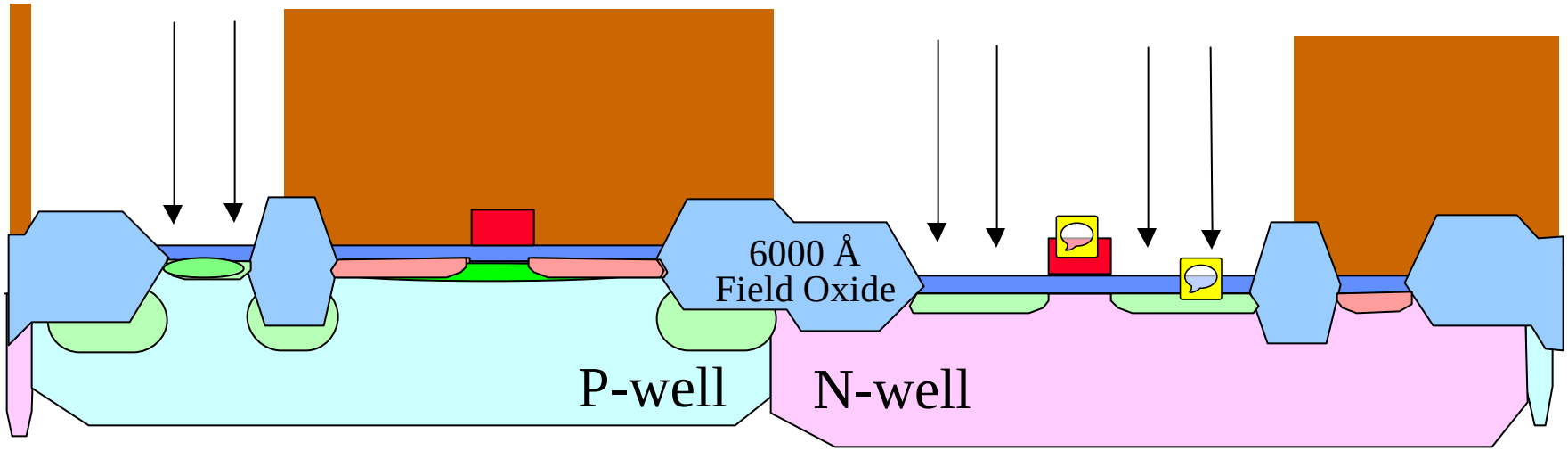
PHOTO 7 LDD P-TYPE IMPLANT



N-type Substrate 10 ohm-cm

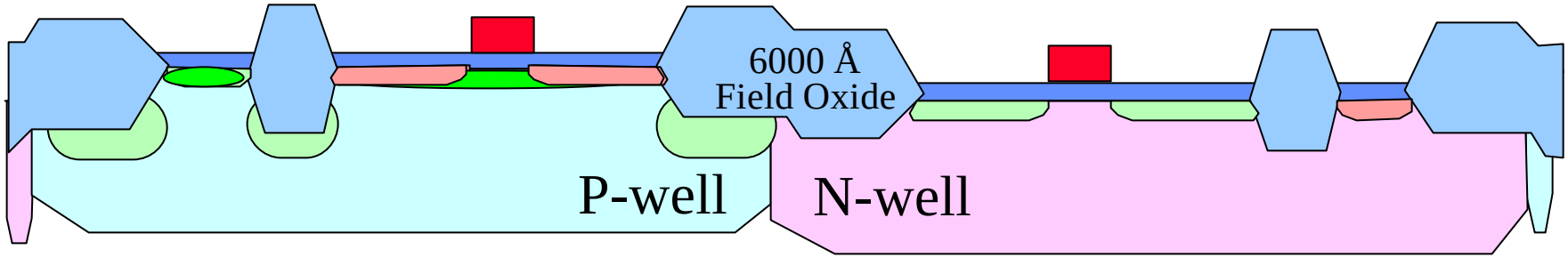
IMPLANT LDD

B11, Dose = 4E13, E = 50 KeV



N-type Substrate 10 ohm-cm

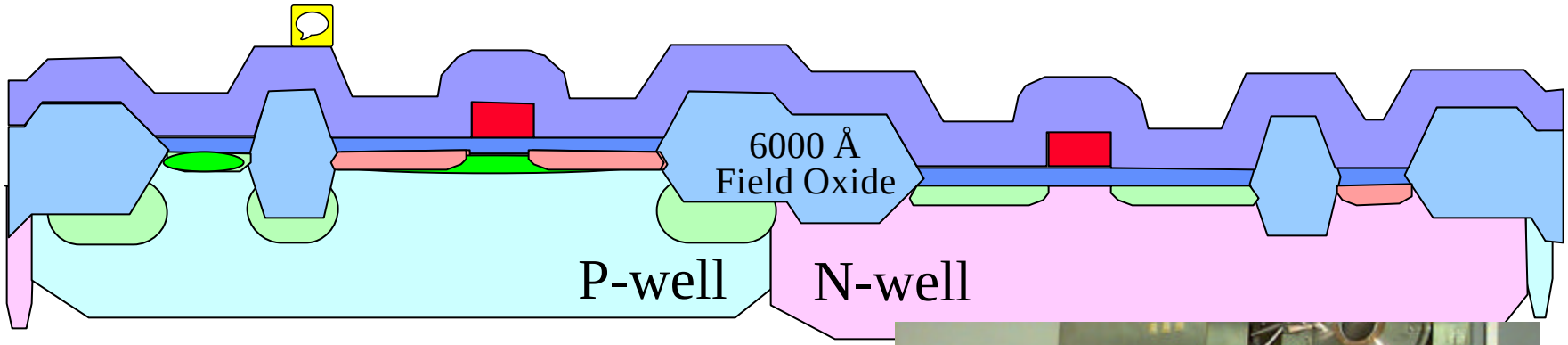
STRIP RESIT

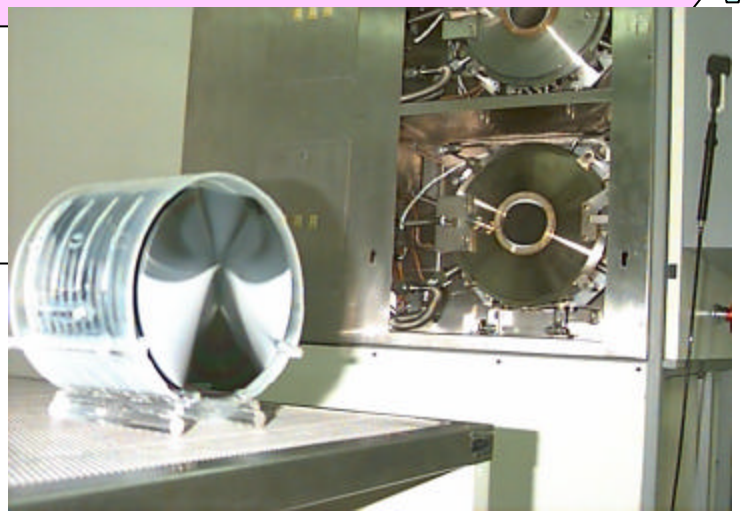


Include D1-D3
Strip Photresist in Branson Asher

LPCVD OXIDE

Target 4000 Å





ASM 6” LPCVD Tool

PECVD OXIDE FROM TEOS

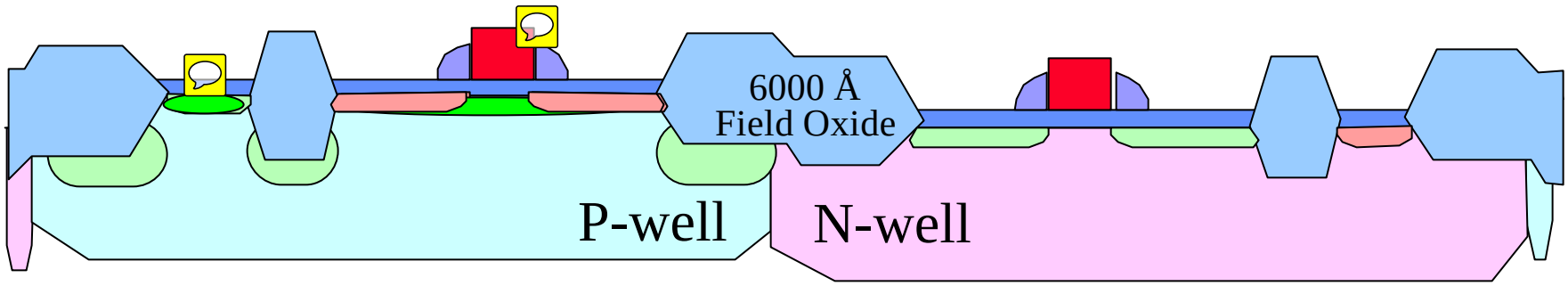
TEOS Program: (Chamber A)
Step 1
- Setup Time = 15 sec
- Pressure = 9 Torr
- Susceptor Temperature= 390 C
- Susceptor Spacing= 220 mils
- RF Power = 0 watts
- TEOS Flow = 400 scc
- O2 Flow = 285 scc

Step 2 – Deposition
- Dep Time = 55 sec (5000 Å)
- Pressure = 9 Torr
- Susceptor Temperature= 390 C
- Susceptor Spacing= 220 mils
- RF Power = 205 watts
- TEOS Flow = 400 scc
- O2 Flow = 285 scc

Step 3 – Clean
- Time = 10 sec
- Pressure = Fully Open
- Susceptor Temperature= 390 C
- Susceptor Spacing= 999 mils
- RF Power = 50 watts
- TEOS Flow = 0 scc
- O2 Flow = 285 scc

ETCH OXIDE TO FORM SIDE WALL SPACERS

TEOS etch rate ~353Å/min
Total time 10 to 13 min



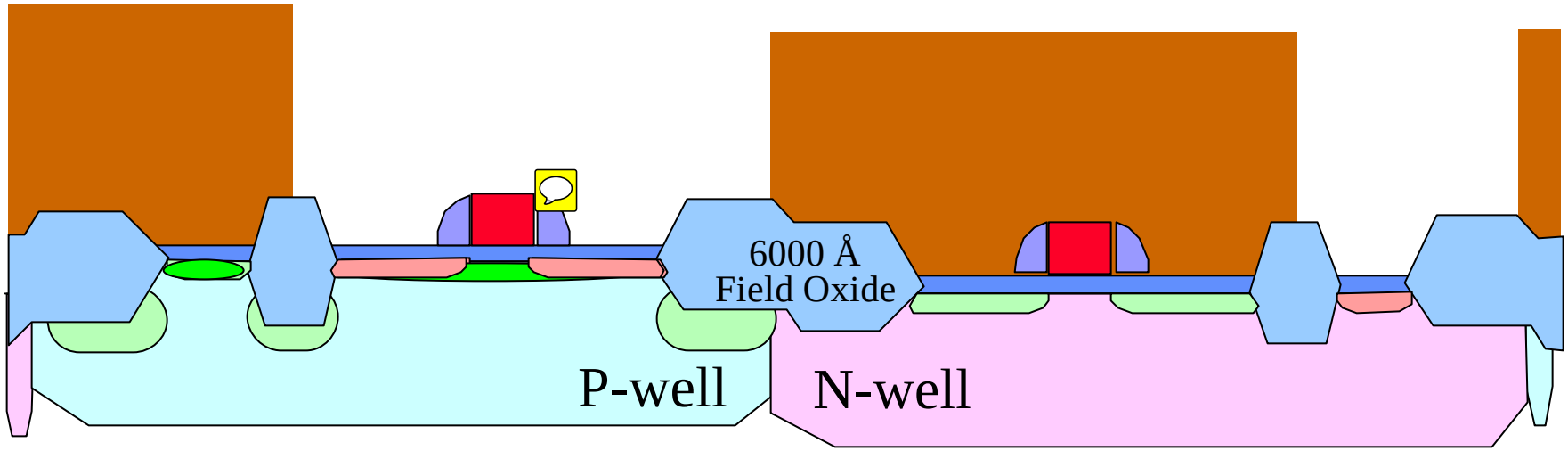
N-type Substrate 10 ohm-cm

Drytek Quad
Recipe FACSPCR
65 sccm Ar
65 sccm CHF3
5 sccm O2
Power = 200 watts
Pressure = 70 mTorr
Etch Rate = 33 nm/min

SIDE WALL SPACER ETCH IN DRYTEK QUAD

Drytek Quad
Recipe FACSPCR
65 sccm Ar
65 sccm CHF3
5 sccm O2
Power = 200 watts
Pressure = 70 mTorr
Etch Rate = 33 nm/min

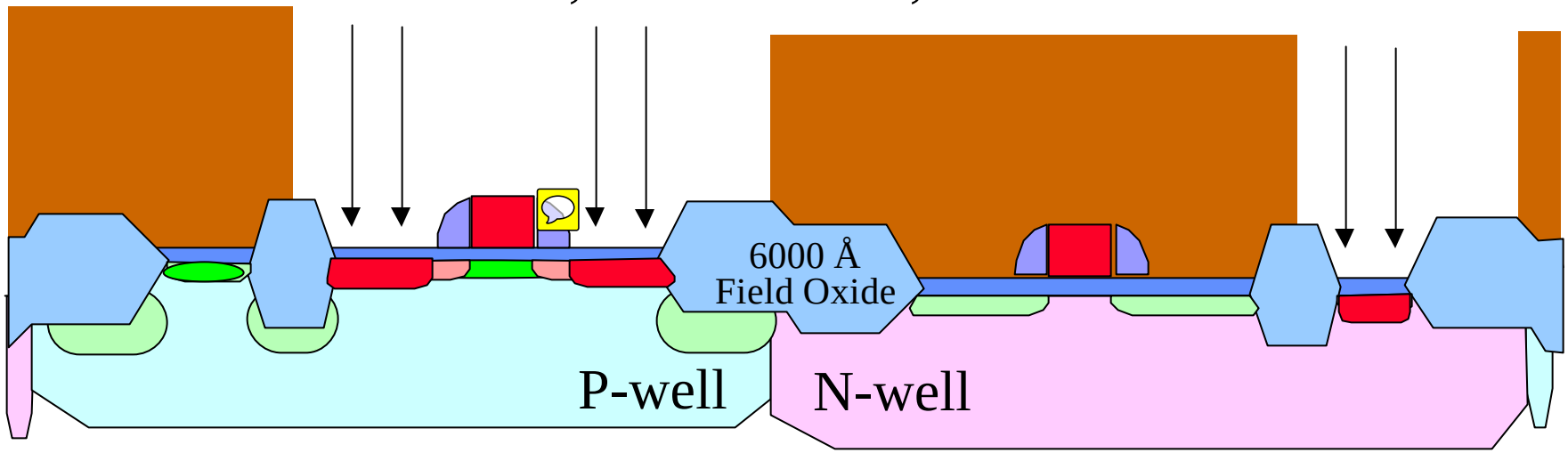
PHOTO 8 N+ D/S



N-type Substrate 10 ohm-cm

IMPLANT N+ D/S

P31, Dose = 2 E15, E = 60 KeV



N-type Substrate 10 ohm-cm

IMPLANT MASKING THICKNESS CALCULATOR

Rochester Institute of Technology					Lance Barron		
Microelectronic Engineering					Dr. Lynn Fuller		
11/20/04							

IMPLANT MASK CALCULATOR **Enter 1 - Yes 0 - No in white boxes**

DOPANT SPECIES

B11	1
BF2	0
P31	0

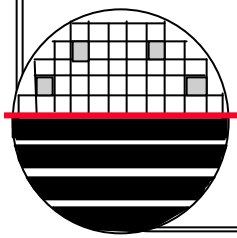
MASK TYPE

Resist	0
Poly	1
Oxide	0
Nitride	0

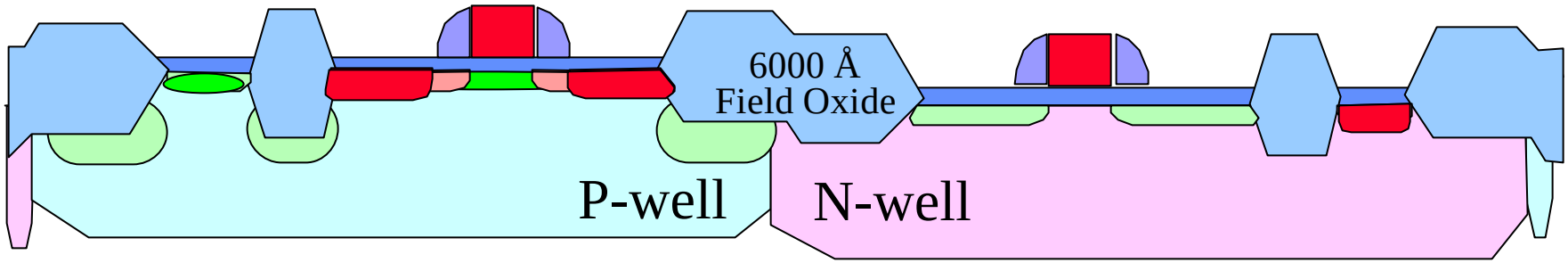
ENERGY

40 KeV

Thickness to Mask >1E15/cm3 Surface Concentration 2961.954 Angstroms



STRIP RESIST



Include D1-D3
Strip Photresist in Branson Asher

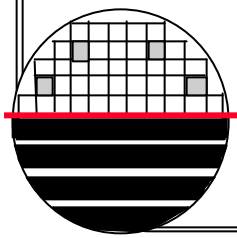
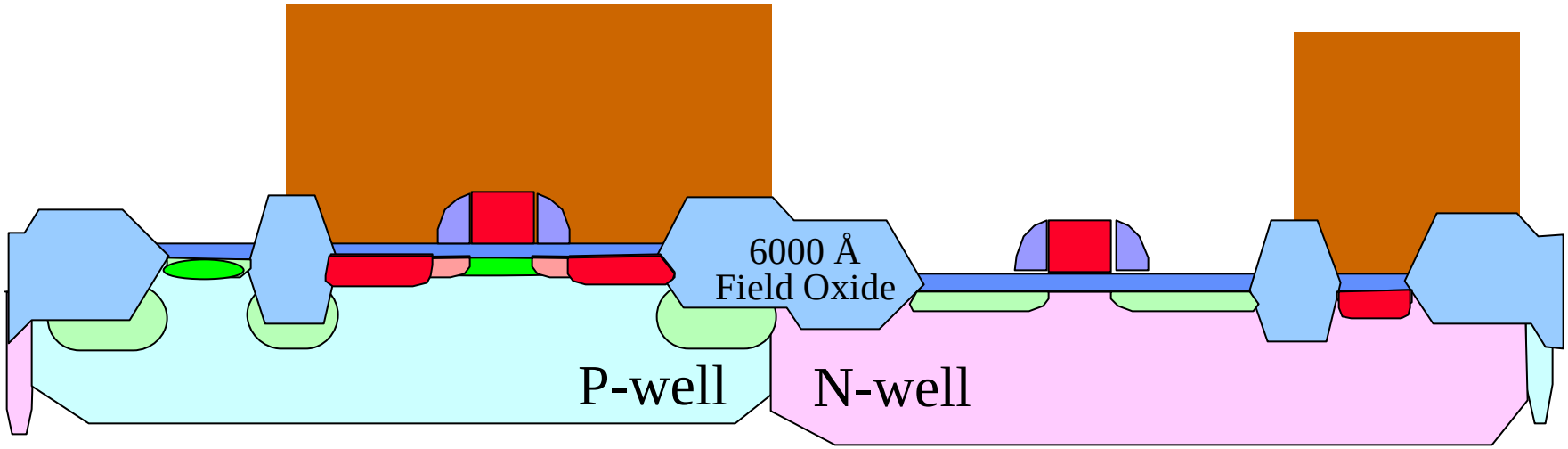
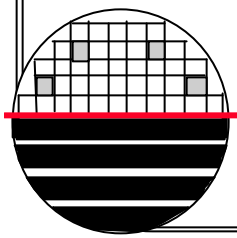


PHOTO 9 P+ D/S

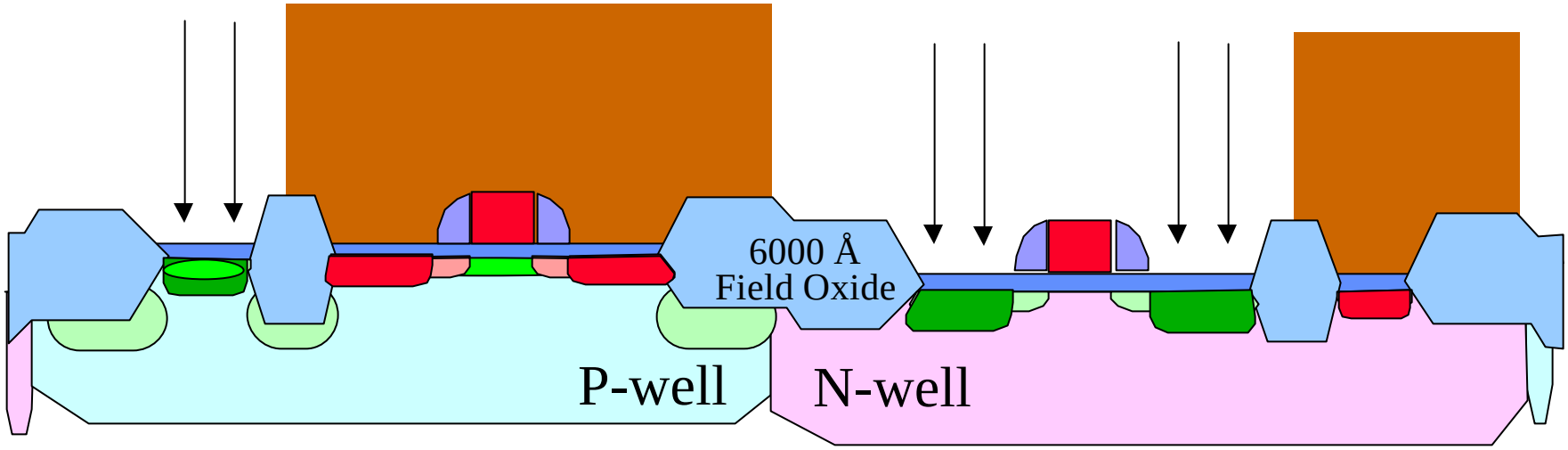


N-type Substrate 10 ohm-cm



IMPLANT P+ D/S

B11, Dose = 2 E15, E = 50 KeV



N-type Substrate 10 ohm-cm

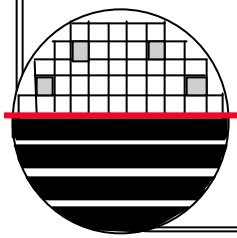
IMPLANT MASKING THICKNESS CALCULATOR

Rochester Institute of Technology					Lance Barron		
Microelectronic Engineering					Dr. Lynn Fuller		
11/20/04							

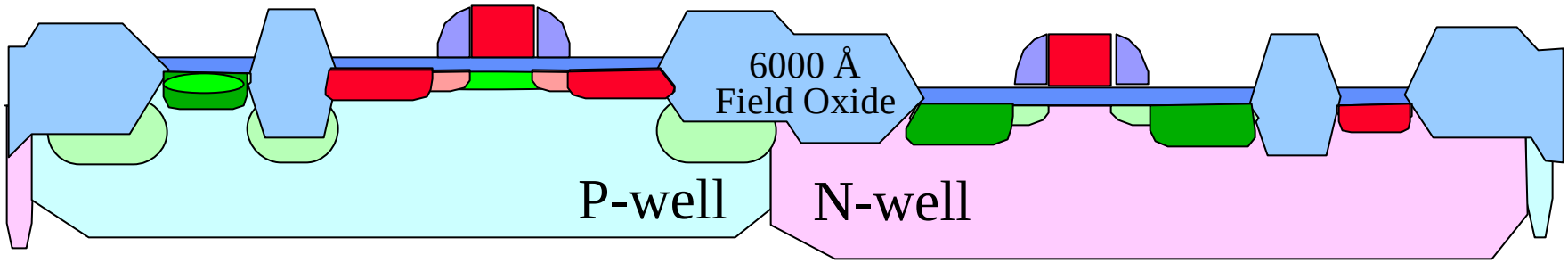
IMPLANT MASK CALCULATOR **Enter 1 - Yes 0 - No in white boxes**

DOPANT SPECIES		**MASK TYPE**		**ENERGY**	
B11	1	Resist	0	40	KeV
BF2	0	Poly	1		
P31	0	Oxide	0		
		Nitride	0		

Thickness to Mask >1E15/cm3 Surface Concentration 2961.954 Angstroms



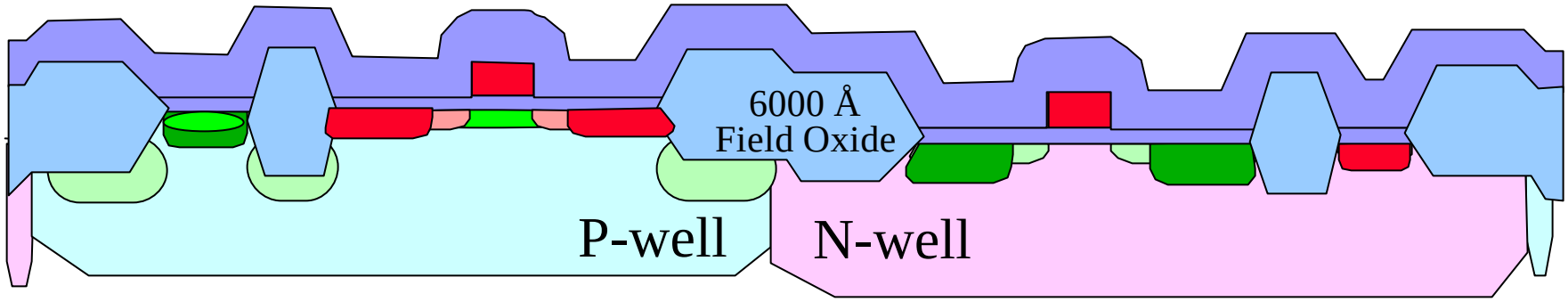
STRIP RESIST, RCA CLEAN



Include D1-D3
Strip Photresist in Branson Asher

RCA CLEAN AND DEPOSIT LPCVD OXIDE

Target 4000 Å



N-type Substrate 10 ohm-cm

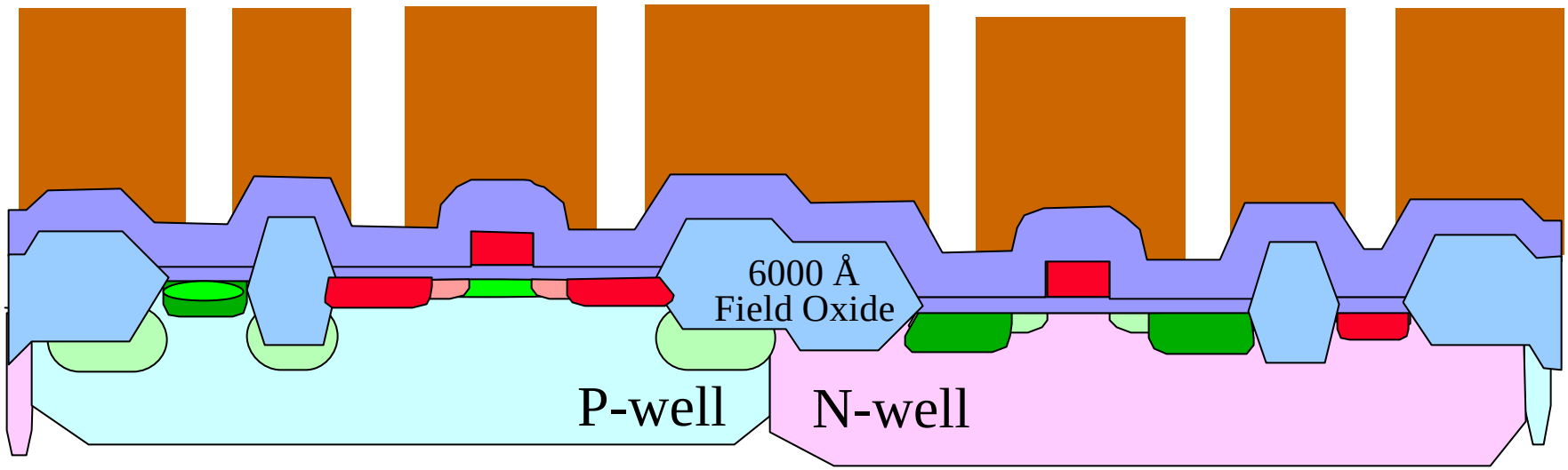
PECVD OXIDE FROM TEOS

TEOS Program: (Chamber A)
Step 1
- Setup Time = 15 sec
- Pressure = 9 Torr
- Susceptor Temperature= 390 C
- Susceptor Spacing= 220 mils
- RF Power = 0 watts
- TEOS Flow = 400 scc
- O2 Flow = 285 scc

Step 2 – Deposition
- Dep Time = 55 sec (5000 Å)
- Pressure = 9 Torr
- Susceptor Temperature= 390 C
- Susceptor Spacing= 220 mils
- RF Power = 205 watts
- TEOS Flow = 400 scc
- O2 Flow = 285 scc

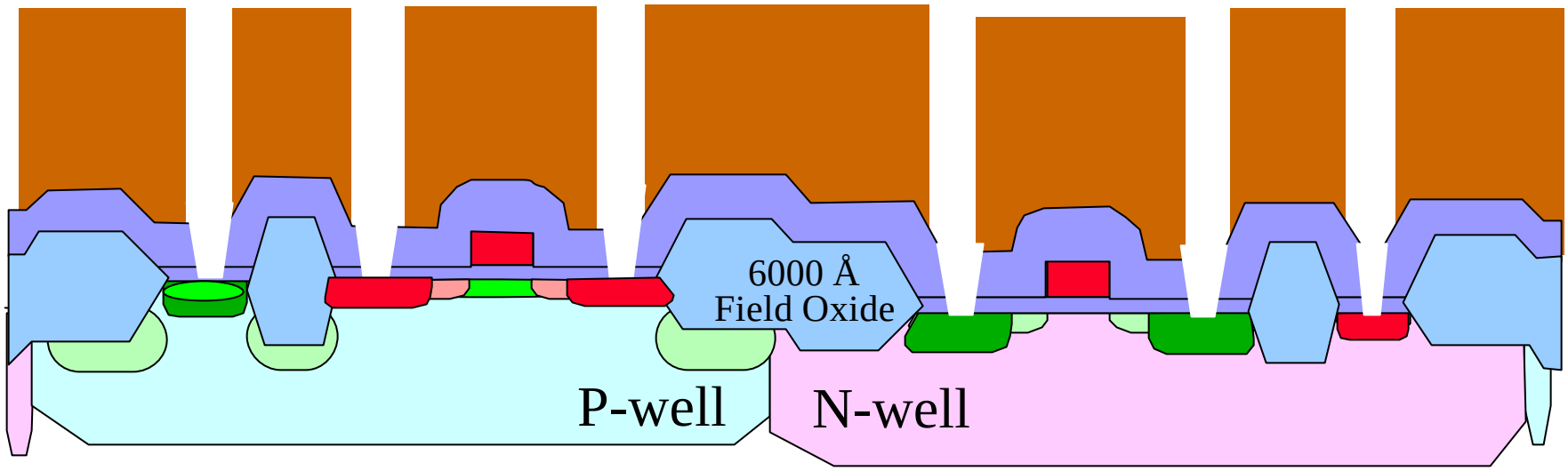
Step 3 – Clean
- Time = 10 sec
- Pressure = Fully Open
- Susceptor Temperature= 390 C
- Susceptor Spacing= 999 mils
- RF Power = 50 watts
- TEOS Flow = 0 scc
- O2 Flow = 285 scc

PHOTO 10 CONTACT CUTS



N-type Substrate 10 ohm-cm

ETCH CONTACT CUTS



N-type Substrate 10 ohm-cm

Wet Etch in BHF, 3 min, SRD

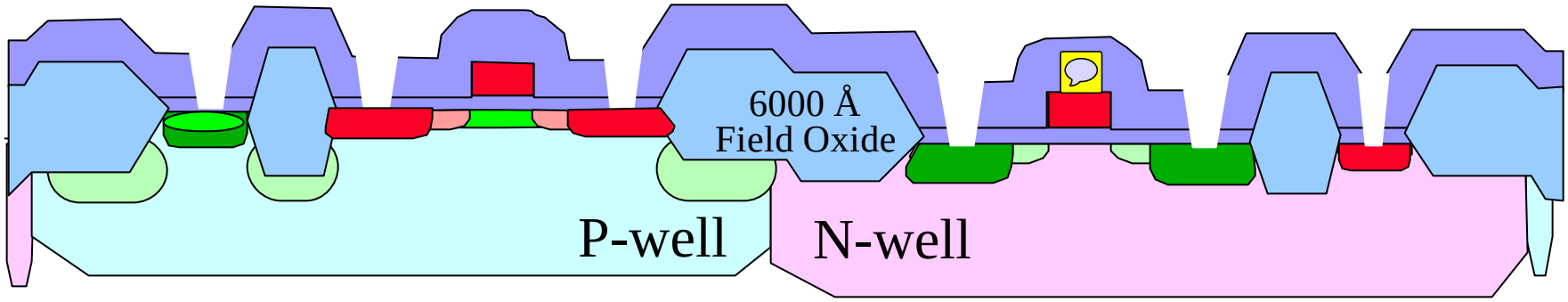
CONTACT CUT ETCH USING RIE

Drytek Quad
Recipe FACCC
65 sccm Ar
65 sccm CHF3
5 sccm O2
Power = 200 watts
Pressure = 70 mTorr
Etch Rate = 33 nm/min

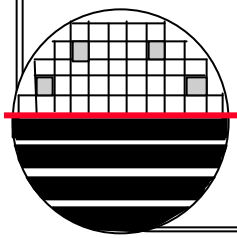
Problem is no endpoint detection available in this tool.

STRIP RESIST, RCA CLEAN

Clean includes 50:1 HF Dip twice once after each bath to remove chemically grown oxide



Include D1-D3
Strip Photresist in Branson Asher



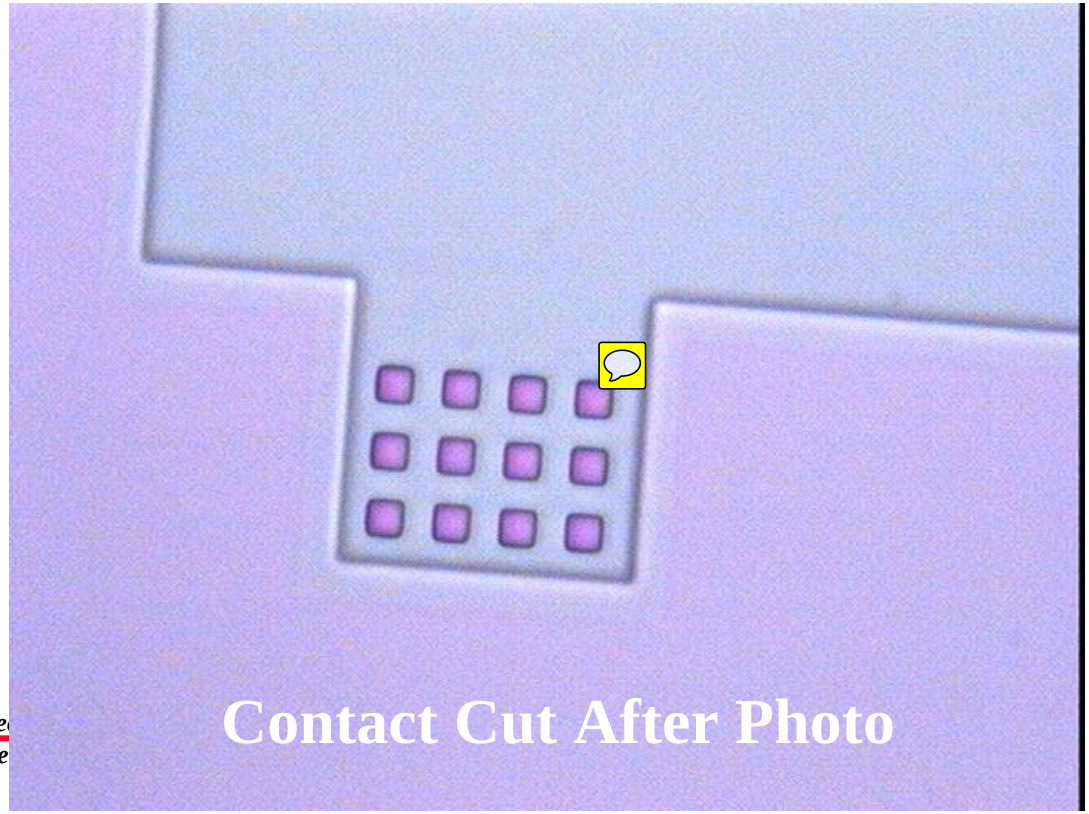
MAKING SMALL (2µm x 2µm) CONTACT CUT BY WET ETCH

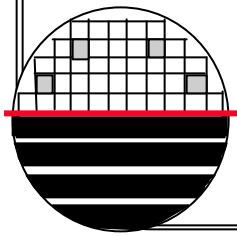
Contact Cut Lithography is difficult because of the complicated film stack. The contacts are through 4000Å TEOS oxide on thermal oxide on poly on gate oxide. The poly has a silicide layer in the Advanced CMOS process. The poly thickness might be 4000Å or 6000Å. The TEOS may be annealed. Other contacts are to drain and source through 4000Å TEOS on thermally grown oxide of ~500Å (from poly reox step) plus gate oxide. The gate oxides are 330Å, 150Å, or 100Å depending on the exact process.

Contact cut etch is also difficult. Plasma etch is difficult because of the different oxide layers and thickness and the poor selectivity between etching oxide and the underlying poly or drain/source silicon. Wet etch has problems with blocking. That is where the BOE can not get into the small contact cut openings. Blocking depends on surface tension as measured by the wetting angle which depends on the type of photoresist used.

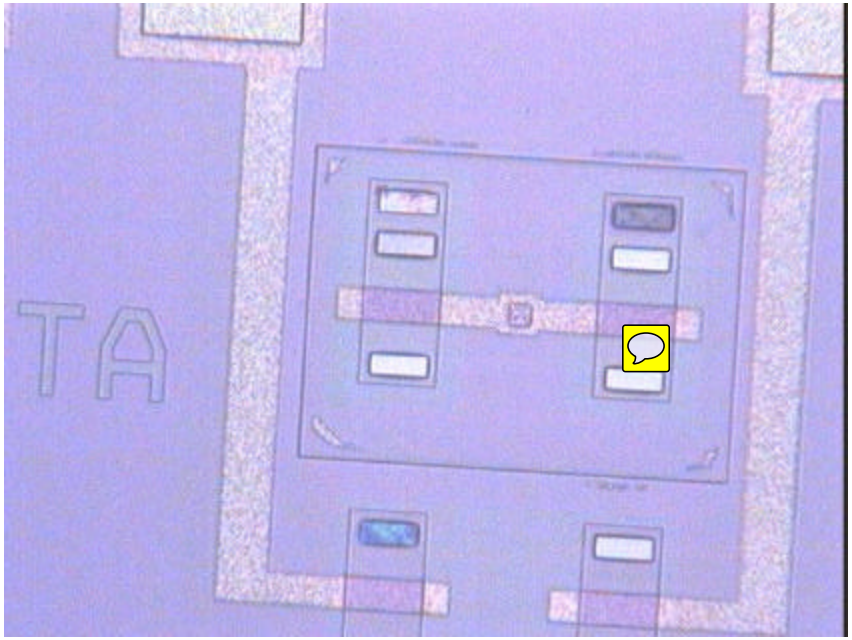
MAKING SMALL (2µm x 2µm) CONTACT CUT BY WET ETCH

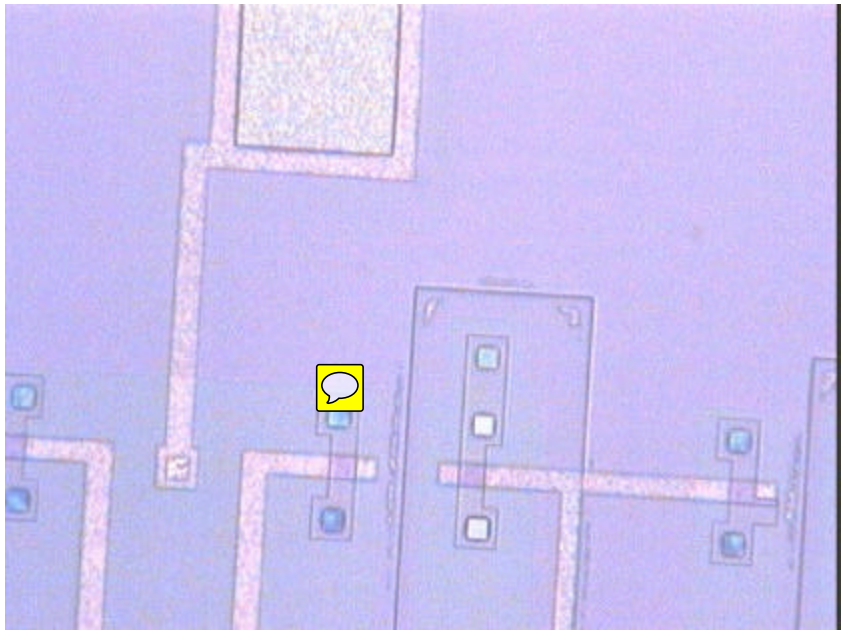
To ensure that the photoresist is cleared in the bottom of all the contact cuts the exposure dose is increased to 285 mj/cm2 and track develop time is increased to 3 min. This makes the 2µm x 2µm contacts a little larger ~2.2µm by ~2.2µm but they are clear regardless of the underlying film stack.





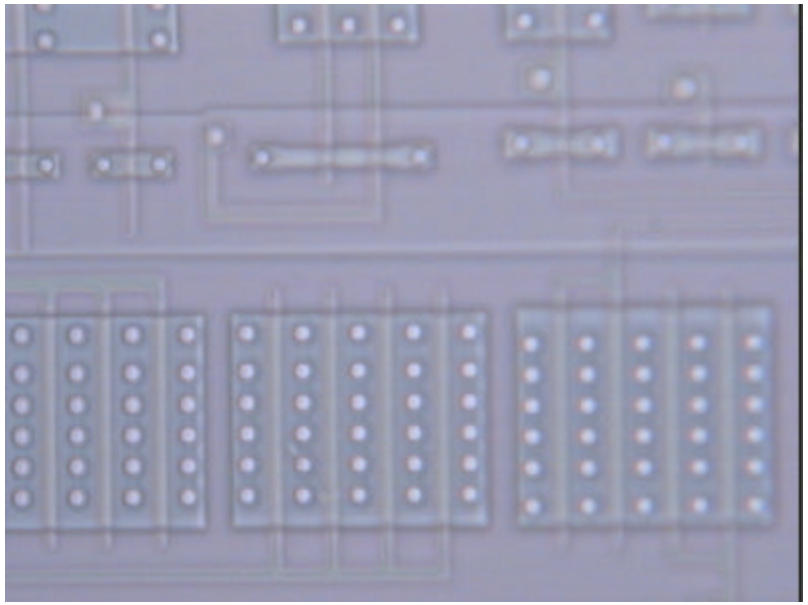
MAKING SMALL (2µm x 2µm) CONTACT CUT BY WET ETCH

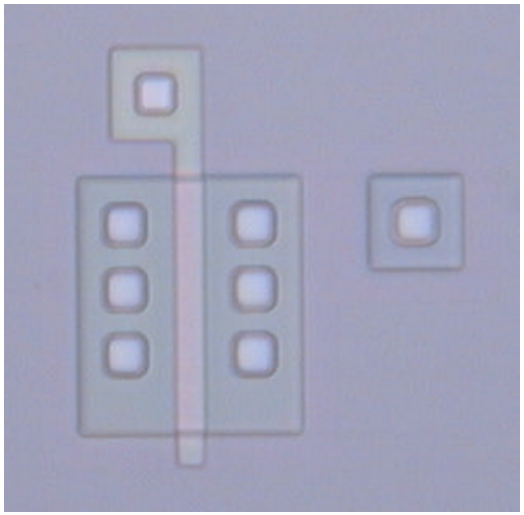




Wet etch has problems with blocking. That is where the BOE can not get into the small contact cut openings. Blocking depends on surface wetting angle. If blocking occurs some contact cuts will etch and clear while others will not etch as illustrated in the pictures above.

MAKING SMALL (2µm x 2µm) CONTACT CUT BY WET ETCH





To overcome the blocking problem we raised the boat completely out of the BOE every 15 seconds throughout the entire etch. To be sure to clear all the contacts the etch time was extended to 5 minutes (approximately twice the expected etch time based on etch rates and approximate film thicknesses) This approach gave excellent results for all the various film stacks as shown in the pictures above.

Microelectronic Engineering

RCA CLEAN

PLAY

APM

NH_4OH - 1part
H_2O_2 - 3parts
H_2O - 15parts
70 °C, 15 min.

DI water
rinse, 5 min.

H_20 - 50
HF - 1
60 sec.

DI water
rinse, 5 min.

HPM

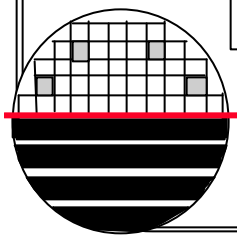
HCL - 1part
H_2O_2 - 3parts
H_2O - 15parts
70 °C, 15 min.

DI water
rinse, 5 min.

H_20 - 50
HF - 1
60 sec.

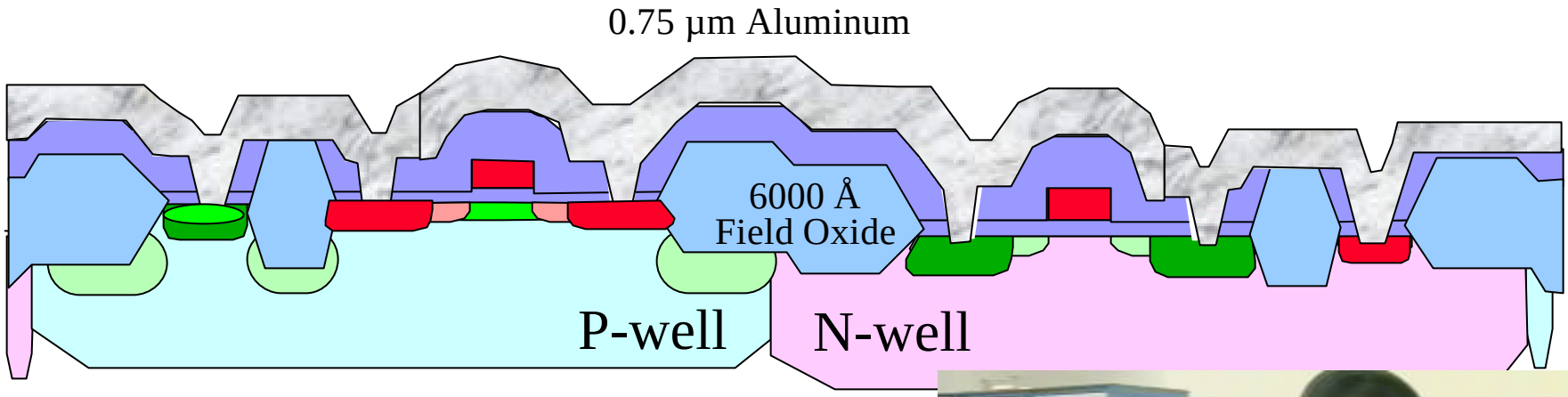
DI water
rinse, 5 min.

SPIN/RINSE
DRY



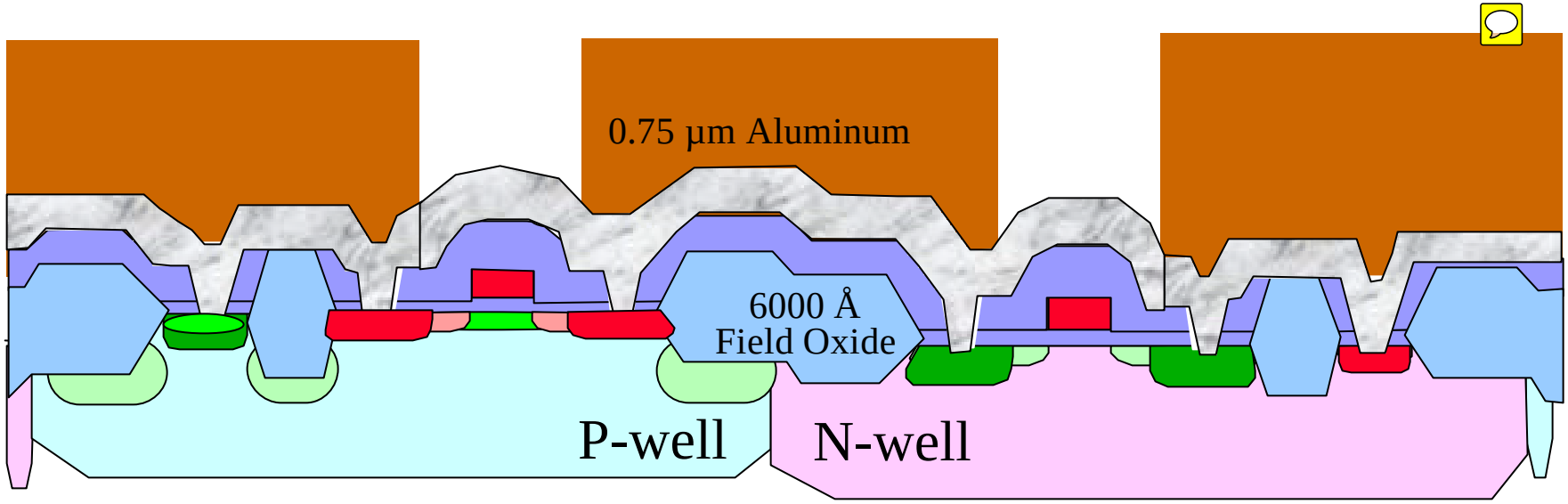
Clean includes 50:1 HF Dip twice once after each bath to remove chemically grown oxide

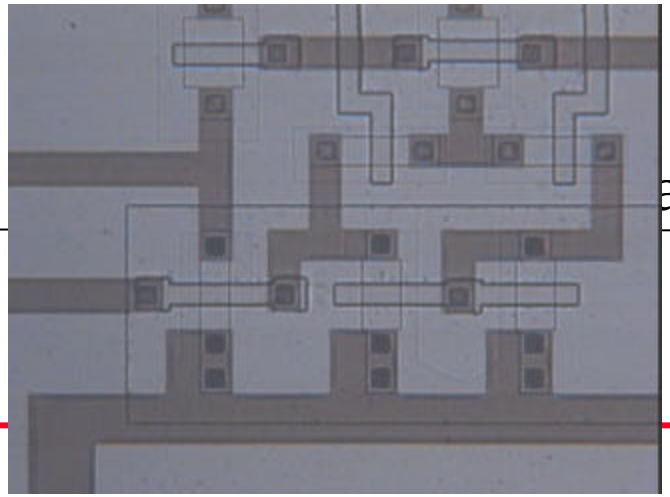
DEPOSIT METAL



CVC 601 Sputter Tool

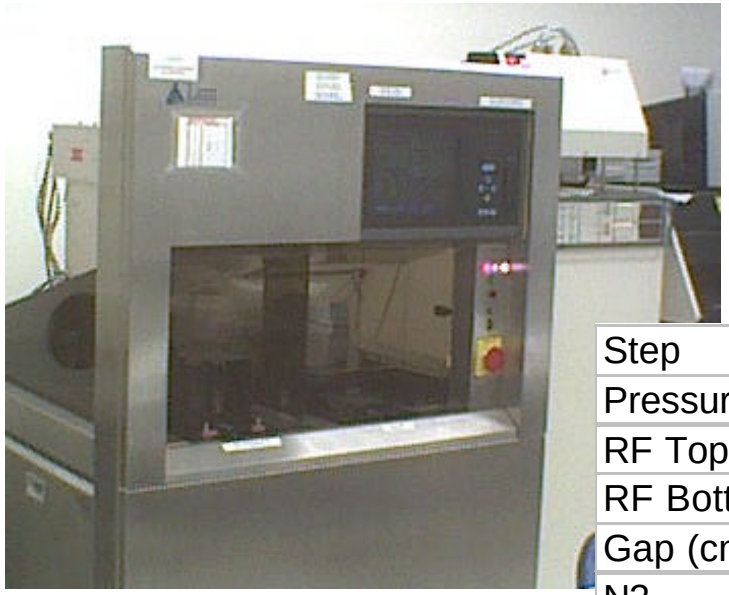
PHOTO 11 METAL





- **Coat (Recipe: COATMTL.RCP)**
  - 400RPM for 2 seconds
  - 2000RPM for 30 seconds
  - Thickness of 13127A
- **Exposure**
  - Energy: 140mJ/cm2
  - Focus: 0.24um
- **Develop (Recipe: DEVMTL.RCP)**
  - Dispense 7 seconds
  - Wait 68 seconds
  - Hard Bake 2 min.

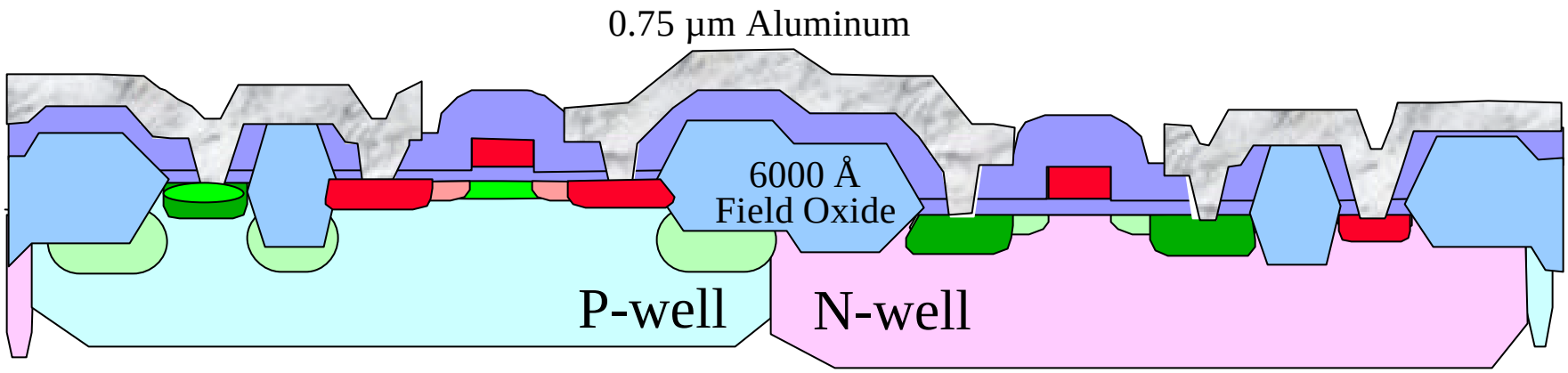
ALUMINUM ETCH



LAM 4600 Aluminum Etch Tool

Step	1	2	3	4	5
Pressure (mtorr)	300	300	300	300	0
RF Top (W)	0	0	0	0	0
RF Bottom (W)	0	250	125	125	0
Gap (cm)	3	3	3	3	5.3
N2	25	25	40	50	50
BCl3	100	100	50	50	0
Cl2	10	10	60	45	0
Ar	0	0	0	0	0
CFORM	15	15	15	15	15
Complete	Stabl	Time	endpoint	Oetch	time
time (s)	15	8	120	25%	15

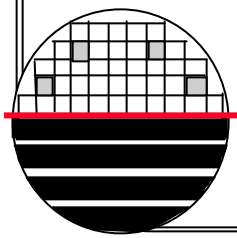
ALUMINUM ETCH, ASH RESIST, SINTER



N-type Substrate 10 ohm-cm

Bruce Furnace 02

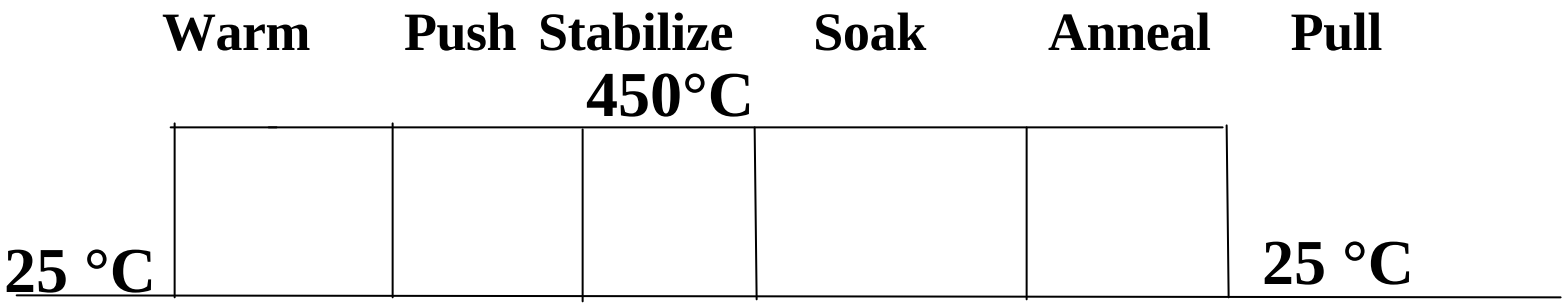
Recipe 101: 450C, H_2N_2, 30min



BRUCE FURNACE RECIPE 101 SINTER

SINTER Recipe #101

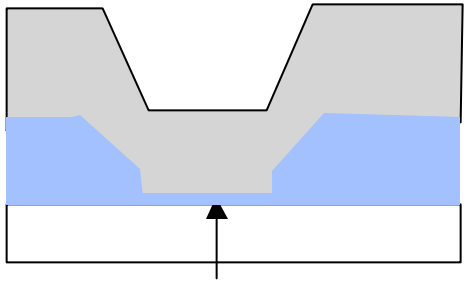
Verified:2-24-04



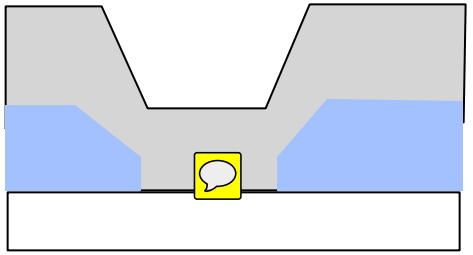
Interval	0	1	2	3	4	5	6	
Any`		90	12	15	30	5	15	min
0 lmp		10	10	10	5	10	5	lpm
None		N2	N2/H2	N2/H2	N2/H2	N2	N2	

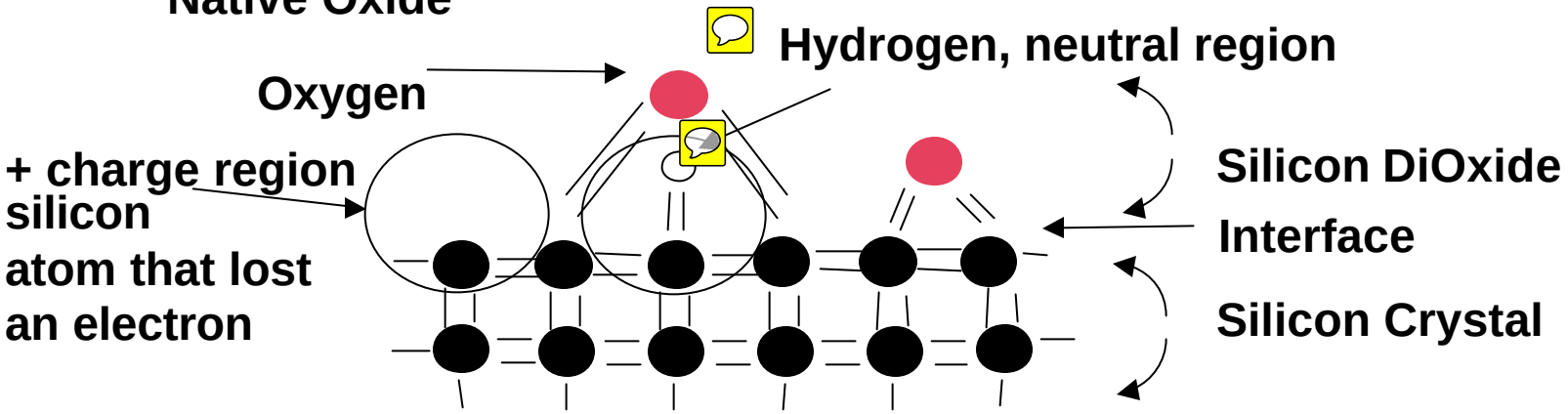
At the end of a run the furnace returns to Interval 0 which is set for boat out, 25 °C and no gas flow. The furnace waits in that state until someone aborts the current recipe or loads a new recipe.

SINTER



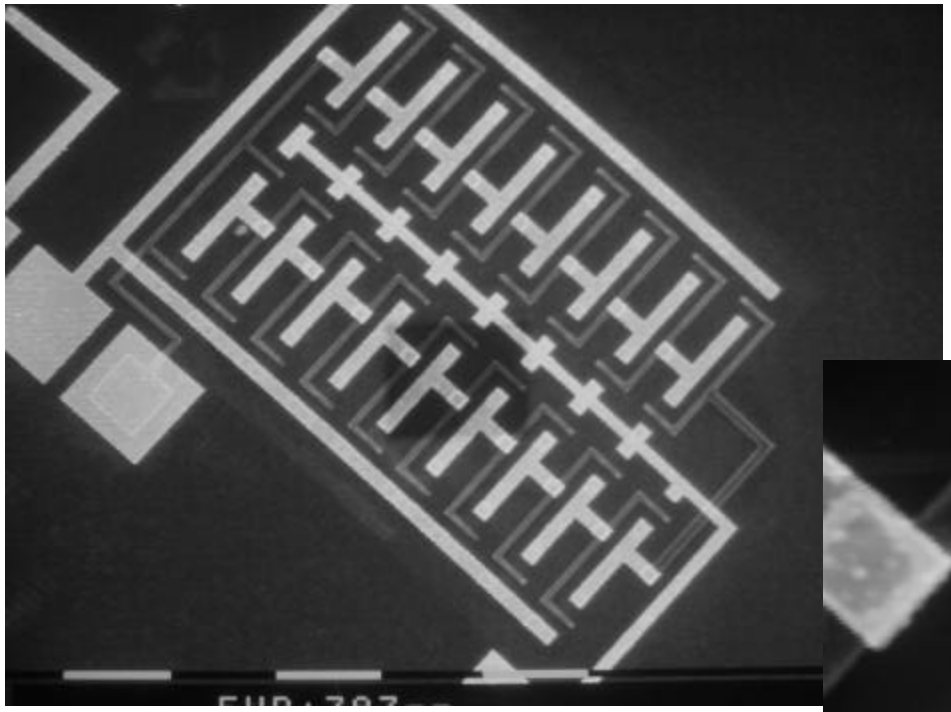
Reduce Contact Resistance

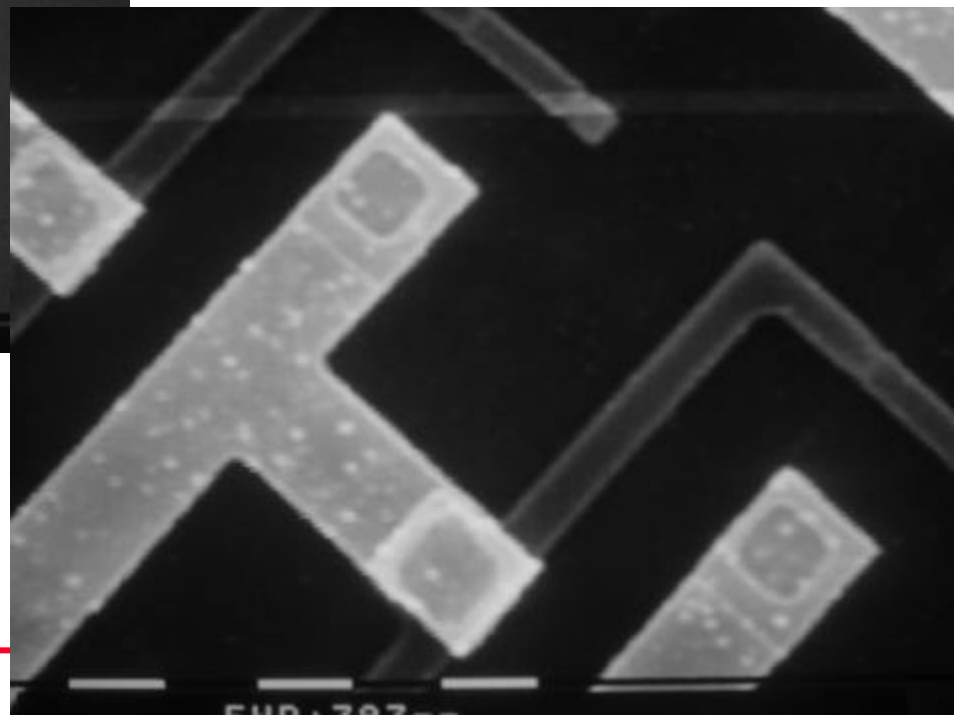




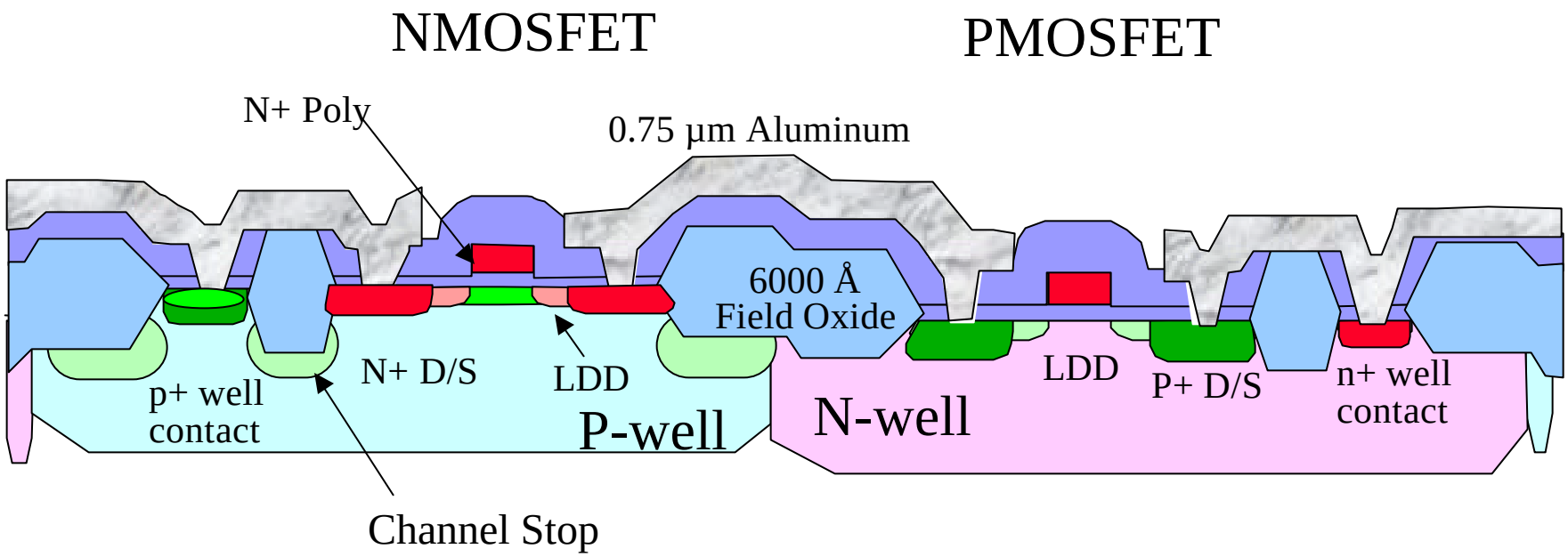
Reduce Surface States

TAKE SEM PICTURES OF RING OSCILLATOR





SUBμ CMOS



N-type Substrate 10 ohm-cm

MESA WIPTRACKING SYSTEM

The process is long and complicated and will take many months to complete each lot. A computerized record keeping system is required to provide instructions and collect data. MESA (Manufacturing Execution System Application) from Camstar, Inc. runs on our AS/400 computer.

SUB MICRON CMOS PROCESS

```
  5/10/01                              MESA                    PCMSINQ    S35401
 14:01:59                      Process Master Inquiry          MICROGURU    RIT

Type information.  Then Enter, or use Roll keys to page.

  Plant  . . . . . :   RIT
  Process/rev  . . . . .   SUB-CMOS   1.0  SUB-MICRON TWIN WELL CMOS 4 INCH WAF

  5=Display                VI=View instructions     VO=View operation
  VS=View spec             VP=View parameters       VM=View move-in ...
                                                Position to  . . . . .  ________
  Opt Seq#     Operation        Spec ID                Rev  Spec description
  __    61.00  ET10 LTO ETCH    SUB-CMOS-ET10-CC       1.0  SUB-CMOS ETCH CC
  __    62.00  ET07 STRIP       SUB-CMOS-ET07-CC       1.0  SUB-CMOS ASH RESIST
  __    63.00  CL01 RCA CLEAN   SUB-CMOS-CL01-METAL    1.0  SUB-CMOS CL01 METAL
  __    64.00  ME01 AL DEPOSIT  SUB-CMOS-ME01          1.0  SUB-CMOS ME01 AL DEP
  __    65.00  PH03 PHOTOLITH   SUB-CMOS-PH03-METAL    1.0  SUB-CMOS PH03 METAL
  __    66.00  ET05 AL ETCH     SUB-CMOS-ET05          1.0  SUB-CMOS AL ETCH
  __    67.00  ET07 STRIP       SUB-CMOS-ET07-METAL    1.0  SUB-CMOS ASH RESIST
  __    68.00  SI01 SINTER      SUB-CMOS-SI01          1.0  SUB-CMOS SI01 SINTER
  __    69.00  TE01 TEST RES    SUB-CMOS-TE01          1.0  SUB-CMOS TE01
  __    70.00  TE02 TEST XTR    SUB-CMOS-TE02          1.0  SUB-CMOS TE02       +
F2=Fold   F3=Exit   F4=Prompt   F12=Cancel   F23=More options   F24=More keys
```

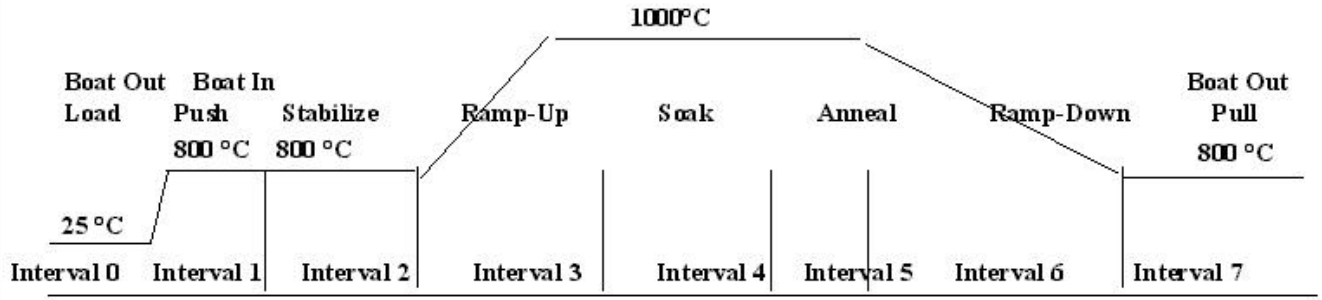
INSTRUCTIONS

```
    5/10/01                          MESA                    IGMSINQ    S36801
   14:05:05                 Instruction Group Inquiry        MICROGURU    RIT

Type information.  Then Enter.
  1=Display document, 5=Display detail

  Plant  . . . . . :   RIT
  Instruction group  . .   CMOS-OX04-ALIGNMENT   CMOS OX04 ALIGNMENT OXIDE
    Revision . . . . .   3.0

  Opt Subgroup  Text
    _           1.0 Include D1-D3
    _           2.0 Use resource FURNACE01 BRUCE TUBE 01  (see OX04.pps)
    _           3.0 Xox desired = 5000 A (see WellOx.pps)
    _           4.0 See SPC chart for operation (align_ox.pps)- execute step
    _           5.0 XRF warm up recipe 888, check gas & hydrogen supply
    _           6.0 When furnace stabilizes at 800 C
    _           7.0 XRF 5000 A wet O2 recipe 350, load wafers, press start
    _               P/P 800C, RU 20min, 120 min soak wet O2 1000C, RD 40 min
    _           8.0 When wafers complete, abort 350 and XRF idle recipe 999
    _           9.0 Record 3-zone temp, soak time, oxide thickness on D1 (se
                                                                      More...
F3=Exit    F4=Prompt    F5=Refresh    F10=View 2    F12=Cancel

MA    a                                                          12/005
```

IMAGE DOCUMENTS

BRUCE FURNACE RECIPES

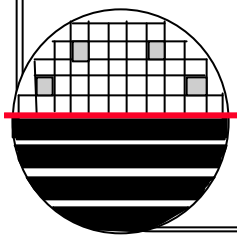
Recipe #350



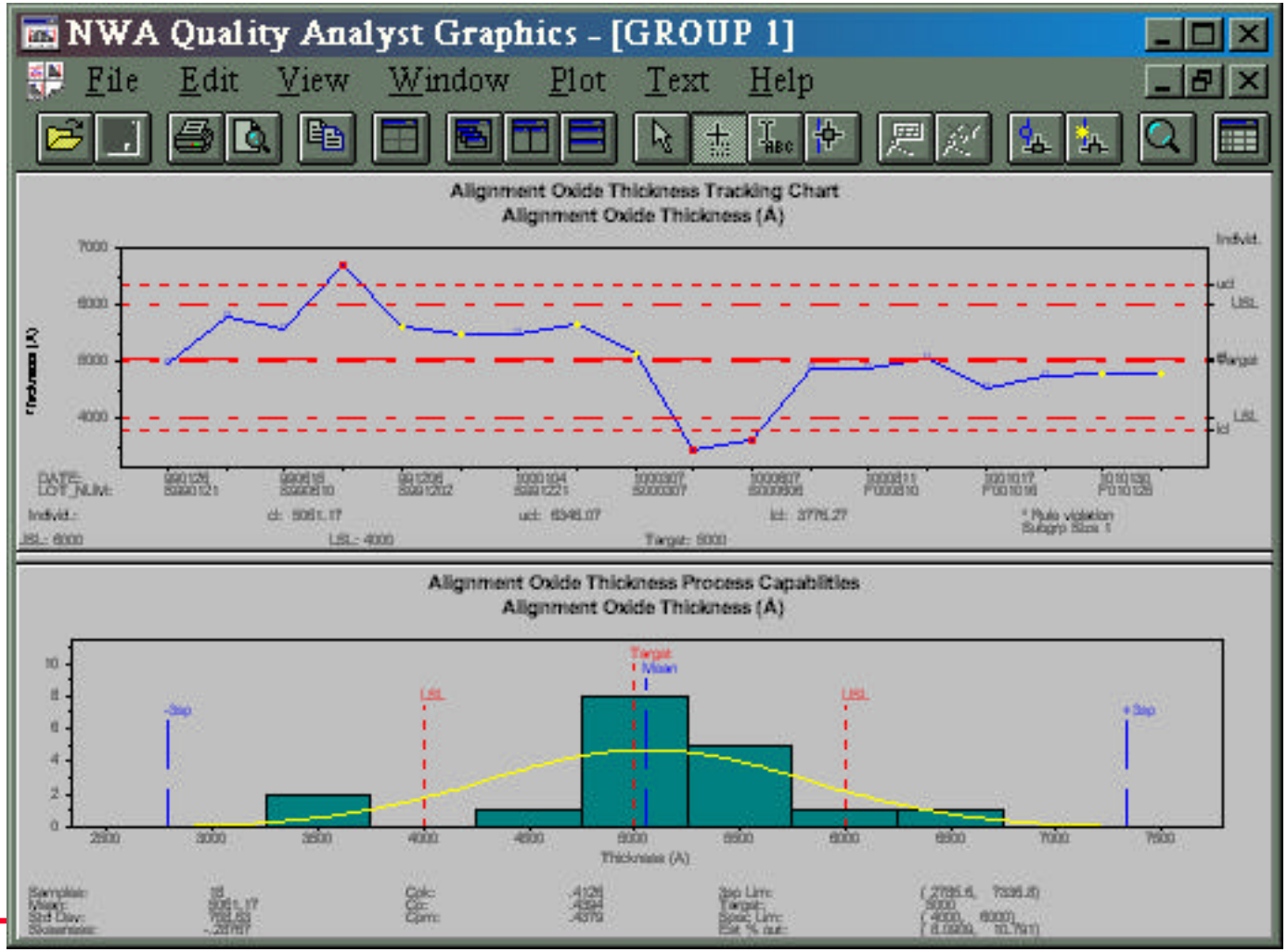
Any	12 min	15 min	20 min	120min	5 min	40 min	12 min
0 lpm	15 lpm	15 lmp	10 lpm	10 lpm	15 lpm	10 lpm	15 lpm
none	N2	N2	O2	O2	N2	N2	N2

At the end of a run the furnace returns to Interval 0 which is set for boat out, 25 °C and no gas flow. The furnace waits in that state until someone aborts the current recipe or loads a new recipe.

WIPTRACKING



SPC CHARTS

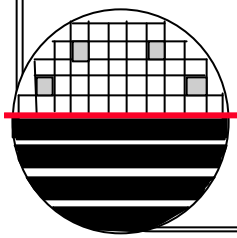

NWA Quality Analyst Graphics - [GROUP 1]
File Edit View Window Plot Text Help
Alignment Oxide Thickness Tracking Chart
Alignment Oxide Thickness (A)
Alignment Oxide Thickness Process Capabilities
Alignment Oxide Thickness (A)
Thickness (A)

SUMMARY

The process described can be used down to ~1.0 µm gate length.

A new process for gate lengths down to 0.5 µm is being developed that involves shallow trench isolation, dual doped gates and other process advances.

Several lots have been processed and final process adjustments are being made.



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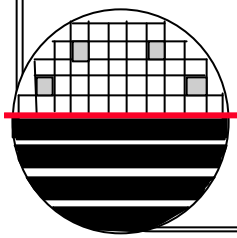
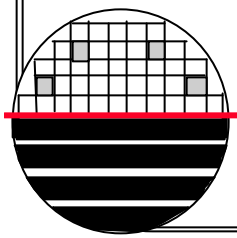
The process described can be used down to ~1.0 µm gate length.

A new process for gate lengths down to 0.5 µm is being developed that involves shallow trench isolation, dual doped gates and other process advances.



REFERENCES

- Silicon Processing for the VLSI Era, Volume 1 – Process Technology, 2nd, S. Wolf and R.N. Tauber, Lattice Press.
- The Science and Engineering of Microelectronic Fabrication, Stephen A. Campbell, Oxford University Press, 1996.



HOMEWORK – RIT CMOS2003

- Calculate the junction depth for both wells.
- Estimate the well doping by calculating the product of dose and junction depth.
- Using the calculated well doping and a surface state density of 1E11 calculate the threshold voltage for nmos and pmos FETs.
- Calculate the threshold adjust implant dose to give 1 and –1 volts for Vth.
- Calculate the width of the space charge layer for the drain when it is reverse biased by 3 volts.