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Nanolithography in Microelectronics: A Review

R. P. Seisyan

Ioffe Physical Technical Institute, Russian Academy of Sciences, Politekhnicheskaya ul. 26, St. Petersburg, 194021 Russia

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Abstract—The current status of basic photolithographic techniques allowing researchers to achieve results that seemed to be unrealistic even a short time ago is reviewed. For example, advanced DUV photolithography makes it possible to exactly reproduce IC elements 25 times smaller in size than the wavelength of an excimer laser used as a lithographic tool. Approaches owing to which optical lithography has pushed far beyond the Rayleigh–Abbe diffraction limit are considered. Among them are optical proximity correction, introduction of an artificial phase shift, immersion, double exposure, double patterning, and others. The prospects for further advancement of photolithography into the nanometer range are analyzed, and the capabilities of photolithography are compared with those of electronolithography, EUV lithography, and soft X-ray lithography.

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PHOTOLITHOGRAPHY IN MICROELECTRONICS

The latter half of the last century was marked by an extremely fast development of microelectronics. Most key figures of microelectronics are making headway so rapidly (exponentially) that no signs of deceleration, not to speak of stagnation, can be distinguished. There is good reason to believe that such a variation of the microelectronics indices is due first of all to a continuous exponential decrease in the IC feature minimal size $a_{\min}$ (the characteristic size of an IC), which is also called the design rule or critical dimension (CD). In this work, the author considers main techniques used to decrease the CD often by surmounting some seemingly obvious physical limitations.

Since the advent of the microelectronics era, advances in CD miniaturization have been bound solely to the progress in photolithography. Only companies having reached the acme of skill in photolithography can today design and produce advanced ICs and other electron semiconductor devices. Owing to the wave character of wave processes, the most important advantage of photolithography is the possibility of simultaneously transferring images consisting of many millions of elementary features [1]. It is this advantage that underlies the high technical and economical efficiency of photolithography and makes it possible to achieve a packing density (the amount of transistors per chip) as high as 10^7–10^{10}. The CD attained by photolithography has overcome a 100-nm limit and is now passing toward still smaller sizes [2], so that since 2000–2005 it can be viewed as a tool of nanotechnology. The aforesaid is illustrated by Fig. 1. First, nanosizes were achieved for the FET gate width in ICs owing to some techniques adding to gate shortening, and then, a few years later, nanometer design rules were applied to other elements of the IC layout. From that time on, microelectronics with features smaller than a certain CD began to be called nanoelectronics, although the principles of microelectronics remain applicable.

WAVE CHARACTER OF IMAGE TRANSFER AND DIFFRACTION LIMIT

The wave character of transferring each IC topological layer patterned by a mask is illustrated in Fig. 2 borrowed from [3]. It should be noted that initially the contact (or shadow-mask) method of image transfer was used, which dominated up to the beginning of the 1980s. Then, it gave place to the projection method

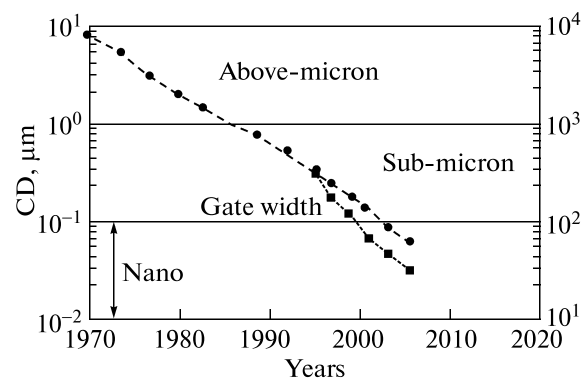


Fig. 1. Variation of IC design rules from year to year. The lower curve (filled squares) refers to the FET gate width.

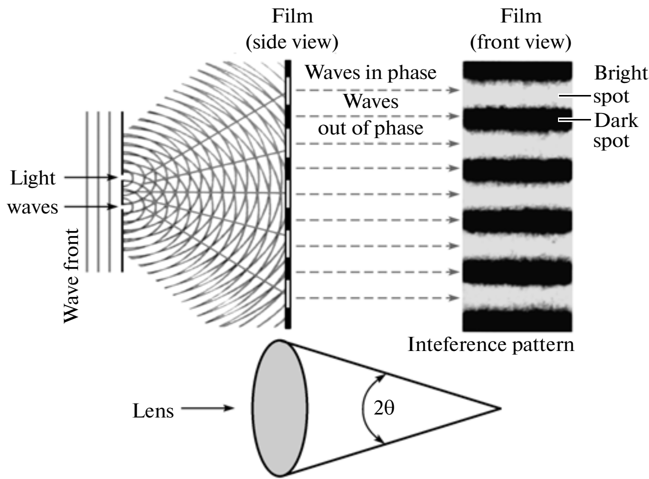


Fig. 2. Illustration of the wave nature of patterning in optical lithography. The lower part of the figure determines the lens aperture.

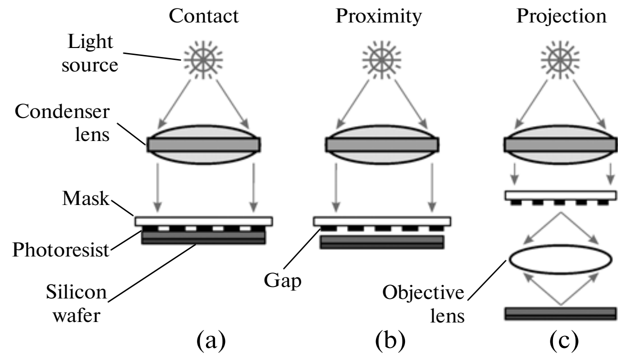


Fig. 3. Various versions of optical lithography: (a) contact or shadow-mask printing, (b) proximity printing, and (c) projection printing.

(Fig. 3), which proved to be much more efficient in CD miniaturization, since here the minimal feature size restricted by the diffraction limit is proportional to the actinic wavelength (in the contact method, the minimal feature size is proportional to the square root of the actinic wavelength [4], which is insufficient for CD significant miniaturization). Eventually, projection image transfer with scaling down was found to be optimal for IC patterning. In this case, the CD is determined by the diffraction limit of the optics (the so-called Rayleigh–Abbe criterion). The image of a point light source (Fig. 4) supports the validity of this criterion, according to which the CD is directly proportional to the product $\kappa_0\lambda$ and inversely proportional to numerical aperture *NA*. Here, λ is the wavelength of the actinic radiation (radiation providing photochemical recording of the image) and κ_0 is a factor equal to 0.61 for incoherent light [5]. Actually, however, this factor is a variable considerably depending on not only the degree of coherence but also on the imaging method (the variable quantity is denoted as κ_1, instead of κ_0, and is called the technological factor). With some technological approaches used successfully, κ_1 can be decreased to ~0.2 [6] (Fig. 5). Since in the case of projection image transfer the CD is directly proportional to the actinic wavelength, it is reasonable to diminish λ, which was the case throughout the history of microelectronics. The decrease in the wavelength and respective radiations are given in Table 1.

Figure 6 demonstrates one of the most sophisticated nanotechnology tools used in semiconductor fabs worldwide—an ASML TWINSCAN XT1700i scanning stepper [8] with a production capacity of 100 Si wafers 300 mm in diameter per hour in one topological layer equivalent (more than 100 33 × 26-mm microprocessor chips on a wafer are exposed). The radiation linewidth of the source (193-nm ArF laser) at a frequency of almost 10 kHz equals several picometers. The main element of the optics is a Zeiss objective lens made of deeply purified quartz and consisting of 30 lenses up to 300 mm in diameter. A Russian analogue of this objective made of fluorite single crystal [9] is shown in Fig. 7.

PHOTOLITHOGRAPHY AND ELECTRONOLITHOGRAPHY

As to the diffraction limit, electronolithography, which was expected to break a path to smaller linewidths, i.e., to nanolithography, was always considered as an alternative to photolithography. The potential of

Table 1. Radiation sources and respective wavelengths used in microelectronics [7]

Radiation source	Spectral line	Wavelength, nm	Spectral range
Mercury arc lamp	*g*	436	Visible
	h	405	"
	i	365	mUV
	DUV	240–255	DUV
Excimer laser	KrF	248	The same
	ArF	193	"
	F_2	157	VUV

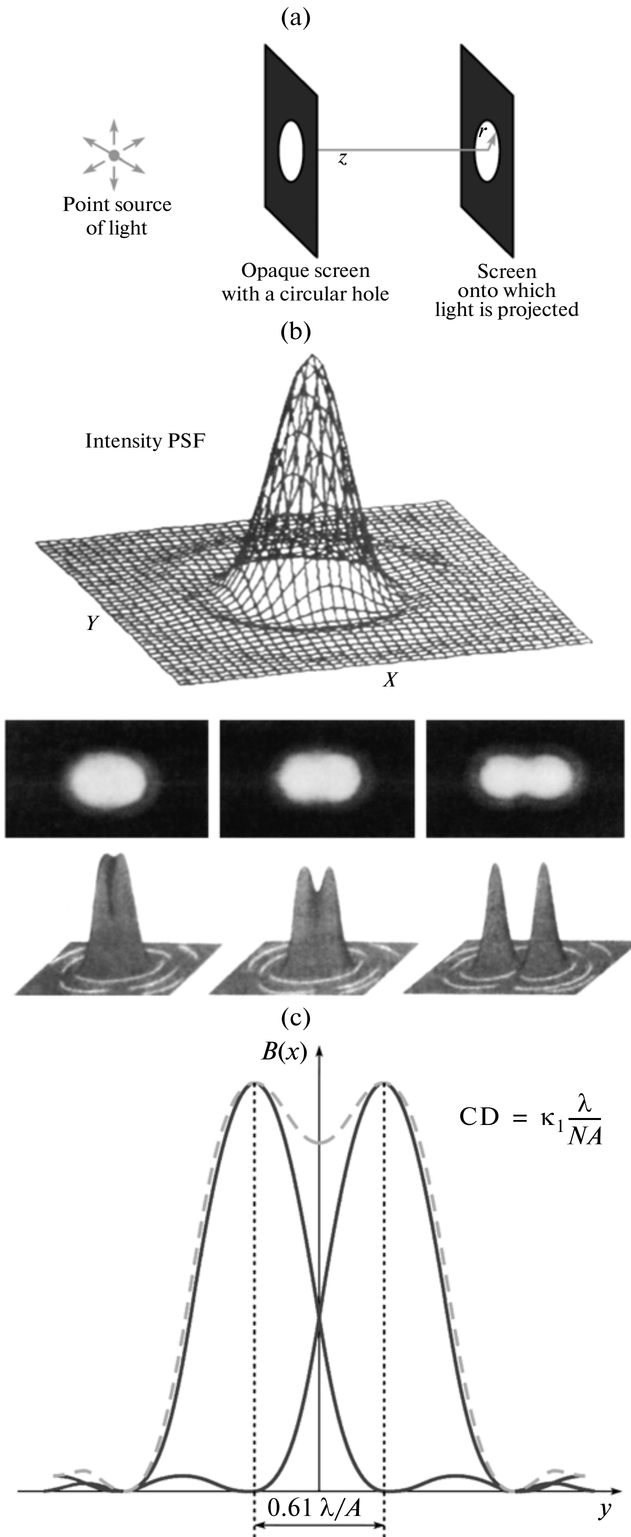


Fig. 4. (a) Image of a point light source, (b) image of two point light sources resolved according to the Rayleigh–Abbe criterion, and (c) explanation of the Rayleigh–Abbe criterion.

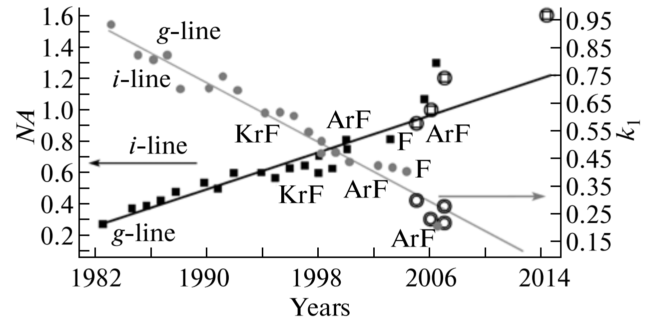


Fig. 5. Year-by-year variation of the parameters entering into the Rayleigh–Abbe criterion: *NA*, numerical aperture; k_1, technological factor. Main sources of radiation are indicated (see Table 1).

electronolithography is well known (the electron microscope is an example). The resolution of electronolithography was almost always higher than that of photolithography. Basically, however, using a fine-focused beam, one can write a pattern elementwise or piecewise, which elongates the writing (exposure) time. This comes into conflict with the exponential law of integration (so-called Moore's law). As early as at the rise of microelectronics, Wallmark [10] noted that there must be a time lag between the achievement of an ultimately small size for a single feature on the surface of a wafer (owing to the application of one or another method) and the achievement of this size in chip production. This lag depends on tolerance $\Delta P/P$ on electrical parameters P and integration level n. This statement continues to be valid. Indeed, for the normal operation of a chip, it is necessary that none of its n elements be out of tolerance on parameter P with a nonzero probability (corresponding to yield η). This means that we cannot take $a_{\min} = \mathrm{CD}$ as a design rule and have to shift toward larger $a_{\min} \gg \mathrm{CD}$. If the size deviations are distributed over a plane uniformly (randomly) and obey a normal (Gaussian) distribution, the probability that the deviation of a parameter from its rated value will not be out of tolerance is given by the Gaussian probability integral [10]

$$S_a = 1 - \left[\sqrt{\frac{2}{\pi}}\int_0^{y_1} \exp\left(-\frac{y^2}{2}\right) dy\right]^2,$$

where $y_1 = \alpha/(2)^{1/2}\delta_a$. According to the probability theory, the deviation is unavoidable, so that we must require that $S_a n > 1$ for n random independent events. In terms of the probability theory, the permissible minimal IC feature size ($a_{\min}$) for a given $\mathrm{CD} = \delta$ can be found from Fig. 8. The results seem discouraging: even for design rules as small as 22–32 nm, the minimal feature size must be 1.5–2.3 μm in ULSIs with 10^6 elements and 1.9–2.8 μm in ULSIs with 10^9 elements. A further shrinkage of design rules toward 5–13 nm (the goal of the next decade) could provide the production

Fig. 6. Appearance of an ASML TWINSCAN XT1700i scanning stepper (one of the most popular instruments today). $NA = 1.2$, $D = 45$ nm.

of at best submicron ULSIs [11]. Smaller sizes at a larger number of elements will inevitably cause inadmissible deviations of IC parameter values. Actually, however, ICs with the above integration levels are now routinely produced and the embodied design rules practically meet the limiting capabilities of photolithography. One can perceive such a situation without considering the fabrication of a single element (transistor) as an independent random event. Such would be the case if IC features were successively and independently written by a fine-focused electron beam rather than being imaged using the wave process, when all features are "written" concurrently and correlatively. It can be believed that exactly this circumstance illustrates the main advantage of photolithography and explains its dominance in microelectronics at all stages of its development [1, 11].

PHOTOLITHOGRAPHY HAS OVERCOME THE DIFFRACTION LIMIT

State-of-the-art optical photolithography has pushed design rules far beyond the diffraction limit toward smaller sizes and now is facing the challenging problem to implement CD = 22 nm. Using an advanced photolithographic objective lens with a numerical aperture of 0.95 and an ArF excimer laser, we obtain 124 nm as the initial Rayleigh criterion in air. Comparing this value with those implemented in practice by means of immersion (depending on wavelength λ, initial numerical aperture, and the increase in the numerical aperture (decrease in λ)), we can see how much the Rayleigh–Abbe diffraction limit is overcome. This overcoming component will be taken into account through technological factor κ_1, which is smaller than Rayleigh factor $\kappa_0 = 0.61$. Four main ways of overcoming the diffraction limit are (i) optical proximity correction, (ii) introduction of an artificial phase

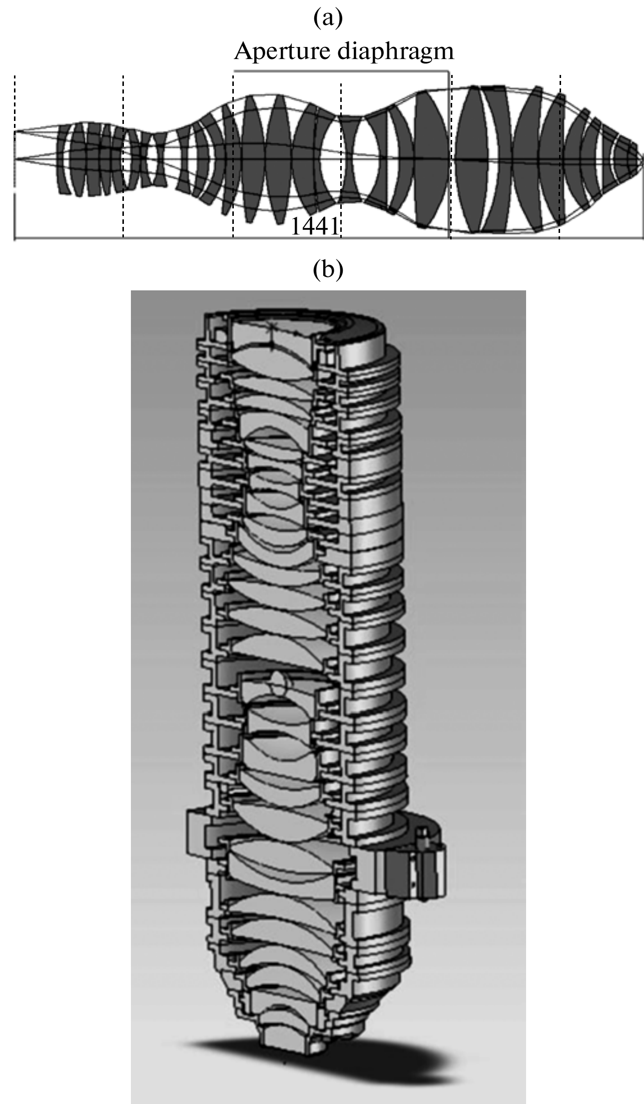


Fig. 7. (a) Longitudinal section and (b) structure of a typical imaging objective lens [9].

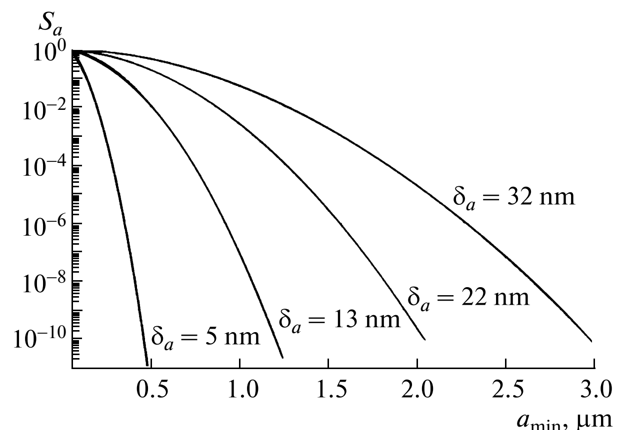


Fig. 8. Minimal permissible IC feature size a_{min} for the feasible CD (δ in the figure) according to the probability theory.

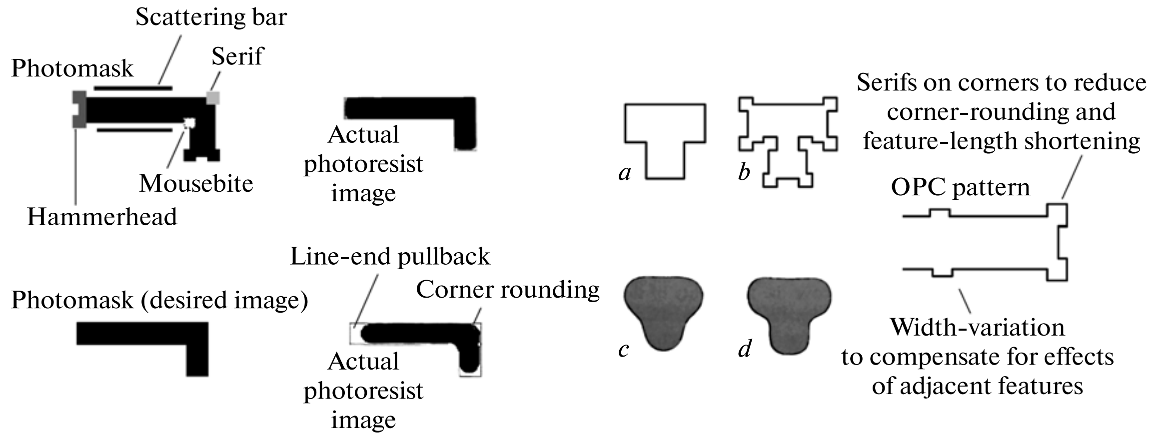


Fig. 9. Optical proximity correction using T-shaped and Γ-shaped IC features.

shift, (iii) immersion, and (iv) double exposure and double patterning.

Along with the above methods to overcome the diffraction limit, other independent approaches can be simultaneously used with this aim in mind: off-axis mask illumination and the application of a multilayer resist and silylation during resist development. Let us consider the ways listed above separately.

Optical Proximity Correction

When a mask microfeature with sizes equal to, or smaller than, the Rayleigh–Abbe limit is exposed, its image experiences different distortions, such as constriction or underexposure of a long narrow line, shortening and rounding of its ends, optical spread of narrow gaps and sharp corners, etc. Such distortions can be avoided by providing compensating elements on the photomask (see, e.g., [3, 4]). A typical way of distortion correction is demonstrated in Fig. 9 with T-shaped and Γ-shaped IC features. Here, we see corner serifs to reduce corner rounding and prevent IC feature shortening and also local variations of the linewidth to prevent its narrowing. These features make it possible to transfer a desired IC pattern with feature sizes much smaller than the "Rayleigh" size calculated for a given wavelength and a given numerical aperture by the Rayleigh formula (Fig. 4c). The application of these correcting features, while considerably complicating the photomask and imposing more stringent requirements for mask production tools, makes the IC pattern suitable for standard functioning of IC features with sizes beyond the diffraction limit. Program packages have been devised allowing designers to introduce elements correcting the optical proximity effect into a photomask and simulate the results of their application. The ways for correcting optical proximity effects have become an essential part of VLSI and ULSI technologies.

Introduction of an Artificial Phase Shift

The introduction of phase-shift elements is a very efficient approach to patterning ICs with a feature size beyond the diffraction limit. It was suggested as early as in the 1980s by Levenson et al. [12], and consists in adding extra features to a mask or in etching a groove that shift the phase of transmitted light. The idea is illustrated in Fig. 10. It is seen that an electromagnetic wave having passed through two adjacent areas of a photomask pattern can interfere destructively and, if the phase shift is 180°, quench the signal. To this end, either a rectangular groove is etched in the photomask substrate or a transparent layer with a given thickness and a higher-than-unity refractive index $n > 1$ is applied. It is easy to check, however, that the unmediated use of phase-shift insertions with a thickness such that $\Delta\varphi = (2\pi/\lambda)(2n - 1)$ is not generally applicable and so cannot completely solve the micropatterning problem. At least five types of phase-shift insertions are applied in different parts of an IC (see Levinson's work [7] and Table 2). They are often used together or in combination with masks for other elements of pla-

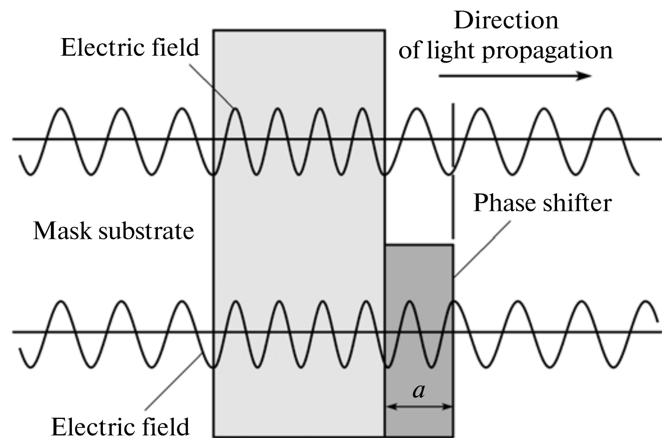


Fig. 10. Action of a phase-shift mask.

Table 2. Phase-shift masks [7]

Type of mask	Other name	Effect of resolution improvement	Application area
ALT	Levenson mask	Strong	Clusters of lines and spacings
RIM		Weak	Contacts, separate features
ATT	Semitransparent chrome, halftone pattern	The same	The same
PHE	Chromeless, unattenuated	Strong	Narrow lines
OTR	Subresolution, additional aperture	Weak	Separate features

nar technology. Nevertheless, all types of insertions spring from [12]. Alternating (ALT) phase-shift masks greatly improve the resolution, but they are efficient only for a pileup of narrow closely spaced lines. Rim (RIM) phase-shift masks, while producing a weak effect of resolution improvement, have a wide range of application, including IC solitary features. The same is true for cantilever-type (OTR) phase-shift elements, which however require additional space. Efficient resolution-improving means are also phase-edge (PHE) elements, but they are suitable first of all for patterning thin solitary lines. For example, a wide transparent chromeless mask that is etched out in the photomask substrate produces two dark extremely narrow strips at both phase edges upon exposure (Fig. 11). Halftone attenuated (ATT) phase-shift masks consisting of a transparent phase-shift layer covered by a semitransparent absorptive layer have a much wider area of application and are now in common use. These masks are often used to make contact pads and other separate features. Different phase-shift elements are shown in Fig. 12. Figure 13 demonstrates how a combination of phase-shift elements can be applied in patterning an FET unit of an advanced IC. Here, two types of masks and two photoresist layers are used. The first layer serves to etch six rectangular holes in the mask substrate to a depth providing a 180° phase shift, which is needed to pattern narrow FET gates. The second, chrome, layer serves to bound these gates and pattern other features.

OFF-AXIS MASK ILLUMINATION

Correct illumination of the mask is a key aspect of photolithography. It can be shown that the normal illumination of a mask with feature sizes smaller than the diffraction limit cannot provide adequate image transfer (see, e.g., [7]). Indeed, under normal incidence of light, only the zeroth order of diffraction falls within the aperture of the objective lens, while other rays (+1st and –1st orders of diffraction) remain outside the field of vision (Fig. 14). Imaging is absent, since each separate ray is a plane wave bearing no spatial information. When the mask is illuminated at an angle, both the zeroth-order ray and the first-order one fall within the aperture of the optics. In this case imaging takes place and, in addition, the depth of focus improves. Patterns thus formed by objectives with a smaller numerical aperture offer an increased depth of focus.

Immersion

Immersion has given powerful boost to the further development of microelectronics and specifically to further miniaturization of the IC feature size. Figure 5 shows a jump in the numerical aperture value observed in 2007–2008. While the use of immersion in optics is far from being a new approach (it dates back to the 18th century and was mentioned by Levenhuk in his letters to the British Royal Society), this way has long been considered doubtful. It is generally agreed that B. Smith, a professor at the Rochester Institute of Technology (United States), was the first to have success in this field [13]. He demonstrated that ordinary water injected into the space between the object and wafer can well be applied as an immersion liquid (Fig. 15). Water is transparent for 193-nm radiation, and its refractive index at this wavelength is 1.44. Accordingly, the laser wavelength in the immersion medium will be 134 rather than 193 nm. The numerical aperture of the objective lens can be calculated as $NA = n\sin\alpha$. The best value of the numerical aperture of an imaging objective in air is today $NA_0 = 0.95$, which is close to the limit. When combined with water immersion, the numerical aperture will be $NA = nNA_0 = 1.368$ (the ray paths in the immersion system are shown in Fig. 16). The use of water resulted in a considerable drop of the chip yield because of the evolution of dissolved gases in the form of bubbles. For this reason, some firms held back from applying immersion until effective countermeasures to bubbling were contrived. Moreover, immersion liquids have been found with a refractive index greater than that of water. However, they are not used today for various reasons.

Double Exposure and Double Patterning

Double exposure and double patterning [14] have appeared in the “toolbox” of planar technology quite

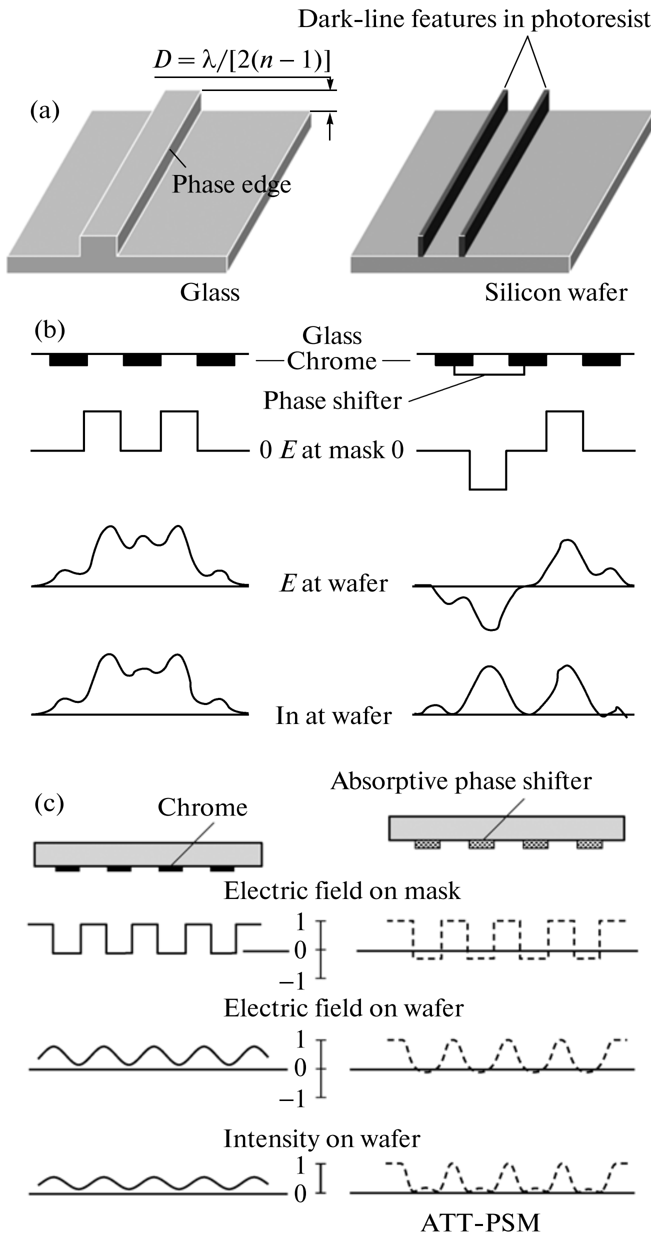


Fig. 11. Action of (a) PHE, (b) ALT, and (c) halftone ATT phase-shift elements.

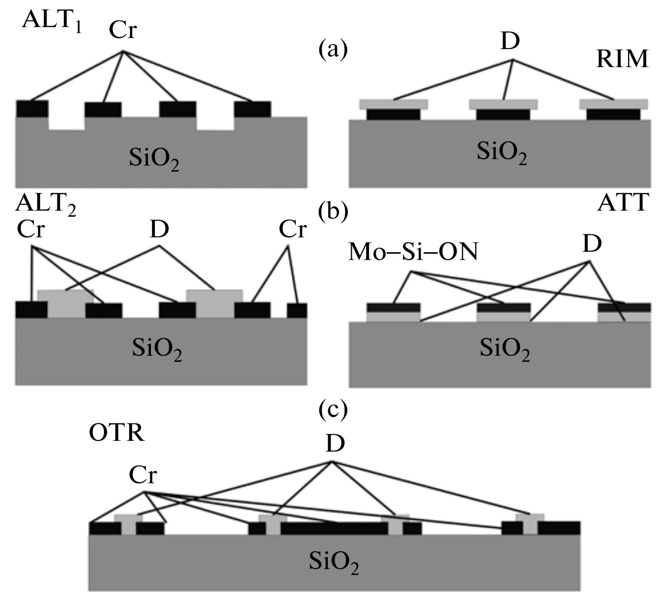


Fig. 12. Structure of (a) ALT, (b) RIM, (c) halftone ATT, and (d) OTR phase-shift elements.

recently. Yet, the application of exactly these procedures has provided a breakthrough in diminishing the IC feature CD. Double exposure consists in using two photomasks with complementary micropatterns when exposing the same photoresist layer. Double patterning is a more drastic technique. In this case, two complementary micropatterns are applied using a pair of matched photomasks. A photoresist is applied, exposed, and developed twice, so that two micropatterns embedded one in the other are created (Fig. 17). Obviously, these procedures became possible only after a new class of photoresists (so-called chemically amplified photoresists) [13] had been developed by IBM early in the 1980s. They were intended to prepare the transition to 250-nm design rules. It turned out that conventional resists with naphthoquinone diazide (NQD) and novolac resin as a sensitive component become inefficient at a wavelength of 248 nm or shorter, since both NQD and novolac resin strongly absorb in this spectral range and, in addition, the latter is of a low photosensitivity. Chemically amplified (CA) resists are resists of a radically new type in which a main photochemical reaction is not a direct consequence of the photon absorption. The operating principle of CA resists is illustrated in Fig. 18. A photon enters into a reaction with a photoacid generator (PAG), which is added to the resist in a small amount. The PAG generates an acid, which modifies polymer matrix links, making them soluble. Importantly, the PAG, having reacted with polymer chain links, recovers like a catalyst. Recovering may take place 500–1000 times mostly in the course of postexposure heat treatment. CA resists offer a high sensitivity (10–50 mJ/cm^2), which persists down to very short waves including extreme ultraviolet; a high resolution; and a high contrast of the transferred image [15] (Fig. 18). The high contrast is crucial for doubling the resolution and consequently the packing density of a chip. Note that the side walls of the developed resist in Fig. 17 are depicted vertical by convention, which to some extent approximates the high contrast. The disadvantages of CA resists, which reflect the catalytic nature of the process, are, e.g., a high probability of reaction quenching because of surface contamination by ambient air impurities in the interval between exposure and postexposure heat treatment. For example, contamination by ammonia makes the cross section of a strip

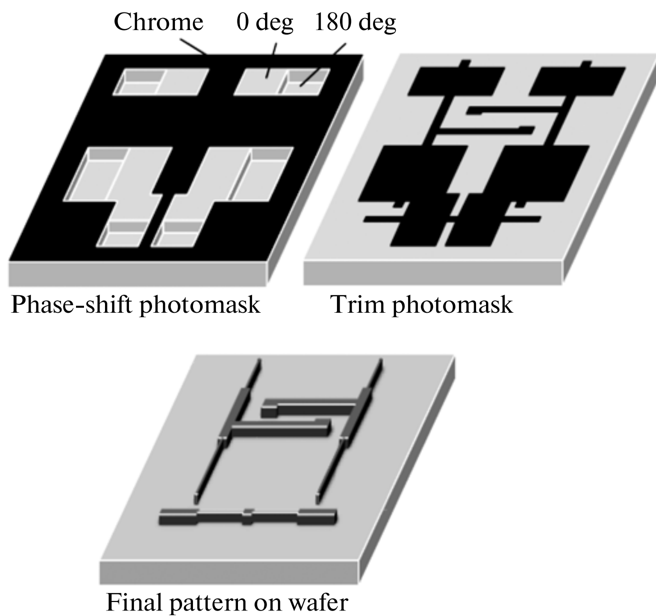


Fig. 13. Transistor unit patterned with a set of different phase-shift masks [13].

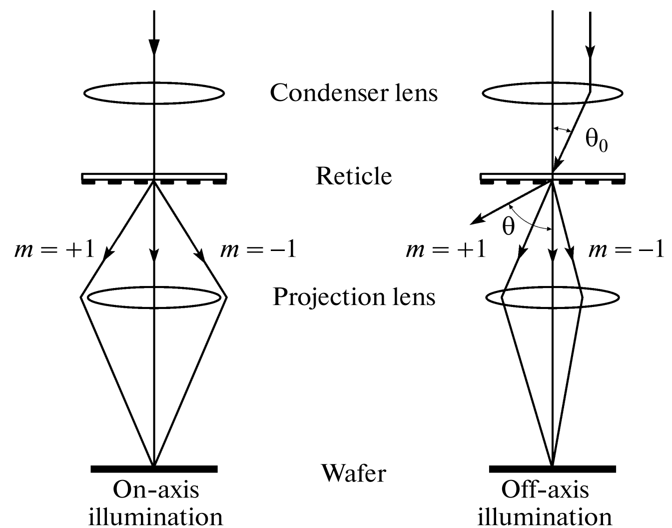


Fig. 14. On-axis vs. off-axis mask illumination.

T-shaped. To avoid contamination requires that special measures be taken to filter the ambient medium. This can be conveniently done by providing isolated "photoislands" on which a complete set of photolithographic procedures, starting from resists application, will be accomplished [3]. The inherent disadvantages of CA resists show up at CD ≤ 20–30 nm. They, as expected, arise from the extension of the polymeric matrix and the diffusion nature of sensitization (Fig. 18). In search of ways to decrease the adverse effect of these two factors, a low-molecular matrix is used and the diffusion process is optimized by properly selecting the PAG and postexposure heat treatment conditions [16]. Eventually, compositions and technologies have been found that provide the reproducible patterning of ICs with CDs of ≤20 nm down to 11–16 nm in the EUV range [15]. Still smaller CDs can be achieved with inorganic resists, in particular, semiconducting chalcogenide glasses. Chalcogenide glasses, which are applicable, specifically, in the DUV and EUV ranges, have been tested as resists for a long time [2, 17]. Experiments with 13.4-nm synchrotron radiation showed that a higher-than-30 nm resolution is feasible. However, chalcogenide glasses as resists must be applied in vacuum rather than by standard spinning in air. This hinders their use in microelectronics.

Double-Layer Resist and Silylation

If the IC pattern is developed isotropically, the photoresist thickness must be no greater than a minimal reproducible size. Certainly, this requirement may make the photoresist unstable against subsequent attacks necessary in IC fabrication. The way out of the situation is to use a multilayer, for example, double-layer, resist. The top layer should be thin so as to reproduce a fine pattern, while the thickness of the bottom one should be selected so as to make the resist stable against subsequent procedures; that is, the bottom layer must be thicker than the top one. In this case, one should make sure of the patterning accuracy in both layers. This problem can be solved by anisotropic image transfer, for example, by means of reactive ion etching. To this end, a silicon-enriched intermediate layer is provided between the top and bottom resist layers. Then, the resist is exposed to warm (90°C) silane in a thermostat at a pressure of 250 Torr for a time sufficient for silicon to diffuse to a depth of 300 nm. If now the sample is placed in an oxygen plasma at a pressure below 10 Torr, silicon dioxide SiO_2 forms in silicon-containing parts and silane-untreated regions are stripped off (burn out in the plasma). The resulting SiO_2 mask will reliably protect the top resist layer when

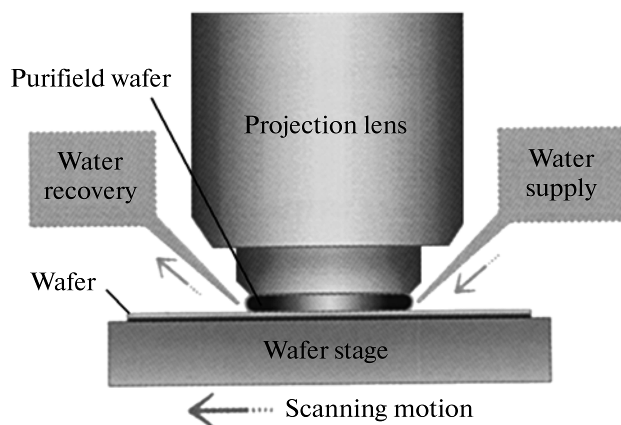


Fig. 15. Schematic of the immersion method in projection optics.

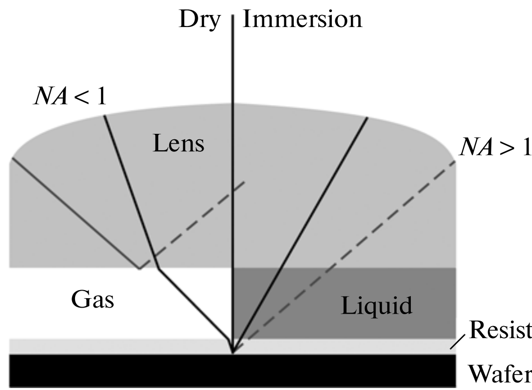


Fig. 16. Ray paths between an imaging object and a semiconductor wafer in air and in an immersion liquid.

its pattern is transferred to the thicker bottom layer and will provide quasi-vertical etching of the top layer. This process (Fig. 19) is called silylation [18]. It is successfully used in Si IC planar technology. Other ways of implementing this process are possible, but its essence remains the same: introduction of silicon into a single resist layer or into a resist system with subsequent application of the resulting SiO_2 film as a solid mask for reactive etching or oxidation.

CURRENT STATUS AND PROSPECTS OF OPTICAL NANOLITHOGRAPHY

The achievements of advanced optical lithography are amazing. Figure 20 shows the cross section of an isolated-gate FET fabricated in the Lincoln Laboratory at the Massachusetts Institute of Technology (the micrograph was taken under a transmission electron microscope) [19]. The transistor was patterned using two double exposures through phase-shift masks. The gate length here is as small as 9 nm. Remarkably, the structure was fabricated with a lithographer based on a 248-nm KrF laser. That is, the structure is less than 4% of the exposing radiation wavelength in size and is accommodated over 18 periods of the silicon lattice. This result shows that design rules above 10 nm are feasible using conventional optical lithography. Obviously, the selection criterion for the lithographic technique is today its cost efficiency rather than its technical performance. Figure 21 shows the SEMATECH consortium's forecast (2008) for lithographic techniques that will prevail in fabrication of microprocessors with design rules shrinking in the sequence 45—32—22 nm [20]. Optical lithography is predicted to dominate in the range 45—32 nm, while EUV lithography will prevail for design rules from 22 nm and below. Here, the cost and throughput of equipment, as well as

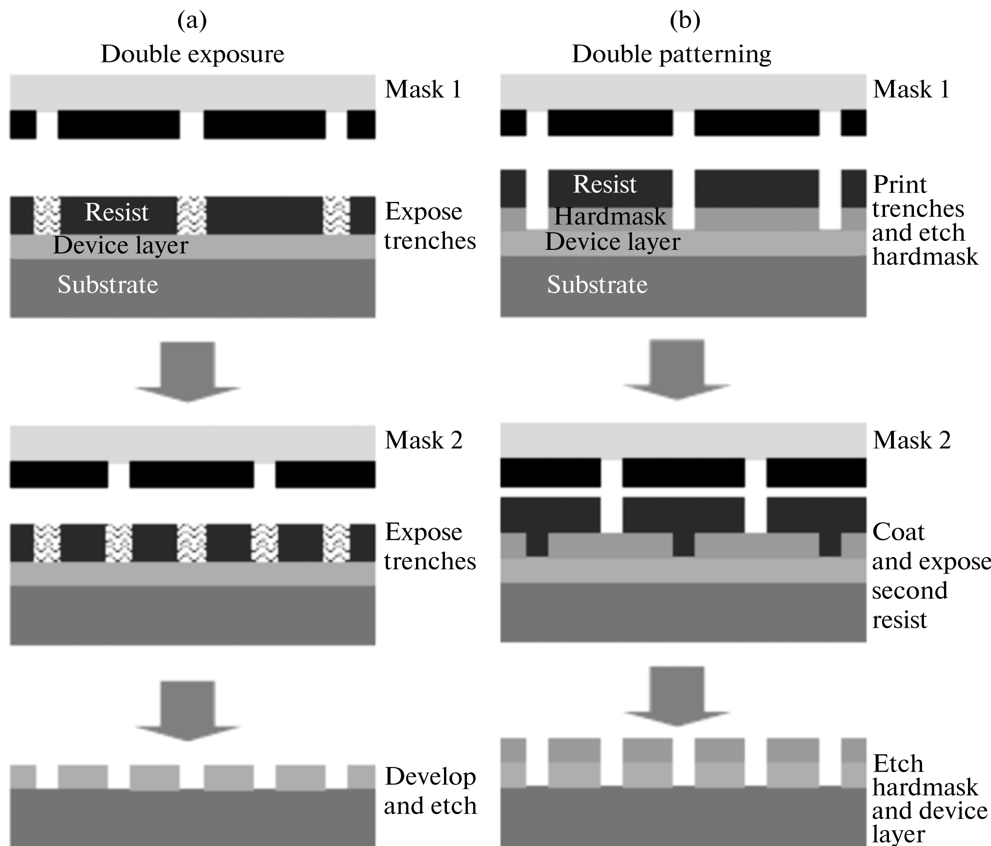


Fig. 17. (a) Double exposure and (b) double patterning. In the latter case, such approaches as lithography—etching—lithography—etching, lithography—freeze—lithography—freeze, and the spacer-defined process are used.

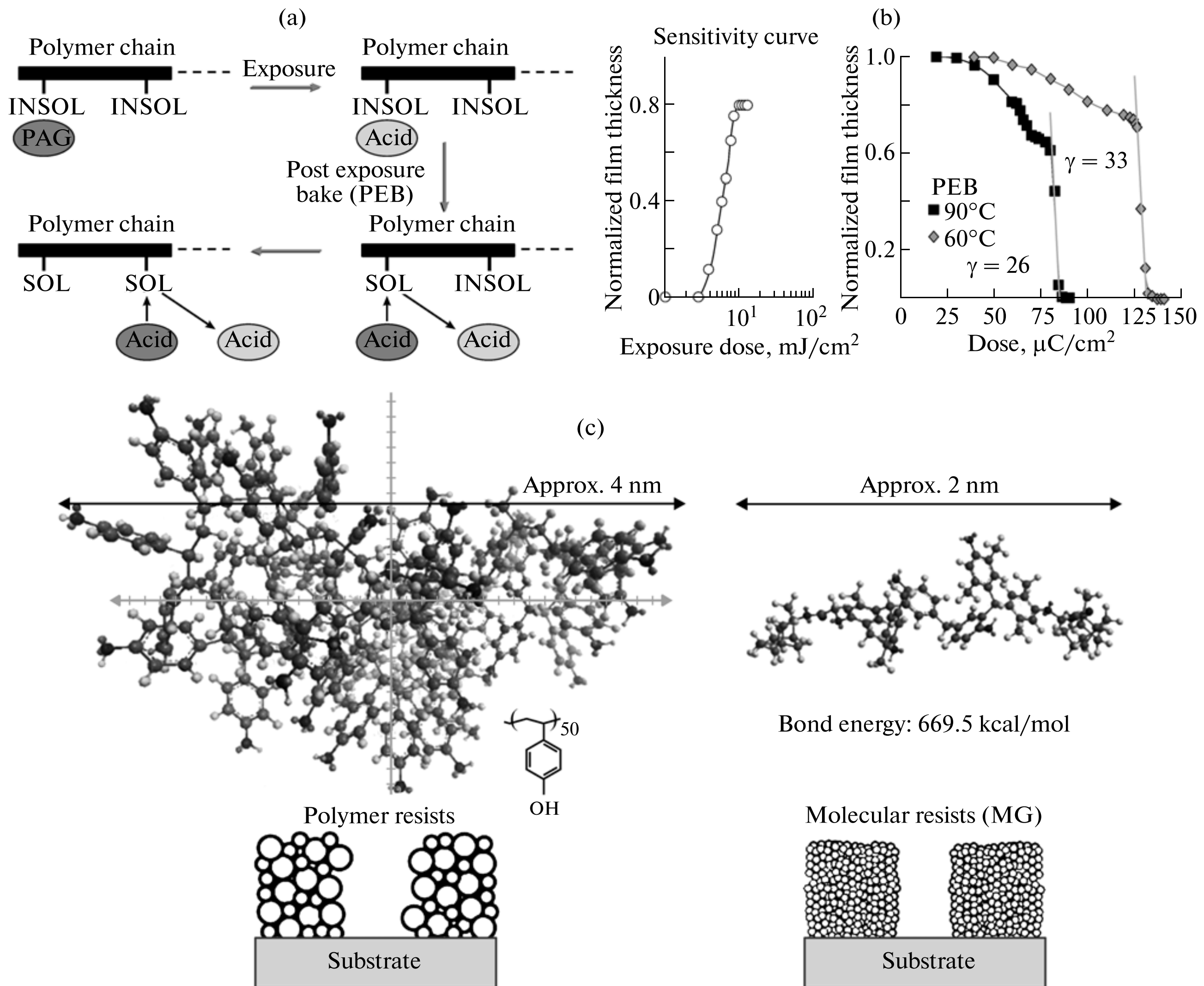


Fig. 18. (a) Action of the CA resist [3], (b) contrast achieved in the CA resist upon exposure to EUV radiation (on the left) and to an electron beam (on the right), (c) model and action of CA resists with extended and low-molecular matrices, and (d) patterning of the CA resist by 13.4-nm EUV synchrotron radiation (upper panels) vs. patterning of the chalcogenide glass by the same radiation (interference illumination, lower panels).

the cost of materials and mask sets, are taken into account (Table 3). A later forecast (2010) shifts the optical lithography boundary from 32 to 22 nm, leaving feature sizes smaller than 16 nm for EUV lithography. The question arises: how long will optical lithography dominate and how much will it advance toward smaller CDs? The battery of tools aimed at conquering the diffraction limit seems exhausted today. When discussing the competitiveness of EUV lithography, one should take into consideration first of all that the Rayleigh length at $\lambda = 13.5$ nm equals 18.7 or 16.5 nm at a numerical aperture of 0.3 and 0.5, respectively. Therefore, no special measures, such as the optical proximity correction and introduction of the phase shift, should be taken at CD $\leq$ 22–16 nm. This considerably simplifies the photomask design and technology and also cuts the number of lithography steps. As to EUV lithography, we also note that it is also characterized by wave image transfer and consequently offers all the advantages of wave patterning techniques. The above ways to overcome the diffraction limit (by artificially introducing a phase shift), which are typical of optical lithography using excimer lasers, are also quite feasible here. Possible approaches to introducing a phase shift in the case of EUV lithography are presented in Fig. 22. In addition, one should not disregard the transition to still shorter wavelengths from the soft X-ray range. Investigations of new-generation multilayer Bragg mirrors indicate that there are pairs of metallic coatings appropriate for wavelengths from 3 to 7 nm [21, 22]. Interestingly, since dispersive elements are absent in the optical components, their base can well be retained

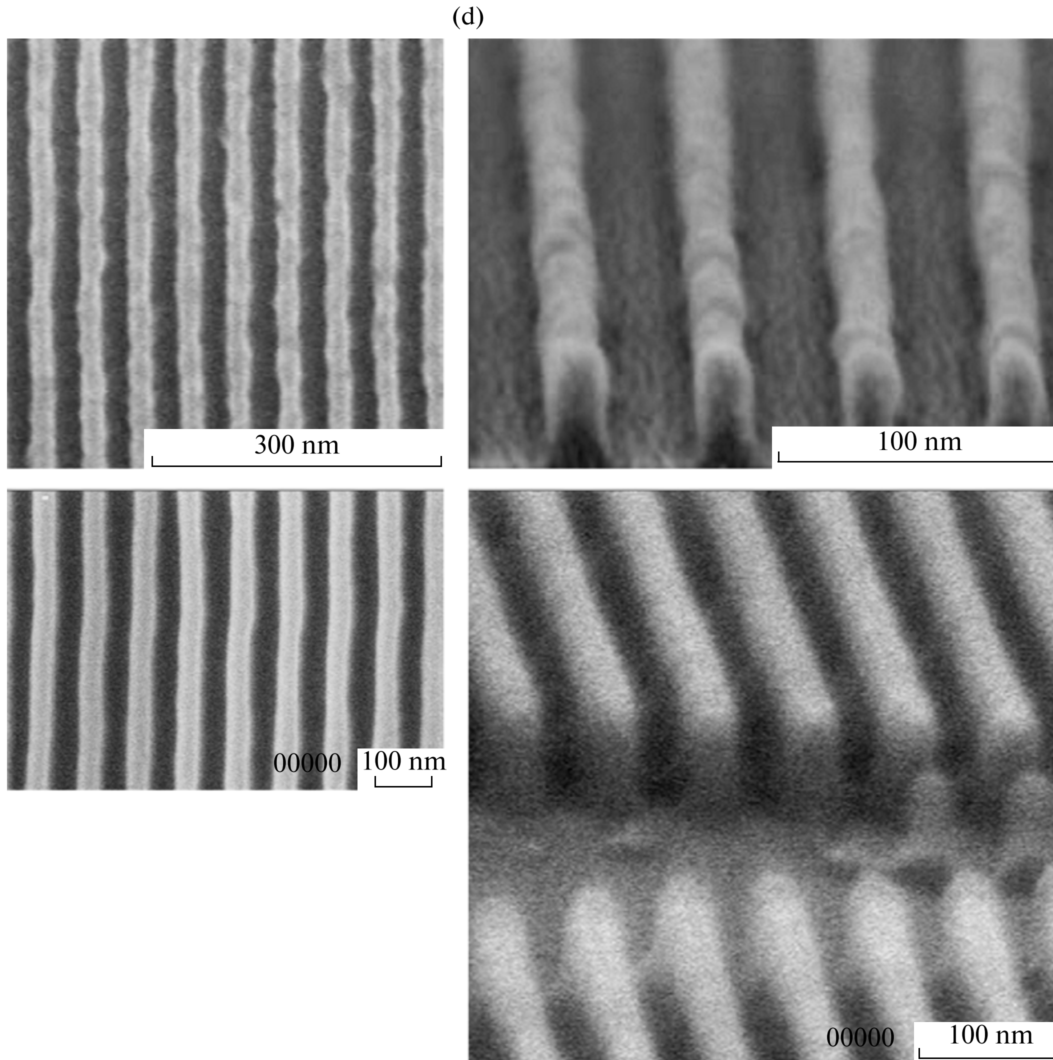


Fig. 18. (Contd.)

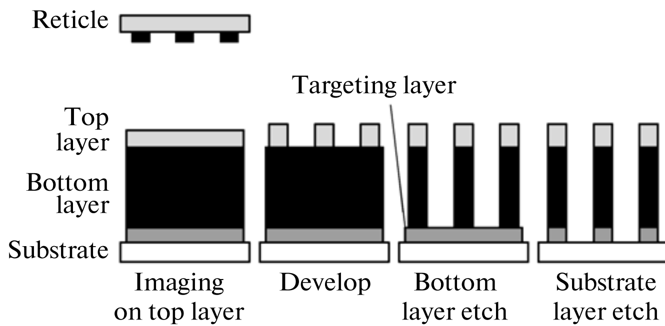
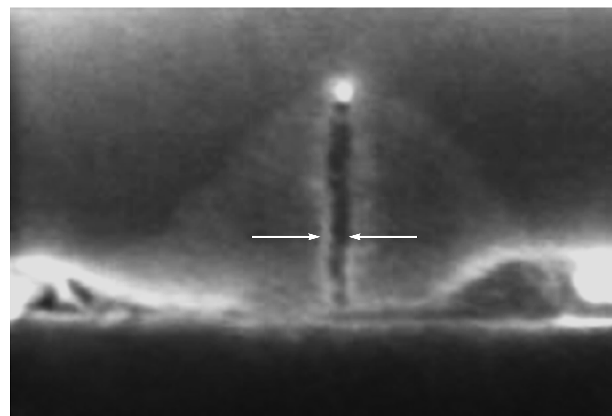


Fig. 19. Silylation process: exposure of a positive resist, heat treatment in silane (90°C, 250 Torr), enrichment by silicon to a depth of 300 nm, processing in a low-pressure (<10 Torr) oxygen plasma, formation of SiO_2, and stripping unexposed areas.



Gate length = 9 nm

Fig. 20. Isolated-gate FET as an element of an IC obtained with two double patternings (transmission electron microscope) [22].

Table 3. Parameters of the production costs model that were used for predicting the prospects of nanotechnology tools (see Fig. 21) [23]

	45 nm	22 nm		
	ArF (immersion), single exposure	ArF (immersion), double patterning	EUV lithography	nanoimprint lithography
Cost of lithographer, $M	40	52	89	
Throughput (number of wafers per hour)	200	200	100	
Cost of lithographer per wafer	0.3	0.3	0.9	0.3
Cost of mask (reticle), $	200000	1176000	252000	622000

but requirements for the surface roughness will be more stringent. However, one has to put up with a considerable decrease in the maximal reflection coefficient. In this case, the number of mirrors should be minimized and the power of the radiation source should be increased.

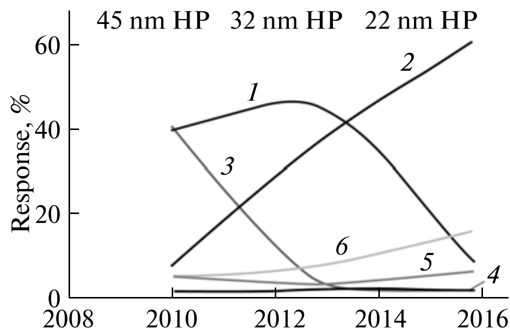


Fig. 21. Competitiveness of different lithographic techniques for the CD < 45 nm (result of the specialist opinion poll in 2008): (*1*) 193 nm, immersion and double patterning; (*2*) EUV lithography; (*3*) 193 nm, immersion and single exposure; (*4*) nanoimprint; (*5*) 193 nm, immersion in high-refractive-index liquids; (*6*) maskless lithography (including electron-beam writing).

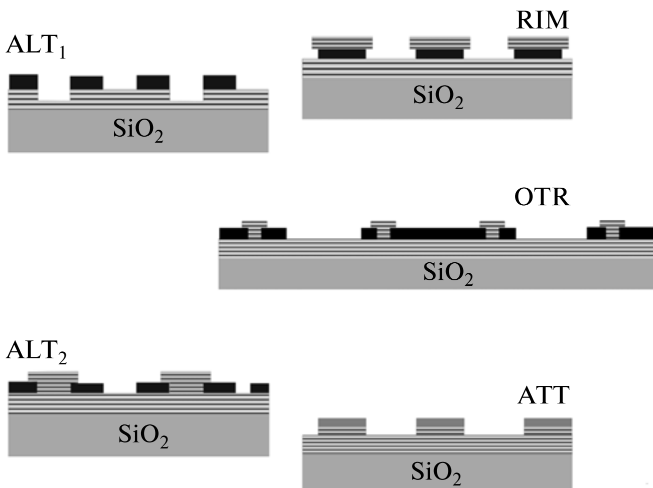


Fig. 22. Possible ways to introduce a phase shift in the EUV range (for abbreviations, see Figs. 11 and 12).

It seems that immersion should be excluded from consideration in the case of EUV, since no natural liquids are transparent in this spectral range. However, one can apply so-called metamaterials [23]. Note that optical lithography using excimer lasers still has room for advancement associated with fluorine (157 nm), argon (126 nm), and hydrogen (116 nm) lasers, which have not yet been in demand because of the rapid progress of 193-nm lithography. "Superimmersion" in liquids capable of raising the refractive index of water (1.44) by 20–30% also has not found wide application. The application of the listed lasers is restricted by the lack of optical materials appropriate for imaging objectives and photomasks, and the application of superimmersion is encountered with technological difficulties.

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