Departamento de
Engenharia Elétrica e
de Computação

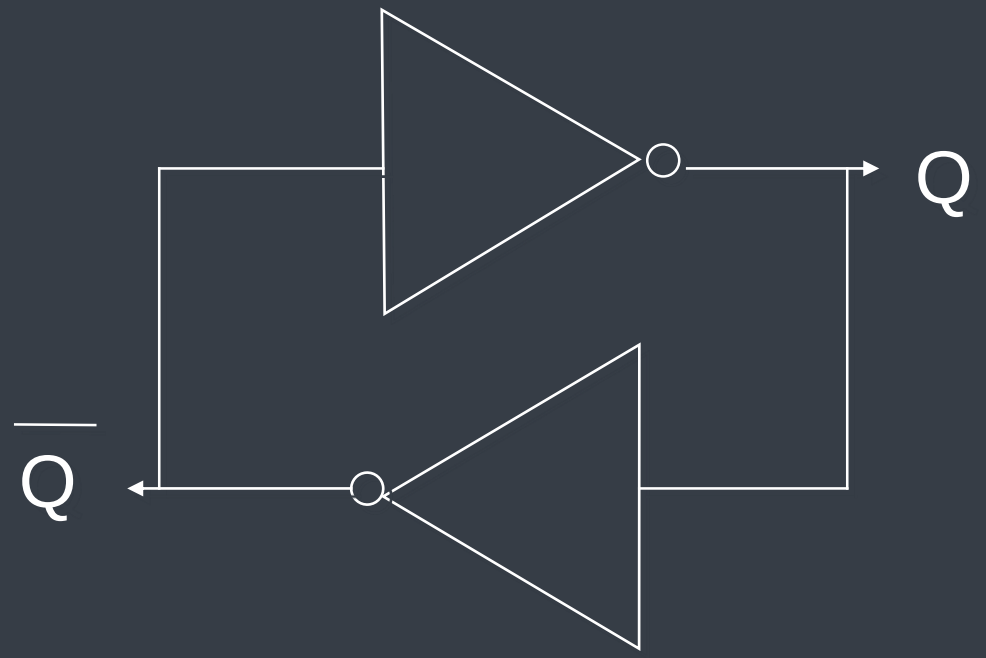
EESC • USP

SEL 414 - Sistemas Digitais

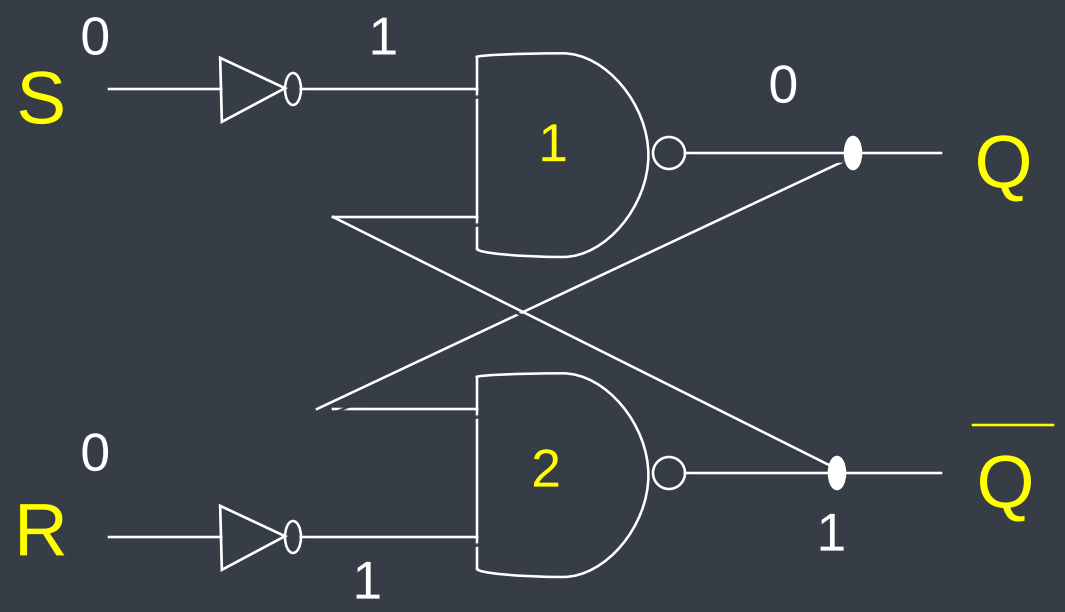
SISTEMAS SEQUENCIAIS (BIESTÁVEIS)

Prof. Homero Schiabel

*LATCH **RS***

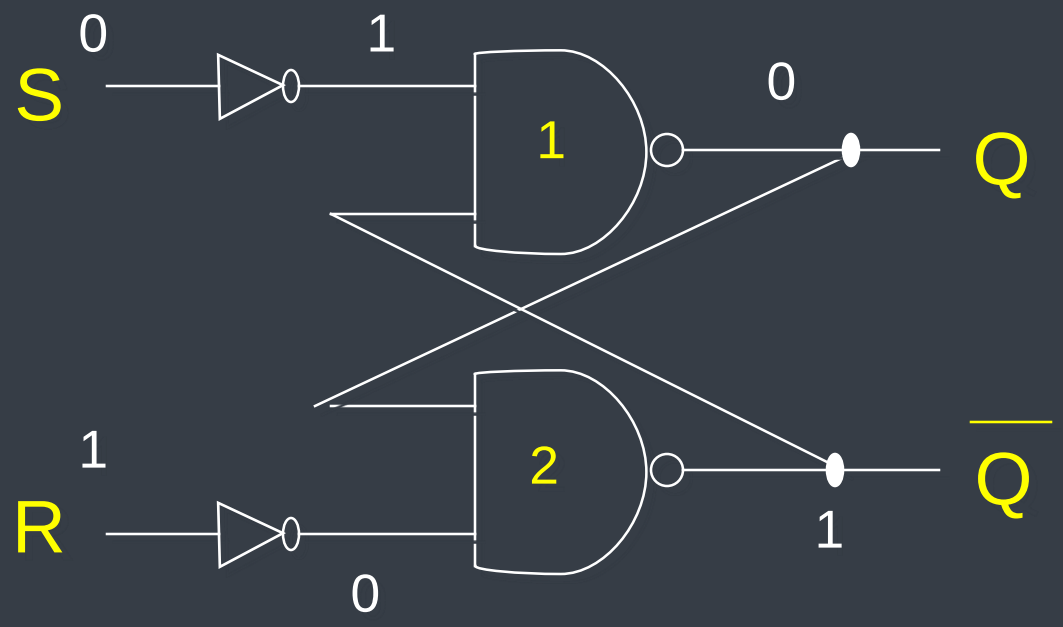


Condição Inicial ➔ Q = 0



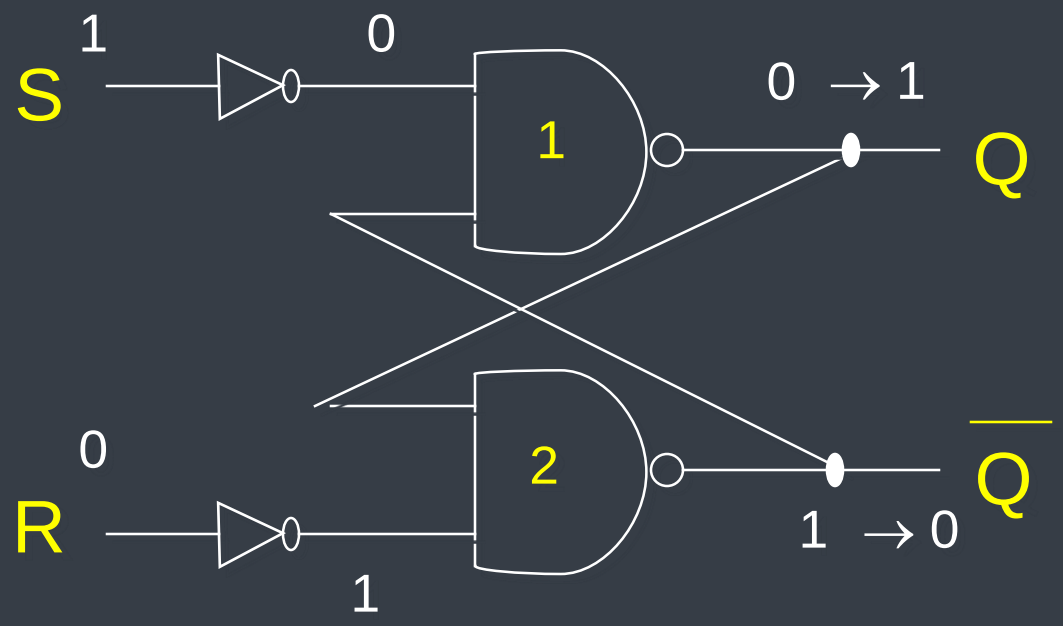
S	R	1	2	Q	$\overline{Q}$
0	0	1 1	0 1	0	1

Condição Inicial ➔ Q = 0



S	R	1		2		Q	$\overline{Q}$
0	0	1	1	0	1	0	1
0	1	1	1	0	0	0	1

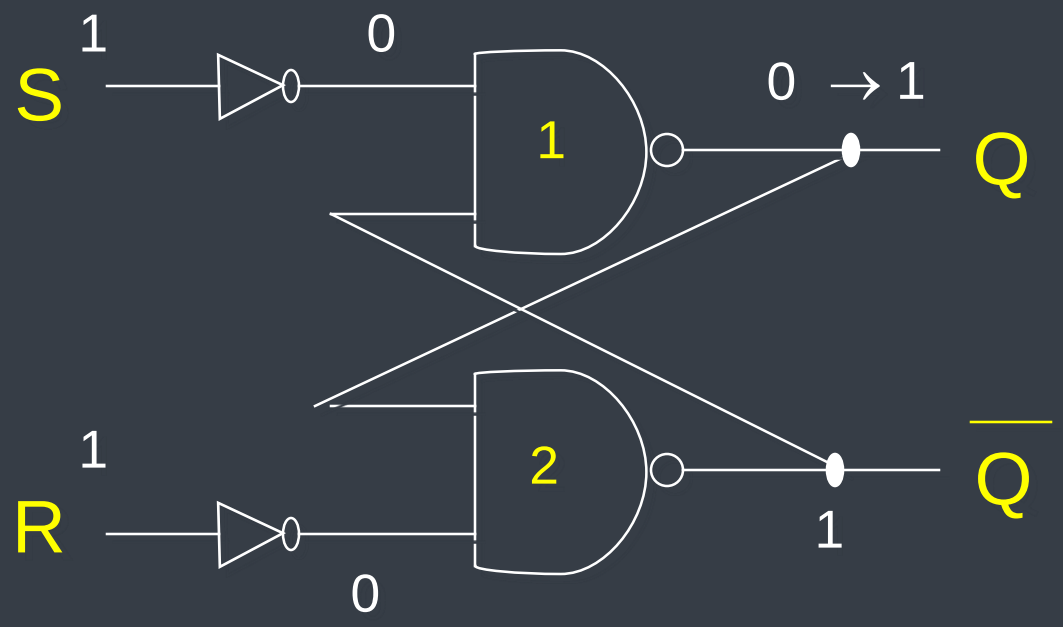
Condição Inicial ➔ Q = 0



S	R	1	2	Q	$\overline{Q}$	
0	0	1 1	0 1	0	1	
0	1	1 1	0 0	0	1	
1	0	0 1	0 1	1	1	*
		0 1	1 1	1	0	

* Estado instável

Condição Inicial ➔ Q = 0

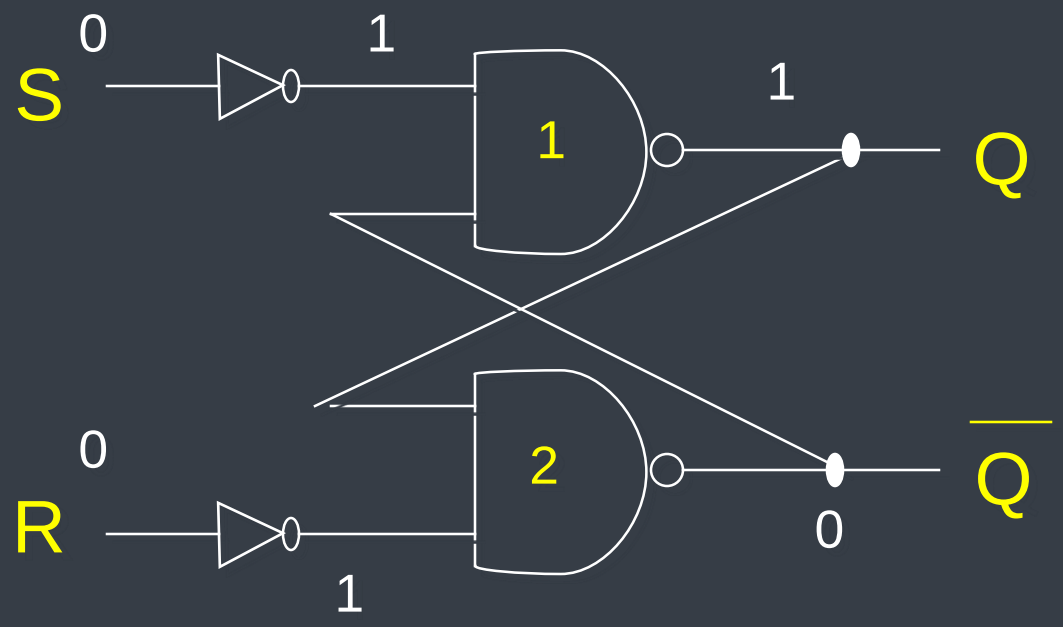


S	R	1	2	Q	$\overline{Q}$	
0	0	1 1	0 1	0	1	
0	1	1 1	0 0	0	1	
1	0	0 1	0 1	1	1	*
		0 1	1 1	1	0	
1	1	0 1	0 0	1	1	
		0 1	1 0	1	1**	

* Estado instável

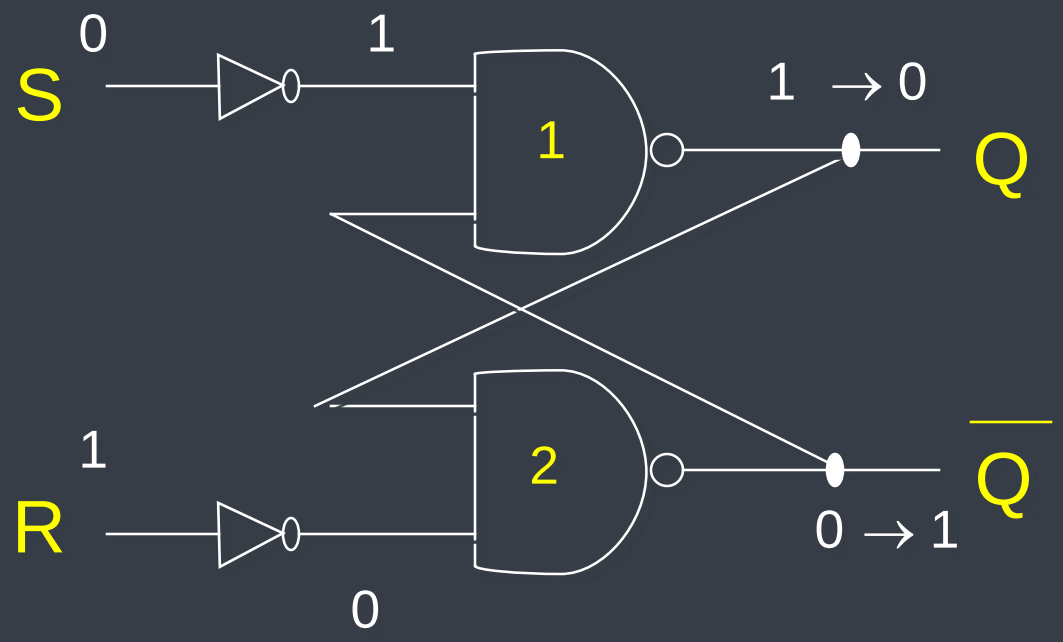
** “Incompatibilidade” (Est. “proibido”)

Condição Inicial ➔ Q = 1



S	R	1	2	Q	$\overline{Q}$
0	0	1 0	1 1	1	0

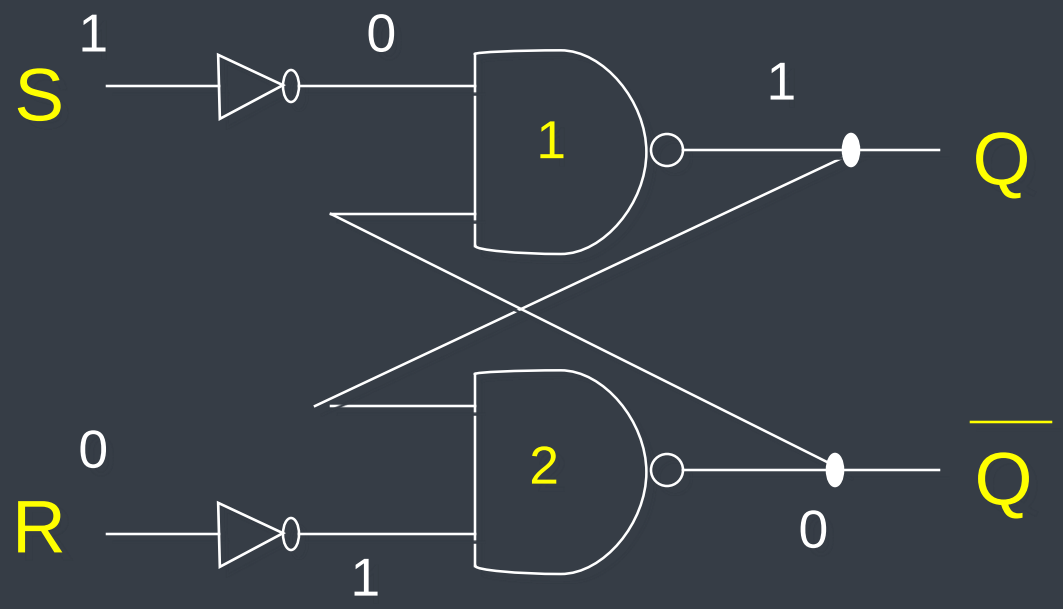
Condição Inicial ➔ Q = 1



S	R	1	2	Q	$\overline{Q}$
0	0	1 0	1 1	1	0
0	1	1 0	1 0	1	1 *
		1 1	1 0	0	1

* Estado instável

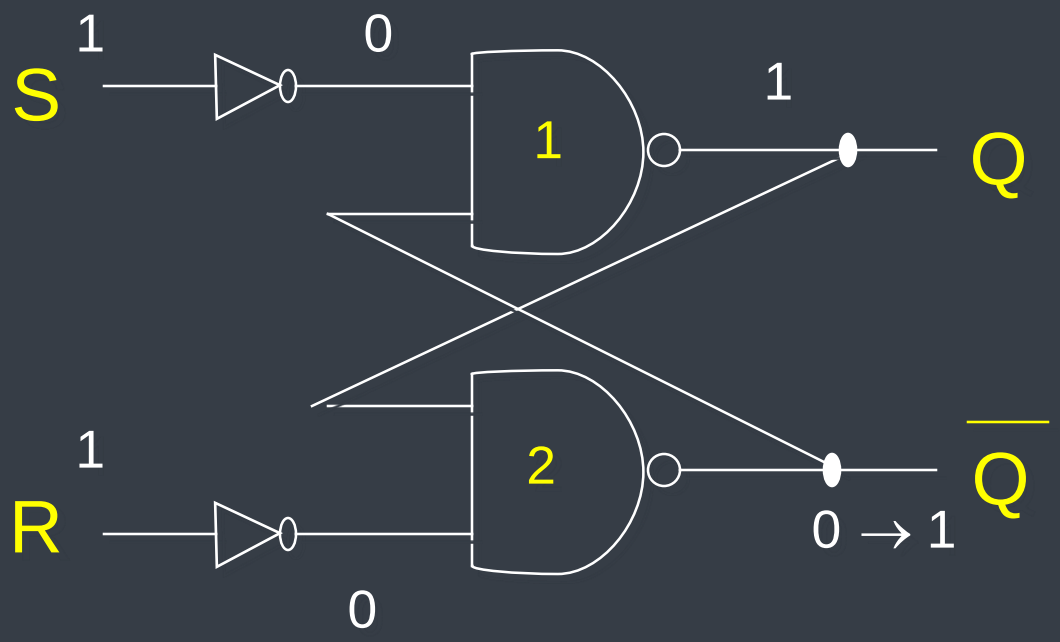
Condição Inicial ➔ Q = 1



S	R	1	2	Q	$\overline{Q}$
0	0	1 0	1 1	1	0
0	1	1 0	1 0	1	1 *
		1 1	1 0	0	1
1	0	0 0	1 1	1	0

* Estado instável

Condição Inicial ➔ Q = 1



S	R	1	2	Q	$\overline{Q}$
0	0	1 0	1 1	1	0
0	1	1 0	1 0	1	1 *
		1 1	1 0	0	1
1	0	0 0	1 1	1	0
1	1	0 0	1 0	1	1
		0 1	1 0	1	1**

* Estado instável

** “Incompatibilidade”
(Est. “proibido”)

Tabela da verdade:

Q = 0

S	R	Q	$\overline{Q}$
0	0	0	1
0	1	0	1
1	0	1	0
1	1	1	1**

Q = 1

S	R	Q	$\overline{Q}$
0	0	1	0
0	1	0	1
1	0	1	0
1	1	1	1**

Condição de memória!

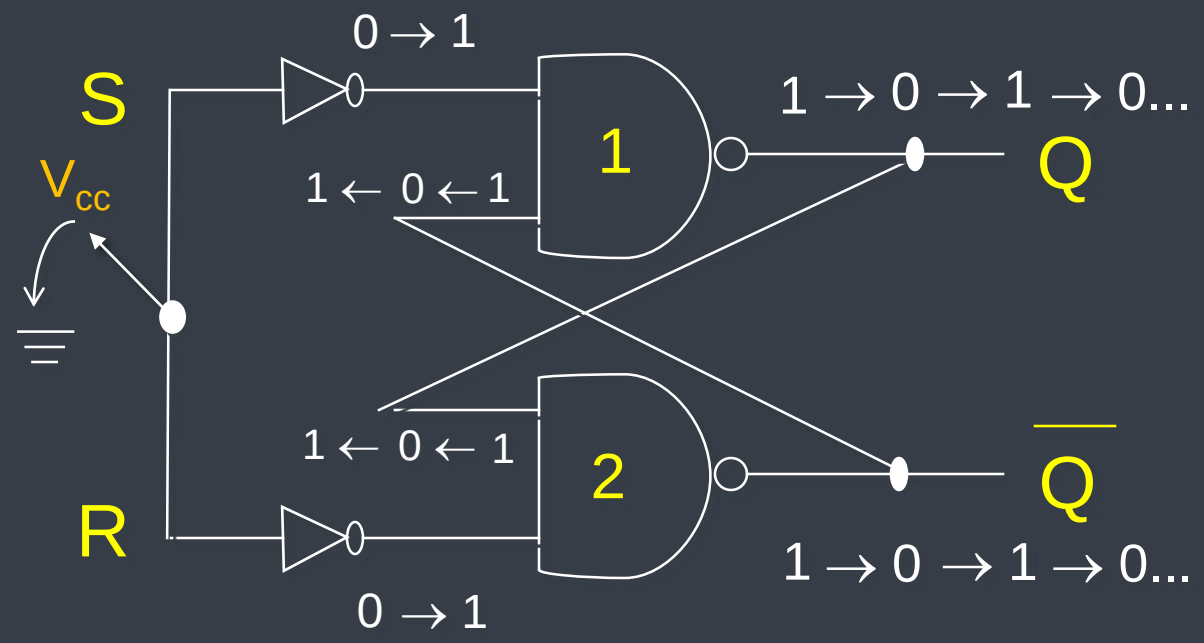
S	R	Q*
0	0	Q
0	1	0
1	0	1
1	1	1 **

Reset

Set

** “Incompatibilidade”
(Est. “proibido”)

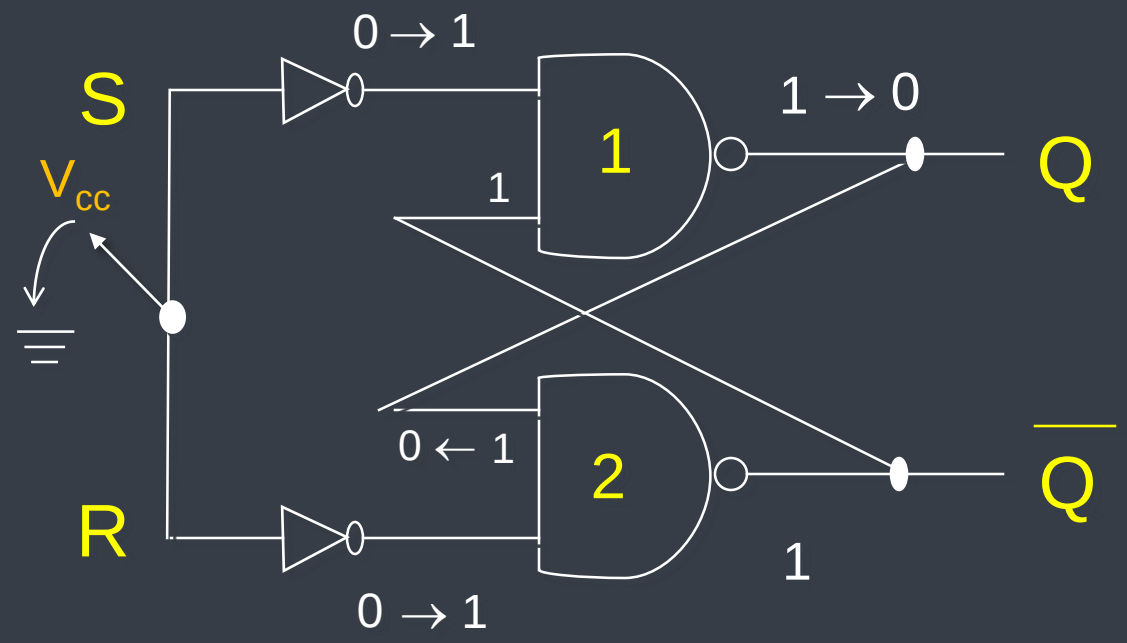
Mas... Por que “Estado proibido” (S=R=1)?



Condição de memória

S	R	Q*
0	0	Q
0	1	0
1	0	1
1	1	1 **

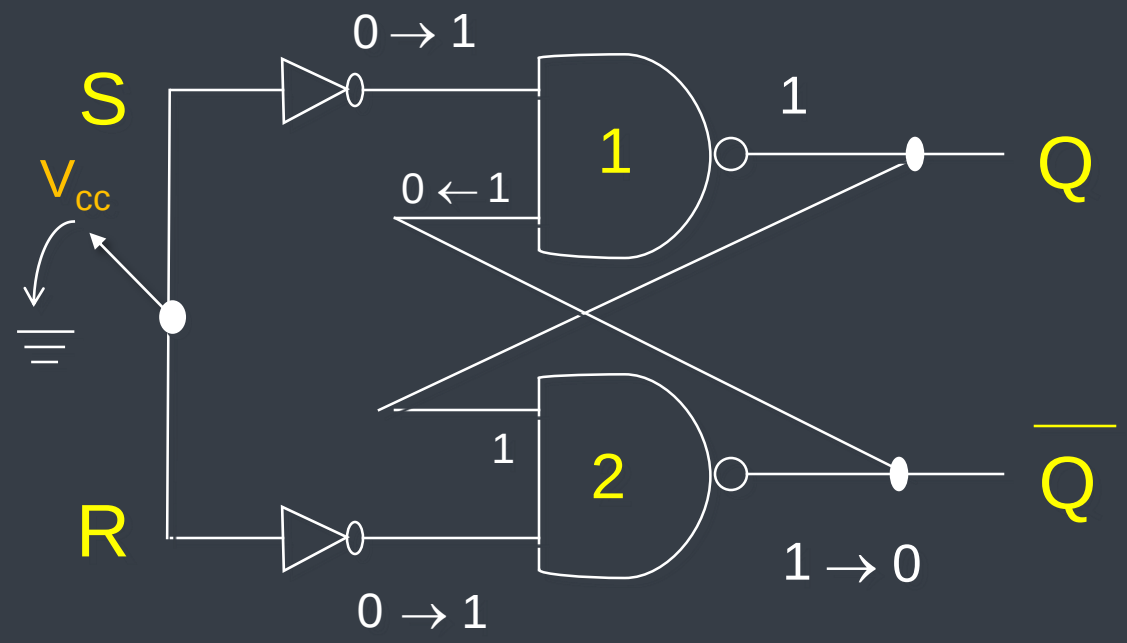
** “Incompatibilidade”
(Est. “proibido”)



Condição de memória

S	R	Q*
0	0	Q
0	1	0
1	0	1
1	1	1 **

** “Incompatibilidade”
(Est. “proibido”)



Condição de memória

S	R	Q*
0	0	Q
0	1	0
1	0	1
1	1	1 **

** “Incompatibilidade”
(Est. “proibido”)

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SISTEMAS SEQUENCIAIS BIESTÁVEIS

(Latch RS)

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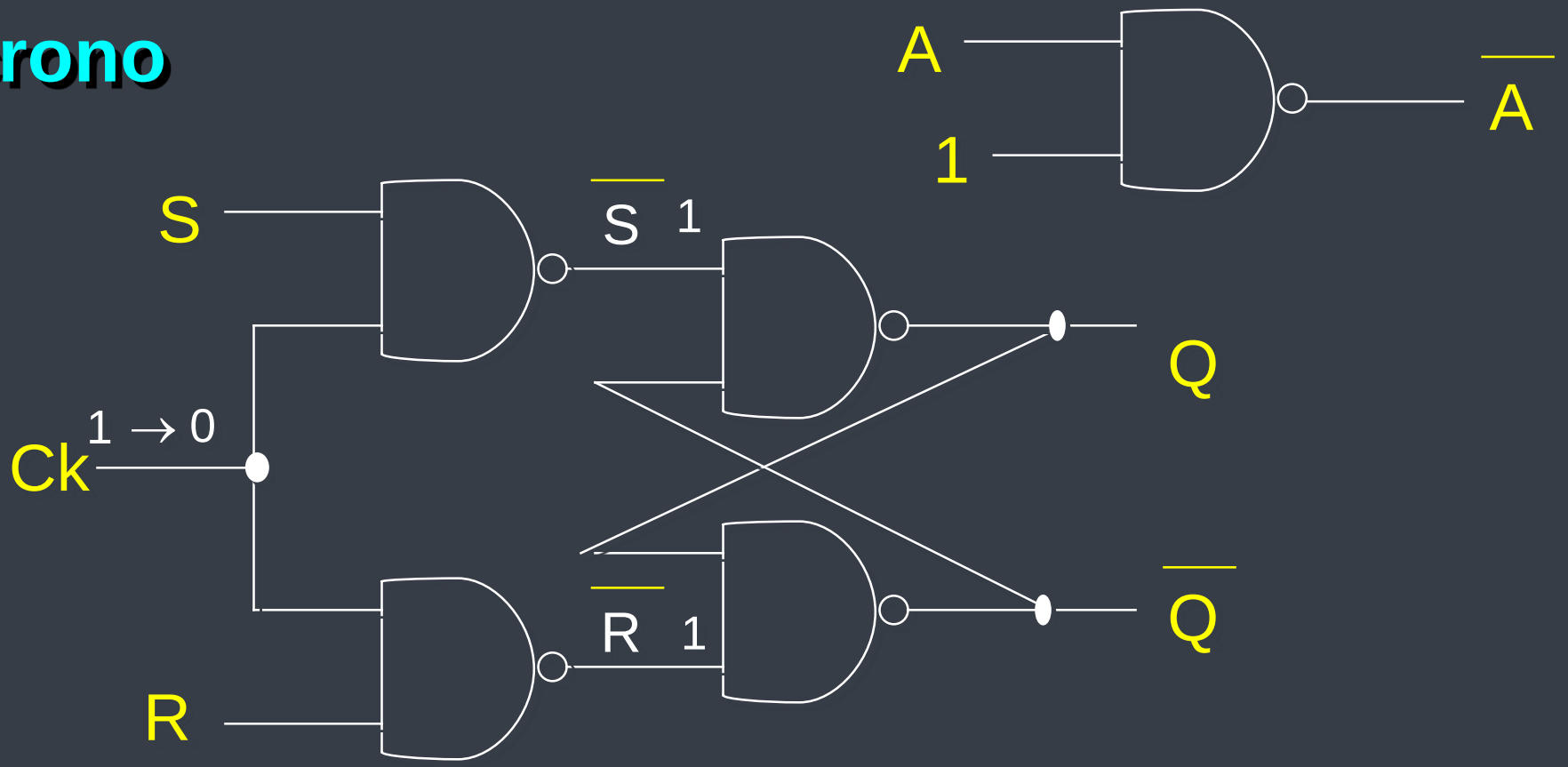
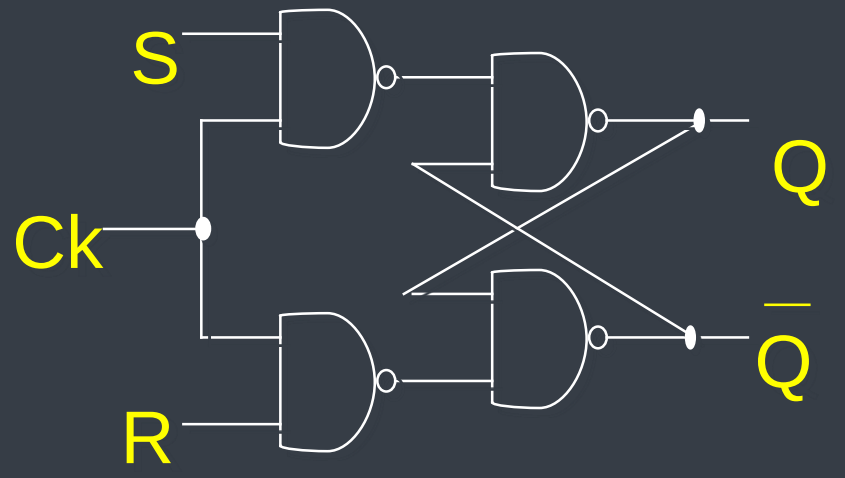
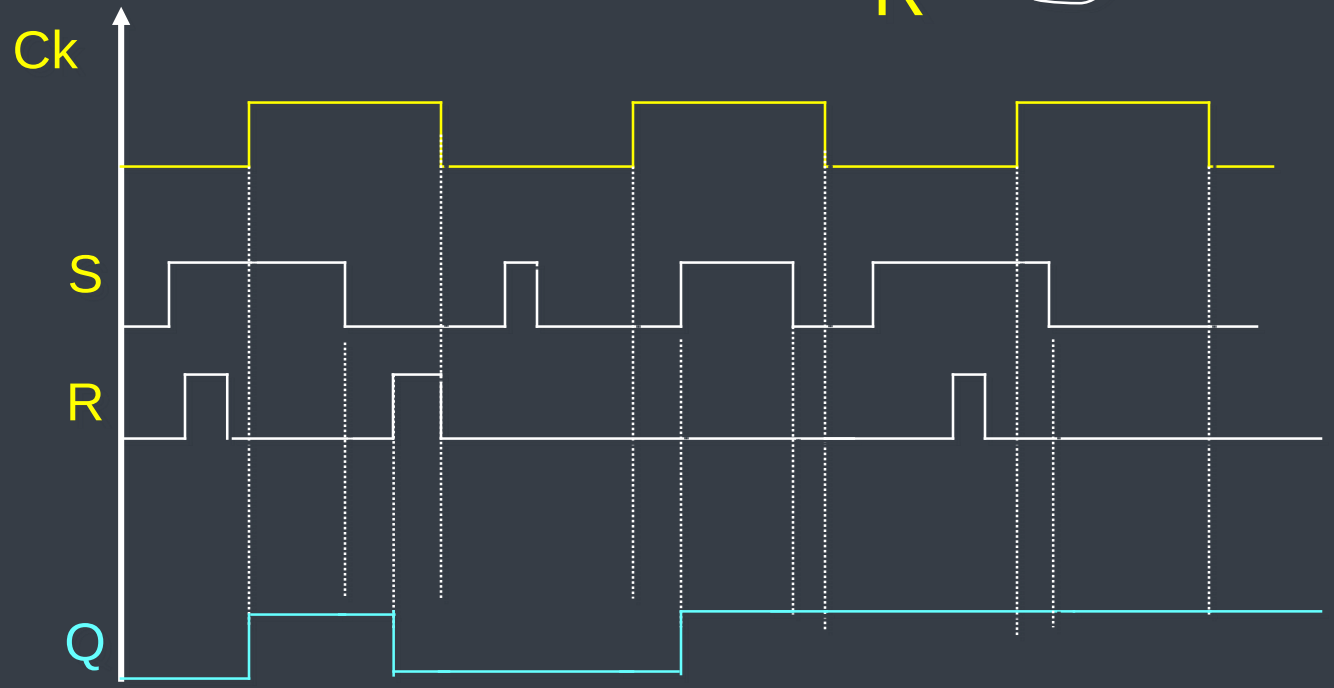
RS Síncrono



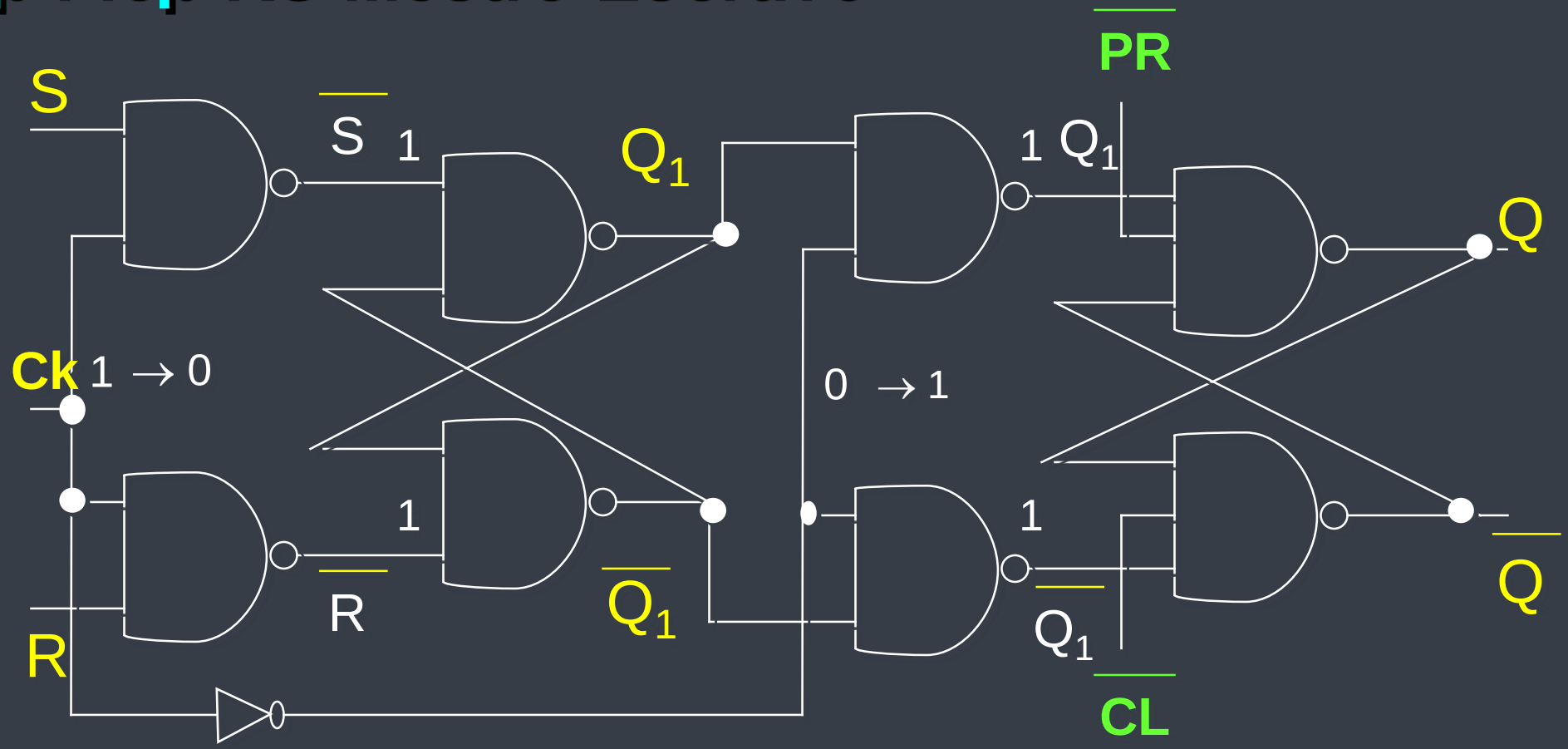
- Para Ck=0 ➔ Q e $\overline{Q}$ não “sentirão” eventuais variações nas entradas
- Para Ck=1 ➔ funcionamento normal (portas de entrada habilitadas)

RS Síncrono

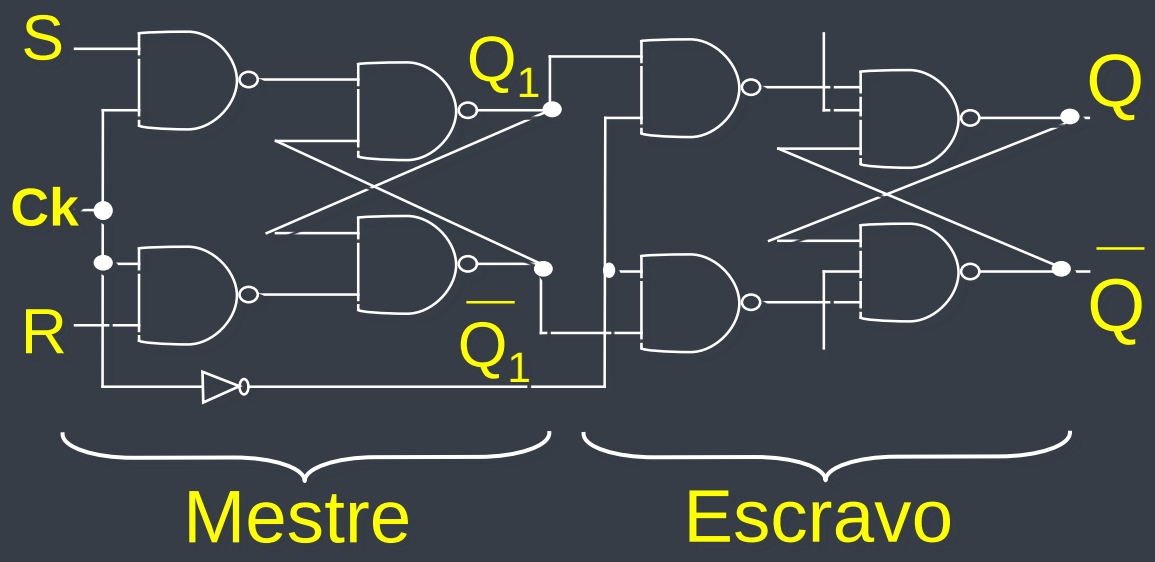




Flip Flop RS Mestre-Escravo



Flip Flop RS Mestre-Escravo

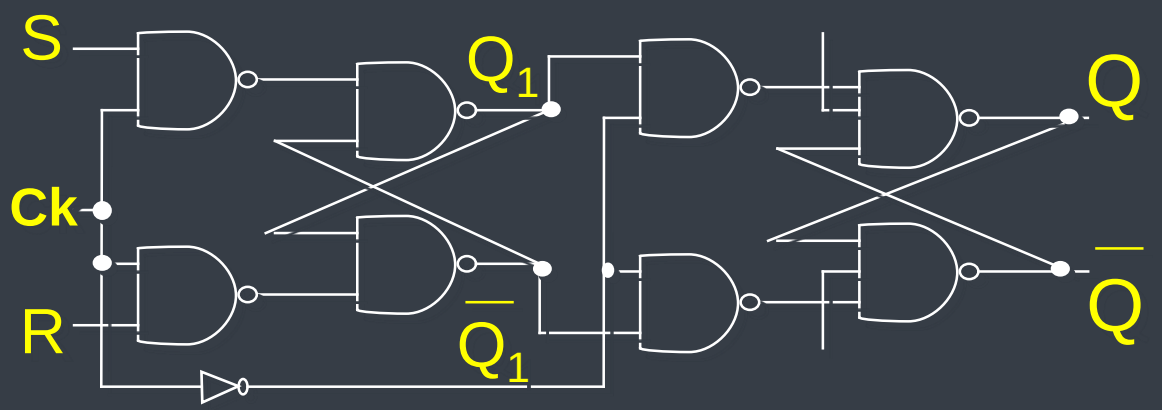


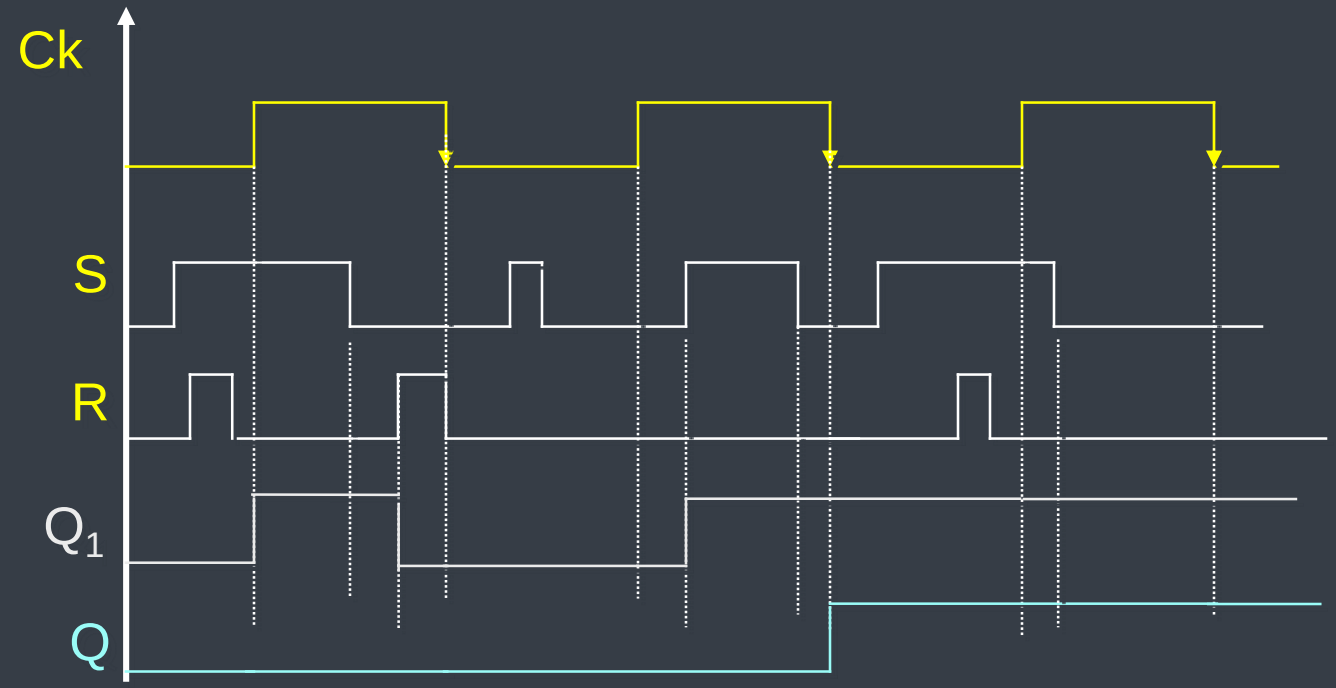
- Ck=1 ➔ Q_1 e $\overline{Q_1}$ respondem às variações de S e R (circuito Mestre habilitado) ➔ entradas do circuito Escravo: desabilitadas ➔ Q e $\overline{Q}$ = ctes)
- Ck=1→0 ➔ Q_1 e $\overline{Q_1}$ passam adiante (circuito Escravo habilitado) e podem afetar Q e $\overline{Q}$ ➔ entradas do circuito Mestre: desabilitadas
- Ck=0 ➔ Q_1 e $\overline{Q_1}$ = ctes ➔ Q e $\overline{Q}$ = ctes

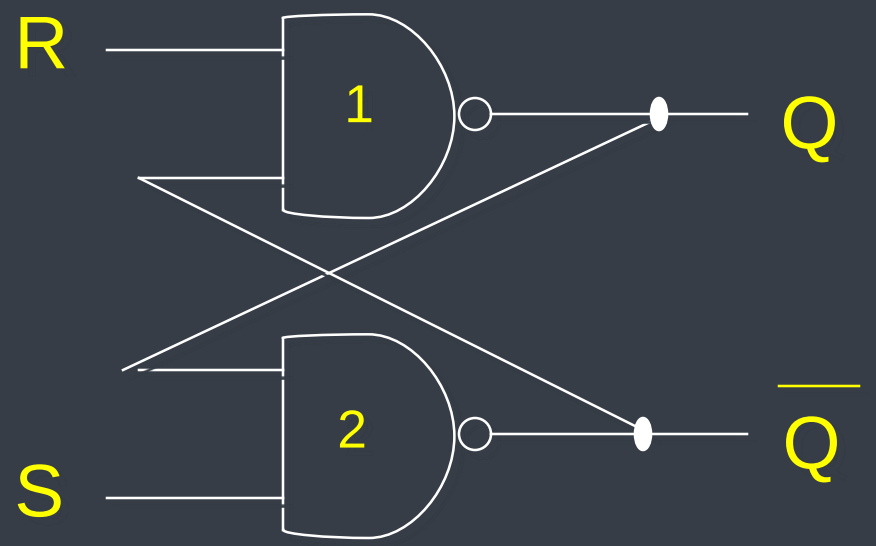
Controle ✓

Estabilidade ?

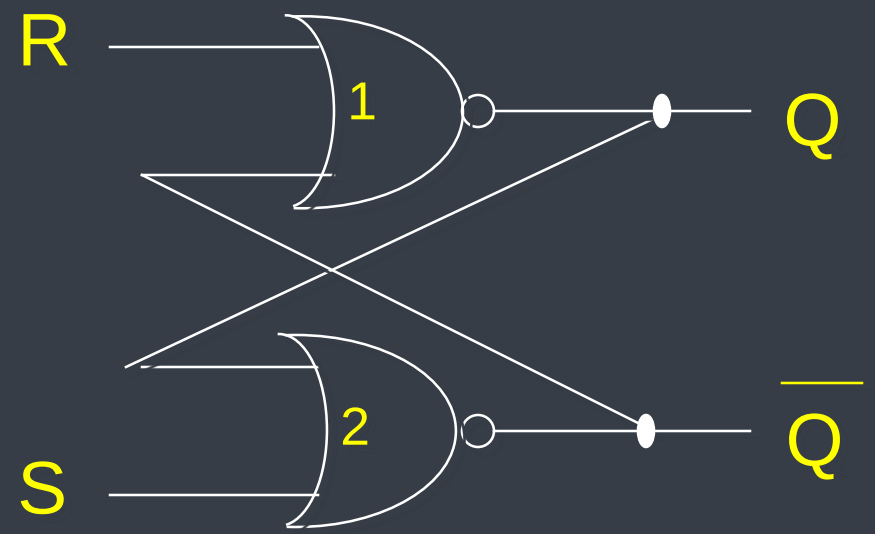
(S=R=1)







R	S	Q
0	0	1 **
0	1	1
1	0	0
1	1	Q_a



R	S	Q
0	0	Q_a
0	1	1
1	0	0
1	1	1 **