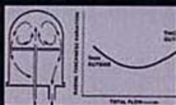
# Handbook of THIN FILM DEPOSITION

## Processes and Technologies

**SECOND EDITION**



Edited by
Krishna Seshan

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Gary E. McGuire, Series Editor
Stephen M. Rossnagel, Series Editor
Rointan F. Bunshah (1927-1999), Founding Editor

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# HANDBOOK OF THIN-FILM DEPOSITION PROCESSES AND TECHNIQUES

## Principles, Methods, Equipment and Applications

## Second Edition

Edited by

**Krishna Seshan**

Intel Corporation
Santa Clara, California

**NOYES PUBLICATIONS**

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*Dedications*

*To the memory of George Narita (1928–2001):*
*kind, patient, wise, nurturing editor, and good friend.*

*To the memory of my beloved parents,*
*Kalpakam and P. K. Seshan.*

# Foreword

## *Gordon E. Moore*

Increasingly any references to the current technology for the manufacture of integrated circuits as "semiconductor technology" is a misnomer. By now the processing relating to the silicon itself contributes relatively few steps to the total while the various processes associated with the deposition and patterning of the increasing number of metal and insulating films have grown in importance. Where the first metal-oxide-transistor circuits of the 1960's took five masking steps to complete, and even early silicon-gate circuits with single metal layer interconnections took only seven, modern circuits with as many as six layers of metal take well in excess of twenty. Not only are there more layers, but the composition of those layers is often complex. Metal conduction layers might require barrier films to prevent inter-diffusion or to enhance adhesion. Insulators not only isolate circuit elements electrically, but are used to prevent ions from harming the electrical properties of the transistors. In fact, if the technology for integrated circuit manufacture as practiced today were named for the majority of the processing steps, the technology could probably be more accurately described as *thin-film technology*.

Consistent with this change, the processing for the deposition and patterning of films has received major research and engineering emphasis and has evolved rapidly over the last few decades. Where in the '60's, thermal oxidation or vapor deposition was sufficient for the insulators and evaporation or sputtering of aluminum took care of the needs for conductors, a large variety of sophisticated deposition techniques have grown with the industry. Today one can control both the electrical and mechanical

properties while achieving uniform and reproducible films from a few atomic layers thick to several micrometers. The chemistry and physics of the films are becoming increasingly better understood, but as they are, the demands of the device designer become more stringent. For example, where the dielectric constant of silicon oxide-based insulators was accepted as a design parameter to live with for thirty years or so, capacitance associated with interconnections now can be a real limitation on circuit performance. Designers want an insulator with all the good properties they have come to love with $SiO_2$, but with a dielectric constant as close to that of a vacuum as possible. Similarly, with conductors no one will be happy until we have room temperature super-conducting films in multi-layered structures.

The simple furnaces and evaporators of yesteryear have become multi-chamber creations of stainless steel that allow a series of processes to be done without exposing the work to air. The lithography machines for creating the desired precise and fine-scaled patterns now cost several million dollars each as the industry pushes the limits of optical systems in the continuing pursuit of performance and small size. The cumulative investment in developing and improving processes must exceed a hundred billion dollars by now. Such a huge investment of money and technical talent has created a vast amount of knowledge, much of which is summarized in this volume.

The film technology developed primarily for the silicon integrated circuit industry is finding its way into several other areas of application. It has become a general technology for designing and constructing complex structures, layer-by-layer. Micro-electromechanical devices (MEMs) use the same deposition and patterning techniques. Micro-fluidic gadgets with micro-sized pipes, valves and all the plumbing necessary to make tiny chemical factories or analytical laboratories are increasingly important, and again use the film technologies that grew up around semiconductor integrated circuits. Even the gene chips the biotech industry uses to speed up their analysis come from the same bag of tricks.

This book takes a snapshot of the state of the art in various technologies relating to thin films. It brings together in one convenient location a collection of the research results that have been gathered by many groups over the last few decades. It will be something that the concerned engineer will return to time after time in the course of his or her work. This is the forefront of science and process engineering with important bearing on many modern industries.

# Preface to the Second Edition

This book is the second edition of the popular book on thin-film deposition by Klaus K. Schuegraf. The previous edition is more than twelve years old. While the fundamentals have not changed, the industry has grown enormously. We've included an introductory chapter, "Recent Changes in the Semiconductor Industry," which describes these changes. In addition, many new manufacturing processes, like chemical mechanical polishing (CMP), have become mature. These are among the many factors that necessitated this new edition.

After the introductory chapter, this second edition starts with the "Introduction and Overview," Ch. 1 from the first edition written by W. Kern and K. Schuegraf. This chapter contains fundamentals that have not changed.

While the methods of growing epitaxial silicon have become much more sophisticated, the fundamentals are still the same and this is reflected by our inclusion of the original chapter on "Silicon Epitaxy by Chemical Vapor Deposition" by M. L. Hammond.

Chapter 3 on "Chemical Vapor Deposition of Silicon Dioxide Films" by J. Foggiato covers some new aspects of atmospheric and low pressure CVD oxide deposition methods.

Chapter 4 on "Metal Organic CVD" by J. L. Zilko has been updated with new material. These four chapters constitute the first part of the book.

A completely new chapter on "Feature Scale Modeling" by V. Singh helps make the transition to physical deposition methods. Modeling of

deposition processes has become mature, improving our ability to define design rules for metal height and spacing to avoid porosity and pinholes that later compromise reliability.

Going hand-in-hand with modeling is our ability to measure both thickness and spacing of submicron dimensions. This has led to the growth of many automatic and sophisticated metrology tools, and the fundamentals behind these instruments is described in the new chapter on the "Role of Metrology and Inspection" by M. Keefer, et al.

New metrology methods are also the backbone of "Contamination Control, Defect Detection and Yield Enhancement" by S. Bhat and K. Seshan, Ch. 7. The understanding of the connection between lithography and contamination has become much more quantitative and this new chapter deals with this subject.

A new chapter on "Sputtering and Sputter Deposition" by S. Rossnagel and three chapters from the first edition bring together all the Physical Vapor Deposition methods. The chapters from the first edition include Ch. 9, "Laser and E-beam Assisted Processing," by C. Moore, et al., Ch. 10 on "Molecular Beam Epitaxy" by W. S. Knodle and R. Chow, and Ch. 11, "Ion Beam Deposition," by J. R. McNeil, et al. These methods remain central to many metal interconnect technologies.

Chapters 12 and 13 are devoted to two entirely new areas. Chapter 12, "Chemical Mechanical Polishing" by K. Cadien, deals with this method of attaining the flatness that is required by modern lithography methods. This technique is so central that several—if not all—layers are polished. Chapter 13, written by K. Seshan, et al., describes new materials that are used for interconnect dielectric materials—specifically organic polyimide materials.

Chapter 14, "Performance, Processing, and Lithography Trends" by K. Seshan, contains a summary of the book and a peek into the future.

The audience for this handbook is the practicing engineer in the microelectronics industry. It will also be useful for engineers in related industries like the magnetic memory, thin film displays, and optical interconnect industries. These industries use many of the same processes, equipment, and analysis techniques. The book could also be used as a supplement to graduate courses in semiconductor manufacturing.

San Jose, California — Krishna Seshan
August, 2001

# Preface to the First Edition

The technology of thin film deposition has advanced dramatically during the past 30 years. This advancement was driven primarily by the need for new products and devices in the electronics and optical industries. The rapid progress in solid-state electronic devices would not have been possible without the development of new thin film deposition processes, improved film characteristics and superior film qualities. Thin film deposition technology is still undergoing rapid changes which will lead to even more complex and advanced electronic devices in the future. The economic impact of this technology can best be characterized by the worldwide sales of semiconductor devices, which exceeded $40 billion in 1987.

This book is intended to serve as a handbook and guide for the practitioner in the field, as a review and overview of this rapidly evolving technology for the engineer and scientist, and as an introduction for the student in several branches of science and engineering.

This handbook is a review of 13 different deposition technologies, each authored by experts in their particular field. It gives a concise reference and description of the processes, methods, and equipment for the deposition of technologically important materials. Emphasis is placed on recently developed film deposition processes for application in advanced microelectronic device fabrications that require the most demanding approaches. The discussions of the principles of operation for the deposition equipment and its suitability, performance, controls, capabilities and limitations for production applications are intended to provide the

reader with basic understanding and appreciation of these systems. Key properties and areas of application of industrially important materials created by thin film deposition processes are described. Extensive use of references, reviews and bibliographies provides source material for specific use and more detailed study.

The topics covered in each chapter of this book have been carefully selected to include advanced and emerging deposition technologies with potential for manufacturing applications. An attempt was made to compare competing technologies and to project a scenario for the most likely future developments. Several other deposition technologies have been excluded since adequate recent reviews are already available. In addition, the technology for deposition or coating of films exceeding 10 microns in thickness was excluded, since these films have different applications and are in general based on quite different deposition techniques.

Many people contributed and assisted in the preparation of this handbook. My thanks go to the individual authors and their employers, who provided detailed work and support. I am especially indebted to Werner Kern, who provided many valuable suggestions and assisted in co-authoring several sections of this book. Last but not least, my special thanks go to George Narita, Executive Editor of Noyes Publications, for providing continued encouragement and patience for the completion of all the tasks involved.

Torrance, California — Klaus K. Schuegraf
July, 1988

# Contributors

**Suresh Bhat**
Intel Corporation,
Santa Clara, CA

**Kenneth C. Cadien**
Intel Corporation
Hillsboro, OR

**Robert Chow**
Thin Film Division
Varian Associates
Santa Clara, CA

**George J. Collins**
Department of Electrical Engineering
Colorado State University
Fort Collins, CO

**Cheri Dennison**
KLA-Tencor Corporation
Milpitas, CA

**John Foggiato**
Quester Technology, Inc.
Fremont, CA

**Martin L. Hammond**
Tetron/Gemini Systems
Fremont, CA

**Mark Keefer**
KLA-Tencor Corporation
Milpitas, CA

**Werner Kern**
David Sarnoff Research Center
RCA Laboratories
Princeton, NJ

**Walter S. Knodle**
High Yield Technology, Inc.
Mountain View, CA

**James J. McNally**
Air Force Academy
Colorado Springs, CO

**John R. McNeil**
Department of Electrical Engineering
University of New Mexico
Albuquerque, NM

**Cameron A. Moore**
Department of Electrical Engineering
Colorado State University
Fort Collins, CO

**Rebecca Pinto**
KLA-Tencor Corporation
Milpitas, CA

**Paul D. Reader**
Ion Tech, Inc.
Fort Collins, CO

**Stephen Rossnagel**
IBM Research Division
Yorktown Heights, NY

**Laura B. Rothman**
IBM
Yorktown Heights, NY

**Dominic J. Schepis**
IBM
East Fishkill, NY

**Klaus K. Schuegraf**
Tylan Corporation
Carson, CA

**Krishna Seshan**
Intel Corporation
Santa Clara, CA

**Vivek Singh**
Intel Corporation
Hillsboro, OR

**Lance R. Thompson**
Sandia National Labs
Albuquerque, NM

**James Turlo**
KLA-Tencor Corporation
Milpitas, CA

**Zeng-qi Yu**
Colorado State University
Fort Collins, CO

**John L. Zilko**
Optoelectrics Division
Agere Systems
Breinigsville, PA

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# Recent Changes in the Semiconductor Industry

*Krishna Seshan*

The size, importance, and the economic impact of the semiconductor industry have undergone a sea change in recent years. The role of equipment has been the fuel for this change. New processing steps have become necessary, old ones have become cleaner, greener and more sophisticated. Everything has become much cleaner and more expensive; it is common for pieces of equipment to cost multiple millions of dollars. The result is a new manufacturing environment for the industry.

## 1.0 COST OF DEVICE FABRICATION

Graphs and tables in this section quantify that semiconductor fabricators generate large revenues, but their manufacturing costs have also become very large. This increase in equipment cost is driven by the need for very clean fabricators and processing steps. The connections between feature size, contamination control, and cost are discussed below.

The graph in Fig. 1 shows a breakdown of the cost of device fabrication into equipment and land/building costs. It is clear that the equipment component of cost is now the major contributor. Notice the increase as the industry moves to 12" wafers.

The growth of the semiconductor industry and the sales of processing equipment are related as shown in Fig. 2.

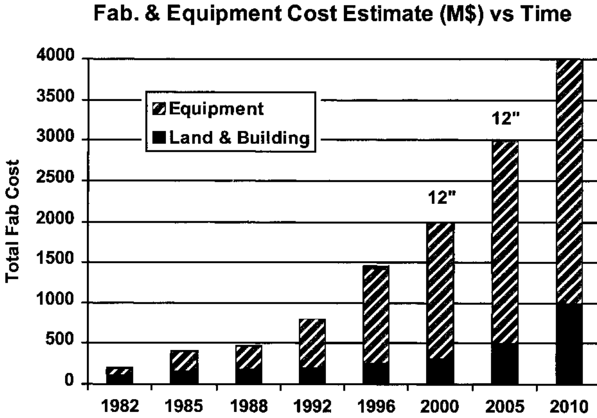


**Figure 1.** Equipment component of total fabrication costs is increasing much faster than land and buildings. *(Source: Dataquest Report 2000.)*

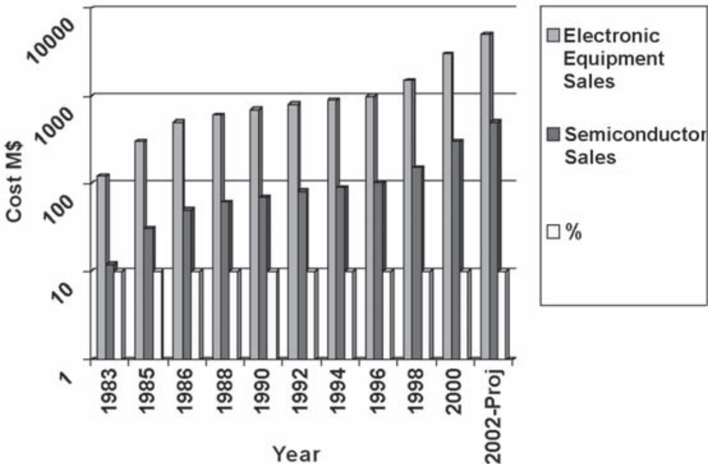


**Figure 2.** Electronic equipment sales, semiconductor sales value, and yearly fluctuations. *(Data adapted from "Worldwide IC Industry Economic Update and Forecast.")*

The graphs above make the following three points:

- Costs of device fabrication have increased. The cost of a 12" fab is in the billions of dollars.
- The value of the semiconductor products manufactured, memory and mircroprocessors, is measured in the billions of dollars.
- A large fraction of the fabricator's cost is the cost of manufacturing equipment. This book is a detailed account of the processes performed by the equipment.

## 1.1 Role of Cleanliness in Cost of Equipment

By far the biggest change has been our understanding of the role of defects and particle sizes as the lithography moves into the nanometer regime. Table 1 shows industry estimates of defect densities that can be tolerated. It is implied that the defects at or smaller than the litho size can be fatal, causing yield loss.

The table also shows how the mask layers increase and the number of defects per unit area have to decrease. This table emphasizes the importance of cleanliness in semiconductor processing. It is for this reason that a new chapter on contamination and contamination control (Ch. 7) has been added to this edition.

**Table 1.** Projected Increase in Mask Layers and Decrease in Allowable Defects

| Year | 1999 | 2001 | 2003 | 2006 | 2009 |
|---|---|---|---|---|---|
| Technology Generation (nm) | 180 | 150 | 130 | 100 | 70 |
| Mask Count | 22 | 24 | 24 | 26 | 28 |
| Allowable Defect per sq. meter to get 60% yield | 78 | 60 | 55 | 43 | 34 |

## 1.2 Role of Chip Size Trends, Larger Fabricators, and 12" Wafers

The importance of clean fabrication facilities and equipment becomes all the more pertinent when we consider that chip sizes with increased functionality increase with time and with decreasing lithography feature size. This is shown in the graph below (Fig. 3).

As chip size increases, so does the need for more wafer starts. One direction the industry has to go is to move the fabricators to larger size wafers.

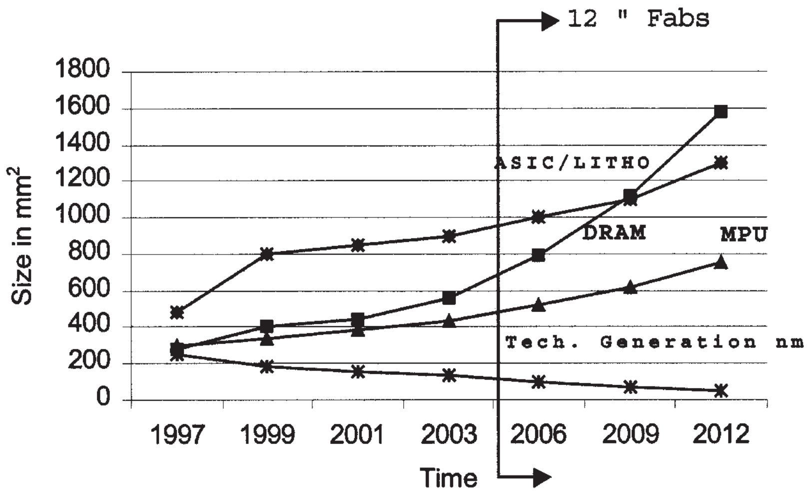


**Figure 3.** Plot of chip size in mm$^2$ vs. lithographic generation. These are best guess estimates. The point to note is that die that can be expected fill the litho field size (800 mm × 800 mm).

## 1.3 Lithography, Feature Size, and Cleaner Fabricators and Equipment

There are two connected variables that one needs to understand. The number of critical mask layers increase; a critical layer is one where high degree of registration and small widths are required. In these layers, defects at the resolution limit can become critical. An example is metal debris shorting two metal lines. The graph in Fig. 4 shows the dimensions that are involved.

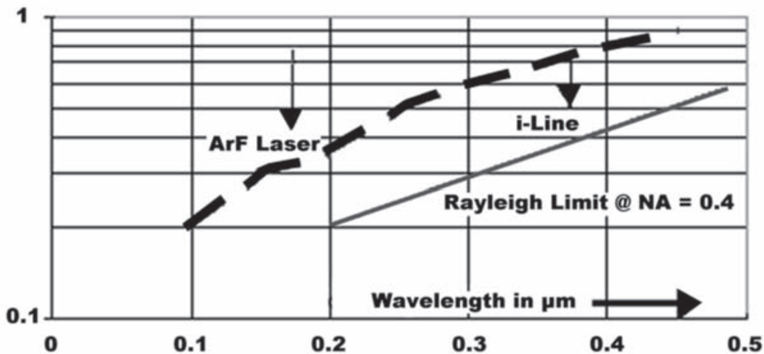


**Figure 4.** This graph of printable line width estimate vs litho wavelength shows that particles as small as 250 nm could become critical defects. As line width decreases, more layers become critical, and cleaner the tool and the fabricators have to become.

## 1.4 Defect Density and the Need for Cleaner Fabricators

There are two complications with defect density. First, the mask count is increasing and the number of critical layers is increasing. Mask layers are expected to increase from 20 mask layer levels to 30. Secondly, the line size is decreasing—so smaller defects become killer defects. The net result is that both fabricators and equipment has to become cleaner. One way to measure this is to track what the critical defect density, $D_0$ (defects/m$^2$), needs to be to get 60% yield as shown in Table 2. These numbers are based on predicted chip size areas and are shown here in order to explain the trend. These are not exact numbers.

The need for decreased feature sizes and the increase in the number of critical masking layers drive cleaner fabricators. It is instructive to examine the plot of cumulative yield vs the critical defect concentration as shown in Fig. 5. This graph shows that a defect density of 0.5/cm$^2$ will reduce the yield by about 1%. It is evident from the graph that both fabricators and equipment will have to meet stringent cleanliness standards, at least Class 10 or better. Class 10 clean rooms are expensive to build—with estimates of thousands of dollars per sq. foot.

Cleanroom Class designations generally refer to the Federally agreed-upon standards set forth in FED STD 209B which is shown in part in Table 3.[1]

**Table 2.** Estimates of $D_o$, the Critical Defect Density Required

| | 1999 | 2001 | 2003 | 2006 |
|---|---|---|---|---|
| Generation | 250 | 180 | 150 | 130 |
| DRAM $D_0$ for 60% yield | 1400 | 1000 | 850 | 700 |
| Logic $D_0$ for 60% yield | 1400 | 1200 | 1000 | 900 |

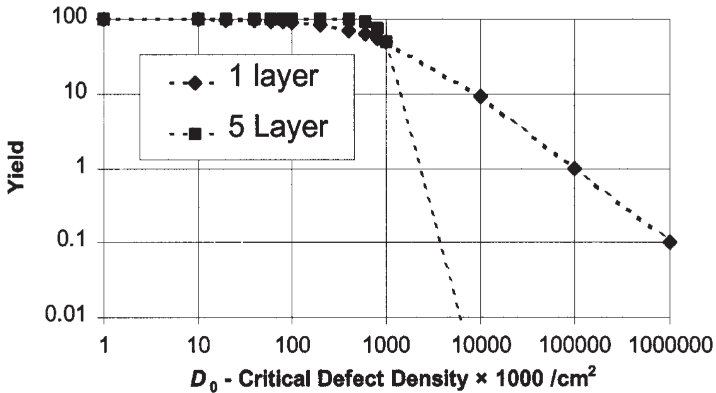


**Figure 5.** The yield equation is plotted for a one and a five critical-layer process. Notice that to get 60% yeild, the equipment and fabricators have to be better than a defect level of 0.01–0.03 defects/cm$^2$.

**Table 3.** Specifications From FED STD 209B

| Class | Particles/liter 0.5 µm and larger | Particles 5 µm and larger |
|---|---|---|
| 100 | 3.5 | |
| 1000 | 35 | |
| 10,000 | 350 | 65 |
| 100,000 | 3500 | 700 |

### 1.5 Conclusions

The preceding brief discussion and data shows the following:

- Improved lithography decreases feature size.
- The number of mask layers increase because of higher integration of chip design.
- These combine to call for smaller defects and cleaner processing conditions.
- Equipment then has to become more sophisticated, cleaner, and more expensive.

## 2.0 TECHNOLOGY TRENDS, CHIP SIZE, PERFORMANCE, AND MOORE'S LAW

The semiconductor industry follows a predictable trend—one where the transistor density doubles every generation, in about 3-year cycles. This has come to be known as Moore's Law. In the section below, these trends are examined in detail

In order to simplify and unify the growth predictions of the industry, the SIA (Semiconductor Industry Association) publishes a roadmap, the SIA Industry Roadmap. The numbers shown in Table 4 are drawn from that report.[1]

**Table 4.** SIA Industry Roadmap[1]

| Year of Shipment | 1997 | 1999 | 2001 | 2003 | 2006 | 2009 | 2012 |
|---|---|---|---|---|---|---|---|
| DRAM Half Pitch(nm) | 250 | 180 | 150 | 130 | 100 | 70 | 50 |
| Memory (sample) | 256M | 1G | | 4G | 16G | 64G | 256G |
| Memory (ship) | 64M | 256M | 1G | 1G | 4G | 16G | 64G |
| Bits/cm$^2$ at sample | 96M | 270M | 380M | 770M | 2.2B | 6.1B | 17B |
| Logic Txtor/cm$^2$ | 3.7M | 6.2M | 10M | 18M | 39M | 84M | 180M |

DRAM devices are historically viewed as technology drivers. Now microprocessors have closed the technology gap. DRAM focus is on minimization of area occupied by memory cells. To increase cell density the cell size must be as small as possible. In microprocessors, performance is dominated by the length of the transistor gate and by the number of interconnect layers.

## 2.1 Performance of Packaged Chips—Trends

Performance increase follows the decrease in cell size: the transistor drives increase and switching times decrease because the charge being switched decreases. This enables larger chips to be designed and more functionality to be integrated. These trends may be seen in the Fig. 6

An empirical observation made by Gordon Moore can be seen in Fig. 7. Often chip size, or the number of transistors, or the density is plotted. All three graphs show the same trend: one that says that density doubles every generation or about three years.

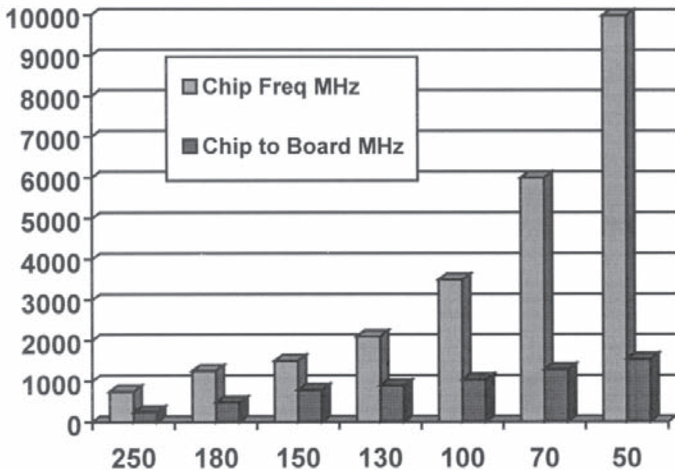


**Figure 6.** As cell sizes decrease, the chip frequencies increase.

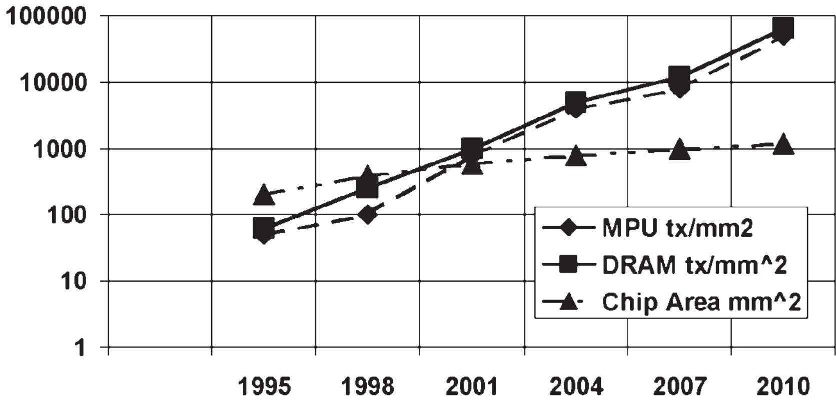


**Figure 7.** Projected growth of DRAMs and MPUs. The chip sizes are also plotted. Microporcessor density tends to be lower than DRAM density because logic circuits cannot be drawn as tightly as memory.

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# 1

# Deposition Technologies and Applications: Introduction and Overview

*Werner Kern and Klaus K. Schuegraf*

## 1.0 OBJECTIVE AND SCOPE OF THIS BOOK

The aim of this book is to provide a concise reference and description of the processes, methods, and equipment for depositing technologically important materials. Emphasis is placed on the most recently developed processes and techniques of film deposition for applications in high technology, in particular, advanced microelectronic device fabrication that requires the most sophisticated and demanding approaches. The volume is intended to serve as a handbook and guide for the practitioner in the field, as a review and overview of this rapidly evolving technology for the engineer and scientist, and as an introduction to the student in several branches of science and engineering.

The discussions of the principles of operation of deposition equipment and its suitability, performance, control, capabilities, and limitations for production applications are intended to provide the reader with a basic understanding and appreciation of these systems. Key properties and areas of application of industrially important materials created by thin-film deposition processes are described. Extensive use of references, reviews, and bibliographies is made to provide source material for specific use and more detailed study.

The chapter topics have been carefully selected to include primarily advanced and emerging deposition technologies in this rapidly evolving field. Many other important deposition technologies have not been included if adequate recent reviews are already available, or if the technologies are primarily intended for forming thick films or coatings that generally exceed a thickness of about ten micrometers, but the importance of these technologies is nevertheless recognized. Finally, an attempt has been made to compare competing technologies and to project a scenario for the most likely developments in the future.

## 2.0 IMPORTANCE OF DEPOSITION TECHNOLOGY IN MODERN FABRICATION PROCESSES

Deposition technology can well be regarded as the major key to the creation of devices such as computers, since microelectronic solid-state devices are all based on material structures created by thin-film deposition. Electronic engineers have continuously demanded films of improved quality and sophistication for solid-state devices, requiring a rapid evolution of deposition technology. Equipment manufacturers have made successful efforts to meet the requirements for improved and more economical deposition systems and for in situ process monitors and controls for measuring film parameters. Another important reason for the rapid growth of deposition technology is the improved understanding of the physics and chemistry of films, surfaces, interfaces, and microstructures made possible by the remarkable advances in analytical instrumentation during the past twenty years. A better fundamental understanding of materials leads to expanded applications and new designs of devices that incorporate these materials.

A good example of the crucial importance of deposition technology is the fabrication of semiconductor devices, an industry that is totally dependent on the formation of thin solid films of a variety of materials by deposition from the gas, vapor, liquid, or solid phase. The starting materials, epitaxial films of semiconductors, are usually grown from the gas phase. Chemical vapor deposition of a single-crystal silicon film on a single-crystal silicon substrate of the same crystallographic orientation, a process known as *homoepitaxy*, is accomplished by hydrogen reduction of dichlorosilane vapor. If a single-crystal film of silicon is deposited on a non-silicon crystal substrate, the process is termed *heteroepitaxy*. Layers of single-crystal compound semiconductors are created to a thickness of a few atom layers by molecular beam epitaxy.

Subsequent steps in the fabrication process create electrical structures that require the deposition of an insulating or dielectric layer, such as an oxide, glass, or nitride, by one of several types of chemical vapor deposition (CVD) processes, by plasma-enhanced chemical vapor deposition (PECVD), or by any one of a number of sputtering deposition methods. The deposition of conductor films for contact formation and interconnections can be accomplished by vacuum evaporation or sputtering. CVD processes are especially suitable if polysilicon, polycides, or refractory metals are to be deposited.

The deposition of subsequent levels of insulator is repeated to build multilevel structures. Deposition may be complemented by spin-on techniques of organic polymeric materials, such as a polyimide, or of organometallic-based glass-forming solutions. Spin-on deposition is especially useful if planarization of the device topography is required, as in the case of most high-density, multilevel conductor, VLSI circuits. The sequence of alternate film deposition of metals and insulators may be repeated several more times, with repetitive spin-on deposition of photopolymer masking solution for the delineation of contact openings, grid lines, and other pattern features by etching operations and lift-off techniques. Film formation by methods other than deposition are used in a few steps of the fabrication sequence; these include thermal oxidation of the substrate, ion implantation, nitridation, silicide formation, electrolytic and electroless metal deposition, and spray deposition (e.g., of organometallic solutions for forming antireflection coatings). These examples attest to the fact that the vast majority of material formation processes in semiconductor device technology (and in other areas of electronic device fabrication) are crucially dependent on film deposition technology.

## 3.0 CLASSIFICATION OF DEPOSITION TECHNOLOGIES

There are many dozens of deposition technologies for material formation.[1]–[4] Since the concern here is with thin-film deposition methods for forming layers in the thickness range of a few nanometers to about ten micrometers, the task of classifying the technologies is made simpler by limiting the number of technologies to be considered.

Basically, thin-film deposition technologies are either purely physical, such as evaporative methods, or purely chemical, such as gas- and liquid-phase chemical processes. A considerable number of processes that are based on glow discharges and reactive sputtering combine both physical and chemical reactions; these overlapping processes can be categorized as physical-chemical methods.

A classification scheme is presented in Table 1 where we have grouped thin-film deposition technologies according to evaporative glow-discharge, gas-phase chemical, and liquid-phase chemical processes. The respective pertinent chapter numbers in this book have also been indicated. Certain film formation processes such as oxidation, which, strictly speaking, are not deposition processes, have been included because of their great importance in solid-state technology.

## 4.0 OVERVIEW OF VARIOUS THIN-FILM DEPOSITION TECHNOLOGIES

The following is a brief description of the principles, salient features, applications, and selected literature references of the more important technologies for thin-film deposition and formation categorized in Table 1. Technologies that are not covered in the chapters of this book have also been included in this discussion to present a more comprehensive overview of the entire field.

### 4.1 Evaporative Technologies

Although one of the oldest techniques used for depositing thin films, thermal evaporation or vacuum evaporation,[5]–[7] is still widely used in the laboratory and in industry for depositing metal and metal alloys. The following sequential basic steps take place: (*i*) a vapor is generated by boiling or subliming a source material, (*ii*) the vapor is transported from the source to the substrate, and (*iii*) the vapor is condensed to a solid film on the

**Table 1.** Survey and Classification of Thin-Film Depositon Technologies

| | |
|---|---|
| EVAPORATIVE METHODS | |
| • ***Vacuum Evaporation*** | |
| Conventional vacuum evaporation | Molecular-beam epitaxy (MBE) |
| Electron-beam evaporation | Reactive evaporation |
| GLOW-DISCHARGE PROCESSES | |
| • ***Sputtering*** | • ***Plasma Processes*** |
| Diode sputtering | Plasma-enhanced CVD |
| Reactive sputtering | Plasma oxidation |
| Bias sputtering (ion plating) | Plasma anodization |
| Magnetron sputtering | Plasma polymerization |
| Ion beam deposition | Plasma nitridation |
| Ion beam sputter deposition | Plasma reduction |
| Reactive ion plating | Microwave ECR plasma CVD |
| Cluster beam deposition (CBD) | Cathodic arc deposition |
| GAS-PHASE CHEMICAL PROCESSES | |
| • ***Chemical Vapor Deposition (CVD)*** | • ***Thermal Forming Processes*** |
| CVD epitaxy | Thermal oxidation |
| Atmospheric-pressure CVD (APCVD) | Thermal nitridation |
| Low-pressure CVD (LPCVD) | Thermal polymerization |
| Metalorgainc CVD (MOCVD) | |
| Photo-enhanced CVD (PHCVD) | |
| Laser-induced CVD (PCVD) | |
| Electron-enhanced CVD | Ion implantation |
| LIQUID-PHASE CHEMICAL TECHNIQUES | |
| • ***Electro Processes*** | • ***Mechanical Techniques*** |
| Electroplating | Spary pyrolysis |
| Electroless plating | Spray-on techniques |
| Electrolytic anodization | Spin-on techniques |
| Chemical reduction plating | |
| Chemical displacement plating | |
| Electrophoretic deposition | Liquid phase epitaxy |

substrate surface. Although deceptively simple in principle, the skilled practitioner must be well versed in vacuum physics, material science, mechanical and electrical engineering, as well as in elements of thermodynamics, kinetic theory of gases, surface mobility, and condensation phenomena.

Evaporants cover an extraordinary range of varying chemical reactivity and vapor pressures. This variety leads to a large diversity of source components including resistance-heated filaments, electron beams; crucibles heated by conduction, radiation, or rf-induction; arcs, exploding wires, and lasers. Additional complications include source-container interactions, requirements for high vacuum, precise substrate motion (to ensure uniformity) and the need for process monitoring and control.

**Molecular Beam Epitaxy.** MBE[8]–[16] is a sophisticated, finely controlled method for growing single-crystal epitaxial films in a high vacuum ($10^{-11}$ torr). The films are formed on single-crystal substrates by slowly evaporating the elemental or molecular constituents of the film from separate Knudsen effusion source cells (deep crucibles in furnaces with cooled shrouds) onto substrates held at a temperature appropriate for chemical reaction, epitaxy, and re-evaporation of excess reactants. The furnaces produce atomic or molecular beams of relatively small diameter, which are directed at the heated substrate, usually silicon or gallium arsenide. Fast shutters are interposed between the sources and the substrates. By controlling these shutters, one can grow superlattices with precisely controlled uniformity, lattice match, composition, dopant concentrations, thicknesses, and interfaces down to the level of atomic layers.

The most widely studied materials are epitaxial layers of III-V semiconductor compounds, but silicon, metals, silicides, and insulators can also be deposited as single-crystal films by this versatile and uniquely precise method. Complex layer structures and superlattices for fabricating gallium arsenide heterojunction solid-state lasers, discrete microwave devices, optoelectronic devices, waveguides, monolithic integrated optic circuits, and totally new devices, have been created. An additional important advantage of MBE is the low temperature requirement for epitaxy, which for silicon is in the range of 400°C to 800°C,[15] and for gallium arsenide, 500°C to 600°C.[9] Several production systems with associated analytic equipment are now available.[16] The extremely limited product throughput, the complex operation, and the expensive equipment are, at present, the major limitations of this promising deposition technology for production applications.

## 4.2 Glow-Discharge Technologies

The electrode and gas-phase phenomena in various kinds of glow discharges (especially rf discharges) represent a rich source of processes used to deposit and etch thin films. Creative exploitation of these phenomena has resulted in the development of many useful processes for film deposition (as well as etching), as listed in Table 1.

**Sputtering.** The most basic and well-known of these processes is sputtering,[17]–[25] the ejection of surface atoms from an electrode surface by momentum transfer from bombarding ions to surface atoms. From this definition, sputtering is clearly an etching process, and is, in fact, used as such for surface cleaning and for pattern delineation. Since sputtering produces a vapor of electrode material, it is also (and more frequently) used as a method of film deposition similar to evaporative deposition. *Sputter deposition* has become a generic name for a variety of processes.

***Diode Sputtering*.** Diode sputtering uses a plate of the material to be deposited as the cathode (or rf-powered) electrode (target) in a glow discharge. Material can thus be transported from the target to a substrate to form a film. Films of pure metals or alloys can be deposited when using noble gas discharges (typically Ar) with metal targets.

***Reactive Sputtering*.** Compounds can be synthesized by reactive sputtering, that is, sputtering elemental or alloy targets in reactive gases; alternatively, they can be deposited directly from compound targets.

***Bias Sputtering*.** Bias sputtering or ion-plating[25] is a variant of diode sputtering in which the substrates are ion bombarded during deposition and prior to film deposition to clean them. Ion bombardment during film deposition can produce one or more desirable effects, such as re-sputtering of loosely-bonded film material, low-energy ion implantation, desorption of gases, conformal coverage of contoured surface, or modification of a large number of film properties. The source material need not originate from a sputtering target, but can be an evaporation source, a reactive gas with condensable constituents, or a mixture of reactive gases with condensable constituents and other gases that react with the condensed constituents to form compounds.

It should be noted that all glow discharge processes involve sputtering in one form or another, since it is impossible to sustain a glow discharge without an electrode at which these processes occur. In "electrodeless" discharges, rf power is capacitively coupled through the insulating wall of a tubular reactor. In this case, the inside wall of the tube

is the main electrode of the discharge. However, sputtering can also lead to undesirable artifacts in this and other glow-discharge processes.

***Magnetron Sputtering.*** Another variant in sputtering sources uses magnetic fields transverse to the electric fields at sputtering-target surfaces. This class of processes is known as *magnetron sputtering*.[20]–[22] Sputtering with a transverse magnetic field produces several important modifications of the basic processes. Target-generated secondary electrons do not bombard substrates because they are trapped in cycloidal trajectories near the target, and thus do not contribute to increased substrate temperature and radiation damage. This allows the use of substrates that are temperature-sensitive (for example, plastic materials) and surface-sensitive (for example, metal-oxides-semiconductor devices) with minimal adverse effects. In addition, this class of sputtering sources produces higher deposition rates than conventional sources and lends itself to economic, large-area industrial application. There are cylindrical, conical, and planar magnetron sources, all with particular advantages and disadvantages for specific applications. As with other forms of sputtering, magnetron sources can be used in a reactive sputtering mode. Alternatively, one can forego the low-temperature and low radiation-damage features and utilize magnetron sources as high-rate sources by operating them in a bias-sputtering mode.

***Ion-Beam Sputtering.*** Ion beams, produced in and extracted from glow discharges in a differentially pumped system, are important to scientific investigations of sputtering, and are proving to be useful as practical film-deposition systems for special materials on relatively small substrate areas. There are several advantages of ion-beam sputtering deposition.[23] The target and substrate are situated in a high-vacuum environment rather than in a high-pressure glow discharge. Glow discharge artifacts are thereby avoided, and higher-purity films usually result. Reactive sputtering and bias sputtering with a separate ion gun can be used.

**Plasma Processes.** The fact that some chemical reactions are accelerated at a given temperature in the presence of energetic reactive-ion bombardment is the basis of processes for surface treatments such as plasma oxidation, plasma nitriding, and plasma carburizing.[26]–[28] A metal to be oxidized, nitrided or carburized is made the cathode of a glow discharge and is simultaneously heated by radiant or rf-induction means. The discharge gas is either $O_2$, $N_2$ plus $H_2$, or $CH_4$. Very thick (0.1–2 mm)

protective coatings on a variety of metals can be produced in this way to render surfaces hard and/or corrosion resistant.

***Anodization.*** Plasma anodization[26][28][29] is a technique for producing thin oxide films (less than 100 nm) on metals such as aluminum, tantalum, titanium, and zirconium, collectively referred as *valve metals.* In this case, a dc discharge is set up in an oxygen atmosphere and the substrates (shielded from the cathode to avoid sputter deposition) are biased positively with respect to the anode. This bias extracts negative oxygen ions from the discharge to the surface, which is also bombarded with electrons that assist the reaction. The process produces very dense, defect-free, amorphous oxide films that are of interest as gate material in III-V compound semiconductor devices such as in microwave field-effect transistors.

***Deposition of Inorganic/Organic Films.*** Plasma deposition of inorganic films[27][29]–[37] and plasma polymerization of organic reactants to produce films of organic polymers[38] involve the introduction of a volatile reactant into a glow discharge which is usually generated by an rf force. The reactant gases or vapors are decomposed by the glow discharge mainly at surfaces (substrate, electrodes, walls), leaving the desired reaction product as a thin solid film. Plasma deposition is a combination of a glow-discharge process and low-pressure chemical vapor deposition, and can be classified in either category. Since the plasma assists or enhances the chemical vapor deposition reaction, the process is usually denoted as PACVD or PECVD. The possibilities for producing films of various materials and for tailoring their properties by judicious manipulation of reactant gases or vapors and glow-discharge parameters are very extensive. Plasma deposition processes are used widely to produce films at lower substrate temperatures and in more energy-efficient fashion than can be produced by other techniques. For example, they are widely used to form secondary-passivation films of plasma silicon nitride on semiconductor devices, and to deposit hydrogenated, amorphous silicon layers for thin-film solar cells.

***Microwave Electron Cyclotron Resonance Deposition.*** ECR plasma deposition[39][40] employs an electron cyclotron resonance (ECR) ion source to create a high-density plasma. The plasma is generated by resonance of microwaves and electrons through a microwave discharge across a magnetic field. The main feature of this recently introduced process is the high rate of deposition obtained at a low temperature of deposition.

**Cluster Beam Deposition.** Ionized cluster beam deposition (ICB) or cluster beam deposition[41]–[45] is one of the most recent emerging technologies for the deposition of thin films with growth-control capabilities not attainable by other processes. ICB deposition is one of several techniques classified as ion-assisted thin-film formation. The material to be deposited emerges and expands into a vacuum environment from a small nozzle of a heated confinement crucible, usually constructed of high-purity graphite. The vapor pressure within the crucible is several orders of magnitude higher than the pressure of the vacuum chamber so that the expanding vapor supercools. Homogeneous nucleation results in the generation of atomic aggregates or clusters of up to a few thousand atoms held together by weak interatomic forces. The clusters passing through the vacuum towards the substrate can, in part, be positively charged by impact ionization with electron beam irradiation. Closely controlled accelerating voltages add energy to the ionized clusters which then impinge on the substrate, diffuse or migrate along the plane of the surface, and finally form a thin film of exceptional purity. The complete and detailed process is extremely complex but offers unprecedented possibilities of film formation once the fundamentals and engineering technology are fully understood and exploited. Plasma deposition (and plasma etching) processes represent cases in which technology is leading science. The detailed interactions of plasma chemistry, plasma physics, and possible synergistic effects are still largely unexplained. In view of the technological importance of these processes, much more research and process modeling is required to obtain an adequate understanding of these deposition mechanisms.

## 4.3 Gas-Phase Chemical Processes

Methods of film formation by purely chemical processes in the gas or vapor phases include chemical vapor deposition and thermal oxidation. Chemical vapor deposition (CVD)[26][33[46]–[55] is a materials synthesis process whereby constituents of the vapor phase react chemically near or on a substrate surface to form a solid product. The deposition technology has become one of the most important means for creating thin films and coatings of a very large variety of materials essential to advanced technology, particularly solid-state electronics where some of the most sophisticated purity and composition requirements must be met. The main feature of CVD is its versatility for synthesizing both simple and complex compounds with relative ease at generally low temperatures. Both chemical

composition and physical structure can be tailored by control of the reaction chemistry and deposition conditions. Fundamental principles of CVD encompass an interdisciplinary range of gas-phase reaction chemistry, thermodynamics, kinetics, transport mechanisms, film growth phenomena, and reactor engineering.

Chemical reaction types basic to CVD include pyrolysis (thermal decomposition), oxidation, reduction, hydrolysis, nitride and carbide formation, synthesis reactions, disproportionation, and chemical transport. A sequence of several reaction types may be involved in more complex situations to create a particular end product. Deposition variables such as temperature, pressure, input concentrations, gas flow rates and reactor geometry and operating principle determine the deposition rate and the properties of the film deposit. Most CVD processes are chosen to be heterogeneous reactions. That is, they take place at the substrate surface rather than in the gas phase. Undesirable homogeneous reactions in the gas phase nucleate particles that may form powdery deposits and lead to particle contamination instead of clean and uniform coatings. The reaction feasibility (other than reaction rate) of a CVD process under specified conditions can be predicted by thermodynamic calculations, provided reliable thermodynamic data (especially the free energy of formation) are available. Kinetics control the rate of reactions and depend on temperature and factors such as substrate orientation. Considerations relating to heat, mass, and momentum transport phenomena are especially important in designing CVD reactors of maximum efficiency. Since important physical properties of a given film material are critically influenced by the structure (such as crystallinity), control of the factors governing the nucleation and structure of a growing film is necessary.

Thin-film materials that can be prepared by CVD cover a tremendous range of elements and compounds. Inorganic, organometallic, and organic reactants are used as starting materials. Gases are preferred because they can be readily metered and distributed to the reactor. Liquid and solid reactants must be vaporized without decomposition at suitable temperatures and transported with a carrier gas through heated tubes to the reaction chamber, which complicates processing, especially in the case of reduced-pressure systems. Materials deposited at low temperatures (e.g., below 600°C for silicon) are generally amorphous. Higher temperatures tend to lead to polycrystalline phases. Very high temperatures (typically 900°C to 1100°C in the case of silicon) are necessary for growing single-crystal films. These films are oriented according to the structure of the

substrate crystal; this phenomenon, known as *epitaxy*, is of crucial practical importance in solid-state device technology.

CVD has become an important process technology in several industrial fields. As noted, applications in solid-state microelectronics are of prime importance. Thin CVD films of insulators, dielectrics (oxides, silicates, nitrides), elemental and compound semiconductors (silicon, gallium arsenide, etc.), and conductors (tungsten, molybdenum, aluminum, refractory metal silicides) are extensively utilized in the fabrication of solid-state devices. Hard and wear-resistant coatings of materials such as boron, diamond-like carbon, borides, carbides and nitrides have found important applications in tool technology. Corrosion resistant coatings, especially oxides and nitrides, are used for metal protection in metallurgical applications. Numerous other types of materials, including vitreous graphite and refractory metals, have been deposited mainly in bulk form or as thick coatings. Many of these CVD reactions have long been used for coating of substrates at reduced pressure, often at high temperatures.

**Reactors.** The reactor system (comprising the reaction chamber and all associated equipment) for carrying out CVD processes must provide several basic functions common to all types of systems. It must allow transport of the reactant and diluent gases to the reaction site, provide activation energy to the reactants (heat, radiation, plasma), maintain a specific system pressure and temperature, allow the chemical processes for film deposition to proceed optimally, and remove the by-product gases and vapors. These functions must be implemented with adequate control, maximal effectiveness, and complete safety.

The most sophisticated CVD reactors are those used for the deposition of electronic materials. Low-temperature (below 600°C) production reactors for normal- or atmospheric-pressure CVD (APCVD) include rotary vertical-flow reactors and continuous, in-line conveyorized reactors with various gas distribution features. They are used primarily for depositing oxides and binary and ternary silicate glass coatings for solid-state devices. Reactors for mid-temperature (600°C to 900°C) and high-temperature (900°C to 1300°C) operation are either hot-wall or cold-wall types constructed of fused quartz. Hot-wall reactors, usually tubular in shape, are used for exothermic processes where the high wall temperature avoids deposition on the reactor walls. They have been used for synthesizing complex layer structures of compound semiconductors for microelectronic devices. Cold-wall reactors, usually bell-jar shaped, are used for endothermic processes, such as the deposition of silicon from the halides or

the hydrides. Heating is accomplished by rf induction or by high-intensity radiation lamps. Substrate susceptors of silicon carbide-coated graphite slabs are used for rf-heated systems.

Reactors operating at low pressure (typically 0.1–10 torr) for low-pressure CVD (LPCVD) in the low-, mid-, or high-temperature ranges are resistance-heated hot-wall reactors of tubular, bell-jar, or close-spaced design. In the horizontal tubular design, the substrate slices (silicon device wafers) stand up in a carrier sled and gas flow is horizontal. The reduced operating pressure increases the mean free path of the reactant molecules, which allows a closely spaced wafer stacking. The very high packing density achieved (typically 100 to 200 wafers per tube) allows a greatly increased throughput, hence substantially lower product cost. In the vertical bell-jar design, the gas is distributed over the stand-up wafers, hence there is much less gas depletion and generation of few particles, but the wafer load is smaller (50 to 100 wafers per chamber). Finally, the close-spaced design developed most recently processes each wafer in its own separate, closed space chamber with the gas flowing across the wafer surface to achieve maximal uniformity.

In LPCVD, no carrier gases are required, particle contamination is reduced and film uniformity and conformality are better than in conventional APCVD reactor systems. It is for these reasons that low-pressure CVD is widely used in the highly cost-competitive semiconductor industry for depositing films of insulators, amorphous and polycrystalline silicon, refractory metals, and silicides. Epitaxial growth of silicon at reduced pressure minimizes autodoping (contamination of the substrate by its dopant), a major problem in atmospheric-pressure epitaxy.

**Vapor-Phase Epitaxy.** Vapor-phase epitaxy (VPE)[46][47][51]–[55] and metal-organic chemical vapor deposition (MOCVD)[46][47][51]–[55] are used for growing epitaxial films of compound semiconductors in the fabrication of optoelectronic devices. Composite layers of accurately controlled thickness and dopant profile are required to produce structures of optimal design for device fabrication.

**Photo-Enhanced Chemical Vapor Deposition (PHCVD).** PHCVD[56]–[58] is based on activation of the reactants in the gas or vapor phase by electromagnetic radiation, usually short-wave ultraviolet radiation. Selective absorption of photonic energy by the reactant molecules or atoms initiates the process by forming reactive free-radical species that then interact to form a desired film product. Mercury vapor is usually added to the reactant gas mixture as a photosensitizer that can be activated

with the radiation from a high-intensity quartz mercury resonance lamp (253.7 nm wavelength). The excited mercury atoms transfer their energy kinetically by collision with the reactants to generate free radicals. The advantages of this versatile and very promising CVD process is the low temperature (typically 150°C) needed to form films such as $SiO_2$ and $Si_3N_4$, and the greatly minimized radiation damage (compared to PECVD). The limitations at present are the unavailability of effective production equipment and the need (in most cases) for photoactivation with mercury to achieve acceptable rates of film deposition.

**Laser-Induced Chemical Vapor Deposition (LCVD).** LCVD[59]–[61] utilizes a laser beam for highly localized heating of the substrate that then induces film deposition by CVD surface reactions. Another mode of utilizing laser (or electron radiation) is to activate gaseous reactant atoms or molecules by their absorption of the specific wavelength of the photonic energy supplied. The resulting chemical gas phase reactions are very specific, leading to highly pure film deposits. On the other hand, the activation matching of the spectral properties with the reactant species limits the choice of reactions and hence the film deposits that can be obtained. LCVD is still in its early development stages but promises many interesting and useful applications in the future.

**Ion Implantation.** Recently, ion implantation[62]–[64] has been used to form silicon-on-insulator structures by implanting large doses of atomic or molecular oxygen ions in single-crystal silicon substrates to produce a buried oxide layer with sharp interfaces after annealing.[63] Simultaneous high-dose implantation of low energy oxygen and nitrogen ions into silicon yields very thin films of silicon oxynitride, whereas low-energy implantation of nitrogen or ammonia into silicon yields a low-density silicon nitride layer.[65]

**Thermal Oxidation.** In the gas phase, thermal oxidation[27][28][66][67] is a chemical thin-film forming process in which the substrate itself provides the source for the metal or semiconductor constituent of the oxide. This technique is obviously much more limited than CVD, but has extremely important applications in silicon device technology where very high purity oxide films with a high quality $Si/SiO_2$ interface are required. Thermal oxidation of silicon surfaces produces glassy films of $SiO_2$ for protecting highly sensitive p-n junctions and for creating dielectric layers for MOS devices. Temperatures for this process lie in the range of about 700°C to 1200°C with either dry or moist oxygen or water vapor (steam) as the oxidant. Steam oxidation proceeds at a much faster rate than dry

oxidation. The oxidation rate is a function of the oxidant partial pressure and is controlled essentially by the rate of oxidant diffusion through the growing $SiO_2$ layer to the $SiO_2$/Si interface, resulting in a decrease of the growth rate with increased oxide thickness. The process is frequently conducted in the presence of hydrochloric acid vapor or vapors of chlorine-containing organic compounds. The HCl vapor formed acts as an effective impurity getter, improving the Si/$SiO_2$ interface properties and stability.

**Oxidation of Silicon.** Silicon oxidation under high pressure[26][66][67] is of technological interest where the temperature must be minimized, such as for VLSI devices. Since the oxidation rate of silicon is approximately proportional to pressure, higher product throughput and/or decreased temperatures can be attained. The oxidant in commercial systems is $H_2O$, which is generated pyrogenically from $H_2$ and $O_2$. Pressures up to 10 atm are usually used at temperatures ranging from 750°C to 950°C.

**Other Gas-Phase Oxidations.** Gas-phase oxidation of other materials[26] is of limited technical importance. Examples include metallic tantalum films converted by thermal oxidation to tantalum pentoxide for use as antireflection coating in photovoltaic devices and as capacitor elements in microcircuits. Other metal oxides grown thermally have also been used as capacitor dielectrics in thin-film devices, to improve the bonding with glass in glass-to-metal seals and to improve corrosion resistance.

### 4.4 Liquid-Phase Chemical Formation

The growth of inorganic thin films from liquid phases by chemical reactions is accomplished primarily by electrochemical processes (which include anodization and electroplating), and by chemical deposition processes (which include reduction plating, electroless plating, conversion coating, and displacement deposition). A number of extensive reviews[26][68]–[70] of these film formation processes discuss theory and practice. Another class of film forming methods from the liquid phase is based on chemically reacting films that have been deposited by mechanical techniques.[26][69] Finally, liquid phase epitaxy[51] is still being used for growing a number of single-crystal semiconductors.

**Electrolytic Anodization.** In anodization, as in thermal oxidation, an oxide film is formed from the substrate. The anode reacts with negative ions from the electrolyte in solution and becomes oxidized, forming an oxide

or a hydrated oxide coating on semiconductors and on a few specific metals, while hydrogen gas is evolved at the cathode. Nonporous and well-adhering oxides can be formed on aluminum, tantalum, niobium, titanium, zirconium, and silicon. The most important applications are corrosion-protective films and decorative coatings with dyes on aluminum and its alloys, and layers for electrical insulation for electrolyte capacitors on aluminum and tantalum.

**Electroplating.** In electroplating a metallic coating is electrodeposited on the cathode of an electrolytic cell consisting of a positive electrode (anode), a negative electrode (cathode), and an electrolyte solution (containing the metal ions) through which electric current flows. The quantitative aspects of the process are governed by Faraday's laws. Important electroplating variables include current efficiency, current density, current distribution, pH, temperature, agitation, and solution composition. Numerous metals and metal alloys have been successfully electroplated from aqueous solutions. However, the technically most useful electroplated metals are chromium, copper, nickel, silver, gold, rhodium, zinc, and a series of binary alloys including chromium/nickel composites. Electroplating is widely used in industry and can produce deposits that range from very thin films to very thick coatings (electroforming).

**Chemical Reduction Plating.** Chemical reduction plating is based on reduction of a metal ion in solution by a reducing agent added just before use. Reaction is homogeneous, meaning that deposition takes place everywhere in the solution, rather than on the substrate only. Silver, copper, nickel, gold, and some sulfide films are readily plated. The oldest application of the process is the silvering of glass and plastics for producing mirrors using silver nitrate solutions and one of various reducing agents, such as hydrazine.

**Electroless Plating.** Autocatalytic or electroless plating is a selective deposition plating process in which metal ions are reduced to a metallic coating by a reducing agent in solution. Plating takes place only on suitable catalytic surfaces, which include substrates of the same metal being plated, hence the definition autocatalysis. Electroless (or electrodeless) plating offers a number of advantages over electroplating, such as selective (patterned) deposition, but is limited to a few metals and some alloys. Nickel, nickel alloys, and copper are most widely used commercially on conductive and on sensitized insulating substrates, including plastic polymeric materials.

**Electrophoretic Deposition.** Electrophoretic coating is based on deposition of a film from a dispersion of colloidal particles onto a conductive substrate. The dispersion in a conductive liquid dissociates into negatively charged colloidal particles and positive ions (cations), or the reverse. On application of an electric field between the positive substrate electrode (anode), the colloidal particles migrate to the substrate, become discharged, and form a film.

Chemical or electrochemical treatments of a metal surface can produce a thin and adherent layer on that metal. Examples of such conversion coatings are black oxides on steel, copper, and aluminum. Widely used chromate conversion coatings on zinc, cadmium, silver, copper, brass, aluminum, and magnesium are formed by reaction of hexavalent chromium ions with the metal, forming protective and decorative films that consist of oxides, chromates, and the substrate metal. Phosphate conversion coatings result from treatments, especially of iron and steel, with phosphoric acid-containing salts of iron, zinc, or manganese.

**Immersion Plating.** Deposition of a metal film from a dissolved salt of the coating metal on a substrate by chemical displacement without external electrodes is known as displacement deposition or immersion plating. Generally, a less noble (more electronegative) metal displaces from solution any metal that is more noble, according to the electromotive force series. Actually, different localized regions on the metal surface become anodic and cathodic, resulting in thicker films in the cathodic areas. The industrial uses of this process are limited to a few applications, mainly thin coatings on copper and its alloys.

**Mechanical Methods.** Mechanical techniques[71] for depositing coatings from liquid media that are subsequently reacted chemically to form the inorganic thin film product are spraying, spinning, dipping and draining, flow coating, roller coating, pressure-curtain coating, brushing, and offset printing of reagent solutions. Chemical reaction of the coating residue, often by thermal oxidation, hydrolysis, or pyrolysis (in the case of metalorganics) produces the desired solid film. Spin-on deposition of film-forming solutions is widely used in solid-state technology.

Liquid spray coating is probably the most versatile mechanical coating technique of the deposition techniques noted, and it is particularly well-suited for high-speed automated mass production. Deposition of very thin films is possible by judicious selection and optimization of spray machine parameters for forming "atomized" droplets and the reagent and solvent systems used to formulate the spray liquid. An example of the

capability of this refined method is the mass production spray-on deposition of organometallic alkoxy compounds, such as titanium-(IV)-isopropoxide, in an optimally formulated spray solution. Controlled pyrolysis of the deposit can form $TiO_2$ films of 70 nm thickness which serves as a highly effective and low-cost antireflection coating for silicon solar cells.[72]

It should be noted that spray deposition encompasses several other types of spraying processes that are based on either liquid sources, such as harmonic electrical spraying, or on dry source reactants that include flame spraying, arc plasma spraying, electric arc spraying, and detonation coating.[71]

**Liquid-Phase Epitaxy.** LPE[51] is used for the thermally-controlled overgrowth of thin single-crystalline films of compound semiconductors and magnetic garnets from the melt on a single-crystal substrate. This relatively old and simple technique has been successfully applied in the semiconductor industry for fabricating optoelectronic devices. However, compared to MBE, LPE is limited by poor uniformity and surface morphology.

Various additional film formation techniques[71] that are used industrially have not been discussed here, since they are essentially thick-film processes. These methods include powder or glass frit sedimentation and centrifugation, dipping, screen-printing, tape transfer, fluidized bed coating, and electrostatic spraying, all followed by thermal treatments for drying and fusion, or for chemical reaction of the deposit to form a coherent coating.

## 5.0 CRITERIA FOR THE SELECTION OF A DEPOSITION TECHNOLOGY FOR SPECIFIC APPLICATIONS

The selection of a specific technology for the deposition of thin films can be based on a variety of considerations. A multitude of thin films of different materials can be deposited for a large variety of applications; hence, no general guidelines can be given of what the most suitable deposition technology should be. In selecting an appropriate deposition technology for a specific application, several criteria have to be considered.

## 5.1 Thin-Film Applications

In considering the different applications of deposited thin films,[73][74] the following generic categories can be identified.

**Electronic Components.** The fabrication of electronic components, especially solid-state devices and microelectronic integrated circuits, have undoubtedly found the widest and most demanding applications for thin-film depositions. These films typically consist of semiconductor materials, dielectric and insulating materials, and metal or refractory metal silicide conductors.

**Electronic Displays.** Electronic displays are used for interfacing electronic equipment with human operators. Different components and device structures are required, such as:

Liquid-crystal displays

Light-emitting diodes (LEDs)

Electroluminescent displays

Plasma and fluorescent displays

Electrochromic displays

The fabrication of these displays requires conductive films, transparent and conductive films, luminescent or fluorescent films as well as dielectric and insulating layers.

**Optical Coatings.** Optical coatings are applied for antireflection purposes, as interference filters on solar panels, as plate glass infrared solar reflectors, and for laser optics. In the fabrication of filter optics, thin films with refractive index gradients are deposited on preforms from which the optical fibers are drawn. These coatings require dielectric materials with precisely defined indices of refraction and absorption coefficients. Laser optics require metal reflective coatings which can withstand high radiation intensities without degradation. Infrared reflecting coatings are applied to filament lamps to increase the luminous flux intensity.

**Magnetic Films for Data Storage.** Thin films of magnetic materials have found wide commercial applications for data storage in computers and control systems. The substrates can be metal, glass or plastic polymeric materials. Thin film deposition processes for magnetic materials and for materials with a high degree of hardness are required.

**Optical Data Storage Devices.** Thin films are finding increasing commercial use for optical data storage devices in compact disks and computer memory applications. Processes for the deposition of organic polymer materials as storage media and as protective overcoats are required for this technology.

**Antistatic Coatings.** Thin films of conductive or semiconductive materials are deposited to provide protection from electrostatic discharges.

**Hard Surface Coatings.** Thin film coatings of carbides, silicides, nitrides, and borides are finding increased uses to improve the wear characteristics of metal surfaces for tools, bearings, and machine parts. Of particularly great current interest are films of diamond-like carbon because of this material's heat dissipation properties, electrical insulation, hardness, and resistance to high-temperature and high-energy radiation.

## 5.2 Material Characteristics

The desired material characteristics of the deposited films[73][74] will be, in most cases, the decisive factor for the selection of a preferred deposition technology. In many, if not most, instances the characteristics of a thin film can be quite different from the bulk material properties, since thin films have a large surface area to bulk volume ratio. In addition, the morphology, structure, physical and chemical characteristics of the thin film can also be quite different from those of the bulk materials. The surface and/or interface properties of the substrate can drastically influence thin film characteristics due to surface contamination, nucleation effects, surface mobility, chemical surface reactions, adsorbed gases, catalytic or inhibitory effects on film growth, surface topography, and crystallographic orientation, and stress effects due to thermal expansion mismatch.

The major physical and chemical parameters of the thin film to be considered can be listed as follows:

Electrical: Conductivity for conductive films
Resistivity for resistive films
Dielectric constant
Dielectric strength
Dielectric loss
Stability under bias

| | |
|---|---|
| | Polarization |
| | Permittivity |
| | Electromigration |
| | Radiation hardness |
| Thermal: | Coefficient of expansion |
| | Thermal conductivity |
| | Temperature variation of all properties |
| | Stability or drift of characteristics |
| | Thermal fusion temperature |
| | Volatility and vapor pressure |
| Mechanical: | Intrinsic, residual, and composite stress |
| | Anisotropy |
| | Adhesion |
| | Hardness |
| | Density |
| | Fracture |
| | Ductility |
| | Hardness |
| | Elasticity |
| Morphology: | Crystalline or amorphous |
| | Structural defect density |
| | Conformality/step coverage |
| | Planarity |
| | Microstructure |
| | Surface topography |
| | Crystallite orientation |
| Optical: | Refractive index |
| | Absorption |
| | Birefringence |
| | Spectral characteristics |
| | Dispersion |

| | |
|---|---|
| Magnetic: | Saturation flux density |
| | Coercive force |
| | Permeability |
| Chemical: | Composition |
| | Impurities |
| | Reactivity with substrate and ambient |
| | Thermodynamic stability |
| | Etch rate |
| | Corrosion and erosion resistance |
| | Toxicity |
| | Hygroscopicity |
| | Impurity barrier or gettering effectiveness |
| | Carcinogenicity |
| | Stability |

## 5.3 Process Technology

As discussed before, a wide variety of process technologies are available for the deposition of thin films. The technologies differ to a large degree in their physical and chemical principles of operation and in the commercially available types of equipment. Each process technology has been pursued or developed because it has unique advantages over others. However, each process technology has its limitations. In order to optimize the desired film characteristics, a good understanding of the advantages and restrictions applicable to each technology is necessary.

The desired film thickness is closely related to the deposition or formation rates, since economical considerations determine, to a large degree, the selection of the most appropriate deposition technology. Thin films cover a thickness range from about 1 nm to several micrometers, or from film monolayers to thicknesses approaching bulk material characteristics.

Of increasing importance is the particle density associated with the deposited film. Particles originating from the equipment, the substrate, the environment, or from the reactant materials supplied to the deposition equipment can impose serious limitations to the utility of a deposition process or the equipment used. This is especially true for the fabrication of high-density microelectronic devices where the particle size can be equal

to or exceed the minimum device dimensions. Deposition processes for very-large-scale integrated (VLSI) circuits require, or will require in the near future, particle densities of less than 0.1 per $cm^2$ for particles down to 0.2 µm in diameter.

All thin film deposition equipment is quite susceptible to the integrity of the processing environment. The deposition processes described in the following chapters operate over a wide range of pressures in the reaction chamber. For proper pressure or residual gas control inside the reaction chamber, the leakage of external gases has to be minimized. For molecular beam epitaxy of thin films, for example, a maximum leak rate of $10^{-12}$ torr-liter/$cm^2$-sec is required, whereas some other process technologies can easily tolerate much higher leak rates.

Considerable attention has to be given to the source materials and their delivery into the deposition reactor. They can not only be a hard-to-detect source of impurity contamination, but can also influence the uniformity of the deposited films. The source materials used for thin film deposition can be either solid, liquid or gaseous. Special techniques for source material delivery have been developed for each type of material and rate of delivery to the deposition reactor.

The purity of the deposited film not only depends on the purity of the source materials delivered to the reactor and the leak-tightness of the system, but also to a large degree on the substrate cleaning procedure. Deposition techniques have been developed which permit film deposition with purity levels down to $10^{12}$ impurity atoms per $cm^3$, or roughly one part in $10^{10}$.

The stability and repeatability of the processes are of considerable importance, especially in the large-scale manufacturing of semiconductor devices. Many different factors can influence the deposition process, and it is extremely important to understand and control these parameters. To make a film deposition process acceptable for device manufacturing, an extensive and careful characterization of the processes and equipment is often required. Any process instabilities or uncontrolled deposition parameters should be discovered and rectified during this procedure.

The uniformity of the deposited films, both in thickness and composition, is of great concern for most deposition processes. In the manufacturing of integrated circuits, small variations in film uniformity can have a large influence on the manufacturing yield. For VLSI circuits, film uniformity deviations of less than 5% are required at present. It is expected that the uniformity requirements will become even more

stringent, decreasing to a deviation limit of 1 to 2% in the near future. These requirements impose severe restrictions on the design of the deposition reactor, the delivery of the reactant materials, and the control of the process parameters.

Thin-film deposition processes for solid-state device fabrication are needed in many steps in the fabrication process sequence. It is important that compatible deposition processes are selected that do not interfere with the structures already built into the device. The process integration, which has to consider thermal effects, chemical and metallurgical compatibility as well as functional requirements and limitations, is a major consideration in successful process selection.

Frequently, the deposition processes have to offer a high degree of flexibility in meeting the demands for specific device requirements. The process selection has to be based on adjusting deposition parameters such as film thickness, uniformity and composition. During the process characterization described above, a good understanding of the sensitivity and control of the film characteristics can be obtained.

In a device fabrication process sequence, one frequently has to deposit films on a nonplanar surface. The deposited film should be uniform across all structural details of the substrate topography. For example, in VLSI structures, contact holes with micron or submicron dimensions should be uniformly coated with metal films not only inside the small contact cavities, but also on their vertical walls. This is referred to as *step coverage* or *conformality*. The different deposition processes described in the following chapters can result in quite different degrees of step coverage.

An important requirement for high-density VLSI devices is planarization of the substrate topography after film deposition. This is necessary in multilevel device fabrication processes where subsequent photolithographic pattern definition of very small geometries is required, or where deposited material step coverage is essential. The focal depth of the photolithographic equipment is on the order of one micron. To image the pattern across the entire field of view demands a highly planar surface topography.

The large number of process parameters that can affect the uniformity and composition of the deposited films make in situ monitoring of the deposition parameters highly desirable. Many process parameters, such as reactor pressure, substrate temperature, reactant gas composition and deposition rates can be monitored in real time. However,

significant improvements in process monitoring devices, real-time analytical instruments and process simulation can be expected in the next couple of years that promise to enhance the overall fabrication yield for devices manufactured by thin-film deposition processes.

### 5.4 Thin-Film Manufacturing Equipment

The equipment for the deposition of thin films can be classified into three basic categories:

- Thin-film deposition equipment for device research and development.
- Prototype equipment for the study of new or established deposition processes.
- Thin-film production equipment for device manufacturing.

The prototype equipment for the development of new deposition processes can encompass a wide variety of designs and constructional details. Only the future outlook for the requirements and applications of such equipment is discussed in the following chapters in this book.

The deposition equipment for the research and development of new device structures has to meet, in general, quite different requirements than the equipment used in the manufacturing of devices on a large scale. Research and development equipment requires a high degree of flexibility in deposition parameters, in accommodation of a variety of substrates, and in process monitoring equipment. High product throughput and a high degree of equipment automation are usually not required.

Thin-film deposition equipment used in high volume manufacturing is designed, in most cases, for a very limited range of applications. The major consideration is the cost-effectiveness of the equipment, which can be characterized as the ratio of cost per device divided by the value added to the device. The equipment cost, consisting of acquisition cost, amortization and maintenance cost is a major consideration for the selection of production-worthy deposition equipment. System throughput, expressed in the number of substrates processed per hour for a given film thickness, is a major selection criterion. Equipment reliability, characterized by equipment uptime, mean time between failures (MTBF) and mean time to repair (MTTR) is becoming increasingly a part of equipment specifications and is subject to standards for fabrication equipment. Expectations for equipment uptime, as currently required in the semiconductor industry,

is in excess of 90%. The high cost of manufacturing equipment for film depositions mandates the need for ease of maintenance and repair. Undesirable deposition on reactor walls and fixtures should be minimized. Self-cleaning features using reactive gas plasma discharges are rapidly gaining in popularity.

Until recently, most deposition equipment used in thin film manufacturing has been of the batch processing type. A limited number of substrates to be coated is loaded into the deposition chamber and processed as a unit. Batch processing, although offering good process control, suffers in general from limited throughput. The time required for substrate loading, pump-down, purging, thermal equilibration, recovery, and cool-down accounts for a considerable percentage of the total batch processing time. With the availability of load-lock systems, permitting the insertion of substrates into the reactor chamber without major disturbance of the process chamber pressure and environment, a considerable improvement in product throughput and film quality can be obtained. Therefore, continuous process reactors, including advanced single-substrate reactors, are finding increasing acceptance for film deposition in device manufacturing. The continuous process reactors offer the additional advantages of incorporating process steps for pre-deposition cleaning of the substrate as well as post-deposition treatments, such as thermal annealing.

The automation of deposition equipment is making rapid progress. Automated deposition systems provide automatic loading and unloading, process sequencing, and control of variables, such as reactor pressure, gas flows, and substrate temperature. In addition, diagnostic capabilities for detecting and analyzing equipment failures, maintenance requirements, and process integrity are being incorporated. Equipment communication of process parameters, failure modes and product status with upstream host computers as well as remote process recipe generation is becoming increasingly available for modern deposition equipment.

## 6.0 SUMMARY AND PERSPECTIVE FOR THE FUTURE

The importance of thin-film deposition technology in modern fabrication processes has been discussed with examples from the production of semiconductor devices. Following this overview, thin-film deposition technologies have been outlined and classified into four major generic categories: (*i*) evaporative methods, (*ii*) glow-discharge processes, (*iii*) gas-

phase chemical processes, and (*iv*) liquid-phase chemical film formation techniques. Important technologies from each of these categories have been discussed with respect to the underlying principles, salient features, and typical applications. Criteria for selecting a particular thin-film deposition technology have then been described in terms of specific applications, material characteristics, and processing. Finally, thin-film manufacturing equipment has been discussed and categorized.

A variety of different thin-film deposition technologies and equipment is available from which a selection can be made. These technologies are described in the following chapters in some detail. It is possible to a large degree to tailor the deposition process to the specific needs, based on:

- Physical and chemical material characteristics
- Specific applications
- Advantages and limitations in process technology
- Manufacturing technology and equipment

The fabrication processes established for semiconductor devices during the last two decades have provided an important stimulus for the development of new thin-film materials, processes and equipment. It can be expected that this trend will continue for the decade.

The current trends[52][53][75][76] in deposition technology for the fabrication of semiconductor devices are characterized by:

- A shift to larger substrate sizes
- Automation in substrate handling and process controls
- Reduction in particle and metal contamination
- Improvements in equipment reliability and ease of service and maintenance
- Lower process temperatures
- Improvements in film uniformity
- Reduced in-process damage (due to high voltage, radiation, particle bombardment, electrostatics, etc.)

The number of deposition steps in the fabrication sequence of integrated circuits is expected to increase with the advent of more complex circuits, as shown in Table 2.[75] Less complex devices, such as those introduced a decade ago, typically NMOS and CMOS integrated circuits, have required

only three deposition steps for inorganic film deposition, whereas more advanced devices such as high-performance VLSI silicon integrated circuits, now require 8 to 11 deposition steps. With increasing demands for cost reductions in the manufacturing of integrated circuits, cost-effective, high-volume manufacturing equipment for all deposition processes will be required.

**Table 2.** Film Deposition for Silicon Integrated Circuit Fabrication*

| Deposition | Number of Steps Required for IC Fabrication | | | | |
|---|---|---|---|---|---|
| | H-CMOS | HMOS | CMOS/ NMOS | Schottky TTL | ECL |
| Polysilicon | 2 | 1–3 | 1 | — | 1 |
| Epitaxy | 1 | — | — | 1 | 1 |
| PSG/$Si_3N_4$ | 2–3 | 1–2 | 1 | 2 | — |
| Aluminum** | 1 | 1–2 | 1 | 2 | 2–3 |
| Other Metals | 1–2 | 1 | — | 1 | — |
| Silicides | 1–2 | 0–2 | — | — | — |
| Total Deposition Steps | 8–11 | 4–10 | 3 | 6 | 4–5 |

*Data from Ref. 75, courtesy *Semiconductor International,* Cahners Publishing Company.

**Not usually deposited by CVD.

New semiconductor device structures based on III-V semiconductor compounds for microwave, high-speed and optoelectronic applications will require improved deposition systems and higher throughput capabilities for economic device fabrication, especially molecular beam epitaxy (MBE) and metal-organic chemical vapor deposition (MOCVD) equipment. Superlattice structures with alternating films of a few atomic layers with different compositions will demand a high degree of process control.

Three-dimensional integrated structures consisting of 3 to 5 layers with active components are under development in various laboratories. These structures are likely to require highly sophisticated deposition technologies and equipment.

Considerable interest exists to enhance the survivability of integrated circuits in hostile environments, such as high-energy radiation, high operating temperatures, and polluted atmospheres. The development of protective layers and more resistant device structures will require new thin-film materials and deposition processes.

Complex high-density integrated circuits face increased limitations in interconnecting the numerous components on a chip. Optical interconnection schemes are under development which can reduce this problem considerably. This trend will lead to new technologies combining optoelectronic device technology with the existing semiconductor process technologies. Thin-film deposition techniques will most likely play an important role for the fabrication of these interconnections.

This overview of the important processes and techniques used industrially for forming thin films indicates the extremely powerful and versatile arsenal of methods that is now available to the technologist. Coatings can be prepared that can meet a very wide range of requirements for specific industrial or scientific applications. While remarkable advances in thin-film technology have been made, there are still areas in which the technology is leading science. This is particularly true for photo-induced, ion-assisted, and plasma-enhanced processes; these areas should provide fertile ground for future research.

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# 2

# Silicon Epitaxy by Chemical Vapor Deposition

*Martin L. Hammond*

## 1.0 INTRODUCTION

The word *epitaxy* is derived from the Greek "epi"—upon, and "taxis"—to arrange. Thus, epitaxial silicon deposition requires the ability to add and arrange silicon atoms upon a single crystal surface. Epitaxy is the regularly oriented growth of one crystalline substance upon another. Specific applications require controlling the crystalline perfection and the dopant concentration in the added layer.

Two different kinds of epitaxy are recognized:

Homoepitaxy growth in which the epitaxial layer is of the same material as the substrate.

Heteroepitaxy growth in which the epitaxial layer is a different material from the substrate.

Virtually all commercial silicon epitaxy is homoepitaxy, with the exception of silicon-on-sapphire.

Epitaxial silicon layers can be created by a wide range of techniques, including evaporation, sputtering, molecular beams, and various

regrowth concepts. This chapter discusses epitaxial deposition by chemical vapor deposition (CVD) in which the silicon and dopant atoms are brought to the single crystal surface by gaseous transport.[1][2]

Chemical vapor deposition is the formation of stable solids by decomposition of gaseous chemicals using heat, plasma, ultraviolet, or other energy sources, or a combination of sources. CVD is a relatively old technology. It was used to refine refractory metals in the 1800s, to produce filaments for Edison's incandescent carbon filament lamps in the early 1900s, for hard metal coatings in the 1950s, and for semiconductor material preparation beginning in the 1960s.[2a]

Commercial silicon epitaxy production, at present, is accomplished primarily by CVD using heat as the energy source for decomposing the gaseous chemicals.

With the silicon epitaxy process, radical changes in materials' properties can be created over small distances within the same crystal. This capability permits the growth of lightly doped single crystal silicon on top of heavily doped single crystal silicon. At present, no other process technique permits this configuration of doped regions within a single crystal substrate.

Many different configurations are made possible by the CVD epitaxial deposition process. Some of the possibilities in use today include:

- *n*-type silicon over *p*-type silicon
- *p*-type silicon over *n*-type silicon
- Lightly doped over heavily doped of either type
- Lightly doped over heavily doped buried layer patterns
- Conducting silicon layers over insulating surfaces
- Silicon layers with controlled dopant profiles
- Silicon selectively deposited through oxide

## 1.1 Applications of Silicon Epitaxy

Silicon epitaxy is required for isolation and for device performance in bipolar integrated circuits. It is also important far discrete device performance, and is becoming important for MOS integrated circuits (ICs).

For bipolar devices, epitaxy provides a wide range of device performance benefits too numerous to describe here. Among these benefits are:[1]

- Higher switching speeds
- Improved high voltage, linearity characteristics
- Simplified isolation
- Lower base resistance
- Independently controlled dopant profiles
- Buried layer patterns

MOS ICs have not required an epitaxy layer to create device isolation; however, as MOS ICs have become more complex, epitaxial layers can provide many device benefits.[3] MOS ICs are usually created in lightly doped substrates. When a lightly doped epitaxial layer is used over a heavily doped substrate, the benefits to MOS ICs include:

- Lower diffused-line capacitance
- Better diffused-line charge retention
- Better control of spurious charge (such as alpha particles and static charge)
- Improved dynamic random access memory performance

For complementary MOS (CMOS) ICs, the benefit is a very significant improvement in latch-up protection.

Because of its wide-ranging applications to semiconductor technology, approximately 50% of all silicon processed requires an epitaxy layer, and this percentage is expected to increase to 60–70% when epitaxy is used more extensively in MOS IC production.[4]

Silicon epitaxy is used in a wide range of thicknesses and resistivities. In commercial silicon epitaxy, layer thickness is usually expressed in micrometers (µm), commonly abbreviated microns (µ) or $10^{-4}$ cm. Resistivity is expressed as ohm-cm, and resistivity is related to the electrical carrier concentration by Irwin's curves.[5]

Table 1 lists typical specifications for the common silicon device structures now in production. With the trend to ever smaller feature sizes and ever higher circuit densities, there is a long range tendency toward thinner epitaxial layers; however, the values noted in Table 1 will probably be valid until well into the 1990s.

**Table 1.** Typical Epitaxy Specifications

| Device Type | Thickness (microns) | Resistivity (ohm-cm) |
|---|---|---|
| Bipolar discrete devices | | |
| High Frequency | 0.5–3 | 0.15–1.5 |
| Power | 5–100+ | 0.5–100+ |
| Bipolar integrated circuits | | |
| Digital memory | 0.5–5 | 0.3–1.5 |
| Microprocessor | 0.5–5 | 0.3–1.5 |
| Linear | 3–15 | 2–20 |
| MOS-on-epitaxy integrated circuits | | |
| $P/P^+$ (Back-sealed substrates) | 4–20 | 10–40 |
| $N/N^+$ | 0.5–7 | 1–10 |
| BiMOS* | 0.5–3 | 0.5–3 |

* BiMOS = Bipolar and MOS devices together in the same device.

Evaluation of silicon epitaxy is a major technology and detailed information for standardized techniques is available in Refs. 5 and 6. This chapter on silicon epitaxy will address:

- Theory of silicon epitaxy by CVD
- Silicon epitaxy process chemistry
- Process adjustments
- Equipment considerations for silicon epitaxy
- Other equipment considerations
- Defects in epitaxy layers
- Safety
- Key technical issues

## 2.0 THEORY OF SILICON EPITAXY BY CVD

Successful silicon epitaxy depends upon having:

- High surface mobility for the arriving atoms.
- Numerous, equivalent growth sites.
- Commercially significant growth rates.

Production silicon epitaxy since the early 1960s has been manufactured by chemical vapor deposition in $H_2$ from the chlorosilanes: $SiCl_4$, $SiHCl_3$, $SiH_2Cl_2$, and $SiH_4$ in open tube, vapor transport systems. Alternate chemistries using iodides and bromides have been investigated but no overwhelming advantages have been noted. Fluorine chemistry has not been explored significantly because the Si-F bond is thermodynamically very strong and very high temperatures would be required to crack most Si-F compounds.

As illustrated in Fig. 1, CVD is a heterogeneous reaction involving at least the following steps:[1d][2b][7]

Arrival

1. Bulk transport of reactants into the process volume
2. Gaseous diffusion of reactants to the surface
3. Absorption of reactants onto the surface

Surface reaction

4. Surface reaction (reaction can also take place in the gas volume immediately above the surface)
5. Surface diffusion
6. Crystal lattice incorporation

Removal of reactant by-products

7. Reaction by-product desorption
8. Gaseous transport of by-products
9. Bulk transport of by-products out of process volume

The rate of chemical vapor deposition is primarily controlled by one of the following major groups of process steps:

- The rate of arrival of reactants
- The surface reaction rate
- The rate of removal of by-products

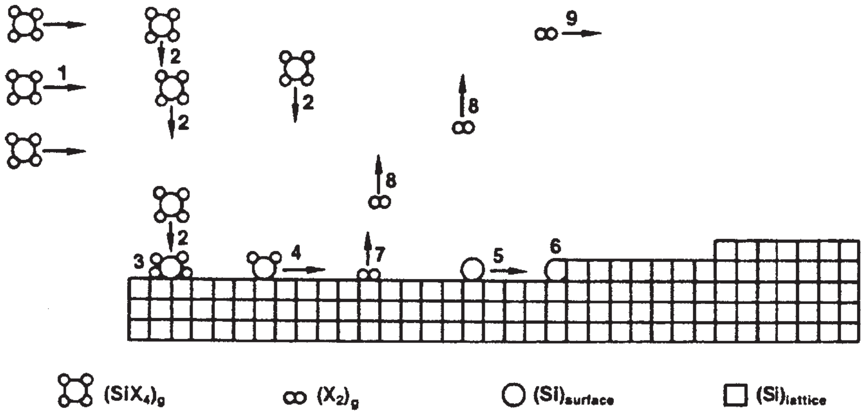



**Figure 1.** Heterogenous reaction rate model illustrating arrival (*1*, *2*, *3*), surface reaction (*4*, *5*, *6*), and by-product removal (*7*, *8*, *9*).

For typical epitaxy process, the reaction conditions are established so that the rate of arrival of the reactants controls the growth rate. This procedure gives the best crystal quality, a feature necessary in good device performance.

The crystal quality of the epitaxial layer is controlled primarily by:

- The nature of the surface prior to epitaxial growth
- The arrival rate relative to the surface diffusion rate
- The nature of the lattice incorporation

If the surface prior to deposition has contamination, such as oxides, which are not removed during heat-up and etch, or if the crystal upon which the epitaxial layer is to be grown is defective, then the epitaxial layer will have crystal defects. If the rate of arrival of reactants greatly exceeds the surface diffusion rate, then the diffusing atoms cannot move to positions of lowest energy, and again, crystal defects occur.

The rate of lattice incorporation is a function of crystal orientation because the density of atomic sites is a function of which crystallographic faces are exposed. Figure 2 shows the effect of substrate orientation on growth rate for (111), (110), and (100) faces. For silicon, the (110) plane has the highest growth rate, followed by the (100) and (111) planes.[8]

For epitaxial growth on crystal faces directly on orientation, the low growth rate for the (111) planes encourages a defect called faceting or orange peel. Growth perpendicular to the (111) surface is slow, while growth on a facet not parallel to the surface is faster. The result is a shingle-like faceted surface. To prevent faceting, (111) surfaces for epitaxial growth are cut a few degrees off the (111) to cause the growth to proceed in waves across the surface. Epitaxial growth on the (100) plane does not have this problem; therefore, (100) surfaces are usually cut directly on orientation.

Surface preparation is an important factor in producing good epitaxial crystal quality. The surface requires a high quality, defect-free chemical/mechanical polish that leaves the surface polished without mechanical damage to the crystal structure. Foreign matter such as organic compounds must be removed because it will react with the crystal surface during heat-up to form undesirable silicon compounds, leading to defects.

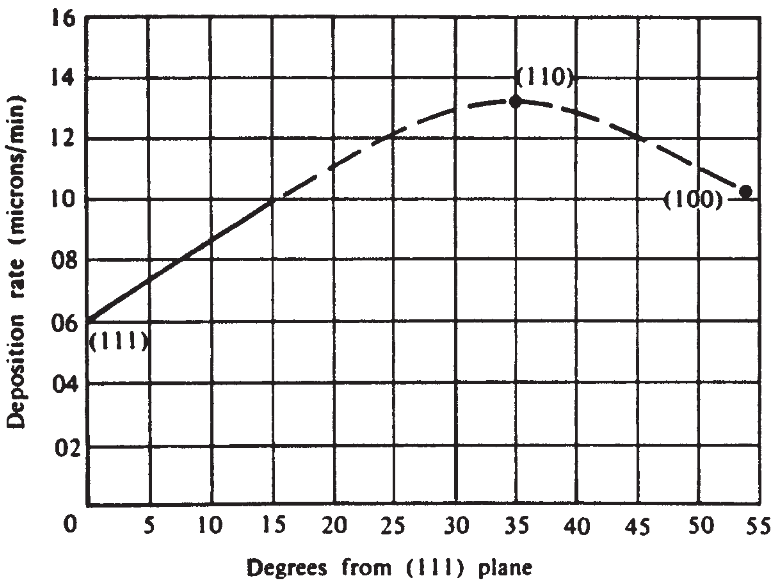



**Figure 2.** Effect of substrate orientation on epitaxial silicon growth rate.[1c]

## 3.0 SILICON EPITAXY PROCESS CHEMISTRY

The conditions for acceptable commercial silicon epitaxy are outlined in Table 2. Generally, the lower the temperature, the lower the growth rate for acceptable epitaxy quality, and the lower the tolerance for oxidizers in the process space. If silicon oxides, including SiO, are allowed to form during deposition, they interfere with surface diffusion and lattice incorporation, leading to various defects in the epitaxy layer.

**Table 2.** Silicon Epitaxy Growth Conditions

| Chemistry | Growth Rate (microns/minute) | Temperature Range (°C) | Allowed Oxidizer (ppm) |
|---|---|---|---|
| $SiCl_4$ | 0.4–1.5 | 1150–1250 | 5–10 |
| $SiHCl_3$ | 0.4–3.0 | 1100–1200 | 5–10 |
| $SiH_2Cl_2$ | 0.3–2.0 | 1050–1150 | <5 |
| $SiH_4$ | 0.1–0.3 | 950–1050 | <2 |

Epitaxy quality is especially sensitive to the presence of oxidizers during heat-up. Water vapor absorbed on cold wafer carriers can be a significant source of oxidizer in the process chamber; therefore, there is a substantial difference in surface quality between beginning the epitaxy cycle with a cold or warm wafer carrier. In a leak-free system, water vapor from a cold wafer carrier can easily be the largest source of oxidizer in the reactor.[9a]

At low concentration, water vapor etches Si surfaces by formation of volatile SiO in $H_2$. However, at about 1 part per million (ppm) $H_2O$ at 900°C, water vapor begins to form $SiO_2$ on the Si surface, and this $SiO_2$ can lead to surface and crystal defects.[9b] The presence of excess $H_2$ will reverse this reaction somewhat; however, only a few ppm of water vapor during heat-up will seriously degrade the epitaxy quality. (See Table 2 and Ref. 9a).

Epitaxial silicon can be grown from less than 1 micron thickness to more than 100 microns. Thicknesses below about 2 microns are considered very thin and careful consideration must be given to the dopant transition from a heavily doped substrate to a more lightly doped epitaxy layer. Thicknesses above about 30 microns are considered very thick and care must be taken to reduce defects that can develop during long deposition times.

Epitaxial silicon is normally doped with $PH_3$, $AsH_3$, and $B_2H_6$. Resistivity levels below about 0.1 ohm-cm are considered heavily doped and require proportionately much higher dopant concentrations in the gas stream to achieve the desired resistivity levels. As the dopant solid solubility is approached (nominally 0.001 ohm-cm), very high concentrations of dopant are required in the gas stream and the epitaxial layer can become a two-phase polycrystalline deposit if the solid solubility is exceeded. When very high concentrations of dopant are added to the reactor, dopant can be absorbed onto the reactor walls and be liberated into the room upon exposure to room air and water vapor. Rigorous safety procedures and adequate ventilation are required when using dopant hydrides, especially when using concentrations in the supply cylinder greater than about 100 ppm.

Resistivity levels above about 10 ohm-cm are considered very lightly doped because the intended dopant level is low enough to be influenced by the typical background dopant levels in the reactor. The undoped or intrinsic dopant level in a commercial epitaxy reactor is a function of the purity of the deposition chemicals, the integrity of the SIC coating on the graphite wafer carrier, the level of other unwanted contamination, and the dopant history of the heated parts within the system. A clean reactor with a fresh wafer carrier and commercially available deposit chemicals should be able to demonstrate an intrinsic resistivity level of greater than 100 ohm-cm *n*-type on 0.005–0.010 ohm-cm Sb ($n^+$) and on >10 ohm-cm *p*-type substrate. In most reactor designs, autodoping from more heavily doped As-, P-, or B-doped substrates will affect the intrinsic resistivity. The larger the area of heavily doped silicon in the reactor, the more effect.

Gaseous HCl is used to etch the silicon surface and remove surface damage prior to epitaxial deposition. The etch rate slowly increases with increasing temperature and, at about 1150°C, a 0.1% $HCl/H_2$ mixture will remove silicon at 0.1–0.3 micron/minute. If the HCl etch rate is too high for a given temperature, the surface will be pitted instead of being polished. For temperatures above about 1150°C, silicon can be etched at up to 1.5 microns/minute without pitting. In the 1050–1100°C range, an etch rate of 0.1–0.5 micron/minute will polish the surface. Below 1050°C HCl is more likely to pit rather than polish the water surface.[10a,d] $SF_6$ has been considered as a Si etchant because it provides a smooth surface at etch temperatures below 1100°C.[10e] Unfortunately, $SF_6$ reacts with the $H_2$ to form $H_2S$, and the resulting odor makes $SF_6$ unusable in a commercial environment.

Because of the quality of chemical/mechanical polishing available today,[10f] there is generally little requirement to remove silicon from the surface to achieve good epitaxy quality. An $H_2$ bake at 1150°C for 10 minutes will remove native oxide and provide good surfaces.[10g,h] Nonetheless, commercial epitaxy processes often call for a light HCl etch to remove a micron or less Si just to ensure a low defect density.

When depositing with chlorosilanes, HCl is created by surface and gas phase reactions. This HCl enhances film quality by etching the high energy surface atoms during deposition. When HCl is added to $SiH_4$, this simultaneous etch/deposit process also occurs and the etch reaction can be treated as if it were separated from the $SiH_4$ deposition process.

For conditions used in commercial production, the epitaxial silicon growth rate is proportional to the concentration of silicon source gas in the process stream.[1][11a,b] Dopant incorporation, for a given temperature, is approximately proportional to the dopant concentration; however, temperature is a primary factor. As and P exist as metallic vapor at deposition temperature;[11b] therefore, higher temperatures increase the escaping tendency of these dopants and, thereby, increase the resistivity for fixed dopant concentration in the gas stream. As is more sensitive to temperature than P. B forms complex hydrides at deposit temperatures; therefore, higher temperatures promote higher reaction rates near the wafer surface and produce lower resistivities. B doping is more sensitive to the presence of oxidizers than As or P.[11d] Oxidizers generally inhibit the incorporation of dopant.

## 4.0 COMMERCIAL REACTOR GEOMETRIES

The reactor chamber geometry affects the gas flow characteristics which, in turn, affect the properties of the deposited layers.

Chemical reactors can be described by one of two flow types:

- Displacement or plug flow in which the entering gas displaces the gas already present with a minimum of mixing.
- Mixed flow in which the entering gas thoroughly mixes with the gas already present before exiting the reactor.

When making a gas composition change in a displacement or plug flow reactor, one volume change can produce an approximately 100% change in gas composition by displacing the volume of gas already present. When

making a gas composition change in an ideal mixed flow reactor, the gas composition changes exponentially with the number of volume changes.

Because the epitaxy process involves complex intermediate chemical reactions with trace quantities of dopant making significant changes in material properties, the nature of gas flow in the reactor can have a major effect on reactor performance. In general, mixed flow reactors have very uniform wafer-to-wafer resistivity control, even if there is significant autodoping from the substrate. Displacement flow reactors can have sharper dopant transition widths, with autodoping effects increasing from wafer to wafer along the length of the process gas stream. High total flow rate, reduced pressure operation, and other reactor design elements will strongly influence these generalizations.

Figure 3 illustrates the three principal reactor geometries used in commercial epitaxy production.

## 4.1 Horizontal Reactor

The horizontal reactor is a displacement flow system in which the depletion of reactants downstream is accommodated by tilting the susceptor up to increase the local velocity, and thereby, increase the local growth rate. Overall gas velocities are in the 30–70 cm/sec range.[12]

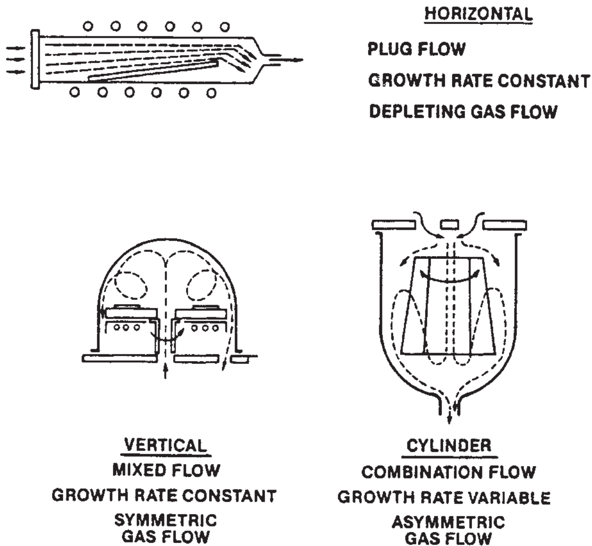



**Figure 3.** Principle CVD reactor geometries for silicon epitaxy.

## 4.2 Cylinder Reactor

The commercial cylinder reactor is a combination flow system with a substantial degree of gas mixing and a complex flow path in which the entering gas eventually displaces the depleted gas out the exhaust port.[13] Depletion is accommodated by having the wafer carrier tilt out at the bottom to increase the local velocity and by having two gas jets which give a strong downward velocity to the gas as it enters the reaction space. This downward velocity is locally 40–70 cm/sec and averages 10–20 cm/sec over the surface of the cylindrical wafer carrier. Rotation of the carrier through the high velocity/high concentration and low velocity/low concentration portions of the mainstream improves uniformity. Tangential velocities for the cylinder reactor are nominally 2–3 cm/sec.

## 4.3 Vertical Reactor

The vertical reactor is a mixed flow system in which fresh process gas enters the process space through a central port and mixes with the depleted gas as it flows radially inward over the wafer carrier surface. The fresh process gas stimulates a convection current which rises from the center of the carrier plate, cools at the bell jar surface, and flows back toward the carrier plate along the bell jar wall. Radial gas velocities near the carrier plate are estimated to be 5–10 cm/sec, compared with the tangential velocities of 2–4 cm/sec where wafers are placed on the wafer carrier.[14]

## 4.4 New Reactor Geometry

A new commercial epitaxy reactor geometry was introduced in May 1986[15] in which a circular cluster of wafer carriers create tapered cavities, with each cavity having two wafers facing each other, as illustrated in Fig. 4. Process gas enters at the outer diameter defined by the tapered cavities and flows by displacement flow toward the center of the circular cluster of cavities. Process gas depletion is accommodated by the acceleration of the gas in the tapered cavities in a manner similar to that for the horizontal reactor geometry. Because of displacement flow, each cavity is isolated from the others so that very little interaction occurs. With this design, very high intrinsic resistivities can be achieved, even with up to fifty 150-mm diameter heavily doped substrates in the reactor. Radial gas velocities of 15–30 cm/sec are typical compared with 2–3 cm/sec tangential velocities.

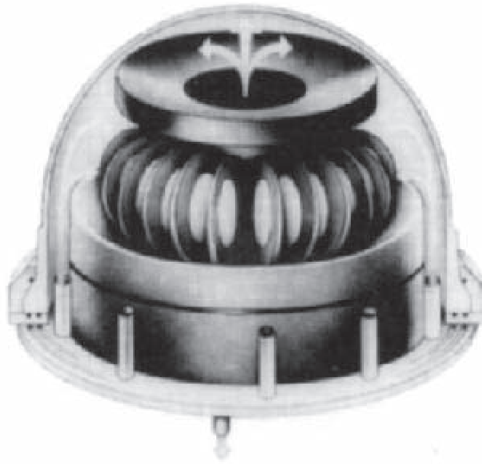


**Figure 4.** Tapered cavity epitaxy reactor.[15]

## 5.0 THEORY OF CHEMICAL VAPOR DEPOSITION

An understanding of the theory of CVD is useful in developing techniques for making process adjustments in commercial production. The theory of CVD is based on chemical kinetics, fluid mechanics, chemical engineering principles, and an understanding of growth mechanisms.[1][2][12][14]

Heterogeneous CVD reactions follow the general reaction path outlined in Fig. 1. For simplicity, one reaction step is considered to be rate controlling. When CVD reaction rates for a particular chemistry and reactor geometry are plotted over reciprocal temperature (Fig. 5), the deposition or growth rate varies exponentially with temperature,[1] and two regimes are recognized.[16]

- The kinetic or surface reaction rate controlled regime which occurs at lower temperatures.
- The diffusion or rate of arrival controlled regime which occurs at higher temperatures.

The diffusion controlled regime is also termed the mass transport controlled regime.

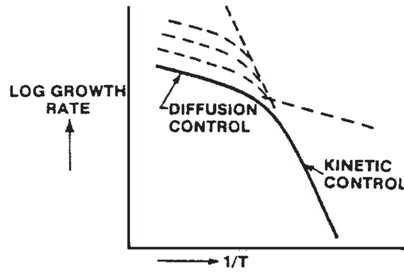



**Figure 5.** Typical overall reaction rate for CVD reactors vs. reciprocal temperature.[16]

Below some temperature, the surface reaction rate normally controls because, for a given reactor geometry, the rate of arrival is greater than the surface reaction rate. As the temperature is increased, the overall surface reaction rate usually increases more rapidly than the overall mass transport rate, and the rate of arrival or mass transport rate becomes the limiting factor.

Growth rates vs. reciprocal temperature for the chemicals commonly used in silicon epitaxy are plotted in Fig. 6.[16] The individual curves in Fig. 6 can be moved vertically on the scale by changing the reactant concentration and reactor geometry; however, the shape of the curves is relatively stable. Each growth rate curve can be described by a kinetic and a diffusion controlled regime, as done in Fig. 5. Note that, for a given temperature and concentration, the growth rate is lower for the more thermodynamically stable compounds.

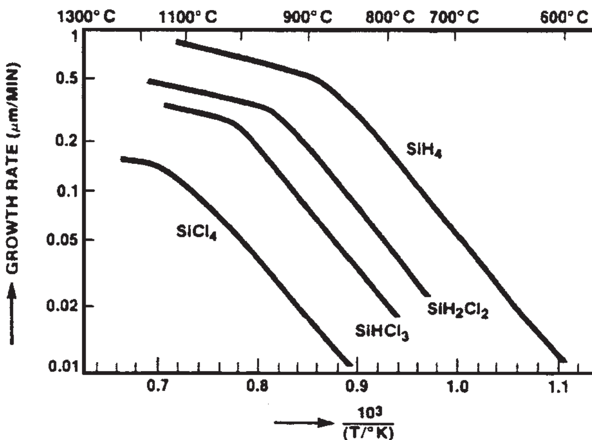



**Figure 6.** Temperature dependence of silicon growth rate.[16]

Epitaxial silicon is normally grown in the diffusion or mass transport limited regime, at a temperature near the high temperature side of the knees of the curves in Fig. 6. This temperature region is selected to be high enough to thermally decompose the selected chemical at a rate commensurate with the surface diffusion rate.

Bloem's data[16b] in Fig. 7 demonstrate how growth rate controls the morphology of the deposited layer. In all cases, increasing the rate of arrival causes a decrease in the degree of crystalline order for the polycrystalline-to-amorphous transition in the 550–650°C range and the single crystal-to-polycrystalline transition in the 1000–1400°C

The concept that morphology is controlled by the rate of arrival relative to the surface diffusion rate applies on the finer scale of epitaxial crystal perfection. In general, the lower the temperature of deposition, the lower the growth rate must be to accommodate a given level of crystal perfection. It is this concept that controls the growth rate/temperature conditions used in commercial silicon epitaxy.

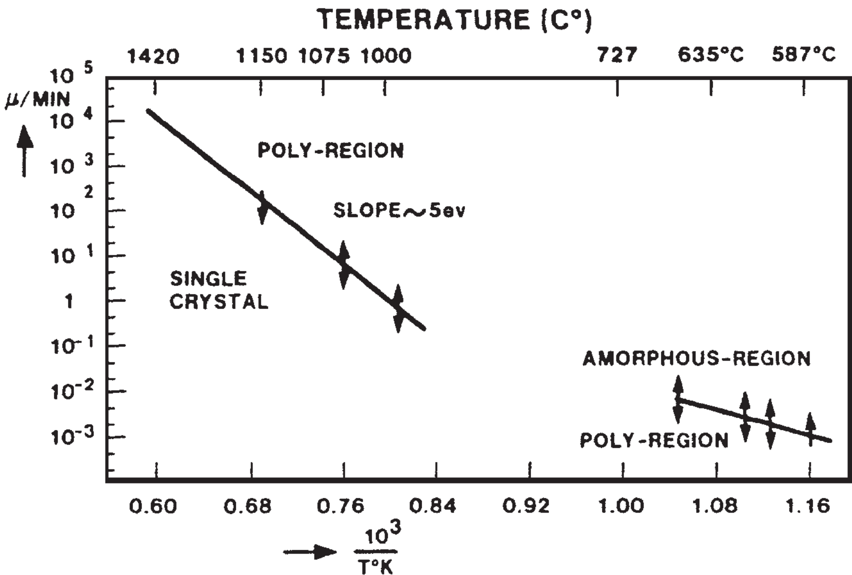



**Figure 7.** Relationship of growth rate, morphology, and growth temperature for silicon epitaxy.[16b]

## 6.0 PROCESS ADJUSTMENTS

The important CVD reactor control parameters can be divided into two categories: reactor design variables and operator variables. Each has a direct influence on the uniformity, productivity, and quality of the epitaxial layer.

The reactor design variables are:

- Tilt angle or equivalent
- Gas inlet geometry
- Wafer/carrier configuration
- Wafer/reactor wall configuration
- Exhaust configuration

Operator variables include:

- Gas flow rate
- Gas composition
- Temperature profile
- Temperature value
- Chemistry

Uniformity of an epitaxy layer refers to uniformity of both thickness and resistivity. Thickness is primarily controlled by the mass transport and surface reaction rates. Resistivity is controlled by dopant incorporation which, in turn, depends primarily on local concentration of dopant and local temperature.

The most effective process adjustment strategy is:

1. Establish a flat temperature profile with the desired chemistry, temperature, pressure, and growth rate.
2. Mechanically adjust for thickness uniformity.
3. Fine tune resistivity with local temperature adjustments.

Selections of chemistry, temperature, pressure, and growth rate are determined by the desired materials and device properties. The usual operating conditions for commercial silicon epitaxy are presented in Table 1.

The key to thickness control in a mass-transport-limited epitaxial CVD process is compensation for depletion.

## 6.1 Horizontal Reactor

The horizontal reactor depicted in Fig. 3 offers a simple model for describing how to compensate for depletion and the lessons learned here are applicable to other reactor geometries.

It can be useful to break the thickness profile in the direction of gas flow along the wafer carrier or susceptor into the front and back half, as illustrated in Fig. 8. Each half can then be described as thick or thin in front, or thick or thin in back. The advantage is that the mechanical adjustments for thickness uniformity are also divided into those that affect the front half and those that affect the back half of the profile.[17]

The overall concave-down profile in Fig. 9 can be described as thin in front and thin in back, rather than thick in the middle. The S-shaped profile in Fig. 9 can be described as thin in front and thick in back.

Figures 10 and 11 illustrate the action necessary to correct a thickness profile that is thick or thin in the front or back. The underlying principle is that local growth rate is a direct consequence of local reaction rate. Therefore, local growth rate can be increased by increasing local velocity, temperature, and concentration, and vice-versa.

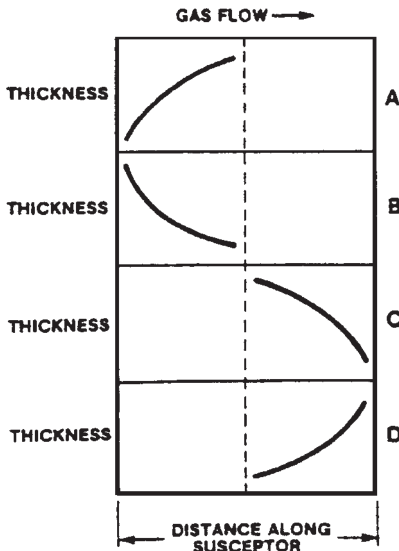



**Figure 8.** Thickness variation possibilities along the direction of process gas flow for horizontal reactor.[17a]

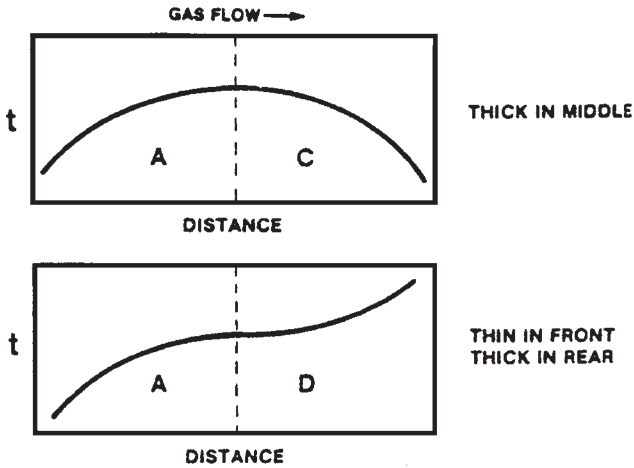



**Figure 9.** Thickness variation combinations along direction of process gas flow for horizontal reactor.[17a]

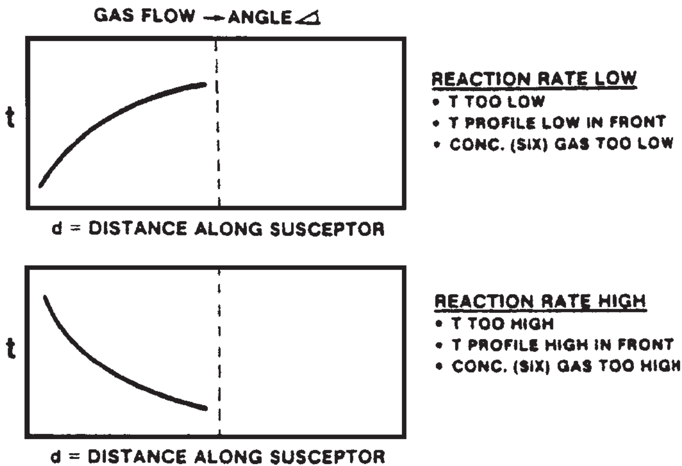



**Figure 10.** Process adjustments for correcting thickness variations in the front half of the horizontal reactor.[17a]

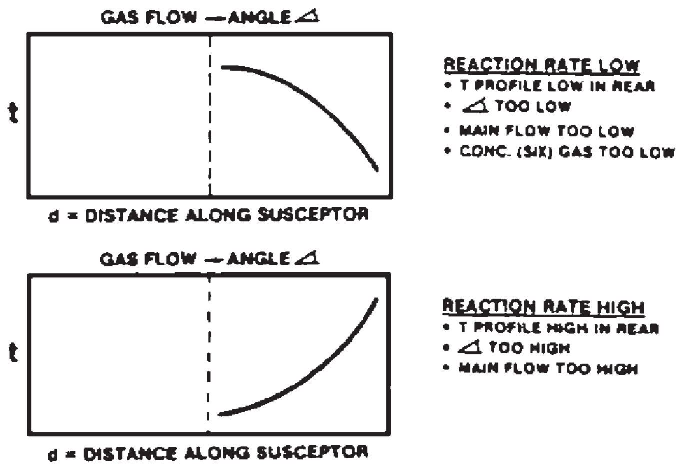



**Figure 11.** Process adjustments for correcting thickness variations in the back half of the horizontal reactor.[17a]

## 6.2 Cylinder Reactor

Corrective action for the cylinder reactor is presented in Fig. 12. In this reactor configuration, thickness is increased in the front (top of carrier) by increasing the temperature and/or concentration of reactant. Thickness is increased in the back (bottom of carrier) by increasing the total flow rate, directing the gas jets in a more downward direction, and bringing the back pressure toward a more positive value. Thickness within a wafer from left to right is improved by balancing the two jet flows, by lowering the temperature to make the overall reaction become more surface reaction rate controlled and less dependent upon rate of arrival, and by increasing the distance between the flat wafer surface and the curved bell jar. Reducing the process pressure can cause the process gas to heat more slowly, and thereby, decrease the thickness in front and increase the thickness at the back. Thickness variation at any distance along the carrier is averaged by rotation.[17b]

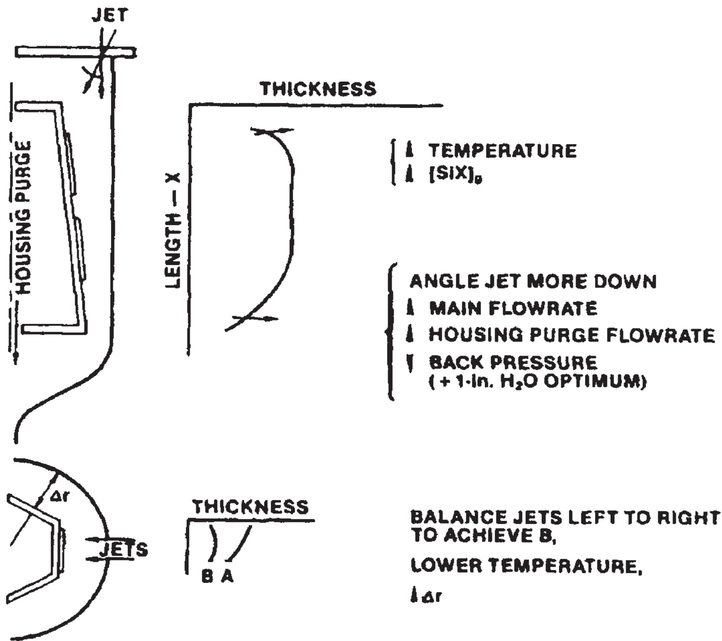



**Figure 12.** Process adjustments for correcting thickness variations in the cylinder reactor.[17b]

## 6.3 Vertical Reactor

Vertical epitaxy reactor behavior is depicted in Fig. 13. Thickness variation at any radius is averaged by rotation of the susceptor. The radial variation is a function of total flow rate and tends to have an optimum value of flow rate for a particular reactor configuration. For low total flow rates, the thickness tends to be thin to the outside, and for high total flow rates, the thickness tends to be thick toward the outside.[17c]

Assuming that the total flow rate is approximately optimum for a particular vertical reactor configuration, Fig. 14 analyzes further effects on thickness uniformity in a vertical reactor. To correct thick on the outside and thin on the inside, one must reduce the reaction rate on the outside by lowering the total flow rate, decreasing the concentration of reactants, and/ or lowering the temperature. To correct the opposite situation, one must make the opposite changes. When optimized, the vertical reactor should be thin on the inside and outside, and thickness uniformities of ±1–3% are possible.[33]

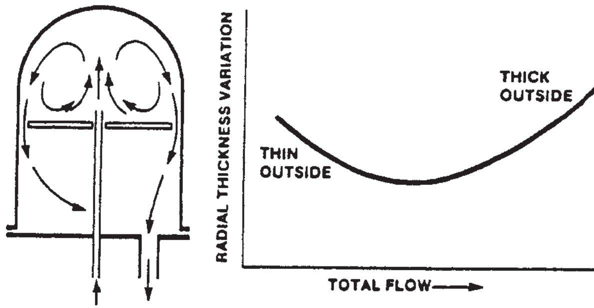



**Figure 13.** Effect of total flow rate on thickness variation in the vertical reactor.[18]

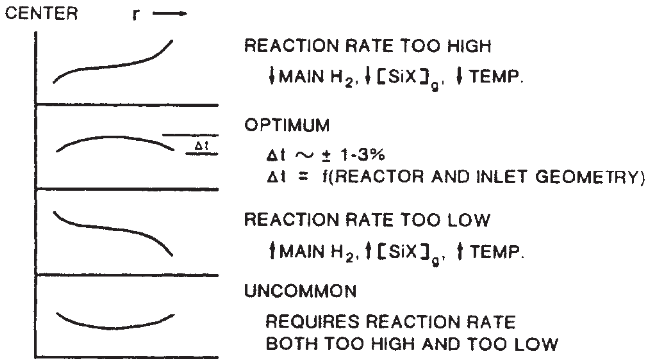



**Figure 14.** Process adjustments for correcting thickness variations in the vertical.[18]

Being thick on the inside and outside at the same time is uncommon with a vertical reactor because that profile requires the reaction rate to be too high at the inside and outside of the carrier at the same time. Such a radical thickness profile is normally an indication of not having a flat temperature profile. Depending upon the total flow rate, temperature, and reactant concentration, the temperature can be too high on either the inside or outside of the wafer carrier to achieve this thickness profile.

## 6.4 Control of Variables

The operator variables of flow rate, gas composition, temperature, temperature profile, and reactant chemistry are primary control items for any reactor geometry. Table 3 lists the primary control items for reactor design variables and notes the importance of each for the three different commercial reactor geometries.

**Table 3.** Thickness Adjustment Variables

| Variable | Vertical | Horizontal | Cylinder |
|---|---|---|---|
| tilt angle | NA | major | major, fixed |
| gas inlet | varies | minor | major |
| wafer/carrier | recessed | recessed | recessed |
| wafer/wall | minor | major | major |
| exhaust pressure | minor | minor | major |

Tilt angle is not applicable to the vertical, is a major adjustment parameter for the horizontal, and is a major but fixed item in the cylinder. The gas inlet system is a major adjustment parameter for cylinder but is less important for the vertical and horizontal systems.

For all reactors, the wafers usually reside in recessed pockets because the recessed pockets prevent the wafers from moving when being unloaded; thereby minimizing generation of particles. Edge crown and crystallographic slip can also be prevented by appropriate design of the recessed pockets.[18]

Spacing between the wafer and the reactor wall is a minor parameter in vertical reactors because the wall is so far away from the wafer. In horizontal and cylinder reactors, the wafer/wall spacing is a major parameter because the distance is short and the local gas velocity is directly controlled by this spacing.

Exhaust pressure is a major adjustment parameter for the cylinder because it directly affects the local gas velocity at the bottom of the susceptor. If the exhaust pressure is too low, the gas inlet jet apparently goes directly into the exhaust region and does not circle back up into the process space. As a result, the growth rate is reduced near the bottom of the susceptor.

Adjustment parameters for the tapered cavity reactor illustrated in Fig. 4 generally follow those for the horizontal reactor. Rotation of the circular cluster of tapered cavities averages the initial velocities and concentrations from multiple gas inlets.

## 7.0 EQUIPMENT CONSIDERATIONS FOR SILICON EPITAXY

The silicon epitaxy process requires control of:

- reaction temperature
- wafer temperature
- reactant concentrations
- process sequence
- reactor pressure
- carrier temperature gradient
- total flow rate and velocity
- exhaust effluents

Equipment design must include consideration of:

- operator safety
- process reliability
- automation
- operator convenience
- clean air load/unload
- maintenance access

A silicon epitaxy reactor is a complex assembly of subsystems including:

- power supply
- gas flow control
- cabinetry
- exhaust treatment
- reaction chamber
- wafer carrier

- automation
- gas supply

The reactor chamber geometry has already been reviewed. Here, gas flow control, power supply, temperature measurement/control, and some wafer carrier effects will be reviewed. Cabinetry, automation, exhaust treatment, gas supply and other subsystems are vital parts of an epitaxy reactor system; however, they will not be discussed in this chapter.

## 7.1 Gas Control System

The silicon epitaxy process requires precise control of the mainstream $H_2$, etching gas, silicon source gas, and dopant, while maintaining appropriate purge flows in various parts of the reactor. Provision must be made to vent the process gases without directing them through the process chamber to avoid contaminating that space with excessive dopant or unwanted silicon gas. This venting capability is often used just before depositing with a process gas to provide fresh gas to the process space.

Gas flow control is one of the most critical subsystems. Gas shutoff must be better than $10^{-6}$ $cm^3/sec$ to eliminate process problems, and multiple gaseous and liquid sources must be precisely controlled. Gas compositions must be maintained with less than ±1% variation because reaction rates are generally proportional to composition. In addition, the plumbing system must safely handle noxious, corrosive, poisonous, pyrophoric, and flammable gases.[19] Passivated 316 stainless steel is required for all plumbing components. Some consideration has been given to using more exotic metals such as Ta or Ni alloys. In general, these metals are only marginally more corrosion resistant against wet HCl than 316 stainless steel. If the plumbing system is kept clean, leak-free, and dry, there is little or no performance advantage to working with exotic metal alloys. If wet atmosphere is allowed to leak into a chlorine-containing line, corrosion products will contaminate the deposition, regardless of what alloy is being used.

## 7.2 Leak Testing

Leak-tight plumbing is absolutely essential for epitaxy reactor gas systems. Leak testing techniques include bubble testing with sensitive detergent solutions, He mass spectrometers, high sensitivity combustible

gas detectors, and pressure decay techniques. Soap bubble testing is useful but is not very sensitive, inside of the plumbing system if large leaks are present when the detergent solution is applied. He mass spectrometers offer excellent sensitivity and highly localized detection sensitivity. Unfortunately, He mass spectrometers are complex, require considerable operator training, and are relatively expensive. Highly sensitive combustible gas detectors can provide a lower cost portable method of leak detecting; however, the He mass spectrometer provides the most sensitive leak detection technique.

Leak testing individual components and joints in a system is useful; however, pressure decay testing assures that no leaking joint has been overlooked. For a leak rate specified in atmosphere $cm^3$/sec, the leak rate of a system is measured by pressure decay as follows:[20]

Eq. (1)

$$\text{Leak rate}\left(\text{atms cm}^3/\text{sec}\right)=\frac{\left(\text{pressure change}\right)\left(\text{system volume in atms cm}^3\right)}{\left(\text{absolute pressure}\right)\left(\text{time in seconds}\right)}$$

The purity of the $H_2$ supply must be considered along with the system leak rate for the silicon epitaxy process. Assuming that the $H_2$ supply has approximately 1 part per million (ppm) combined oxidizer and that the epitaxy process requires less than 2 ppm, then the entire gas control system and reactor chamber seal must add less than 1 ppm to the process gas. For a mainstream flow rate of 100 liters/minute operating in a displacement flow mode, the total system leak rate must be less than $2 \times 10^{-3}$ $cm^3$/sec in order to maintain the required oxidizer concentration of less than 2 ppm.

Leak rates for individual components are routinely specified at less than $10^{-6}$ $cm^3$/sec; however, a collection of 100 such components can have a leak rate approaching $10^{-4}$ $cm^3$/sec. A total system leak rate of $10^{-4}$ $cm^3$/sec has been considered satisfactory; however, as processes are extended to lower temperatures where less total oxidizer can be tolerated, this specification will have to be improved.

For a plumbing system with 500 $cm^3$ total internal volume, a pressure decay of 0.45 psig from 30 psig (45 psia) in 16 hours (57,600 seconds) corresponds to a leak rate of approximately $10^{-4}$ atms $cm^3$/sec (5 $cm^3$/57,600 seconds). For relatively small volumes incorporating less than 100 feet of 0.25-in tubing at 5$cm^3$/ft, pressure decay is a useful leak

checking procedure. For volumes exceeding 500 $cm^3$, the time of measurement or the resolution of pressure difference must be substantially increased to be able to measure meaningful leak rates. A more effective approach for complex systems is to divide the system into several sections, each having less than 500 $cm^3$ total volume. For a plumbing section with 100 $cm^3$ total internal volume, a pressure decay of (2.2 psig)/(45 psia) corresponds to approximately $10^{-4}$ $cm^3$/sec.

Pressure decay testing of large process volumes is not practical because the reactor walls, typically made from quartz, will not withstand high pressures, and the system volume is too great for adequate sensitivity. Pressure decay is useful as gross leak check of the process chamber; however, more sensitive He mass spectrometers or combustible gas detectors are required to properly leak check the process chamber O-ring seals.

## 7.3 Gas Flow Control

Four different methods for controlling the flow rate of individual gases in a CVD epitaxy reactor are:

- Fixed or variable orifices
- Ball-in-tube flowmeters
- Mass flow controllers
- Source controllers

Fixed or variable orifices have the advantages of being simple, reproducible, and low cost. They do not offer a read-out of flow and fixed orifices have an easily controlled dynamic range of only about 5:1 using pressure as a variable.

Ball-in-tube flowmeters offer visual read-out and a dynamic range of 10:1 at relatively low cost; however, there are numerous elastometer seals which can leak, and the units must be mounted on a front panel for observation. The calibration of a ball-in-tube flowmeter is a function of pressure within the gauge tube, and that relationship is:

Eq. (2) $$\frac{\text{Actual flow rate}}{\text{Calibrated flow rate}} = \sqrt{\frac{\text{Actual pressure in absolute units}}{\text{Calibrated pressure in absolute units}}}$$

Mass flow controllers, based on the principle of measuring mass flow using gas heat capacity, provide remote location, closed-loop control with an electronic readout, and a dynamic range of 50:1. The disadvantages of mass flow controllers are higher cost, increased complexity, and the fact that only a portion of the gas passing through the unit may actually be measured. Most mass flow controllers depend upon the performance of a by-pass orifice which can become clogged and give false readings. Nonetheless, the control, convenience, and dynamic range of mass flow controllers have led to their widespread use in gas systems.

Some chemicals, such as $SiCl_4$ and $SiHCl_3$, are liquids at room temperature with fairly high vapor pressure. These silicon source chemicals require bubblers to convert the liquid into a gas. $H_2$ is bubbled through the chemical and the quality of chemical transported is proportional to the efficiency (eff.) of the bubbler, the $H_2$ flow rate [$F(H_2)$], and the ratio of the vapor pressure of the chemical [$P$(gas)] divided by the total pressure (absolute units) within the bubbler; i.e., for $SiCl_4$:

Eq. (3)
$$F(\mathrm{SiCl_4}) = \frac{[F(\mathrm{H_2})][P(\mathrm{SiCl_4})][\mathrm{eff.}]}{\text{Total absolute pressure in the bubbler}}$$

Bubbler flow rates are often controlled by source controllers which combine an $H_2$ mass flow controller with a second sensor that measures the concentration of chemical in the combined flow stream.[21] For the most repeatable performance, bubblers require a constant temperature and pressure.

Bubbler efficiency is fixed primarily by the size of the bubbles and the path length the bubbles travel within the liquid. The smaller the bubble diameter, the closer it will be to saturation before it breaks through the liquid surface. To achieve a saturated flow stream, it is better to have many small diameter holes in the bubbler dip tube than one big hole. Because of the influence of path length, there is some reduction in chemical concentration as the liquid level in the bubbler is lowered. This reduction in concentration can be reduced by installing two bubblers in series. Chemical in the first bubbler is transported into the second, which will maintain an approximately constant liquid level. Two bubblers in series provide effective concentration control; however, the second bubbler can accumulate contamination and must be replaced and cleaned regularly.

Bubblers must be adequately sized for their total mass flow rate. Evaporation of the chemical absorbs energy, and if the heat loss caused by evaporation reduces the bubbler temperature by even a few degrees centigrade, there is a strong effect on vapor pressure.

It is critical that the "$H_2$ to Bubbler" flow line be automatically valved to turn on and off with the valve controlling the "$H_2 + SiH_xCl_y$" flow line. If the "$H_2$ to Bubbler" valve is not present, the bubbler will remain pressurized at line pressure and any reduction in $H_2$ supply pressure will cause $SiH_xCl_y$ to flow back into and contaminate the $H_2$ supply line. Pressure regulators and check valves help prevent this back flow but they should not be relied upon. White powder in the $H_2$ supply line and haze on the epitaxial surface are strong indications that silicon source liquid has leaked back into the $H_2$ supply line.

## 7.4 Dopant Flow Control

Epitaxial silicon is normally doped with the hydrides $B_2H_6$, $PH_3$, or $AsH_3$. In order to dope epitaxial layers to the 0.05–50 ohm-cm resistivity range, dopant concentrations in the process chamber are nominally $10^{-6}$ times the silicon source gas concentration.

Silicon gas and dopant are both added to the mainstream and the ratio of dopant to silicon source is an important factor in determining the concentration of dopant in the epitaxial layer. In practical application, the additions of dopant and silicon source to the mainstream are treated as totally separate and independent variables because that approach simplifies the control requirements. Graphs in Figs. 15 and 16 show how the gas phase ratio of dopant to silicon can affect the epitaxial layer impurity or dopant concentration and resistivity.[11][22]

The 25–250 ppm dopant supply must be diluted prior to joining the mainstream in order to be at the desired concentration relative to the silicon source gas.

Two different dopant dilution schemes are presented in Fig. 17. In Fig. 17(*a*), the $H_2$ flow is added, unmeasured, from a controlled pressure source to the dopant flow from the "Tank" mass flow controller. The combined gas streams pass through a gas mixer and are directed to "Inject" and "Dilute" flow controllers. The Inject flow is directed to the reactor mainstream or to vent and the Dilute flow goes directly to vent.

The dilution system in Fig. 17(*b*) adds a measured $H_2$ flow from the Dilute flow controller to the Tank flow. As before, the Inject flow goes to mainstream or vent and the unmeasured flow goes to vent through a back pressure regulator.

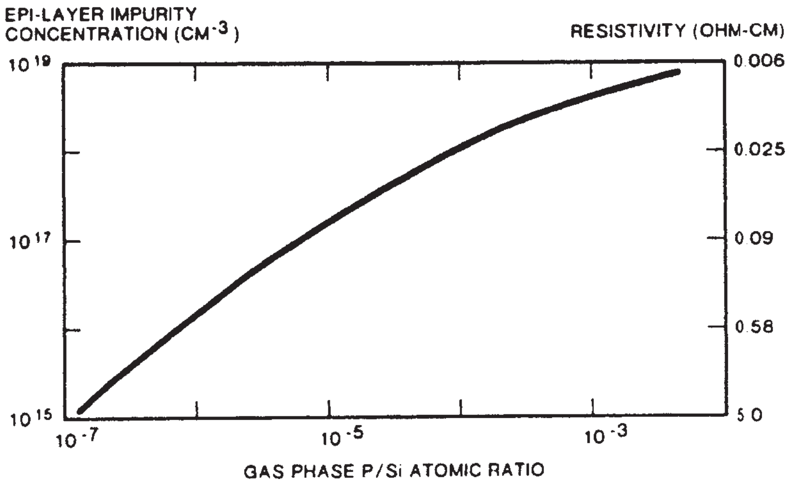



**Figure 15.** Epitaxy layer impurity concentration and resistivity versus gas phase phosphorus/silicon ratio.[22]

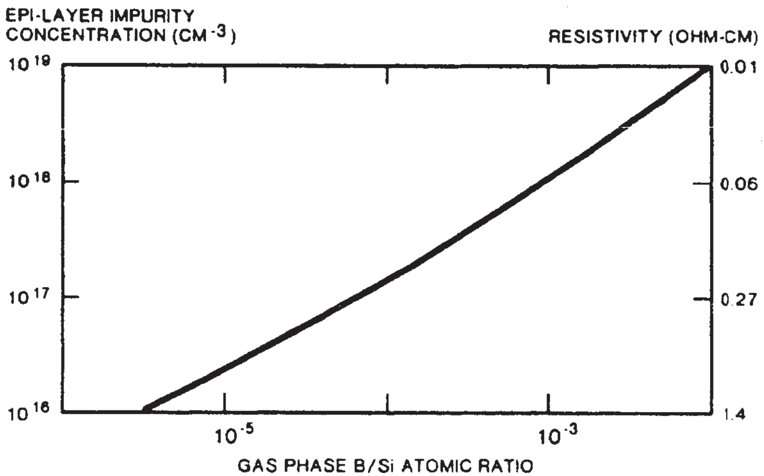
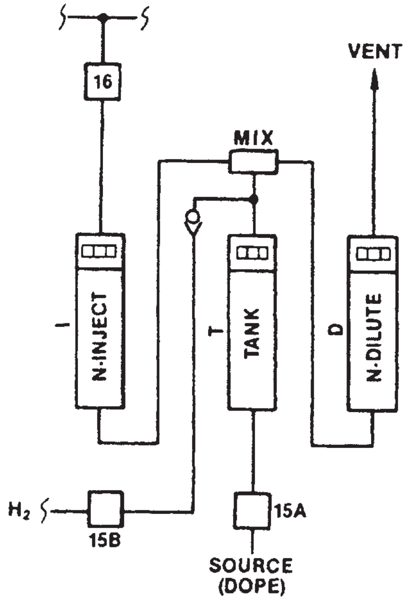
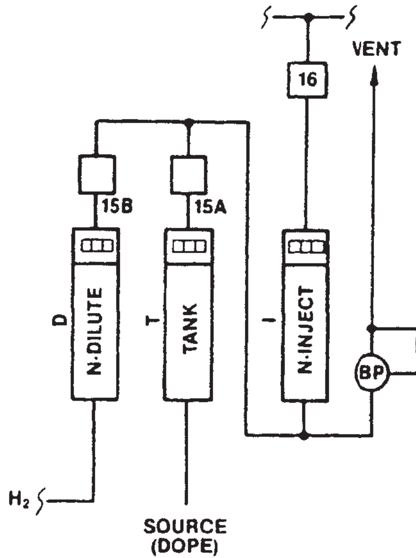



**Figure 16.** Epitaxy layer impurity concentration and resistivity versus gas phase boron/silicon ratio.[22]




(a)




(b)

**Figure 17.** Dopant dilution control systems.

Both systems perform equally well; however, most commercial systems utilize the flow schematic of Fig. 17(*a*). The thought is that the upstream pressure regulator for the unmeasured $H_2$ flow in Fig. 17(*a*). is more reliable than the back pressure regulator for the unmeasured vent flow in Fig. 17(*b*)

Mathematically, the flow of dopant *F*, already diluted in the gas cylinder to concentration *C*, passing through the Inject flow controller and into the mainstream in Fig. 17(*a*). is given by:

Eq. (4) $$F = C\frac{T}{D+I}I$$

where *D*, *T*, and *I* are the measured flows through the Dilute Tank, and Inject flow controllers, respectively, as each is defined in Fig. 17(*a*). It is important to note that the units of *F* are volume/unit time. If the Dilute flow were zero, the Inject flow values would cancel in the equation and the dopant flow *F* would simply be the concentration *C* in the gas cylinder times the tank flow rate. Similar reasoning is applied to Fig. 17(*b*), using the following equation:

Eq. (5) $$F = C\frac{T}{D+T}I$$

In commercial epitaxy reactors, it is convenient to make the Tank and Inject flow controllers have equal full scale flow rates, with the Dilute flow controller being 10–100 times that full scale value. For systems in which the mainstream flow rate is 100–500 liters/min, the Tank and Inject flow controllers are usually sized to be 300 $cm^3$/min while the Dilute controller is 30 liters/min.

When the Inject and Tank flow controllers have the same flow values for all settings, as done in the control scheme described below, the equations governing Figs. 17(*a*). and 17(*b*) become identical because the values for *I* and *T* become identical.

To a first approximation, the resistivity is inversely proportional to the dopant flow into the mainstream, assuming that all other parameters are constant. Thus, the dopant dilution equation should be exercised each time the epitaxy resistivity is altered.

One simple approach to dopant dilution is to keep the ratio of Tank to Dilute constant and vary only the Inject. This approach is limited to about a 10:1 ratio before the Tank/Dilute ratio must be changed.

For adjustment convenience over a wider range of values, an automatic dopant control system can be created by causing the Dilute, Inject, and Tank flow control setpoints to have related values that automatically adjust the dopant concentration.

In the automatic dopant control system shown schematically in Fig. 18, the Tank and Inject flow controllers always have the same setpoint and that setpoint is always inversely proportional to the Dilute setpoint. In Fig. 18, this relationship is depicted schematically by ganged slide-wide potentiometers in which the Tank and Inject setpoints move from 0 to 100% full scale while the Dilute flow controller setpoint moves from 100 to 0% full scale. These relationships can be achieved by various electronic control circuits.

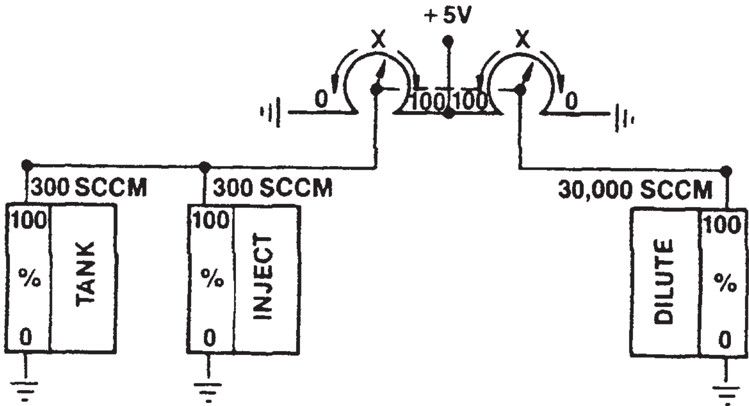



**Figure 18.** Automatic dopant control system.

If $X$ represents the intermediate setpoint controllers, with a value between 0 and l, then:

$$I = X\,I(\text{max}) = T = X\,T(\text{max})$$

$$D = (1\text{-}X)\,D(\text{max})$$

$$I(\text{max}) = T(\text{max}) = 300\ \text{cm}^3/\text{min}$$

$$D(\text{max}) = 30{,}000\ \text{cm}^3/\text{min}$$

and

Eq. (6) $$F = C\frac{T}{D+I}I$$

Therefore,

Eq. (7) $$F = C\frac{XT(\max)}{(1-X)D(\max)+XI(\max)}XI(\max)$$

But: $D(\max) = 100I(\max)$;

therefore,

Eq. (8) $$F = C\frac{X^2 \quad I(\max)^2}{D(\max) - XD(\max) + \frac{XD(\max)}{100}}XI(\max)$$

But: $I(\max)^2/D(\max) = 3$;

therefore:

Eq. (9) $$F = C\frac{X^2}{1-0.99X}3$$

With this setpoint algorithm, the dopant flow $F$ equals three times the concentration of dopant in tank $C$ times the function $X^2/(1 - 0.99\,X)$. The factor of three is an arbitrary result of the choice of the full scale flow rates of the Dilute and Inject flow controllers and is usually ignored in dopant flow calculations because changes in resistivity are usually expressed in ratios of resistivity and dopant flow.

The function, $X^2/(1 - 0.99\,X)$, has the advantage of changing from 0.0026 when $X = 0.05$ to 15 when $X = 0.95$. Thus, the dopant flow rate can be changed over a range of about 6000:1 by changing $X$ only 19:1.

The function $X^2/(1 - 0.99\,X)$ is sometimes called the dopant number and a slide rule has been created to easily ratio resistivity values with $X$ values.[23]

## 8.0 OTHER EQUIPMENT CONSIDERATIONS

### 8.1 Heating Power Supplies

Silicon epitaxy requires temperatures in the 900–1300°C range. Process limitations concerning gas purity have dictated batch operations with cooled elastomer seals; therefore, relatively rapid heating and cooling is necessary for commercially significant production.

The primary heating systems for silicon epitaxy are:

- Induction heating, using frequencies from 3 kHz to 400 kHz, with coils located internal and external to the process chamber.
- Radiant heating, using high intensity infrared heating lamps, located external to the process chamber.
- Radiant heating, using resistance heaters, located internal to the process chamber.
- Combinations of the above.

For the simple cold-wall reactor geometries illustrated in Fig. 3, power densities of 15–30 W/cm$^2$ are required to achieve the temperatures and heat/cool cycles times.

Resistance and induction heating were the first techniques to be used to achieve the high power densities required for silicon epitaxy. In the case of induction heating, the wafer carrier was directly induction heated and was properly called a susceptor. This terminology has been carried over to other heating methods and wafer carriers are often referred to as susceptors, regardless of the heating method.

Each heating method has advantages and the technique used does not significantly alter the information provided in this chapter.

### 8.2 Effect of Pressure

Prior to 1978, virtually all silicon epitaxial deposition was done at atmospheric pressure. Process pressure does affect certain properties of epitaxy films such as pattern shift and autodoping. There are process benefits for epitaxial growth in the 20–250 torr range, and these benefits are discussed in the Key Technical Issues section (Sec. 11).

In the pressure range of 5–760 torr, gas flow is characterized by viscous flow. From the fluid mechanics viewpoint and for the condition of

constant mass flow rate, there is little difference in the rate of arrival of reactants between operating at 760 torr or 5 torr absolute pressure. If the total mass flow rate is kept constant, the different effects of velocity, density, and diffusion rate balance and comments made about the effect of gas flow on deposition uniformity apply equally well for all pressures in this range. Chamber pressure, at constant total mass flow rate, can have a slight effect on how quickly the process gas is heated. A cooler gas has a lower reaction rate and this effect can be used to reduce the reaction rate at the beginning of the reaction path.

When the mean free path of a gas molecule becomes comparable to the dimensions within the process chamber, molecular diffusion is the dominant mode of mass transport. Molecular diffusion begins to be important below about 5 torr and is normally the dominant mode of mass transport below about 0.5 torr.[20]

Because epitaxy processing is usually done in the mass transport limited or rate of arrival regime, the total mass of gas passing through the reactor is kept approximately the same regardless of process pressure. The result is the number of volume changes per unit time is increased in inverse proportion to the absolute pressure. This increased number of volume changes per unit time can have a strong effect on the materials properties of the epitaxy layer, such as, pattern shift, dopant incorporation, and crystal perfection at lower temperatures.

## 8.3 Temperature Measurement

Temperatures for the silicon epitaxy process must be measured and controlled with a precision of a few degrees centigrade in the 900–1300°C range, in $H_2$ with a silicon source chemical. In these process conditions, the only convenient temperature measurement method is radiation pyrometry. Thermocouples are generally not stable in an $H_2$ environment, and most thermocouple shield materials react with silicon at high temperature.

Radiation pyrometry measures the brightness or intensity of light in a narrow range of wavelengths being emitted by the target. The intensity of radiation is related to temperature by the Stefan-Boltzmann radiation law:

Eq. (10) $$W = \varepsilon \sigma T^4$$

where $\varepsilon$ is the emissivity, $\sigma$ is the Stefan-Boltzmann constant and $T$ is the absolute temperature. If the emissivity is known, the temperature of the emitting body can be determined.[24]

Pyrometers are generally of two types:

- Disappearing filament pyrometers in which the brightness within a narrow wavelength range of a heated filament of known temperature is matched with the brightness of the target.
- Electronic pyrometers in which the intensity of light within a narrow range of wavelengths is directly measured by a photovoltaic cell or a thermopile.

The disappearing filament pyrometer operates at 0.65 micron wavelength and can provide approximately ±5°C precision. Calibration sources are available which permit absolute temperature reference.

Electronic pyrometers with silicon photocells operate in the 0.8 micron range: PbS photocells detect in the 2.2 micron range. Thermopiles are simply assemblies of thermocouples on which the radiation is focused. As such, they are broad band detectors and are easily affected by a wide range of absorptive effects. To prevent this source of imprecision, narrow band-pass optical filters are provided to minimize absorptive effects.

The emissivity of silicon ranges from 0.48 to 0.60[25] for a light wavelength of 0.65 micron, while that of SiC-coated graphite is slightly higher. Emissivities are a function of wavelength and generally increase for longer wavelengths. In the 2.2 micron range, the emissivity of silicon is approximately 0.70 for temperatures above 600°C. Below 600°C, the emissivity of Si is a strong function of temperature for wavelengths of 1–5 microns.[26]

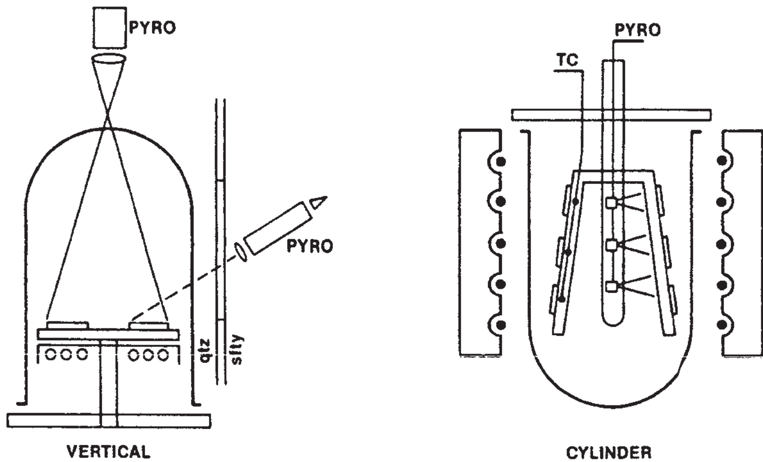
Optical temperature measurements are further complicated by absorption effects of reactor walls, safety glass windows, and deposits on the reactor wall.

Figure 19 illustrates two configurations for optical radiation pyrometry in epitaxy reactors. In the case of the vertical reactor, an electronic radiation pyrometer is located above the bell jar and has a wide field of focus on top of the susceptor. A window is provided in the cabinetry to permit separate observation and calibration with a hand-held pyrometer. For this configuration, the pyrometer above the jar will be somewhat sensitive to load because the emissivity of rough polycrystalline silicon is slightly greater than polished single crystal. This pyrometer configuration

is also sensitive to bell jar coating. In an improved version, fiber optics are inserted through the baseplate to measure the temperature of the bottom of the susceptor.

For the radiantly heated cylinder reactor in Fig. 19, electronic pyrometers are located inside the wafer carrier, within a cooled and purged quartz tube. For calibration, a thermocouple can be inserted into a special wafer carrier plate. When the thermocouple is in place, the carrier cannot be rotated and the averaging effect of rotation cannot be observed. In this pyrometer configuration, deposits on the quartz tube will alter the measurement accuracy.

Because of reflected light having the same wavelength that the pyrometer is using, it is difficult to measure temperature in a radiantly heated reactor with a pyrometer aimed at the same surface heated by the radiation source. As a practical matter, pyrometers using a nominally 2.2 micron wavelength are acceptable for this application because the radiant heat lamps have very little radiation with wavelengths longer than 2 microns.




$$T_{TRUE} = T_{obs} + \Delta T_{\epsilon} + \underbrace{\Delta T_{qtz} + \Delta T_{slty}}_{\Delta T_{abs}}$$

$$T_{TRUE} = T_{TC} + DT_{G} + \Delta T_{gap} + \Delta T_{W}$$

**Figure 19.** Optical pyrometer configurations for the vertical and cylinder reactors.

## 8.4 Backside Transfer

While the CVD process takes place on the face of the wafer, chemical activity also occurs between the wafer and its carrier. If silicon has been deposited on the carrier where a wafer is to be placed, and if the wafer is cooler than the carrier during process, then it is possible for silicon to be transferred from the carrier to the cooler wafer. This transfer is driven by the temperature difference, and its rate is significantly enhanced by the presence of chlorine which creates volatile silicon compounds in the space between the wafer and the carrier. If the wafer is hotter than the carrier, then chlorine can promote the transfer from the wafer to the cooler carrier.

The method of heating directly affects the relative temperature between the wafer and its carrier. As noted in Fig. 20, when the wafer is located on the same side of the carrier as the radiant heat source, the wafer is hotter than its carrier and the backside of the wafer can be etched during process. For heavily doped substrates, this etching can release dopant into the process space. This backside transfer/etch process occurs more rapidly at higher temperatures because of greater temperature differences and faster chemical reaction rates.

When the wafer carrier is directly heated, as with induction heating, the wafer is usually cooler than the carrier, and backside transfer of silicon occurs. If the substrate is heavily doped, this backside transfer will partially seal the back of the wafer.

Where wafer flatness is critical, backside transfer can be undesirable. Backside transfer is reduced by depositing at lower temperatures and by operating with less chlorine in the process gas. Careful placement of a wafer into the pocket formed by the previous wafer can prevent such transfer.

In the tapered cavity reactor described in Fig. 4, the wafers facing each other across the cavity are at nearly the same temperature as their carriers, and conditions can be adjusted so that neither backside transfer or backside etching occurs.

If a back-seal is required for resistivity control, it should be applied during the wafer making process. Adding oxide, nitride, or polycrystalline Si to the back of a polished wafer usually leads to unacceptable defect densities in the epitaxial layer caused by front surface damage.

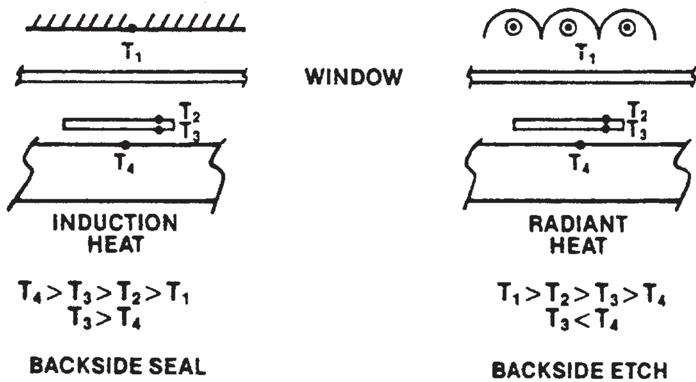



**Figure 20.** Wafer/carrier temperature difference as a function of heating method.

## 8.5 Intrinsic Resistivity

Intrinsic resistivity is the doping level from the reactor when no dopant is supplied in the gas stream during deposition. Doping silicon is an algebraically additive process; therefore, the intrinsic doping level must be substantially less than the intentional doping level to achieve resistivity control.

Unwanted dopant comes from inadequately purified wafer carriers, dopant in the silicon source gases, thermal degradation of seal o-rings, residual dopant in the wafer carrier from prior heavily doped runs, and contamination such as vacuum grease touching hot parts. Insufficiently purified graphite and vacuum grease normally contribute *p*-type dopant to the background while gas contamination is usually *n*-type.

Individual wafers can also be contaminated by such sources as sputtering from ion-implant hardware, spin-on dopant solutions, and Al scratched onto the wafer during handling.

Intrinsic resistivities should be at least ten times the intentional level in order to maintain adequate control. The intrinsic resistivity value of a clean epitaxy reactor should exceed 100 ohm-cm *n*-type and values of 100–1000 ohm-cm are often obtained.

### 8.6 Phantom *p*-Type Layer

Most bipolar ICs require an *n*-type epitaxial layer over $n^+$ buried layer regions. Unwanted *p*-type contamination can create a so-called phantom *p*-layer in the epitaxial silicon which can be observed by groove and stain or by spreading resistance probe profiles. Sources of this unwanted *p*-type contamination include:

- A low *p*-type intrinsic resistivity caused by the contamination sources described above.
- A *p*-type contamination (usually B) in the substrate due to use of contaminated remelt during crystal pulling (especially true for heavily doped *n*-type substrates).
- A *p*-type contamination from the doping technique used to create the buried layer.
- A *p*-type contamination coming from B in a dual B/As buried layer structure.
- A *p*-type contamination coming from $Al_2O_3$ used in some $H_2$, purifiers.

Intrinsic resistivities and spreading resistance probe profiles should be measured and recorded on a regular basis so that the origin of phantom *p*-layers can be determined when they occur.

## 9.0 DEFECTS IN EPITAXY LAYERS

Defects in silicon epitaxy layers include:

- haze
- pits
- orange peel
- faceted growth
- edge crown
- slip dislocations
- growth dislocations
- stacking faults

- spikes and hillocks
- shallow pits

Methods for observing and measuring these defects are described in Ref. 6.

**Haze.** Haze, as revealed by reflected light, is a fine pitting or slightly textured surface caused by oxidizer in the process space or by subsurface crystal damage in the substrate. To cure or reduce haze, eliminate all sources of oxidizer (such as air leaks), verify the purity of the $H^2$, extend purge times, hold reactor at 850°C during heat-up to dry it out before proceeding, and increase the deposition temperature.

**Pits.** Pits are localized etching of substrate defects or local inhibition of epitaxy growth, often caused by contamination left on the surface prior to heat-up. Improving the pre-epitaxy clean, extending the HCl time, increasing the HCl etch temperature, and verifying the HCl purity are steps to prevent pitting.

**Orange Peel.** Orange peel is a roughened surface appearance caused by having the growth rate too high for the deposition temperature. Subsurface crystal damage can also cause orange peel. Increasing the temperature and lowering the growth rate will reduce orange peel if the wafers have been correctly polished.

**Faceted Growth.** Faceted growth is irregular, stepped growth over the surface that is caused by growing on (111) faces cut on-orientation. Substrates should be cut 3–5 degrees off the (111) plane towards the nearest (110) plane for smooth growth. Epitaxial growth on the (100) plane does not have this problem.[1a][1b][2c][2d][27]

**Edge Crown.** Edge crown occurs when the growth rate at the edge of the wafer greatly exceeds that over the rest of the wafer surface. Edge crown is caused by local convection currents at the edge of the wafer and by growth enhancement due to a sharp wafer edge. Recessed wafer pockets and edge rounding will eliminate edge crown.

**Etch Pits.** Etch pits created by decorative etch techniques reveal crystal dislocations produced by slip, as well as other defects. Crystallographic slip can be distinguished from other dislocations because the bases of the etch pits caused by slip [triangles for (111) and squares for (100) surfaces] lay on a common line.

**Slips.** Crystallographic slip during epitaxial deposition is dislocation motion in response to thermal stress. Slip can be reduced by uniform heating of the wafer, and operating at lower temperatures where the wafer is stronger. Defects at the wafer edge can be a major source for dislocation generation. Rounded and defect-free edges are essential for slip-free epitaxy.

**Stacking Faults.** Stacking faults are geometric defects nucleated at crystallographically disturbed sites on or near the growth surface. A uniform size of stacking faults indicates that the disturbance was all at the original surface prior to epitaxy. In this case, the likely candidate is residual oxide which survived the pre-epitaxy clean and $H_2$ bake, or which was created in the reactor during heat-up. Stacking faults of varying size indicate that foreign matter or particles were being generated during the deposition cycle.

For stacking faults that originate at the original wafer surface, the length $L$ of the side of the fault is related to the thickness $t$ of the epitaxy layer as follows:[28]

- For (111) planes: $t = 0.816\,L$
- For (100) planes: $t = 0.707\,L$

Cleaning the wafer surface, eliminating sources of particulate or other foreign matter, and increasing the deposition temperature all help to reduce stacking fault density.[29]

**Spikes and Hillocks.** Mounds, tripyramids, hillocks, and spikes are more severe defects also caused by crystallographically disturbed sites. The greater the disturbance, the more severe the defect. The larger defects are usually the result of particle contamination generated by scraping the wafer on the carrier during loading and/or particles coming from dirty surfaces such as the reactor walls.

**Shallow Pits.** Shallow pits or haze revealed by decorative etching alone or decorative etching following an oxidation cycle indicate the presence of heavy metal precipitates.[30] Clean, dry plumbing does not contribute measurable amounts of metal contamination; however, any corrosion in the plumbing or inside the reactor can cause metal contamination. Other sources of metal contamination include the use of metal tweezers, metal spinner chucks in pre-epi clean, or sputtering from the wall of a plasma etcher or ion implanter.

## 10.0 SAFETY

The epitaxy process and reactor utilize several hazardous items, including gases which are flammable, noxious, poisonous, corrosive, and pyrophoric; high voltages; and chemicals which are strongly oxidizing or flammable.

Table 4 lists some of the common gases used in the epitaxy and CVD processes, together with information about their relative hazard. A well thought-out safety plan, in combination with good ventilation is essential to safe operation.

Good safety practice requires knowledge of the hazards involved, a well-developed preventive action plan, awareness of the specific safety plan that has been developed for the area, and a trained reaction to unexpected events. Many safety plans are not well thought out, do not make available the necessary information, and do not reinforce the plan with sufficient practice.

References 6 and 31 provide further information regarding CVD safety practice.

## 11.0 KEY TECHNICAL ISSUES

The key technical issues for commercial silicon epitaxy are productivity/cost, uniformity/quality, autodoping/buried layer control, and new materials technology.

### 11.1 Productivity/Cost

The maximum reactor productivity,

Eq. (11) $$P_{(\max)} = \frac{\text{runs}}{\text{hr}} \; \frac{\text{wafers}}{\text{run}} \; \frac{\text{area}}{\text{wafer}}$$

must be derated by the factors of yield, uptime, and utilization. Yield to commercial specification is typically 90%; uptime is approximately 70–95%, and utilization is 50–70%, for a total derating of approximately 50%. Utilization of the reactor includes time lost for scheduling (3–7%), etch/cost (5–20%), test runs (3–10%), test wafers in place of production material (2–15%), and facilities downtime (3–10%).[32]

**Table 4.** CVD Gas Safety Summary

| Gas | Flammable % In Air | Pyrophoric % In Air Auto Ignition °C | PPM Lethal Few Min. | PPM Lethal Few Hrs. | PPM Irritant Level | PPM Approx. Odor Level | PPM 8 Hour TLV | Comments |
|---|---|---|---|---|---|---|---|---|
| $AsH_3$ | Yes | ? | 250 | 6 | – | 1 | 0.05 | Highly poisonous |
| $PH_3$ | Yes | 40-50 | 2,000 | 100 | 8 | 2 | 0.3 | Highly poisonous |
| $B_2H_6$ | 0.8–88 | 37–52 | 160? | ? | – | 3 | 0.1 | Highly poisonous |
| $NH_3$ | 15-28 | 650 | 30,000 | – | 25 | 5 | 50 | Reacts strongly with chlorides. |
| $N_2O$ | Supports Combustion | non- | ? | – | 100 | 10 | 5 | Anesthetic. Possible nerve damage. |
| $NO_2/N_2O_4$ | Supports Combustion | non- | 200? | – | 60 | 10 | 5 | |
| $CO_2$ | No | non- | ? | 20,000 | – | – | 5,000 | |
| $O_2$ | No | non- | non- | – | – | – | – | Keep separate from reducers. Supports fierce combustion. |
| $SiH_4$ | Yes | 0.5% $SiH_4/H_2$<br>4% $SiH_4/N_2$ | non- | non- | ? | – | 0.5 | Forms fine silica dust and vigorous flame. |
| $SiH_2Cl_2$<br>$SiHCl_3$, $SiCl_4$ | No | – | ? | ~8,000 | ~10 | ~1 | – | Decomposes to HCl and $SiO_2$ in air. |
| $H_2$ | 4-80 | 585 | Asphyxiant | – | non- | non- | – | Store <2000 $ft^3$ in building. |
| $N_2$ | No | – | Asphyxiant | – | non- | non- | – | |
| HCl | No | – | 1,300 | 1,000 | 10 | 1 | 5 | Noxious |
| HF | No | – | 100(?) | ? | ~30 | ? | 3 | Noxious |

*See Reference 31a.

The typical epitaxy process sequence listed in Fig. 21 is accomplished in approximately 60 minutes; however, the epitaxy process can be divided into steps which require the heating power supply to be on and those which do not. A system designed with two process chambers that time-share a single power supply can process up to 1.8 times the number of runs that a single chamber system can produce.[32]

To understand epitaxy cost per unit area, it is useful to include the various factors as follows:

Eq. (12) $$\frac{\text{cost}}{\text{area}} = \frac{\text{fixed cost} + \text{variable cost}}{\text{hour}} \times \frac{\text{hour}}{\text{area processed}}$$

Fixed cost includes all amortized items such as system price, installation, initial spare parts, and facilities allocations which continue whether the reactor is utilized or not. Variable costs only include those items directly related to system operation such as chemicals, wafers, power, labor, and maintenance.

RUNS/HOUR

| STEP | SINGLE CHAMBER SMALL LOAD (MINUTES) | SINGLE CHAMBER LARGE LOAD (MINUTES) | DUAL CHAMBER LARGE OR SMALL LOAD SIZE, MAIN POWER OFF (MINUTES) | DUAL CHAMBER LARGE OR SMALL LOAD SIZE, MAIN POWER ON (MINUTES) |
|---|---|---|---|---|
| UNLOAD/LOAD | 9 | 11 | 9-11 | - |
| $N_2/H_2$ PURGE | 2 | 2 | 2 | - |
| HEAT TO 1120°C | 12 | 12 | - | 12 |
| ETCH | 2 | 2 | - | 2 |
| CLEAR | 1 | 1 | - | 1 |
| HEAT TO 1060°C | 2 | 2 | - | 2 |
| DEPOSITION | 15 | 15 | - | 15 |
| CLEAR | 1 | 1 | - | 15 |
| $H_2$ COOL | 6 | 12 | 6-12 | - |
| $H_2/N_2$ PURGE | 2 | 2 | 2 | - |
| TOTAL | 53 | 60 | 19-27 | 33 |
| RUNS/HR | 1.1 | 1.0 | | 1.8 |

**Figure 21.** Typical epitaxial silicon process sequence for single and dual chamber silicon epitaxy reactors.

An epitaxy reactor must be sized for the production requirement. If the system is not fully utilized, the fixed costs become very high per unit area.

For a typical reactor having a total amortized value of $1,200,000, the fixed cost per hour will range from $15 to $200 per hour, depending upon the period of depreciation, with the typical value being about $50 per hour.[32]

Variable (operating) costs are summarized in Fig. 22. When maintenance labor is considered, the hourly cost of repair/maintenance is about equal to the operating cost; therefore, it is convenient to use $50–$75/hour as a constant variable cost, whether the system is in an operational or maintenance mode.

| ITEM | TYPICAL COST/HOUR |
|---|---|
| PROCESS GAS | $12 to $16 |
| POWER | $6 to $12 |
| CONSUMABLES | $8 to $12 |
| TEST WAFERS | $5 to $10 |
| LOADED LABOR RATE | $19 to $25 |
| TOTAL (EXCLUDING MAINTENANCE) | $50 to $75 |
| LOADED MAINTENANCE LABOR RATE | $50 to $75 |

**Figure 22.** Typical epitaxy reactor operating costs.[32]

Combined fixed and variable costs are $100–$125/hour for a typical reactor in 1986 dollars. Other factory costs add $25–$50/hour. With a maximum productivity of 10–20 wafers/hour and a 50% derating factor, the manufacturing cost of silicon epitaxy is approximately $20 per 125–150 mm diameter wafer. Substrate cost, including yield loss and test wafers, brings the manufacturing cost of an epitaxy wafer to the $40–$50 range. Non-manufacturing costs, plant utilization, and profit further increases the market price of a 125–150 mm diameter epitaxy wafer to $75–$100, in 1986 US dollars.

Epitaxy cost is expected to be reduced during the late 1980s as more productive reactors are put into service and better utilization is achieved through centralized operations, especially where buried layer patterns are not required.[4][15]

## 11.2 Uniformity/Quality

Uniformity and quality are the most important technological aspects of silicon epitaxy because device performance often depends directly upon these factors.

Thickness uniformity of ±2–4% and resistivity uniformity of ±4–10% are available in commercial systems.[33] Such capability is more than adequate for most device applications.

Statistical techniques can be used to characterize variations in film properties. Average and standard deviation are well known concepts; however, results are often expressed as $\pm xy\%$ without specifying the definitions, as was done in the paragraph above.

The uniformities noted above are for 90% of all points measured. Another specification frequently used is the total variation from maximum to minimum value, expressed as $\pm xy\%$ of the average. The maximum-minimum variation is easily calculated from the formula:

Eq. (13) $$\pm \text{ variation } \% = \frac{\text{max - min}}{\text{max} + \text{min}} \frac{\%}{100}$$

The term "90% of all data points" can be directly related to the standard deviation. Assuming there is a normal distribution of data, "90% of all data points" would be equal to 1.64 standard deviations. The maximum-minimum variation is not directly related to statistical calculations; however, three standard deviations will normally include 99.6% of the data points.

Epitaxy quality includes crystal and surface defects, as well as metallic contamination. Causes and cures for these defects are discussed in an earlier section.

## 11.3 Buried Layer Pattern Transfer

Buried layer pattern transfer[27] is vital to the construction of bipolar integrated circuits. The buried layer (actually a pattern of heavily doped

regions in the original substrate surface) is created in the wafer surface before epitaxial growth to provide low resistance paths for the collectors of the bipolar transistors. If the subsequent patterns are not aligned directly above these buried layer patterns, the transistors will not operate to specification.

Buried layer patterns in the wafer surface are created because the oxidation rate is higher in areas where the dopant concentration is higher. When the oxide is removed after buried layer diffusion, the higher oxidation rate leaves depressions in the wafer surface over each buried layer region. These depressions are used to align subsequent masks in the creation of an IC.

Because of different growth rates in different crystallographic directions, the buried layer patterns can be shifted relative to the region of high doping, and the pattern can be distorted or washed out. Figure 23 describes the various possibilities of symmetrical and unsymmetrical distortion with and without size change.[27a][27b]

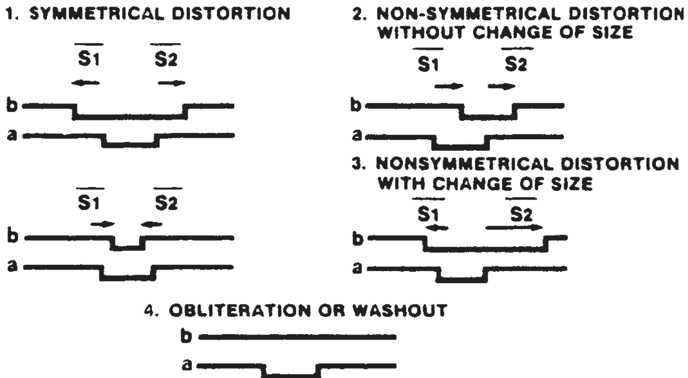



**Figure 23.** Possibilities for epitaxy buried layer pattern shift/distortion.[27a][27b]

Pattern distortion is a change in size of the original pattern dimensions, often accompanied by sidewall faceting. Patterns can enlarge, shrink, facet and virtually disappear, depending upon the deposition conditions and orientation of the wafer. Pattern distortion occurs:

- With symmetrical pattern shift on off-orientation (111) surfaces, when the off-orientation is in the direction of the nearest (110) plane

- With unsymmetrical pattern shift on off-orientation (100) surfaces
- Without pattern shift on on-orientation (100) surfaces

Pattern distortion is reduced by:

- Decreasing the chlorine concentration in the depositing gas
- Increasing the growth temperature
- Decreasing the growth pressure

Pattern shift is the motion of the surface pattern relative to the heavily doped buried layer region. The pattern shift ratio is the amount of shift divided by the thickness of the epitaxy layer. Pattern shift must be controlled to permit accurate registry of subsequent masks with the actual buried layer pattern. A zero pattern shift ratio is desirable but it is not achieved in commercial production except by reduced pressure deposition. A pattern shift ratios of 1:1 to 1.5:1 are commonly utilized.

When a wafer is cut from a (111) oriented crystal, it is cut in a specific off-orientation direction, as depicted in Fig. 24.[27f] This orientation off the (111) plane toward the nearest (110) plane eliminates orange peel surface growth and provides for symmetric pattern shift during epitaxy growth. It is convenient to note that the symmetry of a dislocation etch pit reflects the symmetry of the off-orientation cut, as shown in Fig. 24. This observation provides a useful test for incorrect off-orientation wafers.

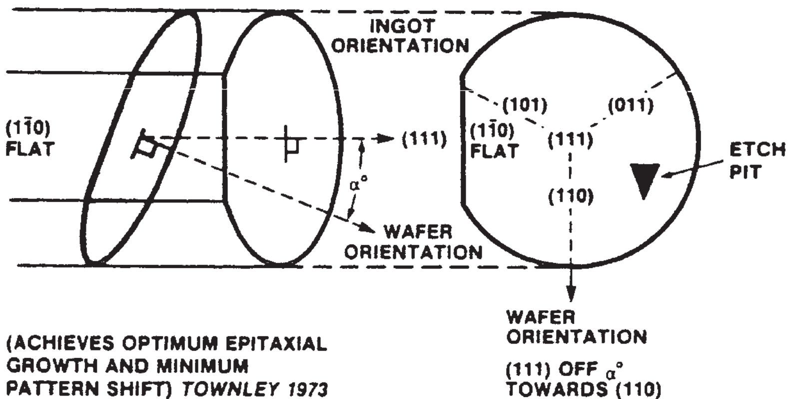



**Figure 24.** Off-orientation (111) wafer cut from (111) crystal ingot.[27f]

For atmospheric pressure deposition, pattern shift is minimized by:

- Orienting (111) plane 3–5 degrees toward the nearest (110) plane
- Orienting the (100) plane parallel to the wafer surface within ± 0.15 degrees
- Reducing the growth rate
- Increasing the growth temperature
- Reducing the growth pressure
- Reducing the chlorine content of the process gas

Fortunately, the conditions for reducing pattern shift are essentially the same as those for reducing pattern distortion, except that pattern distortion can be significant for on-orientation (100) surfaces.

$SiH_4$ offers the best results in terms of reduced pattern shift and distortion; however, the $SiH_4$ growth rate is normally less than 0.25 micron/minute because of bell jar coating and gas phase reactions.

For epitaxy layers thicker than about 1.5 microns, the best compromise is considered to be $SiH_2Cl_2$, operating at reduced pressure with growth rates in the 0.3–0.5 micron/minute range. For epitaxy layers less than 1.5 microns, $SiH_4$ offers the advantage of lower temperature and the disadvantage of being more sensitive to oxidizer leaks.

For lower growth pressures, pattern shift occurs to a lesser degree, becomes zero, and then becomes "negative," in that the pattern shift is in the direction opposite that for atmospheric pressure. The effect of pattern shift on pressure is illustrated in Fig. 25[34] where "negative" pattern shift was found for pressures below 100 torr at 0.3 micron/minute using $SiH_2Cl_2$, at 1080°C in a cylinder reactor. Because of the "negative" pattern shift concept, process changes that "reduce" pattern shift must be considered in the algebraic sense. That is, if "negative" pattern shift is present, process changes that would "increase" pattern shift would actually cause the "negative" shift to be closer to zero. Process changes that would "decrease" pattern shift will actually cause "negative" pattern shift to become more "negative" or further from zero.

Pattern shift ratios versus pressure are provided in Fig. 26 for a radiantly heated cylinder and an induction heated vertical reactor.[35] For pattern shift ratios above zero, decreasing the pressure and growth rate brings the shift closer to zero. For pattern shift ratios below zero, increasing the pressure and growth rate bring the shift closer to zero.

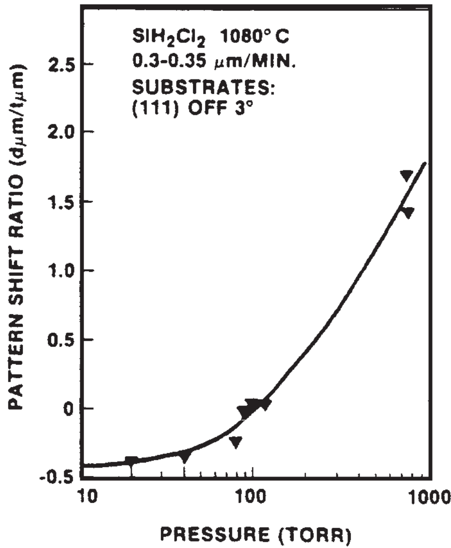



**Figure 25.** Effect of pressure on pattern shift ratio.[34]

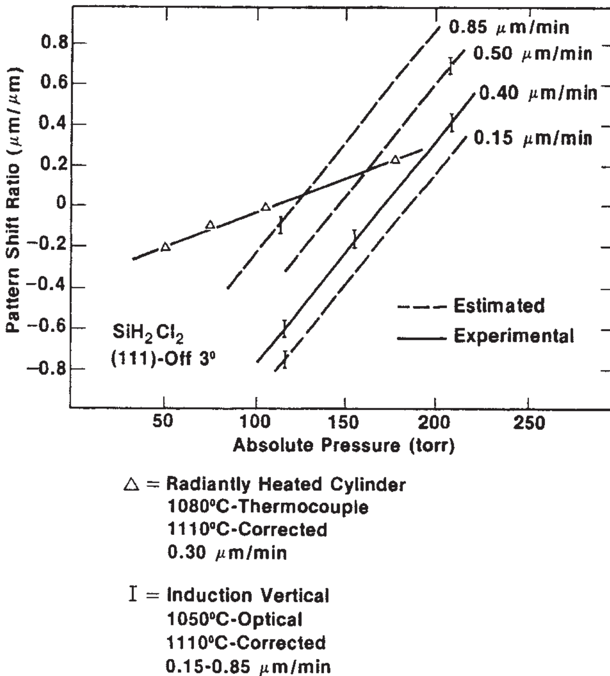



**Figure 26.** Pattern shift ratio versus pressure for various growth rates in vertical and cylinder reactors.[35]

Growth temperature has the strongest effect on pattern shift. A change of only 20–30°C has a major impact on the pattern shift ratio. Decreasing the deposition temperature causes the pattern shift ratio to increase in absolute terms; i.e., for "negative" pattern shift, decreasing the deposition temperature brings the pattern shift closer to zero.

## 11.4 Autodoping[36]

Autodoping is the presence of unwanted dopant contributed to the epitaxy layer by the wafers themselves. The intrinsic doping level is unwanted dopant contributed by the reactor parts. Two kinds of autodoping are recognized:

- Macro-autodoping in which dopant from the wafer surfaces (front and back) contribute dopant generally to all the growing layers.
- Micro-autodoping in; which dopant from one location on a wafer migrates to another location on the same wafer.

Autodoping increases with increasing vapor pressure and increasing diffusion rates of the dopant. Sb causes the least autodoping, followed by As, B and P.

Macro-autodoping can be reduced by many techniques, including:

- Sealing the back of the wafer with CVD oxide, nitride, or polycrystalline silicon during the wafer preparation steps before epitaxy (most effective).
- Operating the reactor so that backside transfer of silicon occurs to seal the back of the wafer during HCl etch (effective but requires etch/coat time).
- Using a two-step process in which a thin, undoped cap layer is deposited first, the system is then purged with Hz and the desired epitaxy layer is grown; (more effective for plug flow reactors where the gas composition can be rapidly changed).
- Using a high/low temperature sequence in which the surface of the wafer is depleted of dopant by a high temperature bake, followed by a lower temperature epitaxy growth step (most effective for As).

- Decreasing the gas residence time by increasing the total flow rate and/or reducing the reactor pressure or volume.
- Operating at reduced pressure where the escaping tendency of the dopant on the wafer surface and the number of volume changes per minute is greatly increased (most effective for As).
- Reducing the concentration of dopant on the wafer surface by using ion implantation instead of dopant diffusion to dope the wafer surface prior to epitaxy growth (effective for all dopants).

Micro-doping is depicted schematically in Fig. 27. Here, the $n^+$ buried layer encroaches into the epitaxy layer by a combination of solid state diffusion and vapor transport during growth. Both vertical and lateral autodoping occur. Vertical autodoping is dopant moving vertically into the growing layer; lateral autodoping is movement to the sides of the buried layer region.

Micro-autodoping is reduced by the same techniques as macro-autodoping. Backside sealing is usually not required because IC processing is normally structured to avoid backside doping.

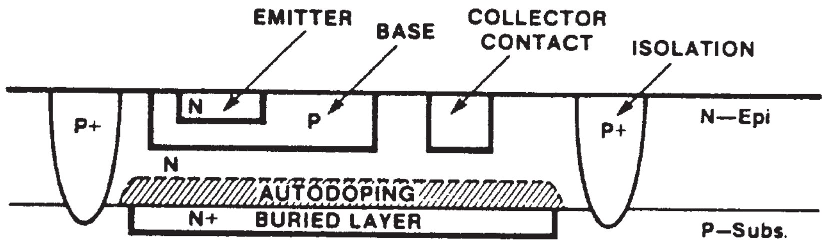



**Figure 27.** Micro-autodoping in a buried layer bipolar device structure.

Pre-epitaxy oxidation can have a strong effect on autodoping. B is preferentially absorbed by a growing thermal oxide on silicon and the concentration near the single crystal surface is reduced.[37] The opposite is true for As and P. This effect of the oxide segregation coefficient for different dopants and different pre-epitaxy oxidation conditions is summarized in Fig. 28.[38] The number of arrows pointing up indicates an

increasing degree of autodoping; arrows pointing down indicate a decreasing degree. If possible, pre-epitaxy doping for As and P should be accomplished with higher temperature, dry oxidation rather than lower temperature, wet oxidation. The opposite is true for B.

Vertical and lateral autodoping are measured by spreading resistance probe (SRP) resistivity profile techniques as illustrated in Fig. 29.[34] When the SRP profile is taken through the epitaxy layer and into the buried layer region, the vertical autodoping profile is measured. When the profile is taken to the side of the buried layer region, one slice through the lateral autodoping profile is measured.

The SRP profile measures many different contributions to autodoping and these contributions are summarized in Fig. 30.

| | HIGH TEMP | LOW TEMP | WET OXID | DRY OXID |
|---|---|---|---|---|
| As | ↓ | ↑↑ | ↑↑↑ | ↑ |
| P | ↓ | ↑↑ | ↑↑↑ | ↑ |
| B | ↓ | ↑ | ↓↓ | ↓ |

**Figure 28.** Effect of pre-epitaxy drive-in oxidation on autodoping.

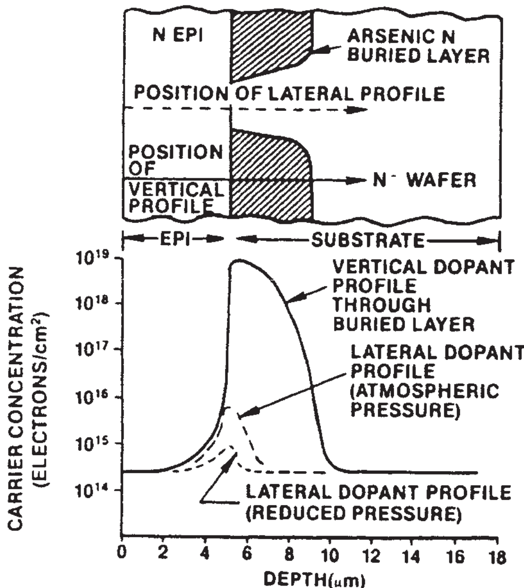



**Figure 29.** Vertical and lateral autodoping measurement using spreading resistance probe resistivity profiles.[34]

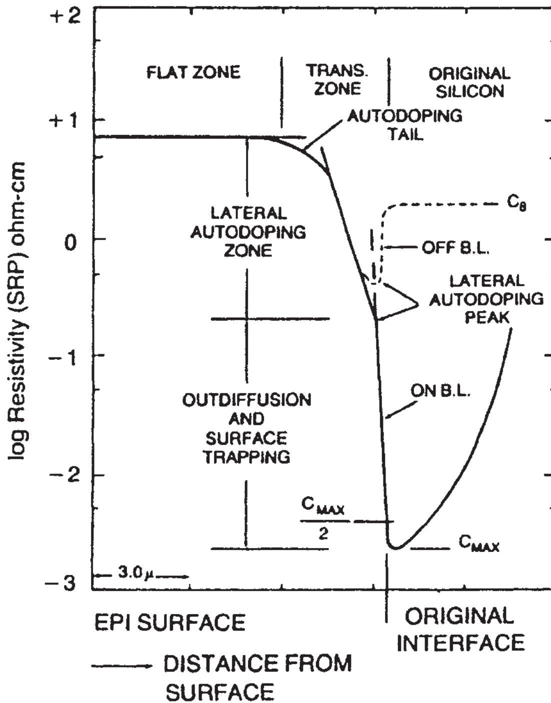



**Figure 30.** Spreading resistance probe resistivity profile on and off buried layer region (150 torr, $SiCl_4$, 1060°C optical).

**Dopant Transitions**. As silicon devices become faster and smaller, the epitaxy layer becomes thinner, and autodoping effects on transition width and circuit density become more important.

Figure 31 is an SRP resistivity profile through an epitaxy layer over a heavily doped As buried layer.[35] The epitaxy layer was grown in a vertical reactor at 1110°C in $SiH_2Cl_2$ at 0.5 micron/minute with a reactor pressure of 150 torr. The buried layer minimum resistivity is 0.0027 ohm-cm and the controlled dopant region has a resistivity of 0.27 ohm-cm. If the autodoping tail is ignored, a straight line can be drawn using semi-log paper through the resistivity points and a "transition width" can be defined as the distance required for this straight line to traverse two orders of magnitude in resistivity. For consistency, this straight line should pass through the resistivity value corresponding to one-half the maximum dopant concentration (the location of the original wafer surface). This unusual definition of transition width permits an analysis of the effect of pressure on the initial slope of the vertical autodoping profile.

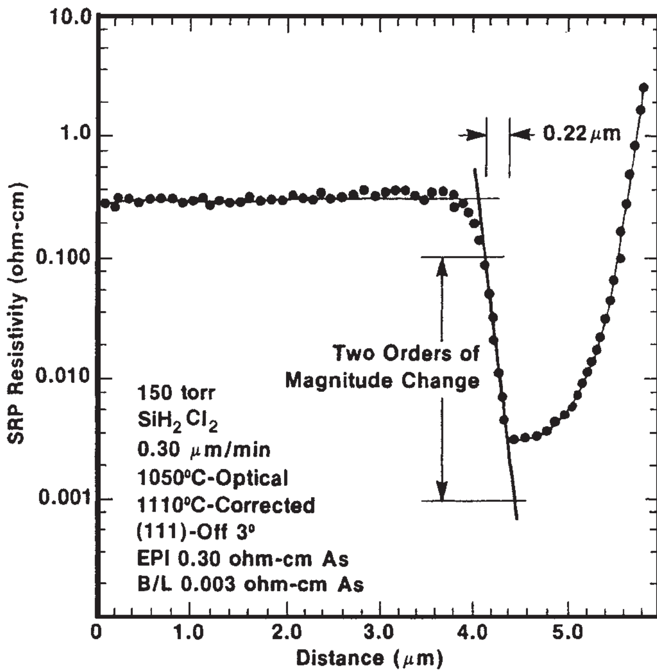



**Figure 31.** Spreading resistance probe resistivity profile over buried layer region illustrating one definition of transition width (distance required for a two order of magnitude resistivity change).[35]

Figure 32 is a plot of the "transition width" as defined above versus reactor pressure in the 50–250 torr region for a vertical reactor operating under the deposition conditions described above.[35] Data for both B and As are presented. For pressures above about 250 torr, the transition width decreases fairly slowly with decreasing pressure. In the 100–200 torr range, the transition width decreases rapidly with decreasing pressure and then becomes essentially constant as the pressure is decreased below about 100 torr.

The data in Fig. 32 are explained as follows. Above about 200 torr, the escaping tendency for either B or As is not strongly affected by pressure, and the volume changes per unit time are increased by only 3.8 times compared to 760 torr for the same total flow rate. From 200 torr to 100 torr, the number of volume changes per unit time doubles to 7.6 per unit time and the lower pressure encourages dopant to escape from all surfaces. As the pressure is reduced to below 100 torr, the autodoping by gas transport is

essentially eliminated and only solid state diffusion remains as the mechanism for dopant encroachment into the epitaxy layer. Solid state diffusion is virtually unaffected by reduced pressure; therefore, the transition width no longer decreases with decreasing pressure.

The radiantly heated cylinder reactor has been reported to show increased B autodoping for process pressures below 100 torr,[39] in contrast with the data presented here.[35]

Device structures can have both B and As buried layer patterns. The data presented in Fig. 32 support the idea[39a] that the 100–150 torr pressure range is optimum for minimizing both B and As autodoping.

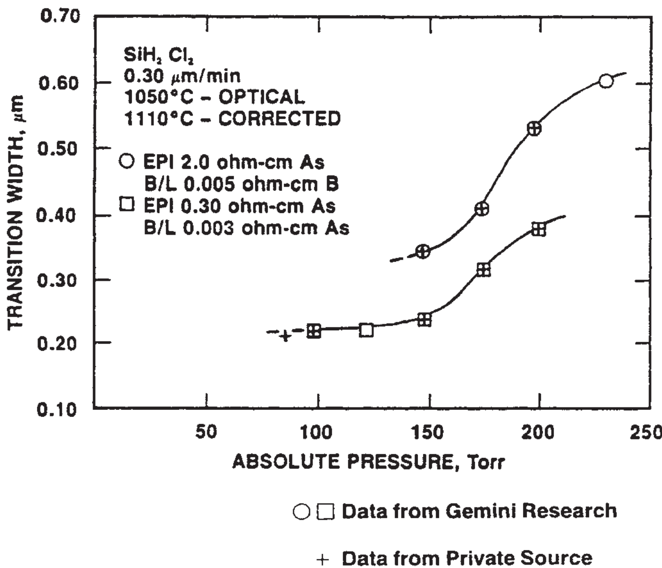



**Figure 32.** Transition width (as defined in Fig. 31) versus deposition pressure.[35]

For some bipolar ICs, B buried layers are used to reduce the amount of diffusion time required to create the $p^+$ isolation regions. The concern is that B autodoping will cause a compensation resistivity peak above the As buried regions and adversely affect device performance. Figure 33 includes a schematic cross section through an epitaxy layer grown in a vertical reactor over both B and As buried layers. Figure 33 illustrates how the SRP resistivity profiles and groove/stain cross section would be affected if there were or were not significant autodoping.[35]

Figure 34 contains an SRP resistivity profile through an epitaxy layer grown in a vertical reactor for a real device structure using both B and As buried layers. Figure 35 presents a grooved and stained cross section through the same structure represented in Fig. 34. Clearly, for the conditions cited in Fig. 34, there is little or no lateral autodoping effect of the B above the As buried layer region.[35]

Autodoping is complex and all the process conditions are closely related. Key issues must be resolved by direct experiment on each device structure using the autodoping reduction techniques described above.

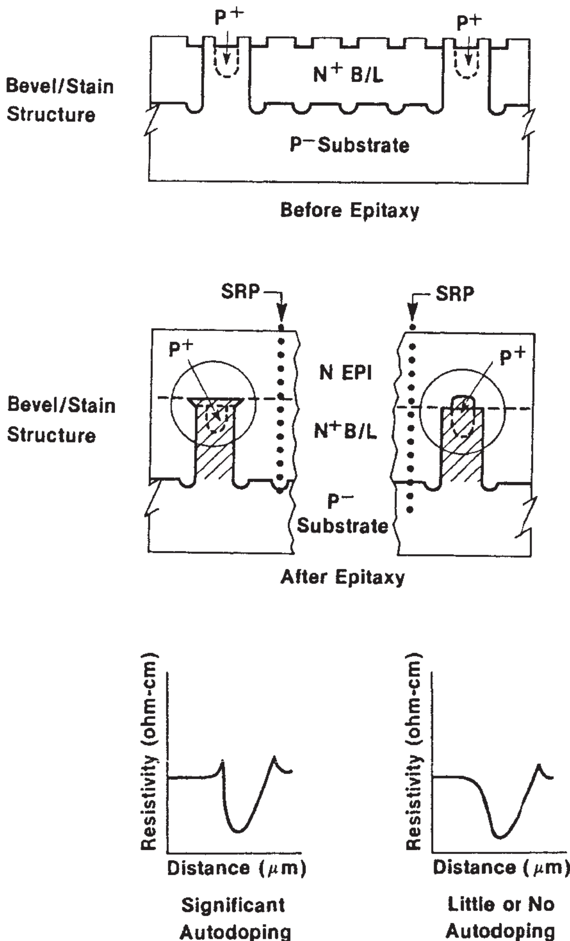



**Figure 33.** Schematic diagrams illustrating possible effects of autodoping in an As-doped epitaxy layer grown over both B and As buried layer patterns.[35]

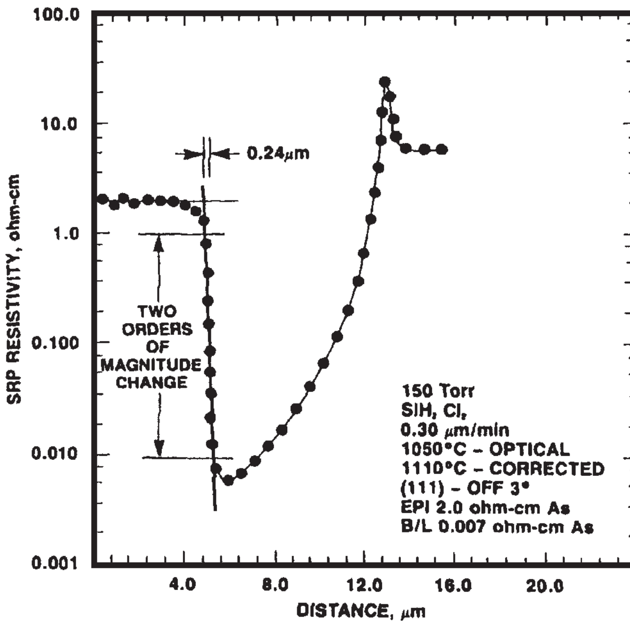



**Figure 34.** Actual spreading resistance probe resistivity profile over As buried layer region in a device structure with both B and As buried layer patterns.[35]

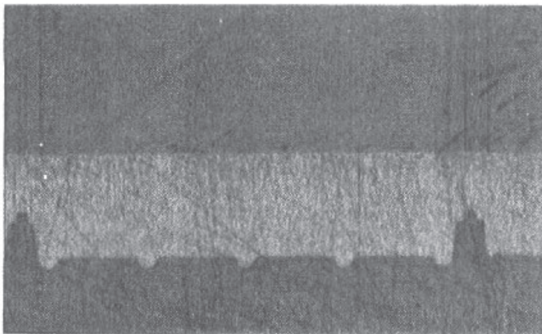


**Figure 35.** Grooved and stained cross section through same device structure in Fig. 34.[35]

## 12.0 NEW MATERIALS TECHNOLOGY FOR SILICON EPITAXY

The epitaxy process has been well-defined since the mid-1970s in terms of temperature and pressure ranges, growth rates, and chemical choices. Special techniques which were developed in that time frame but are only now becoming more widely used include:

- Silicon-on-sapphire
- Selective epitaxy
- Epitaxial lateral overgrowth
- Epitaxial trench refill
- Low temperature epitaxy

Silicon-on-sapphire provides single crystal (100) silicon grown on top of single crystal sapphire substrates cut and polished on the (1102) plane where there is a geometrical relationship between the two different crystal structures. Successful growth of silicon-on-sapphire requires:[40]

- A complete absence of chlorine which attacks the sapphire at high temperature and liberates Al, a *p*-type dopant.
- An oxidizer level below 1 ppm in the reactor.
- A deposition temperature of 900–920°C in $SiH_4$.
- A well-polished sapphire substrate.
- A high initial growth rate, followed by one somewhat slower after the growth mechanism becomes silicon on silicon rather than silicon on sapphire.

Selective epitaxy is the growth of single crystal silicon in windows etched into thermally grown oxide on the wafer surface. Selective epitaxy with and without controlled polycrystalline silicon being grown on top of the oxide is possible.[35][41]

Selective epitaxy *without* polycrystalline silicon overgrowth on the oxide is accomplished by depositing with conditions that do not promote nucleation. These conditions include depositing:

- With approximately a 3:1 ratio of chlorine to silicon, created by adding HCl to the deposit gas.

- At a slightly higher temperature to enhance the etching rate of the chlorine.
- At a reduced pressure where escape of volatile silicon chlorides is enhanced.
- A growth temperature of 1000°C using $SiH_2Cl_2$ with a 3/1 $HCl/SiH_2Cl_2$ ratio at 100 torr is currently recommended for selective epitaxy without polycrystalline overgrowth.[35]

Epitaxial lateral overgrowth is another variation on selective epitaxy in which the selectively grown epitaxy is permitted to grow up out of the windows and over the oxide surface. The single crystal layer on top of the oxide can be etched to disconnect it from the single substrate, thereby creating high quality single crystal islands on top of thermally grown oxide. Such structures have considerable promise for three-dimensional device structures.[41]

Selective epitaxy with polycrystalline silicon overgrowth utilizes deposition conditions that promote nucleation, such as:

- The absence of chlorine.
- The use of $SiH_4$.
- The use of lower temperatures and higher pressures.

Selective epitaxy *with* polycrystalline silicon overgrowth can be accomplished with $SiH_4$ at 975°C and 760 torr deposition pressure.[35][42]

In device applications, the polycrystalline silicon overgrowth provides a place to create heavily doped contacts to the single crystal area without affecting the more lightly doped device regions.

## 13.0 LOW TEMPERATURE EPITAXY

Silicon epitaxy by CVD at lower temperatures is now of significant interest.[43][44] Silicon epitaxy has been successfully demonstrated:

- In the 800–1000°C range in a conventional reactor using $SiH_4$ or $SiH_2Cl_2$ after first initiating growth at a higher temperature.[45]
- In the 800–1000°C range using $SiH_4$ and substituting He for $H_2$ as the main carrier gas.[46]

- In the 850–1000°C range in a conventional reactor using $SiH_4$ with wafers that were etched in HF just prior to placing in the reactor.[47]
- In the 850–900°C range in a conventional reactor using $SiH_2Cl_2$, at reduced pressures of 10–20 torr.[41b]
- In the 800–900°C range using photodissociation of silane and other silicon compounds.[48]
- In the 750–950°C range in a cold wall reactor after removing the native oxide with a plasma etch.[49]
- In the 700–900°C range by operating at very low pressure in a loadlocked, hot wall reactor.[50]

All these low temperature epitaxy processes have limited application because they require very low growth rates to achieve even partially satisfactory crystal quality.[16b][16c][51] As the required epitaxy layer thicknesses go below 0.6 micron, such techniques must be further developed and characterized for commercial production.[44]

## CONCLUSIONS

Silicon epitaxy is a vital and growing semiconductor process technology that is becoming more important as device geometries shrink and MOS ICs begin to depend upon its unique advantages.

Fluid mechanics and other chemical engineering principles can be used to understand the process adjustments. The technology is somewhat complex but understandable and reproducible in a production environment.

Epitaxy quality is very sensitive to pre-epitaxy crystal surface preparation and to the deposition conditions. Crystal quality is especially sensitive to the presence of oxidizers during heat-up and deposit. Commercial equipment is progressing to meet the industry's needs in terms of productivity and quality, and CVD will continue to be the dominant silicon epitaxy technology through the century.

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# 3

# Chemical Vapor Deposition of Silicon Dioxide Films

*John Foggiato*

## 1.0 INTRODUCTION

The use of chemical vapor deposition for various insulator films is paramount in the fabrication of semiconductor devices. The initial use of such films for passivation led to the development of low temperature techniques for film deposition. With the availability of silane, the pyrolysis of silane in the presence of oxygen at atmospheric pressure provided the deposition mechanism. Further enhancements in film characteristics through the use of phosphorus as a dopant within the film allowed the film to provide gettering of impurities during wafer fabrication. This led to the need for "smoothing" the films, now known as *reflow*, to minimize the sharp corners that metal lines had to cover. Reflow was further enhanced by the addition of boron as the dopant. This technology continues to be used today with better implementation of the reflow processes.

With the addition of more than a single metal layer, dielectric films were needed for electrical isolation. These dielectrics had to be deposited at less than 400°C to prevent affecting the underlying metal layer. Initially, using silane at atmospheric pressure, suitable films could be formed. The

advent of plasma enhanced film deposition enabled or improved dense film deposition. Low frequency power during deposition improved both the film deposition process and the film properties. Both atmospheric and plasma enhanced films are extensively used today.

More recently, other reactants in the form of liquid precursors have been developed to provide other film properties, generally focused toward better step coverage. Although initially used at high deposition temperatures (>650°C), today TEOS (tetraethylorthosilicate) is used as a precursor in plasma enhanced deposition and for atmospheric pressure deposition with ozone. New precursors are being developed to deposit interlevel and intermetal dielectrics. As the technology drives towards 0.10 µm linewidths and gaps, better gap filling capabilities are needed and, as much as possible, dielectric films need an in-situ flow characteristic.

This chapter focuses on the deposition of dielectric films suitable for interlevel and intermetal dielectrics. A brief review of future directions of dielectrics for DRAM memory cells is given. Starting with atmospheric deposition of films, the first portion of the chapter covers the history of this technology. Plasma enhanced CVD follows with a short overview of new techniques, including HDP (High Density Plasma), ECR (Electron Cyclotron Resonance) and photo enhanced deposition.

After reviewing the basis for deposition for each of the technologies within their respective sections, current deposition methods are reviewed. The reaction mechanisms and the film characteristics that are obtained are given along with the basis by which the film properties are achieved.

An important advancement in achieving the ability to reflow deposited films came as a result of incorporating phosphorus as a dopant. Later optimizations included adding boron to form boron phosphorus silicon glass (BPSG). A review of the dopant incorporation mechanisms is given for this important step in enhancing integrated circuit reliability and manufacturability of smaller device geometries.

In summarizing the chapter, film properties from the different technologies are compared, especially the film properties required for applications in integrated circuit manufacturing.

## 2.0 OVERVIEW OF ATMOSPHERIC PRESSURE CVD

The initial techniques for depositing films of $SiO_2$ employed atmospheric pressure reactors (APCVD). Operating at atmospheric pressure,

the reactor designs were simple, yet provided high deposition rates. By using silane ($SiH_4$) and oxygen, injected as separate gases, the surface reaction on the heated wafer, typically at 400°C, grew films in the 2000 to 3000 Å/min range. The resultant films had suitable electrical characteristics, however, due to gas phase reactions, the step coverage was poor. Examples of such coverage are shown in Figs. 1(a) to 1(c) with the notation that a "bread-loafing" effect appears as the film becomes thicker. Figure 1a illustrates the conformal deposition initially achieved, however with additional deposition (Fig. 1b), the formation of the "bread-loafing" effect can be seen. With typical film thicknesses of 0.5 to 1.0 µm, narrow gaps will fill with a void (empty hole) forming as shown in Fig. 1(c). With a better understanding of the reaction mechanisms and the injection of reactants, some of these step coverage problems could be minimized. Various new reactors have been built around these enhancements and are used today.

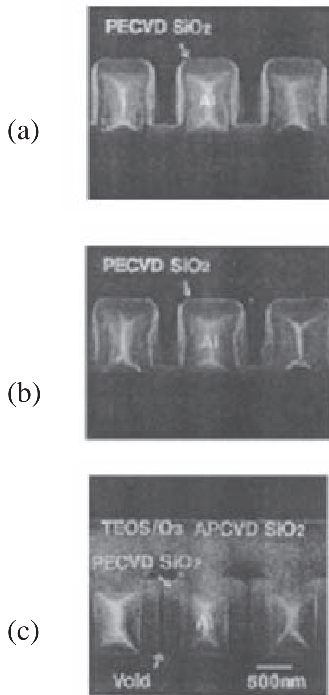



**Figure 1.** Step coverage comparison of dielectric films deposited at atmospheric pressure. (*a*) Initial deposition. (*b*) Further deposition shows "bread-loafing" effect. (*c*) Closure of gap with void formation.

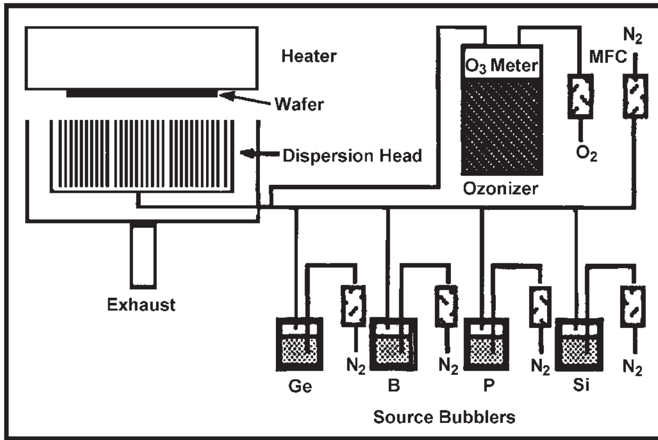
Another approach to overcome APCVD limitations is to find new chemistries that can overcome the gas phase nucleation of the $SiH_4$ processes. TEOS was readily used in low pressure CVD systems at high temperature to decompose in the presence of oxygen and deposit high quality $SiO_2$ films. However, at atmospheric pressure, the decomposition was very slow due to minimal presence of reactive oxygen. During the mid 1980s, various researchers (i.e., K. Maeda[1]) proposed mixing TEOS with ozone in the presence of moderate temperatures. This resulted in growth of good oxide films at 400°C with growth rates of 0.1 µm/min or more. The advantages provided by the TEOS/ozone based films are excellent step coverage and in-situ flow resulting from the surface mobility of the reactants prior to formation of $SiO_2$. Other chemicals, to be discussed later, can serve as reactants and are being evaluated to further enhance film properties.

With atmospheric systems where the reactions take place in a "mass transport limited" regime, careful design of the reactant supply system is required to prevent reactions from taking place within the gas dispersion plumbing. Deposition uniformity is sensitive to the uniform availability of reactants and the exhaust of resulting by-products. Two gas dispersion architectures are in use today, one employing gas injectors with separated reactants evolving from each injector, and the other employing an areal injector. With the gas injector type, high velocity reactants are presented in a narrow line over the heated wafer, referred to as a "knife edge," while the wafer is moved horizontally under the injector. The reactant mixing takes place on the wafer surface. With the areal injector, also referred to as a *dispersion head,* the reactants are premixed prior to reaching the "reaction zone" and the hot wafer surface. This reactant supply technique enhances film thickness uniformity. One drawback of atmospheric reactors is the large amount of $SiO_2$ powder formed which has to be removed from the wafer area. This requires very good design of the by-product exhaust systems and good control of the reactant injector temperature.

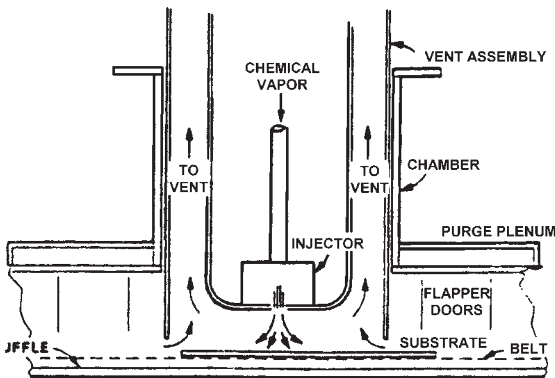
In one APCVD reactor system, shown in Fig. 2a,[2] the wafers are held facing downward which minimizes the number of particles which stick to the wafer surface. In this case, reactants are brought through an areal dispersion head and reach the heated wafer by traversing a 6 mm air gap. By-products and unused reactants are exhausted around the areal dispersion head. In the knife-edge injector system (Fig. 2b),[3] exhaust is provided adjacent to the injectors and through a plenum around the reaction zone. For both types of reactors, the injector temperature must be

low (<100°C) to prevent premature reaction and minimize film deposition in the injectors.

Overall, APCVD technology continues to be used today for both logic and DRAM device fabrication. The $SiH_4$ based films with their low moisture content still dominate the logic market. With the in-situ planarization offered by TEOS/ozone based films, DRAM's use these films extensively in production.




(a)



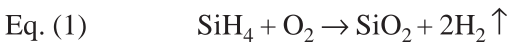

(b)

**Figure 2.** Comparison of APCVD reactor types. (*a*) Areal injector-dispersion head. (*b*) Linear injector.

## 2.1 Basis of Atmospheric Deposition

This section gives a basic overview of film depositions which take place at atmospheric pressure. Its purpose is to familiarize the reader with reaction dynamics which affect the resultant film properties. Extensive coverage of the reactions and their chemical representations is given in Refs. 4 and 5.

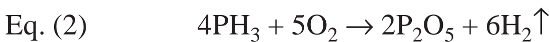
The chemical, $SiH_4$, is pyrophoric; the formation of $SiO_2$ takes place just through its exposure to oxygen. The fundamental reaction is given by:



Eq. (1) $$SiH_4 + O_2 \rightarrow SiO_2 + 2H_2\uparrow$$

With the wafer at 400°C, an amorphous film of $SiO_2$ is formed which is used as the interlayer dielectric. In these reactions, it is important to minimize the residual $H_2$ in the film and to provide a film with suitable electrical properties. The film will undergo additional processing, primarily etching or in some cases densification, so it is necessary to have film thickness uniformity of better than 5%. A theoretical study of the reaction mechanisms and kinetics was given by Cobianu[6] with an emphasis on low temperature deposition.

In a similar manner, phosphorus, for subsequent reflow of the film, is added through the decomposition of phosphine:

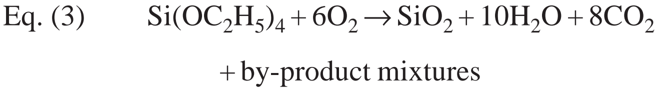


Eq. (2) $$4PH_3 + 5O_2 \rightarrow 2P_2O_5 + 6H_2\uparrow$$

Through the incorporation of the phosphorus pentoxide ($P_2O_5$), generally in the range of 4 to 7 weight percent, the films will reflow at temperatures of 900°C.

In the reaction noted above, the hydrogen release is dictated by the mechanisms driving the reaction, one being deposition temperature. As hydrogen can introduce "hot electron" failures in integrated circuit devices, the amount left in the film must be minimized. These failures are due to hydrogen presence in the transistor gate, thus lowering the transistor transconductance. If allowable, a densification step, at up to 700°C, can be used to outgas the hydrogen. Film deposition uniformity is sensitive to wafer temperature, which must be kept to tolerances of less than 2°C across the wafer surface.

With TEOS, the reaction is one of oxidizing the reactants on the hot wafer surface. In this case the reaction is:



Eq. (3) $$Si(OC_2H_5)_4 + 6O_2 \rightarrow SiO_2 + 10H_2O + 8CO_2 + \text{by-product mixtures}$$

Note that in this case, water, also an undesirable residue within the film, is formed as one of the by-products. Unfortunately, this water with its hydrogen cannot be removed unless heated to the 500°C range. For oxides which are reflowed or densified at higher temperatures, the moisture may be eliminated. The TEOS/ozone deposition generates silanol (Si-OH) which also can be found in the film, however, these silanol groups can be eliminated by high temperature annealing.

In the case of TEOS, initial deposition is performed in a low pressure CVD (LPCVD) system employing the TEOS in vapor form with oxygen. The reactions are exemplified by the conditions given in the Arrhenius plot shown in Fig. 3.[1] At high temperatures, exceeding 750°C, moderate deposition rates are achievable through pyrolysis. With the addition of oxygen, the deposition can be significantly increased or the temperature may be lowered. However, for applications where low temperatures, <500°C are required, a new reaction system is needed employing ozone for the oxidizing agent. As noted, deposition rates greater that 1000 Å/min are achievable at 400°C. A theoretical model describing the kinetics is given in Ref. 7.

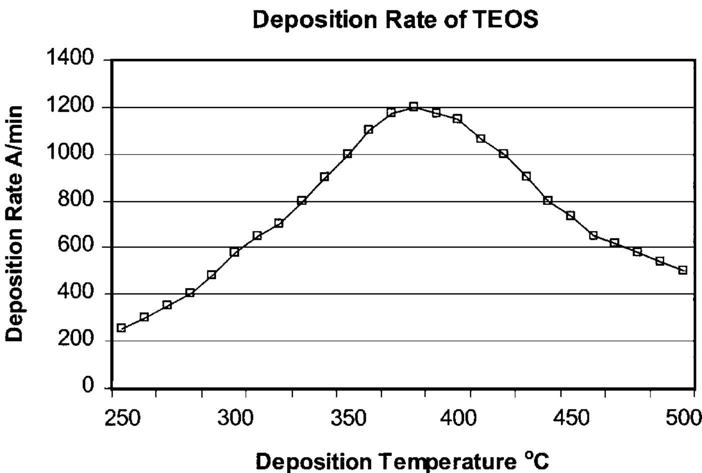
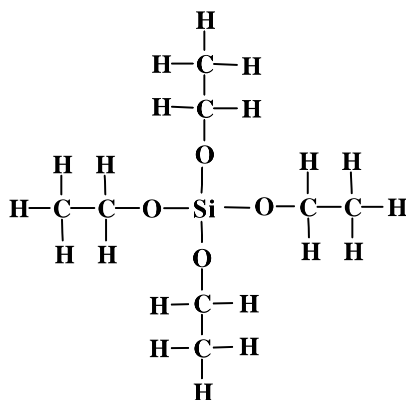



**Figure 3.** Arrhenius plot of CVD $SiO_2$ film formation using TEOS.

Both $SiH_4$ and TEOS based films are doped with phosphorus and boron to lower the films' melting points allowing reflow or planarization of the film. For $SiH_4$, the dopants are phosphine ($PH_3$) and diborane ($B_2H_6$), which are oxidized to form their respective oxides $P_2O_5$ and $B_2O_3$. For phosphorus oxide, an intermediate state can be formed, $P_2O_3$ which is unstable and must be converted to $P_2O_5$ for stabilization. This generally is done through the reflow cycle which takes place at 800°C to 950°C. At the lower temperature, little reflow takes place, however, the film is densified and stabilized. Above 850°C, the reflow process results in a better planar surface.

For TEOS based chemistries, the compatible dopants are also liquids, with a variety being available. To dope with boron, TEB (triethylborate) and TMB (trimethylborate) are used, the latter being developed more recently. Phosphorus doping is obtained with TMPO (trimethylphosphate) or TMPI (trimethylphosphite), the latter having less oxygen in the molecule, thus being more active.

The liquid chemical TEOS (tetraethylorthosilicate or the equivalent tetraethoxysilane) is a safer alternative to the gases silane and dichlorosilane. TEOS and its companion dopants, TEB and TMB for boron, and TMPO and TMPI for phosphorus, slowly hydrolyze into their respective oxides through the decomposition, for example, of the TEOS molecular structure shown here.



It is to be noted that the TEOS molecule already is oxidized and the conversion of TEOS to silicon dioxide is essentially a rearrangement of the molecular structure. The reaction for deposition requires removing two oxygen atoms. At high temperatures, 650 to 850°C, TEOS chemisorbs onto silanol (Si-OH) groups at the surface of the molecule, releasing the ethane molecule. Further desorption takes place and forms Si-O-Si bridges with neighboring molecules.

In a similar manner, the dopants TEB and TMB decompose to their oxide, $B_2O_3$, which becomes the dopant. In the case of phosphorus, TMPO and TMPI decompose to $P_2O_3$ initially, and with additional reaction and high temperature processing, convert to $P_2O_5$. These dopants are incorporated to allow the films to "flow" during subsequent high temperature annealing. This planarization facilitates subsequent lithography and improves reliability.

Other dopants, both gaseous and liquid are becoming available with germanium being the most practical. Germanium oxide, when combined with $SiO_2$ can further lower the melting point of the resulting film. Although still in the development phase, the four component system of Ge oxide, B and P oxides and silicate glass, resulting in GeBPSG, has shown good reflows at temperatures of 750°C or less. Although very porous resulting in moisture absorption, through multiple film structures, the dielectric has suitable electrical properties.[8] One application results from the higher refractive index of the Ge BPSG allowing optical waveguides to be formed on silicon wafers.

An application demonstrating the use of Ge as the dopant in BPSG films is described in Ref. 8. A range of doping levels were tried with RTP (Rapid Thermal Processing) being used for reflow. Overall, lower reflow temperatures were possible for film planarization. Additional characteristics using furnace flow process were reported in Ref. 9, with complete planarization at a temperature of 800°C.

In summarizing the chemical reactions and resulting films, Table 1 provides the basic parameters. With the development of organic silicon sources and their corresponding dopants, the safety problems associated with $SiH_4$ are minimized and new resultant film properties can be achieved.

**Table 1.** Temperatures and Reactants for Forming Silicon Dioxide Films at Atmospheric Pressure

| | | Reactants | | | |
|---|---|---|---|---|---|
| Film Formed | Base Si Source | Phosphorus Dopant | Boron Dopant | Base Gas | Reaction Temp. Range |
| $SiO_2$ | $SiH_4$ | | | $O_2$ | 300–500°C |
| PSG | $SiH_4$ | $PH_3$ | | $O_2$ | 300–500°C |
| BSG | $SiH_4$ | | $B_2H_6$ | $O_2$ | 300–500°C |
| BPSG | $SiH_4$ | $PH_3$ | $B_2H_6$ | $O_2$ | 300–500°C |
| $SiO_2$ | TEOS | | | $O_3$ | 300–450°C |
| PSG | TEOS | TMPO | | $O_3$ | 300–450°C |
| PSG | TEOS | TMPI | | $O_3$ | 300–450°C |
| BSG | TEOS | | TEB | $O_3$ | 300–450°C |
| BSG | | | TMB | $O_3$ | 300–450°C |
| BPSG | TEOS | TMPO | TEB | $O_3$ | 300–450°C |
| BPSG | TEOS | TMPI | TEB | $O_3$ | 300–450°C |
| BPSG | TEOS | TMPO | TMB | $O_3$ | 300–450°C |

## 2.2 Parameters Affecting Chemical Reactions

As previously noted, the reaction sensitivity of atmospheric deposition focuses on the control of a mass-transport dominated reaction. With the reaction taking place at atmospheric pressure, the only control is the exhaust pressure for removal of unused reactants and reaction by-products. The gas injection to the reaction zone depends on the type of injector and conditions of gas mixing, so the resultant film composition and deposition rates vary. Varying the deposition temperature provides some variation in growth rates

and resultant film quality. We first discuss the parameters affecting $SiH_4$ based films followed by TEOS/ozone films.

The effects of exhaust on the deposition characteristics of a system are highly dependent on the reactor design, and a number of practical guidelines can be drawn from currently operating systems. In general, the exhaust and its control affect deposition uniformity and particles which may remain on the wafer. As these reactions are mass-transport driven, the exhaust affects the gas flows across the wafer surface which results in a nonuniform film deposition. Many particles are formed as part of the reaction, so the particle density within the reaction zone is also affected by system exhaust. Systems have evolved where exhaust sensitivity is being decreased, but the factors affecting exhaust must be carefully monitored including periodic cleaning of the system.

Temperature is a major factor in growth rate control, requiring careful control of not only the base wafer temperature, but its distribution across the wafer. Various means have been employed with multiple zone control and/or wafer susceptors with suitable thermal conductivity to achieve uniform wafer temperature. The temperature sensitivity for $SiH_4$ and TEOS are shown in Fig. 4 where for $SiH_4$, increasing the temperature increases the film deposition rate. In the case of TEOS, at low temperature deposition, a maximum growth rate is achieved at 380°C while growth decreases at lower and higher temperatures. To achieve excellent film thickness uniformity of better than ±2%, the temperature distribution across the wafer must be very uniform. Temperature variation of less than ±1°C across a 200 mm diameter wafer is required for the film thickness nonuniformity to be less than ±2%. The optimum deposition temperature is chosen on the basis of film growth rate. In the case of TEOS based films, temperature can also affect the film's ability to fill narrow gaps, so a compromise must be chosen between growth rate and gap-fill capability.

For the case of silane based films, the deposition rate at lower temperatures, ranging from 300 to 500°C, is linear with an activation energy of 10 eV.[6] In the case of TEOS, at lower temperatures, insufficient energy is available to achieve a high growth rate. As temperature is increased to 380°C, a maximum growth rate is achieved, typically 1000 Å/min for undoped oxide films. Further increasing the temperature causes the reactant ozone to decrease in concentration thus decreasing the TEOS/ozone reaction rate resulting in lower film growth rate.

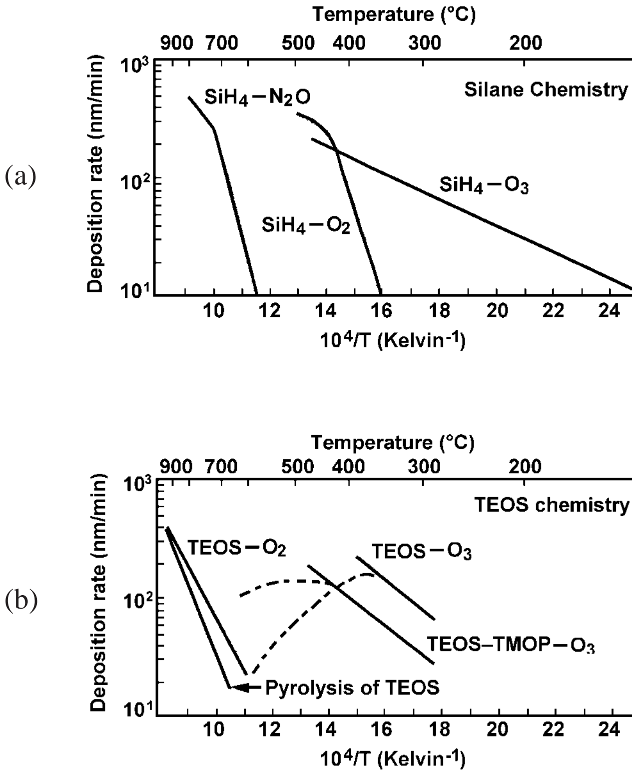



**Figure 4.** Comparison of deposition rate sensitivity with temperature for $SiH_4$ and TEOS.

With mass-transport reactions, the availability of reactants affects growth rate. Within the constraints of the reactor, namely exhaust and reactant transport, increasing the reactant flow rate increases deposition rate. In the deposition of doped films, there is an interaction between the phosphorus and boron reactants which can affect both growth rate and the level to which the dopants can be incorporated into the film. As reactant supply is increased, one must also adjust process exhaust to optimize film thickness uniformity.

In the case of TEOS/ozone chemistry, the reactants are derived from vaporization of the liquid chemicals. The vapor pressure, as depicted in Fig. 5, is sensitive to temperature requiring the chemical containers' temperatures to be precisely controlled. Generally the chemicals are kept

at temperatures providing vapor pressures of 20 mm Hg. Systems now are being developed to directly inject the liquids through a vaporization system to more precisely control reactant flows.

With the variations described above, one can note the process parameters which can be varied to obtain optimal film characteristics. The principle parameters are listed in Table 2 indicating trends with deposition conditions.

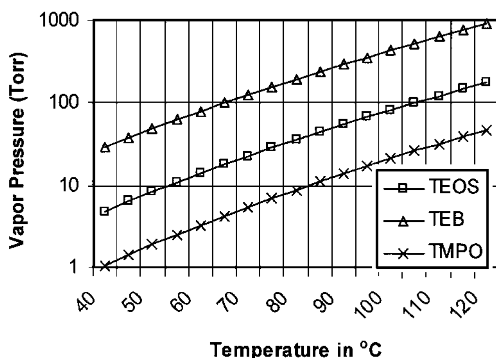



**Figure 5.** Vapor pressure of TEOS and dopants TEB and TMPO.

**Table 2.** Film Parameter Variations with Increasing Process Parameters

| Process Parameters | Increasing Deposition Temperature | Increasing Reactant Temperature | Increasing Reactant Flow | Increasing Exhaust |
|---|---|---|---|---|
| **$SiH_4$ Based** | | | | |
| Deposition Rate | Increases | Slight change | Increases | Slight change |
| Film Thickness Uniformity | Decreases at higher temperature | Slight variation | Decreases with higher flow | Very sensitive |
| **TEOS/Ozone** | | | | |
| Deposition Rate | Increases to 380°C Decreases beyond 400°C | Increases with with increasing temperature | Increases with reactant flow | Slight changes |
| Film Thickness Uniformity | Decreases at higher temperature | Slight variation | Needs balance with exhaust | Very sensitive |

## 2.3 Reaction Chamber Designs

A variety of reactors have been developed for atmospheric film deposition. Original designs employed a pancake configuration with wafers subjected to a gas stream from injectors dispersed around the reactor. With continual adjustments of the injectors and methodical placement of the wafers, reasonable uniformities were achieved on wafers up to 100 mm diameter. The introduction of the Applied Materials 2100 launched a new concept that had fixed areal type injectors and moved the wafers under the injector. Wafers were heated through the moving chain, with wafers placed on plates. This reactor led to the reactors available today.

Reactors of the moving belt type have a linear injector that covers the belt width plus some overlap.[11] As depicted in Fig. 6, the reactant gases are injected from separate nozzles and allowed to mix over the hot wafer. The resultant film deposition takes place with the peripheral exhaust controlling the expenditure of unused reactants and by-products. Nitrogen curtains are used to control gas flows and dispersion. Today's reactors have three or four injectors resulting in an equivalent deposition rate of 2000 Å/min.

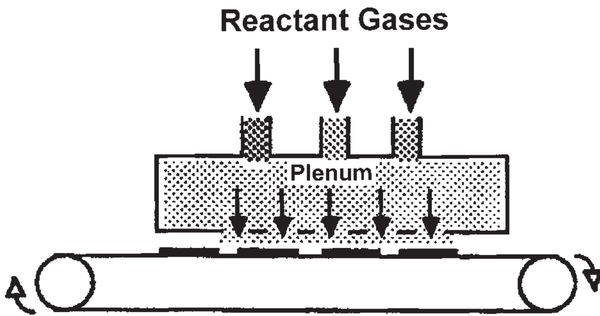



**Figure 6.** Reactor schematic showing wafer moving under injectors.

An areal type reactor utilizes a wider area injector, achieving more control over film thickness uniformity by depositing over the entire wafer. Further expanding the use of an areal injector, a system with multiple reactors for deposition has been developed. Utilizing up to five single wafer reactors, the entire film thickness is deposited within the reactor

with good throughput and film thickness uniformity.[12] Taking advantage of the averaging effects when depositing a portion of the film across multiple reactors, the system concept shown in Fig. 7 was developed. With five reactors, 20% of the film is deposited at each reactor resulting in a high number of wafers processed (high throughput) through the system.

In all the reactors, the mechanical designs have been optimized to minimize the formation of particles and achieve high deposition rates. As deposition is very dependent on the injector-to-wafer distance, the flow dynamics of reactants is controlled by process exhaust. Injector cooling is important to reduce deposition on the injector while still allowing what is deposited to adhere to the injector to prevent particles on the wafer surface.

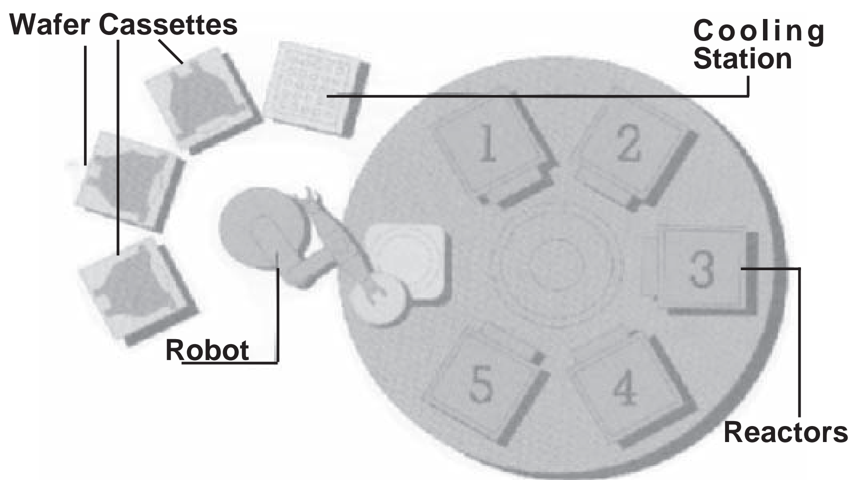



**Figure 7.** Dispersion head type reactor with five reaction chambers. *(Courtesy of Quester Technology.)*

## 2.4 Process Exhaust and Particle Containment

As previously mentioned, the process exhaust controls the deposition characteristics of the injector with film thickness uniformity depending on the mechanical configuration and the resultant exhaust. The reactant lifetime and its reaction on the surface control the deposition rate, so the process exhaust can also affect the resultant deposition rate. This applies to both the linear and areal injector types.

Another effect of the exhaust is particle control. In these deposition processes, the resultant by-products are in the form of particles and must be removed prior to reaching the wafer surface. Exhaust control is used to maintain laminar flows and levels to assure minimal particle formation. In the areal reactor shown in Fig. 7, the wafer is held facing downward with reactants injected upward toward the hot wafer.

Another aspect of particle containment relates to particles on the wafer's backside. With the belt system, an in-situ cleaning of the belt is performed during operation. With the areal deposition system, the wafer is held to a susceptor by vacuum. Sealing of the wafer edge to the susceptor is important in minimizing backside particles.

Atmospheric pressure deposition systems continue to provide films suitable for high-density, small-geometry semiconductor devices. Whereas the emphasis is toward the use of TEOS/ozone due to the film's planarization capability, continued system optimization and new chemistries will further extend the use of APCVD. We now review another technology for depositing films that uses plasmas to initiate and sustain the chemical reactions.

As wafers are processed in a reactor, the uniformity of the film deposition is dependent on the uniformity of the gas distribution, the wafer temperature and the reactor exhaust characteristics. To optimize the film thickness uniformity, it is advantageous to deposit portions of the film in multiple reactors, thus through averaging of the non-uniformities, a better uniformity is achieved. This was initially demonstrated for sputtering of metal films and then implemented in a number of ways for CVD. The Novellus system utilizes multiple deposition sites within a single vacuum chamber for PECVD deposition of films. The Quester system employs multiple reactors in a circular configuration at atmospheric pressure. The reactor of Fig. 6 uses multiple reaction sites in a linear configuration. Experimental data on the Quester system[13] has shown that a single reactor uniformity of 2.5% can be reduced to less than 1% through averaging and balancing reactor operation.

## 3.0 PLASMA ENHANCED CHEMICAL VAPOR DEPOSITION

The previous discussion focused on atmospheric deposition of silicon dioxide with good deposition rates and resultant film characteristics, however, improved deposition rates and denser films are obtained by using plasma for promoting deposition reactions. With the ability to vary the input energy to the reactor via the RF used to generate the plasma, the

deposition rates, and to some extent, the film properties can be optimized. The stress in most films deposited at atmospheric pressure is tensile. The addition of secondary low frequency RF power provides a mechanism for varying the resultant deposited film stress, making it compressive.

### 3.1 Deposition Rates

As noted in Fig. 8, the film parameters for plasma enhanced CVD (PECVD) films can be controlled through varying the plasma-sustaining RF power as well as varying the flow rates of reactants.[13] In addition, working in a vacuum provides a longer mean free path, hence time for the reactants to react and form a film. This results in a higher usage efficiency of the reactants, although at the expense of a more complex system. A comparison of atmospheric and PECVD in Table 3 indicates the characteristics of PECVD systems.

With PECVD technology, other process variables are available to control film characteristics; this flexibility leads to the adoption of PECVD for dielectric film deposition. A plasma process requires control and optimization of several deposition parameters. Within the reaction zone, primarily the wafer temperature must be controlled to achieve good film uniformity. Other parameters providing the reactant decomposition energy include RF power density, frequency and possible duty cycles. The deposition process is dependent in a very complex and interdependent way on these parameters, and the gas composition, flow rates, temperature and pressure must also be considered.

A review of the process parameters as they affect the film characteristics shows the trends for different film parameters. PECVD TEOS films will absorb moisture when exposed to ambient as demonstrated by an increase in dielectric constant. Depositing at higher temperature provides a denser film with lower moisture absorption. Through the use of a lower frequency (about 400 kHz) in conjunction with the RF used for chemical disassociation during deposition, the film is densified which also reduces the moisture absorption. Increasing the deposition rate through higher reactant flow increases the hydrogen content within the film. The hydrogen is found in the form of -OH and water, both of which can be changed by varying reactor operating parameters. To optimize the moisture resistance of these films, both low and high frequency power are used resulting in a film with compressive stress. Also, the deposition parameters are optimized through the deposition rate and by depositing at the highest temperature possible.

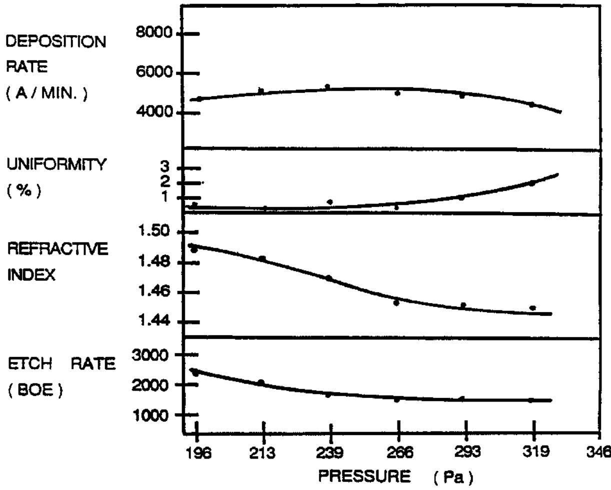



**Figure 8.** Film characteristic variation by varying reactor power.

**Table 3.** Comparison of APCVD and PECVD Systems

| Comparative Parameter | APCVD | PECVD |
|---|---|---|
| Deposition Rate | | |
| $SiH_4$ based | 1000 to 3000 Å/min | 5000 to 6000 Å/min |
| TEOS based | 1000 to 2000 Å/min | 5000 to 7000 Å/min |
| Film Stress | Tensile | Tensile→compressive |
| Dual frequency | | Compressive |
| Film $H_2$ Content | 9 to 12 at % as Si-OH and $H_2O$ | 3 to 5 at % as Si-OH |
| System Complexity | | |
| # of reactors | 1 to 5<br>4 linear reactors, 5 areal reactors | 1 to 4, clustered<br>Single with up to 7 deposition sites |
| Wafer Load/Unload | Robot at atmospheric pressure | Vacuum load locks, robots |
| Vacuum System | None | Multiple stages |

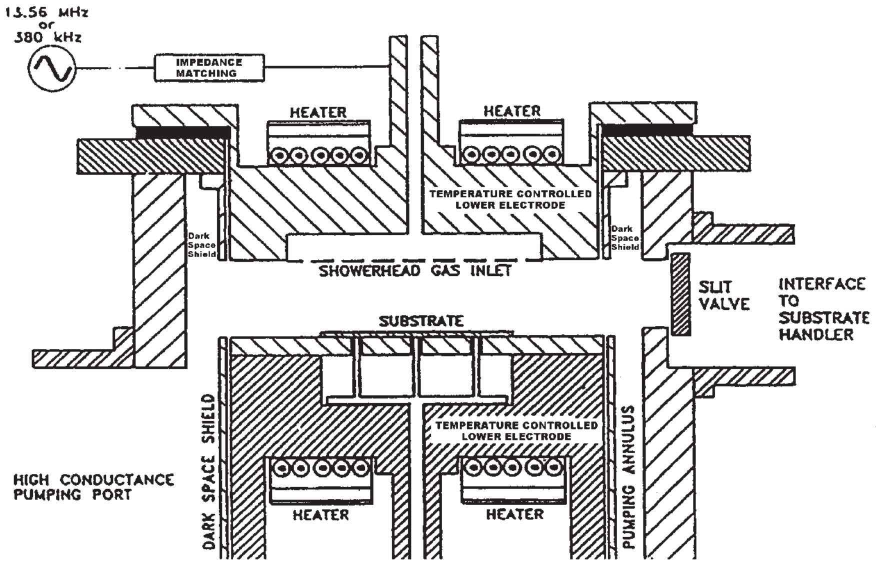
Three types of PECVD systems are in use today: 1) single wafer, 2) multiple wafer, clustered tools, and 3) systems employing a single chamber with multiple deposition sites to achieve better film thickness uniformity. Other features being implemented include a dc or RF bias (dc: 400 kHz) for modifying the film stress. Examples of these are shown in Fig. 9. In Fig. 9a, a single chamber reactor is shown with associated plasma confinement shields. These assist in minimizing deposition outside the area of the wafer and thus particles which may be generated within the system. RF power is applied through the "showerhead" electrode which injects reactants into the process chamber. A second bias, either dc or more recently, low frequency RF, can be applied to the lower electrode. This bias controls ion species bombardment of the deposited film, especially during deposition, leading to an ability to control film stress from a low compressive to a high compressive value.

To attain higher productivity, multiple reactors may be clustered as shown in Fig. 9b. Each of the reactors is independently controlled allowing deposition of films with varying process conditions during deposition. This provides the capability of depositing "sandwiched" layer films to address varying film deposition requirements.

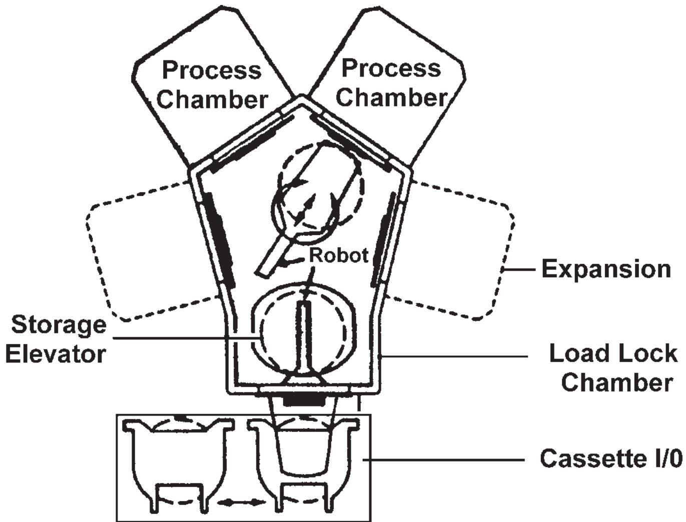
Additional productivity can be obtained by multiple reaction locations within a large single process chamber as shown in Fig. 9c. Although less flexible in terms of process variables, the concept provides high throughput and better film uniformity through the "averaging" effect as discussed in Sec. 2.4.

The important parameters affecting PECVD film during deposition encompass the reactant flow rates, wafer temperature, and rf power used to sustain the plasma. Secondary effects to change film properties include the bias, generally applied to the wafer holder, and plasma confinement to minimize particles. To clean the systems, the convenience of changing process gas and using the plasma to generate reactive species is very convenient. A listing of these parameters as related to film properties is given in Table 4.

Various techniques are being employed to further enhance PECVD films with the incorporation of high plasma density sources. These new directions for depositing high density, good gap-fill films will be described later. We will review some of the chemistries being explored to enhance films characteristics.

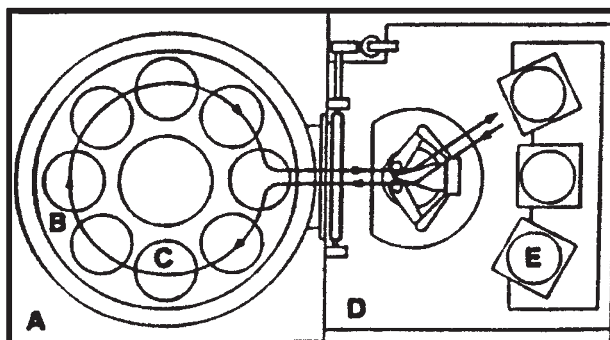



(a)




(b)

**Figure 9.** Various PECVD reactor configurations. (*a*) Single reactor with plasma confinement shields *(courtesy STS Corporation)*. (*b*) Multiple reactor system in cluster tool configuration. (*c*) Multiple deposition sites within single chamber.




A = Process Chamber
B = RF Powered Al Susceptor
C = Deposition Stations
D = Vacuum Loadlock
E = Cassettes (3)

(c)

**Figure 9.** *(Cont'd.)*

**Table 4.** PECVD Process Parameters as Related to Deposited Film

| Deposited Film Parameter | PECVD Design and Process Control Parameters |
|---|---|
| Deposition Rate | Electrode/Showerhead Proximity Reactant Flow, RF Power |
| Thickness Uniformity | Electrode/Showerhead Parallelism Reactor Chamber Vacuum Exhaust |
| Stress | Dual Frequency (Bias) RF Deposition Rate |
| Hydrogen Content | Operating Vacuum Levels Reactants Used Deposition Rate |
| Density | Bias Level (RF/Bias Power Ratio) Operating Vacuum Levels |

## 3.2 Film Characteristics for Different Chemistries

With the reactivity control attainable with PECVD, a variety of chemistries have been developed for depositing silicon dioxide and silicon nitride films. A comparison of these is given here to address different applications.

As a follow-on to APCVD, the initial chemistry used silane and oxygen. The reaction given by:

Eq. (4) $$SiH_4 + O_2 \rightarrow SiO_2 + 2H_2\uparrow$$

which indicates the possible inclusion of hydrogen in the film. As previously mentioned for the case of APCVD, hydrogen can induce "hot electron" effects which can lead to circuit reliability problems. With the additional available energy to disassociate molecules, $N_2O$ was introduced as the oxidant for $SiH_4$. The PECVD oxides contain hydrogen in various forms, Si-H, Si-O-H and H-O-H, thus a low level of nitrogen is incorporated in the film leading to decreased diffusivity of hydrogen.

Takasaki[15] describes the use of $N_2O$ as the oxidizing reactant with the resultant film properties. Through the use of $N_2O$, the "critical" amount of oxygen is generated for film deposition, however the removal of hydrogen may be decreased leading to a higher level of hydrogen in the deposited film.

Another important parameter comprises the film's ability to fill narrow-high aspect ratio gaps. This is becoming more important as films are subjected to CMP (Chemical Mechanical Polishing) after deposition; the films must be free of voids. A number of mechanisms have been proposed as the means to achieve excellent gap-fill. Fujino, et al.[12] have proposed a mechanism for APCVD deposited films. The formation of oligmers in various steps as the reactants reach the wafer surface provides a means of moving across the patterned wafer surface. This molecular mobility allows the oligmers to flow thus providing void-free gap filling. In a similar manner, the same mechanisms have been proposed in PECVD deposition.[15] With the added low frequency bias used in PECVD, it is proposed the formed ions are accelerated into film formation, thus enhancing gap fill compared to operating with a single frequency.

The use of TEOS as the silicon-supplying reactant provides a more conformal film than obtainable with $SiH_4$ chemistry. With $SiH_4$, there is a slow surface migration leading to a reentrant angle as shown in Fig. 10(a).

Experience gained with TEOS in APCVD reactors has enabled rapid surface migration resulting in a conformal step coverage regardless of topography. With a similar process environment and low pressure, the TEOS films deposited by PECVD show the same conformal characteristics as shown in Fig. 10(b).

Use of PECVD oxide films for various applications depends on the allowable hydrogen content, the film step coverage, and resultant stresses. Table 5 lists the various films with possible applications.

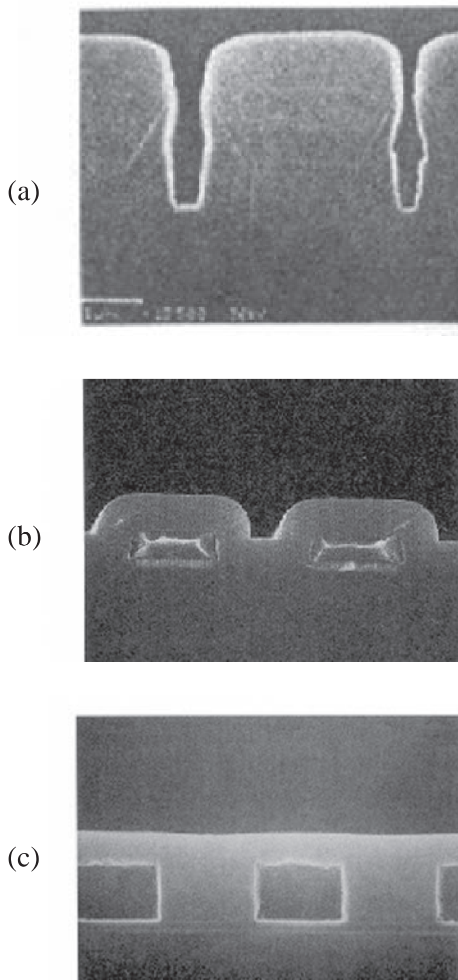



**Figure 10.** Film deposition characteristics: (*a*) $SiH_4$ based films, (*b*) TEOS in APCVD or PECVD, and (*c*) after reflow.

**Table 5.** PECVD Oxide Films and Their Applications

| Film | Chemistry | Application |
|---|---|---|
| $SiO_2$ | $SiH_4$, $O_2$ | Interlevel (ILD), Intermetal (IMD) Dielectric |
| $SiO_2$ | $SiH_4$, $N_2O$ | ILD, IMD, Hydrogen Sensitive ICs |
| $SiO_2$ | $SiH_4$, $N_2O$ | Spacer Oxide, LDD Structure |
| PSG | $SiH_4$, $PH_3$, $O_2$ or $N_2O$ | ILD, IMD |
| BSG | $SiH_4$, $B_2H_6$, $O_2$ or $N_2O$ | Special Applications |
| BPSG | $SiH_4$, $PH_3$, $B_2H_6$, $O_2$ | ILD |
| $SiO_2$ | TEOS, $O_2$ | ILD, IMD |
| $SiO_2$ | TEOS, $N_2O$ | ILD, IMD |

Similar to APCVD, one important aspect of the dielectric films encompasses use of boron and phosphorus doping to lower the films' melting points. With the conformality of the deposition, films are heated and "reflowed" to obtain a "smoother" film for subsequent processing. Figure 10(b) shows films at deposition with excellent conformality as deposited. Heating to 700°C leads to film densification, and some depletion of incorporated unreacted species, i.e., Si-H, Si-O-H, H-O-H, however, the film topography is nearly the same as deposited. Heating to 850°C, typically for 30 minutes in nitrogen, causes the film to soften and reflow, thus providing a smoother topography. To achieve this reflow, boron and phosphorus are incorporated at levels of 3.5 weight percent (wt %) and 5 wt % respectively. Figure 10c shows such films reflowed at 900°C where nearly true planarity is achieved. Higher concentrations of boron and phosphorus allow lower temperatures and shorter times to be used, however, the films tend to readily absorb moisture from the environment.

With PECVD and $SiH_4$ based chemistry, the dopants diborane ($B_2H_6$) and phosphine ($PH_3$) are utilized. When TEOS is used, compatible chemistries, reactants in liquid form, are available; TEB and TMB for boron, TMPO and TMPI for phosphorus. In both applications, the doping reactants are delivered in a manner similar to the silicon supply, just requiring additional control hardware and software.

With the higher energy required to form $Si_3N_4$ from $SiH_4$ and $N_2$, the PECVD technology allowed deposition of these films at low temperatures. Used primarily as a passivation layer, the $Si_3N_4$ film deposition temperature cannot exceed 380°C. As a passivation layer, it behaves as nearly an impervious diffusion barrier, with a low compressive stress, and its coverage of underlying layers, especially metal, is conformal. With PECVD, the stress can be varied, generally to achieve a low compressive level, and with uniform deposition, a pinhole free film can be obtained.

With PECVD, the film is nonstoichiometric and contains hydrogen. Ammonia has been also used as the nitrogen source; the $NH_3$ molecule disassociates at lower energy than $N_2$. Table 6 provides a comparison of the nitride films in use today and their applications.

**Table 6.** Silicon Nitride Film Properties and Applications

| Property | Deposition Method | |
|---|---|---|
| | LPCVD | PECVD |
| Composition | $Si_3N_4$ | $Si_xN_yH_z$ |
| Si/N ratio | 0.75 | 0.8–1.0 |
| Density | 2.8–3.1 g/cm$^3$ | 2.5–2.8 g/cm$^3$ |
| Refractive Index | 2.0–2.1 | 2.0–2.1 |
| Dielectric Constant | 6–7 | 6–9 |
| Dielectric Strength | $1 \times 10^7$ V/cm | $6 \times 10^6$ V/cm |
| Stress at 25°C on Si | 1.2–1.8×$10^9$ dyne/cm$^2$ Tensile | 1–8 × $10^9$ dyne/cm$^2$ Compressive |
| Step Coverage | Fair | Conformal |
| $H_2O$ Permeability | Zero | Low–None |
| Na Penetration | <100 Å | <100 Å |
| Application | Selective Oxidation Gate Dielectric | Passivation |

## 4.0 PROPERTIES OF DIELECTRIC FILMS

There are secondary film properties which are becoming very important for high density, small geometry integrated circuit applications. These are summarized here with some explanation of their effects on circuit performance.

With smaller geometry metal lines, the stresses introduced by the dielectric films can affect reliability. The APCVD films comprised of TEOS/ozone are tensile thus affecting the electromigration of underlying metal lines. A slightly compressive film is desired to counter the tensile stress within the metal films. PECVD films are compressive and their level of compressiveness can be controlled by utilizing a low frequency bias during deposition.

Film thickness uniformity becomes important in subsequent processing steps which involve etching small via holes for intermetal level connection. The etch process can be continued for a short time beyond the nominal endpoint to assure via holes are completely etched, but not too long, otherwise regions where an endpoint is reached initially will have oversize vias. As smaller geometries and larger wafers are being used, the thickness uniformity becomes very important.

Particles introduce point defects which translate to a number of circuit defects, depending on the particle composition and its position. The particles contributed by the CVD processes generally are $SiO_2$ in various forms, from "dust" to pieces which come from depositions within the reactor. With the continuing focus on this problem, today's CVD reactors have become quite clean with maintenance playing a major role in keeping particle counts to a minimum.

Although not heavily emphasized, the refractive index indicates the films' optical properties but also gives an indication of density and dielectric constant. With the $SiO_2$ films, the refractive index provides an indication of the hydrogen content in the form of Si-OH or water. The content can be kept at a minimum by monitoring the deposition process operation through the refractive index measurement.

Film density is measured in a number of ways, the easiest being etch rate in a fixed diluted HF solution, typically 100:1 water:HF. The importance of this parameter is in subsequent etching processes to provide repeatability of the etch process. The etch rate also indicates the films' composition, with higher content of $SiO_2$ giving a lower etch rate.

Reactants for film deposition have achieved remarkable cleanliness through the distillation processes for liquids and their handling and transport. The resultant impurity levels are near or below the detection levels of SIMS and other analytical techniques.

Electrical properties constitute dielectric constant and strength. With the concerns of circuit performance degradation, a lower dielectric constant is desired, however, the basic deposited oxide dielectric constant still remains higher than thermal oxide. Some oxide films have moisture, or are Si or N rich, and the dielectric constant is above that of thermal oxide. Dielectric strength is adequate, greater than 5 MV/cm, for the majority of applications. In high voltage applications, the impurities or unreacted species may introduce premature dielectric background.

Step coverage capability of the films is very important for achieving high yield and high reliability. Substrates typically have different interconnect layers crossing over multiple steps of various heights, and the films' coverage determines circuit isolation. Going to smaller geometries further requires better step coverage as films will need to be thinner for acceptable via hole definition.

As a contradiction to step coverage, there is the need for planarization of the film surface. Ideally, the film can be planarized as part of the deposition process, however, such is not the case today. The APCVD TEOS/ozone process provides a degree of planarization especially for small gaps. The rapid molecular migration during deposition provides some planarization along with good filling of gaps between metal or polysilicon lines.

In Table 7, the properties of films are compared to determine suitability for an application.

## 5.0 NEW DEPOSITION TECHNOLOGIES

With smaller geometries for high performance/high density semiconductor technologies, dielectric films need the capability to fill gaps between polysilicon and metal lines. The typical structure shown in Fig. 11 requires a dielectric film to completely fill the gap without voids as shown in Fig. 11a. The ideal structure shown in Fig. 11b provides the desired filling of metal lines assuring no voids are present. As may be surmised, the voids can accumulate impurities during subsequent processing along with making it difficult to lithographically define contact vias.

**Table 7.** Comparison of Deposited Film Properties

| Type of Film | $SiO_2$ | | | | | | $Si_3N_4$ |
|---|---|---|---|---|---|---|---|
| Deposition | APCVD | | PECVD | | Dual Freq. PECVD | | PECVD |
| Chemistry | $SiH_4$ | TEOS | $SiH_4$ | TEOS | $SiH_4$ | TEOS | $SiH_4$ |
| Primary Reactant | $O_2$ | $O_3$ | $O_2$, $N_2O$ | $O_2$ | $O_2$, $N_2O$ | $O_2$ | $NH_3$ |
| Dopants: Boron | $B_2H_6$ | TEB<br>TMB | $B_2H_6$ | TEB<br>TMB | $B_2H_6$ | TEB<br>TMB | |
| Phosphorus | $PH_3$ | TMPO<br>TMPI | $PH_3$ | TMPO<br>TMPI | $PH_3$ | TMPO<br>TMPI | |
| Stress Type | Tensile | Tensile | Tensile to Compressive | Tensile to Compressive | Tensile to Compressive | Tensile to Compressive | Compressive |
| Stress Level $10^9$ dynes/cm$^2$ | 1.0 | 1.5 to 2.0 | <1.5 | <1.5 | <1.0 | <1.0 | 1.0 |
| Hydrogen Content | | | | | | | |
| Level | 1–2% | 10% | 1–2% | 3% | 1% | 3% | 15% |
| Form | Si-H | $H_2O$ Si-OH | Si-H | $H_2O$ Si-OH | Si-H | $H_2O$ Si-OH | Si-H |
| Deposition Rate Å/min | 2000 | 1000–2000 | 5000–6000 | 3000–4000 | 5000–6000 | 3000–4000 | 1800 |
| Uniformity (1,000 to 10,000 Å) | <3% | <3% | <3% | <3% | <3% | <3% | <3% |
| Refractive Index | 1.45 | 1.44 | 1.45–1.46 | 1.45–1.47 | 1.45–1.46 | 1.45–1.47 | 2.0–2.1 |
| Dielectric Constant | 4.1 | 4.3 | 4.1 | 4.2 | 4.1 | 4.2 | 6-9 |
| Dielectric Strength MV/cm | 6–7 | 5–6 | 6–7 | 6–7 | 6–7 | 6–7 | >7 |
| Step Coverage | Conformal | Gap-fill | Conformal | Gap-fill | Conformal | Gap-fill | Conformal |
| Mechanical Properties | | | | | | | |
| Hardness, GPa | | 3.18 | | 8.24 | | | 25.2 |
| Young's Modules, GPa | | 91 | | 101 | | | 170 |

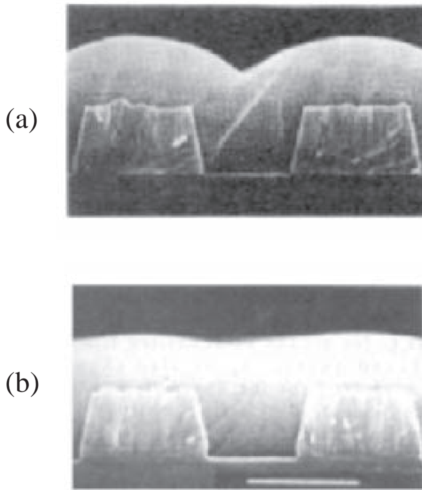
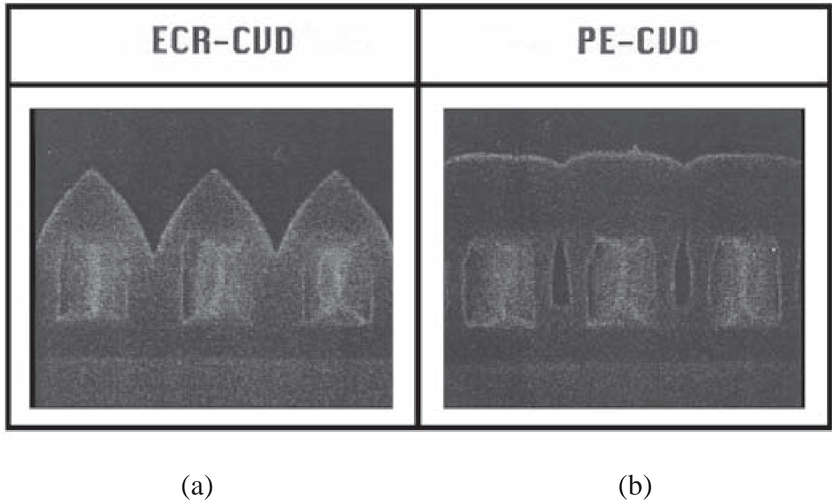



**Figure 11.** Deposited films (*a*) after deposition and (*b*) after reflow at 900°C. *(Courtesy of Quester Technology.)*

In the deposition of the dielectric films, the previously mentioned "bread-loafing" effect causes closure of the gap at the top thus preventing good gap fill. Initial attempts to overcome this problem entailed partial deposition of the dielectric film, then etching back the upper corners of the film as depicted in Fig. 12.[16] Further film deposition followed with repetition of the etching process if needed. Unfortunately the concept was demonstrated, but much too expensive for use in production. Why not develop an environment where deposition and etching could be sequentially done in the same system? This led to the development of ECR technology for deposition where both deposition and to some extent directed etching could take place.

As illustrated in Fig. 12b, the initial film deposition was conformal with eventual closing at the top of the gap. By switching into a directed etching mode, the top could be etched back at a typical 45° angle. Subsequent deposition filled the gap leaving the structure as shown in the actual structure (Fig. 12a).




(a) (b)

**Figure 12.** Depiction of gap fill with partial etch back. Notice the voids in (*b*) the PE-CVD photo. (*a*) The ER-CVD films don't have voids between the lines.

Film properties for the ECR deposited films are given in Table 8 with some notation of the deposition conditions for the ECR system shown in Fig. 13. The deposition plasma is generated above the deposition chamber and directed downward by a magnetic field bias. With injection of reactants, deposition takes place on the wafer which is held down with an electrostatic chuck. The plasma densities are high, so the wafer is cooled with helium dispersed underneath the wafer. Considerable effort has gone into making the ECR technology commercially viable, but problems associated with particle generation, uniformity control, and cost have led to alternative high-density plasma sources for CVD applications.

During the development of ECR, other plasma sources were developed to provide high density plasmas suitable for both deposition and etching of dielectric films. The objective was to develop a directed plasma which would direct reactants into the gaps, provide a means for periodically etching the deposition at the top of the gap, and achieve good electrical characteristics. Further improvements lead to the simultaneous ion bombardment (sputtering) of the top of the gap during deposition.

Equipment manufacturers initially extended the sources developed for film deposition into the “high density” plasma regime. This led to plasma damage of active device regions and numerous limitations in film deposition.

One development was the MORI™ source previously supplied by Trikon.[14] A cross section shown in Fig. 14 notes that the plasma is formed above the biasing magnets. The resulting plasma reaching the wafer can be confined to desirable species with high energy ions kept from the wafer. Developments are continuing in the use of these sources for deposition, however, less complex sources are currently being used..

Transformer-coupled plasma sources have been used extensively for etching and are now migrating towards use for deposition.

Inductively coupled sources have also been developed for deposition; they were some of the earliest sources of high density plasma. All these have certain attributes and require careful design of the reactant injection systems within the confines of a high vacuum plasma environment.

**Table 8.** Film Properties of ECR Deposited Films

| Film Parameter | $SiO_2$ | $Si_3N_4$ |
|---|---|---|
| Thickness Nonuniformity | <3% | <4% |
| Deposition Rate (Å/min) | 3000 to 4000 | 200 to 500 |
| Etch Rate | 30% | |
| Net Deposition Rate (Å/min) | 2100 to 2800 | |
| Refractive Index | 1.46 | 1.98 to 2.10 |
| Dielectric Constant | 4.1 | 8 |
| Stress ($10^9$ dynes/cm$^2$) | 2.0 to 2.5 | 0.6 to 1.4 |
| H Content (at %) | 2 to 3 | 8 |
| RF Power (watts) | 400 to 1000 | 500 to 2000 |
| Deposition Temperature (°C) | 300 | 350 |

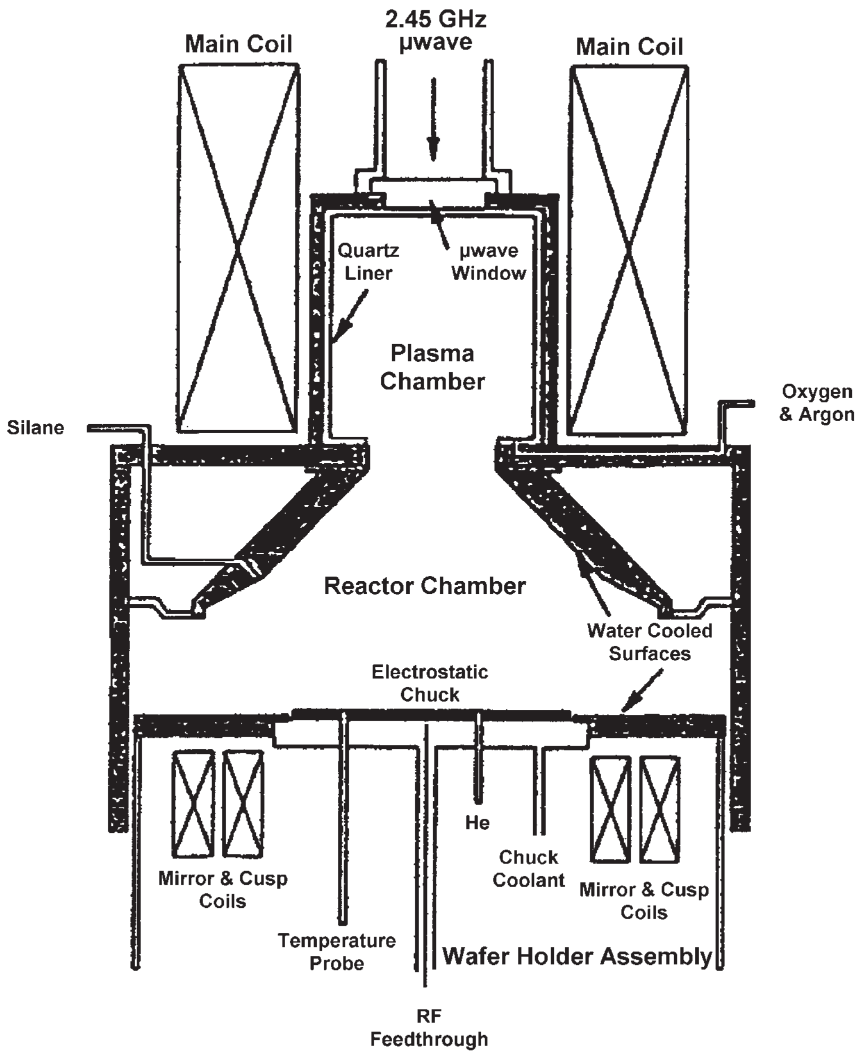



**Figure 13.** ECR system schematic.

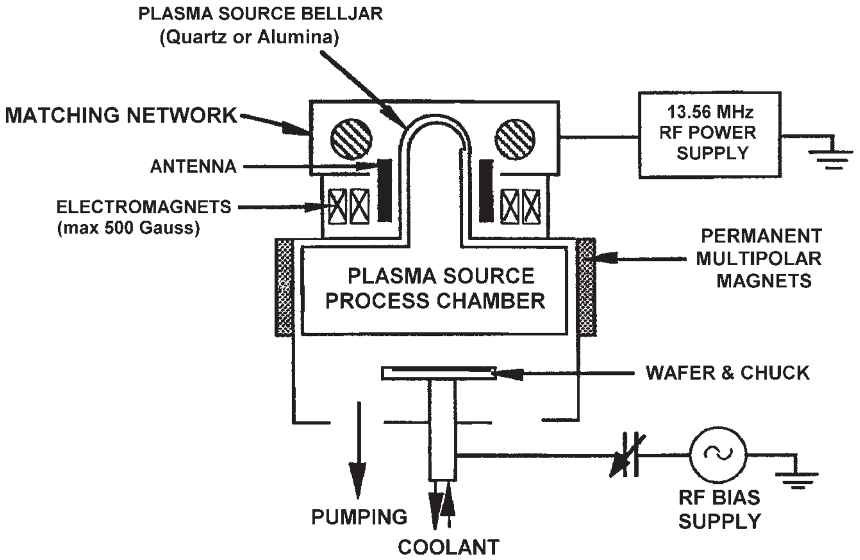



**Figure 14.** Mori source schematic.

## 5.1 Trends for CVD of Dielectric Films

For dielectrics used as capacitors in memory cells, the trends are toward use of higher dielectric materials. These consist of $Ta_2O_5$, $Al_2O_3$, and, more recently, $ZrO_2$ and $HfO_2$, all having the capability for deposition by CVD techniques. The $Ta_2O_5$ materials have made the most progress in possible use for future memory circuits, however, the higher dielectrics constant BZT has received considerable attention.

The higher dielectric materials utilize various precursors for deposition in reactors similar to those used for TEOS. The listing in Table 9 provides available properties of the films, but all the films still need refinement to grow thin layers which are defect free. Along with deposition, the technologies for etching the films also need development.

For interlevel and intermetal dielectrics, the emphasis is toward excellent gap-fill and planarization capabilities. The current technologies, with some refinement, will provide these capabilities as illustrated in Fig.

15. The films consist of a PECVD oxide over metal lines at the gap bottom with typical thickness of 1000 to 2000 Å. A TEOS/ozone overlying layer provides the gap-fill. A third layer, typically 1.5 micron thick PECVD TEOS is then subjected to Chemical Mechanical Polishing (CMP) to provide the planarization shown. Work is currently in progress to CMP the TEOS/ozone films directly.

**Table 9.** Properties of Various Hi-K Dielectrics

| Film Type | Thermal $SiO_2$ | $Al_2O_3$ | $Ta_2O_5$ | $ZrO_2$ | $HfO_2$ |
|---|---|---|---|---|---|
| Dielectric Constant | 3.95 | 9 | 26 | 25 | 25–40 |
| Bandgap (eV) | 8.9 | 8.7 | 4.5 | 7.8 | 5.7 |
| Barrier Height to Silicon | 3.2 | 2.8 | 1–1.5 | 1.4 | 1.5 |
| Deposition Technique | Thermal Growth | CVD | CVD | CVD | CVD |

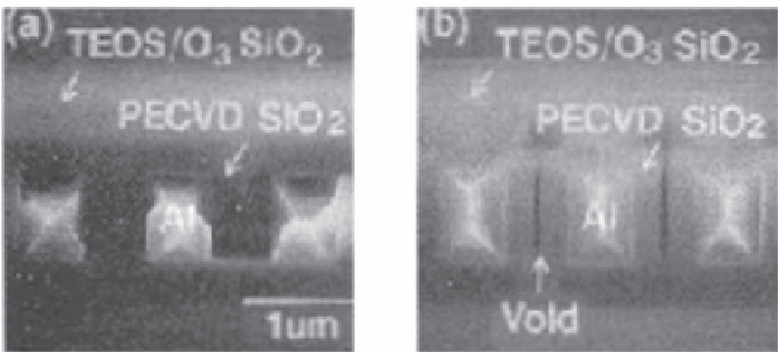



**Figure 15.** Dual layer film stack employing PECVD and TEOS/$O_3$ based $SiO_2$.[19]

Additional progress with plasma deposited films for excellent gap-fill is being made at the same time lowering the dielectric constant. By adding fluorine to the $SiO_2$ film, the interaction during deposition shows an improvement of the gap fill. This work has also led to lowering the dielectric constant of the deposited films. Dielectric constants in the range of 3.5 to 3.8 have been measured with recently reported film characteristics given in Table 10. Lowering of the dielectric constant is the next direction for the ILD and IMD films. As has been well published, lower dielectric constants enhance circuit performance as will be required for future generation microprocessors and memory circuits.

The most prevalent approach for lower dielectric constant of $SiO_2$ based films is to add fluorine to the film. Although leading to film instabilities, absorption of moisture, and formation of hydrofluoric acid, the films after annealing can be stabilized. Other approaches include use of boron-doped glasses and inclusion of boron nitride in the films. With all these films, the lower dielectric constant can be achieved, however, the technologies of subsequent processing steps have to be developed.

Extensive work has been performed using organic films for dielectrics with the development of MCM's (Multi Chip Modules) and to some extent with forays toward wafer scale integration. Various polymers are being investigated with parylene being the most developed. Whereas these films were suitable for the larger geometry technology in MCM's, they are a challenge to use for submicron technology. Examples and properties of such films are given in Table 11.

**Table 10.** Properties of Fluorine Doped $SiO_2$ Films

| Film Type | SiOF | SiOF | a-C:F |
|---|---|---|---|
| Reported in Reference | [22] | [23] | [25] |
| Dielectric Constant | ≈3.5 | 2.7 to 3.2 | 2.5 to 2.8 |
| Deposition Technique | Room Temperature Flow CVD | PECVD and HDP CVD | HDP CVD |
| Source | FTES (fluoro-triethoxysilane) | TEOS | $CH_4$ |
| F Source | Included | $C_2F_6$ | $C_4F_8$ |

To overcome the limitations of spin-on coating of the organic films, CVD methods are being developed.

Various reactors are being used to derive such films using CVD methods, with a typical example shown in Fig. 16. A reactor consisting of a reaction (deposition) chamber has the reactants delivered through two reactant "cracking" chambers. A detailed description is given in Ref. 26 with some results. Still limiting this technology are the problems associated with surface nucleation on the wafer and defect formation by the large molecular structure of the parylene.

**Table 11.** Properties of Organic Dielectrics

| Film Type | Parylene | BCB | PTFE |
|---|---|---|---|
| Film Parameters | | | |
| Dielectric Constant | 2.6 | 2.7 | 1.9 |
| Deposition Technique | CVD | Spin-on | Spin-on |
| Reactants | Poly-p-xylylene | Divinyl-benzo siloxane and Bis-cyclo-butene | Polyfluoroteton-ethylene |
| Temperature Limit °C | 300 | 350 | 400 |

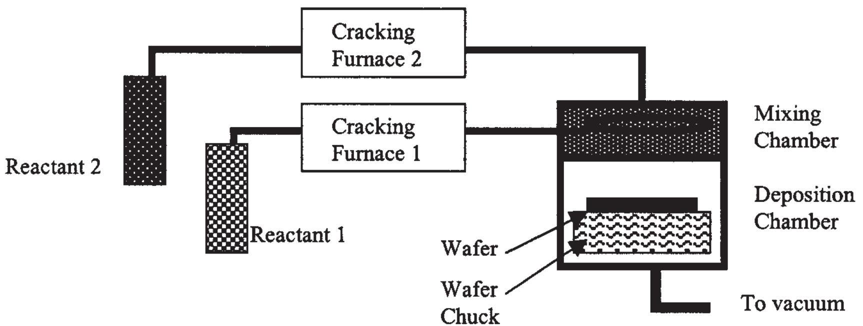



**Figure 16.** Low-K polymer based CVD reactor schematic.

## 6.0 FUTURE DIRECTIONS FOR CVD OF DIELECTRIC FILMS

As we peer into the next centuries' requirements for the films, the challenges for CVD deposition are definitely there. Whereas the focus has been toward production of films suitable for semiconductor devices, the areas of flat panel displays present some formidable challenges. Not only are the deposition areas becoming larger, the perfection requirements for the film are becoming extremely tight. There is much to do to overcome some of the limitations.

With respect to achieving film uniformity and understanding deposition over patterned wafer surfaces, the modeling efforts are giving insight into the reactions that are taking place. Insight into the parameters that affect uniform deposition and its reactions can be derived. However, as surfaces become more demanding, i.e., smaller geometry patterns, further model refinements have to be made.

More difficult is the controllability of particle generation as so many interacting phenomena can result in formation of particles. Various mechanical enhancements to exhaust by-products and unused reactants provide some means of minimizing particles. Through optical observations of reactions plus laser-based particle monitors, particle generation phenomena within reaction zones may be determined. Continued progress in reactor cleaning technology, both the methods and chemistries used, will lead to minimization of particles.

With the need to alter film properties in-situ the deposition reactor, pre- and post-deposition processing will be implemented. Use of electron-beam radiation on SOG films has demonstrated an altered film with more suitable properties.[24] To achieve an in-situ reflow, the BPSG films can be deposited at higher temperatures, currently being performed in Model 9900 systems by LAM Research, Inc.

Continued need for providing tolerable depth-of-focus (DOF) for lithography places emphasis on global planarization of the films. Whereas currently attained through CMP technology, and to some extent by spin-on-glass, it is desirable to find ways for global planarization while depositing the film. Of course, this would lead to a selective deposition as is possible with some metal films. The prospect of a pre-deposition treatment of the wafer surface to achieve selective deposition would be a major breakthrough.

New chemistries are being explored to provide more suitable films within the confines of currently available reactors.[25] An example is the

recently reported use of TMS, within a dual frequency PECVD system, to achieve enhanced film deposition conformity on patterned wafers.

Lower dielectric constant materials, both in the form of organics and inorganics, will be derived from new chemistries. As noted in Table 12, a variety are under development, all focused toward extending current reactor technologies.

## 7.0 SUMMARY

An overview of CVD technologies for dielectric films has provided some insight on film deposition techniques along with film properties. Detailed descriptions of many factors associated with the depositions are given in the cited references. With the continued importance of these films in semiconductor manufacturing and for flat panel displays, a continued, concerted effort will be made to provide the nearly perfect films required for future technologies. Technological progress in theoretical understanding and practical deposition designs will provide films for 300 mm wafers and large area flat panel displays.

**Table 12.** Chemistries for Low-K Materials Deposited by CVD

| Material | K Value | Glass Transition Temperature, °C | Reference |
|---|---|---|---|
| Fluorinated Silicate Glass (FSG or SiOF) | 3.2–3.6 | >800 | [29] |
| Methylated Silica from Tetramethyl Silane | 2.7 | 375 | [29] |
| Parylenes (including copolymers) | 2.2–2.6 | 375 | [29] |
| Fluorinated Amorphous Carbon (a-C:F) | 2.1–2.5 | 350 | [29] |
| Poly(p-xylylene) | 2.3 | 450 | [30] |
| Carbon-doped $SiO_2$ | 2.6–3.2 | 500 | [31] |

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# 4

# Metal Organic Chemical Vapor Deposition: Technology and Equipment

*John L. Zilko*

## 1.0 INTRODUCTION

The growth of thin layers of compound semiconducting materials by the co-pyrolysis of various combinations of organometallic compounds and hydrides, known generically as metal-organic chemical vapor deposition (MOCVD), has assumed a great deal of technological importance in the fabrication of a number of opto-electronic and high speed electronic devices. The initial demonstration of compound semiconductor film growth was first reported in 1968 and was initially directed toward becoming a compound semiconductor equivalent of "Silicon on Sapphire" growth technology.[1][2] Since then, both commercial and scientific interest has been largely directed toward epitaxial growth on semiconductor rather than insulator substrates. State of the art performance has been demonstrated for a number of categories of devices, including lasers,[3] PIN photodetectors,[4] solar cells,[5] phototransistors,[6] photocathodes,[7] field effect transistors,[8] and modulation doped field effect transistors.[9] The efficient operation of these devices requires the grown films to have a number of excellent materials properties, including purity, high luminescence efficiency, and/or abrupt interfaces. In

addition, this technique has been used to deposit virtually all III-V and II-VI semiconducting compounds and alloys in support of materials studies. The III-V materials that are lattice matched to GaAs (i.e., AlGaAs, InGaAlP) and InP (i.e., InGaAsP) have been the most extensively studied due to their technological importance for lasers, light emitting diodes, and photodetectors in the visible and infrared wavelengths. The II-VI materials HgCdTe[10] and ZnSSe[11][12] have also been studied for far-infrared detectors and blue visible emitters, respectively. Finally, improved equipment and process understanding over the past several years has led to demonstrations of excellent materials uniformity across 50 mm, 75 mm, and 100 mm wafers.

Much of the appeal of MOCVD lies in the fact that readily transportable, high purity organometallic compounds can be made for most of the elements that are of interest in the epitaxial deposition of doped and undoped compound semiconductors. In addition, a large driving force (i.e., a large free energy change) exists for the pyrolysis of the source chemicals. This means that a wide variety of materials can be grown using this technique that are difficult to grow by other epitaxial techniques. The growth of Al-bearing alloys (difficult by chloride vapor phase epitaxy due to thermodynamic constraints)[13] and P-bearing compounds (difficult in conventional solid source molecular beam epitaxy, MBE, due to the high vapor pressure of P)[14] are especially noteworthy. In fact, the growth of P-containing materials using MBE technology has been addressed by using P sources and source configurations that are similar to those used in MOCVD in an MBE-like growth chamber. The result is called the "metal-organic MBE"—MOMBE—(also known as "chemical beam epitaxy" technique).[15][16] As mentioned in the first paragraph, the large free energy change also allows the growth of single crystal semiconductors on non-semiconductor (sapphire, for example) substrates (heteroepitaxy) as well as semiconductor substrates.

The versatility of MOCVD has resulted in it becoming the epitaxial growth technique of choice for commercially useful light emitting devices in the 540 nm to 1600 nm range and, to a somewhat lesser extent, detectors in the 950 nm to 1600 nm range. These are devices that use GaAs or InP substrates, require thin (sometimes as thin as 30 Å, i.e., quantum wells), doped epitaxial alloy layers that consist of various combinations of In, Ga, Al, As, and P, and which are sold in quantities significantly larger than laboratory scale. Of course, there are other compound semiconductor applications that continue to use other epitaxial techniques because of some of the remaining present and historical limitations of MOCVD. For

example, the importance of purity in the efficient operation of detectors and microwave devices, and the relative ease of producing high purity InP, GaAs, and their associated alloys,[17] has resulted in the continued importance of the chloride vapor phase epitaxy technique for these applications. In addition, several advanced photonic array devices that are only recently becoming commercially viable such as surface emitting lasers (SEL's)[18] and self electro-optic effect devices (SEED's)[19] have generally been produced by MBE rather than MOCVD because of the extreme precision, control, and uniformity required by these devices (precise thicknesses for layers in reflector stacks, for example) and the ability of MBE to satisfy these requirements. In order for MOCVD to become dominant in these applications, advances in in-situ characterization will need to be made. More will be said about this subject in the final section of this chapter. Finally, the emerging GaN and ZnSSe blue/green light emitting technologies have used MBE for initial device demonstrations, although considerable work is presently being performed to make MOCVD useful for the fabrication of these devices, also.

Much of the effort of the last few years has centered around improving the quality of materials that can be grown by MOCVD while maintaining and improving inter- and intrawafer uniformity on increasingly large substrates. This effort has lead to great improvements in MOCVD equipment design and construction, particularly on the part of equipment vendors. Early MOCVD equipment was designed to optimize either wafer uniformity, interfacial abruptness, or wafer area, depending on the device application intended. For example, solar cells based on GaAs/AlGaAs did not required state-of-art uniformity or interfacial abruptness, but, for economic viability, did require large area growth.[20] During the 1970s and early to mid-1980s there were few demonstrations of all three attributes—uniformity, abrupt interfaces, and large areas—in the same apparatus and no consensus on how MOCVD systems, particularly reaction chambers, should be designed. A greater understanding of hydrodynamics, significant advancements by commercial equipment vendors, and a changing market that demanded excellence in all three areas, however, has resulted in the routine and simultaneous achievement of uniformity, interfacial abruptness, and large area growth that is good enough for most present applications.

In this chapter, we will review MOCVD technology and equipment as it relates to compound semiconductor film growth, with an emphasis on providing a body of knowledge and understanding that will enable the reader

to gain practical insight into the various technological processes and options. MOCVD as it applies to other applications such as the deposition of metals, high critical temperature superconductors, and dielectrics, will not be discussed here.

We assume that the reader has some knowledge of compound semiconductors and devices and of epitaxial growth. Material and device results will not be discussed in this chapter because of space limitations except to illustrate equipment design and technology principles. For a more detailed discussion of materials and devices, the reader is referred to a rather comprehensive book by Stringfellow.[21] An older, but still excellent review of the MOCVD process technology is also recommended.[22] Although most of the discussions are applicable to growth of compound semiconductors on both semiconductor and insulator substrates, we will be concerned primarily with the technologically useful semiconductor substrate growth. We will use abbreviations for sources throughout this chapter. Table 2 in Sec. 3.1 provides the abbreviation, chemical name, and chemical formula for most of the commercially available and useful organometallics.

This chapter is organized into five main sections. We first motivate the discussion of MOCVD technology and provide a "customer focus" by briefly describing some of the most important applications of MOCVD. We then discuss some of the physical and chemical properties of the sources that are used in MOCVD. Because the sources used in MOCVD have rather unique physical properties, are generally very toxic and/or pyrophoric, and are chemically very reactive, knowledge of source properties is necessary to understand MOCVD technology and system design. The discussion of sources will focus on the physical properties of sources used in MOCVD and source packaging.

The next section deals with deposition conditions and chemistry. Because MOCVD uses sources that are introduced into a reaction chamber at temperatures around room temperature and are then thermally decomposed at elevated temperatures in a cold wall reactor, large temperature and concentration gradients and nonequilibrium reactant and product concentrations are present during film growth.[23] Thus, materials growth takes place far from thermodynamic equilibrium, and system design and growth procedures have a large effect on the film results that are obtained. In addition, different effects are important for the growth of materials from different alloy systems because growth is carried out in different growth regimes. For these reasons, it is impossible to write an "equation of

state" that describes the MOCVD process. We will, however, give a general framework to the chemistry of deposition for several classes of materials. In addition, we will give a general overview of deposition conditions that have been found to be useful for various alloy systems.

In the next section, we consider system design and construction. A schematic of a simple low pressure MOCVD system that might be used to grow AlGaAs is shown in Fig. 1. An MOCVD system is composed of several functional subsystems. The subsystems are reactant storage, gas handling manifold, reaction chamber, and pump/exhaust (which includes a scrubber). This section is organized into several subsections that deal with the generic issues of leak integrity and cleanliness and the gas manifold, reaction chamber, and pump/exhaust. Reactant storage is touched upon briefly, although this is generally a local safety issue with equipment and use obtainable from a variety of suppliers.

The last section is a discussion of research directions for MOCVD. The field has reached sufficient maturity so that the emphasis of much present research is on manufacturability, for example, the development of optical or acoustic monitors for MOCVD for real-time growth rate control and the achievement of still better uniformity over still larger wafers. In addition, work continues to make MOCVD the epitaxial growth technique of choice for some newer applications, for example, InGaAlN and ZnSSe.

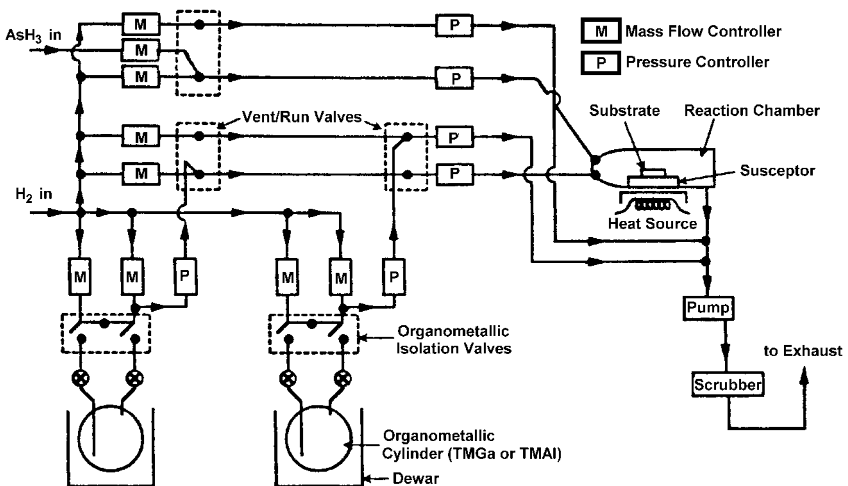


**Figure 1.** Schematic of a simple MOCVD system.

We will not discuss MOMBE in this chapter since the characteristics of MOMBE are, for the most part, closer to MBE than MOCVD. This is largely because of the pressure ranges used in the two techniques. In contrast to MOCVD which takes place at pressures of ~ 0.1–1 atmospheres in cold wall, open tube flow systems, MOMBE uses metal organic and hydride sources in a modified MBE system and produces films at high vacuum. Use of an MBE configuration allows several of the most attractive attributes of MBE, such as in-situ growth rate calibration, through reflection high energy electron diffraction (RHEED), and line of sight deposition, to be applied to materials which are difficult to grow using conventional solid source MBE such as P-containing materials. In-situ growth rate calibration is particularly important in the fabrication of certain advanced optoelectronic array devices such as SEED's and SEL's which rely on the precise growth of reflector stacks. In fact, it is this limitation of MOCVD that drives the work on in-situ monitors.

Finally, we note that even thirty-three years after its first demonstration, there is still no consensus on the proper name of the technique. One still finds MOCVD referred to as organometallic chemical vapor deposition (OMCVD), metal-organic vapor phase epitaxy (MOVPE—the name used by one of the most important conferences), organometallic pyrolysis, or metal-alkyl vapor phase epitaxy. We use MOCVD in this chapter because this is the original name (from the era of sapphire substrate growth) and is the most general term for the process even though most applications require the epitaxial nature of the process. Ludowise gives an interesting discussion of the merits of the various names for this technique.[22]

## 2.0 APPLICATIONS OF MOCVD

Advancements in MOCVD technology have always occurred in response to the requirements of the various applications of this technology, including improvements in materials purity, interfacial abruptness between layers, luminescence efficiency, uniformity, and throughput. In this section, we briefly describe the most important applications of MOCVD, the requirements of those applications, and the most commonly used source combinations that are used to fulfill those requirements.

Most of the commercial applications of MOCVD are in the area of optoelectronics, i.e., lasers, LED's, and to a lesser extent, photodetectors. Electronic applications exist but are likely to become important only for integration of optoelectronic and electronic devices. In general,

stand-alone electronic devices and circuits made from compound semiconductors are used only in limited applications, and are often based on implantation technologies, not epitaxial technologies.

Table 1 lists several of the most important applications, their requirements, substrates and alloys used, materials attributes needed, and the most widely used sources used to produce those materials. The source chemical abbreviations are listed in Table 2 in Sec. 3.1.

**Table 1.** Applications of MOCVD

| Application | Device requirements | Substrate/materials and doping | Materials attributes | Most common sources |
|---|---|---|---|---|
| Telecommunications lasers at 1.3 μm and 1.55 μm | High optical efficiency, high doping, p-n junction control | InP/InGaAsP, InGaAs, InP, Zn (p), Si or S (n), Fe (semi-insulating) | High luminescence, Interfacial abruptness, Controlled lattice match, n, p, semi-insulting doping | TMIn<br>TMGa or TEGa<br>$AsH_3$ or TBAs<br>$PH_3$ or TBP<br>DMZn or DEZn<br>$SiH_4$, $H_2S$, CPFe |
| Telecommunications fiber pump lasers at 980 nm | High optical efficiency, high doping, p-n junction control | GaAs/AlGaAs, InGaAs, InGaP, GaAs, Zn or Mg (p) Si (n) | High luminescence, Interfacial abruptness, Controlled lattice match n, p doping | TMGa<br>TMAl<br>TMIn<br>$AsH_3$ or TBAs<br>$PH_3$ or TBP<br>DMZn or DEZn<br>CPMg<br>$SiH_4$ |
| YAG pump lasers at 780–850 nm, CD lasers for storage at 780 nm | High optical efficiency, high doping, p-n junction control | GaAs/AlGaAs, GaAs, Zn or Mg (p) Si (n) | High luminescence, Interfacial abruptness, Controlled lattice match n, p doping | TMGa<br>MAl<br>$AsH_3$ or TBAs<br>DMZn or DEZn<br>CPMg<br>$SiH_4$ |
| Visible lasers for display at 550–650 nm | High optical efficiency, high doping, p-n junction control | GaAs/InGaP, InGaAlP, GaAs, Zn or Mg (p) Si (n) | High luminescence, Interfacial abruptness, Controlled lattice match n, p doping | TMGa<br>TMAl, TMIn<br>$AsH_3$ or TBAs<br>$PH_3$ or TBP<br>DMZn or DEZn<br>CPMg<br>$SiH_4$ |
| PIN photodiodes at 900–1600 nm | Low dark current, high responsivity | InP/InGaAs | High purity | TMIn<br>TMGa or TEGa<br>$AsH_3$<br>$PH_3$ |

*(Cont'd.)*

**Table 1.** *(Cont'd.)*

| Application | Device requirements | Substrate/materials and doping | Materials attributes | Most common sources |
|---|---|---|---|---|
| Far infrared photo-detectors | High responsivity, low dark current | GaAs/HgCdTe, ZnTe | Low background doping, bandgap control | DMCd<br>Hg<br>DMZn<br>DMTe or DIPTe |
| Far infrared photo-detectors | High responsivity, low dark current | InSb/InAsSb | Low background doping, bandgap control | TMIn<br>$AsH_3$<br>TMSb, TIPSb |
| Solar cells | High conversion efficiency | GaAs/AlGaAs, InGaP, GaAs | Low deep level concentration | TMGa<br>TMAl, TMIn<br>$AsH_3$ or TBAs<br>$PH_3$ or TBP |
| Hetero-structure bipolar transistors | Uniform, controlled gain | GaAs/AlGaAs, InGaP, GaAs<br>InP/InGaAs | Precise, uniform, controlled doping at high levels | TMGa<br>TMAl or TMAAl<br>$AsH_3$ or TBAs<br>$Si_2H_6$<br>$CCl_4$ (C doping) |

All of the applications described above require extremely good interwafer (wafer-to-wafer) and intrawafer (within wafer) uniformity for composition, thickness, and doping since device properties that are important to users are typically extremely sensitive to materials properties. One of the major driving forces behind MOCVD equipment and technology improvements has been the need to achieve good intrawafer uniformity while maintaining excellence in materials properties.

## 3.0 PHYSICAL AND CHEMICAL PROPERTIES OF SOURCES USED IN MOCVD

Sources that are used in MOCVD for both major film constituents and dopants are various combinations of organometallic compounds and hydrides. The III-V and II-VI compounds and alloys are usually grown using low molecular weight metal alkyls such as dimethyl cadmium, [DMCd—chemical formula: $(CH_3)_2Cd$] or trimethyl gallium [TMGa—chemical formula: $(CH_3)_3Ga$] as the metal (Group II or Group III) source. The non-metal (Group V or Group VI) source is either a hydride such as $AsH_3$, $PH_3$, $H_2Se$, or $H_2S$ or an organometallic such as trimethyl antimony (TMSb) or dimethyl tellurium (DMTe). The sources are introduced as

vapor phase constituents into a reaction chamber at approximately room temperature and are thermally decomposed at elevated temperatures by a hot susceptor and substrate to form the desired film in the reaction chamber. The chamber walls are not deliberately heated (a "cold wall" process) and do not directly influence the chemical reactions that occur in the chamber. The general overall chemical reaction that occurs during the MOCVD process can be written:

Eq. (1) $$R_nM(v) + ER'_n(v) \rightarrow ME(s) + nRR'(v)$$

where R and R´ represent a methyl ($CH_3$) or ethyl ($C_2H_5$) (or higher molecular weight organic) radical or hydrogen, M is a Group II or Group III metal, E is a Group V or Group VI element, n = 2 or 3 (or higher for some higher molecular weight sources) depending on whether II-VI or III-V growth is taking place, and *v* and *s* indicate whether the species is in the vapor or solid phase.

The vapor phase reactants $R_nM$ and $ER'_n$ are thermally decomposed at elevated temperatures to form the nonvolatile product ME which is deposited on the substrate and the susceptor, while the volatile product RR´ is carried away by the $H_2$ flush gas to the exhaust. An example would be the reaction of $(CH_3)_3Ga$ and $AsH_3$ to produce GaAs and $CH_4$. Note that Eq. 1 only describes a simplified overall reaction and ignores any side reaction and intermediate steps. We will consider reaction pathways and side reactions in more detail in Sec. 4.1. The MOCVD growth of mixed alloy can be described by Eq. 1 by substituting two or more appropriate reactant chemicals of the same valence in place of the single metal or non metal species. Note that Eq. 1 allows the use of both hydride and organo-metallic compounds as sources. Virtually all of the possible III-V and II-VI compounds and alloys have been grown by MOCVD. An extensive list of the materials grown and sources used is given in a review that can be obtained from Rohm and Haas.[24]

We next discuss some of the physical properties and chemistry of MOCVD sources, both organometallic and hydride. We will emphasize those properties that are important for the growth of material, including vapor pressure, thermal stability, and source packaging. Growth conditions, materials purity and chemical interactions between species will be discussed in Sec. 4 on deposition chemistry. For more extensive information, several useful reviews are available.[32][33] Because organometallics and hydrides have rather different physical properties, we will discuss them separately in this section.

## 3.1 Physical and Chemical Properties of Organometallic Compounds

The organometallic compounds that are used for MOCVD are generally clear liquids or occasionally white solids around room temperature. They are often pyrophoric or highly flammable and have relatively high vapor pressures in the range of 0.5–100 Torr around room temperature. They can be readily transported as vapor phase species to the reaction chamber by bubbling a suitable carrier (generally $H_2$) through the material as it is held in a container at temperatures near room temperature. The organometallic compounds are generally monomers in the vapor phase except for trimethyl aluminum (TMAl) which is dimeric.[22] Typically, low molecular weight alkyls such as TMGa or DMCd are used for compound semiconductor work because their relatively high vapor pressures allow relatively high growth rates. As a general rule, the low molecular weight compounds tend to have higher vapor pressures at a given temperature than the higher molecular weight materials. Thus, TMGa has a vapor pressure of 65.4 Torr at 0°C while triethyl Ga (TEGa) has a vapor pressure of only 4.4 Torr at the much higher temperature of 20°C.[24] The lower vapor pressure of TEGa can be used to advantage in the growth of InGaAsP alloys lattice matched to InP by providing a better vapor pressure match than the most common In source, trimethyl In (TMIn), than does TMGa. This, in turn, means that carrier gas flows can be reasonable and matched, especially for the growth of high band gap (wavelength $< 1.10$ μm) materials in this alloy system. Table 2 lists a number of commercially available organometallic compounds with their abbreviations, chemical formulas, melting temperatures, vapor pressure equations, and most common use.

It is generally desirable to use organometallic cylinders at temperatures below ambient in order to eliminate the possibility of condensation of the chemical on the walls of the tubing that lead to the reaction chamber. This favors the use of high vapor pressure sources. Of course, if the most desirable source has a low vapor pressure, it may become necessary to use a source temperatures above room temperature in order to achieve the desired growth rates. In this case, condensation can be prevented by either heating the system tubing to a temperature above the source temperature or by diluting the reactant with additional carrier gas in the system tubing so that the partial pressure of reactant becomes less than the room temperature vapor pressure. Of course, the low vapor pressure of a source may also disqualify it from use in the first place due to the difficulty in preventing condensation or other handling problems.

**Table 2.** Physical Properties of Commercially Available Organometallics for MOCVD[24]

| Chemical | Abbrev-iation | Formula | Melt-ing Temp (°C) | Vapor pressure (P in Torr, T in °K) | Use |
|---|---|---|---|---|---|
| **Aluminum** | | | | | |
| Trimethylamine alane | TMAAl | $(AlH_3N(CH_3)_3$ | 76 | | Low C, low O AlGaAs (with TEGa) |
| Aluminum triisopropoxide | | $Al(OC_3H_7)_3$ | 118 | log P = 11.4–4240/T | |
| Diisobutyl aluminum hydride | | $(C_4H_9)_2AlH$ | -80 | | |
| Dimethyl aluminum chloride | | $(CH_3)_2AlCl$ | -21 | | |
| Dimethyl aluminum hydride | DMAlH | $(CH_3)_2AlH$ | 17 | log P = 8.92–2575/T | |
| Triethyl aluminum | TEAl | $(C_2H_5)_3Al$ | -52.5 | log P = 8.999–2361.2 /(T–73.82) | Low C AlGaAs (with TEGa) |
| Triisobutyl aluminum | TIBAl | $(C_4H_9)_3Al$ | 4 | log P = 7.121–1710.3 /(T–83.92) | |
| Trimethyl aluminum | TMAl | $(CH_3)_3Al$ | 15.4 | log P = 8.224-2134.83/T | Most widely used Al source, doped AlGaAs, AlInGaP |
| **Antimony** | | | | | |
| Triethyl antimony | TESb | $(C_2H_5)_3Sb$ | -29 | log P = 7.904–2183/T | GaSb, InSb |
| Triisopropyl antimony | TIPSb | $(C_3H_7)_3Sb$ | | log P = 9.268–2881/T | GaSb, InSb |
| Trimethyl antimony | TMSb | $(CH_3)_3Sb$ | -87.6 | log P = 7.7068–1697/T | GaSb, InSb |
| Trivinyl antimony | | $(C_2H_3)Sb$ | | log P = 7.639–2013/T | GaSb, InSb |

*(Cont'd.)*

**Table 2.** *(Cont'd.)*

| Chemical | Abbreviation | Formula | Melting Temp (°C) | Vapor pressure (P in Torr, T in °K) | Use |
|---|---|---|---|---|---|
| **Arsenic** | | | | | |
| Diethylarsenic hydride | DEAsH | $(C_2H_5)_2AsH$ | | log P = 7.339–1680/T | |
| Monoethyl arsenic | | $(C_2H_5)AsH_2$ | -125 | log P = 7.96–1570/T | |
| Tertiary butyl arsine | TBAs | $(C_4H_9)AsH_2$ | | log P = 7.5–1562.3/T | Primary substitute for $AsH_3$ |
| Triethyl arsenic | TEAs | $(C_2H_5)_3As$ | -91 | log P = 8.23–2180/T | |
| Trimethyl arsenic | TMAs | $(CH_3)_3As$ | -87 | log P = 7.405–1480/T | |
| **Bismuth** | | | | | |
| Trimethyl bismuth | TMBi | $(CH_3)_3Bi$ | -107.7 | log P = 7.628–1816/T | |
| **Cadmium** | | | | | |
| Dimethyl cadmium | DMCd | $(C_2H_5)_2Cd$ | -4.5 | log P = 7.764–1850/T | CdTe, CdS, CdSe growth |
| **Carbon** | | | | | |
| Carbon tetrabromide | | $CBr_4$ | 88–90 | log P = 7.7774–2346.14/T | p doping in GaAs, InGaAs |
| Carbon tetrachloride | | $CCl_4$ | -23 | log P = 8.05–1807.5/T | p doping in GaAs |
| **Gallium** | | | | | |
| Diethylgallium chloride | DEGaCl | $(C_2H_5)_2GaCl$ | -4 | | |

*(Cont'd.)*

**Table 2.** *(Cont'd.)*

| Chemical | Abbreviation | Formula | Melting Temp (°C) | Vapor pressure (P in Torr, T in °K) | Use |
|---|---|---|---|---|---|
| Triethyl gallium | TEGa | $(C_2H_5)Ga$ | -82.3 | log P = 8.083–2162/T | AlGaAs, InGaAsP, InGaAs, InGaAlP growth, low C growth |
| Triisobutyl gallium | TIBGa | $(C_4H_9)_3Ga$ | | log P = 4.769–1718/T | |
| Trimethyl gallium | TMGa | $(CH_3)_3Ga$ | -15.8 | log P = 8.07–1703/T | AlGaAs, InGaAsP, InGaAs, InGaAlP, primary Ga source |
| **Germanium** | | | | | |
| Tetramethyl germanium | | $(CH_3)_4Ge$ | -88 | log P = 7.879–1571/T | |
| **Indium** | | | | | |
| Ethyldimethyl indium | EDMIn | $(CH_3)_2(C_2H_5)In$ | 5.5 | | Alternative liquid source to TMIn |
| Triethyl indium | TEIn | $(C_2H_5)_3In$ | | log P = 8.93–2815/T | |
| Trimethyl indium | TMIn | $(CH_3)_3In$ | 88 | log P = 10.52–3014/T | Primary source for In-containing materials |
| **Iron** | | | | | |
| Bis (cyclopentadienyl) iron | CPFe, ferrocine | $(C_5H_5)_2Fe$ | 172–173 | log P = 10.27–3680/T | Semi-insulating doping for InP |
| Pentacarbonyl iron | | $(CO)_5Fe$ | -25 | log P = 8.514–2105/T | |

*(Cont'd.)*

**Table 2.** *(Cont'd.)*

| Chemical | Abbreviation | Formula | Melting Temp (°C) | Vapor pressure (P in Torr, T in °K) | Use |
|---|---|---|---|---|---|
| **Lead** | | | | | |
| Tetraethyl lead | TEPb | $(C_2H_5)_4Pb$ | -136 | log P = 9.0983–2824/T | |
| **Magnesium** | | | | | |
| Bis (cyclopentadienyl) magnesium | CPMg | $(C_5H_5)_2Mg$ | 176 | log P = 25.14–2.18 ln T- 4198/T | p doping in AlGaAs, AlInGaP |
| Bis (methyl cyclopentadienyl) magnesium | Mg | $(CH_3C_5H_4)_2$ | 29 | | p doping in AlGaAs, AlInGaP |
| **Mercury** | | | | | |
| Dimethyl mercury | DMHg | $(CH_3)_2Hg$ | -154 | log P = 7.575–1750/T | |
| **Nitrogen** | | | | | |
| Tertiary butyl amine | | $(CH_3)_3CNH_2$ | -67 | log P = 7.61–1509.8/T | |
| Phenylhydrazine | | $C_6H_5NHNH_2$ | 19 | log P = 8.749–3014/T | |
| Dimethyl hydrazine | | $(CH_3)_2NNH_2$ | | | |
| **Phosphorus** | | | | | |
| Diethyl phosphine | | $(C_2H_5)_2PH$ | | log P = 7.6452–1699/T | |
| Tertiary butyl phosphine | TBP | $(C_4H_9)PH_2$ | | log P = 7.586–1539/T | Primary alternative to $PH_3$ |
| Triethyl phosphine | TEP | $(C_2H_5)_3P$ | -88 | log P = 7.86–2000/T | |
| Trimethyl phosphine | TMP | $(CH_3)_3P$ | -85 | log P = 7.7627–1518/T | |

*(Cont'd.)*

**Table 2.** *(Cont'd.)*

| Chemical | Abbreviation | Formula | Melting Temp (°C) | Vapor pressure (P in Torr, T in °K) | Use |
|---|---|---|---|---|---|
| **Selenium** | | | | | |
| Diethyl selenide | DESe | $(C_2H_5)_2Se$ | | log P = 7.905–1924/T | ZnSe growth |
| Di-tertiary butyl telluride | DTBTe | $(C_4H_9)_2Te$ | | log P = 4.727–1323/T | |
| Methylallyl telluride | MATe | $(CH_3)(C_3H_5)$ Te | | log P = 8.146–2196/T | |
| **Tin** | | | | | |
| Tetraethyltin | TESn | $(C_2H_5)_4Sn$ | -112 | log P = 8.9047–2739/T | n doping GaAs and InP |
| Tetramethyltin | TMSn | $(CH_3)_3Sn$ | -54.8 | log P = 7.445–1620/T | n doping GaAs and InP |
| **Zinc** | | | | | |
| Diethyl zinc | DEZn | $(C_2H_5)_2Zn$ | -28 | log P = 8.28–2109/T | ZnSSe and ZnTe, p-doping for AlGaAs, InGaAsP, InGaAlP |
| Dimethyl zinc | DMZn | $(CH_3)_2Zn$ | -42 | log P = 7.802–1560/T | ZnSSe and ZnTe, p-doping for AlGaAs, InGaAsP, InGaAlP |
| Diisopropyl selenide | | $(C_3H_7)_2Se$ | | | |
| Dimethyl selenide | DMSe | $(CH_3)_2Se$ | | log P = 7.98–1678/T | ZnSe growth |

*(Cont'd.)*

**Table 2.** *(Cont'd.)*

| Chemical | Abbreviation | Formula | Melting Temp (°C) | Vapor pressure (P in Torr, T in °K) | Use |
|---|---|---|---|---|---|
| **Silicon** | | | | | |
| Silicon tetrachloride | | $SiCl_4$ | -70 | | |
| Tetra ethoxysilane | TEOS | $(C_2H_5O)_4Si$ | -77 | log P = 6.88–1770/T | |
| Silicon tetrabromide | $SiBr_4$ | | 5 | | |
| **Sulfur** | | | | | |
| Diethylsufide | DES | $(C_2H_5)_2S$ | -100 | log P = 8.184–1907/T | |
| Polypropylene sulfide | | $(C_3H_6)S$ | | log P = 6.91–1405/T | |
| Diisopropyl-sulfide | | $(C_3H_7)_2S$ | | log P = 7.7702–1875.6/T | |
| **Tellurium** | | | | | |
| Diallyltelluride | | $(C_3H_5)_2Te$ | | log P = 7.308–2125/T | |
| Diethyltelluride | DETe | $(C_2H_5)_2Te$ | | log P = 7.99–2093/T | |
| Diisopropyl telluride | DIPTe | $(C_3H_7)_2Te$ | | log P = 8.288–2309/T | CdTe growth at low temps |
| Dimethyl ditelluride | DMDTe | $(CH_3)_2Te_2$ | | log P = 6.94–2200/T | |
| Dimethyl telluride | DMTe | $(CH_3)_2Te$ | -10 | log P = 7.97–1865/T | |

The commonly used sources are generally thermally stable around room temperature, although triethyl indium (TEIn) and diethyl zinc (DEZn) have been reported to decompose at low temperatures in the presence of $H_2$.[22] Thus, the materials are, for the most part, expected to be stable under conditions of use even when stored for extended periods of time. The reactant molecules will begin to thermally decompose in the MOCVD reaction chamber as they encounter the hot susceptor. The temperature at which an organometallic compound will begin to decompose is not particularly well defined. It is a function of both the surfaces with which the organometallic comes in contact[25] and the gas ambient.[26] Also, the decomposition will be affected by the residence time of the chemical species near the hot pyrolyzing surface, which implies a flow rate and perhaps a reactor geometry dependence of the thermal decomposition. Generally, however, the reported decomposition temperatures are in the range of 200 to 400°C[25]–[28] for most of the metal alkyls. Exceptions to this are the P- and As-containing alkyls which decompose at much higher temperatures.[23][29] The high decomposition temperatures of the P-alkyls, in particular, eliminate their use as sources for P in MOCVD. On the other hand, heavier metalorganic species tend to have lower decomposition temperatures. Thus, the most important non-hydride P source is the high molecular weight chemical tertiary butyl phosphine [$(C_4H_9)PH_2$] which decomposes in the 400°C range.[30] Additional information on MOCVD sources and source choices can be found in papers by Stringfellow[31][32] and Jones.[33]

In addition to vapor pressure and decomposition temperature, other considerations in the choice of sources include toxicity, the amount of unintentional carbon and oxygen incorporated in the films, and the susceptibility of source combinations to vapor phase prereactions. The high toxicity of the commonly used hydrides $AsH_3$, $PH_3$, and $H_2Se$ (see Sec. 3.3) lead to the substitution of TBAs, TBP, and DMSe for their hydride counterparts in many applications. Unintentional carbon and oxygen contamination of Al-bearing materials has driven the use of higher molecular weight species such as TMAAl instead of TMAl since the chemistry of TMAAl (no direct Al-C bonds) makes this source considerably less susceptible to carbon and oxygen reactions as will be discussed in Sec. 4.2. Source prereactions will be discussed more fully in Sec. 4.1.

## 3.2 Organometallic Source Packaging

Most of the commonly used organometallic compounds are pyrophoric or at least air and water sensitive and therefore require reliable, hermetic packaging to prevent the material from being contaminated by air and to prevent fires resulting from contact with air. The organometallic compounds are generally shipped from the supplier in the package that will be used for film growth. Thus, the package should be considered an integral part of the source product.

Packages used generally consist of welded stainless steel cylinders with bellows or diaphragm valves and vacuum fittings (face seals) on the inlet and outlet, which provide a high degree of leak integrity and which minimize dead volumes. Great care should be taken to prevent connecting a cylinder backwards since the carrier gas will push the liquid organometallic source backwards into the gas manifold with generally devastating effects on the MOCVD gas handling system. At best, pushing condensed organometallics back into the manifold will result in a very messy cleanup of largely pyrophoric chemicals.

For liquid sources, the container is in the form of a bubbler. Carrier gas (typically $H_2$) is passed through the bottom of the material via a dip tube as is pictured in the cross-sectional view of a typical cylinder in Fig. 2. The carrier gas then transports the source material into the reactor. Assuming thermodynamic equilibrium between the condensed source and the vapor above it, the molar flow, $\nu$, can be written:

Eq. (2) $$\nu = (P_v f_v / kT_{std}) P_{std} / P_{cyl}$$

where $\nu$ is the molar flow in moles/min, $P_v$ is the vapor pressure of the organometallic species at the bath temperature, $f_v$ is the volume flow rate of the carrier gas through the bubbler in l/min, $k$ is the gas constant, $T_{std}$ = 273°C, $P_{std}$ = 1 atm, and $P_{cyl}$ is the total pressure in the organometallic cylinder. The $P_{std}/P_{cyl}$ term in Eq. 2 accounts for the increased molar flow from a cylinder that operates at reduced pressure. $P_v$ can be calculated from the data in Table 2. Note that if $P_{cyl} < P_v$, the cylinder contents will boil and the molar flow will become extremely unstable. Typical molar flows for organometallic species are in the range of $5 \times 10^{-6}$ to $5 \times 10^{-5}$ moles/min. A detailed discussion of bubbler operation is given by Hersee and Ballingall.[34]

The approximation of thermal equilibrium between the condensed and vapor phases is a good one for liquid sources such as TMGa. Since most sources are liquids, Eq. 2 is usually a valid description of organometallic molar flows.

This approximation is not necessarily a good one for solid sources, of which TMIn is the most important. Solid sources are in the form of agglomerated powder and are typically packaged in bubblers of the same design as in Fig. 2. Because of the lack of bubble formation and the uncertain surface area of the solid, the condensed phase of the source will often not be in equilibrium with the vapor phase, especially at higher carrier gas flows. In this case, the molar flow of reactant will be less than that calculated from Eq. 2 which was developed assuming thermodynamic equilibrium.[35][36] Mircea, et al.,[36] have measured the time integrated mass flow from a TMIn cylinder at various carrier flows and found that the cylinder deviated from equilibrium at rather low carrier flows. Their curve is reproduced in Fig. 3. In addition, the surface area of the source inside the cylinder can vary as the cylinder is used so that the curve generally described in Fig. 3 can vary with time. Even with continuous feedback and adjustment, this can lead to total source utilization of only 60–70%.

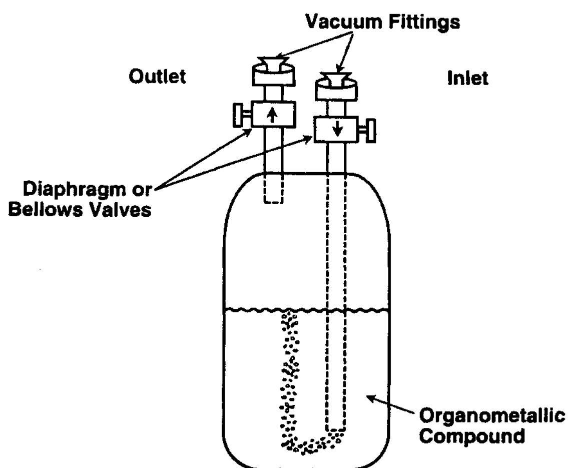


**Figure 2.** Schematic drawing of an organometallic cylinder.

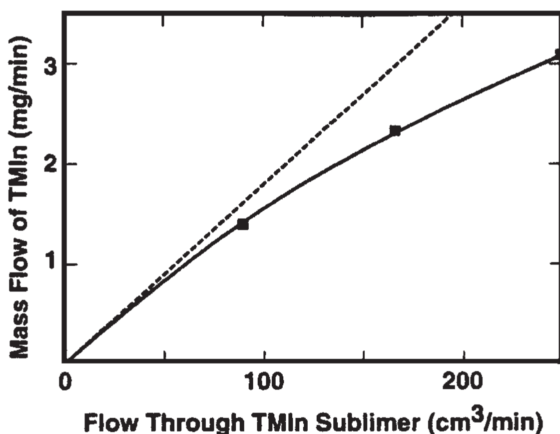


**Figure 3.** Mass flow of TMIn as a function of the flow through the TMIn sublimer. Sublimer temperature = 25°C. Dashed line represents a linear dependence of mass flow on carrier gas flow. *(From Mircea, et al.)*[36]

There are several ways of reducing or eliminating this problem with solid sources. Perhaps the simplest method is to load inert balls into the sublimer when the cylinder is being filled by the vendor.[37] This technique is called "supported" grade and increases the surface area and decreases the tendency for TMIn agglomeration. A second alternative is to use reverse flow bubblers. In this case, the sublimer is assembled by the vendor so that the dip tube is on the outlet, not the inlet side. This forces the carrier gas to contact more surface area and prevents carrier gas channeling. Note that this should only be done with solid sources where there is no danger of pushing the condensed phase organometallic back into the gas manifold. One can achieve a similar effect by connecting the outlet of a standard sublimer in series with the outlet of an empty standard sublimer. In low pressure reactors, the sublimer can be operated at low pressure. This causes the sublimation rate of the solid to increase in proportion to the pressure reduction from atmospheric pressure and works well to maintain vapor saturation even at high flows. Sources used at reduced pressure can be used to about 90% of capacity.

Another alternative is to use liquid sources. A new liquid source, ethyl dimethyl In (EDMIn), has been proposed as an alternative to TMIn. However, concerns about the thermal stability of EDMIn have prevented the wide acceptance of this chemical as the In source. Alternatively, solid

TMIn can be dissolved in a low vapor pressure organometallic solvent which essentially converts the solid source to a liquid source. Utilization efficiencies > 95% can be achieved in the use of this "liquid TMIn" source. There is presently no clear consensus in the literature as to the relative effectiveness or desirability of any of these alternatives. However, it is clear that they all provide a major improvement compared with advantage operating solid sources in the conventional manner.

## 3.3 Hydride Sources and Packaging

In the growth of III-V's containing As or P and II-VI's containing S or Se, the hydrides $AsH_3$, $PH_3$, $H_2S$, and $H_2Se$ are often used as the sources. This is because they are relatively inexpensive (although the cost of safely using them generally exceeds the materials saving), are available as either dilute vapor phase mixtures or as pure condensed phase sources to provide flexibility in concentration, and eliminate some of the concerns regarding C incorporation that exist for organometallic sources.[38][39] All are extremely toxic. In addition, diluted (typically to 0.01% to 2%) mixtures of $SiH_4$, $H_2S$, and $H_2Se$ are often used as dopants in AlGaAs and InGaAsP growth. When used as dilute sources, $AsH_3$, $PH_3$, $H_2S$, and $H_2Se$ are generally mixed with $H_2$ at concentrations of 5–15 %. When these sources are used as pure sources, they are supplied as liquids at their vapor pressures in high pressure gas cylinders. Table 3 lists the most commonly used hydride sources, their vapor pressures at around room temperature, the highest pressure at which a mixture will generally be supplied before condensation of the hydride inside the cylinder becomes likely under typical use and storage conditions, and the threshold limit value, a measure of toxicity that represents the maximum 8 hours/day, 40 hours/week, exposure that will result in no long term deleterious effects.[40]

**Table 3.** Physical Properties of Most Commonly Used Hydride Sources

| Source | Vapor pressure at 21° C (psig) | Maximum pressure of a mixture (psig) | Threshold limit value (ppm) |
|---|---|---|---|
| Arsine - $AsH_3$ | 205 | 1100 at 15% | 0.05 |
| Phosphine - $PH_3$ | 593 | 1800 at 15% | 0.3 |
| Hydrogen selenide - $H_2Se$ | | 2000 at 5% | 0.05 |
| Hydrogen sulfide - $H_2S$ | | 2000 at 5% | 10 |

Since the cylinder pressure of pure sources is the vapor pressure, cylinder pressure can not be used to monitor the consumption of these sources as is possible with mixtures. However, as the pure source becomes nearly all used, all of the condensed liquid phase evaporates and the source can no longer support its own vapor pressure. The source will then be completely in the vapor phase, and the cylinder pressure will begin to drop as the source continues to be used. This generally provides enough time to perform a cylinder change before running out of source material. In practice, the choice of cylinder concentration is determined by the flows needed for growth and safety considerations.

The hydrides, $AsH_3$ and $PH_3$, are rather thermally stable, generally decomposing at temperatures higher than most organometallics (but lower than As and P-containing alkyls) and are thought to require substrate catalysis for decomposition under many growth conditions.[23] This is especially true for $PH_3$. Ban[39] measured decomposition efficiencies for $AsH_3$ and $PH_3$ in a hot wall reactor and found that under his experimental conditions and at typical GaAs or InP growth temperature of 600°C, 77% of the $AsH_3$ but only 25% of the $PH_3$ was decomposed. As expected, the percentage of decomposed $PH_3$ increased more rapidly than $AsH_3$ as the temperature was increased so that, for example, at 800°C, 90% of the $AsH_3$ and 70% of the $PH_3$ was decomposed. It should be recognized that the data that Ban reported should not be used quantitatively. In a cold wall MOCVD reactor, even less $AsH_3$ and $PH_3$ will be decomposed because there will be less time in which the gas is in contact with a hot surface. The poor $PH_3$ thermal decomposition efficiency and the high vapor pressure of P leads to the use of large $PH_3$ flows for the growth of P-bearing compounds and alloys. More will be said on this subject in Sec. 4.2 of this chapter.

The Group VI hydrides thermally decompose at lower temperatures than the Group V hydrides with $H_2Se$ decomposing at a lower temperature than $H_2S$. Although the growth of mixed II-VI alloys containing Se and S is possible at temperatures less than 400°C, the difference in $H_2Se$ and $H_2S$ decomposition temperature results in difficulty in compositional control at these low substrate temperatures.[11] This has driven the movement to organometallic sources for S and Se.

## 4.0 GROWTH MECHANISMS, CONDITIONS, AND CHEMISTRY

### 4.1 Growth Mechanisms

This section briefly discusses growth mechanisms as an introduction to growth conditions used in MOCVD. As mentioned earlier, MOCVD takes place in a cold wall reactor in an environment of large thermal and compositional gradients. Within this environment, a great many chemical reactions can take place, both in the vapor phase and at the growing surface. Many of these potential reactions can have extremely deleterious effects on the growing films. Fortunately, recent advances in source chemistry, equipment design, and process understanding have reduced the number of possible deleterious reactions to a small number which can be avoided.

Stringfellow[23] established a general formalism to understand MOCVD growth chemistry which is presented schematically in Fig. 4. The MOCVD growth process can be divided into four regimes: a reactant input regime, a reactant mixing regime, a boundary layer regime immediately above the substrate, and the growth on the substrate surface, itself. Growth complications that can occur in these regimes include gas phase reactions during reactant mixing, reactant diffusion and/or pyrolysis in the boundary layer above the substrate, and thermodynamic or kinetic rejection of species from the substrate. The worst of these effects can be reduced or eliminated through the use of appropriate equipment design and process conditions, as will be shown in the next two examples.

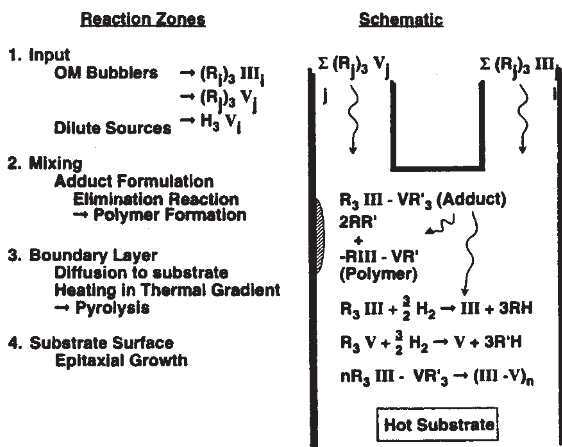


**Figure 4.** Reaction regimes for the MOCVD process. *(From Stringfellow.)*[23]

It is well known that Lewis-acid–Lewis-base gas phase reactions can occur between Group II or III organometallics and Group V or VI organometallics or hydrides, resulting in the formation of a low vapor pressure adduct of the form $R_nM\text{-}ER'_n$, where, as before, R and R´ represent a methyl or ethyl radical or hydrogen, M is a Group II or III metal, E is a Group V or VI element and n = 2 or 3 depending on whether III-V or II-VI sources are being used. In-containing adducts and some Group II-containing alkyls then decompose around room temperature to form a low vapor pressure polymer of the form $(\text{-}RM\text{-}ER'\text{-})_n$[27][29][41][42] which can condense on the walls of the system tubing or reaction chamber prior to reaching the substrate, and cause severe degradation of growth. In order to eliminate this problem, MOCVD reactors are generally constructed to minimize gas phase interaction between Lewis acid and Lewis base sources by physically separating the Group II or III sources from the Group V or VI sources until immediately before the growth area and by using high gas velocities and low pressure growth. In addition, sources less susceptible to gas phase reactions are often substituted. Two examples include the use of TMIn rather than TEIn for the growth of InP-based materials to avoid severe TEIn-$PH_3$ prereactions and the use of DMSe instead of $H_2Se$ for ZnSe-based materials to avoid DMZn-$H_2Se$ prereactions.

Gas phase pyrolysis and therefore significant reactant depletion can occur with some high molecular weight sources such as trimethyl amine alane [TMAAl—$(AlH_3N(CH_3)_3]$[32][33] and triethyl aluminum [TEAl—$(C_2H_5)_3Al]$,[32][33] which are sometimes used because they minimize the incorporation of C in the growth of AlGaAs. The gas phase pyrolysis coupled with the low vapor pressures of these sources limit the Al composition that is practical to grow with these sources to $< \sim 30\%$, even when used under reduced pyrolysis conditions, i.e., at low pressure. This low Al content has limited the use of these sources to very specialized MOCVD applications which require low C. The low C and O incorporation has made TMAAl the Al source of choice in MOMBE growth, however. The high vacuum growth conditions of MOMBE virtually eliminate vapor phase pyrolysis in this technique.

## 4.2 Growth Conditions, Chemistry and Materials Purity

The most basic growth parameters that are varied in MOCVD are the growth (susceptor) temperature and the input reactant molar flows. For the growth of III-V's, temperatures ranging from 550–900°C have

been used successfully, with the relatively low melting temperature materials such as GaAs or InP generally grown at the lower end of that range and relatively high melting temperature materials such as GaP and GaN grown at the higher end of that range. Almost all III-V growth is carried out with the input V/III ratios [moles/min of the Group V precursor(s)/ moles/min of the Group III precursor(s)] between 5 and 400 with GaAs and AlGaAs being the prototypical examples. This is because high vapor pressure Group V species in excess of that concentration required for stoichiometry are rejected back into the vapor during growth. Table 4 lists typical growth conditions for several important III-V materials

It has long been known that the growth rate of III-V's is approximately independent of substrate temperature, proportional to the inlet Group III molar flow rate, and independent of the inlet Group V molar flow rate over a wide temperature range.[21]–[23][43] Compilations of some of these data are found in Figs. 5 and 6. In similar studies, the composition of III-V alloys with mixed Group III elements has been found to be proportional to the relative input ratios of the Group III constituents.[23] An example for several alloys is shown in Fig. 7. These data are consistent with a growth regime in which the growth rate is limited by the gas phase diffusion of Group III species through a boundary layer above the substrate.

**Table 4.** Typical Growth Conditions for Various Epitaxial Materials

| **Material** | **Substrate** | **Typical growth temperature (°C)** | **Input V/III or VI/II ratio** |
|---|---|---|---|
| AlGaAs | GaAs | 700–750 | 50–100 |
| InGaAs (strained) | GaAs | 600–650 | 50–100 |
| InGaAlP | GaAs | 700–750 | 200 |
| InGaAsP | InP | 600–650 | 200 |
| InGaAs | InP | 600–650 | 200 |
| HgCdTe | GaAs | 350–400 | 0.5 |
| ZnSSe | GaAs | 420–550 | 1.5–10 |

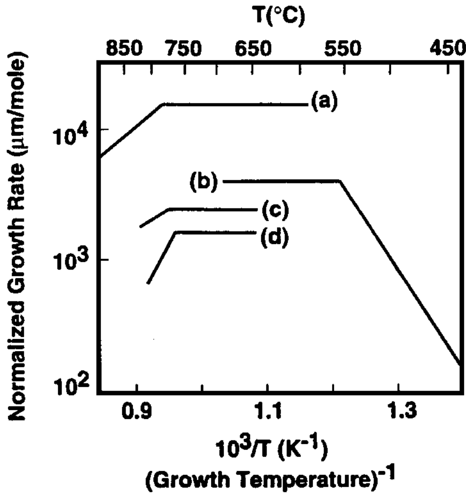


**Figure 5.** Temperature dependence of the growth rate of GaAs using TMGa. The growth rate is normalized to the inlet TMGa molar flow. Data are from (*a*) Manasevit and Simpson, [73] (*b*) Krautle, et al.,[74] (*c*) Gottschalch, et al.,[75] (*d*) Leys and Veenvliet.[76] *(From Stringfellow.)*[23]

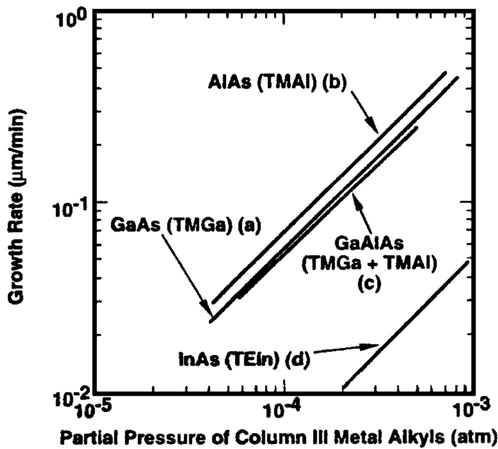


**Figure 6.** Dependence of the growth rate on the inlet partial pressure of the Group III organometallic compounds for a number of III-V's. Data are from (*a*) Manasevit and Simpson,[73] (*b*) Coleman, et al.,[77] (*c*) Aebi, et al., [78] (*d*) Baliga and Ghandi.[79] *(From Dapkus.)*[43]

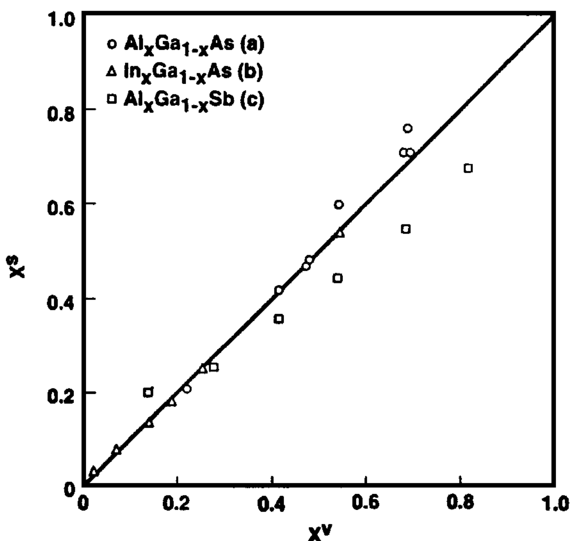


**Figure 7.** Dependence of the solid composition $x^s$ on the vapor composition $x^v$ for a number of III-V alloys. Data are from (*a*) Mori and Wantanabe,[80] (*b*) Ludowise, et al.,[35] (*c*) Cooper, et al.[81] *(From Stringfellow.)*[23]

The individual Group III elements incorporate to similar extents. Of note is the observation that heavier Group III elements tend to incorporate somewhat more poorly than lighter elements and that the difference increases with substrate temperature. For example, Al incorporates better than Ga and Ga incorporates better than In. This is thought to be due to more evaporation of these heavier, higher vapor pressure elements at the elevated temperatures of growth.

For the growth of III-V alloys with mixed Group V elements, one must consider two rather different cases. For alloys containing As and P, the relative As and P incorporation is determined primarily by the relative thermal stabilities of $AsH_3$ and $PH_3$. As previously discussed in Sec. 3.3, $PH_3$ decomposes much more poorly than $AsH_3$ at low temperatures. This is reflected in the relative incorporation of As and P in GaAsP and InAsP alloys as a function of substrate temperature. A compilation of this data is shown in Fig. 8.[23]

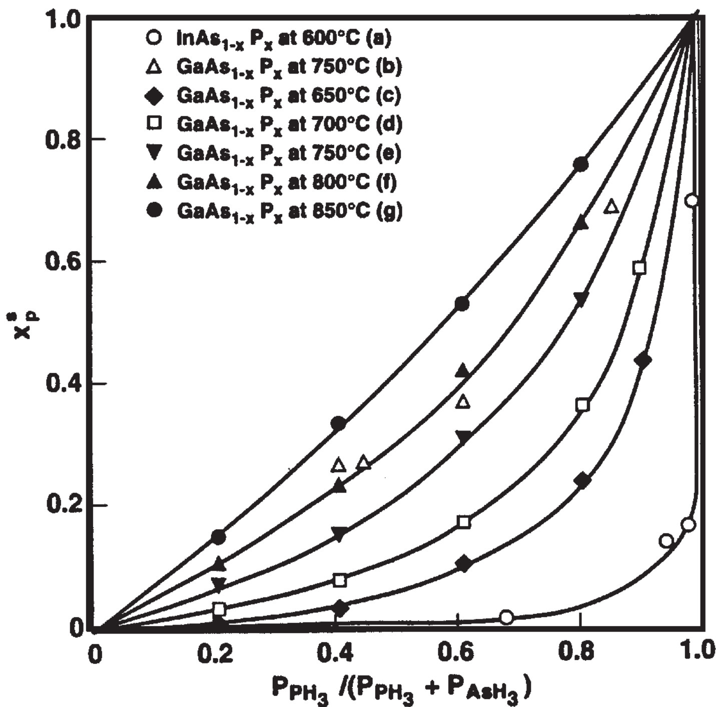


**Figure 8.** Dependence of the P concentration in the solid on the $PH_3$ concentration in the vapor. Data are from (*a*) Fukui and Horikoshi,[82] (*b*) Ludowise and Dietze,[83] (*c*), (*d*), (*e*), (*f*), (*g*) Samualson, et al.[84] *(From Stringfellow.)*[23]

Surprisingly (in view of the large chemical potential difference between the input reactants and the grown film), the incorporation of Sb into mixed As-Sb alloys is controlled by the relative thermodynamic stabilities of the binary antimonides and arsenides. The relative Sb and As incorporation can be predicted from regular solution theory[23][44] when the input V/III ratio is greater than one. In this case, alloy thermodyamics determine the relative As/Sb elemental incorporation and result in much lower Sb than As incorporation. When input V/III ratios less than one are used, the relative Sb incorporation probability increases rather rapidly to one.[23][44] This data is shown in Fig. 9.[23]

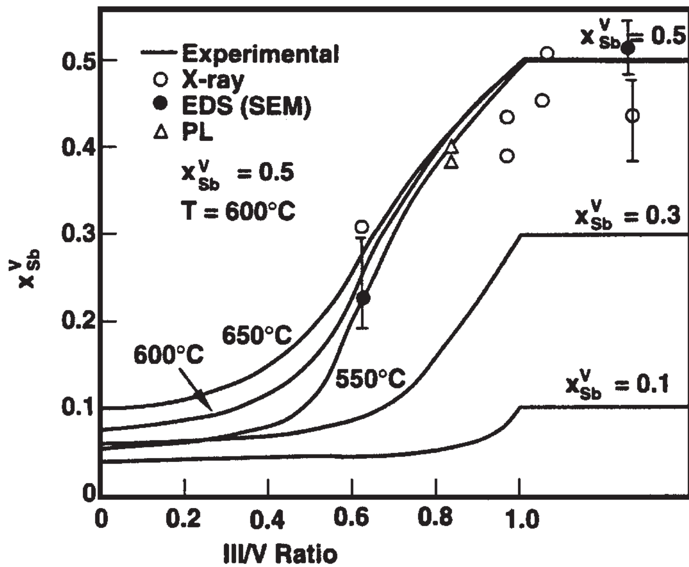


**Figure 9.** Dependence of the GaSb concentration in the solid on the III-V input ratio for various Sb vapor concentrations, $x_{Sb}{}^{v}$ and at various growth temperatures. The solid lines are calculations and the experimental conditions are shown in the box. *(From Cherng, et al.)*[44]

There has been considerably less work on II-VI's than on II-VI's. For the growth of II-VI's, VI/II input ratios greater than one are often used[11] although large overpressures of the Group II element Hg are needed for the growth of HgCdTe.[10] The VI/II ratio required for good growth of the II-VI's appears to be controlled primarily by the relative thermal decomposition of the Group VI sources at the typical growth temperatures of 350–550° C. These temperatures (or lower) are highly desirable for the growth of II-VI's because of the large diffusion coefficients in these materials (of particular importance for the growth of CdTe/HgCdTe multilayer structures), and because of the great decrease in the native defect concentration that can be realized by low temperature growth. These temperatures are just in the temperature range at which organometallic sources begin to thermally decompose (see Sec. 3.1). Thus, the growth of II-VI's is often extremely temperature sensitive. Much recent effort has been devoted to investigating sources that decompose at lower temperatures. As a result, DIPTe has become the Te source of choice for HgCdTe rather than the more stable DMTe or DETe.

Impurity incorporation of most grown materials is determined, for the most part, by the purity of starting source materials. The purity of the most widely used organometallic compounds (especially TMGa and TMIn) is consistently good, as large sales volumes have allowed suppliers to improve their synthesis techniques, source analysis, and quality control. Most of the effort in improving purity has centered around reducing metallic impurities which can be incorporated as electrically active species. The major impurity in hydride sources has often been relatively large and highly variable amounts (several tens of ppm) of $H_2O$ which has extremely deleterious effects on Al-bearing materials. This will be discussed in more detail in Sec. 5.1.

Unintentional carbon and oxygen incorporation is always of concern in Al-bearing alloys because of the extreme affinity of Al for carbon and oxygen. Carbon is incorporated as a shallow acceptor in AlGaAs and comes from the organometallic sources themselves. Carbon can be reduced to acceptable levels for laser and LED applications in standard TMGa-TMAl growth by using high V/III ratios and moderate to high pressure growth (0.1–1 atm).[45] Carbon incorporation can be further reduced through the use of the alternative source chemistries TEGa-TEAl or TEGa-TMAAl which decompose cleanly by $\beta$-elimination.[46]

Oxygen is incorporated from atmospheric contamination (discussed in Sec. 5.1) and the ready formation of alkyloxides by many of the alkyl sources.[47] Oxygen incorporates as a deep acceptor at levels of $10^{17}$–$10^{18}$ $cm^{-3}$ or higher and can greatly reduce free electron concentrations and destroy luminescence efficiency if present in sufficient quantities. Oxygen contamination can be minimized by scrupulous attention to the leak integrity of the MOCVD reactor, minimizing virtual leaks, and using gettering techniques. In addition, the use of TMAAl greatly reduces oxygen contamination because of the lack of reactivity of this source with oxygen. [46] Thus, TMAAl can give the benefit of both reduced carbon and oxygen as long as the low vapor pressure and low decomposition temperature of this source can be accommodated.

Carbon and oxygen contamination does not appear to be major cause for concern for non-Al bearing alloys unless extremely high purity is desired. In fact, material with low carbon and oxygen can be grown even when using unfavorable growth conditions and in systems that have small leaks to atmosphere.[48] For the growth of very high purity GaAs, high V/III ratios and low temperatures (~ 600°C) have been found to lead to significant reductions in background carbon.[22]

## 5.0 SYSTEM DESIGN AND CONSTRUCTION

In this section, we consider system design and construction. Much of the material discussed in the previous sections will be used in this section to formulate guidelines for the design and construction of an MOCVD system. Figure 10 is a block diagram of an MOCVD system in which functional subsystems are defined. Subsystems consist of reactant storage (hydrides, organometallics, and $H_2$); a gas manifold in which flows are metered, controlled, and directed to the proper locations; a reaction chamber in which deposition takes place; and an exhaust which generally includes a pump for low pressure operation and evacuation of the chamber for substrate loading and unloading; and a scrubber. In this section, we first consider the generic issues of leak integrity and oxygen gettering techniques. We then consider the design and construction of the functional subsystems in more detail. Our emphasis will be on the gas manifold and reaction chamber subsections because these are the system subsections that primarily effect the quality of the material that is grown in MOCVD systems.

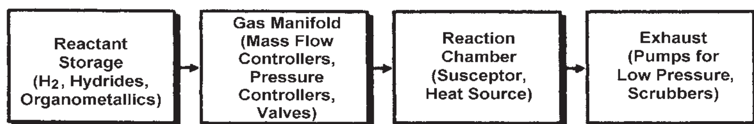


**Figure 10.** Schematic block diagram of an MOCVD system showing functional subsections.

### 5.1 Leak Integrity and Cleanliness

At this point, some comments on the importance of leak integrity and general cleanliness are in order. In all phases of equipment design and construction, it is absolutely critical that leak integrity be established and that components be cleaned and assembled in a clean environment. Not only can system leaks allow toxic chemicals escape to the atmosphere thus presenting a safety hazard, but room air can readily contaminate the

reactants and the system. Although a certain amount of $O_2$ and $H_2O$ contamination can be tolerated in the growth of most compound semiconductors,[48] $O_2$ and $H_2O$ can have extremely deleterious effects on material containing Al (AlGaAs, InGaAlAs, and InGaAlP).[49] In the growth of AlGaAs, for example, altered composition, degraded morphology, deep electronic levels and low photoluminescence intensity have been observed in samples grown in a contaminated system.[48][50]

Oxygen contamination can also come from the hydride sources[51] and organometallics.[47] Hydride contamination can be reduced by several gettering techniques which will be discussed in more detail in the next subsection, while organometallic source contamination is addressed either by growth conditions (mentioned in the next subsection) or source chemistry, as discussed in Sec. 4.2.

In addition to eliminating leaks to atmosphere, it is also important to minimize the number of virtual leaks in the system. Virtual leaks serve to trap residual gases and are very difficult to flush, thus providing internal sources of air contamination. In addition, they trap reactants and thus can contribute to compositional grading, especially at interfaces in grown material.

Finally, residual $H_2O$ in hydrides cylinders often comes from the cylinder walls. Most vendors have addressed this issue by using a variety of passivation techniques to reduce internal surface area and "seal" the surface.

## 5.2 Oxygen Gettering Techniques

Because of the extreme sensitivity of Al-containing materials to $H_2O$ and $O_2$ trace contamination, a considerable amount of work has been done on gettering of these contaminants from the gas stream. It is useful to point out that the need for $O_2/H_2O$ gettering in the growth of Al-containing materials can be reduced or eliminated by using a growth temperature greater than 780°C.[50] However, heterostructures that contain both Al and non-Al containing layers often cannot be produced at high temperatures because non-Al containing materials often degrade at the high temperatures needed to insure high quality Al-bearing materials. For example, the morphology of InGaAs degrades significantly at high temperatures due to a transition from two to three dimensional growth.[52] Thus, a 980 nm pump laser structure that contained both strained InGaAs and AlGaAs layers needs to be grown at different temperatures for each kind of layer.

In addition, compositional control becomes difficult at high temperatures due to differential evaporation rates of constituents. Thus, much effort has gone into removing contaminants from both the gas lines and the reaction chamber.

The first oxygen gettering technique reported was the use of graphite baffles in the reaction chamber.[53] Although highly effective at reducing oxygen incorporation in AlGaAs, the baffles lead to considerable degradation in interfacial abruptness and were quickly abandoned.

Other early attempts involved the use of an Al-Ga-In melt through which the carrier gas was bubbled.[51] The Al in the melt reacted with oxygen and oxygen-containing species to form an $Al_2O_3$ scum which floated to the top of the melt. However, liquid bubblers required the use of particle filters to prevent small, atomized liquid metal particles from being swept into the reaction chamber where they would degrade morphology and regeneration of the bubblers proved to be messy and clumsy.

The most common means of gettering $H_2O$ and $O_2$ from gas streams is the use of in-line getters. The gas stream passes through a commercially available proprietary organolithium resin or proprietary zeolite or Zr-alloy and $H_2O$ and $O_2$ are preferentially removed chemically with little or no chemical reaction with the main constituent and without adding additional impurities to the gas line. Both resins and zeolites or alloys are commercially available for both active reactants ($AsH_3$ and $PH_3$) and carrier and flush gases ($H_2$ and $N_2$). Some resins change color as they become saturated with oxygen-containing species, thus allowing easy monitoring of the useful life of the resin. Again, this feature is commercially available. In general, the getter is shipped in a small, stainless steel cylinder and is placed in the gas stream immediately before the point of use. The installation should contain valves and bypasses for the safe, contamination-free installation and removal of the cylinder when it is saturated. Because a considerable heat of reaction occurs when the getters contact oxygen, the cylinder needs to be evacuated or flushed of air during installation. Hydride getters should also have a means of oxidizing any residual hydride contained within the cylinder after removal.

## 5.3 Gas Manifold Design

The gas manifold contains the computer controlled valves, mass flow and pressure controllers, and tubing that regulate and direct the flows and pressures of all reactants. It is desired that the flows be accurately controlled

with a minimum of fluctuations, particularly when the flows are redirected to a different destination. Most of the major reactants require carrier gas flows in the range of 1 to 400 $cm^3$/min for growth rates in the range of 1 to 10 μm/h. Gas flows can be accurately metered by electronic mass flow controllers. The low reactant flows are then added to a much larger (typically 2 to 30 l/min)dilution flow. The dilution gas is usually $H_2$ (although He or $N_2$ has been used to take advantage of the much different thermal properties), and it acts to increase the speed with which the reactants are swept to the reactor. The dilution gas and the reactant flows are generally mixed individually as illustrated schematically in Fig. 11. In this case, each source has a dilution flow associated with it. The individual diluted gas streams then mix in common tubing or at the reactor inlet. Generally, Group III or II source flows are kept separate from Group V or VI source flows until immediately before introduction into the reactor to prevent predeposition reactions from occurring within the tubing.

The separate introduction of reactants eliminates gas phase prereactions, but can lead to non-uniform gas composition across the cross section of the reaction chamber.[29] Non-uniform gas composition can lead to thickness and film composition variations unless some form of gas stream mixing occurs within the reaction chamber. In fact, gas injection designs are generally a tradeoff between these two effects with the resolution coming from a combination of baffles to promote mixing and low pressure to reduce the time of contact between reactants.

Gas manifolds are designed in a "vent/run" configuration, also shown schematically in Fig 11.[54][55] In this configuration, reactant flows are established in a line that goes directly to vent prior to their introduction into the growth chamber. The establishment of flows helps to reduce transient flow effects and allows the temperature of the organometallic cylinder to reach a constant steady state value. The reactant flows are then simply switched from the vent line to the line that goes to the reaction chamber ("run" line) in order to initiate growth.

Because the simultaneous arrival of reactants at the growth interface is critically important for interfacial abruptness in the growth of III/V and II/VI heterostructures, vent/run switching of individual reactants must also occur simultaneously. To facilitate this, many designs have individual valves ganged together in extremely close proximity while others use specially designed valve blocks that incorporate a number of valves into a single valve body. In either case, care must be taken to ensure smooth walls to reduce

dead volumes in the tubing so that all reactants arrive at the reaction chamber at the same time.

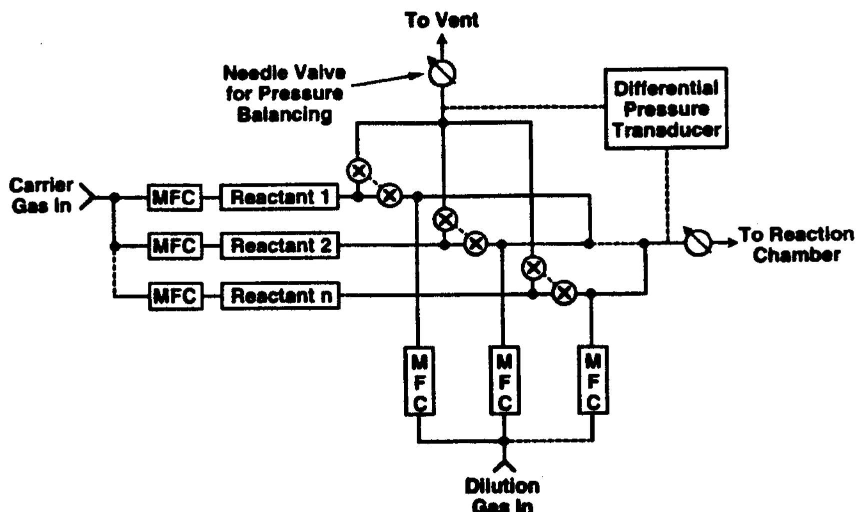


**Figure 11.** Schematic diagram of reactant and dilution gas mixing scheme.

Equally important is the assurance of pressure balancing[54][56] between vent and run legs to prevent either forward or backward flow surges during switching due to pressure differences between the vent and run lines. These can drastically alter compositions at interfaces. Pressure balancing can sometimes be achieved passively if the flows in both vent and run lines see essentially no pressure drop between the source and the pump. This situation occurs most readily when the gas manifold is operated at low pressure, the lines are short and have a large-enough cross sectional diameter, and flows are relatively small, say < 2 l/m through 0.45 cm ID and < 2 m long tubing. In larger systems with numerous sources, flow balancing is difficult to achieve passively and active pressure balancing is generally used. Pressure balancing is accomplished through the use of electronically controlled needle valves using differential pressure measurements of the vent and run lines as feedback. Pressure balancing is facilitated if the vent and run lines are physically identical so that the flow impedances per unit length of tubing are identical.

Mass flow and pressure controllers are critical components for a system. A flow controller uses a flow meter as feedback to an electronically controlled needle value which controls the flow, as shown schematically in Fig. 12. The flow meter works by using a thermometer (generally a thermistor) to measure temperature decreases through an integral flow bypass. The flow can then be calculated from knowledge of the flow dynamics of the flow controller and the thermal conductivity of the gas for which the flow controller is calibrated. Because the thermal conductivity of gases can vary tremendously, one should use caution in quantitatively using flows set by a flow controller calibrated for a particular gas, say $H_2$, with a different gas, say $N_2$. Pressure controllers are similar to flow controllers, with the feedback provided by a pressure transducer rather than a flow meter. Given their complexity and the extensive use of elastomer seals rather than metal seals, flow and pressure controllers are typically considered to be particularly vulnerable to malfunction in reactors. Increasingly, separate measurements are used to verify flows, as will be discussed in the last section on future developments.

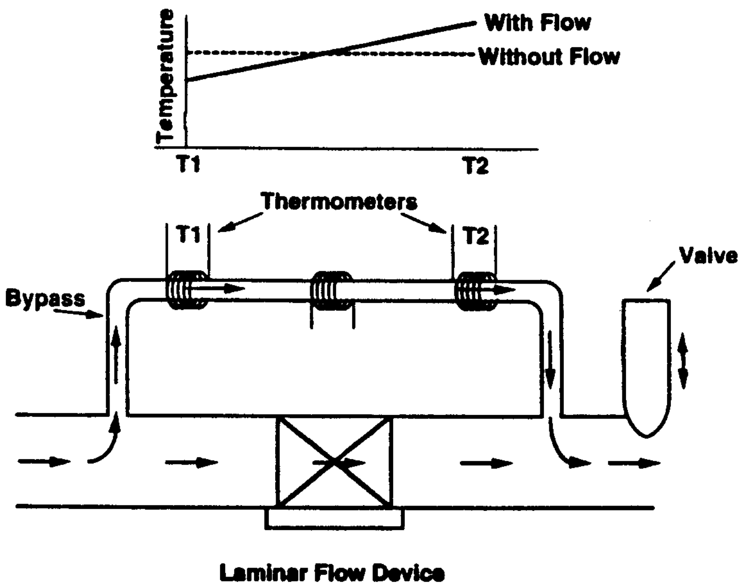


**Figure 12.** Schematic diagram of a flow controller.

## 5.4 Reaction Chamber

The reaction chamber is where the thermal decomposition reaction and deposition occurs. Because the reaction chamber of an MOCVD system contains the longest time constant for reactant flushing, the abruptness of interfaces is largely controlled by this section. In addition, the lateral uniformity of material grown is almost entirely controlled by reaction chamber design. Chambers are cold wall, that is the susceptor upon which the substrate sits is the only part of the reactor that is deliberately heated. The cold wall design reduces the probability that competing chemical reactions at the walls (such as thermal decomposition) will interfere with film growth. Of course, cold wall designs also favor the establishment of thermally driven natural convection in the chamber because of the large temperature gradients present. This natural convection can lead to recirculation cells in the chamber which in turn result in non-abrupt interfaces and reactor non-uniformities. These can be eliminated by reactor design and growth conditions.

Often, reaction chambers are provided with a vacuum and/or $N_2$ flushed load lock. The load lock keeps ambient air from entering the chamber and provides an additional level of safety during sample loading and unloading. The chamber walls can be either water or ambient-air cooled. Ambient air cooled systems can have wall temperatures of 200°C for susceptor temperatures of 650°C.[57] Unintentional changes in wall temperatures can have significant effects on the composition of films grown.

Reaction chamber walls are generally made of either fused silica ("quartz") or stainless steel. Fused silica is often used in single wafer research reactors because of its chemical inertness and transparency, the latter allowing the use of externally mounted IR lamps for susceptor heating. However, the fragility of fused silica and general need for use of elastomer seals at the reactant inlet have led to the increased use of stainless steel as the wall material. With stainless steel chambers, connections to the reactant inlet can be made by the generally more reliable welding and metal compression seals. Windows can be provided in stainless steel systems to provide optical access to the system. However, care must be taken to ensure that chamber temperatures remain relatively low (by water cooling or other means) to prevent warping of the stainless steel.

Substrate and susceptor heating is typically provided by either an infrared (IR) lamp source or by radio frequency (rf) induction heating. Both fused silica and stainless steel chambers can have either kind of heating, mounted either external or internal to the system.

The susceptor must be electrically conducting (for rf heating) or optically absorbing (for IR heating). In addition, the susceptor must be chemically inert at the growth temperature so that the film is not contaminated. It is also highly desirable (for some designs mandatory) for the susceptor material to be machineable so that pockets can be provided in the surface to hold the substrate in place. The susceptor is generally fabricated from graphite coated with SiC or pyrolitic graphite, or is made of a transition metal such as Mo.

There are a number of reaction chamber geometry designs that have been demonstrated to address the issues of interfacial abruptness and uniformity. They either introduce the gas stream at a position normal to the substrate surface ("vertical" geometry) or parallel to the wafer surface ("horizontal" geometry). In either case, the chamber is generally designed to ensure laminar flow across the substrate surface, that is, the gas flow lines are parallel to the substrate surface in the region immediately above the substrate. Thickness uniformity is assured if the "boundary layer" that separates the substrate from the gas stream is of uniform thickness.

Many single wafer "research" reactors are of a horizontal geometry as depicted in Fig. 13. In this case, the reactant flow is introduced parallel to the substrate. In the horizontal geometry, reactor depletion effects cause the thickness and composition of grown material to vary with distance along the susceptor, and lack of reactant spreading can cause center-to-edge variations. Reactant depletion can be modeled[58][59] from the flux of reactant molecules to the substrate surface through a boundary layer as

Eq. (3) $$J = -DN_0/\delta$$

where $D$ is the diffusion coefficient of the reactant molecule within the boundary layer, $N_0$ is the inlet reactant concentration, and $\delta$ is the boundary layer thickness. If the susceptor is parallel to the inlet gas (susceptor angle of 0°), the diffusion boundary layer thickness is

Eq. (4) $$\delta = (\pi Dx/v)^{1/2}$$

where $x$ is the distance along the susceptor and $v$ is the horizontal gas velocity. Equations (3) and (4) predict a linear decrease in flux (and

therefore, thickness) along the gas flow. For an alloy, values of diffusion coefficient, *D*, for each of the reactants will vary, thus, causing compositional variations as well.

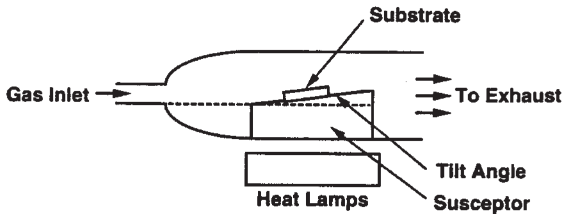


**Figure 13.** Schematic horizontal reaction chamber geometry.

Depletion effects can be compensated for by using small (typically 5–10°) susceptor tilts. However, as shown in Fig. 14, tilting the susceptor does not completely eliminate depletion. Furthermore, tilt does not address center-to-side variations which are caused by inadequate lateral spreading of the gas stream in the chamber and by chamber walls that are too close to the susceptor edges. A better way to compensate for both of these effects is to use rotation of the substrate. Rotation both decreases thickness and compositional variations on a wafer and imparts a rather predictable radial symmetry to the thickness and compositional profiles. Woelk and Beneking[60] obtained standard deviations of thickness and compositional uniformity of $< 1\%$ over the inner 40 mm of a 50 mm InP/InGaAs wafer using substrate rotation.

Implementation of substrate rotation in a horizontal geometry reactor presents a difficult mechanical problem, since direct rotational coupling is generally blocked by the heating source. Thus, indirect means must be used to provide rotation. Probably the most commercially successful is the use of gas foil rotation.[61][62] In gas foil rotation, shown schematically in Fig. 15, the susceptor is mounted on a stylus while $H_2$ or other inert gas is directed to impinge on the susceptor tangentially through the use of spiral grooves. The tangential impingement coupled with buoyancy provided by heating of the gas in the body of the hot susceptor tends to lift the susceptor slightly and impart rotation without any complicated mechanical coupling. Typically, rotation flows of only 50 $cm^3$/min

are used so that flow dynamics in the reaction chamber are not altered. Gas foil rotation schemes have been successfully implemented on both single wafer and multiple wafer systems. An example of a successful multiwafer horizontal system that uses gas foil rotation is shown in Fig. 16.

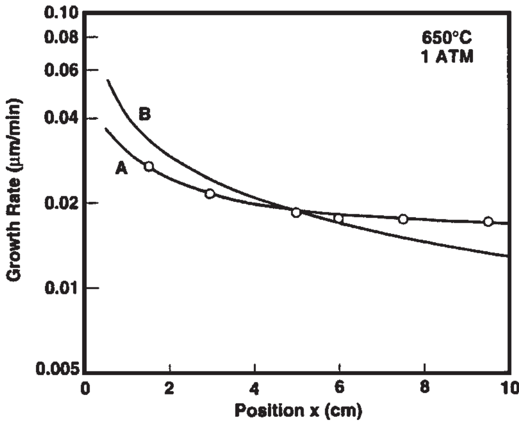


**Figure 14.** Growth rate of GaAs as a function of the distance along the susceptor. *(A)* Numerical calculation (tilt angle = 7°). *(B)* From Eq. (3) and (4) (tilt angle = 0°). *(From Ghandi and Field.)*[59]

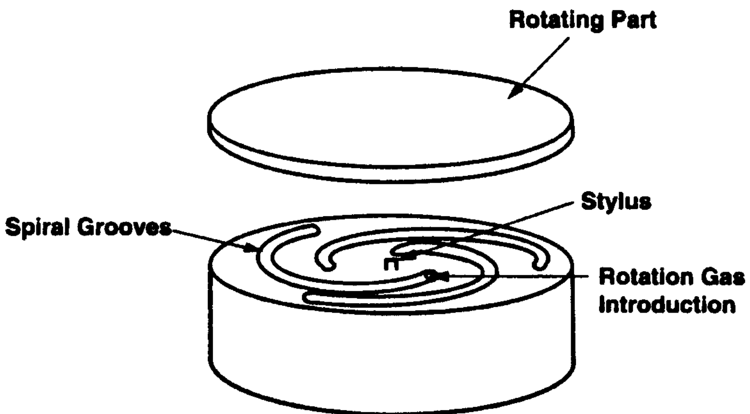


**Figure 15.** Schematic drawing of a gas foil rotation susceptor. *(From Frijlink.)*[61]

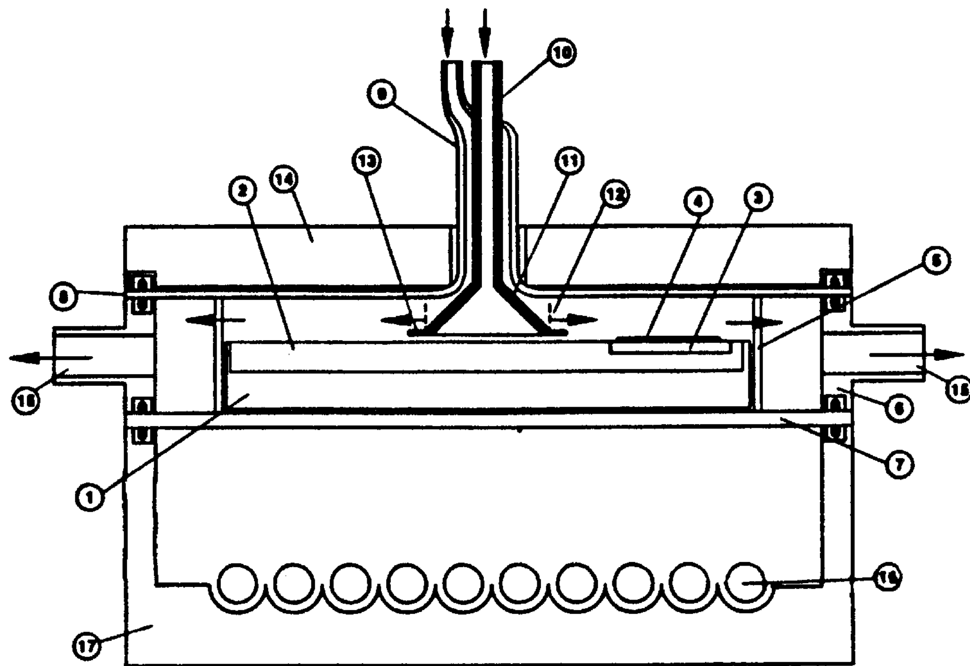


**Figure 16.** Schematic drawing of a multiwafer reaction chamber that uses gas foil rotation for individual substrates. *(1)* base, *(2)* rotating main platform, *(3)* rotating satellite that supports a substrate *(4), (5)* perforated fused silica ring for exhaust, *(6)* $H_2O$ cooled stainless steel ring, *(7)* lower fused silica disk that supports the substrate holder, *(8)* upper fused silica disk, *(9)* outer tube for organometallics and dopants, *(10)* inner tube for hydrides, *(11)* cone for gas injection, *(12)* cylindrical entrance grating for organometallics, *(13)* deflector ring to separate Group III and Group V reactants, *(14)* $H_2O$ cooled Al top plate, *(15)* exhaust tube, *(16)* IR lamps, *(17)* lamp reflector. *(From Frijlink.)*[61]

The vertical geometry was the original configuration used by the originators of MOCVD.[2] Under idealized conditions, this configuration should approximate "stagnation point flow" conditions. Stagnation point flow occurs when uniform flow is introduced normal to a semi-infinite flat surface and is predicted to result in a uniform boundary layer with no recirculation cells.[63] Unfortunately, the finite susceptor size, presence of reactor walls, and the large thermal gradients of real vertical reactors causes departure from the idealized stagnation point flow conditions and makes these reactors very susceptible to the establishment of non-uniform boundary layers and thermally induced convection and recirculation cells upstream of the hot susceptor during growth. These convective cells are very hard to model and can cause compositional grading at interfaces and non-uniform growth. Nevertheless, with care, vertical reactors can be engineered to approximate stagnation point flow conditions. Figure 17 shows a successful implementation of this kind of reactor.[63] In this system, lateral flow field uniformity is provided by a number of injection flow controllers which can be individually tuned to produce excellent uniformity. The large gas introduction area is almost as large as the susceptor area and, with sufficient flow, will also reduce the presence of thermally driven recirculation cells through forced convection at the sidewalls.

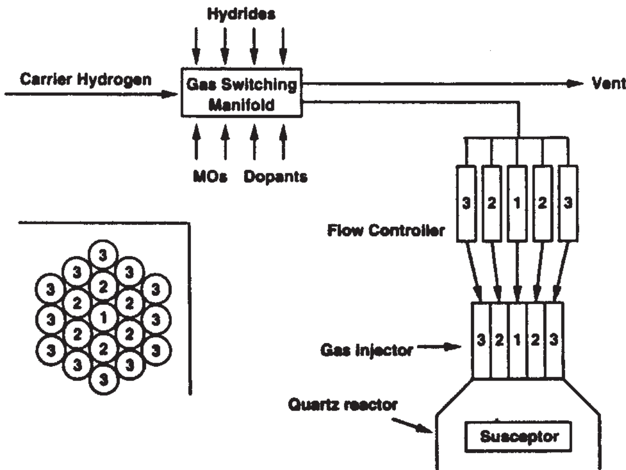


**Figure 17.** Schematic drawing of a single wafer stagnation point flow reactor. (*From Kondo, et al.*)[63]

Another approach to the use of vertical reactors that is amenable to multiwafer growth is the use of rapid (500–1500 rpm) susceptor rotation. Systems of this sort are referred to as "rotating disk" reactors, in analogy to rotating disks that are often set up in liquid processes to provide laminar flow and uniform deposition or etching.[64][65] Rotating disk reactors look schematically very much like the stagnation flow reactor depicted in Fig. 17, including the provision to adjust the lateral flow field, with the addition of extremely fast susceptor rotation through a rotating seal. Due to viscous drag imparted on the gas by the rotating susceptor, rapid rotation imparts a forced flow pattern onto the gas stream. The forced flow pattern overcomes thermally induced convection and "pumps" the flow stream lines to the surface of the susceptor where they then flow laterally over the susceptor surface. The thin boundary layer that is formed increases the temperature gradient in the gas stream immediately above the susceptor, and generally allows both uniformity and interfacial abruptness. Multiwafer reactors are produced by making the susceptor diameter larger and placing the multiple substrates off center of the rotating susceptor. Depletion effects still exist in this multiwafer rotating disk configuration. In one commercially available implementation of this design, one can compensate for these by adjusting the apportionment of flows between the center and edge of the susceptor.[63] Note that a calculation of flow dynamic effects in rotating disk reactors requires the use of numerical techniques.

It is important to differentiate between the use of rotation in a rotating disk reactor and the effect of rotation in a conventional horizontal (or early vertical) reactor. In the latter reactors, rotation is used to compensate for depletion effects by providing the same reactant exposure path for each point on a wafer of any given radius. This provides a radial dependence to a thickness or composition profile. However, the rotation is not intended to affect the flow dynamics in the reactor. In contrast, rotating disk reactors use rotation as a primary means of controlling the flow patterns in the reactor and rotation becomes an integral part of the process. Put another way, if a wafer in a conventional reactor is not rotated, good material (although not very uniform) can be grown. If a wafer in a rotating disk reactor is not rotated, no growth or poor growth is the result.

## 5.5 Exhaust and Low Pressure MOCVD

In recent years, MOCVD systems have evolved to operate largely at reduced pressures, typically 20–200 Torr, because low pressure operation

is more amenable to the simultaneous achievement of large area uniformity and interface abruptness. The most extreme form of low pressure growth is referred to as MOMBE and will not be discussed in this chapter. Pressure reduction in conventional low pressure MOCVD (LP-MOCVD) is accomplished through the use of a vacuum pump which is specially prepared for chemical service and which can be obtained commercially from several vendors. Because of the particulate material that is generated in the reactor, particle filters for the pump oil and the exhaust are usually required. In addition, an inert gas ballast should be used during operation to prevent dissolution of toxic reactants in the hot pump oil.

In order to control the pressure in the chamber, the pump must be throttled using a butterfly throttle valve controlled by a feedback loop to the growth chamber pressure. Both vent and run lines from the gas manifold are directed and controlled by the throttle valve. Periodically, particulate that has accumulated on the throttle valve needs to be removed. This is generally indicated by pressure fluctuations in the chamber and a general inability to control pressure.

From the pump, the reactor effluent is generally directed to a scrubber to remove toxic materials from the gas stream. Scrubbers can be either wet,[66] using a bromate solution, or dry, using adsorption and subsequent oxidization on a suitable medium such as activated C.[67] Both kinds of scrubber have been shown to be highly effective in removing hydrides from the gas stream. For example, in this author's laboratory, $PH_3$ mole fractions of 6% have been reduced to < 10 ppb concentrations. It is important to pay strict attention to manufacturer's instructions in both use and disposal to minimize safety and environmental concerns.

## 6.0 FUTURE DEVELOPMENTS

MOCVD technology has reached sufficient maturity so that future developments are expected to revolve around enhancing the usefulness of the technology for applications rather than in changing the fundamentals of deposition. Three areas appear to be particularly fruitful: improved uniformity over larger areas, in situ diagnostics and control, and the establishment of high quality deposition in additional materials. Much of the recent work has been directed toward improved sources and was discussed in Sec. 3.1. Additional work on improved organometallic sources that appears in the literature is directed toward reducing carbon and oxygen

contamination in MOMBE where inadvertent contamination from sources can be severe. Many of these sources are not suitable for MOCVD because of either very low vapor pressures or low decomposition temperatures. Other areas of MOCVD research, such as photoenhanced growth and atomic layer epitaxy, have a much more narrow focus and address much more specific materials-related problems and will also not be discussed in this chapter.

### 6.1 Improved Uniformity Over Larger Areas

Tighter device specifications and increased device complexity, coupled with the excellent uniformity demonstrated by MBE growth, continue to drive the need for improved thickness, composition, and doping uniformity over larger areas. For example, as telecommunication laser performance moves to higher speeds and longer distances, the lasing wavelength control and uniformity need to get increasingly better to reduce the effects of fiber dispersion. Wavelength control in quantum well lasers relates directly back to improved compositional and thickness uniformity. Exploratory devices like SEL's and SEED's that use reflector stacks require extreme precision and uniformity of thickness to work at all.

Likely approaches to improved uniformity are a continuation of the approaches already used to obtain the present level of uniformity. These include modifying the hydrodynamics and the thermal geometry of the reactor to obtain a uniform boundary layer thickness, uniform incorporation of species, and uniform evaporation rates from the surface. Larger areas are likely to be addressed by taking concepts that have worked with smaller areas and scaling them to large areas, probably through the use of rather complicated mechanics. Several recent commercial examples of this are a reactor from Emcore that uses rotating disk technology and can grow films on nine 100-mm wafers at a time and one from Aixtron that uses gas foil rotation and can grow films on thirty-five 50-mm wafers at a time.

### 6.2 In-situ Diagnostics and Control

The need for in situ diagnostics and run-to-run control and predictability is driven by many of the same needs as improved uniformity discussed in Sec. 6.1, as well as a desire to more rapidly diagnose and fix

reactor problems. For improvements in this area, the incremental approaches that can be used for improved intrawafer uniformity are not adequate. Major advances in measurements are needed to improve the ability to control the MOCVD process and interwafer uniformity, largely because advances here must be in-situ, in contrast to the ex-situ measurements that have been used to improve intrawafer uniformity. Unfortunately, the diagnostics (reflection high energy electron diffraction—RHEED) that have proved vital for the establishment of superior MBE diagnostics and control cannot be used in MOCVD because of the requirement of high vacuum ($< 10^{-5}$ Torr) for the use of electron diffraction. Synchrotron x-ray diffraction has been investigated as an in-situ diagnostic,[68] but obviously, any technique that uses synchrotron radiation cannot be a routine diagnostic tool.

There are two major approaches to improved in situ diagnostics: the use of acoustic cells to monitor the molar flow of the organometallic source into the reactor and the use of optics (generally reflectometry) to monitor the growing film, itself. Acoustic cells address the issues of: *(a)* how to ensure that the organometallic cylinder is not empty (without producing a bad wafer) and *(b)* how to measure the molar flow of material from the cylinder which may not be the same as would be calculated by Eq. (2) in Sec. 3.2 because of a miscalibrated mass flow controller or source depletion effects. The former desire is based to a large extent on the inability to easily determine how much of the source remains in the cylinder. The source pressure is only a function of temperature, not the amount of material, for condensed phase sources while the presence of temperature baths and hardpiped lines make weight measurements unreliable.

Acoustic monitors[69] are placed in the reactant lines that connect the source cylinder with the gas mixing area of the gas manifold. The monitors take advantage of the concentration dependence of the speed of sound in a given medium, and use a short stainless steel cell that contains the flowing chemical and carrier gas to measure the vapor phase concentration of an organometallic chemical. Ultrasonic transducers are provided at opposite ends of the cell. For a given cell geometry and temperature, the time for acoustic pulses to traverse the transducers is a measure of the speed of sound in the gas mixture and thus the concentration of the organometallic. The acoustic cell has been found to be particularly useful to monitor TMIn which, as previously noted, often suffers from depletion, although, in the future, all sources could be monitored using acoustic cells and even be made part of a mass flow controller feedback loop.

Optical monitoring of the growing film, itself, can use either specular or diffuse scattered light. Monitoring the growing film has obvious advantages in the ability to directly obtain diagnostic information on the film product, itself. Diffuse scattering[70] will allow the in-situ monitoring of morphology or morphological changes that might occur during heatup or growth. As such, it would provide valuable diagnostics for growth problems that might occur, for example, at interfaces that would be covered over by later stages of growth. Figure 18 is a schematic of an implementation of diffuse scattering in a vertical reactor.

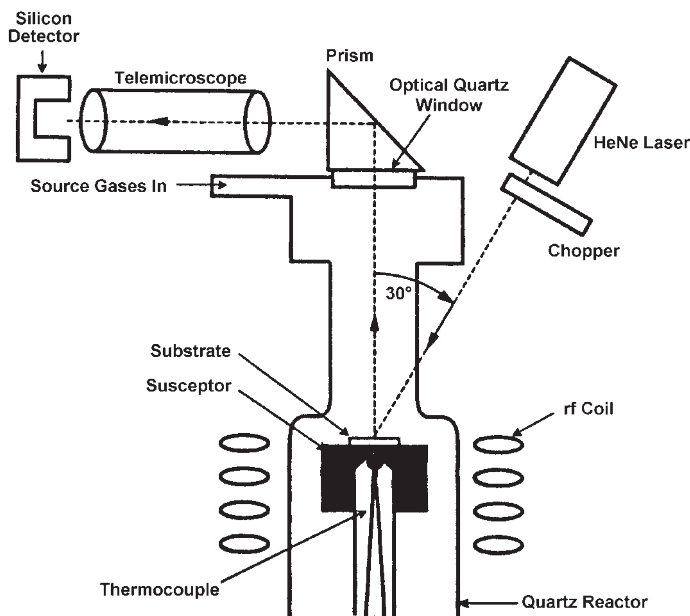


**Figure 18.** Schematic of an MOCVD reactor set up for in situ monitoring using diffuse scattering. *(From Bertness, et al.)*[70]

Specular reflectometry can give even more information on growing film. Figure 19 is a schematic of a specular reflectometry implementation which has a configuration similar to that used for diffuse scattering, except for the angles of incidence and reflection. Spectrally resolved reflectance measurements[71][72] produce interference patterns that can be used to measure growth rates in situ. This could provide an alternative feedback to

growth recipes so that thicknesses could be tuned in precisely. This technology has been demonstrated for GaAs/AlAs reflector stacks, which produce data that are relatively easy to interpret because the interference patterns produced by the reflector stack periodicity as accurately modeled. However, there are a large number of important structures with low or no periodicity (conventional laser and light emitting diode structures, for example) for which the interpretation of reflectance scans is not straightforward. Work in the future will involve inventing a fast and robust real time analysis algorithm that can be applied to less periodic structures to make specular reflectometry more universally useful. Even without advanced algorithms, considerable insight into non-planar growth can be obtained from reflectometry. A recent example from Ebert, et al.,[85] discusses the use of reflectometry in assessing the quality of grating overgrowth for InP/InGaAsP distributed feedback lasers.

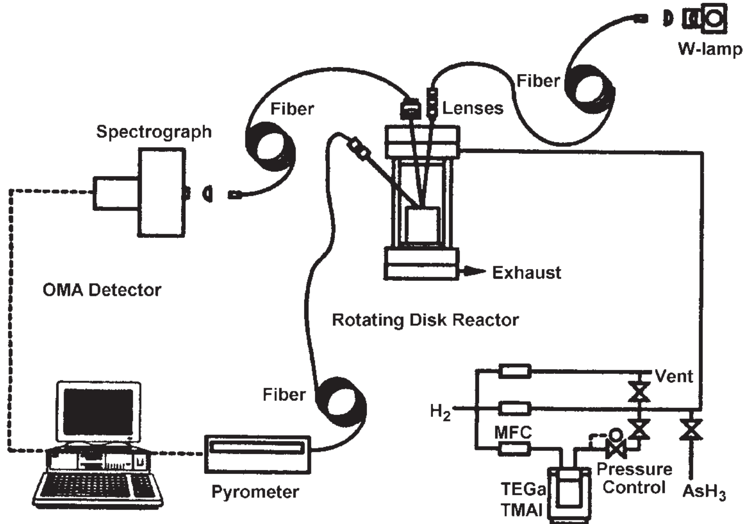


**Figure 19.** Schematic of an MOCVD reactor set up for in situ monitoring using specular reflectometry. *(From Killeen and Breiland.)*[72]

### 6.3 New Materials

Although MOCVD has been used to deposit a large number of III-V and II-VI materials and structures, early exploratory device work on AlGaInN and ZnSSe blue-green lasers and light emitting diodes has used MBE rather than MOCVD. The major breakthrough for these materials was the establishment of robust n and p dopants, which took advantage of the decoupling between substrate temperature and the production of active species that can occur in MBE. In MOCVD, coupling between the growth temperature and the production of active source species is implicit in the technique. However, recently, annealing has been shown to result in high activation of dopant species and has allowed MOCVD to become well used for these kinds of alloys and structures.

In addition to the compound semiconductor work that has been the focus of MOCVD technology since its inception, interest has recently developed in extending the technique to the growth of materials for other electronic applications such as oxides, high critical temperature superconductors, dielectrics, piezoelectrics, and metals. These materials present challenges in both growth conditions—the need or desirability of very high (oxides) or very low (metals) temperatures, for example—and chemistry (oxides, in particular). Sources and source chemistry and the use of compatible materials in reactor construction appear to be the main thrusts of present work on these new materials.

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# 5

# Feature Scale Modeling

*Vivek Singh*

## 1.0 INTRODUCTION

The goal of this chapter is to develop a fundamental understanding of the mechanisms by which the processes of chemical vapor deposition and dry etching proceed, with emphasis on the physics occurring at the length scale of the evolving feature. It is useful, at the very outset, to discuss the issue of scales and the need to divide the modeling section of this book into reactor scale and feature scale portions.

It can be safely asserted that most etch and deposition systems operate much below atmospheric pressure. At the same time, the size of the patterns that are being transferred on the wafer are getting smaller. This combination of low pressure and submicron features implies that gas phase transport, at the length scale of the trench being filled or the contact being etched, occurs in the free molecular flow regime. In other words, particles are traveling in straight line trajectories, and thus the continuum transport equations are no longer valid at that small length scale. On the other hand, depending primarily upon pressure, this may not be true at the length scale of the reactor itself, where the continuum equations might hold. Thus, there are two very disparate length scales in an etch or deposition system, and this leads to different descriptions of the physics occurring at the two scales.

If the reader is convinced that the physical phenomena that occur during deposition and etching proceed along two separate length scales, let

us now address the question of how this physical understanding is relevant to the process engineer. An incomplete list of "product" (wafer level) issues that face technology development and manufacturing is as follows:

1. High aspect ratio via fill
2. Sidewall profile control
3. Deposition of oxides of different quality
4. Etch stopping
5. Micro-loading
6. Pattern dependent etch rates
7. Anisotropic etching (e.g., nitride spacers)
8. Microtrench formation
9. Effect of resist pullback

Understanding the feature scale phenomena sheds useful light on all of the above topics, to varying degrees. The first item listed, high aspect ratio via fill, for example, is a fabrication concern in each new technology development cycle. A reactor that is adequate to deposit tungsten in a fashion that completely fills a 0.4 μm via, may not fulfill the same requirement for the new technology generation involving 0.25 μm vias. Experimental verification of this conjecture can be time-consuming and expensive. Simulations of the deposition process inside the via, on the other hand, can quickly define the processing limitations of the equipment, and suggest a smaller experimental design with which to validate the predictions. Of course, simulations can not completely solve all the feature scale problems. In the above list, pattern dependent etching is an example of areas where the modeling work is only recently being initiated, and as such the models, when they exist, tend to be more empirical. This issue of realistic modeling capability will be carefully addressed throughout this chapter, and summarized at the end.

Another issue that is most appropriately addressed at the outset is wafer-size. With the impending migration to 12 inch wafers, the validity of models developed and calibrated with data on 8 inch wafers may be called into question. At the feature scale, however, the impact of this migration is minimal. Wafer scale uniformity is naturally going to be more difficult to control. Feature scale models, on the other hand, are only concerned with the processing inside a feature *relative* to the processing occurring on a flat surface at the *same* location on the wafer. As long as the impact of

larger wafer size is captured in the reactor scale models, the impact on feature scale models is indirect at most.

In both deposition and etching, the various phenomena can be divided into three categories: a possible redistribution of the species from the gas phase to the surface of the wafer (and into the feature), the transport of these species at the surface, and the surface reaction and subsequent evolution of the interface. It will be shown in this chapter that the transport of the reactive species from the gas phase to the feature and subsequent redistribution is similar for both etch and deposition, and that there are common considerations for both plasma based and low pressure CVD systems. From the point of view of modeling etch and deposition, the biggest fundamental difference is the reaction chemistry at the surface. On the other hand, from a modeling standpoint, the numerical algorithms needed to describe the movement of the interface are the same for both etching and deposition. Each of these steps is described in detail, and the current status of modeling in each area established. In particular, the linking of feature scale models to reactor scale models will be described, in order to attempt to create the utopian scenario where the process engineer can change reactor settings to obtain desirable feature profile changes.

After developing this partially common framework to describe various fundamental etch and deposition mechanisms, specific examples from IC fabrication will be provided. In particular, the deposition processes termed LPCVD, APCVD, and PECVD are discussed. The etch examples include plasma etching, reactive ion etching, and sputter etching. Suggestions are included on capturing specific physics for a particular process by a careful combination of experiments and simulations, and information on available simulators is provided.

## 2.0 COMPONENTS OF ETCH AND DEPOSITION MODELING

In this section, the common basis for what is collectively termed topography simulators, will be developed in greater detail. Let us examine the components that make up a successful topography simulator.

Figure 1 is a flow chart describing the author's strategy for developing and calibrating such a model. Note that this scheme, and the following discussion, assumes a plasma reactor, since that is the more general case of an etch or deposition system. The input to a predictive feature scale

simulator should ideally be obtained from a reactor scale simulator. In a general case, this would include the spatial and temporal fluxes of all the atomic, molecular, and ionic species that are incident upon the wafer. The sheath model (specific, as mentioned, to a plasma system) may be contained within either the reactor scale or the feature scale simulator, but the central idea remains to accurately relate reactor conditions (pressure, power, etc.) to the wafer scale conditions. Once the reactants reach the wafer, they might be transported into features and along the surface. Very often, identifying the nature and mechanism of this transport is the most difficult task, and many researchers have successfully done it with the help of test structures. Beyond this point, the surface reactions that govern either etching or deposition must be identified and quantified. Finally, the model must be calibrated with specific process data, to ensure predictability.

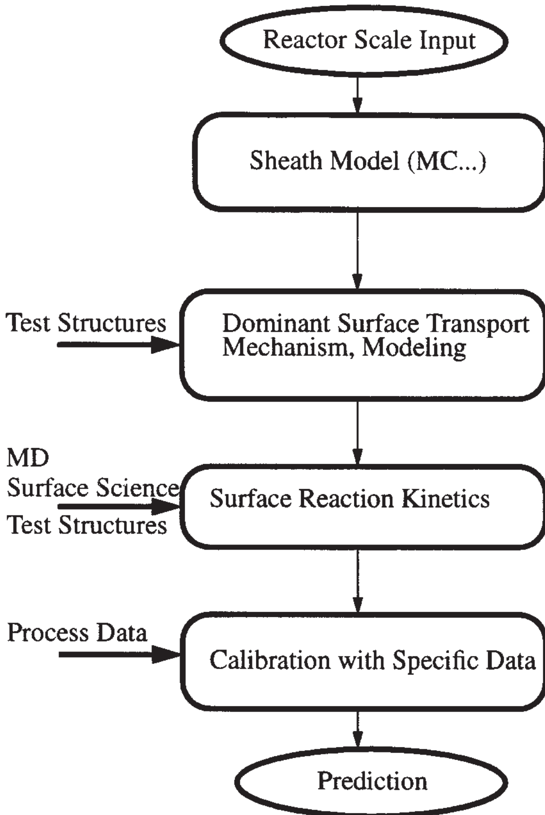
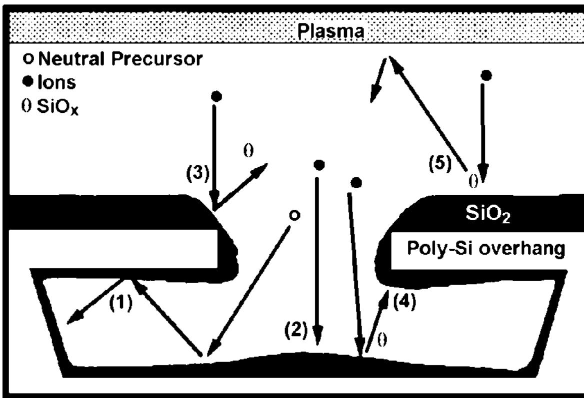



**Figure 1.** Strategy for developing and calibrating feature scale models.

We begin by noting that the pressure in typical plasma systems is of the order of a 100 mTorr. At these low pressures, free molecular flow will exist within features whose characteristic dimension is of the order of a few microns. In other words, particles travel in straight lines as a result of the fact that particle-wall collisions greatly outnumber particle-particle collisions. The particles created in the plasma include ions and radicals (or reaction precursors). These particles can interact with the wafer surface in many different ways, and the type of interaction, by and large, determines the final film profile. Some of these myriad mechanisms are shown in Fig. 2.




**(1) CVD component**
**(2) Ion driven processes**
**(3) Sputtering with angle-dependent sputter yield**
**(4) Redeposition**
**(5) Backscattered deposition**

**Additional Calibrations**
- **Ion angular spread**
- **Surface migration**
- **Surface material dependent processes**

**Figure 2.** Possible mechanisms for transport of species at the feature level.

After the reaction precursor has undergone surface transport, it reacts or is physically deposited at some point on the surface. If a reaction occurs, one must determine the nature of this reaction, in order to model it, and follow the motion of the product species, in order to track the surface profile. There have been a number of studies to determine the kinetics of these surface reaction, but our knowledge in this area is still relatively poor.

Most surface kinetic studies in silicon etching, for example, have employed well-characterized, high vacuum systems. The studies that have been conducted under actual plasma conditions, have typically involved the etching of flat films, which is different from the etching of actual surface features like trenches and holes. Due to geometric shadowing, the fluxes of the relevant chemical species inside the submicron features vary with position, and the etching in different parts of the feature may be controlled by the fluxes of different chemical species, either ions or neutrals. Moreover, and perhaps less importantly, if one were to model every reaction that occurs on the surface, the modeling problem would be limited by computation time, as well as by imperfect knowledge of reaction kinetics.

Just as plasma modelers have found it instructive to consider simplified gas phase chemistry to study surface kinetics, efforts directed at simulating and understanding the evolution of topography benefit similarly from simplifying the surface kinetics involved.[1] This is especially relevant when the main focus is on distinguishing between two different mechanisms responsible for the transport of precursors inside these features. Therefore, we suggest making the kinetic assumption that the etch or deposition rate is a simple function of the number or energy of the reaction precursors (preferably a single one) that react at any position along the profile.[2]–[5]

## 3.0 ETCH MODELING

The process of dry etching involves exposing a substrate (covered by a patterned mask) to the chemical species generated in a plasma, and thus removing (or etching) material away from the exposed surface by chemical or physical means. The large variety of structures and materials involved in this technology imposes many different etching requirements, and these requirements differ widely for the various etch steps used in the production of a single device. Reactive ion etching (RIE) is a term used to describe a type of plasma etching process where the energy of ion bombardment significantly affects the etch profile obtained. The increasingly important characteristic of etching processes is the so called directionality of the etch, which refers to etch rates which are much larger in one direction than in any other. In many plasma etching systems, however, the lateral etch rate or rate of undercut is significant. A typical example is

the etching of silicon with sulfur hexafluoride using an oxide mask, where, inevitably significant undercut is found immediately below the mask, and anisotropy is lost. Figure 3 shows one such etching profile of a two dimensional trench in the etching of silicon. This large lateral undercut renders the etching system inappropriate for many applications, even though the etch rate is desirably high. In order to control the etch profiles in such systems, it is important to understand the mechanism by which etching proceeds and, thus, undercut develops. In this section, the example of silicon RIE, in an $SF_6$ plasma will be considered to develop a general framework for the feature scale modeling of etch processes, and this framework will be extended in the following section, to comprehend other etch systems.

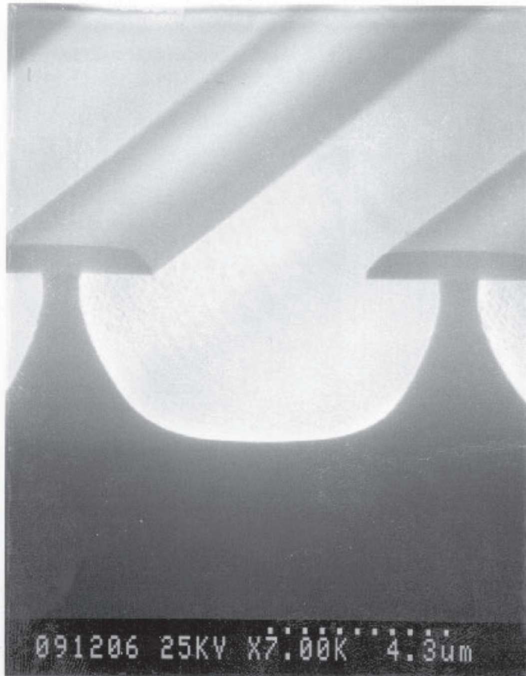



**Figure 3.** SEM of a trench etched in silicon in a $SF_6$ plasma, showing large undercut beneath the mask.

### 3.1 Ion Transport in Sheath

Before we can simulate profile evolution, we need to know the angular statistics of the ions in the sheath. As mentioned in Sec. 1.0, we calculate these distributions by a Monte Carlo simulation program developed by Rey and McVittie.[6][7] This simulation tracks both momentum transfer and charge transfer collisions in the plasma sheath. The sheath thickness, pressure, and the DC bias in the reactor are measured. We assume $SF_5^+$ and $SF_3^+$ to be the important ions in the plasma. Without discussing the details of the Monte Carlo technique, we simply present an example of one of the ion angular distributions that were obtained for the experiment in Fig. 4. For the details, reference should be made to the appropriate publication.[6]

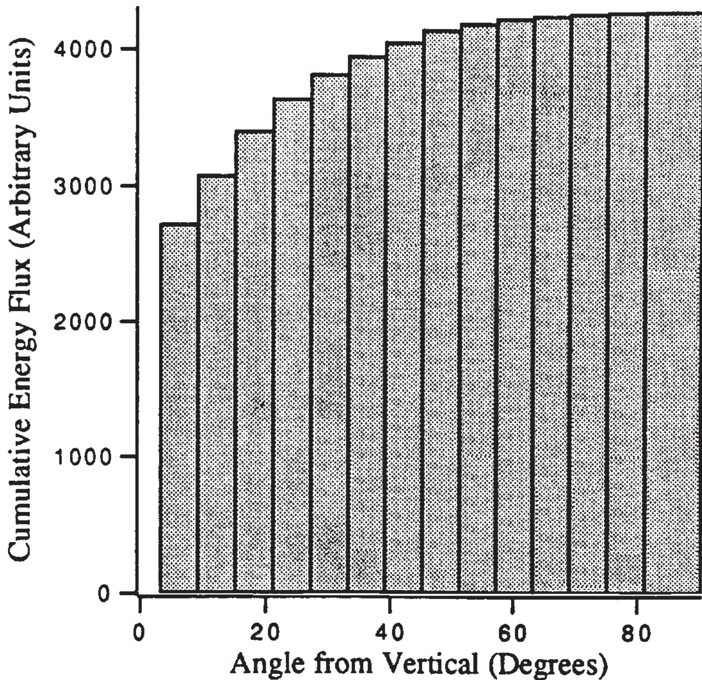



**Figure 4.** A cumulative ion-energy angular distribution obtained with a Monte Carlo technique.

## 3.2 Selection of Surface Transport Mechanism

In RIE, the electrode holding the substrate develops a time-averaged negative DC bias, and this causes the positive ions to be accelerated toward the substrate with high energies. Coburn and Winters have shown that RIE proceeds due to a synergism between ions and neutral etch precursors,[2][9] and various mechanisms for this synergism have been suggested. These include increased uptake of fluorine by a silicon surface under ion-bombardment through lattice damage,[10][11] acceleration of the product formation step,[3] and enhancement of the product desorption step via sputtering.[12] Under certain conditions, however, the etch rate due purely to the radicals is significant. This is demonstrated in etch profiles exhibiting large etch rates in regions (such as those immediately beneath the mask) that are completely shadowed from ion bombardment. Previous authors who considered this purely chemical etch rate[13][14] have modeled it to be a constant etch rate superimposed on the ion-assisted etch rate. In order for this to truly model the etching process, a transport mechanism must exist by which reacting species might be transported to all points on an evolving interface. One such mechanism is diffuse re-emission.[15]–[20] Since the radicals are incident on the substrate with thermal velocities, they may be re-emitted from the surface before they react. Therefore, the probability of their sticking and reacting at the surface on incidence should be considered. This can be described through specification of a reactive sticking coefficient, or reaction probability, $Sc$. If this sticking coefficient is less than unity, the radicals can be re-emitted from the interface, thus, establishing a mechanism for their transport to portions of the interface that are "shadowed" from the plasma itself. The transport of radicals to the evolving interface may also occur by diffusion of radicals along the surface.[21] Sato and co-workers postulated that surface diffusion explained their experimental results on etched depth reduction in silicon RIE.[22] This confusion about the mechanism governing etching in fluorine based plasmas was resolved to a large extent in favor of surface re-emission, with the help of etch experiments in specially fabricated test structures, shown in Fig. 5. It was found that the etch rate deep in the cavity of the test structures was dependent on the size of the opening at the top, an observation that is only supported by surface re-emission, since the precursor diffusion length on the surface is independent of the opening size.

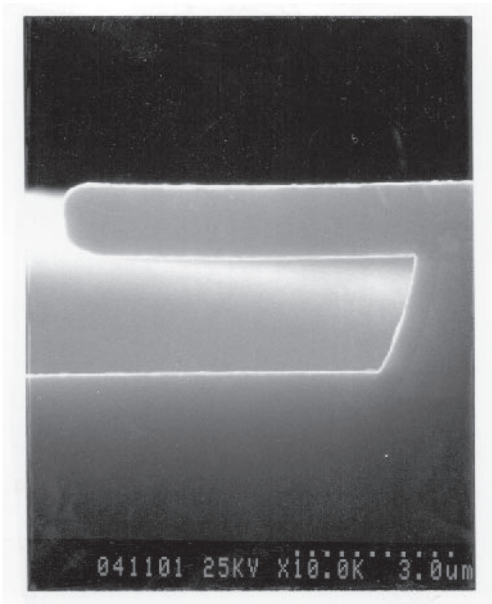



**Figure 5.** An SEM of a test structure, consisting of overhanging ledges as well as a blanket covering of polysilicon.

## 3.3 Surface Reaction Kinetics

Plumb and Ryan[23] have published a detailed set of elementary reactions for the etching of silicon in $CF_4/O_2$ plasmas. Other workers[24]–[26] have used a reduced set of such reactions to model the gas phase concentration of the important species in order to explain, inter alia, intra-wafer as well as inter-wafer non-uniformities. To better understand the mechanisms by which etching proceeds, it is essential to relate such gas phase chemistry to surface kinetics. Several workers have investigated the dominant kinetic processes that occur on the surface during the etching of silicon in fluorine-containing chemistries. Basic studies in non-plasma environments have often involved the reaction between a clean silicon

surface and xenon difluoride,[2]–[5] and for a range of conditions, a linear dependence of etch rate on fluorine or fluorine-like radicals has been observed. Flamm and co-workers studied the reaction of fluorine atoms with silicon, and reported the formation of $SiF_2$ to be the rate limiting step.[27] Winters and Plumb[28] have presented evidence to show that ion-enhanced etching of silicon may proceed mainly though chemical sputtering and an increased spontaneous etch rate. McFeely and coworkers[29] have shown that the etching reaction does not take place by the continuous removal of the outermost layer of silicon, but by the formation of a reaction layer containing $SiF_x$ intermediates. Oehrlein[30] has proposed that this reaction layer is made thicker by ion-bombardment, and that ion-induced mixing and damage generation may be important mechanisms in ion-enhanced etching reactions. Schwartz and Schaible[31] suggested that the formation of a polymer on the sidewall of a feature may inhibit the lateral etch rate, and this idea has since been confirmed by many experimental studies.[32] Sawin, et al.,[33] quantified the surface film formation effects in fluorocarbon plasma etching of polysilicon, and showed that the competitive interaction between $CF_2$ and F radicals on silicon surfaces suppresses the ion-enhanced etching yield. The effect of adding oxygen to a $CF_4$ plasma has also been examined.[34]–[38] It has been shown that the addition of small amounts of oxygen results in an increase in the fluorine density and the silicon etch rate, and a corresponding decrease of the fluorocarbon content of the reaction layer. Tachi, et al.,[39] and Ding, et al.,[40] have suggested that there exist two regimes of atomic fluorine flux (relative to ion energy flux) in fluorine based RIE of silicon, one in which neutral flux governs etch rate, and the other where the energy of ion-bombardment is more important.

## 3.4 Simplifying Assumptions

The preceding discussion illustrates the need for making appropriate assumptions to condense the details of the surface kinetics into a tractable etch rate equation. We have made the kinetic assumption that the etch rate is proportional to the number of etching precursors that react at any position along the profile.[2]–[5] This implies that the etch rate is proportional to the flux of direct and re-emitted precursors for the case of surface re-emission, and to the surface concentration of mobile precursors for the case of surface diffusion.

## 3.5 Modeling of Surface Re-emission

With the above assumptions, one can model the evolution of the etch profile. As discussed previously, RIE proceeds due to a synergism between the energetic ions and the neutral etch precursors, or radicals. In order to simulate the profile evolution of features like trenches and holes, therefore, the fluxes of reactant species at all points along the surface of these features must be determined. In the absence of surface transport mechanisms, such as surface re-emission and surface diffusion, the flux of reactants in a feature, received from the plasma, is completely determined by the three-dimensional geometry of the feature. The presence of surface transport redistributes this "direct" flux, and the extent to which this redistribution takes place depends upon the interactions of the reactants with the substrate. The calculation of reactant fluxes under various conditions of surface transport, and the development of techniques to simulate the resulting etch profile evolution, are described in this section.

As mentioned previously, in reactive ion etching the radicals are incident upon the substrate with thermal velocities, and if they do not react immediately, there is a possibility of their being re-emitted. In such cases there is a redistribution of the radicals on the surface, and portions of the interface that are shadowed from the plasma by the mask or the sidewalls, receive a significant re-emitted flux from the remaining profile. To simulate profile evolution with re-emission, we begin by defining the velocity of the interface:

Eq. (1) $$\mathbf{v} = k_i(\mathbf{E} \cdot \mathbf{n})\mathbf{n} + k_r ScF(\mathbf{x})\mathbf{n}$$

where $F(\mathbf{x})$ is the total radical flux at the position $\mathbf{x}$.

Thus, we need to determine $F(\mathbf{x})$ at each position along the interface. To this end, we recall that we have assumed that the Knudsen number (the ratio of the mean free path of any particle to the characteristic length of a feature) is large enough that collisions between all particles within the etching feature can be neglected. In this parameter regime particles travel in straight lines, both during their initial incidence and after re-emission. Under these conditions the re-emitted flux can be calculated by distributing sources of unknown strength along the interface. These sources represent the re-emission of radicals (with known angular statistics) that fail to stick. Thus, each point on the interface receives flux of radical etchants both from the plasma and from other sources on the interface. Consider two such sources, at $\mathbf{x}$ and $\mathbf{x}'$. Let the total fluxes at

these two locations be F(**x**) and F(**x**´) and let the surface normals be **n** and **n**´ respectively. Define xx´ as the unit vector pointing from **x** to **x**´, and **x**´**x** as the unit vector pointing from **x**´ to **x**. A small area dA acts as a re-emission source from a position **x**´. Note that the flux decreases as the square of the distance away from the source, if we assume isotropic re-emission, which will be defined presently.[41] If we integrate the re-emitted flux received at **x** from all other sources, and add to it the flux received directly from the plasma, then we arrive at the integral equation

Eq. (2)
$$F(\mathbf{x}) = \mathbf{j} \bullet \mathbf{n} + (1 - Sc) \int_{\partial D} \frac{(\mathbf{x x}' \bullet \mathbf{n})(\mathbf{x}' \mathbf{x} \bullet \mathbf{n}) F(\mathbf{x}') dA}{\pi |\mathbf{x} - \mathbf{x}'|^2}$$

The integral in Eq. (2) is over all positions with a line of site access to **x**. If we look at the evolving interface in discrete increments, then the discrete version of Eq. (2) can be solved to arrive at the source strength at each discrete element. Knowing the total flux at each element, the interface can be advanced according to the velocity defined by Eq. (1).

A re-emission distribution has been assumed in this formulation, and this was first studied by Knudsen.[41] This function depends on the specific nature of the interaction between the wall and the colliding particles. There is said to be complete accommodation if the particles re-emitted from each element of the interface have the same distribution (regardless of the magnitude and direction of their velocity before the impact) as that leaving a small aperture in a vessel containing gas at a temperature equal to that of the interface.[42] In other words, with complete accommodation, the gas scattered by the walls reaches thermal equilibrium with it. This particular re-emission pattern is also called diffuse re-emission, and the flux over a unit hemisphere centered at **x**´ is normalized to unity.

## 3.6 Modeling of Surface Diffusion

As mentioned in the Sec 1.0, adsorbates on surfaces may exhibit high mobility below the desorption temperature. Thus, a radical which strikes the etching substrate but does not react with it, may diffuse along the interface. If this diffusion length is significant, radicals will be redistributed on the surface, and this will affect the etch rate at various positions on the interface. In this section, we describe the effect of surface diffusion of radicals on the evolution of etch profiles. This analysis assumes that there is no re-emission from the surface, and that the etch rate is first order in the

concentration of the diffusing radicals.[43] We also assume that the total flux of the radicals at any position along the profile reaches a quasi-steady state in a time much smaller than that required for the interface to etch or evolve significantly.

By performing a mass balance on the diffusing radicals, we can write the following equation describing the concentration of radicals, $c$, along a two-dimensional etching surface:

Eq. (3) $$-D\nabla_s^2 c + kc = Scj(\mathbf{x})$$

In Eq. (3), $D$ is the diffusivity of radicals along the surface, $k$ is the *reaction frequency*, and $\nabla_s$ is the *surface Laplacian*. The source of radicals received from the plasma is given by $j(\mathbf{x})$. Let $s$ be a coordinate running along the etch profile. We can make all lengths dimensionless with the width of the feature, $W$, time dimensionless with $1/k$, and the flux of radicals, $j(s)$, dimensionless with the flux on an unshadowed surface, $J$. The dimensionless concentration is then given by $ck/J$. The dimensionless equation describing simultaneous surface diffusion and reaction, in a trench, now becomes

Eq. (4) $$\frac{d^2c}{ds^2} - Da^2 c = -Da^2 j(s)$$

$Da$ is the Damkohler number, and is given by $W/\sqrt{D/k}$.

Physically, $Da$ represents the ratio of the characteristic feature length to the characteristic diffusion length. The latter is defined as the distance a typical diffusing radical travels before it reacts with the substrate. $Da$ may also be understood as the ratio of a characteristic diffusion time to reaction time.

Equation (4) can be solved by imposing the appropriate boundary conditions. These conditions result simply from the fact that, at points on the mask far from the etching feature, there is no "shadowing" from other parts of the profile, and the flux of radicals approaches $J$. Once the concentration of radicals along the profile is known, the interface can be advanced according to a rate equation similar to Eq. (1). Up to this point, we have described and modeled two mechanisms for the transport of radicals along the evolving interface. The numerical implementation of our analysis, and the resulting profile evolutions are presented in the next section.

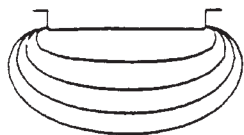
## 3.7 Numerical Methods

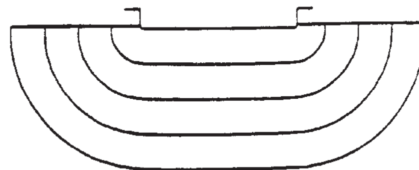
**Surface Re-Emission.** We demonstrated in Sec. 3.5 that this problem involves the solution of a set of line integral equations. This, in turn, requires that at each time step, we discretize the line and invert a matrix to solve for the source strength at each discretized element. We use the Gauss Jordan method with full pivoting to invert the matrix when it is small (approximately 30 to 40 sources), and the Gauss Seidel iterative method when the matrix is larger. The latter technique is suitable because the matrix is diagonally dominant. The LU decomposition method, with an iterative improvement, is used as a check to verify the accuracy of the solution. Once the source strength (or alternatively, the total radical flux) is obtained at each point, the surface is advanced along the surface normal using a simple Euler difference formula.[44] The surface normal itself is approximated by the angle bisector of the two segments connecting a given element to the two adjacent elements.

In the implementation of the intermediate sticking coefficient, it is important to control the number of elements describing the interface while the time stepping is carried out. For a fixed number of elements, the resolution of the profile becomes poorer as the etching time increases. Moreover, when the substrate directly beneath the mask is etched away by the action of re-emitted radicals, the exposed underside of the mask also acts as a source of re-emitted radicals. Therefore, our program adds elements (by linear interpolation) to the interface when and where their density becomes low, or in other words, our mesh is "adaptive." Typically, the maximum dimensionless distance allowed between elements is about 0.1. This value is determined by a testing convergence upon grid refinement. The results of this simulation are presented in a series of profile evolutions shown in Fig. 6.

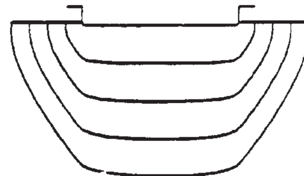
There are two dimensionless parameters, $N$ and $Sc$. The effect of varying sticking coefficient is demonstrated for the case of etching by radicals alone, and the effect of differing the ratio of the radical etching component to the ion-assisted component is also shown.

**Surface Diffusion.** Equation (4), when written for the discretized surface elements along the etching profile, leads to a system of equations that is tridiagonal. This can be solved by using standard techniques,[45] and the result of this implementation gives the concentration of the diffusing radicals as a function of position along the profile. Figure 7 shows the effect of diffusion on the quasi-steady state flux of radicals at various positions in a trench of unity aspect ratio.





SC = 1.0 SC = 0.5 SC = 0.0



N = 0.0 N = 0.5 N = 1.0

**Figure 6.** A series of trench profile evolutions given by the implementation of the intermediate sticking coefficient formulation. Series *(a)* shows the effect of varying the sticking coefficient for purely radical etching, and series *(b)* shows the effect of varying N, the ratio of radical to ion-assisted etch rate.

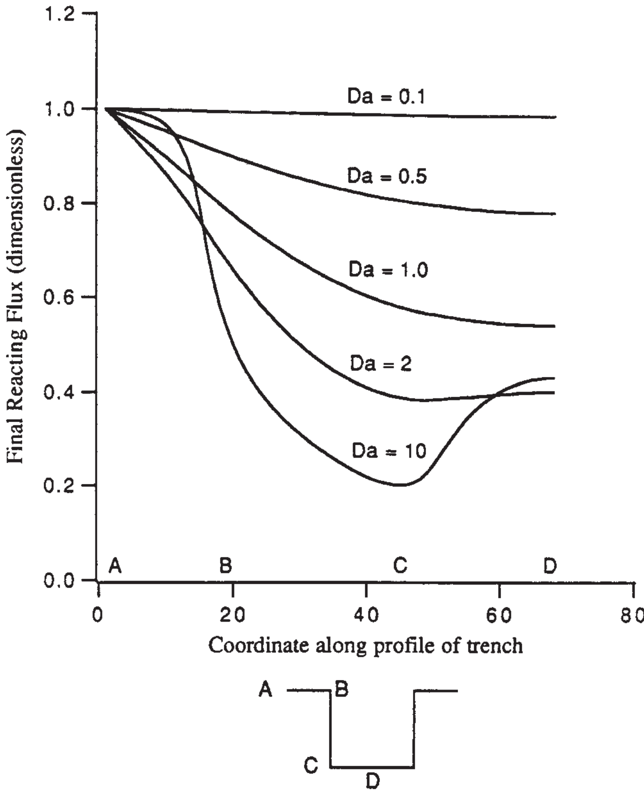



**Figure 7.** The effect of diffusion on the quasi-steady state flux of radicals at various positions in a trench of unity aspect ratio. The coordinate running along the profile is plotted on the *x* axis.

When the Damkohler number is large (or, in other words, diffusion is slow compared to reaction), the steady state value of the flux is equal to the flux received directly from the plasma. As $Da$ is decreased, the increased diffusion length has the effect of smoothing any concentration gradients and, for $Da = 0$, the concentration of radicals is uniform across the profile and is equal to $J/k$. Figure 8 shows the profile evolution of a trench simulated for $Da = 1$.

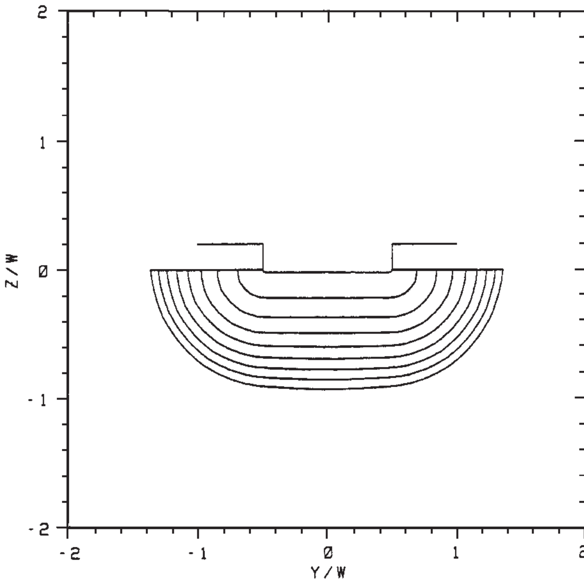



**Figure 8.** Profile evolution for a trench simulated by the surface diffusion mechanism for $Da = 1$.

In this simulation, only the purely radical etching component is included. Note that the etch rate decreases along the entire profile with time. This is because the specification of a Damkohler number also specifies a characteristic diffusion length, and this limits the mobility of the radicals. Therefore, as the trench gets deeper, fewer radicals can diffuse to the bottom of the trench from other parts of the interface.

## 4.0 ETCH EXAMPLES

In the previous section, we have described the framework for simulating profile evolution in plasma etching processing. In this section, we explain how such a framework can be used to simulate actual etch processes.

Before we do that, it is useful to recollect the main reasons for the use of plasmas for etching semiconductor layers.

i. *Etch Directionality.* The etching is frequently required to proceed in the vertical direction.

ii. *Etch Selectivity.* The etching occurs in the presence of a mask. The selectivity often refers to the preferential etching of the substrate over the mask. In other cases, selectivity might refer to the reduction of etch rate on a material other than the one being etched. This causes the etch to stop when the layer is completely etched away.

The first example will be the continuation of the $SF_6$ process that we have described earlier. As explained earlier, etching of silicon in pure $SF_6$ produces an undesirable amount of lateral undercut beneath the mask, rendering the process virtually useless for most applications. Nevertheless, it is instructive to simulate this system to understand the governing mechanisms. An experimental time evolution of the etch profile of a trench was obtained for 0.5, 1.0, and 1.5 minutes of etching time. The etch was carried out in a Drytek-100 reactive ion etcher. The masking layer was made up of 500 nm of patterned low temperature oxide. The pressure in the reactor was 100 mTorr, the power was 250 Watts, the DC bias varied between 100 and 110 volts, and the flow rate of $SF_6$ was 100 sccm.

The etch profile at any given time, here the one at 1.5 minutes, is digitized as shown in Fig. 9. We then attempt to simulate this profile with the surface re-emission model. The parameters involved, as mentioned previously, are the sticking coefficient of the etch precursor *(Sc)*, and the ratio of the purely radical to the ion-assisted etch rate *(N)*. As shown in Fig. 9, a good match to the experimental profile is obtained by a value of *N* equal to 2 and *Sc* equal to 0.01, to within 5 % accuracy. This fit itself is of course not remarkable, but as Fig. 10 shows, the same values of *N* and *Sc* can be shown to simulate the entire profile evolution for this feature as well as other features, including that of a cylindrical hole. The latter is especially interesting since the calculation of geometric shadowing for a hole is very different from that of a trench, from the choice of coordinate system to the nature of symmetry in the third spatial dimension.

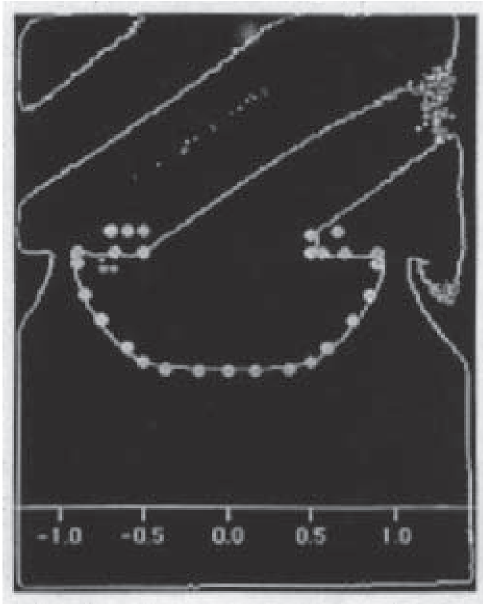



**Figure 9.** The digitized profile of the trench etched for 1.5 minutes. The simulation is shown superposed on the digitized image.

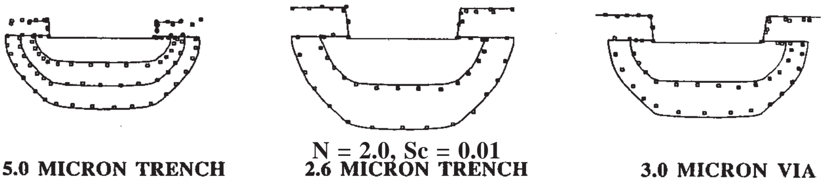



**Figure 10.** Comparison of experimental etch profiles (shown by symbols) and simulated profiles for two different trenches and a cylindrical hole. The time evolution is shown for each feature.

Another example of fluorine based etching is the etching of polysilicon in $CF_4/O_2$ chemistry. This time we consider the etching of test structures that are covered with a polysilicon layer deposited uniformly by an LPCVD process. Different structures (similar to Fig. 5) are etched for 4 minutes in a $CF_4/O_2$ plasma, in a Drytek 100 parallel plate etcher at 150 mTorr, 350 Watts, 100 sccm $CF_4$, and 10 sccm $O_2$. The thickness of the polysilicon layer remaining inside the "cavity" is measured, leading to a determination of the amount of etch at that location, and this is shown in Table 1. The same phenomenon is simulated independently assuming surface re-emission and surface diffusion, one at a time, to be the governing transport mechanism. The results, also included in Table 1, show that surface re-emission explains the experimental observation much better than surface diffusion.

**Table 1.** Simulation by Surface Re-emission and Surface Diffusion

Surface Re-Emission

| Source | Opening size, μm | Side layer etched, μm |
|---|---|---|
| Experiment | 7.25 | 0.24 |
| Simulation (Sc = 0.04) | 7.25 | 0.20 |
| Experiment | 0.42 | 0.09 |
| Simulation (Sc = 0.04) | 0.42 | 0.10 |

Surface Diffusion

| Source | Opening size, μm | Side layer etched, μm |
|---|---|---|
| Experiment | 7.25 | 0.24 |
| Simulation (Da = 4.35) | 7.25 | 0.007 |
| Experiment | 0.42 | 0.09 |
| Simulation (Da = 0.252) | 0.42 | 0.002 |

In many etch chemistries, there is in fact competition between the processes of etching and deposition, with the carbon containing radicals often acting as deposition precursors. The ratio of the etch to deposition flux is constant on a flat surface, but varies along a topographic profile, for purely geometric reasons. This variation is often responsible for the directionality of the etch, by increasing the lateral deposition rate, and the vertical etch rate. Figure 11 is an SEM showing this phenomenon, in an etch profile obtained after 10 minutes of etching in 70 sccm $SF_6$, 70 sccm $C_2ClF_5$, 106 mTorr pressure, and 304 volts DC bias. One clearly notices the layer of sidewall polymer that is so strong mechanically and chemically that it is left intact even as the photoresist is etched away. If such a process is simulated accurately, one obtains the ability to predict the effect of process changes on topographic features. An example of this is the patterning of a feature in oxide with a resist mask, in a $CHF_3/O_2$ plasma. The effect of adding oxygen is to consume the carbon containing radicals in the gas phase, thus, reducing the deposition rate at all points in general, and on the sidewall in particular. This effect results in the possibility of modulation of the sidewall angle, by modulating the amount of oxygen, as shown in Fig. 12.

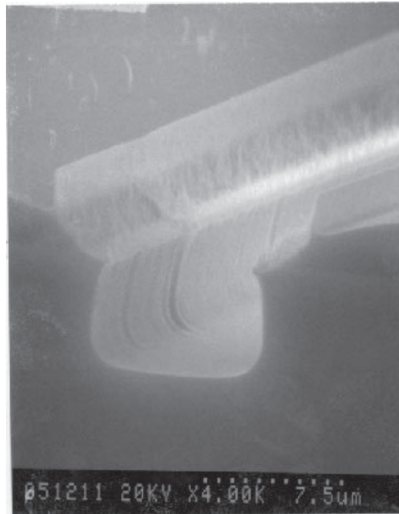



**Figure 11.** SEM of an etch profile showing a polymeric residue on the sidewall.

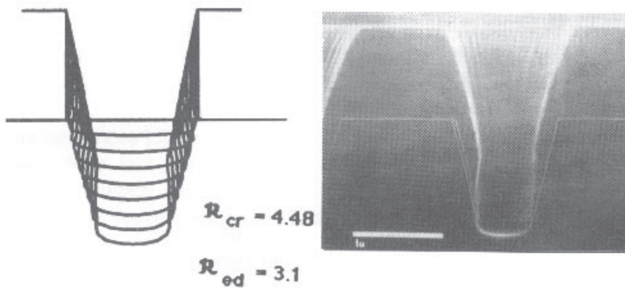



**Figure 12.** The effect of polymer deposition on sidewall slope. The amount of polymer deposition can be reduced by adding oxygen.[18] *(Reprinted with permission J. P. McVittie.)*

The final example in this section is that of etching of organic materials. This process is becoming increasingly important as optical lithography is being pushed beyond its originally perceived limit, while other lithography technologies are struggling for manufacturing viability. Jurgensen and coworkers[46] have studied the etching characteristics of a silyl novolak polymer and an organic novolak polymer in an oxygen plasma. They found that the effect of a number of different process conditions was manifested in a single effective variable: the energy flux deposition at any given point along the profile. The energy flux deposition on a flat surface can be calculated by a number of different theories,[46] the simplest of which is the Child-Langmuir formula:

Eq. (5)
$$J_{CL} = \frac{4\triangle^{3/2}\varepsilon_o}{9S^2}\left(\frac{2}{em_i}\right)^{1/2}$$

where $\triangle$ is the voltage drop across the sheath, $S$ is the sheath thickness, $\varepsilon_o$ is the vacuum permittivity, $e$ is the electron charge, $m_i$ is the mass of the ion. This equation assumes a collisionless sheath, neglects the contribution of electrons to the space charge, and assumes a zero velocity for the ions at the plasma-sheath boundary where the electric field is assumed to be zero. Jurgensen, et al., used corrections to this equation to conclude that the etch

rate of organic materials is linearly proportional to the ion energy flux at any point. One can then use this simple kinetic rule to simulate profile evolution for the etching of photoresist, as shown in Fig. 13.

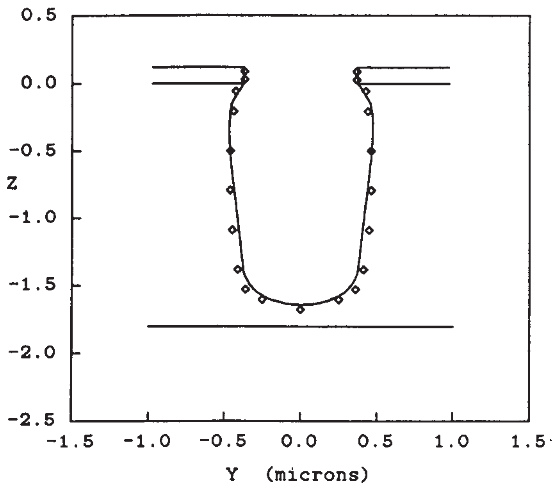



**Figure 13.** Comparison of theoretically predicted etch profile with experimental measurements from SEM for a 2.4 aspect ratio trench.[1] *(Reprinted with permission.)*

## 5.0 DEPOSITION MODELING

The modeling of deposition processes at the feature scale level has much in common with the modeling of etch processes, as was mentioned in Sec. 2. Thus, the description of etch modeling in Sec. 4 will suffice for deposition modeling as well, and we shall simply point out the differences here.

In the case of deposition under low pressure conditions, as with etch processes, one must first establish whether molecular flow exists, for which the present discussion holds. If the mean free path is of the deposition precursors is of the order of the feature size, or less, one must resort to continuum modeling techniques. If, on the other hand, molecular flow exists, the flux of the deposition precursors inside a feature is determined by purely geometric calculations, as described previously. The surface transport of the precursors can be similarly calculated, using Eqs.

(2) and (4). From a modeling viewpoint, the main differences arise in considerations of surface advancement, which now occurs in the opposite direction. This portion of the simulation is simpler for deposition because there is only one material boundary to consider, that of the material being deposited. On the other hand, the difficulty in surface advancement for deposition lies in the fact that deposition is numerically an unstable process, while etch is a stable process (when no surface transport occurs). This is because the "hills' of topography receive higher flux than the "valleys," leading to a greater difference in the growth rate of the two, as shown in Fig. 14. The same phenomenon occurs numerically, necessitating steps to prevent numerical instability.

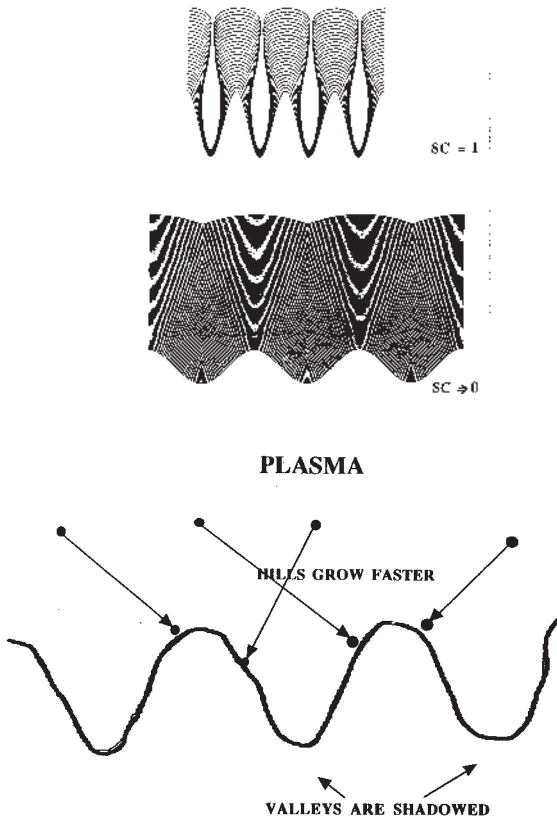



**Figure 14.** Simulation of the effect of shadowing leading to evolution of "hills" and "valleys" during low pressure deposition.

An emerging field in the simulation of deposition processes is the prediction of thin film microstructure.[47][48] It is clearly important to understand this microstructure, since it has bearing on the electrical, as well as thermo-mechanical properties of the film. To simulate the microstructure of the film, let us first consider the mechanisms that cause this microstructure to develop. One of the most important stages in film growth is the deposition of the first monolayer. In this time period, the "seeds' of the film are deposited, and the structure, geometry, and spacing of these seeds are determined by flux values, substrate characteristics, surface mobility, and the thermodynamics of the interactions of the deposition precursors with each other and with the surface. As the film continues to grow, given enough surface mobility, the constituent moieties of the film try to reduce their free energy, and one of the ways to do that is by reducing the curvature of the film surface. Finally, the instability determined by geometry, mentioned above, is another mechanism affecting film microstructure. We shall briefly describe this last effect, since it is closely tied to the rest of the discussion in this chapter.

Let us consider simple two dimensional topographic variation, given by a sinusoidal wave $z = A\cos(ay)$, where $A$ is the amplitude of the roughness and $\alpha$ is the wavenumber. We now place this surface in a system which demands that the rate of growth of any point on the surface is given by $v = F\overrightarrow{n}$, i.e., the velocity is proportional to the flux of deposition precursors received at that point, and is in the direction of the local surface normal. One can solve the evolution of this surface in a fashion similar to that described in Sec. 4, and this can be done for a number of different wavenumbers. For the case when there is no surface transport, or the sticking coefficient for the re-emission process is unity, the "hills" grow, the "valleys" are shadowed, and the solution at long time is columns growing vertically, as shown in Fig. 15. For the limiting case of the sticking coefficient approaching zero, the flux at all points along the profile is uniform, and the amplitude of the evolving sinusoidal surface starts decaying at a time determined by its wavenumber. This is shown in Fig. 16. These results show how microstructure might be affected by the extent of surface transport. This effect is shown more starkly by considering a statistically rough surface as the initial substrate, and then letting it grow under deposition characterized by different values of sticking coefficients. The results, shown in Fig. 17, demonstrate that redistribution of flux caused by surface transport cause "smoother," void-free films to be deposited, whereas, in the absence of such mechanisms, a more columnar microstructure might result. Simulations of microstructure are only recently beginning to be characterized, and in general are not yet predictive.

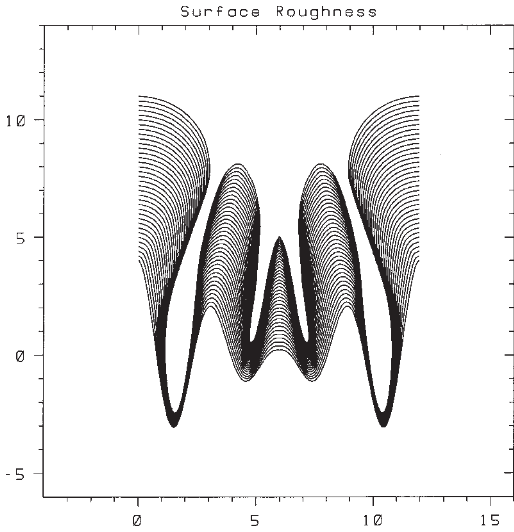



**Figure 15.** Simulation of the evolution of "model" surface roughness grows into columns at long times for the case of zero surface re-emission, or sticking coefficient equal to unity.

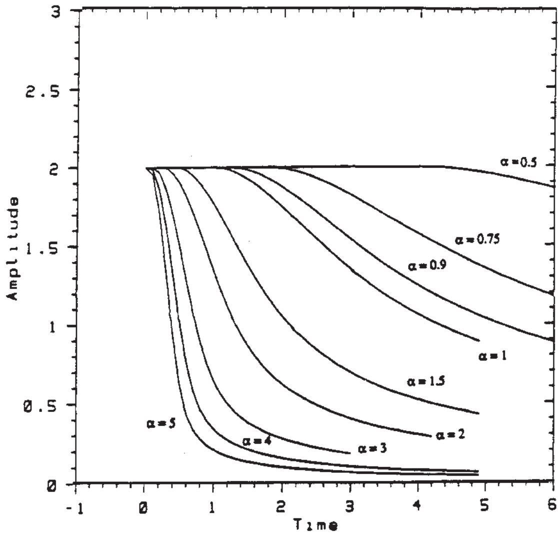
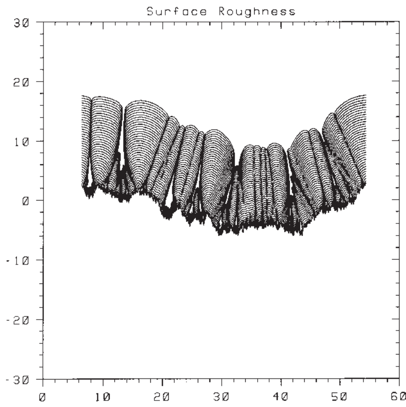
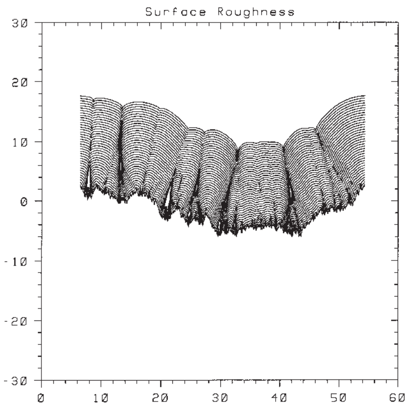


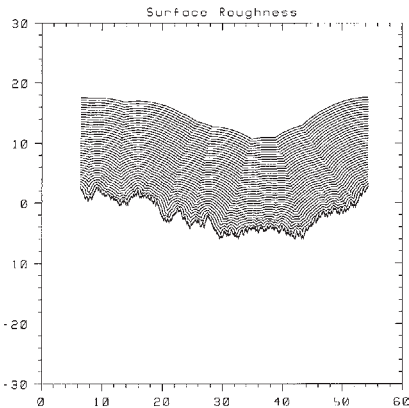

**Figure 16.** The dependence of surface roughness decay time and rate on the wavenumber of the roughness.




**Sc = 1**




**Sc = 0.75**




**Sc = 0**

**Figure 17.** Deposition on statistically rough surfaces modeled with different sticking coefficients.

## 6.0 DEPOSITION EXAMPLES

The first example in this section concerns the deposition of silicon dioxide from different source gases. It has been observed that the deposition of oxide from a silane source results in profiles with poor step coverage. Figure 18 shows SEMs of such a process occurring in trenches of aspect ratio 0.7 and 1.2, with the source gas being $SiH_4$ and $PH_3$, at a temperature of 380°C and a pressure of 250 mTorr.[49] This process can be simulated with the surface re-emission model, assuming a sticking coefficient of 0.35, as shown in Fig. 18. When oxide is deposited from a DES source, the conformality is better, as can be seen in the SEM in Fig. 19. Here deeper trenches, with aspect ratios 2.1 and 4.8, are filled with oxide using DES/oxygen in a ratio of 2:1, at a pressure of 950 mTorr and a temperature of 380°C. The simulation of this process is shown in Fig. 19, using a sticking coefficient of 0.07. Thus, different chemistries are characterized by different values of the relevant transport parameter, which has to be determined by calibration. Once we determine this value, one can study the effects of geometry on the process capability. Figure 20 shows the values of sticking coefficients that have been successfully used for some deposition processes.[49]

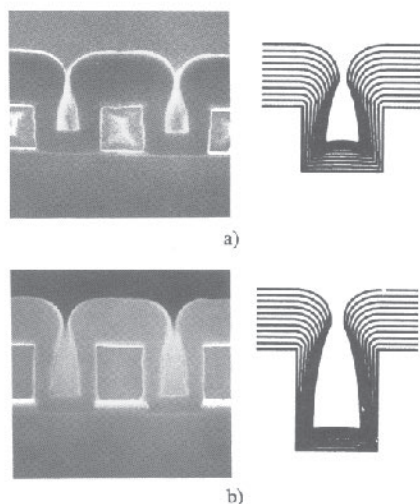



**Figure 18.** Deposition of PSG from a silane source in trenches of different aspect ratios, and simulations assuming a sticking coefficient equal to 0.35.[18] *(Reprinted with permission J. P. McVittie.)*

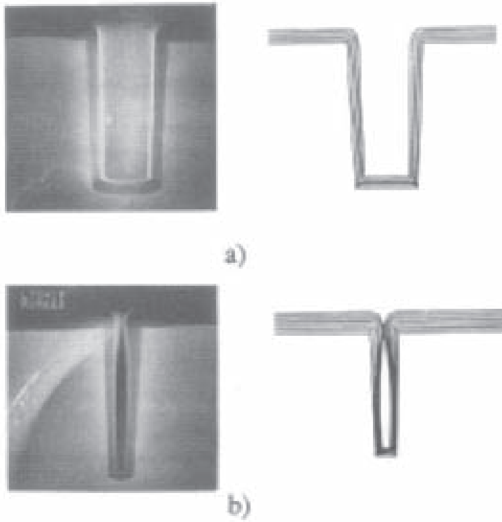



**Figure 19.** Deposition of oxide from a DES gas source in high aspect ratio trenches. The simulation in this case is with a sticking coefficient equal to 0.07.[18] *(Reprinted with permission J. P. McVittie.)*

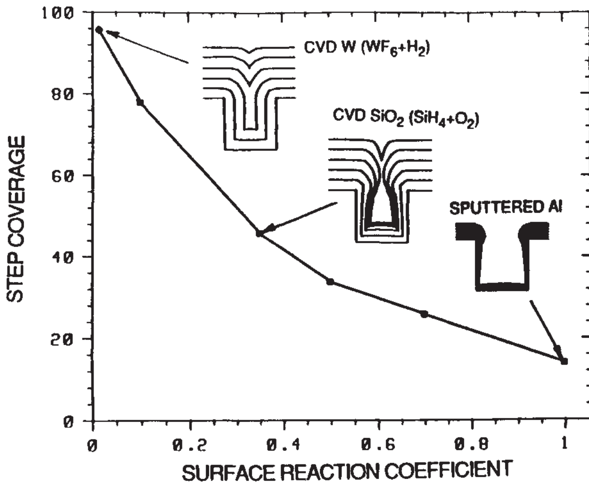
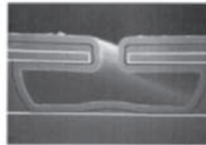



**Figure 20.** The step coverage for a trench of aspect ratio equal to unity, with varying sticking coefficients. Three deposition examples are placed in this context.[18] *(Reprinted with permission J. P. McVittie.)*

Let us now consider another process for the deposition of oxide: Plasma Enhanced Chemical Vapor Deposition (PECVD). In this process, the local deposition rate at any point along the profile is determined not just by the flux of deposition precursors reaching that point (as in the previous CVD example), but also by the energy delivered due to ion bombardment. A typical model for this process assumes that the sticking coefficient for ions is unity (since they do not undergo much reflection or re-emission), and the neutral precursors might be re-emitted. The parameters that must be characterized for predictive simulation are *(i)* the sticking coefficient of the LPCVD (or neutral) component, *(ii)* the ion angular distribution just above the wafer, and *(iii)* the ratio of neutral to ion-enhanced deposition. Figure 21 shows an SEM of a "test structure" exposed to a PECVD process at 9 Torr and 390°C, with TEOS and $O_2$ flowing at 180 sccm and 240 sccm, respectively. A simulation of this process is shown alongside, using a sticking coefficient of 0.07, an ion-angular distribution represented by the analytical expression $f(\theta) = \cos^{10}\theta \sin\theta$, and a neutral to ion-enhanced ratio of 0.55.[50]



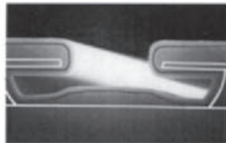


**Figure 21.** SEM and simulation for a PECVD process for the deposition of oxide from TEOS. *(Reprinted with permission J. P. McVittie.)*

The third example of oxide deposition is termed Atmospheric Pressure Chemical Vapor Deposition (APCVD) or Sub-Atmospheric CVD (SACVD). This process is the only one in this chapter where the assumption of free molecular flow at the feature scale does not hold. Due to the higher pressures employed in this process, the model must be based on the continuum transport equation, combined with a description of the surface reaction kinetics. The transport equation for diffusion, in dimensionless form,

Eq. (6) $$\nabla^2 C = 0$$

should be solved with appropriate boundary conditions. In matching simulations with experimental data, it has been found that a typical APCVD process is limited by the rate of reaction at the surface. If this were the predominant phenomenon, the simulation would simply result in equal growth rates at all points along the profile. However, it is observed that concave corners tend to grow at a slightly faster rate compared to convex corners. This might be captured phenomenologically by explicitly altering the reaction rate at a point depending upon the local curvature. Figure 22 shows SEMs and simulations for an APCVD process for deposition of oxide from $O_3$/TEOS.

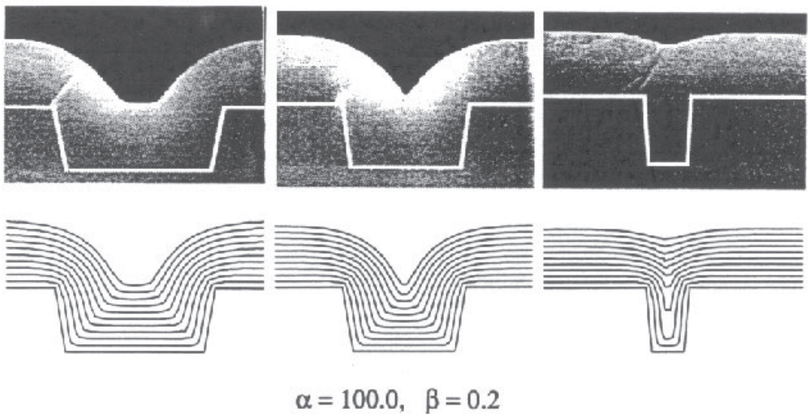



**Figure 22.** SEMs for rounding of film deposited by the atmospheric CVD process, and simulations assuming a 20% enhancement of reactivity at concave corners and 20% reduction at convex corners.[56] *(Reprinted with permission J. P. McVittie.)*

The final example in this section is that of Physical Vapor Deposition (PVD). The relative simplicity of PVD makes it, generally speaking, the most accurately predicted process from the point of view of feature scale simulation. In the model, one species of deposition precursors is tracked, and is assumed to contribute to the growing film at the point where the particles first strike the wafer. This obviates the need to calibrate a number of different transport and kinetic parameters, such as the sticking coefficient or the ratio between ion and radical fluxes. For illustration of PVD effects, one only need consider the unity sticking coefficient cases of deposition on rough surfaces discussed earlier. Note that even in features of low aspect ratio, the step coverage of the PVD process is rather poor. This facet of PVD has led to a reexamination of alternatives to pure PVD as the aspect ratio of contacts and vias has continued to increase.

## 7.0 REAL LIFE

Some final words are in order about the application of these feature scale models for actual process investigation. Before all else, one needs to obtain a simulator. Unless one would like to develop one's own simulator (as a few of us have done!), there are a number of commercial or otherwise supported simulators available. These are, in alphabetical order, EVOLVE,[51] SAMPLE,[52] SIMBAD,[53] and SPEEDIE.[54] A version of SPEEDIE is being commercialized by Technology Modeling Associates company. I would classify most of these simulators as being in a validation phase of their development, and some questions about their robustness and fundamental integrity continue to be asked. I suspect that the strengths and weaknesses of all of these, for specific applications, reside in the accuracy with which the relevant physical mechanisms have been identified and the models for these mechanisms been calibrated. The calibration of these models is a fairly complex issue, and as mentioned previously, can presently be conducted through (a combination of) three different techniques. These are (listed in order of usefulness): test structure experiments[55] in the actual process, fundamental surface science studies (in-situ, or beam studies), and molecular dynamics computer simulations. The test structure experiments benefit from eliminating any dependencies on the specific equipment being used, and can be run with minimum effort. The fundamental surface science studies are extremely useful, if rather specialized, and the techniques include Auger

Electron Spectroscopy (AES), X-Ray Photoemission Spectroscopy (XPS), and Angle-Resolved XPS. In addition, some specialized techniques were developed specifically to study wafer or near-wafer compositions and distributions. These include independent studies by Sawin and Aydil to study angular distributions of species just before incidence upon the wafer. The molecular dynamics studies have been conducted by, among others, Graves and Jensen. The MD studies are cheap, but they suffer from less than perfect knowledge of the interatomic potentials that are central to the predictions of such simulations. In light of these complications, the average user will perhaps best benefit from obtaining one of the available simulators and satisfying oneself of the accuracy of the developers' models by validating with existing experimental data.

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# 6

# The Role Of Metrology And Inspection In Semiconductor Processing

*Mark Keefer, Rebecca Pinto, Cheri Dennison, and James Turlo*

## 1.0 OVERVIEW

As integrated circuits (IC) are incorporated into more and more products, the market demand for lower cost, higher performance devices continues to grow. In order to design and manufacture a high performance integrated circuit cost-effectively, the parameters of the manufacturing process need to be carefully controlled: film thicknesses and material properties must be accurate, uniform and controlled; linewidths and edge profiles must fall within tight limits, and the devices need to be free of defects that affect yield.

Thin film metrology and wafer inspection for defects are integral to controlling the semiconductor manufacturing process. Film properties, linewidths, and defect levels need to be measured, first to optimize the manufacturing process, then later to ensure that it is operating under control.

This chapter explores the subjects of metrology and inspection of integrated circuits. After the introduction, implementation strategies for metrology and inspection are examined from a historical perspective. Then, as we anticipate increasingly complex devices having critical dimensions of 0.18 and 0.13 μm, manufactured on 300 mm wafers, we look at how metrology and inspection will evolve to meet these measurement challenges, while simultaneously meeting increasing pressure for automation, higher throughput and higher reliability. In the final section we provide a technology reference that discusses theory of operation, equipment design principles, main applications, and strengths and limitations of the metrology and inspection systems. The sections are organized as follows:

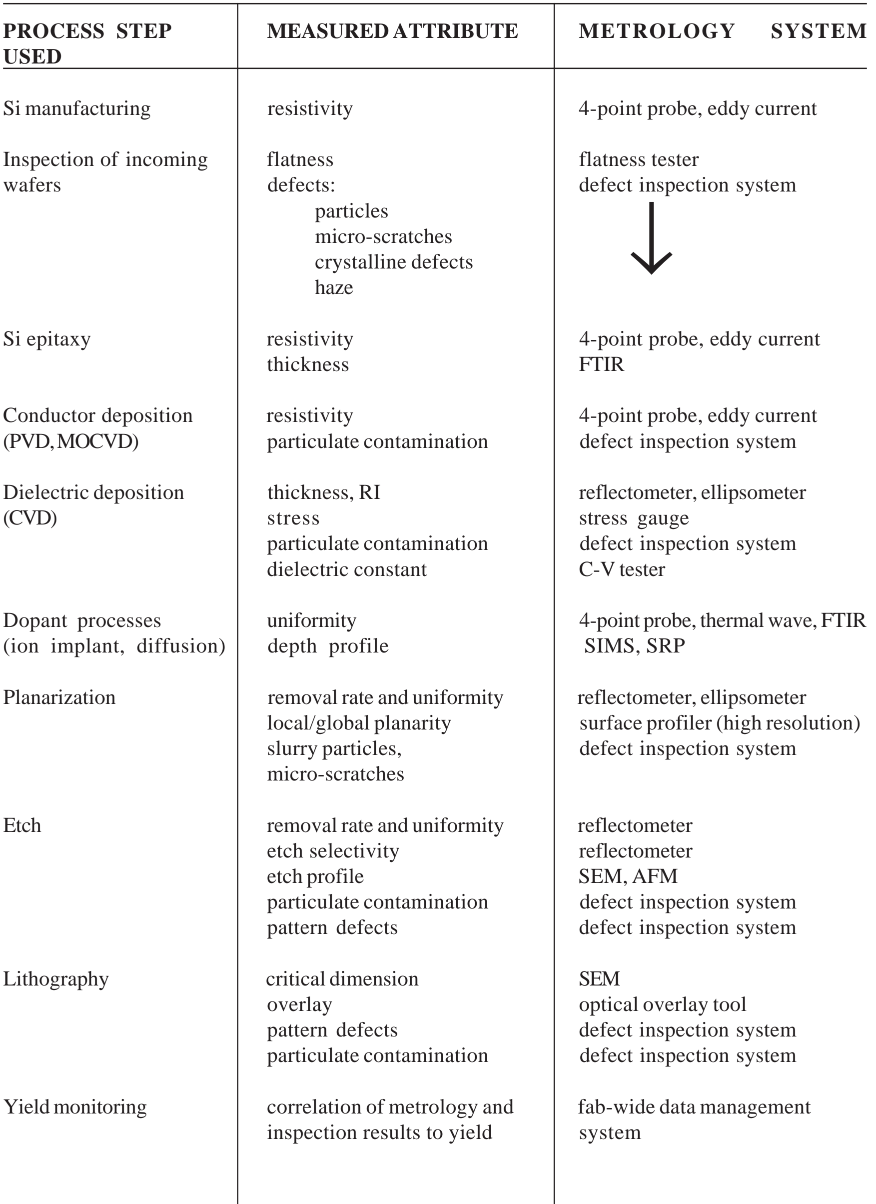
1.0 Overview
2.0 Introduction to Metrology and Inspection
3.0 Metrology and Inspection Trends: Past, Present and Future
4.0 Theory of Operation, Equipment Design Principles, Main Applications, and Strengths and Limitations of:
  4.1 Film thickness measurement systems
  4.2 Resistivity measurement systems
  4.3 Stress measurement systems
  4.4 Defect inspection systems
  4.5 Automatic defect classification
  4.6 Defect data analysis systems

## 2.0 INTRODUCTION TO METROLOGY AND INSPECTION

Metrology and inspection systems can be broadly separated into three main classifications by application: critical dimension (CD) and overlay measurements, particle and pattern defect detection, and thin film parameter measurement (such as resistivity, thickness and stress). The typical processing steps, and metrology and inspection equipment used to monitor and/or control them, are given in Table 1.

In the semiconductor industry, the continual demand for denser integrated circuits with higher performance and higher speeds drives technological advances in all facets of manufacturing. A key to the success of semiconductor processing is an understanding of the chemical, mechanical and kinetic properties of the wide range of materials used to make a typical circuit.

**Table 1.** Typical Metrology and Inspection Parameters Monitored, by Process Step



| PROCESS STEP USED | MEASURED ATTRIBUTE | METROLOGY SYSTEM |
|---|---|---|
| Si manufacturing | resistivity | 4-point probe, eddy current |
| Inspection of incoming wafers | flatness<br>defects:<br>particles<br>micro-scratches<br>crystalline defects<br>haze | flatness tester<br>defect inspection system<br>↓ |
| Si epitaxy | resistivity<br>thickness | 4-point probe, eddy current<br>FTIR |
| Conductor deposition (PVD, MOCVD) | resistivity<br>particulate contamination | 4-point probe, eddy current<br>defect inspection system |
| Dielectric deposition (CVD) | thickness, RI<br>stress<br>particulate contamination<br>dielectric constant | reflectometer, ellipsometer<br>stress gauge<br>defect inspection system<br>C-V tester |
| Dopant processes (ion implant, diffusion) | uniformity<br>depth profile | 4-point probe, thermal wave, FTIR<br>SIMS, SRP |
| Planarization | removal rate and uniformity<br>local/global planarity<br>slurry particles,<br>micro-scratches | reflectometer, ellipsometer<br>surface profiler (high resolution)<br>defect inspection system |
| Etch | removal rate and uniformity<br>etch selectivity<br>etch profile<br>particulate contamination<br>pattern defects | reflectometer<br>reflectometer<br>SEM, AFM<br>defect inspection system<br>defect inspection system |
| Lithography | critical dimension<br>overlay<br>pattern defects<br>particulate contamination | SEM<br>optical overlay tool<br>defect inspection system<br>defect inspection system |
| Yield monitoring | correlation of metrology and inspection results to yield | fab-wide data management system |

To maintain control of the product, thin film quality is regularly monitored by tools that measure electrical, physical, optical and mechanical properties of films. Film parameters typically monitored include thickness and refractive index, resistivity and stress.

Another key area for process control is the reduction of defects that affect production yield. Defect reduction is typically achieved through an iterative process that involves detection of defects, classification of defects, identification of the source of the yield-limiting defects, correction of the process to eliminate or reduce the defect mechanism, then monitoring the process for yield excursions. The process is iterative in that, while the process is monitored for defect excursions, further defect analysis is conducted in parallel to drive continuous improvement of the yield.

Defect reduction is employed for five main applications:

- Inspection of bare wafers for contamination and surface quality, either during the wafer manufacturing process or as incoming material at the IC manufacturer
- Inspection of bare wafers used to monitor the cleanliness of process (or metrology) equipment
- Inspection of product wafers to *decrease defectivity* during the early phases of the product life cycle, and throughout the life cycle for continuous improvement
- Inspection of product wafers to *monitor* processes that introduce contamination, scratches or pattern defects
- Prediction of yield

Specific tool sets have been developed to address each of these needs. Bare wafer or unpatterned wafer inspection systems are optimized for scanning wafers at high throughput without the constraint of coping with the interference of pattern signals. Inspection of patterned wafers for yield improvement or process monitoring requires a system that not only copes with pattern, but provides high capture of key defect types at reasonable throughput. For yield prediction, the ability to integrate defect information—number, type, spatial signature—with other parameters such as electrical test results, becomes the key. Theory of operation as well as equipment design principles for each of these categories of defect inspection systems are described in Sec. 4.0 of this chapter.

## 3.0 METROLOGY AND INSPECTION TRENDS: PAST, PRESENT, AND FUTURE

Metrology systems have undergone tremendous changes since the home-built bench top characterization tools of the 1960s. Inspection systems have gone through similar changes, moving from manual inspection by operators to automated inspection tools. As the semiconductor industry has grown and matured, metrology and inspection systems have kept pace. Measurement performance—predominantly sensitivity and repeatability—has steadily improved. The level of automation has dramatically increased, beginning with automated wafer handling, then pattern recognition, remote operation through development of the Semiconductor Equipment Communication Standard (SECS) protocol, development of automated algorithms that "learn" best measurement setups for monitoring a given product and process, and now automatic defect classification. These developments have supported the growing practice of making measurements on product wafers (rather than designated monitor wafers), a practice driven by the increase in wafer diameter to 200 mm, with a consequent rise in monitor wafer cost. Now, increasing attention is being paid to reliability, up-time and ease-of-use attributes, with the goal of increasing overall effectiveness of the equipment.

In the future, price-performance pressures on IC manufacturers will continue to be passed on to equipment manufacturers. The shift from off-line sampling to on-line control will accelerate, with increasing use of in-line and in situ measurements. Reliability and ease-of-use emphasis will drive the implementation of integrated, automated systems for measurement optimization, data interpretation, and adaptive feedback to the process equipment.

### 3.1 Trends in Metrology

Thin film measurements have progressed from simple single layer thickness measurements to multiple layer thickness and refractive index measurements. The trend towards multiple layer measurements has been partially driven by the increasing use of cluster deposition systems, where no opportunity exists for single layer measurements. Additionally, economics plays a role, in that as wafer sizes increase, cost savings can be realized by reducing the use of monitor wafers. In many cases, measurement of a layer on a product wafer requires measurement of the underlying layer(s) as well.

Measurement of film quality and stoichiometry has become as important as film thickness control. This is especially true with the advent of plasma enhanced CVD films such as silicon-rich anti-reflective oxynitride layers, since the film properties are strong functions of the process parameters such as plasma energy and reactant flow rates.[1]

At the same time, higher accuracy and tighter system-to-system matching are required to facilitate process transfer and reduce the time to start up new wafer fabs.

In the future, significant changes in the approach to process monitoring will occur. The trend will be to monitor processing parameters inside the processing chamber, not film characteristics; that is, process variables, not product variables. The shift from off-line sampling to on-line control will continue, with increasing use of in-line and in situ measurements. Prevention of process excursions by process control sensors should significantly reduce product loss.[2] Sensors can be equipment state (mechanical, electrical), process state (chemical/physical, temperature) or wafer state (product parameter, uniformity).

## 3.2 Trends in Defect Inspection

In the 1980s the first inspection systems were entirely manual and thus operator-intensive. Typically operators used a bright light source, and conducted visual inspections of incoming silicon, then manual microscope inspection of production wafers at various points in the process. Data was only as accurate and repeatable as the operators themselves. Results from these inspections were commonly written on paper and stored in binders and cabinets. Operators manually correlated defects to yield using two sheets of transparency paper for map-to-map comparisons. Over the intervening years advancements in IC technology, as well as economic pressures, have driven the need for enhancements in sensitivity, throughput, repeatability and automation for the defect reduction process.

In this section, we examine a few key trends in defect inspection:

- How the sensitivity of defect inspection systems has tracked critical dimensions of ICs—and how these systems are predicted to meet sensitivity needs for inspection of 0.18 and 0.13 µm devices, and beyond
- Challenges specific to inspecting 300 mm wafers

- Shifts in inspection strategies: from monitoring processes using bare wafers to using product wafers; towards differentiating yield-learning from in-line inspection; and looking forward to *in situ* inspection and adaptive process control
- Increasing automation of inspection equipment using automated wafer handling, automated data transfer, mini-environments, and remote operation
- The movement towards automated systems for measurement optimization, data interpretation, and adaptive feedback to the process equipment
- The growing emphasis on cost of ownership, overall equipment effectiveness, and ease of use

**Sensitivity Challenges as Critical Dimensions Decrease.** A good rule of thumb in defect inspection is that the critical dimension (smallest linewidth) of the device determines the minimum size of defect likely to affect yield. At early steps in the process, defects as small as one-third the critical dimension can cause an electrical failure; at back-end levels, detecting defects about as large as the CD is sufficient to protect yield. Until recently DRAM devices had the smallest critical dimensions of any device on the market; at present, logic devices also have leading-edge critical dimensions. Historically manufacturers of inspection equipment watched DRAM manufacturers closely, striving to stay ahead of the design rule of the next memory device, so that the inspection system would be able to detect yield-limiting defects. Today we have various industry consortia, and in particular, the National Technology Roadmap for Semiconductors,[3] to guide metrology and inspection equipment manufacturers in the design of next-generation inspection systems.

Figure 1 shows a history of how the detection limit of inspection systems has kept ahead of the critical dimension of IC devices. Unpatterned wafer inspection systems currently on the market can now detect defects as small as 80 nm, whereas patterned-wafer systems can detect defects less than 100 nm.* The advances that have allowed inspection systems to continue to improve performance include:

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* Quoted detection limits are referenced to NIST-traceable polystyrene latex spheres of known size deposited on clean, well-polished bare silicon wafers.

- New optical designs
- More powerful and/or shorter-wavelength light sources
- More accurate wafer stages
- Higher resolution cameras
- Better signal processing algorithms

These evolutionary changes are ongoing for optical-based inspection systems, and the existing technology is proving to be extendible for inspection of 0.18 and 0.13 μm devices.

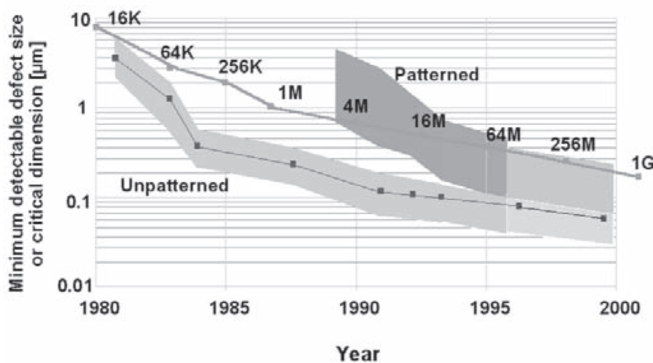


**Figure 1.** Critical dimension of integrated circuits (upper line) determines detection limit specifications for defect inspection systems (wide bands). Historically, smaller defects have been detectable using unpatterned systems, where the additional challenge of coping with pattern signal is not present.

An inspection technology based on scanning electron microscopy (SEM) is being used in addition to optical-based inspection systems for development of 0.25 and sub-0.25 μm processes. The biggest challenge for such high sensitivity inspection is providing cost-effective throughput. Despite this challenge, SEM-based automated inspection systems are used in advanced IC lines throughout the world.

SEM-based automated inspection systems provide two unique defect-detection capabilities. The first results from a SEM's high resolution and large depth of focus: these systems can find small defects hidden in dense geometries where they can not be seen by optical microscopy. The second unique capability is the result of new, nontraditional SEM designs that

enable a properly optimized system to see contrast differences in electrically defective IC features. A common example of this type of defect is an electrical fault caused by voids in the metal that fills a contact or via. Here the structure of the metal plugs appears correct when viewed from the top surface, but a cross-section reveals that the metal doesn't fill the bottom of the contact hole. In this and similar cases an electron-beam inspection tool that is designed to maximize the charge-induced voltage contrast effect may detect the problem as a slight difference in contrast of the feature in the SEM image. This voltage contrast imaging ability has opened up new applications for automated defect inspection tools. For further information on this capability, see Ref. 4.

**Inspection Challenges for 300 mm Wafers.** As pilot lines are coming up for production of devices on 300 mm wafers, inspection systems that accommodate these wafers are entering the market as well. Unpatterned inspection systems for 300 mm wafers have been on the market since early 1997, as these are required well in advance of production to allow process equipment vendors to develop their 300 mm equipment. Patterned wafer inspection systems are expected to be introduced in 1998. The main challenge for inspecting 300 mm wafers is cost of ownership; particularly the increased footprint of the system, and the challenge of maintaining high throughput. Compared to a 200 mm wafer, a 300 mm wafer has an area 2.25 times as large, and for most equipment designs, throughput scales roughly linearly with inspected area. Maintaining the same wafer-per-hour throughput specifications for 300 mm as currently available for 200 mm wafers could be achieved in one of several ways:

- Evolutionary improvements to subsystems including faster data rates, faster scanners, less reliance on scanning the stage since its mass is relatively large.
- Revolutionary new scanning designs, such as the spinning wafer strategy currently employed on some high throughput unpatterned wafer inspection systems.
- Adapting the sampling strategy to inspect a sparser fraction of the wafer area.

The high cost of 300 mm wafers also exerts economic pressure for devices to be built all the way to the edge of the wafer, and thus inspection closer to the wafer edge is necessary to protect yield.

## 3.3 Trends in Inspection Strategies

**Shift of Process Monitors from Bare Wafers to Production Wafers.** Monitor wafers have been used widely for tool qualification and process monitoring throughout the IC manufacturing process. Bare wafers have been run on every shift to qualify the equipment for use. In recent years, focused contamination reduction efforts on the equipment have enabled a better understanding and control of the contribution of the process equipment to contamination of product wafers. Defect types and mechanisms are better characterized, and programs for cleaning or preventive maintenance of the equipment are in place. Thus the need for such rigorous equipment monitoring is predicted to decrease.

The cost of monitor wafers has always been significant, and has become more so with the introduction of 200 mm wafers and the imminent move to 300 mm. Thus, more fabs have begun to relegate the use of monitor wafers to bringing up new tools and diagnosing specific contamination problems, while using product wafers to monitor their processes.

Interestingly, the predicted decline in use of monitor wafers has not been reflected in declining sales of unpatterned wafer inspection equipment. The rapid expansion in the semiconductor industry during the 1990s has driven strong growth in unpatterned wafer inspection system sales, dominating any effects of decreasing monitor wafer use.

**Looking Ahead to *In Situ* Inspection and Adaptive Process Control.** A logical extension to process monitoring is to incorporate the inspection system into the process tool itself. An in situ inspection system could provide information to the process tool, so that when defect excursions are detected, the process tool could be flagged and shut down, or perhaps even adjusted to eliminate the defect mechanism. Having the inspection tool provide closed-loop control of the defectivity of the process is an example of adaptive process control.

The barriers that currently exist for achieving this scenario are significant. At present, the capability of a stand-alone inspection system would be difficult to reproduce inside the economic and physical constraints of a process chamber. Also, understanding how to adapt a process to eliminate the defects detected by the inspection system is nontrivial for a team of experienced engineers. Designing an expert system to replace that body of knowledge would be a significant challenge. However, strong economic pressures exist to reduce the cost of the defect reduction process, and part of the solution may involve meeting the challenges of in situ inspection.

An alternative approach—and another example of adaptive process control—is to provide tighter control of the process parameters through improvements to in situ environmental sensors. This more direct, causal means of addressing process control issues involves rapid measurement and feedback based on process parameters, e.g., temperature and pressure. In contrast, an in situ inspection system measures the effects of out-of-control process parameters: defects incurred on the product wafer.

**Trends in Automation of Wafer Inspection Equipment.** An ongoing trend for IC inspection has been a growing emphasis on automation of the inspection process: automating the inspection and defect review equipment itself, and integrating it with yield data using defect data management systems. The cost of ownership of the inspection process decreases as automation is introduced, because trained engineers and operators can focus elsewhere in the fab. Repeatability and accuracy increase as the subjective nature of human judgment is replaced by standard algorithms. Automation facilitates the de-localization of a given manufacturing process, allowing the process to be copied exactly from fab to fab around the world. Automation can also support a more rapid return on investment by helping ramp a process to yield in a shorter time.

Automation began with the introduction of automated wafer handling using mechanical robots, and has expanded its scope to include other subsystems within the wafer inspection and defect review tools. In an effort to reduce operator error and increase throughput, Optical Character Recognition (OCR) and Bar Code Reading (BCR) were incorporated into these tools to read lot and wafer information during automatic inspection or review sequences. Signal towers communicate the status of the systems through colored or flashing lights, and mini-environments and pods enclose the wafer cassette or the inspection or review tool to enhance the cleanliness of the local environment.

The development of the Semiconductor Equipment Communication Standard (SECS) protocol allows a host computer to operate the inspection and review systems remotely, initiating automatic inspection and controlling the flow of data from the inspection tool to the review tool to the fab database. One benefit of this automation is the reduction of operator error in the selection of measurement recipes and data entry of basic lot information.

Automated defect data management systems were introduced to deal with the tremendous amount of data generated by automatic defect inspection systems. Yield correlation is one of the primary tasks of the defect data management system. The newest systems automate yield

correlation by overlaying maps of electrical test results with defect maps, bringing in defect type information from review stations, then delivering yield statistics by process level and defect types. This information has given the defect reduction engineer the ability to focus quickly on the defect types and process layers that most affect yield.

Defect data management systems have also adopted the use of statistical process control (SPC) monitors that flag out-of-control defect data. In a typical fab today, the inspection tools automatically feed data (defect count, type, intensity, spatial signature) to the data management system. The data management system constructs SPC charts from the incoming data and checks for out-of-control status (using conditions predetermined by the engineer). If the data are out-of-control, the system alerts the engineer by e-mail or pager.

Automated transfer of data from the inspection system to the review station represented a tremendous step forward in automating the inspection process. Review stations—traditional white-light, laser confocal or SEM; stand-alone or incorporated into the inspection system—take the coordinates of the defects reported by the inspection system and automatically drive to those locations on the wafer. The defects are then quickly reviewed, and classified either manually or using automatic defect classification (discussed in next section). This capability led to faster and better understanding of defect origins and mechanisms and their impact on yield.

**Trends in Automation through Advanced Algorithms.** A further step in automation is the use of algorithms to replace human operators for optimization of system parameters to create "recipes" to inspect a given level for a given set of defect types, and automatic defect classification (ADC). Advancements in these algorithms are likely to reduce cost of ownership of the inspection process substantially over the next few years.

***Automated Recipe Creation Procedures.*** When a new device and/or process level is inspected for the first time, a recipe has to be generated that contains optimized measurement parameters such as optical and signal processing configurations. The procedures for creating these recipes—and the number of parameters involved—have become more complex as inspection technology has advanced. Thus, automation of the procedure has escalated in importance. Automated recipe creation is particularly important in an ASIC fab in which many different products are manufactured, and during an excursion when quick recipe creation at a nonstandard inspection point may be needed.

Simply stated, automated recipe creation works by evaluating changes in the signal-to-noise ratio as the different optical and signal-processing parameters are systematically varied. A brute-force approach would try every combination of every parameter. For today's complex systems, the number of variables would make this a cost-prohibitive task. A more elegant approach would make use of existing knowledge, at least to eliminate certain combinations of parameters, and perhaps even to find an efficient path through the multivariable space that arrives at a unique, repeatable solution.

Today, automated recipe creation results in a recipe that sometimes can benefit from further optimization by a well-trained engineer. Improving automated recipe-creation algorithms is an area of focus for developers of wafer inspection tools, due to its importance in increasing the overall effectiveness of the equipment.

***Automatic Defect Classification (ADC).*** One of the biggest bottlenecks in the inspection process is classification of defects, a necessary step to determining and eliminating their source. At present, most defect classification is still manual, requiring a trained operator to judge a microscope image and sort defects into categories based on the operator's experience (often using a reference book containing pictures of "typical" defects). This process is limited in speed, accuracy and repeatability, and thus does not fit well into an industry driven by time to market and cost control.

For these reasons automatic defect classification (ADC) has gained tremendous attention of late. ADC has begun to reduce significantly the amount of manual classification needed, increasing the throughput of the classification process, and reducing subjectivity and error from operator classification.[5] ADC thus enables more and better analysis of defect information.

The current implementation of ADC begins first by teaching the system to recognize the defect types by providing it with clear example images. Then during actual automatic classification a review microscope (off-line or built into the inspection tool) drives to the coordinates of the detected event on the wafer and re-detects the event within the field of view. The review station generates a digital image of the event using traditional optical, confocal or SEM-based techniques. The ADC algorithm then extracts features from the event and compares those features statistically to the example images. The output includes a classification for the event along with a goodness-of-fit value that describes the image's similarity to the images from the example defects in its class.

The ultimate implementation of ADC would be for classification to happen in parallel with inspection, without having an impact on inspection throughput. Partial accomplishment of the goal of real-time ADC is available today using the techniques of *real-time grouping* and/or *spatial signature analysis*.

Real-time grouping (also called real-time defect classification or RTDC) makes maximum use of whatever descriptive information can be recorded during inspection. The intensity of the scattering signal; the difference in intensity seen by collectors spanning different solid angles of the scattering hemisphere; the gray scale intensity or perimeter of the pixels comprising the image—these are examples of types of information that might be captured in real time by an optical inspection system. Separating defects into coarse groups such as "large," "small," "bright," "dark," and so forth can now be accomplished by many inspection systems during inspection.

The spatial relationship between detected events (also called the signature) can be used to discriminate between typical extended defects found on wafer surfaces. Novel clustering algorithms are used to capture the spatial signature of extended defect types such as polishing scratches, handling damage, crystallographic defects, voids, foreign particles and stress related defects.

Real-time grouping reduces the number of detected events that need to be classified manually or using high-resolution ADC. Every step towards improving time to results provides value for cost-effective IC manufacturing.

**The Growing Emphasis on Cost of Ownership, Overall Equipment Effectiveness, and Ease of Use.** Many of the trends in inspection technology discussed above are driven by the need for integrated circuits to be brought to market quickly and at contained cost. The challenge to the inspection part of the process is to provide more defect information in an increasingly cost-effective manner. The concept of lowering cost of ownership (COO) has been replaced recently with a new concept: overall equipment effectiveness (OEE). As applied to inspection equipment, COO includes the purchase price of the system and its throughput, whereas OEE also weights heavily those characteristics that enable a system to provide the best defect information in the fastest time, with maximum ease of use and minimum cost, in a production environment.

For inspection equipment, key elements of high overall equipment effectiveness include:

- High defect capture probability, i.e., high probability of detecting a representative fraction of defects from the population of all defect types present on the wafer.
- High correlation of detected events with yield-limiting defects: low false or nuisance counts.
- High throughput.
- Low system purchase price.
- High reliability: high repeatability of measurements; minimum downtime; minimum maintenance.
- System matching: highly correlated results using systems of same model number; easy transfer of recipes between tools and between fabs.
- Ease of use: automated recipe learns and operation with minimum intervention of highly paid personnel.
- Maximum integration of defect inspection, review, classification and analysis process.

Not all of these elements may be captured in equations measuring OEE, but all of them are key elements for operating the defect reduction process at highest possible efficiency and lowest cost.

The final element of successful yield enhancement through defect reduction is close communication between defect metrology and process engineering groups. A highly effective defect reduction program seamlessly integrated with a strong process engineering program is well positioned for success in the semiconductor market.

## 4.0 THEORY OF OPERATION, EQUIPMENT DESIGN PRINCIPLES, MAIN APPLICATIONS, AND STRENGTHS AND LIMITATIONS OF METROLOGY AND INSPECTION SYSTEMS

This section briefly discusses the theory of operation, main applications, and the strengths and limitations of several thin film metrology systems. For a more detailed theoretical discussion, the reader is encouraged to consult Ref. 6.

## 4.1 Film Thickness Measurement Systems

**Theory of Operation.** The common optical measurement techniques include reflectometry (using unpolarized or polarized light) and ellipsometry. System implementations use multiple wavelength or multiple angles of incidence. Regardless of the type of system, the data analysis methods that transform the directly measured quantities to the parameters of interest such as thickness and refractive index are similar. The measurement recipe contains information about the film stack to be measured, such as the type of material, approximate thickness of the material, and (implicitly) the refractive index of the material. The Fresnel reflectance equations are used to calculate theoretical spectra for the film stack. The calculated spectra are compared with the measured spectra, and regression analysis is performed by varying the parameters of interest until the best fit is obtained. The best-fit values are reported, along with a figure of merit referred to as the goodness-of-fit (GOF).

The capability of a system to report parameters of interest such as thickness and refractive index values derives from the amount and type of raw data measured by the system. Generally, the information content of the raw measured values (for one wavelength and one angle of incidence) increases in the following order: unpolarized reflectometry ($R$); polarized reflectometry ($R_p$ and $R_s$); and ellipsometry ($\Psi$ and $\Delta$). Although both polarized reflectometry and ellipsometry measure two values at each wavelength and angle, ellipsometry is unquestionably the more powerful technique for a number of reasons.[7] Ellipsometry measures the phase of the reflected light (not just amplitude). Ellipsometric measurements are relatively insensitive to intensity fluctuations of the illumination source, temperature drifts of electronic components, and macroscopic roughness. Macroscopic roughness causes light loss by scattering incident light away from the detector, which can be a serious problem in reflectometry but not in ellipsometry, for which absolute intensity measurements are not required. Ellipsometry is inherently a double beam technique, because one polarization component serves as amplitude and phase reference for the other.[8]

The other system implementation choice is to collect data using multiple angles of incidence or using multiple wavelengths. Data collected using multiple wavelengths generally have higher information content than data collected using multiple angles of incidence. An examination of the phase term $\phi$ of the Fresnel reflectance equations shows a first order change with wavelength, while a change with angle is contained within a sine term:

Eq. (1) $$\phi = 4\pi \frac{d}{\lambda} n_1 \cos\theta_1 = 4\pi \frac{d}{\lambda} \sqrt{n_1^2 - \sin^2 \theta_0}$$

where $\theta_1$ is the refracted angle of light in the film, $\theta_0$ is the incident angle (in ambient), $d$ is film thickness, and $n$ is refractive index.

The consequence is higher sensitivity to film changes with wavelength than angle. (For oxide, the percentage change in the phase term with wavelength from 200 to 800 nm is an order of magnitude higher than with a change in angle from 0 to 90°). Additionally, multiple wavelength systems take advantage of the fact that a physical property of a film, the refractive index, is a function of the illumination wavelength (refractive index dispersion) as illustrated in Fig. 2. Refractive index is not a function of the angle of incidence of the illumination. Therefore, little information about the physical properties of the material can be deduced by measurements using multiple angles. Conversely, the RI dispersion difference between different materials can be exploited by multiple wavelength systems. The consequence is that a change in the thickness (or RI) of one film in a multiple-layer film stack will change the measured spectra differently than a change in a different layer. The different optical penetration depth as a function of wavelength provides additional information to resolve the thicknesses of several layers in multiple layer structures.[8] This implies that a multiple wavelength metrology system will be sensitive to, and be able to differentiate between, thickness and index changes in multiple-layer film stacks. Spectroscopic ellipsometry provides the highest level of capability of the optical thin film measurement techniques, by collecting ellipsometric data over a large range of wavelengths. Only spectroscopic ellipsometry uses all properties of polarized light: amplitude, phase, and wavelength.

*Unpolarized reflectometers* measure reflectance ($R$) versus wavelength at a single angle of incidence (normal to the wafer). Light reflecting from the top surface of the film interferes with light reflecting from the film to substrate interface, resulting in a periodic variation in reflectance as a function of wavelength spectrum.

*Polarized reflectometers* measure polarized reflectance ($R_p$, $R_s$) versus angle of incidence at a single wavelength. A high numerical aperture objective lens is used to achieve a small spot size, resulting in multiple angles of incidence. Reflectometers, whether using polarized or unpolarized light, require calibration to known standard wafers (referred

to as a *referenced* technique). These wafers can be either bare silicon or wafers of a "known thickness." This is because reflectometers need to know very accurately the value of absolute reflectance, and to be able to compensate for intensity losses through aging of the illumination source, efficiency of the metrology system optics, etc. (referred to as optical throughput).

*Ellipsometers* measure the amplitude ratio ($\Psi$) and phase change ($\Delta$) of polarized light upon reflection from a sample. Single wavelength ellipsometers are available with a high numerical aperture objective lens to achieve a small spot size, resulting in multiple angles of incidence. The use of multiple angles eliminates the problem of thickness order ambiguity.

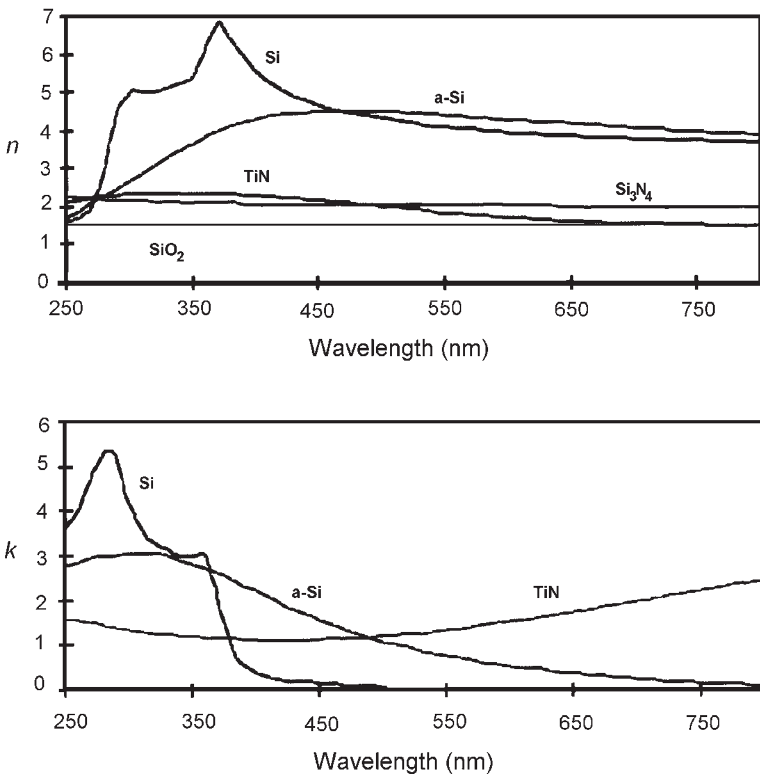


**Figure 2.** RI dispersion of materials commonly used in the semiconductor industry. The refractive index $n$ is the upper plot; the extinction coefficient $k$ is the lower plot.

*Spectroscopic ellipsometers* measure amplitude ratio and phase change versus wavelength at a single angle of incidence. (Research grade spectroscopic ellipsometer systems also offer multiple angles of incidence for material characterization). The angle of incidence is typically 70–75°, near the Brewster angle, selected for its maximum sensitivity to changes in film thickness on silicon substrates (Fig. 3). Attributes of commercially available instruments are summarized in Table 2.

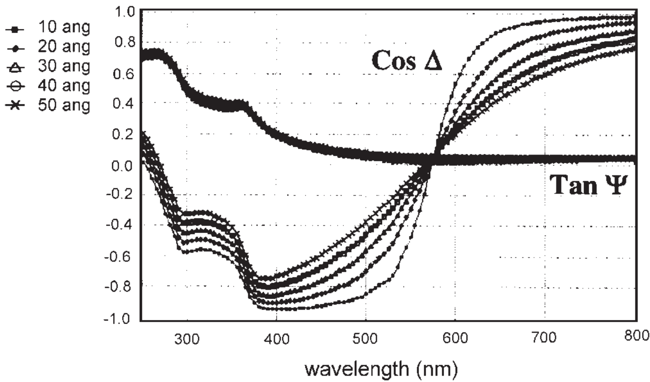


**Figure 3.** Sensitivity of SE technology (phase change term, cos Δ) to very thin oxide thickness changes when operating near the Brewster angle.

**Table 2.** Typical Instrument Configurations Used in Semiconductor Process Monitoring

| | Property of Light Used | | | Angle of Incidence | Referenced Measurement |
|---|---|---|---|---|---|
| | Amplitude | Phase | Wavelength | | |
| Unpolarized Reflectometer | yes | no | yes | single (normal) | yes |
| Polarized Reflectometer | yes | no | no | multiple (~normal) | yes |
| Focused Beam Ellipsometer | yes | yes | no | multiple (oblique) | no |
| Spectroscopic Ellipsometer | yes | yes | yes | single (oblique) | no |

**Main Applications.** Thin film metrology systems are used in every process module in semiconductor fabs; to monitor thickness and/or refractive index uniformity in deposition and diffusion areas, for removal rate and uniformity in etch and planarization areas, and to monitor reflectivity in metal deposition or photolithography areas. Depending on the measurement technique, semitransparent films from several angstroms to several microns in thickness can be measured. Historically, ellipsometry was used in diffusion areas for very thin films, and reflectometry was a general thin film tool. These distinctions are diminishing as advances are made in measurement technology, and many systems now incorporate more than one type of technology.

**Strengths.** The ability of technologies such as spectroscopic ellipsometry to simultaneously and independently measure multiple film thicknesses and refractive indices offers opportunities to semiconductor manufacturers for reduced cost and enhanced process control. Wafer fabrication costs can be reduced through decreased use of monitor wafers. This is especially important for 200 mm and 300 mm wafers. As an example, the ability to measure nitride over amorphous silicon over oxide in a DRAM structure means that a nitride on silicon monitor wafer can be eliminated. Additionally, the increasing use of multi-process chamber cluster deposition tools requires the ability to measure multiple-layer film stacks, since there is no opportunity to measure each layer after it is deposited.

Semiconductor fabs are becoming more interested in monitoring and controlling film quality, as opposed to merely film thickness. The refractive index of a film is a key indicator of film composition. For films such as amorphous silicon and polycrystalline silicon, the extinction coefficient $k$ (part of the complex refractive index $\tilde{N} = n + ik$ ) is directly related to the crystallinity of the film. Process temperature (of the deposition or anneal step) determines the crystallinity. New materials such as silicon-rich oxynitrides and nitrides are increasingly used as anti-reflective layers. The stoichiometry of these films can also be monitored by UV spectroscopic ellipsometry measurement of refractive index.[1] Therefore, the ability to measure refractive index, not only of a single-layer film, but also of a film in a multiple-layer film stack, is beneficial.

**Limitations.** Reflectometers require calibration using wafers of known reflectance, and can be subject to measurement drift over time. Single wavelength ellipsometry is known for limitations such as thickness order uncertainty, and thickness regions where refractive index cannot be calculated. Multiple angle systems eliminate thickness order ambiguity for single

layer films. Use of a small spot size and a single wavelength can be problematic when measuring rough films that scatter light.

All optical tools require a film stack model for their regression analysis. Accuracy can be affected by selection of an appropriate refractive index dispersion model. Materials which do not have a consistent spatial composition, e.g., their refractive index changes with depth, require special models to measure correctly.

Future gate dielectric process control will be a difficult challenge, if composition information is required as well as thickness uniformity. Increasing attention will need to be paid to the interface between the gate dielectric and the silicon substrate for proper measurement accuracy.[9] There is also an inherent difficulty in monitoring metrology system stability at a 4 nm gate dielectric thickness, as these wafers tend to change thickness over time due to environmental effects.

Measurement spot size considerations result in the use of test structures, typically located in the scribe lines, since no metrology system can currently measure inside of submicron features.

## 4.2 Resistivity Measurement Systems

**Four-Point Probes.** ***Theory of Operation.*** Four-point probe (4PP) systems measure sheet resistance ($R_s$), the local resistance of a sheet of material, in units of ohms/square. Sheet resistance is expressed in the equation $R_s = R_b/t$, where $t$ is the thickness of the conductive layer, and $R_b$ is the bulk resistivity (ohm-cm) of the layer. For a material with constant bulk resistivity, the sheet resistance is only a function of thickness. A four-point probe consists of four spring-loaded conductive probes (usually in a linear array) which are placed in contact with the material whose sheet resistance is to be measured. (The four-point probe technique requires some isolating junction or blocking layer to the DC current used).

Typically, a known current is forced between the outer probes, and the resulting voltage across the inner two is measured. Ohm's Law ($V = IR$) is then used, with a geometrical correction factor, to calculate the sheet resistance of the material. To compensate for geometric errors arising from variations in probe tip spacing and proximity to the wafer edge, the dual configuration technique was developed. A second measurement is made, with current forced through pins 1 and 3, and voltage measured between pins 2 and 4 (Fig. 4). The geometrical correction factor can then be calculated based on the ratio of the measured resistivities.[10]

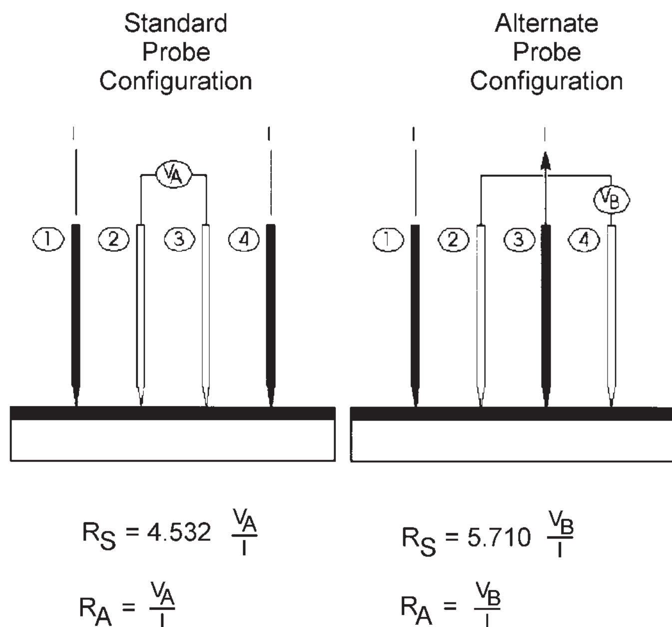


**Figure 4.** Dual configuration four-point probe measurement setup.

***Main Applications.*** Resistivity systems are used throughout the fab to measure any conductive semiconductor layer; from incoming silicon wafer inspection, to metal deposition and etch/planarization for removal rate and uniformity, to dopant uniformity in diffusion and ion implant operations. Ion implantation was the first process to extensively use 4PP for process control, and also the first to exploit the power of full wafer uniformity mapping as a process diagnostic. The normal range for sheet resistance in semiconductor processing is from less than 0.02 ohm/square for aluminum films, to about 1 mega-ohm/square for low dose implants into silicon.

***Strengths.*** The four-point probe is the most common tool used to measure sheet resistance, due to its accuracy, repeatability (~ 0.2% 1σ), and relatively low cost. The most accurate systems employ temperature compensation, to account for variations in the resistance that occur with variations in ambient temperature. Temperature compensation is especially important to achieve system to system accuracy matching, an increasingly common requirement not only within a fab, but also for process transfers between fabs.

***Limitations.*** Because the 4PP technique is based on physical contact with the wafer, its use is limited to monitor wafers. Care must be taken to ensure low contact resistance between the probe tips and the conductive layer. Probe tip "conditioning" and qualification routines have been developed to manage this concern.

The most challenging applications for 4PP are low energy (ultra-shallow junction), low dose (high sheet resistance) ion implants. These processes require enough probe tip pressure to penetrate down to a more conductive depth but not so far as to penetrate past the junction. Reductions in measurement edge exclusion are also required.

**Eddy Current (Mutual Inductance).** ***Theory of Operation.*** Eddy current or mutual inductance techniques determine sheet resistance of a film by creating a time-varying magnetic field from a coil ("probe head"). The coil radiates energy, is placed close to the conductive layer, and eddy currents are generated by the absorbed energy in the conductive layer. The eddy currents in turn create a magnetic field that induces a reverse current in the coil (hence the term mutual inductance). The sheet resistance of the conductive layer determines how much current is induced in the $R_s$ sensing circuit. The more conductive the film, the more energy is trapped in the film to create eddy currents. The magnetic field drops off with distance (depth into the film).

Various configurations exist: "single-side," where the wafer is placed under the inductive coil (Fig. 5), and "dual-side," where the wafer is placed inside the turns of the inductive coil. The dual-side approach, developed first, typically has a larger spot size and greater measurement range. The measurement is made in a transmission mode. Decreasing the spot size requires decreasing the distance between the coils. A practical limit of spot size results from clearance between the sample and the coils. The single-side approach, essentially a reflection measurement, offers advantages of higher sensitivity to the top layer than the underlying layer/substrate, smaller measurement spot size, and reduced edge effect.

***Main Applications.*** Historically, eddy current systems have been used for incoming inspection of resistivity of prime silicon wafers. More recently, as the RC time delay of interconnect layers has become a gating item to increasing device speeds, the technique has been applied to measurement of blanket metal layers prior to patterning.[11] Since the metal layer is unpatterned, it supports eddy current formation. Underlying metal films are patterned, which prevents the formation of eddy currents. The typical resistance range covered by eddy current systems is 0.001~50 ohms/square for single-side and 0.01~5000 ohms/square for double-side.

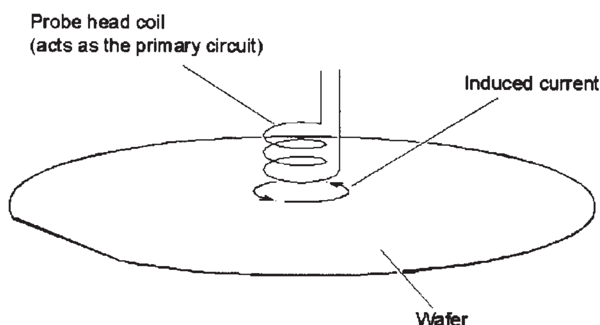


**Figure 5.** Eddy current measurements (single-side configuration).

***Strengths.*** Because it is a non-contact technique, it can be used on product wafers. This is desirable for several reasons: significant cost savings by reducing monitor wafers, better equipment utilization by processing fewer monitors, and improved process control by measuring actual product wafers.

***Limitations.*** Since the magnetic field penetrates through the top metal layer of interest, the technique works best when the resistivity of the underlying layers/substrate is high relative to that of the conductive metal layer (e.g., typical memory applications). In the case of low resistivity substrates, the technique can be extended somewhat by calibration or software correlation.[12] Eddy current systems are typically calibrated using four-point probes. Spot size can be an issue as smaller measurement edge exclusions are required.

### 4.3 Stress Measurement Systems

Although properties like film thickness, density, and resistivity can be immediately related to device performance, the level of stress in a thin film is more important to long term device reliability and lifetime.

Stress in a thin film develops primarily during the deposition process and consists of two components: the intrinsic stress and the extrinsic stress. The intrinsic stress is the component of stress in the film caused by the deposition process itself. For example, a slowly sputtered metal film deposited onto a heated substrate will grow with near zero stress, although the film structure may be metastable. By contrast, a chemical vapor deposition (CVD) oxide film can have a highly variable stress level depending on

film density, moisture content or residual reactants such as hydrogen. Within a wide range, the intrinsic film stress for most materials can be controlled by the process parameters of the deposition system.

The extrinsic stress is the component of stress caused by a change in the external conditions on the wafer. For example, most films have a thermal expansion coefficient different from the silicon substrate, so when the temperature changes, the film and substrate try to expand or contract by different amounts. However, because they are bound together, a stress will develop in both the film and the substrate. Since films are typically deposited above room temperature, the process of cooling after deposition will introduce a thermal component of stress into most films. The total film stress will be the sum of the intrinsic and extrinsic components.

**Theory of Operation.** To maintain static equilibrium, the forces and moments in the film must balance the forces and moments in the substrate, which requires a shape change of the wafer when a stressed film is deposited. For the geometry of a thin uniform film deposited on a much thicker, but platelike wafer, the shape change caused by the addition of a film will be a uniform bowing of the wafer like a spherical bowl or dome, but several assumptions are involved:

- The substrate can be treated as a plate which simplifies the elasticity equations. The basic requirement for meeting the plate geometry is that the characteristic length dimension be more than about 10 times the thickness. The approximation errors can be significant unless the ratio is notably higher, and in the semiconductor industry, a typical 200 mm wafer is under 1 mm thick. The ratio is well over 100:1, so the plate approximation is quite accurate.
- The film is uniform and homogeneous in any feature that can influence stress, primarily the thickness. The stress in a film deposited only on one face of a wafer will give rise to forces and bending moments that change the shape of the wafer. If the film is uniform, the forces will be evenly distributed causing an even shape change. The stress is biaxial, so the elasticity equations can be solved to relate radius of curvature of the resulting shape change to the film stress. Any significant variations in the film thickness, chemical composition or internal structure of the film can lead to nonuniform bending and an inaccurate average stress calculation.

- The film is much thinner than the substrate. The assumption leads to the simplest equation to relate film stress to change in curvature of the wafer which is called the Stoney equation (Eq. 2). Most researchers and equipment companies use the Stoney equation to calculate stress. The equation relies only on the elastic properties of the substrate, so the stress in any film material regardless of quality can be determined. However, if the film thickness reaches about 5% of the substrate thickness, the calculation error will be about 10%. Again, in the semiconductor industry, films are typically less than a few microns on substrates over 500 microns, so the ratio is under 1% and the error is insignificant.

An important point about the typical commercial equipment available to determine stress is that all systems measure curvature or shape. The raw data must be analyzed to yield a radius of curvature before and after film deposition. The change in radius is then used to calculate stress. A tool to accurately and conveniently measure film stress directly does not exist. The stress calculation is based on the Stoney equation,

Eq. (2) $$\sigma_f = \frac{1}{6}\frac{E_s}{1-V_s}\frac{t_s^2}{t_f}\left[\frac{1}{R_f}-\frac{1}{R_s}\right]$$

The subscripts *s* and *f* refer to the substrate and film, respectively, while *E* is Young's modulus, *v* is Poisson's ratio, *t* is thickness and *R* is the measured radius of curvature.

**Main Applications.** Film stress can give rise to a number of problems that can lead to failure in the operation of an integrated circuit, so determining film stress is important for maintaining a reliable process. Two common issues are cracks forming in highly stressed, brittle passivation layers, and voids forming and growing in aluminum lines. Stress also contributes to reliability failures such as electromigration. Other issues can include debonding of high stress metal films like tantalum, or sorption of volatiles like water and organic solvents from porous films.

Stress measurement can be divided into two categories with distinctly different goals: testing done at room temperature and testing done while thermally cycling a wafer. Room temperature testing is typically used for monitoring an established deposition process for an SPC style control.

Thermal cycling is typically used for process development and materials characterization.

***Room Temperature Testing.*** Room temperature testing provides basic process control data. The stress level in a film can be influenced by controlling the deposition parameters such as temperature, pressure, reactant flow rates and input power, so film stress can be used as part of the process development. Once an acceptable set of deposition conditions are established, continual monitoring of the resultant film stress will give a measure of the long-term stability of the deposition system. The results are ideally suited to a simple SPC control on the film deposition process.

Advanced stress measurement systems include stress mapping capabilities over the surface of the wafer. Information about the stress distribution throughout the film is especially valuable in determining the uniformity of a deposition process beyond basic film thickness uniformity results.

***Thermal Cycle Testing.*** Thermal cycling of a film-wafer sample provides data that delves more deeply into the mechanisms of stress generation and evolution. Generally, the thermal expansion coefficient of the film and substrate will be different, so changing the sample temperature will impose a thermal component of strain that can lead to high stresses in the film.

Optical techniques are required in which a laser can be aimed through a transparent window to measure curvature and stress continuously during thermal cycling. Numerous thin film effects have been observed including yield behavior in metals, effusion of volatiles from porous films, phase changes, and hillock formation.

Thermal testing allows for a more fundamental examination of the mechanical behavior of thin film materials. The stress data obtained during thermal cycling can be used to approximately determine thermal expansion coefficient, modulus of elasticity and some activation energies. The technique has also been used on polymeric films to determine glass transition temperatures.

**Deflection Measurement Techniques.** Several techniques relying on differing technologies have been developed to measure film stress, but all basically measure the average radius of curvature of a wafer before and after the film deposition. An overview of four measurement techniques will be given: one directly measures bow optically, and the other three scan the shape of the wafer surface using either a two plate capacitor, a contact stylus profiler, or a laser lever.

***Bow Measurements.*** The most direct measurement technique uses a fiber optic sensor to determine the bow at the wafer center before and after film deposition. The wafer is supported by a knife edge ring of diameter $D$, so the bow, $d$, is related to the radius of curvature by the equation

Eq. (3) $$R = \frac{D^2}{8d}$$

The change in radius caused by the film is related to the stress using the Stoney equation. The fiber optic sensors can measure bow changes with a resolution in the range of 0.05 microns, but using one central measurement to represent the entire wafer shape limits the accuracy of the stress measurement. Advanced versions of these systems include multiple probes that allow deflection and stress mapping over the entire wafer.

Strengths of this technique are that it is simple, non-contact, and sensitive. Limitations are a limited amount of data (one data point) and poor thermal performance.

***Capacitance Measurements.*** The capacitance probe technique measures the capacitance between a small probe and the surface of the wafer from which the distance to the wafer can be determined. By using probes simultaneously on the front and back surface of the wafer, the wafer thickness is determined along with the wafer position between the two probes. The wafer is automatically moved through the probe to obtain a map of thickness and shape. Using the Stoney equation and numerically fitting the shape data, average stress or stress maps can be obtained. The capacitance probes determine bow with a repeatability ($1\sigma$) of about 0.5 microns and wafer thickness repeatability ($1\sigma$) of about 0.05 microns.

Strengths of this technique are high measurement speed, so a large quantity of data can be collected. A limitation is the lack of thermal capability.

***Profilometry.*** Profilometry uses a contact stylus sensor to determine step heights and general surface topography over a wafer. By scanning over a sufficiently large area of the wafer, a map of the wafer shape can be obtained before and after film deposition. The data are fit to determine the change in radius and put into the Stoney equation. Profilers can achieve exceptional performance with approximately 0.01 micron repeatability ($1\sigma$) in vertical resolution of the surface shape.

The main strength of profilometry is its high sensitivity. Limitations are slow measurement speed, the probe tip contacts the sample, no thermal capability, and full wafer data must be "stitched" together.

***Optical Lever Measurements.*** Optical lever systems aim a laser at the surface of a wafer and measure the direction of the reflected beam using a position sensitive light detector. From knowledge of the system geometry, the wafer surface normal and therefore the tangent are measured. Scanning over the wafer surface provides a map of tangent versus position which is fit to determine the change in radius and put into the Stoney equation. Optical systems can determine bow with a repeatability ($1\sigma$) of about 0.5 microns.

Strengths include simplicity, measurement speed, and thermal capability. Limitations are that the laser is diffracted by patterned wafers, and interference effects occur in some films.

## 4.4 Defect Inspection Systems

This section covers theory of operation and equipment design principles, main applications, and strengths and limitations for unpatterned and patterned wafer inspection systems. The section is organized as follows:

- General Theory of Inspection System Operation and Design
  - Optical Imaging
  - Optical Scattering
- Unpatterned Inspection Systems
  - Applications
  - Strengths and Limitations
- Patterned Inspection Systems
  - Applications
  - Strengths and Limitations

**General Theory of Inspection System Operation and Design.** Very generally, an inspection system must be able to detect the presence of the defects on the wafer and identify their spatial locations. Defect detection requires some kind of contrast mechanism to distinguish the defect from its surroundings. Typical contrast mechanisms include those associated with optical imaging (both dark-field and bright-field); optical scattering (dark-field); and electron imaging. In this section we will focus on the optical techniques as these are the most commonly used in monitoring defectivity for IC production today.

In order to discuss the technology of optical inspection, some usage conventions are helpful. On a perfect mirror surface, the light incident at a given angle reflects at the equivalent angle in the plane of incidence to form the *specular* beam (Fig. 6). On a real surface some of this light will be *scattered*: absorbed, diffracted or otherwise directed to an angle outside the specular beam. Particles, scratches, surface roughness, local device topography or interfaces between different materials can cause light to scatter.

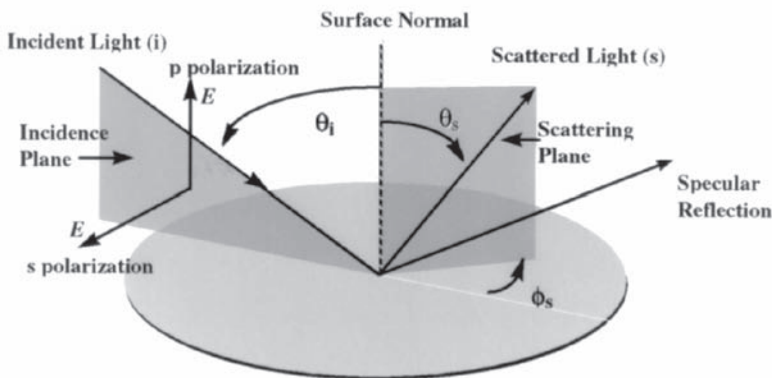


**Figure 6.** Simplified schematic of optical subsystem for optical defect detection. There are three beams of light: the incident beam, the specular beam and a ray representing the scattered light. The plane formed by the wafer surface and the scattered light beam is at an angle $\phi_s$ from the incident plane, which is formed by the wafer surface and the incident beam. The specular beam lies in the incident plane.

***Optical Imaging.*** For optical imaging an area of the surface of the wafer is illuminated uniformly. Features and defects within the illuminated area scatter the light according to their material properties and topography. A series of lenses captures the specular beam (bright-field design) or scattered light (dark-field design), imaging its spatial variation on the wafer surface onto an area detector such as a CCD camera or TDI detector. The information conveyed by the image arises from the differences in the way the defects and features on the surface scatter light. Defects are detected by comparing the digital image of one part of a die with the image from equivalent areas in neighboring dies, and identifying differences.

The resolution of an optical imaging system is determined by the pixel size of the area detector, the spectrum of the light source and photon density of the illuminated area, and the optical contrast between the defect and its surroundings.

***Optical Scattering.*** For optical scattering, a small spot of high photon density is illuminated on the wafer surface. Features and defects within the illuminated spot scatter light according to their material properties and topography. The specular beam is discarded, and the scattered light is collected over a particular solid angle, then focused onto a point detector such as a photomultiplier tube (PMT). In essence, the amount of light scattered by that illuminated area into a given solid angle is recorded. Various signal processing schemes are then employed to determine whether or not a defect is present at the location of the illuminated spot. For example, this signal could be compared with a signal from an equivalent area elsewhere on the wafer. The entire surface of the wafer is sampled by moving the beam across the wafer, or the wafer under the beam, or a combination thereof.

The resolution of an optical scattering inspection system is determined by the ratio of the light scattered by the defect to that scattered by its surroundings. This is in turn determined by the photon density of the illuminated spot, the wavelength and incident polarization of the light source, the solid angle(s) subtended by the collection optics, the polarization collected in the detector, and details of the optical and topographic properties of the defect and its local environment.

Thus the probability of capturing a defect of a particular shape, material and size, residing on a particular film stack and in the presence of a given local device topography varies with many parameters. The specifics of the optical design of the inspection system—in particular the angles of incidence and of collection—influence the capture probability, as does the signal processing technique. Capture probabilities can be predicted rather well through mathematical modeling for spherical particles on bare wafers.[13] For specific defect types on patterned wafers, simple models can be constructed that also produce useful results.[14]

**Unpatterned Wafer Inspection Systems.** Typically dark-field optical scattering is used for detection of particles, scratches and crystal defects of unpatterned wafers. The complexities of the pattern signal are not present, and the cost of the unpatterned wafer is lower than that of the product wafer. For cost-effective inspection, throughput is very important in unpatterned wafer applications.

The original unpatterned wafer inspection systems used a red helium neon laser (633 nm), but in the early 1990s a switch was made to a blue argon ion laser (488 nm) whose shorter wavelength provides increased sensitivity.[15] Unpatterned wafer inspection systems use either a normal-incidence or oblique-incidence design (Fig. 7).

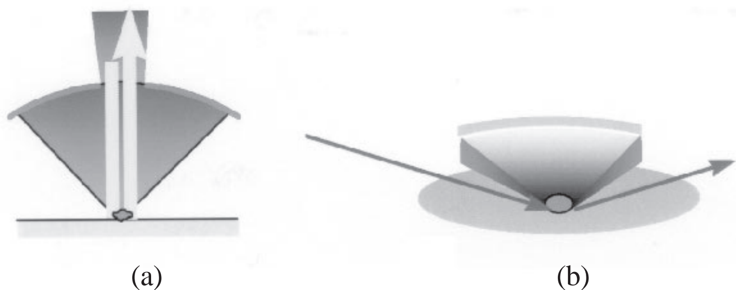

**Figure 7.** (*a*) A normal-incident laser-scattering system avoids the specular beam, but collects a large portion of the light in the hemisphere above the wafer. (*b*) An oblique-incident laser-scattering system avoids the specular beam, but also avoids the higher-angle non-specular light and collects light close to the wafer horizon and to the side of the incident and reflected specular beam.

Many unpatterned inspection systems in use today scan the laser spot in the x-direction while the wafer moves in the y-direction. The scattered light is collected either in a large solid angle near the specular beam (for normal-incidence systems), or to the side of the wafer close to the horizon (for oblique-incidence systems). The beam spot is typically 10s or 100s of micrometers across, and every defect is sampled several times by several sweeps of the laser spot.

Another successful commercial unpatterned inspection system uses a markedly different optical design. For improved sensitivity and uniformity the entire incident and collection optics are held stationary, while the wafer is rotated and translated beneath the optical system (Fig. 8). The laser spot traverses a spiral path to sample the entire wafer surface. The system has two collection channels that together span almost the entire scattering hemisphere. The collection optics are axially symmetric, allowing very uniform defect capture even for defects that scatter light highly directionally,

like scratches. The system also includes a Nomarski differential interference contrast microscope to distinguish concave from convex defects, and to capture large-scale, low-topography defects such as a surface quality problem called "orange peel." This inspection system is described in more detail in Ref. 16, and Nomarski microscopy is discussed in Ref. 17.

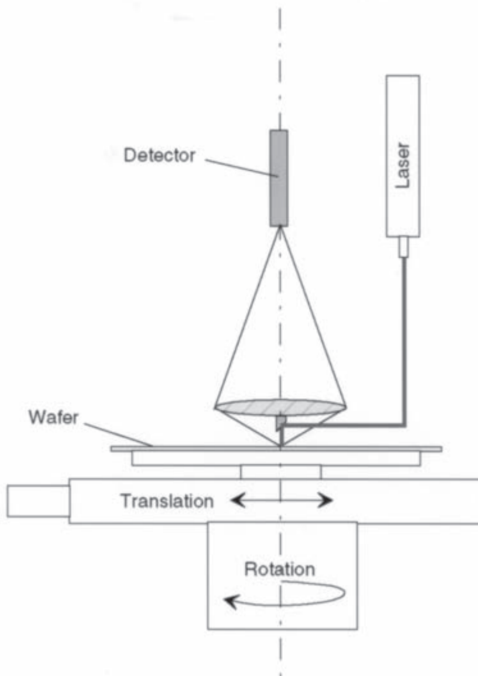


**Figure 8.** Schematic of unpatterned wafer inspection system showing dynamic wafer stage, and rotationally symmetric (static) collection optics.

During signal processing the scatter arising from surface roughness or haze is separated from the defect scatter. The resulting information is typically divided into three categories: haze, point defects, and large-area scattering events like scratches. The values reported for the defects include their coordinates, scattering cross-section ($\mu m^2$) and/or "diameter" (μm).[13] The "diameter" values are calibrated from the scattering cross-sections of populations of polystyrene latex (PSL) spheres of known size, deposited on the film of interest.

***Applications.*** Unpatterned inspection systems are used for the main applications shown in Table 3.

**Table 3.** Applications of Unpatterned Inspection Systems

| Application | Defect Types | Wafer | Goal |
|---|---|---|---|
| Silicon wafer manufacturing | Particles, pits, scratches, crystal defects, haze | Bare wafers | Increase quality<br>Increase yield<br>Monitor yield |
| IC manufacturing | | | |
| Incoming inspection | Same as above | Bare wafers | Quality control |
| Equipment qualification | Particles | Bare wafers | Ensure tool is not adding defects, is ready for production |
| Equipment monitoring | Particles | Bare wafers | Monitor tool for change in added defects |
| Process monitoring | Particles; scratches (CMP area) | Blanket films | One monitor wafer in cassette with product wafers tracks defectivity of process |

Unpatterned inspection systems are used heavily by silicon manufacturers and IC manufacturers for inspection of bare silicon and blanket films. Silicon manufacturers use the systems to measure the number of particles, pits, scratches, and crystal defects[18,19] and to characterize haze on the wafers.[20][21] In IC manufacturing they are typically used to measure PWP—Particles per Wafer Pass—to characterize particles added by process or metrology tools during wafer processing. From this measurement a tool is qualified for production use and/or monitored using SPC charts to understand if the tool is degrading and causing any defect issues. For example, a process tool may be studied with PWP tests to understand how often the chamber needs to be cleaned, and then monitored with PWP tests for any other abnormal excursions.

***Strengths and Limitations.*** See Table 4 for some of the strengths and limitations of defect detection systems.

**Patterned Wafer Inspection Systems.** Patterned-wafer inspection systems may use bright-or dark-field imaging, or dark-field scattering, or any combination of these as their fundamental defect detection technology. The challenges specific to patterned-wafer defect inspection come directly from the presence of pattern near the defects, and from the fact that the types of possible defects are extended to include defects in the pattern itself—bridges, opens, missing vias, etc. Several different system designs exist

among successful commercial inspection systems; these can each be optimized for sensitivity and throughput using several configurable system parameters. Capture probability for a given defect type on a given layer for a given IC product will vary according to the configuration of the system and its overall design. Determination of the optimum inspection system to detect a range of key defects for a given segment of the process is best determined experimentally.

**Table 4.** Strengths and Limitations of Defect Detention Systems for Unpatterned Wafers

| Unpatterned Wafer Inspection Systems | |
|---|---|
| Strengths | Limitations |
| • Can detect defects as small as 80 nm on bare silicon wafers<br>• Excellent sensitivity to particles on smooth and rough blanket films<br>• Can detect crystal defects<br>• Can measure haze/surface roughness<br>• Low cost per inspection<br>• Automated<br>• High throughput | • Unpatterned wafers only<br>• Defect must have some type of light-scattering signature to be detected: topography, or change in material properties<br>• Sizing calibration is based on known polystyrene latex spheres |

Bright-field imaging systems work by flood-illuminating an area of the wafer, then using an objective lens to construct an optical image of that area from the specular beam reflecting off the surface. The image is captured by a digital camera, and that image is compared with another image from a similar area on the wafer. In periodic areas such as memory cells the compared area may be within the same memory cell; for non-periodic areas an equivalent area from a neighboring die is used. Differences between images become candidates for identification as defects.

Dark-field imaging is a similar technique, but instead of utilizing information from the specular beam, the detector is placed away from the specular beam to intercept a fraction of the scattered light. Although both dark-field imaging and dark-field scattering use scattered light to detect defects, dark-field imaging differs in that it preserves the spatial relationships among features illuminated within the spot. Both dark-field techniques should provide similar defect capture probabilities, if angles of incidence and collection (and other system parameters) are comparable.

Dark-field scattering technology for patterned wafer inspection is similar in principle to unpatterned wafer inspection technology except that the scattering signal from the pattern must be managed. In the first patterned wafer inspection systems all signals having a period similar to that of the die spacing were discarded, while all aperiodic signals became candidates for identification as defects. The latest dark-field scattering inspection systems retain all signals above a threshold, then employ a die-to-die comparison algorithm similar to that described above for imaging systems.[22]

A critical requirement of all patterned wafer inspection systems is fast and reliable alignment of the wafer to the scan axes. This is necessary for proper implementation of the signal processing algorithms, and this requirement has driven the use of highly precise stages and sophisticated alignment algorithms in these systems.

***Applications.*** Patterned wafer inspection systems were introduced in the 1980s to drive yield enhancement by providing a direct look at defect densities on production wafers. These systems replaced the long-standing tradition of inspection by operators using optical microscopes. Today's inspection systems are very automated and offer higher throughput than an operator, more repeatable and objective results, and significantly higher detection sensitivity and defect capture.

Patterned wafer inspection systems are used to inspect wafers for defects at any level in the IC manufacturing process. Two main applications of these systems have been discussed previously in this chapter: in-line monitoring and yield learning. Patterned wafer inspection systems are usually integrated closely with data analysis systems, review stations, and automatic defect classification (ADC) to provide an entire system for identifying and eliminating yield-limiting defects, and to monitor the process line to catch defect excursions and drive continuous improvement.

Increasingly, these systems are being used for process equipment monitoring with patterned production wafers. The trend towards reducing the cost of monitor wafers in the fab has led to increased dependence on

production wafer defect data to help determine the defect contribution of process equipment.

***Strengths and Limitations.*** See Table 5 for some of the strengths and limitations of defect detection systems.

**Table 5.** Strengths and Limitations of Defect Detection Systems for Patterned Wafers

| Optical Patterned Wafer Inspection Systems | |
|---|---|
| Strengths | Limitations |
| • Can detect defects as small as 0.1 μm on front-end, patterned layers, on product wafers<br>• Techniques exist to reduce noise effects of film nonuniformity and process variation<br>• Automated<br>• Integrated with defect review and classification systems, defect data analysis systems | • Defect must have some type of light-scattering signature to be detected: topography, or change in material properties<br>• Lower throughput than unpatterned inspection systems |

## 4.5 Automatic Defect Classification

The main goal of Automatic Defect Classification is to reduce the number of defects that require manual review and classification. ADC incorporates several levels of operation to achieve this. The first level involves the use of clustering algorithms that group together defects with certain spatial signatures, such as scratches. These cluster algorithms are normally also available on the inspection system, providing a first-pass defect classification that happens while the wafer is scanned.

After clusters have been removed a smaller group of defects is left behind to classify. This group can be reduced further by using a data analysis system to compare the current defect map with maps from previous layers, and selecting only defects from the current layer. Next, defects can be removed from the remaining group by considering characteristics stored during inspection, such as defect size. After the data set has been significantly reduced by these techniques, the remaining defects are reviewed and classified automatically or manually, comparing the characteristics of the reviewed image of the defect to information in a database. Manual classification involves having a trained operator compare the microscope image to example images in a defect scrapbook. The remainder of this section describes how this part of the review and classification process can be done automatically, via high-resolution automatic defect classification.

The database used for high-resolution ADC is built by the user and requires multiple example images of each type of defect. Typically 5 to 20 examples of each defect type are needed to construct the database. The system measures the value of each of a number of features describing the defect. For a given defect category, each feature spans a particular range. The set of feature ranges distinguishes one defect category from another. These category features are used as a reference for high-resolution automatic classification of new defects.

After the system has been trained, new defects are classified as follows:

> If ADC is on board the inspection system the system already has the wafer aligned and in the system. Otherwise the wafer must be loaded and automatically aligned. Using the coordinates determined by the inspection system, the ADC system drives to a defect's position and re-detects the defect. The re-detection algorithms are similar to the die-to-die processing discussed previously. Depending on the type of device being inspected, the ADC system will drive to another location within the die that has identical pattern (for example, to another location within the memory array for a DRAM), or will drive to one or two adjacent die to compare the corresponding image(s) and subtract the images to determine the defect image. After the defect has been re-detected, the system compares the values of the features of the defect image to those stored in the database.

The final results include the best match of that defect to a known category, and a number indicating how good the match is between the defect's particular characteristics and that category's stored characteristics. Some systems will also show the second-best match for the defect being classified.

**Applications.** Early ADC systems in production-level fab focused on a few specific types of layers in the front-end of the process. Continuing developments in ADC technology have opened up the entire process for automatic defect classification. There are several different types of review stations available with various illumination sources (e.g., optical microscopes, confocal laser-scanning microscopes, scanning electron microscopes), and ADC is available with many of these. ADC with white light and with confocal laser-scanning review stations is being used currently in fabs for classification of defects in both the front end and back end of the process (back end being defined here as all process steps used for forming the metal interconnects that wire together all of the transistors formed in front end processing). Future technology advancements in ADC will see the inclusion of ADC with scanning electron microscopes (SEMs). This will be particularly important as the linewidths of devices decrease, and the identification of defects smaller than 0.2 micron becomes necessary on a regular basis. For further reading on automatic defect classification, please see Ref. 23.

**Strengths and Limitations.** Automatic defect classification reduces the amount of time and resources necessary to do in-line monitoring of the IC process. ADC is available integrated directly with the inspection tool, or separated from the inspection tool in an off-line review station. The former is useful because it minimizes the overall time between when the wafer is loaded, and when the defects are classified. The latter is useful because the inspection tool's time is not occupied with ADC activities (both creating a database and doing actual ADC), and it can therefore remain dedicated to wafer inspection. (See Table 6.)

ADC using a white-light source provides excellent results on front-end layers. Some challenges arise in the back-end of the process when the topography of the surface of the device is complicated by the presence of many etched layers. In this case consistent autofocus on the top surface can be difficult with a white-light microscope, and this can affect ADC by lowering the rate of successful defect re-detection. Fortunately, ADC results using confocal laser scanning have demonstrated improvements in re-detection rates on back-end layers. These systems have a restricted depth of focus with variable height positioning that can be used to generate a digitized 3-D surface image for automatic defect classification.[24]

**Table 6.** Strengths and Limitations of ADC Systems

| Automatic Defect Classification Systems | |
|---|---|
| Strengths | Limitations |
| • ADC is faster, more repeatable and more accurate than classification by operators: faster time and results<br>• White light or laser-confocal ADC can be used to reduce number of defects needing slower SEM review<br>• Flexibility in platform: available off-line from, or integrated with, the inspection system | • Images of typical defects in each class need to be acquired for setup<br>• Differing defect types must have different appearance to be properly classified |

## 4.6 Defect Data Analysis Systems

Data analysis became a more critical part of the defect reduction process with the adoption of automated defect inspection systems, particularly patterned wafer inspection systems. Patterned inspectors resulted in a dramatic increase in the amount of defect data generated for analysis. Defect data analysis systems are now networked multi-user systems that provide access to and analysis of inspection data throughout the fab, and incorporate and correlate defect data with other metrology and parametric measurements such as electrical test results.

The data analysis systems function in several ways:

***Defect data analysis systems manage the information flow and maintain a historical database of inspection, review, and metrology and parametric data throughout the fab.*** Data analysis systems usually have a large amount of memory allocated for data coming from all types of inspection systems (data include defect density, size, coordinates, etc.) and from review stations (i.e., defect images and classification information). Typically this flow of information between the tools and the analysis system is automated and requires little or no operator intervention.

***Defect data analysis systems provide basic SPC functionality and real-time feedback for in-line monitoring of the process.*** The systems provide basic graphical analysis such as wafer maps and trend charts. Since the flow of data into the system is automated, the system can be programmed to alert an operator or engineer automatically, and shut down the process equipment, if the density of a given defect type at a particular inspection point in the process exceeds set control limits.

***Defect data analysis systems provide capabilities for correlating defect data to yield data.*** Clustering algorithms group defects based on their spatial relationships on the wafer. Identification of these clusters helps track excursions in defect density—and yield—more intelligently. Clustering algorithms may also help identify the source of the defects, as some process equipment may create defects having a distinct spatial signature. Partitioning analysis helps determine at what layer the defects first arose. This information helps significantly to pinpoint the source of defects. Finally, the capability of correlation of defect information with electrical test sort maps establishes which defect types are yield-limiting.

The output of the data analysis system can be in a variety of formats: wafer maps, Pareto charts or histograms, or tabular reports. These systems are also able to output new wafer map review files with only certain defects included. This may be useful, for example, for reviewing only defects added at a given process layer.

For further reading on defect data analysis systems, see Ref. 25.

## GLOSSARY

| | |
|---|---|
| ADC | Automatic Defect Classification, a means of categorizing detected events by comparing their digital optical images with reference images. |
| AFM | Atomic Force Microscope, an instrument derived from a Scanning Tunneling Microscope and related to a stylus profilometer, used to form 3-D high resolution topographic images of solid surfaces. |
| ASIC | Application Specific Integrated Circuit. |
| Back end | See BEOL. |
| BCR | Bar Code Reader, used for wafer identification and tracking. |

| | |
|---|---|
| BEOL | Back End Of Line; the process steps used for forming the metal interconnects that wire together the transistors formed in front end processing. |
| Bright-field | Describes a technique based on collection of the specularly reflected light from the sample. |
| CCD | Charge Coupled Device; in this context describing a type of digital camera. |
| CD | Critical Dimension, or smallest linewidth of a conductive line on an IC. |
| CMP | Chemical-Mechanical Polishing, a global planarization technique. |
| COO | Cost Of Ownership, a metric used to evaluate semiconductor equipment. |
| C-V | Capacitance-Voltage. |
| CVD | Chemical Vapor Deposition, a technique commonly used to deposit dielectric layers. |
| Dark-field | Describes a technique based on collection of the non-specularly reflected (scattered) light from the sample. |
| Defectivity | The quality of having defects; the number of defects on the wafer. |
| DRAM | Dynamic Random Access Memory, a type of semiconductor memory. |
| Electromigration | The process resulting in current-induced open circuit failure in metal interconnect lines. |
| FTIR | Fourier Transform InfraRed spectroscopy, used for chemical compositional analysis. |
| GEM | Generic Equipment Model, a communications standard used for factory automation (newer than SECS). |
| IC | Integrated Circuit. |
| In-line | Relating to measurements that occur in a processing tool, outside of the process chamber. |
| *In situ* | Relating to measurements that occur within a process chamber. |

| | |
|---|---|
| Junction | The point at which the conductivity changes from p-type to n-type or vice versa. |
| MOCVD | Metal-Organic CVD, used for depositing certain conductive layers. |
| OCR | Optical Character Recognition, used for wafer identification and tracking. |
| OEE | Overall Equipment Effectiveness, a metric used to evaluate semiconductor equipment (newer than COO). |
| Off-line | Relating to measurements that occur on a stand-alone metrology system in the manufacturing area. |
| Nomarski | Differential interference contrast microscope, a technique for detecting the phase difference between two adjacent points on the sample. This method uses a birefringent crystal, and polarized light, to separate the incident light into two adjacent beams, and determines the phase difference between the beams through interference. |
| Pareto analysis | A list of items contributing to a problem communicating the order of their importance. |
| PMT | Photo Multiplier Tube, a type of light detector chosen for its fast response, that quantifies the amount of light striking its active area per unit time. |
| PSL | PolyStyrene Latex sphere, a standard used to characterize the defect capture performance of defect inspection systems. |
| PVD | Physical Vapor Deposition, commonly used to form metal interconnects. |
| RC | Resistive-Capacitive, a time delay constant that affects chip operation speed. |
| Recipe | An electronic file of system parameter values used to control semiconductor processing or metrology equipment. |
| RI | Refractive Index, the ratio of speed of light in a vacuum to speed of light in a material. |

| | |
|---|---|
| $R_p$, $R_s$ | The Fresnel reflection coefficients, *p* and *s* polarized. |
| RTDC | Real Time Defect Classification; a first pass defect classification that uses only information collected during defect inspection, such as intensity, size and spatial distribution of collections of defects *s* and *p* polarization, the perpendicular and parallel components (respectively) of the polarization vector. |
| SECS | Semiconductor Equipment Communications Standard, used for factory automation. |
| SEM | Scanning Electron Microscope; uses an electron beam to produce very highly magnified images. Used for surface viewing and cross sectional analysis of device dimensions. |
| Slurry | An abrasive suspension of hard particles in a viscous chemical solution used in chemical-mechanical polishing. |
| SIMS | Secondary Ion Mass Spectrometry, used for characterizing dopant and impurity distribution with depth profiles. |
| Solid angle | The 3-dimensional equivalent of angle, often defined by azimuth and elevation. |
| SPC | Statistical Process Control, a method of tracking the variations in process parameters to help identify out of control situations. |
| SRP | Spreading Resistance Probe, used for characterizing dopant distribution with depth profiles. |
| Stoichiometry | The chemical combination of a material composed of other materials. |
| TDI | Time Delay Integration, in this context describing a type of camera. |
| Yield | The percentage of wafers or die produced in an operation or process that conform to specifications. |

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# 7

# Contamination Control, Defect Detection, and Yield Enhancement in Gigabit Manufacturing

*Suresh Bhat* and Krishna Seshan*

## 1.0 INTRODUCTION

With the prevalence of ultra-large-scale-integrated circuits (ULSICs), conventional wisdom about contamination control needs to be questioned and usual practices need to be reassessed. Profound change in the industry is impacting fundamental areas in process and equipment design, wafer handling, wafer environments, and metrology. In the past, much emphasis was placed on the cleanroom environment—state-of-the-art ULSI fabrication facilities are usually Class 1 or better. Further reduction in airborne contamination, especially particulate, is not appearing to be cost-effective. Today's limiters of higher yields are the process equipment and the processes themselves where the probability of contaminating the wafer is much higher than from the Class 1 cleanroom environment. Every process step is a source of contamination and modern ULSI processes have well over 300 steps.

*(1957–2001)

Integrated circuit manufacturing requires the extensive use of thin films of dielectric and conducting materials. These films are subsequently patterned using state-of-the-art lithography and etching techniques to realize the critical feature sizes for state-of-the-art CMOS, bipolar, and BiCMOS devices. Contamination control during processing is paramount to obtaining yielding devices in order to make device manufacturing economical. This is especially true for very large scale (VLSI) and ultra large scale integrated circuits (ULSI).

The yield and hence the cost of manufacturing these devices is directly dependent on the density of defects in the thin films. Defects are generated by the presence or inadvertent introduction of contamination into the thin film deposition process environment. Particle formation during thin film deposition is a phenomenon that is known to lead to defects in the thin films. The detection and control of particles that cause "killer defects" during thin film processing is the biggest challenge in manufacturing processes where yield is important.

Since the deposition of most thin films for integrated circuit devices, magnetic and optical media, display devices (such as flat panel liquid crystal displays), and photovoltaic devices is usually performed in subatmospheric reactors, the reactors themselves are a major source of particle contamination. Trace levels of atomic and molecular contaminants such as oxygen and moisture in the reactors are also known to cause film defects leading to failure of the devices.

While the detailed discussion of the sources of such contamination and its impact on the devices manufactured is beyond the scope of this chapter, methods to detect, analyze, and control microcontamination originating in the process reactors are discussed with most of the emphasis on semiconductor device manufacturing. Contamination control issues in related technologies such as display device manufacturing, and magnetic and optical storage media are discussed very briefly.

The final section of this chapter discusses traditional as well as advanced surface preparation techniques that reduce or eliminate contamination on the substrate prior to thin film deposition. Residual contamination on the substrate will be decorated and enlarged by the film that is subsequently deposited. The substrate cleaning techniques include those using the traditional aqueous chemicals as well as dry (gas-phase), cryogenic as well as plasma cleaning.

**Figure 1.** Many different and diverse fields are included in the term "contamination and contamination control," as shown in this figure. *(After Tolliver, Ref. 11.)*

## 2.0 CONTAMINATION AND DEFECT GOALS FOR ULSI DEVICES

Several models are being used by the industry used to predict the yield of integrated circuits. One of the earliest such models applicable to IC yield is based on a Poisson and binomial distribution.[1][2] These are described by Eqs. (1) and (2), respectively,

Eq. (1) $$Y = \exp(-A \times D_0)$$

Eq. (2) $$Y = 1/(1 + A \times P_f \times D_0)$$

where:

$Y$ = Defect-limited yield

$A$ = Device Area

$P_f$ = Probability of fault

$D_0$ = Defect density

Over the years, the yield models have been enhanced and experimentally verified, some with actual manufacturing data.[3] Regardless of the model used for yield prediction, contamination-induced defects historically have and will always play a major role in determining actual IC yields.

In 1992, the Semiconductor Industry Association (SIA) developed a trend line and a roadmap with goals for defects in ULSI manufacturing, with the help of SEMATECH, the U.S. industry-government consortium (Table 1). Individual companies and consortiums in Japan and Europe have developed their own or similar roadmaps, and Table 1 may only serve to exemplify the trends rather than the actual defect levels required for future ULSI manufacturing.

Table 1 lists the key parameters for future ULSI manufactured devices and the projected microcontamination requirements to keep defects under control for cost-effectiveness. Substantial effort will be required to achieve electrical defect densities shown in Table 1.

Rapid yield learning will be governed by the effective use of wafer-level defect-detection tools. More inline defect inspections will need to be performed as well as capabilities for rapid review and classification. Optical defect-detection tools are reaching their limit, and 0.08 μm and smaller defects will require use of scanning electron microscopy (SEM).

Reducing contamination in processing equipment will be key to achieving the goals stated in Table 1. Reducing the contamination levels in process fluids and fluid delivery systems, as well as providing clean wafer environments for transporting and storing the wafers, will be required. Extensive use of numerical modeling will help equipment vendors understand sources of contamination and design contamination-free features into the tools.

In situ contamination sensors will be the first line of defense against contamination-induced defect excursions. Wafer-level inspections will be uneconomical in manufacturing, especially as wafer sizes increase from 200 mm to 300 mm diameter. Low-cost contamination sensors interfaced to the process tool via computer control will be required.

Contamination can be broadly classified into optically visible (particulate) and optically invisible contamination. The latter includes ionic (Na, K, Li) as well as heavy metal contamination (Fe, Cu, Cr, etc.). Trace amounts of moisture, oxygen, and hydrocarbons are another source of contamination especially in vacuum processing systems.

**Table 1.** SIA Roadmap

| Year of manufacturing | 1995 | 1998 | 2001 | 2004 | 2007 | 2010 |
|---|---|---|---|---|---|---|
| Minimum feature size | 0.35 μm | 0.25 μm | 0.18 μm | 0.13 μm | 0.1 μm | 0.07 μm |
| DRAM density bits/chip | 64MB | 256MB | 1GB | 4GB | 16GB | 64GB |
| Wafer diameter (cm) | 200 | 200 | 300 | 300 | 400 | 400 |
| DRAM chip size ($mm^2$) | 190 | 280 | 420 | 640 | 960 | 1400 |
| DRAM defects/$m^2$ | 560 | 375 | 250 | 165 | 110 | 75 |
| Microprocessor chip size ($mm^2$) | 250 | 300 | 360 | 430 | 520 | 620 |
| Microprocessor defects/$m^2$ | 425 | 350 | 300 | 245 | 200 | 170 |
| In situ sensor requirements | | | | | | |
| Particles in vacuum, corrosives (μm) | 0.11 | 0.08 | 0.06 | 0.04 | 0.03 | 0.02 |
| Moisture in vacuum, corrosives (ppb) | 10 | 1 | 0.1 | T.B.D. | T.B.D | T.B.D |
| Particles in liquids (μm) | 0.11 | 0.08 | 0.06 | 0.04 | 0.03 | 0.02 |
| Fluid Purity | | | | | | |
| Key impurity levels bulk gases (ppb) | 0.5–1 | 0.1–1 | 0.1–1 | 0.1–1 | 0.01–0.1 | 0.01–0.1 |
| Particles/$ft^3$ spec. gases >0.03 μm | 1–10 | 1–10 | <1 | <1 | T.B.D | T.B.D |
| Key impurity levels spec. gases (ppb) | 0.1–1 | 0.001–0.1 | 0.001–0.01 | 0.001–0.01 | T.B.D | T.B.D |
| Particles/$ft^3$ spec. gases >0.02 μm | 1–10 | 1–10 | <1 | <1 | T.B.D | T.B.D |
| Key metallic impurities liquids (ppb) | <0.1 | <0.05 | <0.01 | <0.01 | T.B.D | T.B.D |
| Particles/ml >0.1 μm (liquids) | <100 | <10 | <10 | <1 | <1 | T.B.D |

Source: "National technology roadmap for semiconductors," Semiconductor Industry Association.

## 3.0 SOURCES OF PARTICLES

In order to control particle contamination levels during processing, the fundamental nature of particle sources, their mechanism of generation and growth kinetics as well as transport must be understood. Research in this subject is in its infancy and models are generally incomplete, sometimes with little supporting experimental data and a few contradictions. Nevertheless, it is a field that is rapidly gaining visibility in the quest to control contamination levels.

Particles may be generated by heterogeneous as well as homogeneous means. With reference to thin film processing, both mechanisms may coexist in the same processing tool. The most frequently cited cause of heterogeneous particle formation is physical in nature and is a result of buildup of reaction by-products. In addition, the film growth on reactor walls "releases" particles or nucleation sites for further particle growth on the substrate. These particles typically manifest themselves as peeling films on the reactor walls, flakes from gas showerheads, and polymers from plasma deposition and etching chemistries.

Homogeneous particles are formed under the influence of the chemical reaction of the process, the process conditions such as pressure and RF power, and impurities in the process fluids. A good example of homogeneous particle formation happens during pump down of a vacuum chamber. When a vacuum chamber is pumped down rapidly, especially from atmosphere, there is also a complex change in temperature leading to water vapor condensation that eventually leads to particulate formation. The particle formation in this manner is believed to be due to a liquid-phase chemical reaction of $SO_2$ and $H_2O_2$ to form nonvolatile residue particles of $H_2SO_4$. Liu, in Ref. 4, hypothesizes the above mechanism in the following manner: Homogeneous nucleation converts water vapor to water droplets due to the cooling of the residual water vapor gases in the chamber by adiabatic expansion. Once this occurs, trace gases get adsorbed in the water droplets forming a chemical reaction. The components of this reaction include $SO_2$ and $H_2O_2$ to form aerosol particles of $H_2SO_4$ residue after the water vapor evaporates. The trace contaminants are believed to be air pollution-related.

Another relatively minor source of contamination can be the gas delivery system to the thin film processing tool. Ultra-clean gas panels and gas piping are now required for ULSI manufacturing. The contamination levels in the gas delivery system not only affect the thin film process but also, eventually, the lifetime of the delivery system itself. Specific

requirements for the delivery system and individual components include leak-free fittings, low particles and outgassing, minimum dead-spaces and passivated surfaces wetted by the process fluids. For example, piping is usually electropolished 316L stainless steel with oxygen passivation to reduce outgassing. In a silane delivery system, minute air leaks or trace moisture in the gas piping can cause particulate formation inside the piping that may lead to eventual clogging of components such as mass-flow controllers in the gas delivery system, in addition to process contamination.

It is useful to highlight the factors that impact particle transport within a processing tool. The physical forces that impact particle transport include those due to gravity, viscosity, thermophoresis, and photophoresis, in addition to those in plasma environments, with and without the presence of magnetic fields. Another interesting influence that impacts particle formation as well as transport is mechanical vibration. Sources of vibration in thin film processing include vacuum pumps, wafer chucks and clamping systems, isolation valves, and robotic arms that transfer the substrates from chamber to chamber.

When thin film deposition is done at subatmospheric pressures, the low drag force in a vacuum environment can lead to relatively long particle transport distances compared to conditions when the deposition occurs at atmospheric pressure.

Particles generated in a plasma deposition chamber are often transported under weak electromagnetic fields, depending upon the geometry of the plasma chamber. Often the particles are concentrated by factors such as non-uniformities in the electric field. Experimental evidence suggests that particles remain suspended in the plasma for the duration of the plasma. When this occurs directly over the substrate on which the film is to be deposited, the particle will most likely contaminate the substrate when the plasma turns off.

## 4.0 CONTAMINATION AND DEFECT DETECTION: TOOLS OF THE TRADE

### 4.1 Introduction

An array of tools and techniques are available for detection of contamination and defects, and for measuring yield-loss as a result of the two. While real-time monitoring techniques are attractive and more cost-effective, much work needs to be done to make them applicable to actual

manufacturing tools. It may be noted that no single tool would be adequate. A more complete strategy for detecting and controlling contamination in thin film deposition may require a combination of tools described below to be effective. Figure 2 outlines a few such possibilities.

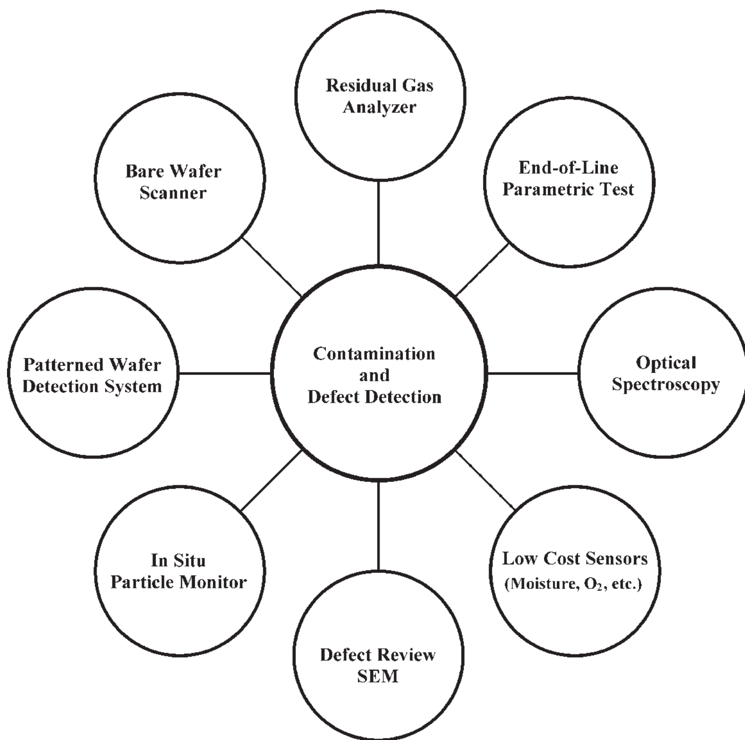



**Figure 2.** Array of tools presently used for detection of contamination.

One of the earliest techniques used to detect and quantify substrate surface contamination and defects, as well as to automate their detection, employed light-scattering techniques. Defects detected in IC wafers include surface particles, blemishes such as haze and surface pits, and crystal defects such as stacking faults and slip lines. Modern instruments are capable of detecting some or all of such defects on bare (unpatterned) substrates, on substrates that have various thin films, and on patterned device wafers. The capabilities and limitations of these techniques are briefly discussed below.

## 4.2 Non-Patterned (Bare) Wafer Surface Defect Detection

The instrumentation generally used to detect surface contamination on substrates consists of a helium-neon laser and photomultiplier or photodiode-based detector. For smooth specular substrates, the laser beam shines at normal incidence for optimum response to scattering of the incident light by surface particles and substrate surface defects (Fig. 3). The detector, which is placed normal or nearly normal to the substrate, collects the scattered light over a large solid angle around the incident beam. The incident beam scans the substrate as the wafer is translated across the beam. The resultant voltage or photocurrent in the detector is proportional to the particle size or scattering cross-section.

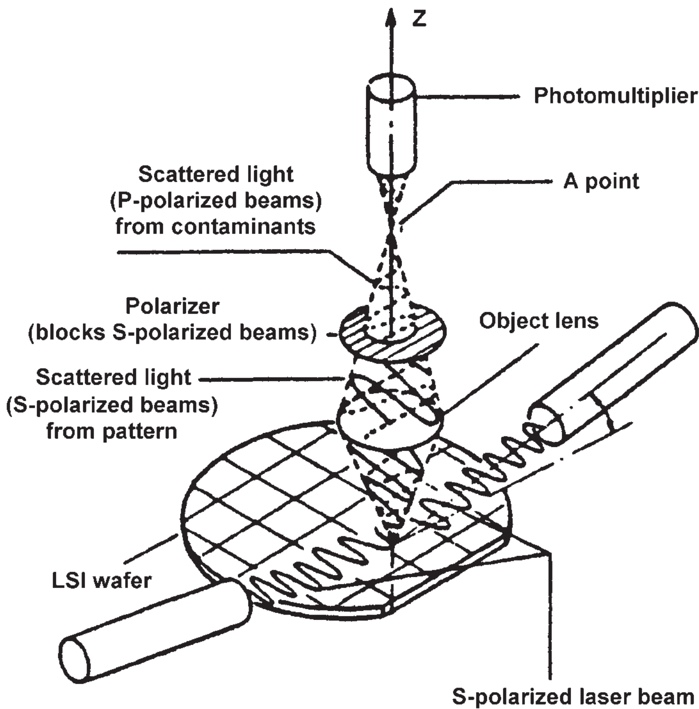



**Figure 3.** Diagram showing how polarized light is used for defect detection. *(From Tolliver, Ref. 11.)*

Light scattering from a particle or surface is determined by the local electromagnetic field, the refractive indices of the particle and surface, and the wavelength of incident light. To simplify the complex light scattering relationships, a classical "Raleigh approximation" is often used, and at the limit of small diameters, the power scattered ($P_s$) by a particle of diameter $a$, illuminated by light of wavelength $\lambda$, can be expressed by Eq. (3).

Eq. (3) $$P_s = k \times (m^2\text{-}1)^2 \times a^6/\lambda^4 \times E^2$$

where $E$ is the local electric field, and $m$ is the (complex) refractive index of the particle relative to the surrounding medium.

The scattered power is a strong function of the particle diameter, the relative index of refraction, and the wavelength of incident light. This approximation is only valid for very small particles ($a/\lambda << 1$). For larger particles, it is common to break the particle volume into smaller volume elements using the coupled dipole method.

On specular substrates, modern instruments can detect particles <0.1 μm in diameter. In practice, there are several limitations to the use of substrate-surface contamination monitoring in thin film deposition equipment. In ULSI manufacturing, a bare Si wafer, premeasured for surface contamination, is cycled through the thin film deposition equipment without an actual deposition occurring. The same wafer is then post-measured and the net particles added or particles-per-wafer-pass (pwp) are measured and their distribution is binned by size. Since this technique only partially mimics the actual deposition (i.e., no deposition occurs), this pwp technique is rather misleading. It is known that the majority of particle deposition occurs during the actual thin film deposition process. Examples of process generated particle formation include the following:

1. Reaction of $SiH_4$ with trace residual moisture or oxygen to cause $SiO_2$ particles during Si CVD.
2. Reaction of $WF_6$ with trace moisture or oxygen to cause $W_xO_y$ particles during W CVD.

In either case, the particle formation may be considered reaction-induced. To assess particle contribution on substrates with the thin film deposited or on rough surfaces, the above pwp technique may still be used but with a significantly modified detection scheme and equipment.

***Future Directions.*** Current generation bare wafer scanners are already stretched to the limits of their capabilities as the laser-based particle detection sensitivity approaches sub-0.1 μm, the minimum particle size that can cause device yield loss in today's devices. Future generation machines must be capable of detecting smaller particles (less than 0.05 μm) at a minimum, with 100% capture rate on a bare Si surface.

Substrate surface microroughness, fine particles, and haze will play a major role in determining the absolute minimum particle size that can be captured by such an instrument. Crystal-originated pits (COPs) will also play a major role in interfering with the minimum detection size because they are indistinguishable from fine particles. Hence the instrument of the future must have capabilities that can discriminate between such varied surface phenomena without having to resort to other independent inspection systems such as scanning electron microscopes (SEMs). In the not-too-distant future, automatic substrate surface inspection stations may even be linked with thin film deposition tools to provide real-time feedback on thin-film induced contamination.

### 4.3 Patterned Wafer Surface Defect Detection

The detection of defects on patterned wafers is quite complex because of the topography created by areas of patterned metal, oxide and resist. The reflectivity and the cleanliness of the wafer can vary greatly and can change during inspection. This is particularly true during a chemical-mechanical polishing (CMP) sequence where, say, a wafer with a coppery appearance gets polished down to a sparse field of copper interconnect lines.

In general, most of the inspection tools are based in the cleanrooms, segregated by the areas where use occurs, and optimized for that area. Since critical dimension (CD) measurement has to occur at all the lithography steps, CD inspection and "CD-SEM" tools have to be dedicated in the lithography areas.

Non-vacuum based patterned wafer inspection tools are based on optical microscopes using polarized or bright field or dark field illumination. Figure 3 is a general diagram showing the principles of using polarized light to illuminate a patterned wafer. The reflected light is detected using standard detectors. The image has to be processed by a computer where correlation of the image with the X,Y coordinates occurs.

Since wafers have grown in size from 100 mm to 200 mm, the cost of detection equipment is now in the millions of dollars. The diagram in Fig. 4 shows the elements of the computer based image comparison methods that are now available with modern wafer detection tools.

Modern automated wafer inspection tools can work in the range of 1 µm to 100 µm and, depending on the magnification, can take as little as six minutes or up to one hour per wafer—depending on the detail of the information required.

Vacuum based inspection—based on scanning electron microscopes—take additional time to pump down and their contaminating influences have to be carefully considered.

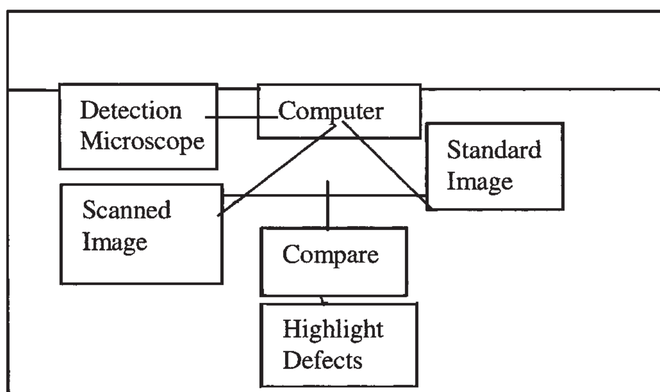



**Figure 4.** Basis of computer based comparator systems.

**Future Challenges for Patterned Wafer Detection.** As processing of wafers becomes more complex requiring many more mask layers, the catalog of defects becomes unmanageably large. Often the challenge is not to find *all* the defects, but only the "killer" defects (see Fig. 5). Further discussion shows that a "defect free" wafer is only a hypothetical possibility.

This problem becomes so complex that many companies are now switching to electrical circuit based defect detection. This is discussed in detail at the end of the chapter.

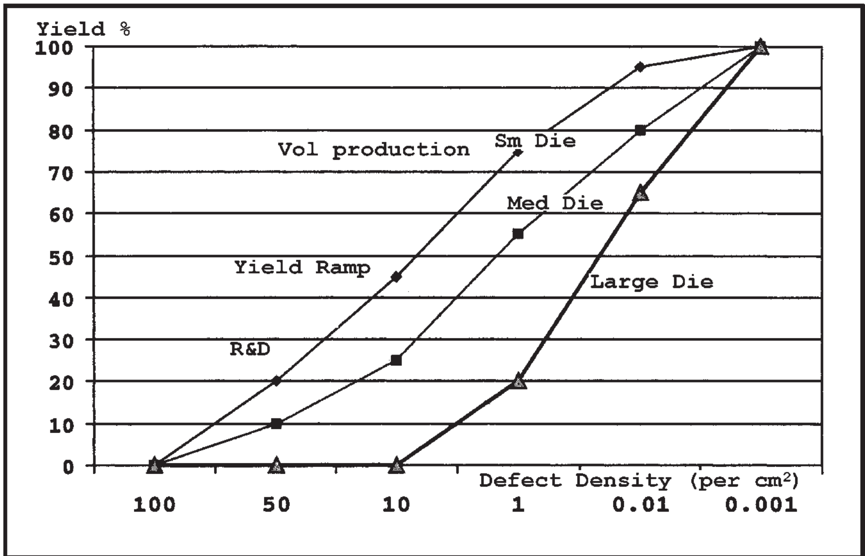



**Figure 5.** Graph shows how defect density and die size vary over different stages of maturity of the process. As systematic defects are eliminated, random particles dominate the yield loss processes.

## 5.0 ADVANCED TECHNIQUES FOR TRACE CONTAMINATION MONITORING

### 5.1 Introduction

As the state-of-the-art in ULSI manufacturing advances, sensors that measure particles in real-time will be required to detect and contain trace contamination excursions inside the wafer process chamber as well as wafer transport, buffer, and input-output areas. Most thin film deposition equipment operates under subatmospheric conditions, often under ultrahigh vacuum. A need to control pressure transients, air-leaks, etc., arises since these events are capable of causing particles directly or indirectly by reacting with the process gases. Typically these sensors are laser- and photodiode-based; they detect particles due to scattering of the laser light.

Sensors that can detect atomic or molecular contamination will also be required since trace levels of these can perturb film properties resulting in yield loss. Examples of background contamination include trace levels of oxygen, moisture, halides, hydrocarbons, etc. These contaminants can be detected by mass-spectrometry including residual-gas-analyzers (RGAs), optical emission spectroscopy, interactive laser spectroscopy, etc. Like particle sensors, these trace gas sensors are best utilized when interfaced directly with the process equipment for real-time detection and control.

## 5.2 Laser Light Scattering-Based In Situ Particle Detectors

Laser light—and specially polarized laser light—provides a very sensitive method for inspecting pellicles and reticles for lithography. Particles scatter light depending on size. Laser scanning detectors use collection lenses with analysis systems and computer systems to extract signal from noise. The elements of a light-scattering detector are shown in the Fig. 6.

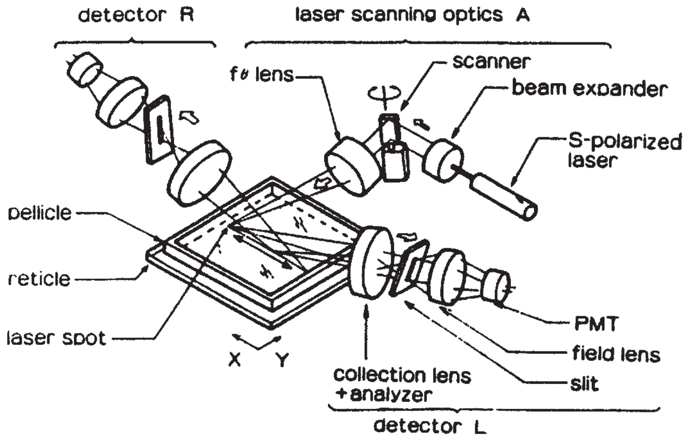
Some end point detection schemes now use this method and are incorporated into manufacturing equipment.

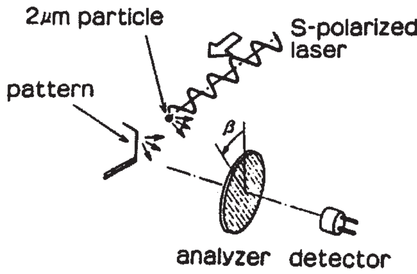
## 5.3 Residual Gas Analyzers, Mass Spectrometry

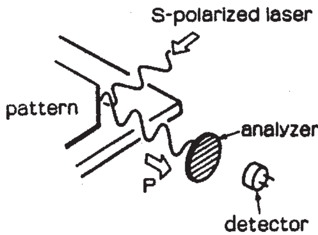
The detection, measurement and control of trace amounts of gaseous contamination has always been an important consideration in high and ultrahigh vacuum systems. It has been estimated that ppb levels of residual gas contamination such as oxygen, moisture, and hydrocarbons can have a deleterious effect on the quality of thin films.

The sources of such contamination are many, and include loadlocks, process chambers, wafer handling robots, atmospheric leaks, process gases, reaction by-products and even the incoming wafers.

While particles can cause optically visible, geometric defects in thin films, other forms of trace contamination, most notably residual (impurity) gases, can directly cause, or be precursors of, phenomena that cause film defects. These defects may be of the type that are visible by optical techniques described above or they may be optically invisible. The most commonly used instrument to measure trace gaseous contaminants in subatmospheric thin film deposition equipment is the quadrupole mass spectrometer-based residual gas analyzer (RGA).



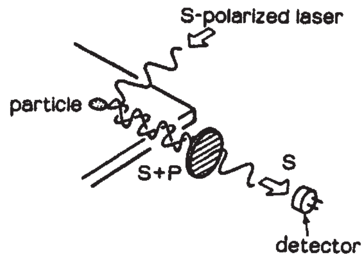




**Figure 6.** The range of detection of these laser scattering methods can vary from about 1 μm to 5–10 μm and procedures for calibration are more difficult at the smaller size ranges. Calibration is achieved by using latex spheres. Data can be converted into 2D maps.

These mass analyzers based on quadrupole instruments operate by ionizing the gas molecules and atoms, separating and counting the impurity molecules according to the mass-to-charge ratio. RGAs have three main parts, namely an ion source, a mass filter, and a detector. The function of the ion source is to create ions from the sampled gas molecules and atoms by electron impact, and to focus and accelerate these ions into the mass filter. The mass filter or quadrupole separates the ions by their mass-to-charge ratio and allows scanning of individual or all ions. The mass filter maintains the focus of ions on the detector. The detector, usually based on a Faraday cup ion collector, collects and measures the ion current. Most detectors are provided with an electron multiplier which amplifies the ion current.

Figures 7 and 8 show the most commonly available RGA configurations available, namely the *open source* and *closed source* spectrometers.

In an open ion source RGA, the ion source is exposed directly to the vacuum atmosphere with all portions within the RGA being at the same pressure as the host tool. This type of RGA is typically used at pressures $<10^{-5}$ torr, for example, to sample substrate transfer and buffer chambers. Typically, a small ion pump is provided with this setup along with an isolation valve. The ion pump maintains the vacuum inside the RGA when the isolation valve between the tool and the RGA is closed. RGAs from some vendors do not require a separate pump for the RGA, especially if it is sampling in high vacuum.

Closed ion source RGAs are useful for detecting lower concentrations (ppm to ppb) of trace contaminants as well as for directly monitoring the thin film processes at operating pressures (typically above $10^{-5}$ torr). Figure 9 shows a schematic of such a system.

An orifice or conductance structure is placed between the ionization region of the RGA and host tool. Differential pumping of the RGA is required and is usually provided by a turbomolecular pump. Protection of the RGA as well as host tool is provided by automatic valving that can isolate the RGA from the process chamber if necessary. In a closed source RGA, ionization of the sampled gas occurs at higher pressures and hence the detected peaks usually have higher intensities with suppression of the background levels.

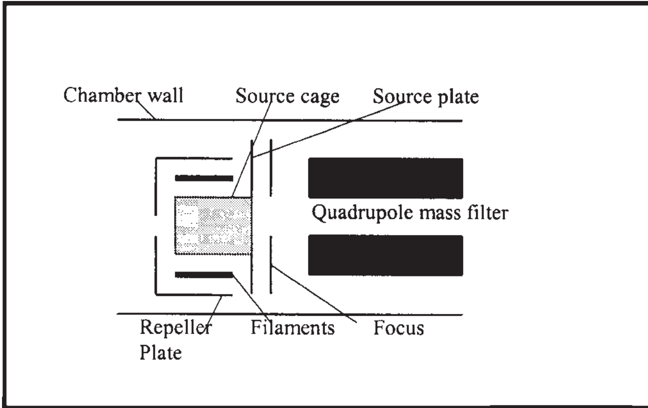



**Figure 7.** Open Ion Source RGA has an internal source.

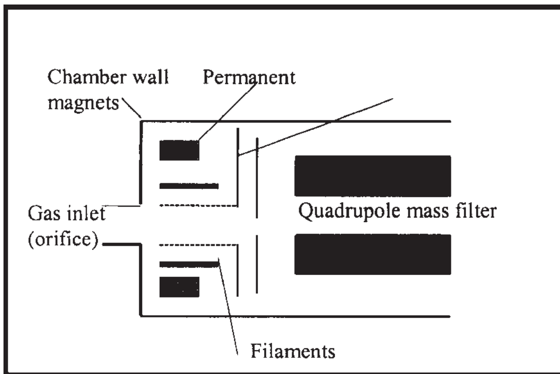



**Figure 8.** Closed Ion Source RGAs are often connected to the equipment and ionize the gas coming from the equipment. This allows end point detection based on chemical species.

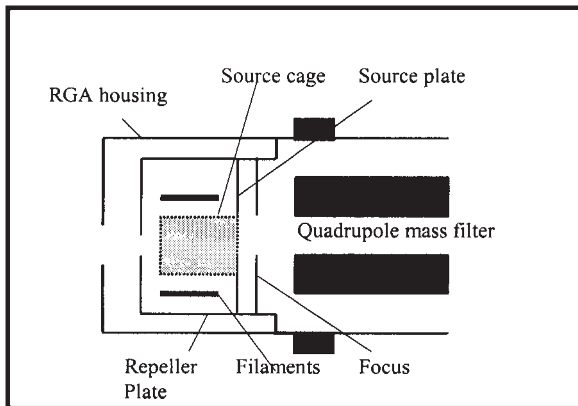



**Figure 9.** Differential RGA does not need such a high vacuum to perform.

Some vendors offer differential ion source configurations quite similar to the open ion source (Fig. 7). This type of RGA is ideal for high as well as low pressure monitoring of residual gases. The ion source contains a collar which effectively reduces the pumping speed to allow it to operate at maximum pressure (typically $10^{-4}$ torr). The quadrupole region is maintained at its ideal vacuum of about $10^{-6}$ torr.

At process pressures, the ratio of the sampled gas signal to the background is increased, thus improving sensitivity. For low pressure sampling, the sensitivity remains high with no losses due to conductance restrictions. With these capabilities, the differential ion source-based RGA is well suited for monitoring base pressure conditions as well as (higher) processes pressure conditions.

## 6.0 SUBSTRATE SURFACE PREPARATION TECHNIQUES

### 6.1 Introduction

Cleaning processes are the most prevalent operations in ULSI manufacturing. Cleaning technology, once relegated to a relative "low-tech" area of semiconductor manufacturing, is now becoming an important yield modulator and is being increasingly researched. There are three common categories of cleaning.

**Cleaning:** to strip off organic and inorganic films after they have served their purpose. Examples of these techniques include stripping of photoresist and hard-masks such as silicon nitride.

**Etching:** to intentionally remove both organic and inorganic films in a controlled manner. Examples of etching processes include plasma etching of polyimide and HF-acid etching of thermal oxide.

**Surface preparation:** which may involve controlled etching and cleaning and, as a result, tailoring the properties of the interface between two layers such as between the substrate and the deposited film. Examples of surface preparation include etching native oxide and cleaning the single crystal Si substrate prior to epitaxial Si growth.

The most common and well-understood approach in substrate cleaning has been and continues to be the use of wet chemicals such as acids and bases. Dry (plasma) processing is a mature and increasingly cost-effective approach for cleaning that involves both stripping and etching. However plasma cleaning usually induces radiation damage and cannot generally be used for surface preparation. Plasma-less, gas-phase and vapor-phase cleaning techniques have found niche applications in surface preparation. For some applications, gas-phase cleaning is the only technologically feasible approach. A good example of this is a vapor HF etching of poly-Si prior to depositing tungsten silicide for the formation of a polycide film.

## 6.2 Aqueous Chemical Cleaning and Etching

Various kinds of liquid based etch, clean, and rinse processes are part of the modern wafer processing fabricators. The supply of clean, defect-free water for rinse is often a major challenge, depending on where fabricators are located. Table 2 shows some of the changes in the arena.

## 6.3 Role of Organic Contamination

Table 2 shows that there are many places in the process where contamination can occur. It was originally thought that all organic contamination was decomposed and vaporized by high temperature annealing. It has been recently reported that levels of organic contamination in

Class 1 cleanrooms are often worse than Class 10 level contamination.[13] Organic residues—benzoids with C=O bonds, $SO_2$ bonds, ethers and phthalic anhydrides—detected by thermal desorption spectroscopy, gas chromatography and mass spectroscopy have been shown to cause reliability failures.

Gate oxides are susceptible to electric breakdown and many cleaning solutions seem to leave trace element impurities (Fe, Cu, Ni, Cr) often after ashing and wet cleaning.

**Table 2.** Cleaning and Processing Solutions Leave Contamination

| | Etches/Cleaners | Timeframe | Comments |
|---|---|---|---|
| Etches | | | |
| | Bufferd etches, OE, oxide cleans | | Still in use. Leaves trace meal Impurities. |
| 1st Generation Cleaners | | | |
| | SC1: $NH_4OH$-$H_2O_2$-$H_2O_2$ | 1970–1990 | Fe-Cr-Ni-Cu contamination left on the surface. |
| | SC2: HCl-$H_2O_2$-$H_2O$ | | |
| 2nd Generation Cleaners | | | |
| | Hydroxyl amine based cleaners | 1990s | These cleaners work with Al-$SiO_2$ systems. |
| 3rd Generation Cleaners | | | |
| | Flouride based cleaners | 2000 | Cu- Low K. |
| 4th Generation Cleaners | | | |
| | Organic cleaners for low K dialectics | 2003 | In development. |
| | CMP based solutions—Metals | | Often leaves organic residues. |
| | CMP based chemicals—Oxides | | |

### 6.4 Summary

Techniques for preparing the substrate surface prior to deposition thin films are summarized below.

- Immersion batch cleaning, use of sonic energy, brush-scrubber (post-CMP cleaning), spin cleaning.
- RCA clean, pre-epi surface preparation, pre-metal deposition cleaning.
- Gas, vapor-phase chemical cleaning and etching.
- Single-wafer cleaning.
- Cryogenic cleaning techniques (ice-scrubber cleaning).
- Plasma cleaning (oxygen and fluorine-based chemistries), UV cleaning (UV-ozone, UV-$Cl_2$, UV-$F_2$).

## 7.0 CHALLENGES TO ULSI (GIGABIT) CONTAMINATION CONTROL

As the industry further scales to smaller features, contamination and defect control issues may be discussed at two extremely different ends of the physical scale. Gate oxides are in the 50 Å or less scale in the vertical direction. Intermediate layers like the short metal lines are in the 100–1000 nm range. In the last layers, larger features can be encountered. Table 3 shows how this determines the choice of detection equipment.

The kinds of defects causing loss of yield are difficult to detect as they may lie at the bottom of deep (1–2 µm) trenches where SEM/optical methods either lack resolution or depth of focus. Illustrations of the kinds of defects that may be found are shown in Fig. 10 and they are described in Table 4.

The increasing number of defect types drives up the cost of defect detection and fault reduction. Companies are forced to buy different kinds of equipment, and this often becomes an economic challenge.[12]

A related question is what is the killer defect size? A killer defect in the DRAM industry is thought to be one-third of minimum feature size as shown in Table 5.[13]

In conclusion—the submicron factory has to consider the process and the kind of defect being sought. In addition, the state of development of the process is also a factor to consider. This is discussed below.

**Table 3.** The Scale of the Defect Determines the Type of Analysis Required

| Range of Physical Size | | Kinds of Defects (size) | Instruments |
|---|---|---|---|
| 10–100 Å | Gate<br>Shallow trench | Pinholes (10 Å)<br>Surface states (electron dimension)<br>Hot electron degradation | Best done with electrical testing TEM etc. |
| 10–1000 nm | Metal<br>Inter layer dielectric | Shorts<br>Metal particles<br>Oxide pin holes shorting | SEM<br>Laser based metrology<br>Electrical testing |
| Organic Contamination | All layers wet steps | Surface analysis<br>Mass spectroscopy | Special techniques needed<br>Electrical testing not very effective |

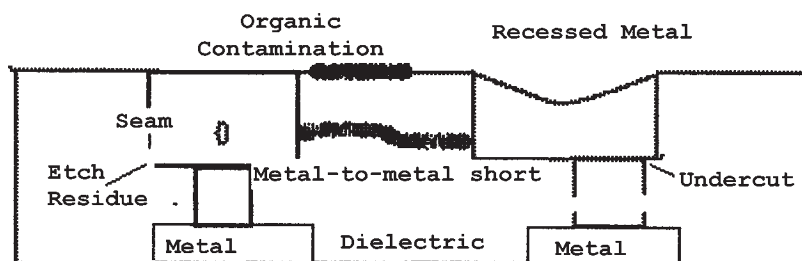



**Figure 10.** Surface, buried, and other kinds of features encountered. These are discussed further in Table 4. For more details, see Ref. 12.

**Table 4.** Classification of defects by "kind" of defect. Which will become killer defects?

| | | | |
|---|---|---|---|
| Surface | CMP Slurry<br>Residue of all kinds<br>Metal dishing<br>Undercut<br>Scratches<br>Pinholes | Sizes can range from nm to μm<br>May cause electrical failures | Not all are killers<br>May not become a problem until the next layer is formed |
| Buried under first layer | Voids in metals<br>Voids in ILD<br>Buried particles | These develop and change as layers are added | Detection next to impossible with inspection techniques |
| Chemical variations | Changes in implant doses<br>Organic contamination | Cause electrical noise<br>Changes in performance | |

**Table 5.** This table highlights the fact that, with scaling, the killer defects will be in the submicron domain.

| DRAM | 16 Mb | 1 Gb |
|---|---|---|
| Min Feature Size | 0.5 μm | 180–150 nm |
| Est. Killer Defect Size | 0.17 μm | 60–50 nm |

## 7.1 Effect of People on Particle Density in Cleanrooms[13]

Particle generation from one person often exceeds 600 counts/sec for particles >0.3 µm. This affects cleanliness of cleanrooms. Without people the room generation is about 200–300 counts/sec (>0.3 µm). The average particle density, $D_0$, is given by

$$D_p = V_{pg} /(V_{air} * Sp)$$

$V_{pg}$ = generation rate per person

$V_{air}$ = flow rate in clean room

$Sp$ = clean room area / person

If: $V_{pg} = 300$ counts/sec

$V_{air} = 1$ ft/sec

$Sp = 1000$ ft$^2$

then: $D_p = 0.3$ particles/ft$^3$

According to US-FS-209 D, the density of >0.5 µm in Class 0.1 is 0.1 particles per ft$^3$. Therefore in the immediate vicinity of people, cleanliness cannot be better than Class 100. This is a consideration when wafers are being handled, moved, or analyzed. Many fabs have automated movement of wafers and cassettes.

The importance of fab cleanliness has been studied by Kitajima and Shiramizu (1997).[13] They have derived calculated yield loss curves which are shown in Fig. 11. These are calculated "estimates," but nevertheless show the importance of the cleanliness of the fabricator. Such graphs are also important to provide accurate cost estimates of fabricators.

After people, process and equipment are the second and third largest producers of defects. It is thought that fabs may not be able to get better than Class 1, and defect detection and contamination control are likely to remain major issues in the fabs of the future.

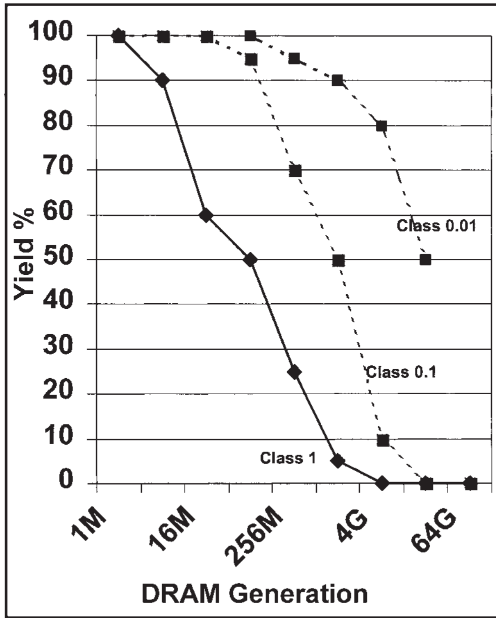



**Figure 11.** Estimates the yield of DRAMs vs. different cleanroom conditions.[13]

## 8.0 PROCESS EVOLUTION

Defect detection and defect reduction are two key components of yield improvement. As processes have become more complex with many more layers, and because fabricators have to start many thousands of wafers per week, several concepts of "high-volume-production" have become widely held. These are discussed in this section.

A concept which has become widely held is that there are generic phases in the manufacturing process life cycle. Table 6 explains some of the aspects of this evolution.[16]

In Phase 3 (Table 6), the key attribute of detection equipment is throughput—sometimes only one wafer per lot can be examined. Tools may scan over 500 SRAMS per wafer, and throughput times of less than six minutes are desirable. In Phase 1, the same test can take up to one hour.

Phase 2 is considered by some to be the most difficult because defects are going down in number, detectability is becoming difficult, and it is not easy to get statistically significant data. This is also the period when "killer" defects are distinguished from less-critical defects by correlation with electrical data.[18]

**Table 6.** Evolution of the Process from R&D to Volume Production

| | | |
|---|---|---|
| Phase 1:<br>Research and Development | Few hundred wafer starts per week. | Detailed characterization using a yield learning vehicle like DRAM or SRAM. Use of test vehicles. Use of detailed TEM/SEM methods. Electrical testing of known modes. |
| Phase 2:<br>Yield Ramp | Up to 1000 wafer starts per week. | Use of test vehicles and product wafers. Yield improves from 20% to 80%. Statistically significant experiments can be performed. Wafer inception tools used in line. Electrical parametric testing done |
| Phase 3:<br>Volume Production | Sometimes over 4000 wafer starts per week. Several products may be running. | Identify process excursions. Use SPC (Statistical Process Control) methods. Optimize and economize process. SRAM and DRAM perform process<br>Shrinks.<br>Wafer monitoring for contamination reduced to a minimum. Use of CD SEM continues.<br>Electrical parametric testing used for optimizing the process. |

## 9.0 EVOLUTION OF CIRCUIT BASED ELECTRICAL DEFECT DETECTION

It has long been recognized that circuit yield and performance are the last and final words in defect detection. Over the years, the industry has evolved several circuit and electrical test methodologies to study electrical defects and yield. The NTRS roadmap projections are shown in Table 7.

Certain special test vehicles—where design rules are especially skewed to promote known marginality—are sometimes used to develop process capability as described in Ref. 14 where a special SRAM was designed as a yield enhancement vehicle. Such vehicles help extract critical layout design rules. Figure 12 shows the cell level drawing of such a test circuit.

The actual six-transistor cell may be drawn as shown in Fig. 13. The six-transistor (2 p-mos, 2 n-mos, and 2 n pull-up transistors) SRAM layout can be the starting point of a yield learning vehicle. This SRAM has to be laid out per the design rule for the technology under evaluation. Reference 177 shows how a 0.35 µm design test vehicle may be used.

A typical layout—taken from Ref. 21—with a fault included is shown in Fig. 14.

**Table 7.** Industry Estimates of Electrical Defects Tolerable for 80% Yield

| Ship date | 1997 | 1999 | 2001 | 2003 | 2006 | 2009 | 2012 |
|---|---|---|---|---|---|---|---|
| NODE (nm) | 250 | 180 | 150 | 130 | 100 | 70 | 50 |
| DRAM, 1$^{ST}$ year Electrical $D_O$ for 80% yield d/m$^2$. Estimates only. | 1390 | 985 | 875 | 695 | 490 | 350 | 250 |
| Microprocessors | 1310 | 1150 | 1025 | 910 | 760 | 640 | 525 |
| ASIC 60% yield | 1210 | 725 | 685 | 645 | 580 | 530 | 450 |
| Min Mask Count | 22 | 22/24 | 23 | 24 | 24/26 | 26/28 | 28 |

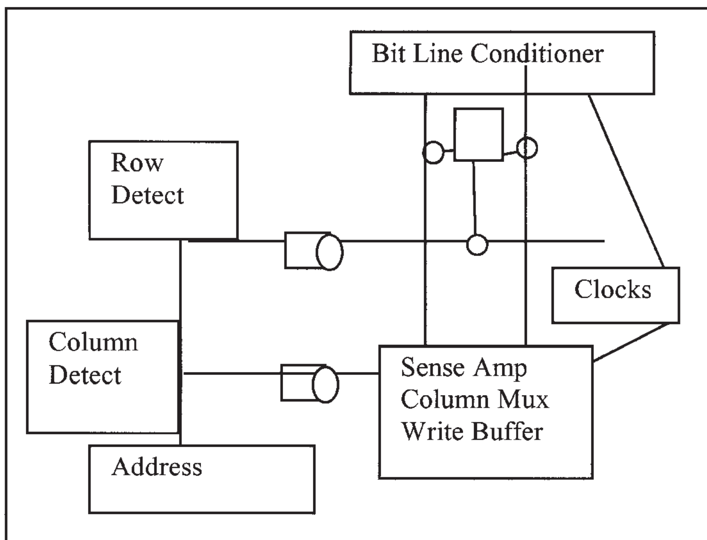



**Figure 12.** Cell level circuit of an SRAM.

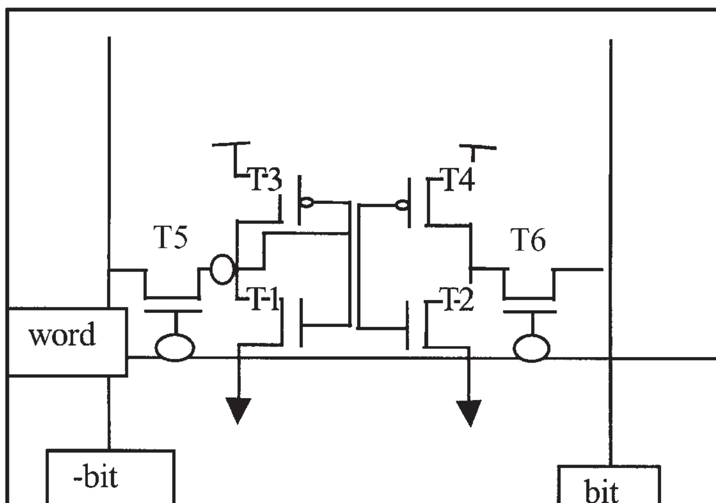



**Figure 13.** A 6-transistor cell schematic.

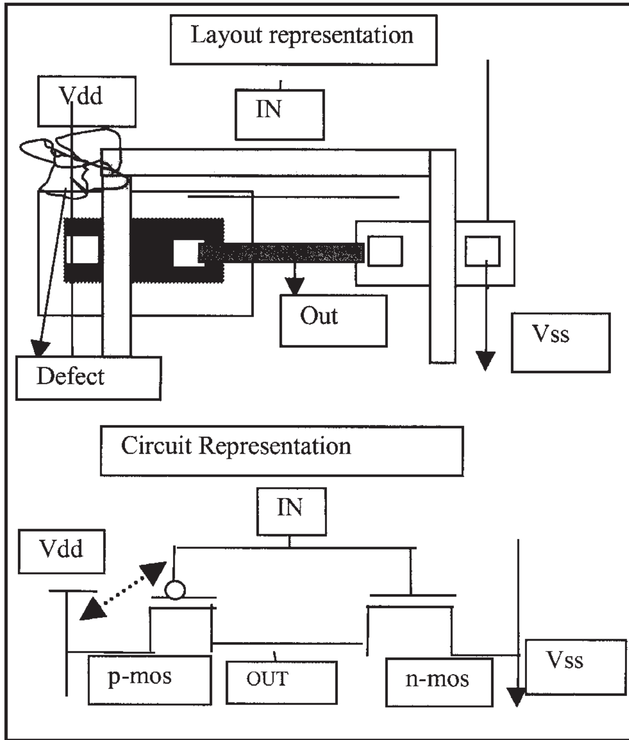



**Figure 14.** Inverter layout showing how a Vdd-to-Gate short induced by a defect could be used to determine electrically active defects.

In order to illustrate the process, it will be noticed that the SRAM cell is nothing but two inverters back to back. Shown here is the layout associated with one inverter. Also shown is a particle (metal) which shorts the Vdd to the gate of the first transistor.

Such a defect is, in principle, easy to detect with electrical testing once a correlation has been done. A catalog of physical-to-electrical defect correlations have to be maintained.

Not all defects are killer defects, therefore the availability of DRAM and SRAM arrays are particularly useful in correlating visible defects with electrically active ones. Since row and column and bit failures can be found by electrical testing, sophisticated correlations are possible. Table 8, from P. Bichebois, is an example of correlation using embedded DRAMs with 0.35 μm design rules.

For ASIC and microprocessor layouts, where there is a great difference in the density of circuits, dedicated test chips have to be laid out. Stapper and coworkers of IBM[22] describe such a test chip containing SRAMS, logic, and I/O areas where the layout densities are vastly different. Using this method, critical areas for layout are determined, and circuit sensitivity to defects can be minimized.

**Table 8.** Failures Caused by Defects Detected During Automatic Inspection[18]

| Electrical Failures | Explained failures caused by one of the detected defects | Unexplained failures - undetected defect of another problem | Ratio of electrical defects caused by detected defects |
|---|---|---|---|
| Single Bit fails | 300 | 394 | 43% |
| Multiple Bit Fails | 54 | 60 | 47 % |
| Column Fails | 232 | 204 | 53 % |
| Row Fails | 366 | 61 | 86 % |

## 10.0 CONCLUSION

Contamination control, defect detection, and correlation with electrical defects will remain very prominent parts of semiconductor manufacturing. This chapter includes a survey of the various methods for contamination control and detection, and shows that visual identification of defects will continue to become more and more difficult as scaling proceeds. The concept of process maturity is briefly discussed. The use of electrical test vehicles and their increasing importance is underscored.

## ACKNOWLEDGMENT

We thank the management at Intel for the time to write this chapter.

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# 8

# Sputtering and Sputter Deposition

*Stephen Rossnagel*

## 1.0 INTRODUCTION

Sputtering and sputter deposition are widely used techniques for the erosion of surfaces and the deposition of films. Sputtering, also known as sputter etching, is used for patterning semiconductor wafers, for cleaning surfaces, for micromachining, depth profiling, and a number of applications which require careful, microscopic erosion of a surface. Sputter deposition is used for film deposition on semiconductor wafers, on magnetic media and head surfaces, for coating tools and cutting surfaces for wear resistance (this includes, by the way, such tools as shaving razors), for reflective coatings on window glass, for coating the insides of plastic bags and the surfaces of automobile parts, and a number of other wide ranging applications.

Sputtering is usually practiced by means of plasmas which generate charged particles which can be accelerated towards a surface electrically. Sputtering is simply the process of erosion of that surface by the energetic particles, a sort of atomistic sandblasting. Sputter deposition is nothing more than the accumulation of these atoms which are blasted off the surface onto a nearby sample. For the most part, this chapter deals with sputtering and sputter deposition with a slant towards semiconductor processing. However, the discussion is wide enough that other areas are introduced from time to time as needed.

## 2.0 PHYSICAL SPUTTERING THEORY

Sputtering occurs whenever any particle strikes a surface with enough energy to dislodge an atom from the surface. The sputter yield is just the ratio of the number of emitted particles per incident particle:

Eq. (1) $$Y = (\text{\# of emitted particles/\# of incident particles})$$

Sputtering can occur for virtually any incident species, including atoms, ions, electrons, photons, and neutrons as well as molecules and molecular ions. For virtually all practical cases, sputtering almost always utilizes ion bombardment, either with inert gas ions such as $Ar^+$ and $Kr^+$, or small molecular ions such as $N_2^+$, $O_2^+$, and so on. The yield for bombardment of a surface with an ion or an atom of the same energy will be virtually identical; physical sputtering relies on the transfer of physical momentum and kinetic energy from the incident particle to the surface atoms, and this is independent of the particle's charge.

The sputtering process is shown generically in Fig. 1. The incident particle impacts the surface or near-surface atoms of the solid with sufficient energy to break bonds and dislodge atoms. If, during this process, one or more atoms are removed from the solid, they are considered to be sputtered atoms.

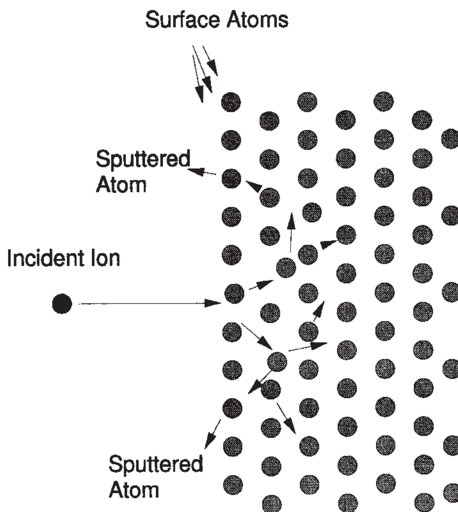


**Figure 1.** Schematic of physical sputtering process.

## 2.1 Energy Dependence of Sputtering

Physical sputtering can be described in four general energy ranges, from energies at near the binding energy to many MeV.

*a. Very low energies.* At incident ion energies of a few eV or so up to 30–50 eV, there is very little sputtering. Early work (1960's)[1] suggested the presence of a sputter threshold in this energy regime below which no sputtering occurred. This has been found to be slightly misleading, and it is now generally thought that the minimum ion energy for sputtering is the binding energy of the most-weakly-bound surface atom

The yields in this energy range are typically below $10^{-2}$ at 30–40 eV ion energies, and fall rapidly at lower ion energies to the $10^{-6}$ level and below. While this may seem insignificantly small, consider a high density plasma source such as an ECR source (ECR stands for Electron Cyclotron Resonance). With 1 kW of microwave energy transmitted into the plasma, the effective ion production rate is on the order of $10^{20}$ per second, or about 15 amperes. If each of these ions reaches the wall with an energy of 10 eV (typical for this type of system), then the erosion rate at a yield of $10^{-6}$ is still about $10^{14}$ atoms/sec. In a few minutes, this will deposit a monolayer or two on all surfaces within the tool, including any windows or insulators. Within an hour, this very tiny sputter yield has the potential to make opaque, conductive films throughout the chamber (including the quartz windows through which the microwave power enters), which could make operation of the system difficult. Very low energy sputter yield measurements are very difficult to make accurately and there is almost no mention of them in the literature.

*b. Knock-on energy regime.* At incident energies of 40 to perhaps 1000 eV, the incoming particle has more than enough energy to dislodge tens to hundreds of atoms. The collision sequence is erratic, though, and depends on exactly where the incident particle hits. After this first collision, the incident particle and the impacted one move on into the material causing more and more collisions. The nature of these collisions is difficult to follow, though, because it depends on exactly where the first particle hits. Eventually, though, these knock-on collisions may result in an atom at or near the surface being ejected from the solid.

Knock-on sputtering has been modeled by computer calculations which follow the trajectories of a large number of incident particles.[2] The yield for each individual collision sequence can vary widely, from 0 to perhaps 10 or more. The average result should then be characteristic of the

experimental sputter yield, which is itself the average of a great number of incident particle collisions.

Knock-on sputtering characterizes the practical energy range used for most sputtering applications. There are several general characteristics of knock-on sputtering:

1. The sputter yield increases linearly (roughly) with incident ion energy (Fig. 2).
2. The highest yields occur for the best mass match between the incident species and the solid.
3. Increasing the angle of incidence from normal incidence (straight down) to perhaps 50 degrees from normal can increase the yield significantly (1.5–3×) for most materials.
4. An increase in the flux (ion current) results in a linear increase in the number of sputtered atoms.

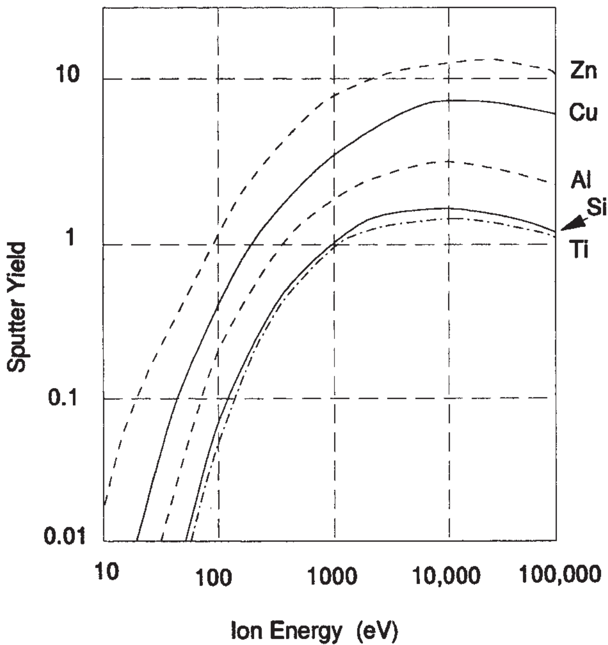


**Figure 2.** The sputter yield for several materials as a function of Ar ion energy.[3]

Items (1) and (4) suggest that the sputtering rate and in many cases the sputter deposition rate will scale roughly with power. Therefore, doubling the discharge power in a sputtering system should result in roughly a 2× increase in deposition rate.

A table of sputter yields for common materials is given for Ar ion bombardment at several ion energies (see Table 1). Tabulated sputter yields are notoriously questionable because over the years yields have been often measured in flawed experiments. The numbers included below should always be taken as approximate.

**Table 1.** Sputter Yields as A Function of Ar Ion Energy for Commonly Used Materials

| Material | 300 eV | 500 eV | 1000 eV |
|---|---|---|---|
| Ag | 1.7 | 2.5 | 3.5 |
| Al | 0.6 | 0.9 | 1.5 |
| Au | 1.1 | 1.7 | 2.5 |
| B | 0.2 | 0.6 | 1.1 |
| Be | 0.3 | 0.5 | 0.9 |
| C | 0.1 | 0.3 | 0.6 |
| Co | 0.7 | 1 | 1.7 |
| Cr | 0.8 | 1.1 | 1.9 |
| Cu | 1.5 | 1.9 | 2.9 |
| Fe | 0.7 | 1 | 1.7 |
| Ge | 0.6 | 1 | 1.5 |
| Hf | 0.4 | 0.6 | 0.9 |
| Mo | 0.3 | 0.5 | 0.9 |
| Nb | 0.4 | 0.6 | 0.9 |
| Ni | 0.7 | 1.0 | 1.7 |
| Pb | 2.5 | 3.2 | 4 |
| Pd | 1.5 | 1.8 | 2.5 |

*(Cont'd.)*

**Table 1.** *(Cont'd.)*

| Material | 300 eV | 500 eV | 1000 eV |
|---|---|---|---|
| Pt | 0.7 | 1 | 1.6 |
| Re | 0.4 | 0.6 | 1.0 |
| Rh | 0.7 | 1 | 1.7 |
| Ru | 0.7 | 1 | 1.7 |
| Si | 0.3 | 0.7 | 1 |
| Sn | 0.6 | 0.9 | 1.4 |
| Ta | 0.3 | 0.5 | 0.9 |
| Ti | 0.3 | 0.5 | 0.7 |
| V | 0.4 | 0.7 | 1 |
| W | 0.3 | 0.5 | 0.9 |
| Zn | 3.7 | 5 | 7 |

*c. Collision-cascade sputtering.* At ion energies of nearly 1 keV to perhaps 50 keV, the incident particle has sufficient energy to break all the bonds between atoms in a spherical region around the impact site. While this regime has generally higher yields than the knock-on regime, the higher energies (and voltages) make it impractical to use for most industrial-scale sputter deposition applications.

*d. High energy implantation.* At ion energies above 50 keV, the incident particle can travel well into the bulk of the solid before depositing its energy. While this can create significant damage a micron or so below the surface, little or no sputtering occurs because the energy is deposited so far away from the surface. In addition, the incident particle is often trapped or implanted within the sample.

## 2.2 Energy and Direction of Sputtered Atoms

Sputtered atoms differ from evaporated atoms in their kinetics, due to the dynamics of the emission process. The kinetic energy distribution of sputtered atoms peaks at a few eV to 10 eV and then decreases as $1/E^2$ (Fig. 3). In general, though, the average energy for sputtered atoms is

much higher than for evaporated atoms, and the qualities of the deposited films will also be different. The average kinetic energy for several species has been measured.

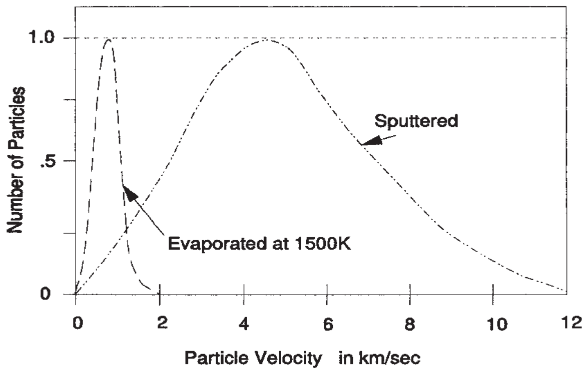


**Figure 3.** The kinetic energy distribution for sputtered Cu compared to Cu evaporated at 1100°C.

The angular emission distribution for sputtered atoms is often described as a cosine distribution. This means that the relative amount of material sputtered at any particular angle can be compared to the amount sputtered at normal incidence times the cosine of the angle from normal incidence. This is shown schematically in Fig. 4. The overall distribution is often drawn as a circle, which is the relative amount emitted at any particular angle. In three dimensions, this would appear as a sphere centered on the impact point.

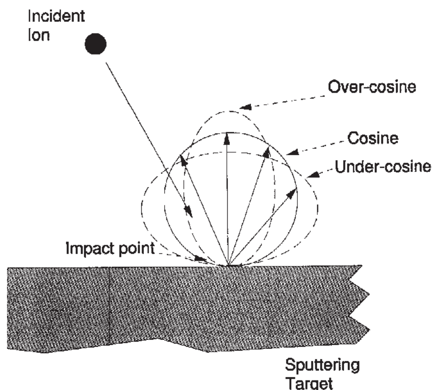


**Figure 4.** The angular emission distribution for sputtered atoms for Ar sputtering of Cu.

In some cases, the angular emission distribution differs from a cosine into either an under- or over-cosine distribution. An over-cosine distribution would be more forward-peaked with less emission out to the side. An interaction distribution would be just the opposite. There is a general trend that, as a function of ion energy in the knock-on regime, low energies result in under-cosine emission, and as the ion energy is increased, the emission becomes more peaked.

## 3.0 PLASMAS AND SPUTTERING SYSTEMS

Incident particle energies in the hundreds of eV range needed for sputtering are much easier to arrange for ions compared to neutral atoms. Ions respond to electric fields and potentials and it is very straightforward to configure an acceleration voltage of a few hundred volts within a vacuum chamber. There are two classes of systems used to generate ions: plasmas and ion beams. The only real difference here is that in the plasma source, the surface to be bombarded is immersed in the plasma, and in the ion beam case, the plasma is physically separated from the target, and an ion beam is extracted from the ion source to bombard the surface. Most of this discussion centers on plasma sources, although a short description of broad beam ion sources is included.

*a. Diode plasmas.* The simplest kind of plasma device, a diode, is simply an anode and a cathode inside a vacuum system (Fig. 5). Under the right conditions, with adequate voltage across the electrodes and the appropriate gas pressure, the gas will breakdown into a plasma discharge. In this discharge, the potential of the plasma is spatially uniform, and actually just slightly higher than the anode potential. Near the cathode is a dark space or sheath in which there is a very large electric field. Ions are accelerated rapidly across the sheath and strike the cathode. As part of this collision (which can cause sputtering), occasional electrons, known as secondary electrons, are emitted from the surface. These electrons are accelerated back across the sheath and gain significant energy. This energy is then used, through collisions with gas atoms, to form more ions to sustain the discharge.

The secondary electron yields are usually pretty low, a few percent or so. The yield is also energy independent at ion energies below 1 keV. The secondary electrons are the primary source of energy to the plasma discharge, and each secondary electron must generate a significant

number of ions. (See Table 2.) A quick estimate of this number is simply the inverse of the secondary electron yield. For example, if the yield was 5%, each secondary electron needs to generate 20 ion-electron pairs to achieve steady state. If fewer are generated, the plasma will quickly reduce in density until a steady state is reached.

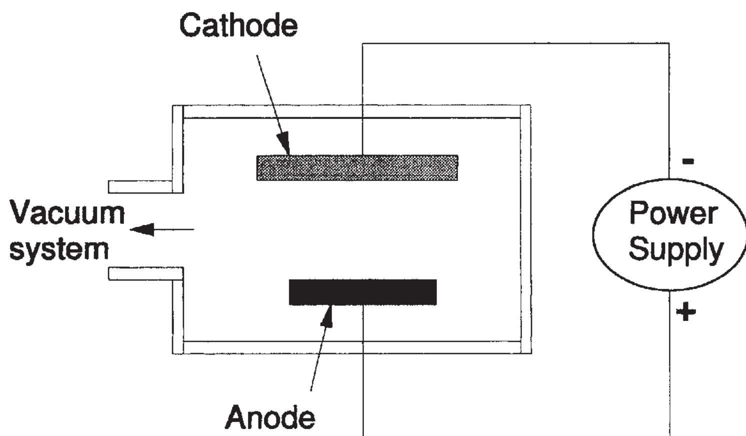


**Figure 5.** A simple diode sputtering device. The vacuum system is not shown, but it would operate at pressures in the mTorr to low Torr range.

**Table 2.** Secondary Electron Yields for Common Materials for Ar Ion Bombardment

| Material | 10 eV | 100 eV | 1000 eV |
|---|---|---|---|
| Mo | 0.122 | 0.115 | 0.118 |
| W | 0.096 | 0.095 | 0.099 |
| Si(100) | 0.024 | 0.027 | 0.039 |
| Ni(111) | 0.034 | 0.034 | 0.07 |
| Ge(111) | 0.032 | 0.037 | 0.047 |

Diode plasmas were historically first used to both erode surfaces and for sputter deposition. They have been limited in their current-day applicability by low rates and the difficulty of sputtering or depositing insulators. The low rates are due to the low ionization cross section for electron-impact ionization of most gas species. This means that some of the secondary electrons can pass right through the plasma and hit the anode. While this is nice for current flow, the loss of this secondary electron means that no new ions are made from gas-phase collisions. This limits the net current flow and hence the sputtering rate. The process also gets worse at higher and higher voltages; as the cross section is decreasing, the electron energy increases. This results in a process that does not "scale," meaning that increasing the power or dimensions of the tool does not result in increased rates.

In addition, conventional diode plasmas cannot be operated if the cathode surface is insulating. This would be the case if the cathode was itself an insulator, or if the cathode was used in a gas such as oxygen which might make the surface of the cathode insulating. The result in either case is extremely low discharge currents and very little sputtering.

*b. RF Diodes.* An rf diode and a dc diode are visually the same thing. The only real difference is that, for diodes, the power supply is operated at high frequency. The most common frequency is 13.56 MHz, although experiments have run the gamut from 60 Hz to 80 MHz or more. Most manufacturing systems use 13.56 MHz or simple multiples (2× or 3×). The rf diode operates in a slightly different way than the dc diode: for a small part of the rf cycle, the cathode and anode are electrically reversed. This eliminates charge buildup on an insulating surface by providing an equal number of ions, then electrons, then ions, and so on. This allows insulators to be sputtered or metals to be sputtered in reactive environments.

A second key advantage of an rf diode system is that the oscillation of fields in the plasma (at the driving frequency) results in additional electron motion within the plasma. This has been described in several ways, although the most interesting is an analogy to the electron "surfing" on the electric field waves in the plasma.[4] The end result of this enhanced electron movement is that the probability of an ionizing collision is increased for a given secondary electron, and this results in an increase in the plasma density compared to a dc diode. This density increase results in higher ion currents to the cathode and a faster sputtering process.

The rf diode system requires impedance matching to operate most efficiently. This matching network, often located in a "matchbox" immediately adjacent to the vacuum system, helps to optimize the transfer of

power from the power supply which is designed to see a load of 50 ohms. The most common matching network is shown in Fig. 6 and consists of two capacitors and a simple inductor. This type of network is known as an "L" network. One important part of this network is the placement of the capacitor between the coil and the cathode. Because of the rapid mobility of electrons in a plasma, the cathode will tend to charge to a negative voltage when exposed to a plasma. The capacitor allows the formation of a net dc bias to the cathode. The dc bias can have a maximum of about 1/2 the applied rf peak-to-peak voltage. Ions in the plasma have too much inertia to respond to 13.56 MHz, so they tend to respond to the average dc bias. This bias is generally associated with the ion energy of ions hitting the cathode.

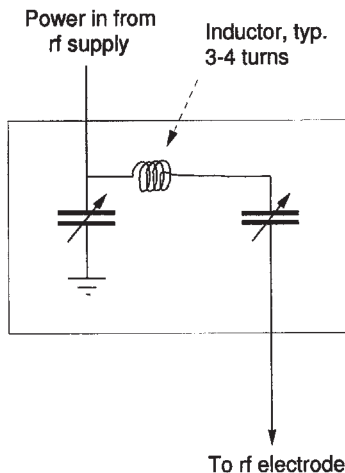


**Figure 6.** A common "L" matching network used on an rf diode sputtering system.

One note of caution here: depending on the equipment manufacturer or the builder of the system (who may have purchased the power supply from another manufacturer), the voltages displayed in rf diode systems are often poorly defined. For example, a displayed voltage could be the peak-to-peak value of the applied rf voltage or it could be the dc bias at the cathode. These values are not always related by a factor of 2. In addition, at high system pressures, the net ion energy of ions hitting the cathode can be

significantly less than the dc bias voltage. This is because ions have collisions part way through the cathode dark space and are stopped and restarted. The whole area of real ion energies in rf diode sputtering is convoluted and system dependent.

*c. Magnetrons.* The term "magnetron" was originally used to describe tubes used to generate microwave power for radar applications. It is still used for this purpose, and the builder or owner of a microwave plasma system will use a "magnetron" power source to run his plasma

The same general magnetron effect found in these tubes can be altered somewhat to make an extremely efficient sputtering cathode. These cathodes operate in a diode mode, either in rf or dc, but are rarely, if ever, called diodes. Magnetron sputtering sources are the current work-horse of the sputter deposition field, used in perhaps 95% of all sputtering applications.

A magnetron uses a static magnetic field configured at the cathode location. The magnetic field is located parallel to the cathode surface. Secondary electrons which are emitted from the cathode due to ion bombardment are constrained by this magnetic field to move in a direction perpendicular to both the electric field (normal to the surface) and the magnetic field. This is known as an **E**×**B** (E cross B) drift, which is also the basis for the Hall Effect. This drift causes electrons to move parallel to the cathode surface in a direction 90 degrees away from the magnetic field. If the magnetic field is set up correctly, this **E**×**B** drift can be arranged to close on itself, forming a current loop of drifting secondary electrons (Fig. 7).

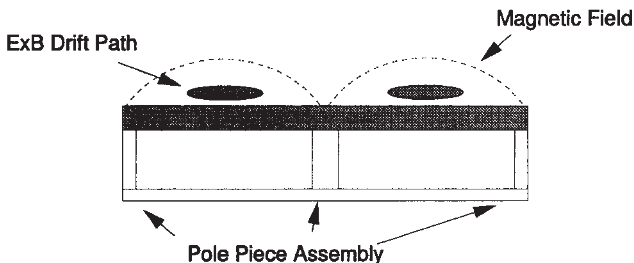


**Figure 7.** The magnetic field configuration for a circular planar magnetron cathode.

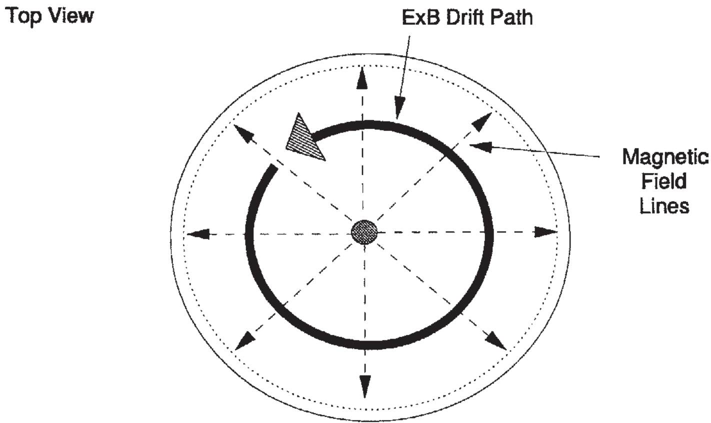


**Figure 7.** *(Cont'd.)*

Unlike the dc and rf diodes, these secondary electrons are essentially trapped in a region close to the cathode. Eventually they lose their kinetic energy due to collisions with gas atoms (ionization) or with other electrons (electron heating), and the net result is an extremely dense plasma in this drift ring. Visually this is quite easy to see in a magnetron sputtering system. The drift path lights up dramatically and there is no question that the density is much, much higher in this region. The location of this ring is also known as the *etch track* because the erosion of the cathode is highest here and deep groves can be eroded onto the cathode.

Ions which are made in the drift region have a high probability of hitting the cathode which is close by. This results in even more production of secondary electrons and eventually an extremely dense plasma. A measure of this is the discharge current. For a typical 1 kW dc diode discharge, the discharge current might be 0.1 A at 10 kV. In a 1 kW magnetron system, the current might be 3.3 A at 300 V.

Magnetrons operate with an unusual voltage-current relation:

Eq. (2) $$I = kV^n$$

where $I$ is the discharge current, $V$ the voltage, and $k$ and $n$ are system material and gas-dependant constants. This relation is only accurate above

a turn-on voltage, but then characterizes many different magnetron systems. For many years, much effort was put into calibrating the various constants for different systems without much insight into what they meant. With rare exceptions, there has been very little work on attempts to derive this relation from first principles.[5] Even though the equation is empirical, it is very often desirable to characterize a given magnetron in this way. This can then be used as a diagnostic for later operation or during the diagnosis of system problems.

The coefficient $n$ in this equation can be thought of as a sort of efficiency factor. A high value of $n$ means that very small voltage increases result in very large current increases. A small value of $n$ means just the opposite. Typical magnetron systems operate with $n$'s of 5–10. A dc diode (non-magnetron), for example, might have an $n$ of two or less. Additional insight into these plasma impedance issues has published over the past ten years, but this is a somewhat empirical area and will not be covered farther.

Magnetrons come in many physical designs, although each is based on the single criteria of a closed-path **E**×**B** drift loop for secondary electrons. The simplest design is the circular planar cathode shown above. It is fairly trivial to stretch this design in one direction forming a more rectangular cathode (Fig. 8). Planar cathodes can be designed with very unusual serpentine paths or nested loops, based on the designer's skills or the need for uniformity. A widely-used version of the planar cathode in the semiconductor industry uses a moving magnet assembly configured behind a circular, planar cathode. The **E**×**B** drift path (etch track) is in the shape of a heart, and this is rotated around the cathode surface by means of a motor drive. This movement results in better cathode utilization as well as better deposition uniformity without the need for moving the sample within the vacuum system.

It is also not necessary to use a completely planar geometry. A widely-used device, known as the "S-Gun," uses a conical cross section for the cathode with the sputtered surfaces inclined at an angle to the eventual sample (Fig. 9).[6] This geometry allows the use of nested loops (multiple etch tracks) for better uniformity as well as the placement of a center anode within the source. Anodes are not commonly used in many sputtering systems because the walls of the chamber act as the effective anodes. However, in the S-Gun geometry, the center anode can be used to adjust the plasma potential, as well as remove unwanted higher-energy electrons from the discharge, resulting in less sample heating.

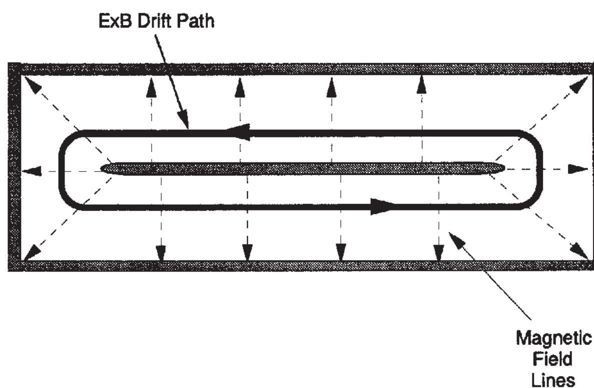


**Figure 8.** A rectangular or "racetrack" magnetron.

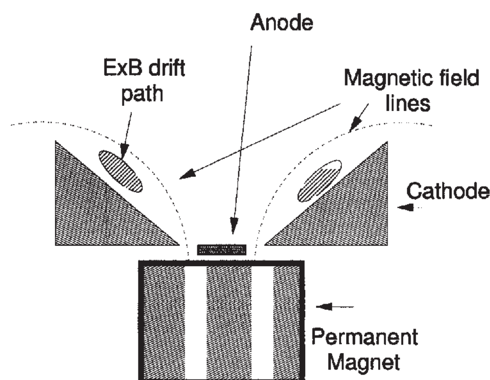


**Figure 9.** The S-gun class of magnetron geometries.

A third geometric class of magnetrons uses a cylindrical post or tube as the cathode. The magnetic field is oriented along the axis of this cylinder. The **E×B** drift paths are then a band which goes around the cylinder, either on the inside or the outside (Fig. 10a and b). These are known as cylindrical post cathodes (Fig. 10a) or hollow cathode magnetrons (Fig. 10b). A lot of early work was done on the cylindrical post cathodes, but they are not widely used anymore. The hollow cathode magnetron is most suited for coating wires or fibers that pass through it. This may turn out to be a solid manufacturing technique.

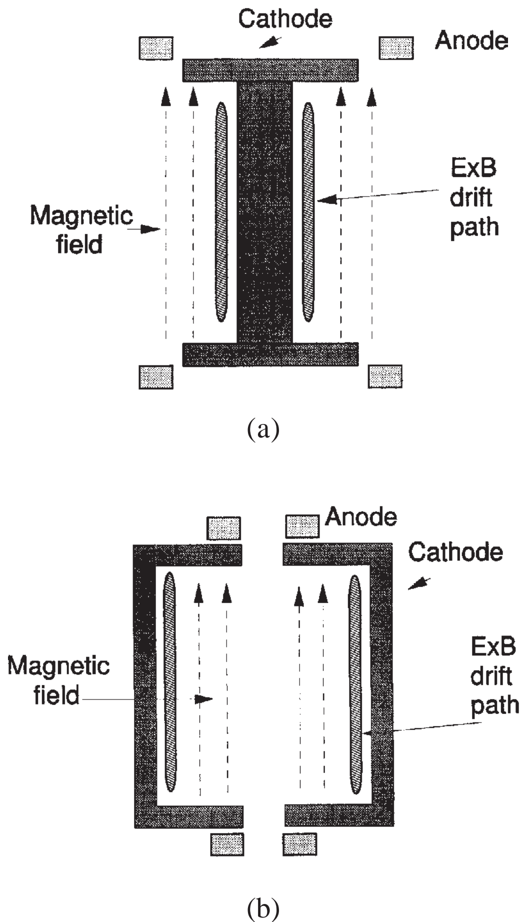


**Figure 10.** (*a*) The cylindrical post magnetron, (*b*) the hollow cathode cylindrical magnetron.

## 4.0 DEPOSITION RATES AND EFFICIENCIES

The general goal for sputter deposition is high rate, controlled, uniform deposition. The nature of the magnetron, which is characterized by a dense plasma **E**×**B** drift loop at the cathode, results in a nonuniform emission, usually from a ring or rectangular geometry. In addition, due to the system geometry, the emission profile of the sputtered atoms, and the distance of the sample from the cathode, the deposition rate is difficult to predict exactly. Various studies have measured the deposition rate and profile as a function of gas pressure and throw distance. Most of these studies are only relatively quantitative in that they are system dependent and there is little effort to calibrate the results.

The deposition process can be quantified in two ways. One uses the intrinsic probability that a sputtered atom emitted from the cathode will be deposited on the sample. This leads to a number between 0 and 1, with 1 being the maximum, ideal transport (all sputtered atoms deposit on the sample). The second approach, perhaps more practical for the operation of systems, quantifies the deposition rate in terms of "rate per watt." In this case, the general assumption is that the deposition rate increases linearly with discharge power (discharge current × discharge voltage). This assumption is fairly accurate in the region of operation of most magnetrons, where the sputter yield increases linearly with discharge voltage and, in practice, the discharge voltage changes very slowly.

**Deposition Probability.** This probability is simply the ratio of atoms which are actually deposited on the sample divided by the total number of atoms emitted from the cathode. The number sputtered, to a first approximation, is simply the discharge current × the sputter yield × the deposition time. This number might be accurate to 20% or so, and is limited by knowledge of the sputter yield for that particular cathode and also by the 5–10% correction caused by the secondary electron yield to the discharge current.

Deposition probabilities are listed in Table 3 for a simple eight-inch diameter planar magnetron in an open vacuum system. Every system is different, though, and the presence of shielding, shutters, and even the chamber walls can alter these probabilities slightly. It should be noted that the best probabilities (highest) occur for low pressure, short throw distance, and a gas species which is lighter than the sputtered species. In addition, sputtering with a heavy gas, such as Kr, is often counterproductive. The sputter yield may be slightly increased, but the probability of an atom getting to the sample and making a film is reduced significantly.

**Table 3.** Deposition Probability for Magnetron Sputtering at 1000 W, 200 mm Diameter Planar Magnetron in Large System[7]

| Throw (cm) | Pressure (mTorr) | Deposition Prob. |
|---|---|---|
| Ar Sputtering of Cu | | |
| 5 cm | 5, 20, 30 | 0.63, 0.49, 0.54 |
| 9.5 cm | 5, 20, 30 | 0.48, 0.47, 0.45 |
| 14.5 cm | 5, 20, 30 | 0.39, 0.35, 0.31 |
| Ne Sputtering of Al | | |
| 5 cm | 5, 20, 30 | 0.80, 0.56, 0.52 |
| 9.5 cm | 5, 20, 30 | 0.40, 0.42, 0.40 |
| Ar Sputtering of Al | | |
| 5 cm | 5, 20, 30 | 0.60, 0.46, 0.42 |
| 9.5 cm | 5, 20, 30 | 0.44, 0.45, 0.35 |
| Kr Sputtering of Al | | |
| 5 cm | 5, 20, 30 | 0.52, 0.45, 0.38 |
| 9.5 cm | 5, 20, 30 | 0.35, 0.27, 0.22 |

**Deposition Rates by Power.** Since discharge power is an easily measured quantity in most sputtering systems, and the deposition rate nominally scales with power, a sputtering system can be characterized by how fast it deposits a given film per watt of power used. These numbers are also very system-dependent, based on the exact configuration of specific tools, operating conditions, etc. These rates are often shown as angstroms/minute/watt. An example of this type of data is shown for a batch-type tool. In this case, however, the sample pallets (37–45 cm wide) were scanned past the cathode such that the rates listed below, in Table 4, are less than the rates for a fixed sample directly in front of the cathode. This is a systematic problem with this type of rate measurement. The numbers apply to this system only.

It is difficult to compare results such as these to another system. For example, present day single wafer semiconductor sputtering tools have a fixed sample position, which would undoubtedly mean a higher deposition rate efficiency than for a moving sample. Results for the sputter deposition of common semiconductor materials are shown in Table 5. The throw distance in this case is about 4 cm.

**Table 4.** Deposition rate per watt for MRC magnetron systems, derived from data by class.[8] Units are Å/min/watt.

| Cathode (Throw distance) | Focest design 1.75 cm | Inset design 5 cm | Planar 5 cm |
|---|---|---|---|
| Al | 0.29 | 0.16 | 0.18 |
| Cu | 0.55 | 0.31 | 0.34 |
| Au | 0.58 | 0.32 | 0.36 |
| Ni-7% V | 0.36 | 0.20 | 0.22 |
| Pt | 0.37 | 0.21 | 0.23 |
| Ag | 0.83 | 0.47 | 0.52 |
| Ti | 0.14 | 0.07 | 0.08 |
| Ta | 0.15 | 0.08 | 0.09 |

**Table 5.** Deposition rates per watt for an Applied Materials "Endura" single wafer sputter deposition system. Cathode is 32.7 cm dia, samples are 200 mm wafers.[9]

| Material | Power | Rate (Å/min/watt) |
|---|---|---|
| AlCu (0.5) | 12.7 kW | 1 (new cathode) |
| | | 0.75 (old cathode) |
| Ti | 1 kW | 0.17 |
| TiN (nitride mode) | 4 kW | 0.15 |
| Ti (collimated,1.5:1) | 7 kW | 0.043 |

This general approach can be extended to specific systems in two ways. The deposition efficiency of any particular system should be related to the numbers listed above by a simple, multiplicative factor. It will be necessary to calibrate each system but, once done, it should not change without major geometry changes. Second, the dependency of the deposition rates listed above can be approximately coupled to the sputter yield, particularly for short throw distances. Therefore, when changing from a cathode included on the list above to another target, a first estimate of the probable deposition rate can be made by comparing the sputter yield of the new material to those listed in the tables.

## 5.0 REACTIVE SPUTTER DEPOSITION

Sputtering is an atomistic process. Most of the atoms emitted from a target, regardless of whether it is an elemental or compound/alloy cathode, are emitted as atoms rather than molecules or clusters. Chemical reactions of these atoms in flight from the cathode to a sample are rare, but it is completely possible that the freshly-deposited atom on a film surface can chemically react with gas atoms that impinge on the surface to form a compound film. A trivial example of this might be the sputtering of Al in the presence of oxygen. The Al is reactive with oxygen, and even though the Al atom is deposited as a "metal" atom, it may quickly react on the film surface to form an oxide. This is generically known as reactive sputtering.

Reactive sputtering is commonly used for the deposition of oxide and nitride thin films. There are two approaches to reactive deposition, one where the cathode is a metal plate, and the other where the cathode is composed of the material of interest to be deposited, for example, a nitride or an oxide. The latter case is usually complicated by the nonconductive nature of many oxide and some nitride targets, requiring the use of rf power to the cathode, as well as the poor physical stability of many of these compounds. This last issue may result in cracking or shattering the compound target, or else in difficulties in bonding it to the cathode, which is usually water cooled.

Reactive sputtering with a metal cathode has received the most attention because of the opportunity for high rate, controlled deposition, as well as the ability to use dc rather than rf power. Reactive sputtering is made more difficult with metallic targets, though, because of the tendency of the cathode itself to react, forming a thin film on the cathode of a nitride or oxide, which can significantly alter the sputtering process.

A reactive sputtering system is shown in Fig. 11. In this system, the cathode is placed in a chamber with walls and a pumping system. The walls are important, because films will also be deposited and reacted there as well as on the sample and the cathode. Typically, a system like this would be operated with some partial pressure of an inert gas, such as Ar, and a partial pressure of a reactive species, such as $O_2$ or $N_2$.

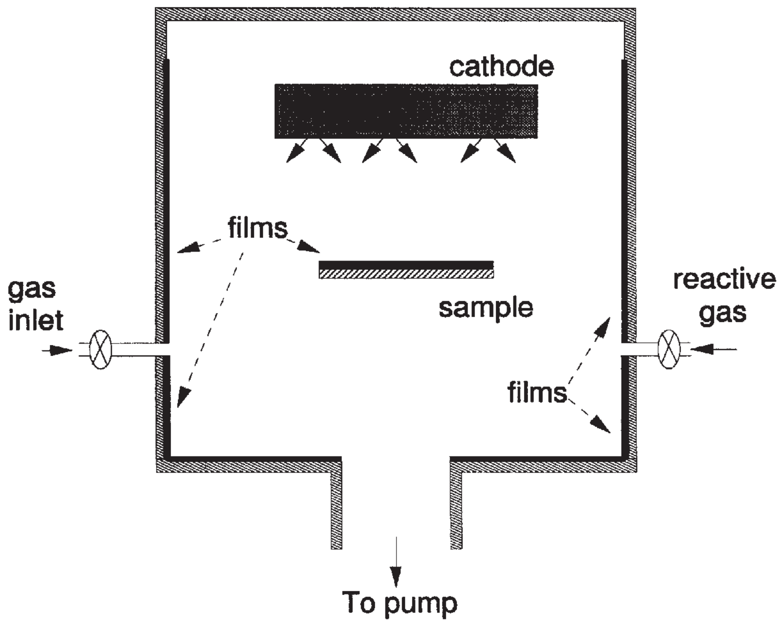


**Figure 11.** A typical reactive sputter deposition system.

The operation of this system can be described by observing the changes in the discharge kinetics as well as the vacuum system as a function of the partial pressure or flow of the reactive species. In Fig. 12, the deposition rate and the discharge voltage are plotted as a function of reactive gas flow rate. There is a constant inert gas pressure in this example, perhaps a few mTorr of Ar. At the far left side of these charts, where there is no reactive gas flow, the cathode is being sputtered with pure Ar and the deposited films are purely metallic. Films are deposited on the sample as well as the chamber walls. As the reactive gas flow is increased (moving to the right from the left-most axis in Fig. 10), very little happens initially. The

reactive gas, oxygen for example, is being absorbed by the deposited films on the sample and the walls. The films are now becoming partially oxidized and form "suboxides." Eventually, a point is reached with increased reactive gas flow where the fully stoichiometric oxide is formed, for example $Al_2O_3$ or $SiO_2$.

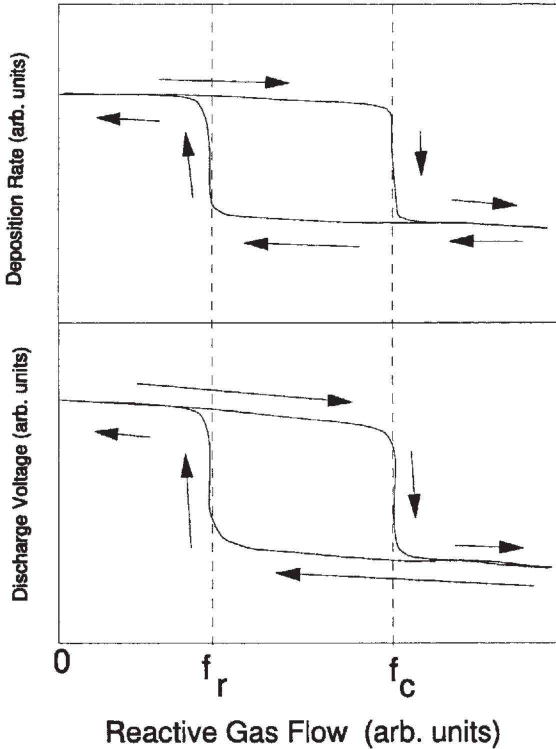


**Figure 12.** *(Top)* The deposition rate and *(bottom)* the discharge voltage as a function of reactive gas flow for the experiment shown in Fig. 11.

This is the critical flow point. Unfortunately, this is an unstable point in the curve. If any additional reactive gas is supplied above this flow, the films will not be able to absorb it as they are already saturated with oxygen. The extra, unused oxygen will now begin to form an oxide layer on the cathode, and this causes an irreversible change. The sputter yield for the oxided cathode is significantly reduced from the purely metallic cathode, sometimes by an order of magnitude or more. This turns

off the supply of metallic atoms to the film surfaces which reduces their ability to absorb the reactive species. The result is then that more of the reactive gas is unused, which causes further oxidation of the cathode, reducing the metal flux even farther. The whole system rapidly changes from a "metallic" mode to a "reacted" mode. The deposition rate goes down rapidly and usually the discharge voltage changes significantly (oxides often go down, nitrides often go up).

This is a one-way transition and is very difficult to control. If the reactive gas flow is reduced after this transition, the system does not convert back at the same flow. This is due to the presence of the residual oxide layer on the cathode. Not until the reactive gas flow is significantly reduced will the cathode clear of oxide and convert back to a metallic mode. The plot of this type of response shown in Fig. 12 is called a hysteresis curve due to its similarity to the response of magnetic materials to a magnetic field although they are completely different effects.

Another factor which changes at the same time as the cathode and the deposition rate is the background gas pressure. This is shown in Fig. 13. The initial starting pressure (of inert gas) is unchanged by the introduction of the reactive gas up to the critical flow point, at which time it rapidly increases. This increase is all in the reactive species, and would also be visible with a mass spectrometer.

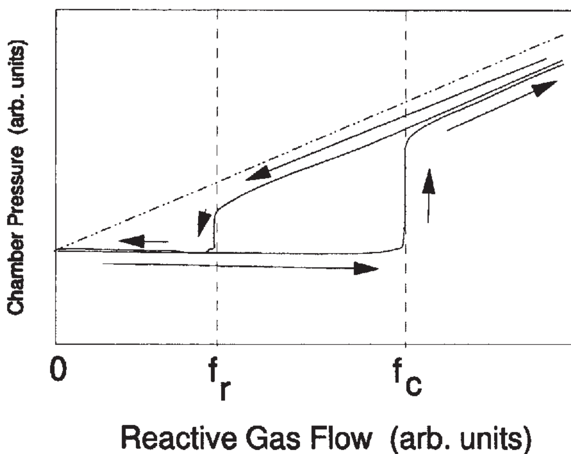


**Figure 13.** The chamber pressure for a reactive sputtering system as a function of increasing reactive gas flow. This figure relates directly to Fig. 12.

A second fundamental issue with reactive sputter deposition, particularly of oxides, is the formation of oxide, nonconducting films on the surface of the anode. In most cases the chamber walls function as the anode. As films are deposited around the chamber, eventually the anode becomes oxidized and current flow is reduced. The problem then often leads to arc formation, resulting in poor film quality and control. It is possible to hide the anode out of the line of sight of the deposition process, but even this eventually becomes oxidized in the background gas and residual deposition.

The nonreversible trend described above and shown in Figs. 12 and 13 present a real problem for the deposition of compound films at a reasonable rate. The best, fully reacted films are deposited at the knee of the curve, yet this point is unstable and difficult to control. There are several approaches to fixing this problem.

a. *Feedback control of reactive gas flow.* This is an obvious approach which monitors some parameter within the system (typically voltage or pressure) and controls the flow of reactive gas to try to operate just at the knee of the hysteresis curve. The most successful attempts have used "optical gas controllers" which are an optical equivalent to a mass spectrometer and are relatively inexpensive and fast. This feedback control process is applicable to small systems, but tends to fail with very large tools which have high substrate-to-wall ratios and poor pumping speeds.

b. *Increased pumping speed.* This technique is based on dramatically increasing the conventional pumping speed of the chamber such that the vast majority of the reactive gas simply goes down the pump port, rather than into the films. A classic experiment showed this effect, in which the hysteresis curve was flattened out by increases in flow and pumping speed at constant pressure.[12] This is shown in Fig. 14.

c. *Dual cathodes.* This technique uses two similar cathodes operated adjacent to each other in which the power is alternated to each cathode. Therefore, for part of each cycle one cathode functions as the cathode and the other cathode functions electrically as the anode, and then for the rest of the cycle, the functions are reversed. This has a dual advantage. First, since one cathode has

always just been sputter-etched during the last half cycle, there is always a fresh, unoxidized surface ready to function as the anode, reducing the probability of arcing. Second, the dual cathodes are less likely to permanently shift into the oxide or contaminated cathode mode than a single static cathode. This allows operation at the knee of the curve in a more stable fashion.

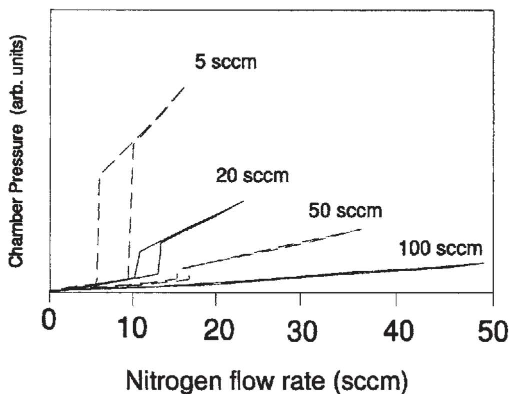


**Figure 14.** Hysteresis curves for reactive sputter deposition as a function of gas flow and pumping speed.[12]

*d. Gas pulsing.* Recently, several researchers have been able to demonstrate that, by pulsing the reactive gas flow into the system, they are able to control the sample oxidation process without allowing the cathode to oxidize. This keeps the cathode metallic and the deposition rate high. Gas pulsing can be thought of as an extreme case of feedback control of the gas flow (*a*).

*e. Sample/cathode separation.* For laboratory-scale deposition, it is often possible to physically separate the cathode and the sample region by grids, baffles, or simply distance, and inject the reactive gas at the sample location. The reactive gas then is mostly absorbed at the sample and little travels to the cathode region to cause it to change. This works well in small scale systems but is hard to scale up.

*f. Oscillating deposition-oxidation.* For a reasonably small sample, it is possible to physically move the sample rapidly between two chambers during deposition. In the first chamber, a thin layer of metal is sputtered down in the metallic mode. In the second chamber, this metal film is reacted by the presence of a reactive gas. This thin, reacted film is then inserted back into the sputtering chamber for another thin film of metal, which is then reacted back in the second chamber. This process can be easily realized in a segmented chamber by a simple rotating sample pallet (Fig. 15).

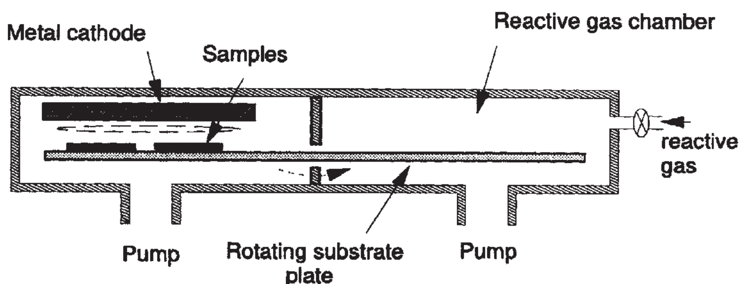


**Figure 15.** A two-chamber tool for the deposition *(left side)* and reaction *(right side)* of a compound film.

## 6.0 SPUTTERING SYSTEMS

Sputtering, whether with a simple diode or a magnetron diode, requires a working gas pressure in the mTorr to 1 Torr range. Most magnetrons are best operated at a few mTorr. In addition, due to the reactive nature of many freshly sputtered atom species, the residual or working gas needs to be fairly clean and often inert, such as Ar or Kr. Sputtering systems typically have a base pressure that is several orders of magnitude (at least two) below the operating pressure, and clean gas is introduced at the base pressure to bring the pressure up to the working level.

The choice of system design and pumping type depends on the application. Semiconductor manufacturing tools often use closed-cycle

cryopumps because they typically operate in Ar or mildly reactive (oxygen, nitrogen) partial pressures, which are safely accumulated in the pumps. From a practical point of view, cryopumps are also considered to last longer and have fewer maintenance problems than turbo pumps. For many other applications, turbo pumps or hybrid turbo-molecular-drag pumps are adequate, backed by oil-filled or dry mechanical pumps.

Sputtering systems are classified as either batch or single-sample systems, based on whether there are a large number of parts coated at the same time or just one at a time. Either type of system may have a load-lock entry port. The load-lock allows evacuation of the new part in a separate chamber, then entry into the main system under vacuum. This eliminates air exposure of the cathode and the clean chamber, resulting in faster attainment of the base pressure before a run.

*a. Batch systems.* A common design for a batch tool uses a fairly small cathode sitting over a large, rotating plate covered with a large number of samples (Fig. 16). The samples are passed under the active cathode and shields are used to help make the deposition more uniform. A permutation of this design would use planetary motion of the samples instead of simple rotation which would give better uniformity without shields.

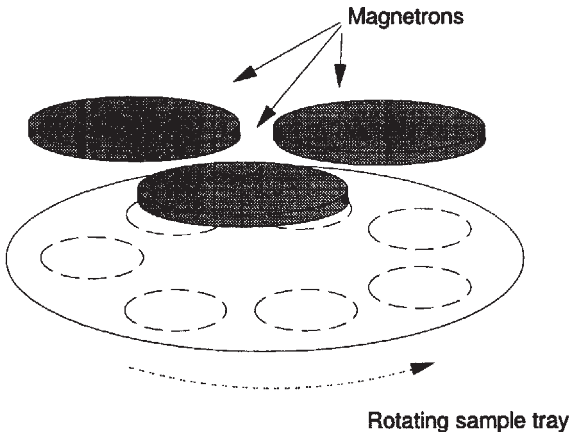


**Figure 16.** Perspective view of a 3-magnetron batch tool. The samples are situated on the plate which rotates under the magnetrons. Shields, not shown, may be placed underneath the magnetron to help with deposition uniformity.

(b) *Single-sample systems.* Two versions of this type are common, the linear system and the integrated-process tool. In the linear system (Fig. 17), samples are put into the system at one end on a pallet, they then pass in front of the sputtering cathode, and are removed either at the end or back at the starting point. This geometry uses rectangular magnetrons where the length of the magnetron is greater than the longest dimension of the part.

The integrated process tool (Fig. 18) uses a central handler which is under vacuum to pick up parts from the load-lock and distribute them to one of several chambers. Each chamber will have a valve that separates it from the central handler. This type of system is the workhorse of the semiconductor system, and the entire system as well as each individual chamber is highly automated for maximum thruput of wafers. More complicated versions of Fig. 18 use multiple stages of integration in which the front-end robot hands off the parts to a second robot which services the back end of the tool. A fully-equipped manufacturing tool of this type may have 6–9 chambers, and several of these chambers may also be used for processes other than sputter deposition.

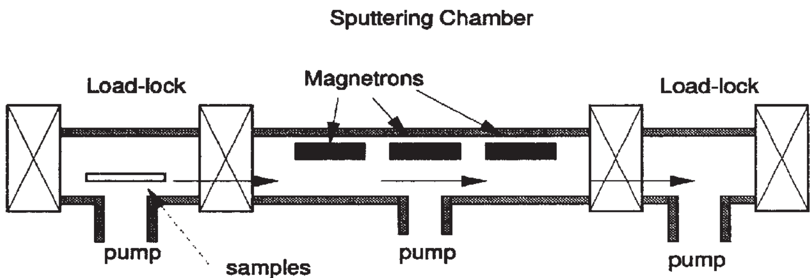


**Figure 17.** A linear, single-sample system with a load-lock and multiple sputtering cathodes.

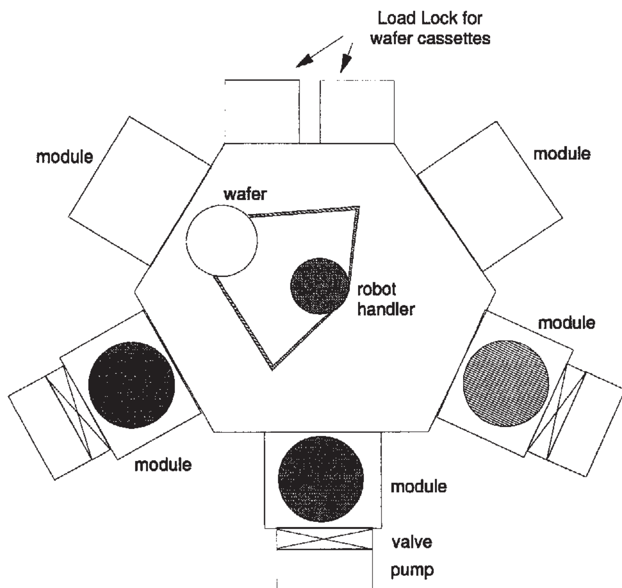


**Figure 18.** Integrated process deposition tool.

## 7.0 CONCLUSIONS AND FUTURE DIRECTIONS

Sputtering is widely used in semiconductor processing for metal and compound deposition. Physical sputtering is well understood and a wide variety of high deposition rate systems are available. Much of the current work in PVD technology areas is either in the area of applications, such as interconnection-wiring on semiconductors, or in the realm of materials, such as the development of high dielectric or piezoelectric films.

Several recent developments have helped extend PVD technology, including collimated sputtering, re-flow or high temperature sputtering and ionized magnetron sputter deposition or I-PVD. While these are not explored in this chapter, the reader is referred to Refs. 11–13 for background reading.

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# 9

# Laser and Electron Beam Assisted Processing

*Cameron A. Moore, Zeng-qi Yu,*
*Lance R. Thompson, and George J. Collins*

## 1.0 INTRODUCTION

The fabrication of submicron microelectronic devices in semiconducting crystals requires inducing a wide variety of physical and chemical processes. Epitaxy, oxidation, lithography, etching, ion implantation, and deposition all must be carried out with a high degree of process control and spatial uniformity. As device and feature sizes shrink below one micron, the inherent limitations of traditional furnace-based thermal processing methods become manifest. Foremost, we must reduce the total time-temperature cycling required to complete fabrication steps.[1] This reduction is motivated by the need to minimize thermal diffusion and its associated redistribution of as-implanted doping profiles, to reduce thermal defect creation and migration in the crystalline substrate, and to minimize thermally-induced substrate warpage as required by submicron lithography.

When fabricating submicron feature sizes, there is also a need to process materials with a minimum amount of process-induced radiation damage,[2] such as that found in plasma etching or deposition, electron or ion beam lithography, and ion implantation.

One way to exert a high degree of spatial and temporal control over the energy input to any processing step is through the use of directed energy beams which are created with both high energy selectivity and spatial directionality. Ion beams, for example, have long been used to implant dopant species with repeatable doses and specific depth profiles. The recent use of ion beam lithography and direct write pattern transfer has also shown promise.[3][4] Photon and electron beams have also long been used for lithography and analytical measurements (optical and scanning electron microscopy, ellipsometry, etc.).

Herein, we discuss recent progress in the application of photon beams (from laser sources) and electron beams (generated in an abnormal glow discharge) to semiconductor device fabrication. Specifically, we examine photon and electron beam assisted CVD of microelectronic films, electron beam induced annealing of ion implantation damage and associated dopant activation, electron beam induced alloying of silicide structures, self-developing electron beam proximity lithography of submicron features and traveling-melt photon and electron beam recrystallization of deposited polycrystalline silicon films on $SiO_2$.

Beam assisted process technology and the related equipment are in general still at an early development stage. However, this technology offers significant prospects for the future fabrication of microelectronic devices. The major advantages of the beam assisted technologies are based on:

- The high dimensional resolution capability.
- The ability to perform low temperature processes and to minimize the thermal exposure of the substrate.
- The ability to perform sequential process steps in-situ without exposing the substrate to the atmosphere, thus minimizing the risk of potential surface contamination and oxidation.

The different beam assisted processes and their characteristics are discussed in more detail in the following section.

## 2.0 BEAM ASSISTED CVD OF THIN FILMS

### 2.1 Conventional CVD Methods

The atmospheric or low pressure thermal CVD of microelectronic films occurs typically at 600 to 1000°C substrate temperatures (corresponding to thermal energies below 100 meV). Thermal CVD relies on high substrate temperatures and catalytic reactions between donor molecules and substrate surfaces to achieve the dissociation of feedstock gases with binding energies in the 1 to 3 eV range. As a consequence, thermal CVD deposition rates are low (100 to 1000 Å/min). One improvement over conventional thermal CVD techniques is plasma-enhanced chemical vapor deposition (PECVD). A plasma, while having a gas temperature of 10's of meV, contains energetic electrons with a distribution of energies which usually average several electron-volts. This plasma electron energy spectrum partially overlaps the electron-impact induced dissociation cross section maxima for many polyatomic feedstock reactants. Thus, the burden of feedstock gas dissociation is carried by the plasma electrons and one can deposit films on substrates at a temperature below 400°C.[5] PECVD processes can lower substrate temperatures and raise deposition rates (>1000 Å/min) because the reactants are more directly and efficiently dissociated. However, PECVD may introduce radiation damage and electrode or vacuum chamber impurities to the substrate and the growing film. Ions in the plasma act as a possible source of physical damage to the substrate or deposited film if the plasma sheath surrounding the substrate accelerates ions to greater than several hundred eV. Radiation damage from plasma electrons and photons is not as severe as that from ions and can be annealed out with a relatively low temperature anneal.[2]

### 2.2 Electron Beam Assisted CVD

The plasma used to deposit films can be an abnormal glow discharge.[6] The combination of the abnormal glow discharge operation together with the use of high secondary electron emissivity cathode materials results in a glow discharge-created electron beam.[7] Conventionally, gamma ($\gamma$) is used for the secondary electron emission coefficient, where $\gamma$ is the number of secondary electrons emitted from a cold cathode per incident ion. One can create an electron beam in an abnormal

glow DC discharge by using, for example, a ceramic-metal compound as a cathode with $\gamma$>2. The use of a thin oxide, nitride or oxynitride layer on a metallic cathode[7] can also result in a high $\gamma$. The cathodic voltage drop controls the electron beam energy. The cathode geometry determines the directionality of beam electrons because the plasma sheath conforms to the chosen cold cathode shape. Compared to conventional DC, RF, or microwave plasmas, the energy spectrum of the electrons created in these abnormal glow discharges has a much greater density of high energy electrons.[6][7] The presence of high energy electrons results in distinctive cracking patterns following electron-molecule collisions in electron beam created plasmas as compared to those found in conventional plasmas. By directing this electron beam into a mixture of feedstock gases, electron impact dissociation of gases occurs and film deposition results.

## 2.3 Laser Assisted CVD

We have used ultraviolet photons from an excimer laser source to photodissociate feedstock reactant molecules.[8] Photodissociation products then subsequently condense on a substrate as a solid film. The energy spectrum of the input laser beam is essentially monoenergetic as compared to electron-induced dissociation sources (conventional DC, RF, and microwave plasmas) which have statistical energy distributions of electron energies. Thus, laser driven photodissociation allows for fewer dissociation channels, better process repeatability and, in some cases, selective bond breakage. Laser-induced chemical vapor deposition (LCVD), unlike PECVD, also has the ability to localize the film deposition by use of simple optics to focus and direct the beam.

## 2.4 Experimental Apparati of Beam Assisted CVD

Laser-induced and electron beam-assisted CVD deposition reactors have many similar features. These apparati have been described previously[8][9] and are briefly reviewed here. The substrate upon which deposition is to occur is placed on a heater capable of temperatures from 50°C up to 450°C. Low substrate temperatures are desirable for submicron silicon processing as well as for processing materials which degrade at elevated temperatures (e.g., III-Vs, II-VIs and heavy metal-fluoride glasses). Once the desired substrate temperature is realized, feedstock gases containing the film precursors are introduced into the chamber. At the substrate

temperatures employed negligible thermal CVD occurs. Feedstock gas flow is monitored using mass-flow control valves, while the deposition pressure is selected via a conventional downstream throttle valve/ capacitance manometer control system. The electron or laser beam is then introduced either parallel or perpendicular to the substrate surface. A common feature of the parallel beam CVD technique is that the deposition-initiating particles, be they either electrons or photons, are directed near and above the substrate but do not impinge directly (except via scattering) upon the growing film. In this way, the film deposition occurs with reduced radiation damage as compared to perpendicular beam assisted CVD.

As shown in Fig. 1, the dissociation volume in beam CVD is well-defined spatially, as compared to a typical PECVD method in which the plasma fills the entire interelectrode and CVD reactor volume. Using LCVD techniques, both insulating ($SiO_2$, $Si_3N_4$, $AI_2O_3$, and AIN) and conducting (Mo, Cr, W, Al) films have been deposited, while EBCVD has been used to deposit silicon dioxide and silicon nitride. The electrical, optical, chemical and physical properties of beam deposited films (LCVD and EBCVD) are contrasted and compared below to those obtained by conventional methods.

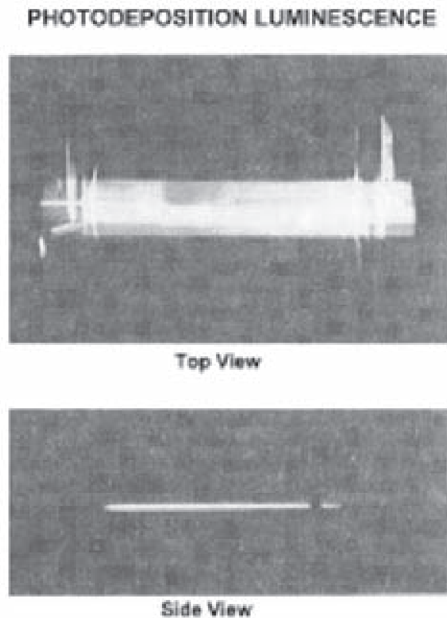



**Figure 1.** Photographs of laser CVD dissociation volume: *(top)* parallel to substrate, and *(bottom)* above substrate.

## 2.5 Comparison of Beam Deposited Film Properties

**Laser-Deposited Dielectric Films**. In Table 1, the typical deposition conditions for the laser assisted CVD of silicon-based insulating films are given. The laser, operating on a mixture of argon and fluorine, emits characteristic 193 nm photons. Tables 2 and 3 show comparisons of the properties of laser-deposited silicon dioxide and silicon nitride insulating films with these same materials deposited using conventional PECVD. The primary differences are that the LCVD films have increased incorporation of oxygen and carbon. This is attributed to the LCVD deposition system's poor vacuum base pressure (~1 mTorr) and inadequate backstreaming prevention in our initial vacuum system. Subsequent LCVD work by J. M. Jasinski at IBM has eliminated the C and O in $Si_3N_4$ films.[8]

**Table 1.** Deposition Conditions for LCVD of Silicon Dioxide and Silicon Nitride (ArF Laser Operating at 100 mJ/pulse, 100 Hz, 10 nsec/pulse)

| Deposition Parameters | Silicon Dioxide | Silicon Nitride |
|---|---|---|
| Substrate temperature (°C) | 380 | 380 |
| Gas flow ratio | $N_2O/SiH_4/N_2$:80/1/40 | $NH_3/SiH_4/N_2$:1/1/40 |
| Total pressure (Torr) | 6 | 2 |
| Deposition rate (Å/min) | 800 | 700 |

**Table 2.** Comparison of LCVD (Parallel Beam Configuration) and PECVD Silicon Dioxide Film Properties

| Film Property | Laser | RF Plasma |
|---|---|---|
| Impurities | | |
| Nitrogen (at.%) | <4 | 3 |
| Carbon (at.%) | <2 | <0.1 |
| Hydrogen bonding | | |
| 2270 $cm^{-1}$ SiH (%) | 2.3 | 2 |
| 3380 $cm^{-1}$ $H_2O$ (%) | ~0.01 | <0.001 |
| 3650 $cm^{-1}$ OH (%) | 0.6 | 0.002 |

*(Cont'd.)*

**Table 2.** *(Cont'd.)*

| Film Property | Laser | RF Plasma |
|---|---|---|
| Etch rate in 7:1 | | |
| Buffered HF (Å/s) | | |
| as deposited | 50–60 | 20 |
| After 60 min 950°C | | |
| $N_2$ anneal | ~18 | — |
| Dielectric strength (MV/cm) | | |
| (1000 Å on Si) | 6–8 | — |
| (2000 Å on Si) | — | 10 |
| Resistivity at 5 MV/cm (Ω-cm) | $10^{14}$ | $10^{16}$ |
| Dielectric constant at 1 MHz | | |
| Thermal oxide (3.9) | 4 | 4.6 |
| Pinholes (#/cm$^2$) | | |
| (2000 Å on Si) | ~1 | ~1 |
| Refractive index (6328 Å) | ~1.46 | 1.46 |

**Table 3.** Comparison of LCVD (Parallel Beam Configuration) and PECVD Silicon Nitride Film Properties

| Film Property | Laser | RF Plasma |
|---|---|---|
| Impurities | | |
| Oxygen (at.%) | 5 | <1 |
| Carbon (at.%) | 4 | <1 |
| Hydrogen bonding by FTIR | | |
| Si-H (%) | 12 | 12–16 |
| N-H (%) | 11 | 2–7 |
| Etch rate: (Å/sec; 5:1 BOE) | 20–50 | 1.7 |
| Refractive index (6328 Å) | 1.85 | 2 |
| Density (g/cm$^3$) | 2.4 | 2.8 |
| Breakdown voltage (MV/cm) | 2.5 | 4 |
| Resistivity at 1 MV/cm (W-cm) | $10^{14}$–$10^{15}$ | $10^{15}$–$10^{16}$ |
| Dielectric constant at 1 MHz | 7.1 | 7 |

Hydrogen incorporation, which is at similar levels for both methods, arises both from incomplete dissociation of feedstock gases as well as subsequent hydrogen-bearing free radical reactions. The high hydrogen content, which increases porosity of the film, can be remedied by subsequent thermal annealing as the etch rate comparison in Table 2 indicates. Alternatively, the impingement of laser radiation on the deposited film during deposition will also reduce the hydrogen content,[10] especially SiH and SiOH bondings. In the parallel beam technique, a high degree of film thickness uniformity can be achieved[11] because a wide area planar source is initiating the film deposition. This is easily appreciated if one considers the geometries of several possible deposition schemes where the source and substrate are separated by a distance $R$. A point source of species (e.g., evaporation) exhibits a $1/R^{[2]}$ (spherical) deposited film thickness uniformity dependence; whereas a line source provides a $1/R$ (radial) dependence on the uniformity of film deposition. With a uniform planar source of large area the deposited film uniformity shows no dependence on the source distance $R$ since the total species flux from the beam dissociation volume averages to a conditionally fixed value. For this reason, superior vertical step coverage is obtained using the parallel beam assisted CVD technique.[11] In Fig. 2, an example of conformal step coverage of LCVD $SiO_2$ is shown. In summary, silicon-based insulating films deposited using laser-induced CVD have properties which are comparable to those obtained in a plasma-enhanced deposition scheme.

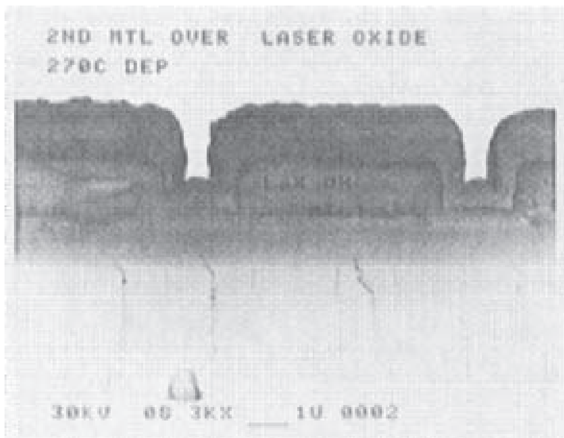



**Figure 2.** Step coverage of LCVD silicon dioxide.

Aluminum-based LCVD dielectric films are compared to sputtered alumina[12] and thermal CVD AIN[13][14] in Tables 4 and 5 respectively. The refractive index and electrical resistivity of LCVD alumina films are improved with increasing substrate temperature.[15] The LCVD alumina films deposited with substrate temperatures of 400°C compare well to RF sputter-deposited films with respect to the AI:O ratio, the dielectric constant, and the pinhole density. However, the LCVD films refractive index is slightly lower and the resistivities are an order of magnitude smaller.

**Table 4.** Comparison of LCVD Alumina Films (Parallel Beam Configuration) With RF Sputtered Films

| Film Property | LCVD (400°C) | RF Sputtered[11] (150°C) |
|---|---|---|
| Al:O ratio | 0.69* | 0.68** |
| Impurities | C<1%* | Ar<5%** |
| Deposition rate (Å/min) | 2000 | 200 |
| Adhesion (dynes/cm$^2$) | >6.5 × 10$^8$ | Strongly adherent |
| Pinhole defects | <1 in 5 cm$^2$ (thickness = 1500Å) | 31/cm$^2$ (thickness = 2500 Å) |
| Stress (dynes/cm$^2$) | <6 × 10$^9$ (tensile) | 2.8 × 10$^9$ (compressive) |
| Refractive index | 1.63 | 1.66 |
| Etch rate in 10% HF (Å/min) | 100 | — |
| Resistivity (Ω-cm) | 10$^{11}$ (@ 1 MV/cm) | 10$^{12}$ (@ 2.6 MV/cm) |
| Dielectric constant (@ 1 MHz) | 10.2 | 9.96 |

* XPS
** RBS

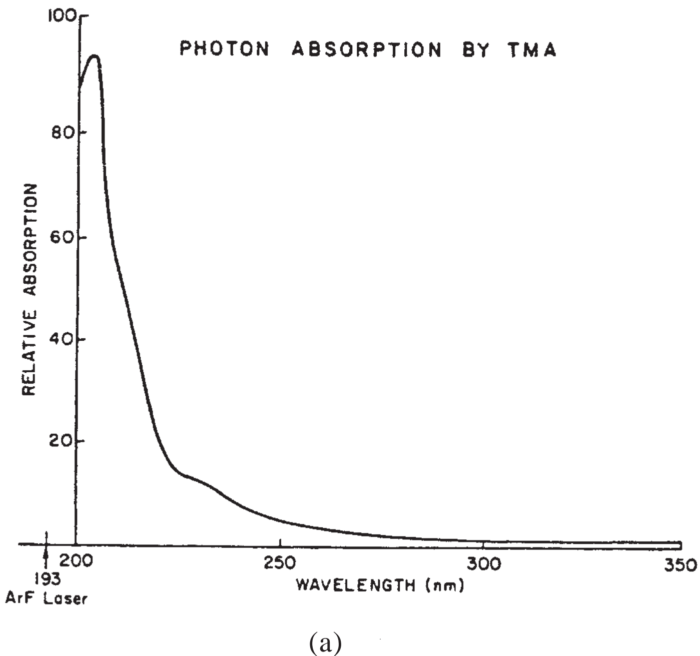
**Table 5.** Comparison of LCVD Aluminum Nitride Films (Parallel Beam Configuration) With TCVD (Thermal CVD) and RF Sputtered Films

| Film Property | LCVD (450°C) | TCVD[12][13] (800–1200°C) | RF[15][16] Sputtering (<450°C) |
|---|---|---|---|
| Impurities | | | |
| Carbon | <5%* | <1%** | <1%* |
| Oxygen | <10%*** | <5%** | <5%* |
| Refractive index (@ 6328 Å) | 1.95 | 2.05 | 2.0–2.1 |
| Electrical resistivity (Ω-cm @ 1.5 MV/cm) | $10^{15}$ | $10^{15}$ | $10^{15}$ |
| Dielectric strength (MV/cm) | 3–5 (@ 1 μA/cm$^2$) | 5–10 | 6–10 |
| Dielectric constant (@ 1 MHz) | 6–8 | 8.1–8.8 | 8.1–9.3 |

* ESCA
** Elecron Microprobe
*** RBS

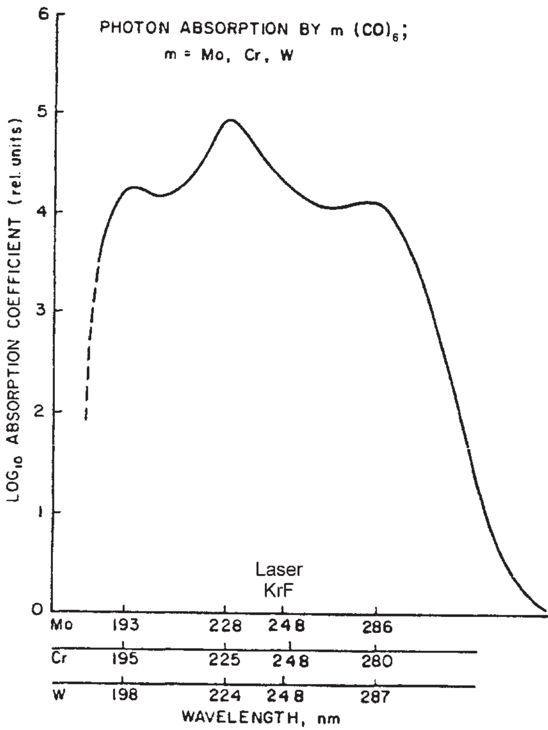
The LCVD AIN films deposited at a substrate temperature of 200°C have substantial amounts of oxygen, hydrogen (bonded as N-H and O-H), and carbon. The hydrogen and oxygen content of the AIN films decreases with increasing substrate temperature. Table 5 summarizes properties for LCVD AIN films deposited at the highest substrate temperature used (450°C). The LCVD AIN film properties of refractive index, dielectric constant and electrical resistivity approach those values reported for thermal CVD films deposited at 800 to 1000°C[13][14] and RF sputter-deposited AIN films.[16][17][18] The LCVD films are lower in dielectric strength and dielectric constant[15] but contain up to 5% oxygen.

**Laser-Deposited Metallic Films**. One can also deposit conducting films simply by changing the gas mixture in the chamber used for laser-deposited insulating films. The feedstock gases used for aluminum and refractory metal (Mo, Cr, W) deposition were trimethyl aluminum and the hexacarbonyls of the refractory metals [e.g., $Mo(CO)_6$]. In order that the photon wavelength would better match the donor gases' photon absorption cross section, a KrF laser operating at 248 nm was used for depositing the refractory metal films. Donor gases photodissociation cross sections vs wavelength are shown in Figs. 3 (a, b); the laser wavelengths used are also indicated.[19][20] Conducting films of molybdenum, tungsten, chromium and aluminum, deposited by photo-driven reactions in the volume, possess electrical resistivities within a factor of 2 to 8 of bulk values.[8] Properties of these LCVD metallic films appear in Table 6. Residual carbon and oxygen incorporation limits the electrical resistivity of the deposited films.




(a)

**Figure 3.** Relative photodissociation cross sections for conducting film donor gases vs photon wavelength. Laser wavelengths used are also indicated. (*a*) Trimethyl aluminum[19] (*b*) Refractory metal hexacarbonyls.[20]




(b)

**Figure 3.** *(Cont'd.)*

**Table 6.** The Properties of LCVD Metallic Films Deposited Using UV Photons From Excimer Laser

| Metal Film | Dep. Rate (Å/min) | Resistivity (Ω-cm) Bulk | Resistivity (Ω-cm) Film | % C in film (ESCA) | Adhesion to Quartz (dynes/cm²) | Tensile Stress (dynes/cm²) |
|---|---|---|---|---|---|---|
| Mo | 2500 | 5.2 | 36 | <0.9 | >5.5 × 10⁸ | <3 × 10⁹ |
| W | 1700 | 5.6 | 40 | <0.7 | >6.5 × 10⁸ | <2 × 10⁹ |
| Cr | 2000 | 12.9 | 56 | <0.8 | >5.4 × 10⁸ | <7 × 10⁹ |
| Al | 500 | 2.6 | 9 | <7.0 | >5.5 × 10⁸ | <1 × 10⁹ |

**Electron-Beam Deposited Dielectric Films**. An abnormal glow discharge created electron beam can be injected into feedstock gases to dissociate them via electron-molecule collisions. The electron beam may be placed just above and parallel to the substrate or directed to impinge perpendicular to the substrate; for either case of electron beam assisted CVD (EBCVD), acceptable film properties result. Clearly, in the parallel beam technique electron radiation damage can be minimized as compared to the case of perpendicular arrangement. Physical damage by kilovolt electrons is less severe than that caused by ions of several hundred volts,[21] such as those present in conventional plasmas. Because the discharge voltages used (and hence, the maximum electron energies) are less than 3 kV, electron-induced damage can be annealed out with a low temperature heat treatment (<450°C) following deposition.[2][22]

Using both electron beam configurations (parallel and perpendicular), films of silicon dioxide and silicon nitride were deposited and the deposition conditions are summarized in Table 7. Note that while EBCVD creates films at a lower reactor pressure than PECVD the deposition rates are approximately the same or higher than those of PECVD. This is thought to occur because of the closer match under EBCVD conditions between the electron energy distribution and the electron impact dissociation cross section of the donor gases; this yields more efficient production of free radicals from the feedstock polyatomic gases following electron impact.

**Table 7.** Deposition Conditions for EBCVD of Silicon Dioxide and Silicon Nitride

| Process Variable | Silicon Dioxide | Silicon Nitride |
|---|---|---|
| Substrate temperature (°C) | 350 | 400 |
| Gas flow ratio | $N_2O/SiH_4/N_2$:75/1/75 | $NH_3/SiH_4/N_2$:60/1/44 |
| Total pressure (Torr) | 0.25 | 0.35 |
| Deposition rate (Å/min) | 500 | 200 |
| Discharge parameters | 4.7 kV, 16 mA/cm$^2$ | 2.3 kV, 13 mA/cm$^2$ |

The properties of $SiO_2$ films deposited with the electron beam directed parallel to and above the substrate are given in Table 8 and are compared with conventional PECVD films. While the index of refraction and the resistivity are comparable, the EBCVD films are inferior with respect to wet chemical etch rate (up to 3 times higher) and pinhole density (10 times higher). These shortcomings are most likely due to film porosity (which is a manifestation of the high deposition rate) and low deposition temperature (which causes a low surface mobility of adsorbed species).

**Table 8.** Comparison of EBCVD Silicon Dioxide Films (Parallel Beam Configuration) and PECVD Deposited Films

| Film Property | Electron Beam | RF Plasma |
|---|---|---|
| Impurities | | |
| Nitrogen (at.%) | <1 | 3 |
| Carbon (at.%) | <2 | 0.1 |
| Hydrogen bonding | | |
| 2270 $cm^{-1}$ SiH (%) | <1 | 2 |
| 3380 $cm^{-1}$ $H_2O$ (%) | <0.001 | <0.001 |
| 3650 $cm^{-1}$ OH (%) | <0.01 | 0.002 |
| Etch rate in 7:1 | | |
| Buffered HF (Å/sec) | 30–60 | 20 |
| Adhesion ($10^8$ dyne/$cm^2$) | | |
| (1000 Å on Si) | >7 | >7 |
| Pinholes (#/$cm^2$) | | |
| (2000 Å on Si) | 10 | ~1 |
| Refractive Index (6328 Å) | 1.46 | 1.46 |
| Stress ($10^9$ dyne/$cm^2$) on Si compressive | 9.4 | 3.6 |
| Dielectric strength (MV/cm) | 2.6* | 10** |
| Resistivity at 1 MV/cm (Ω-cm) | $10^{14}$–$10^{16}$ | $10^{16}$ |
| Dielectric constant at 1 MHz [For comparison: Thermal oxide (3.9)] | 3.5 | 4.6 |

* 1000 Å on Si
** 2000 Å on Si

Films of silicon nitride (nitrogen rich oxynitride) were also deposited via the parallel electron beam-substrate geometry.[23] Silicon nitride films so deposited were also rich in hydrogen bonded to Si. When the EBCVD deposition geometry was altered, so that the beam electrons impinged directly upon the growing film, the Si-H bonding decreased well below (a factor of 20) that of the parallel EBCVD method. The hydrogen bonded to nitrogen level is nearly the same in PECVD, parallel EBCVD, and perpendicular irradiated EBCVD films. The shortcomings of the EBCVD silicon nitride films, as shown in Table 9, were the same as found in the EBCVD silicon dioxide (increased wet chemical etch rates and high pinhole densities). The high (13%) oxygen content of the silicon nitride films is judged to be due to two sources: primarily the poor base vacuum in the EBCVD reactor and secondly the much higher chemical reactivity of silane and associated free radicals ($SiH_2$, etc.) with background oxygen/water as compared to that with ammonia and its associated free radicals ($NH_2$, etc.)

**Table 9.** Comparison of EBCVD Silicon Nitride Films (Perpendicular Beam Configuration) With PECVD Deposited Films

| Film Property | Electron Beam | RF Plasma |
|---|---|---|
| Impurities | | |
| Oxygen (at.%) | 13 | <1 |
| Carbon (at.%) | <0.1 | <1 |
| Hydrogen Bonding by FTIR | | |
| Si–H (%) | <0.1 | 12–16 |
| N–H (%) | 8–10 | 2–7 |
| Etch rate (Å/sec; 5:1 BOE) | 3 | 1.7 |
| Adhesion ($10^8$ dyne/cm$^2$) | | |
| (1000Å on Si) | >5.5 | >6 |
| Pinholes (#/cm$^2$) (1000Å on Si) | 5–100 | 2–3 |
| Refractive index (6328 Å) | 1.87 | 2 |
| Dielectric strength (MV/cm) | 5 | 4 |
| Resistivity at 1 MV/cm (Ω-cm) | $10^{15}$ | $10^{15}$–$10^{16}$ |
| Dielectric constant at 1 MHz | 7 | 7 |

A central concern of any deposition method is its ability to uniformly cover large area substrates (≥ 15 cm dia.). The above EBCVD system deposits films with 4% uniformity over a 100 mm diameter substrate provided two conditions are met: *(1)* the cold cathode diameter is several centimeters larger than the substrate, and *(2)* the reactant gas flow was uniformly introduced into the reaction volume as shown in Fig. 4. A plot of the spatial uniformity of the deposited film is shown in Fig. 5.

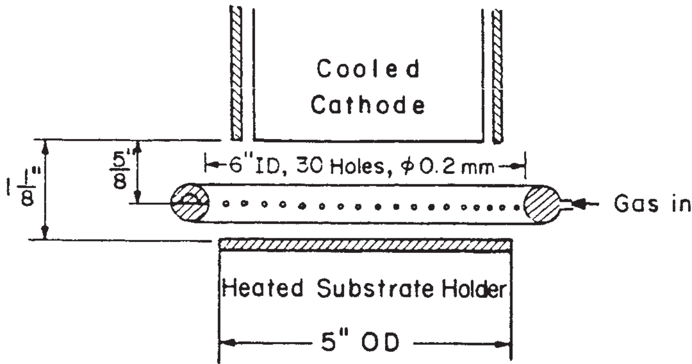



**Figure 4.** Technique of gas introduction in EBCVD to obtain high deposition uniformity.

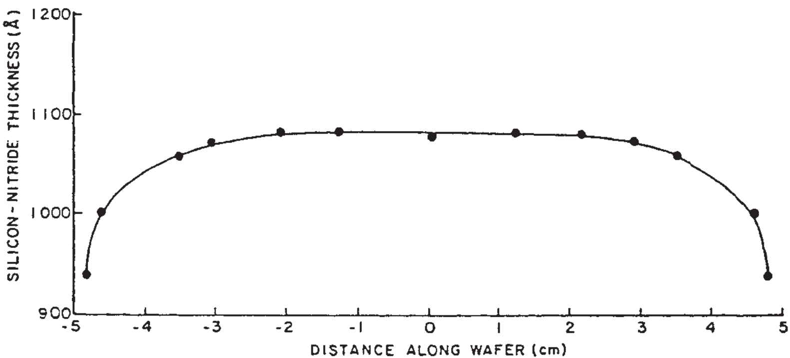



**Figure 5.** Deposition uniformity EBCVD silicon nitride on 100 mm wafer.

It is unlikely that EBCVD will displace conventional PECVD batch wafer processing, but it may have application as wafer dimensions increase to 20 centimeters in diameter and film fabrication becomes more oriented toward single-wafer (non-batch) in-line processing. Applications requiring a low Si-H content $Si_3N_4$ film would be well served by perpendicular EBCVD methods.

## 3.0 SUBMICRON PATTERN DELINEATION WITH LARGE AREA GLOW DISCHARGE PULSED ELECTRON-BEAMS

The fabrication limit of optical lithography is just under 0.75 µm, while x-ray lithography may be applied to feature sizes smaller than 0.5 µm.[24] Optical methods lack the sub-half micron replication capability of electron beam technology while x-ray lithography suffers from registration limits. Both these methods provide larger wafer throughput and better cost effectiveness than serial direct-write electron-beam lithography.

Direct write electron-beam lithography has two serious drawbacks: low wafer throughput and high equipment cost. Recently, we proposed a new method of implementing wide area electron-beam proximity lithography which eliminates the ultra-high vacuum constraint on the e-beam source.[25][26][27] The method proposed uses electrons produced in an abnormal glow discharge operating at 100 mTorr ambient[28] and preliminary experiments showed that adequate electron beam collimation to replicate feature sizes down to 5 µm is possible.[29] The glow discharge electron-beams not only exposed polymer resists such as PMMA but also self-developed these polymer resists. For those polymer resists which did not self-develop completely, we used subsequent wet or dry development to complete the process.

The glow discharge electron beams can be produced in either the CW or pulsed mode. High voltage pulsed beams in soft vacuum were found to be capable of fully self-developing submicron pattern delineation.[30] A typical experimental set-up is shown in Fig. 6. A 25 kV pulsed electron-beam, produced by discharging as little as 2.5 J of stored energy in 50 mTorr of helium or air, could replicate feature sizes 0.5 mm wide in 3.0 µm thick PMMA as shown in Fig. 6.

The chosen gaseous environment had a marked effect on the resist sidewall characteristics (see Fig. 7). While resist exposed in helium showed vertical wall profiles (developed resist thickness is 3 μm), resist exposed in air (Fig. 7b) showed sloped (~60°) walls. It is probable that by judicious mixing of these and other process gases, we can more fully control the wall profile.

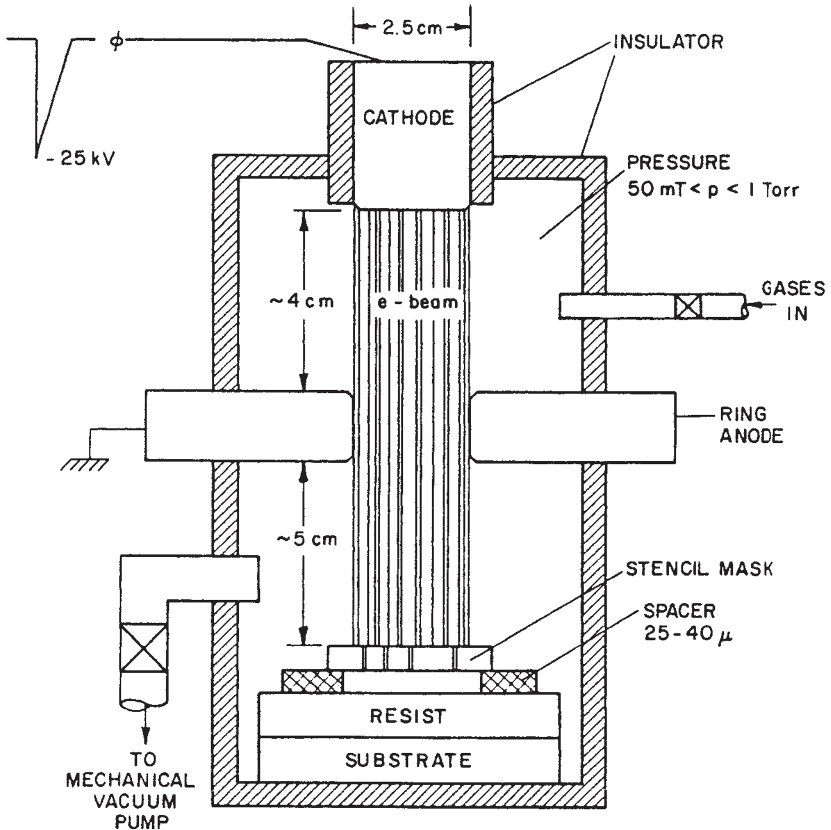
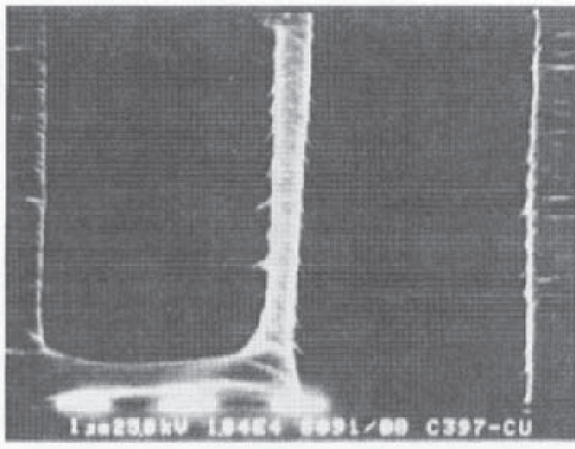



**Figure 6.** Electron beam proximity lithography system.




(a)

(b)

**Figure 7.** Submicron self-developed replication on PMMA: (*a*) in a helium ambient; (*b*) in an air ambient.

The outstanding features of this soft vacuum electron beam process may be summarized as: an electron beam operating in the soft vacuum pressure region (50 mTorr to 1 Torr); large area exposure (>50 cm$^2$) allowing for large field size, peak beam currents ($I_{peak}$ > 100 A) allowing for self-development and in combination high wafer throughput. The short exposure time (1 µsec) and self-development capability makes it a contender to self-development methods employing energetic proton beams[31][32] or excimer laser beams.[33] Using proper resists optimized for the electron beam self-development process, these investigations could lead to a totally dry lithographic technique with submicron replication capable of operating around 1 Torr ambient pressure. The major drawback of wide area proximity electron beam lithography is the high cost and fragile nature of the required transmission masks.

## 4.0 BEAM INDUCED THERMAL PROCESSES

### 4.1 Overview

The application of heat to a semiconductor wafer can induce thermal processes such as annealing, alloying, and dopant diffusion. Conventional furnace-based thermal treatment is performed on 50 to 200 wafers per batch. Furnace processes, however, require initiation and termination times of one-half hour or more to ramp the wafers up to and down from the chosen process temperature. One can reduce the time-temperature cycling to which wafers are subjected and still achieve desired results,[34] provided one still reaches the threshold thermal energy input required to activate the physical processes. Independent of the heat source used, semiconductor annealing requires that the threshold temperature be induced only for milliseconds to seconds to achieve dopant activation and crystal lattice repair. One of these rapid thermal processing techniques is transient electron beam heating.[35][36][37]

To explore transient heat treating of four inch diameter wafers in a single exposure a large area (5 inch diameter) abnormal glow discharge electron beam was constructed. The wide area electron beam source, which is capable of radiating a power density of up to 120 watts/cm$^2$ at 4 to 8 keV continuously in an ambient of 0.1 to 1.0 Torr of helium, is shown schematically in Fig. 8. It consists of a flat cold cathode made from a metal-ceramic of high secondary emission material (MgO-Mo). Electron emission

occurs only from the front circular cathode surface because the remainder of the cathode structure is surrounded by a quartz shield. The MgO cathode component provides for high secondary electron emission following plasma ion bombardment while the molybdenum provides structural support and electrical conductivity. This wide area electron beam created in a glow discharge was used to anneal ion implant damage in single crystal silicon, and was also applied to the beam induced formation of silicide films.

In a later section, we will also compare laser and electron beam induced traveling-melt recrystallization of polysilicon deposited on four inch wafers. This purely thermal process consists of locally melting an area of the deposited polysilicon film followed by propagation of this melt front across the entire wafer surface. Progress in the application of both a scanned point source $Ar^+$ laser beam and an extended line-source electron beam to this SOI (silicon on insulator) process are contrasted and compared.

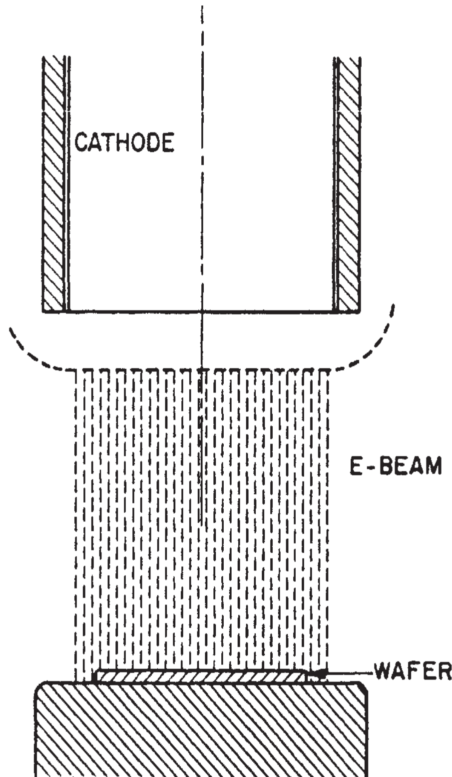



**Figure 8.** Large area electron beam annealing system.

## 4.2 Electron Beam Annealing of Ion-Implanted Silicon

To achieve the controllable introduction of dopant atoms into a semiconductor lattice at predetermined depths, dopant ions are accelerated and subsequently implanted in a thin region near the surface. The drawbacks of ion implantation are that: *(1)* the ions can displace lattice atoms (and in other ways disrupt lattice periodicity); and *(2)* that only a fraction of the implanted species come to rest on substitional (electrically active) lattice sites. Both lattice damage and interstitial dopants adversely affect carrier mobility and minority carrier lifetime in the crystal unless remedied by a post-implant oven anneal at temperatures up to 1000°C. These elevated temperatures, together with the required oven ramp cycles of one-half hour or more, cause dopants to diffuse away from the original as-implanted concentration profile during the oven anneal. This thermal redistribution becomes incompatible with the requirements of submicron VLSI processing when diffusion lengths become comparable to device dimensions. To reduce diffusion lengths, thermal anneals of shorter duration are required since the required threshold anneal temperature cannot be reduced.

The ability of a large-area abnormal glow discharge electron beam to rapidly anneal damage in crystalline silicon and activate dopants was ascertained in the following way. Boron, phosphorus, and arsenic ions were implanted into 8 to 21 ohm-cm <100> silicon wafers; in all cases, the substrate doping was opposite to that of the implanted species. Normalized sheet resistivity, $\rho_A/\rho_B$, Was the parameter used to judge the extent of annealing. This ratio of sheet resistance before and after annealing minimizes geometry-dependent errors such as sample size and preanneal spatial doping variations. Samples with each implant species were annealed with increasing electron beam power densities until the $\rho_A/\rho_B$ stabilized at a low value. Figure 9 shows the $\rho_A/\rho_B$ versus beam power for various anneal times. Implant types and doses as well as varying implantation energy are also noted. The electron beam-induced process is capable of performing the anneal in a short time-high temperature manner.

The diffusion of the implanted species during transient beam annealing was examined using secondary ion mass spectrometry. In Fig. 10, the electron beam-induced diffusion of boron implants in silicon is compared to the as-implanted profile and to that of a conventional furnace anneal. The ion implant and anneal conditions are noted in the figure. This shows that the electron beam can both repair the silicon lattice damage and activate dopants without appreciably altering the original as-implanted dopant profile.

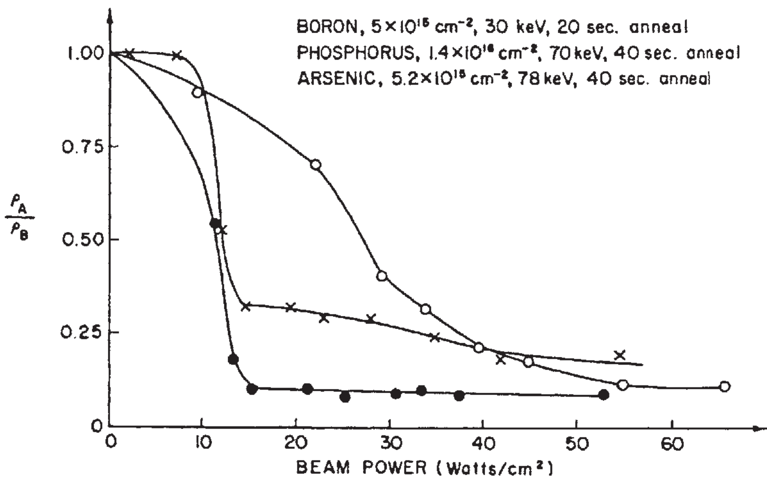



**Figure 9.** Normalized sheet resistivity vs beam power for boron, phosphorus, and arsenic ion implants in silicon. Implant and anneal conditions are noted.

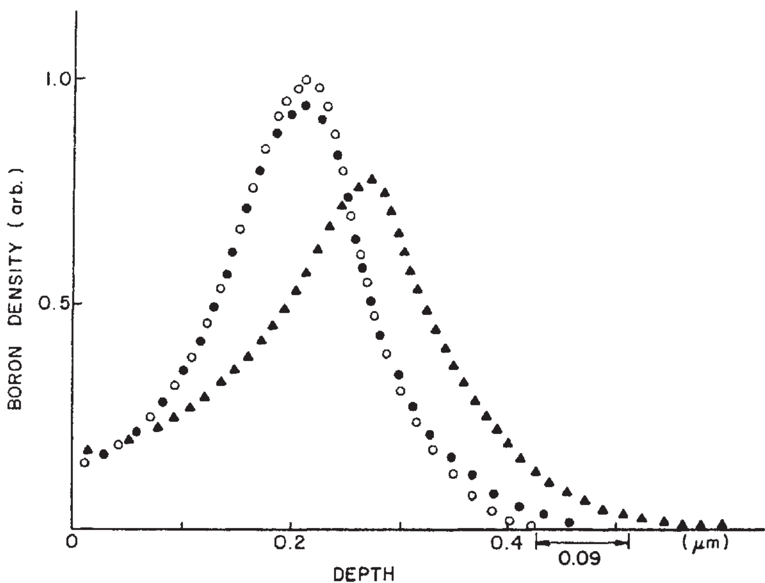



**Figure 10.** SIMS profiles of as-implanted, electron beam annealed and furnace annealed boron implanted silicon. The depth profile of $B^+$ implanted in silicon (o: as implanted; ●: E-beam annealed at 3.5 keV, 25 MA/cm$^2$ for 40 seconds; ▲: furnace annealed at 960$^o$C for 30 minutes).

## 4.3 Electron Beam Alloying of Silicides

Reactions of metals with silicon in the solid phase at elevated temperatures can form silicides, a set of materials whose properties are attractive for use as gates, contacts and interconnects in submicron VLSI fabrication. Silicides may be formed either by annealing of codeposited metal-silicon solid solutions or via interdiffusion of deposited metal films on silicon. In our work described below, tungsten and titanium silicides have been formed using transient exposure to an abnormal glow discharge electron beam as the process-driving heat input.

The starting materials were formed on <100> n-type silicon wafers by either: *(1)* sputter deposition of a 400 Å thick layer of Ti on bare Si or *(2)* PECVD of 1600 Å thick Ti-Si or W-Si films (of overall stoichiometry $TiSi_2$ or $WSi_2$) onto silicon wafers previously thermally oxidized to a thickness of 1000 Å. The wafers were then cleaved into smaller samples for ease of comparison of processing results. Prior to processing, Ti on Si samples had average sheet resistivities of 21 ohm/sq, the codeposited $TiSi_2$ had 10 ohm/sq, the codeposited $WSi_2$ had 40 ohm/sq. The $\rho_A/\rho_B$ values versus beam power for these materials are shown in Fig. 11.

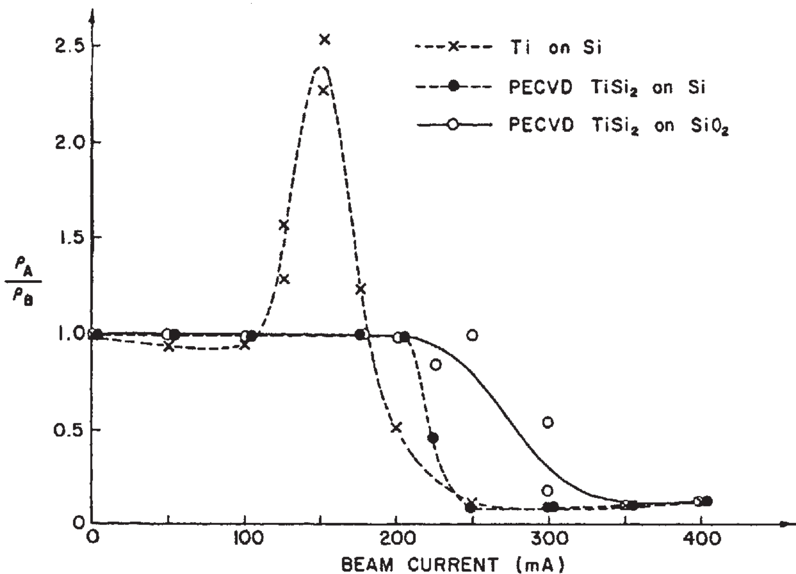



**Figure 11.** Normalized resistivity vs beam power for titanium silicide formation.

For beam-induced interdiffusion of titanium and silicon layers (Fig. 11), the $\rho_A/\rho_B$ increases from 1 to 2.5 before reaching its ultimate value of 0.1 (which corresponds to a bulk resistivity of approximately 20 µohm-cm). This effect was not observed for codeposited $TiSi_2$ which were electron beam alloyed. An explanation for this has been offered previously.[37][38] The spatial uniformity of the electron beam processing was examined by electron beam irradiating where codeposited $TiSi_2$. While the wafer and the cathode are both 7.5 cm in diameter, it was observed that only the central 5.5 cm of the wafer undergoes uniform heating due to the inhomogeneous beam energy profile. Hence, the glow discharge electron beam source must be larger than the sample under process if wafer edge effects are to be avoided.

For electron beam induced alloying of $WSi_2$, the temporal nature of electron beam-induced silicide growth was examined. This was done by measuring the $\rho_A/\rho_B$ as a function of beam exposure time for constant beam power densities of 75 and 100 W/cm$^2$. This is shown in Fig. 12. At the higher beam power a low resistivity film is obtained after about 20 sec., while the lower beam power requires >100 sec. to reach a similar sheet resistivity. In either case, the ultimate film resistivity obtained is 125 µohm-cm, about 2 to 3 times the bulk value; most likely due to oxygen incorporation from the $SiO_2$ underlayer via chemical reduction.[39]

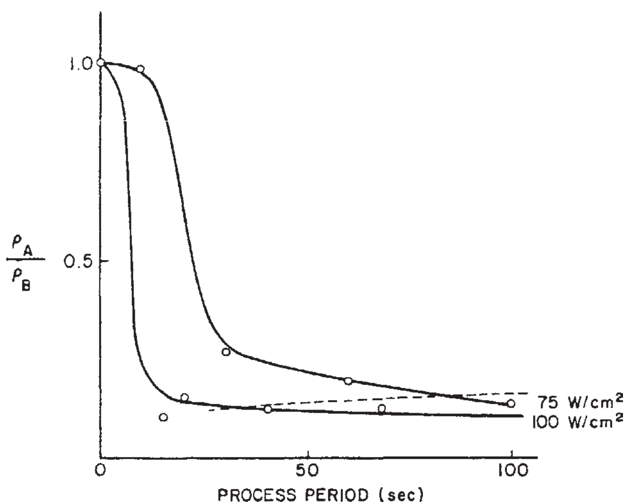



**Figure 12.** Temporal development of normalized resistivity during electron beam formation of tungsten silicide.

## 4.4 Laser and Electron Beam Recrystallization of Silicon on $SiO_2$

Processing microelectronic materials using either electron or photon beams can enable fabrication of structures which are either more costly or not possible to achieve using conventional processing methods. One such example is silicon-on-insulator (SOI) technology, in which one creates a thin crystalline silicon film which is dielectrically isolated from the underlying silicon substrate by a layer of $SiO_2$. The advantages of SOI over bulk silicon are that the devices and circuits in SOI layers have reduced parasitic capacitances (allowing faster circuit operation), increased radiation hardness (due to a thin active layer) and elimination of CMOS latch-up from undesired substrate currents. SOI may also make possible the vertical stacking of MOS devices (three-dimensional integration).

One of the most practical SOI fabrication techniques is traveling-melt recrystallization,[40] where a directed heat source locally melts a deposited polycrystalline film; an encapsulating film layer prevents beading of the silicon while it is molten. This molten zone of polysilicon is then propagated across the substrate. Upon contact of the molten silicon with the single crystal substrate, one is able to seed the resolidifying polysilicon film. This traveling-melt front technique is contingent on having a beam heat source capable of heating the silicon to its melting point (1415°C), a requirement which is met both by finely-focussed point source laser beams as well as wafer-size line source electron beams generated in abnormal glow discharges as described below.

A CW argon ion laser may focus to a spot approximately 40 µm in diameter. The beam is then raster-scanned over an entire SOI wafer surface containing periodic seed structures to melt and recrystallize the polysilicon film. The process is capable of creating 12 µm wide by 3 mm long SOI islands with carrier mobilities approaching bulk values.[41] A novel bilayer lateral CMOS structure was created as shown in Fig. 13. This structure is inherently latch-up free. Laser induced traveling melt recrystallization most likely will not be incorporated into a manufacturing environment because to process one 100 mm diameter wafer with a scanned point source laser beam requires about 20 minutes. One practical alternative is to form a wafer size optical line source via lamps or lasers which can be swept across the upper polysilicon film. However, the total optical power required in such a laser source has not been achieved to date and lamp sources are limited to very slow propagation velocities (≤ 1 mm/sec).

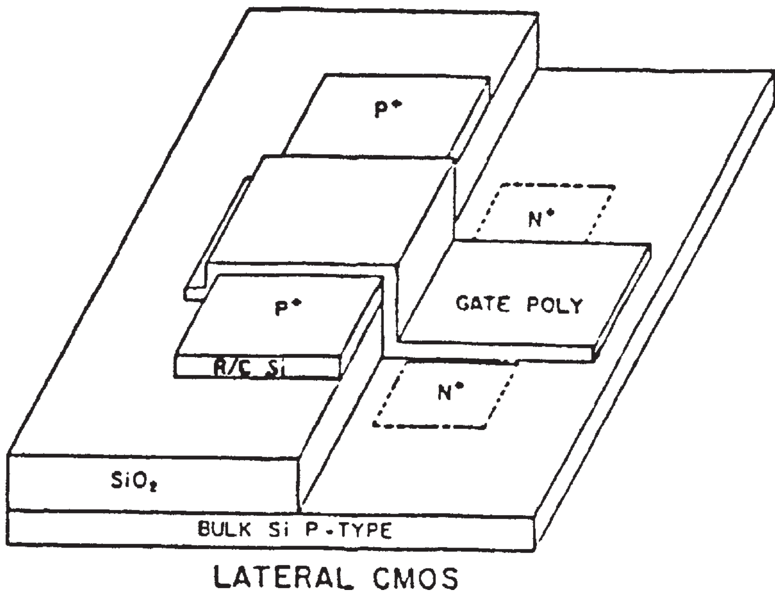



**Figure 13.** Bilayer lateral CMOS structure.

Toward this goal of line source recrystallization[42] we have developed a glow discharge created electron beam. Our 15 cm long line source cathode is capable of generating a multi-kilowatt line beam of ±1% intensity uniformity which extends across a 10 cm diameter wafer. This source allows for wafer scan velocities up to 10 cm/sec and still achieves melt zone formation during the short beam dwell time.[43] Using this method of line source recrystallization, single wafer SOI wafer process times are from 10 to 100 seconds. An optical microphotograph of line source recrystallized[43] silicon which has been decoratively etched is shown in Fig. 14; a few grain boundaries can be seen. With substrate seeding the grain boundaries can be either spatially localized or eliminated.[42] Seeding to the underlying crystalline substrate provides both a preferred crystal orientation as well as a heat sink to create required thermal gradients between seed locations. Unseeded growth is desirable since wafer preparation is greatly simplified (because no lithographic definition is required), but this will require some other method of controlling grain boundary locations.[40]

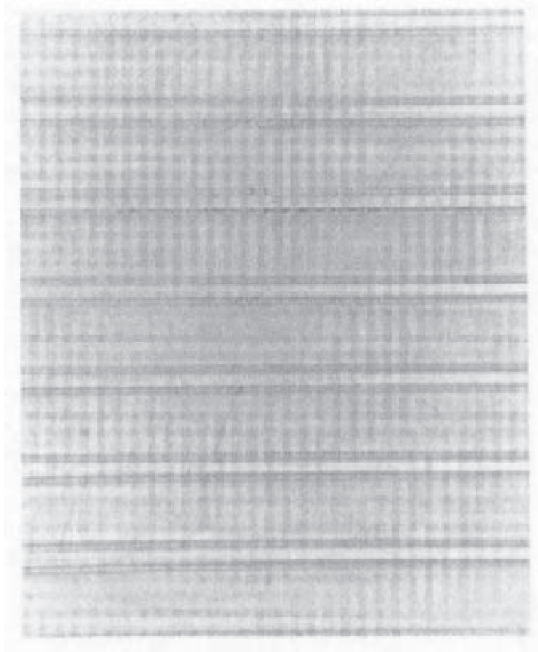


**Figure 14.** Optical micrograph of line-source recrystallized silicon.

## 5.0 SUMMARY AND CONCLUSIONS

The work described herein has demonstrated that photons from a laser are capable of photo-dissociating gaseous reactants whose photofragments can condense and/or react to form microelectronic films. Likewise, an abnormal glow discharge with an enhanced density of high energy electrons is capable of assisting chemical vapor deposition. In either case of beam assisted CVD, the films obtained are generally comparable to those deposited by conventional thermal and plasma-enhanced methods. Relative advantages and disadvantages of beam deposited films are outlined.

Beams of electrons and photons have also been used to induce some purely thermal processes, namely implant damage annealing, silicide alloying, and traveling-melt beam recrystallization. Ion implant damage in crystal silicon substrates can be annealed via transient electron beam exposure obtaining a high degree of electrical activation while minimally

redistributing the original as-implanted dopant profiles. In a similar fashion, silicides of tungsten and titanium have been formed via electron beam initiated processes and silicide resistivities obtained approach bulk values. In either case, uniform treatments are possible if the beam diameter exceeds the wafer size. Electron beam proximity lithography is shown to self-develop submicron feature sizes in PMMA. Finally, laser and electron beams can be used to locally zone-melt a polysilicon film deposited on an insulating $SiO_2$, film which itself is grown on a crystalline silicon substrate. Via seed holes in the isolation $SiO_2$ go through to the crystalline substrate. When molten polysilicon is deposited, it contacts the solid substrate seed and forms a single crystal silicon island with little or no grain boundary defects.

In conclusion, photon and electron beam-induced processes have been shown to have applications to highly controlled spatial and temporal material fabrication. Whether or not these beam assisted techniques will better fulfill the needs of submicron VLSI circuit manufacture better than conventional or other alternative methods is not yet resolved.

## ACKNOWLEDGEMENTS

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# 10

# Molecular Beam Epitaxy: Equipment and Practice

*Walter S. Knodle and Robert Chow*

*Molecular beam epitaxy* has experienced extremely rapid growth over the last ten years. During this time, the publication rate of technical articles has increased by an estimated order of magnitude reflecting the growing application of the MBE process. Similarly, the number of researchers has grown concomitantly with the technology, and a large MBE community has established itself with various specializations according to materials and devices. This large and growing body of research knowledge has advanced and redefined the hardware which, in turn, has assisted further advances in process development. The entry level scientist is often faced with the formidable task of collecting the hardware familiarity and process foundation necessary to begin MBE research. It is the authors' intent in this chapter to present a broad coverage of the present status of the MBE process and equipment, not dwelling in depth on any one aspect, but instead presenting key references to classic and current articles on important topics. By supplying timely leads to the work of leading researchers, we hope to advance the learning curve of those using this source as a starting point. We sincerely hope that the reader finds this goal achieved.

Two texts worth mentioning as a general reference are: *Molecular Beam Epitaxy,* (B. Pamplin, ed.), Pergamon Press, 1980; and *The Technology and Physics of Molecular Beam Epitaxy,* (E. Parker, ed.), Plenum Press, 1985. There are also regularly published proceedings of value from: the MBE Workshop and the International Conference on MBE (both in the *Journal of Vacuum Science and Technology*), the International Symposium on Gallium Arsenide and Related Compounds, and the IEEE GaAs Integrated Circuit Symposium.

## 1.0 THE BASIC MBE PROCESS

Although the basic process of MBE, ultrahigh vacuum evaporation, had been in practice long before, it was not until the works of Arthur[1] and Cho[2] that a fundamental understanding of the process as applied to compound semiconductor growth evolved. Using mass spectrometric and surface analytical techniques, they studied the film growth process of gallium arsenide at the atomic layer level. Their work set the stage for equipment design specific to UHV epitaxial film growth. Subsequently, Chang et al.,[3] and others further advanced the process toward what we recognize today as MBE. The foundation of MBE is rooted in surface analysis and in understanding on an atomic level the nature of epitaxial film growth. Several reviews are of historical and technical significance; for instance, see Cho and Arthur,[4] Chang and Ludeke,[5] Foxon and Joyce,[6] Wood,[7] and Kunzel.[8] MBE equipment development still reflects the strong influence of its surface analytical beginnings. Subsequent advances in equipment design were made by Luscher and Collins[9] and others. The development of new and higher performance devices using MBE has advanced its commercial value. Present trends, reflecting the evolution of MBE from basic research to device production, are redefining and refining the equipment for specific material and device requirements.

A functional schematic of a MBE system is shown in Fig. 1. It consists of a growth chamber and auxiliary chamber (not present with first generation systems) and a load-lock. Each chamber has an associated pumping system. The load-lock facilitates the introduction and removal of samples or wafers without significantly influencing the growth chamber vacuum. The auxiliary chamber may contain supplementary surface analytical tools not contained in the growth chamber, additional deposition equipment, or other processing equipment. Separating equipment in this

manner allows for more efficacious use of the growth chamber and enhances the quality of operations in both the auxiliary and growth chambers.

The growth chamber is shown in greater detail in Fig. 2. Its main elements are: sources of molecular beams; a manipulator for heating, translating and rotating the sample; a cryoshroud surrounding the growth region; shutters to occlude the molecular beams; a nude Bayard Alpert gauge to measure chamber base pressure and molecular beam fluxes; a RHEED (reflection electron diffraction) gun and screen to monitor film surface structure; and a quadrupole mass analyzer to monitor specific background gas species or molecular beam flux compositions.

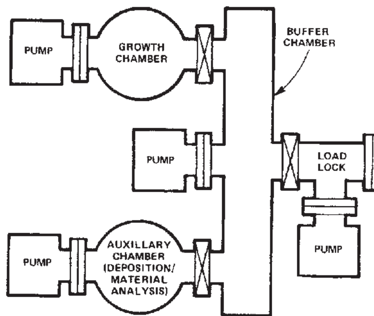



**Figure 1.** Functional schematic of a basic MBE system.

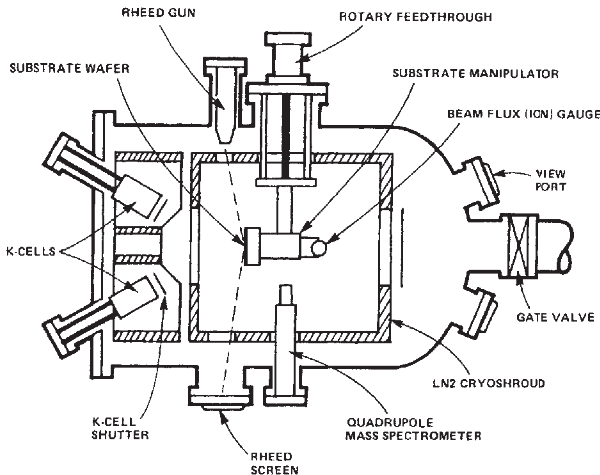



**Figure 2.** Schematic cross-section of a typical MBE growth chamber.

The auxiliary chamber may be host to a wide variety of process and analytical equipment. Typical surface analytical equipment would be: an Auger electron spectrometer, or equipment for secondary ion mass spectrometry (SIMS), ESCA (electron spectroscopy for chemical analysis) or XPS (x-ray photoelectron spectroscopy). There may be a heated sample station and an ion bombardment gun for surface cleaning associated with this equipment. Process equipment may include sources for deposition or ion beam etching.

The MBE growth process involves controlling, via shutters and source temperature, molecular and/or atomic beams directed at a single crystal sample (suitably heated) so as to achieve epitaxial growth. The gas background necessary to minimize unintentional contamination is predicated by the relatively slow film growth rate of approximately one micron per hour and is commonly in the $10^{-11}$ Torr range. The mean free path of gases at this pressure and in the beams themselves is several orders of magnitude greater than the normal source-to-sample distance of about 20 cm. Hence, the beams impinge unreacted on the sample with a cryoshroud cooled by liquid nitrogen. Reactions take place predominantly at the sample surface where the source beams are incorporated into the growing film. Proper initial preparation of the sample will present a clean, single crystal surface upon which the growing film can deposit epitaxially. Timely actuation of the source shutters allows film growth to be controlled to the monolayer level. It is this ability to precisely control epitaxial film growth and composition that has attracted the attention of material and device scientists. Some further reviews of the basics of MBE are: Cho,[10] Luscher,[11] and Panish.[13]

Most MBE research has been performed with elements from Groups III and V of the periodic table (i.e., Al, Ga, In, As, P, and Sb) but much significant work has also been achieved with silicon and germanium, II-VI anti IV-VI compounds and various metals. New milestones in material structures have been attained because of MBE leading to the development of semiconductor devices heretofore difficult or impossible to fabricate and to the invention of entirely new materials[13] and devices previously not imagined. Most of the attention in this review will focus on III-V materials because of their pervasive use in microwave and optoelectronic communication; high speed digital and analog devices; and integrated circuits. Referral to other material systems is given, where appropriate, with references to assist the reader in initiating his (her) own literature search.

## 2.0 COMPETING DEPOSITION TECHNOLOGIES

While MBE has afforded the fabrication of material and device structures not previously possible, many of the early milestones in compound semiconductor growth were attained using other epitaxial film growth techniques. Bench marks for purity and device performance remain valid today. These alternative deposition technologies can be loosely grouped into liquid phase epitaxial (LPE) and vapor phase epitaxial (VPE) processes. A special category of VPE known as OMVPE (organometallic VPE) or MOCVD (metal-organic chemical vapor deposition) has promise as a production worthy process. Each of these epitaxial processes has distinct advantages and disadvantages discussed below. A comparison of GaAs epitaxial processes is shown in Table 1.

**Table 1.** Comparison of Epitaxial Technologies

| | | Vapor-phase epitaxy | | |
|---|---|---|---|---|
| | Liquid Phase Epitaxy | Chemical Vapor Deposition | Metal Organic CVD | Molecular Beam Epitaxy |
| Growth rate (μm/min) | ~ 1 | ~ 0.1 | ~ 0.1 | ~ 0.01 |
| Growth temperature (°C) | 850 | 750 | 750 | 550 |
| Thickness control (Å) | 500 | 250 | 25 | 5 |
| Interface width (Å) | ≥50 | ~ 65 | < 10 | <5 |
| Dopant range ($cm^{-3}$) | $10^{13}$–$10^{19}$ | $10^{13}$–$10^{19}$ | $10^{14}$–$10^{19}$ | $10^{14}$–$10^{19}$ |
| Mobility, 77 K ($cm^2$/Vs) (n-type GaAs) | 150,000–200,000 | 150,000–200,000 | 140,000[a] | 160,000[b] |

[a] Nakanisi, T., Udagawa, T., Tanaka, A., and Kamei, K., *J. Cry, Growth,* 55:255 (1981)

[b] Larkins, E. C., Hellman, E. S., Schlom, D. G., and Harris, J. S., Jr., *Appl. Phys. Lett.* (to be published)

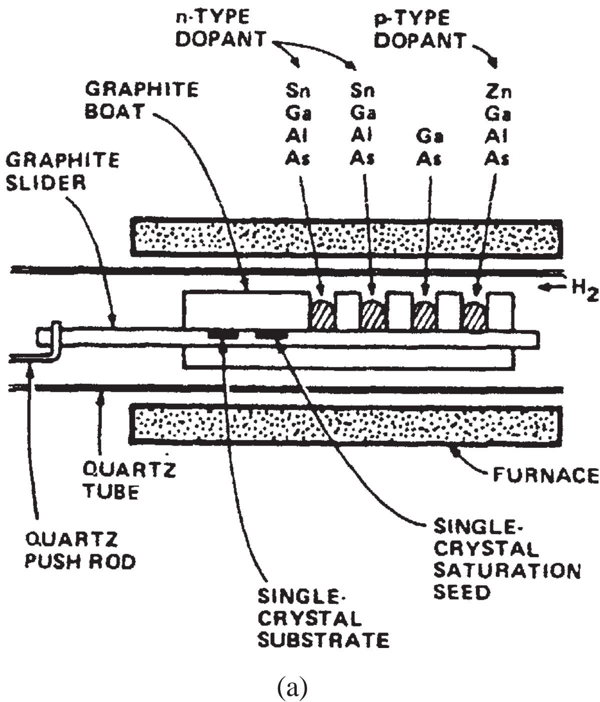
## 2.1 Liquid Phase Epitaxy

Historically, the early compound semiconductor growth was performed using liquid phase epitaxial techniques and many optoelectronic devices are still fabricated using this process. The threshold current values of the best double heterostructure (DH) MBE lasers are typically compared to LPE results. There are several variants of the LPE process, but in the approach most common to multilayer film growth a graphite holder slides a sample between melts of differing composition. A schematic of a graphite slider LPE system is shown in Fig. 3(*a*). The temperature and melt composition determine the stoichiometry and deposition rate. Film growth results from the controlled cooling of the supersaturated melt. Different bins are required for each layer of differing alloy composition. A thorough knowledge of the alloy phase diagram is necessary to accurately control the film composition. Weighted amounts of impurities are added to the melts to control doping. Dopants with relatively high distribution coefficients are not easily controlled.

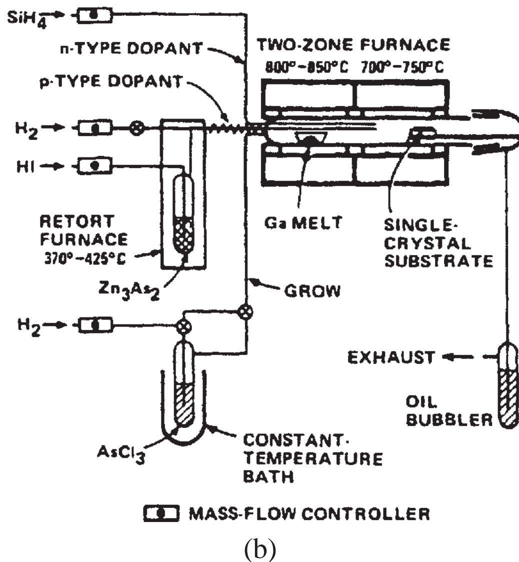
LPE has the advantages of low capital cost, high deposition rates, high material purity, no toxic gases and a relatively wide selection of dopants. Some disadvantages are: an inability to produce abrupt (monolayer) interfaces and poor large area uniformity; and difficulty in varying stoichiometry and controlling the reproducibility of ternary III-V compounds. Advances in LPE equipment have allowed superlattice structures of 200–300 Å thick layers to be produced. (Benchimol, et al.).[14] Despite such progress LPE is not considered amenable to high volume automated manufacturing.

## 2.2 Vapor Phase Epitaxy and MOCVD

Vapor phase epitaxy (VPE) of III-V compounds can be accomplished with different chemistries: hydride, halide or organometallic. The halide and hydride systems are common to the silicon semiconductor industry where epitaxial films are routinely deposited by the hydrogen reduction of chlorosilanes or the pyrolytic decomposition of silane. Gallium arsenide is deposited by passing $AsCl_3$ (with a hydrogen carrier gas) over molten gallium held at 800°C. The resulting gallium chloride and arsenic react at the cooler (700°C) substrate surface to deposit GaAs. Figure 3(*b*) shows a III-V chloride-based VPE system. The reaction chamber is a hot-wall quartz tube. In this diagram, zinc is the p-type dopant. The most limiting disadvantage of III-V halide VPE is the absence of a suitable chemistry for the deposition of aluminum. The deposition of aluminum-bearing compounds such as AlAs, AlGaAs, and AlGaInP can, however, be accomplished using MOCVD.

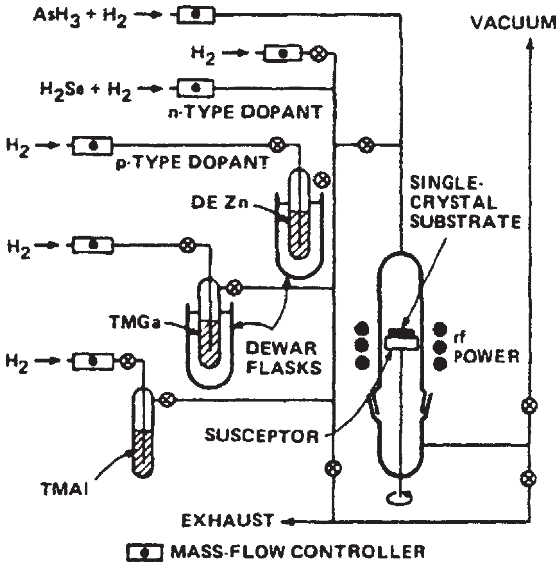



(a)

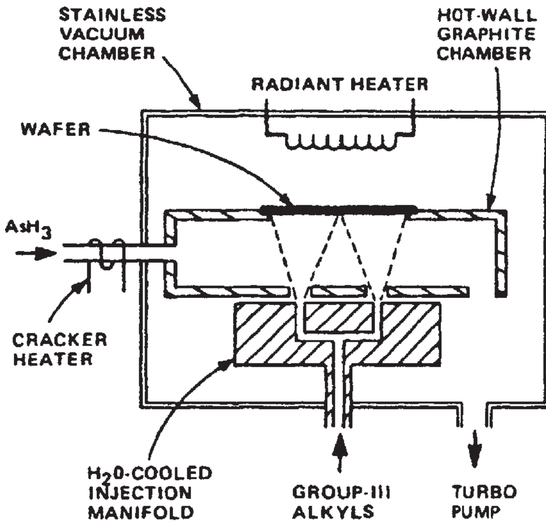



(b)

**Figure 3.** Alternative epitaxial processes: (*a*) liquid phase epitaxy, (*b*) vapor phase epitaxy (halide), (*c*) metal-organic chemical vapor deposition, and (*d*) vacuum chemical epitaxy (see Sec. 7.3).




(c)




(d)

**Figure 3.** *(Cont'd.)*

Hydride VPE is similar to the halide process and shares virtually identical hardware. Gallium chloride is created by the reaction of HCl gas with molten gallium. Arsenic, generated by cracking arsine, is mixed with a hydrogen carrier gas. The same disproportionation and reduction reactions occur at the heated substrate as in the halide process.

MOCVD offers the most competitive alternative to MBE of the epitaxial film processes. Figure 3c shows a vertical reactor employing trimethylgallium, trimethylaluminum, and arsine. All gases are mixed with a hydrogen carrier gas. The organometallics are contained in temperature-controlled bubblers. The sample is heated inductively inside a quart reaction tube (cold wall system) by external RF coils. In either example, the deposition takes place at or near the heated (550–750°C) sample surface by pyrolysis. Gas phase parasitic reactions and adduct formation can seriously complicate some growth processes. Growth rates between 1 and 10 microns per hour are common and excellent surface morphology has been demonstrated. A full metallorganic process would use a Group V organometallic compound in place of a hydride. For example, trimethylarsine would replace arsine. See Table 1 for a comparison of epitaxial technologies for the deposition of GaAs. Recent developments in MOCVD have allowed researchers to deposit thin (<100 Å) alternating layers with abrupt interfaces. Computer control of gas flows is necessary for high quality superlattice growth. Although film purity and thickness uniformity have been difficult to control, recent progress has been made in improving the quality of starting gases and achieving good thickness and doping uniformity (~ ± 5% and ±10%, respectively) across a three-inch wafer. Triethyl compounds have produced material with lower carbon contamination than the trimethyls.[15] One serious disadvantage of MOCVD is the toxicity of the gases required. In addition, some of the less toxic gases are pyrophoric. Expensive safety precautions are required for operating personnel and to reduce environmental liabilities.

While still inferior in terms of absolute thickness and doping control, MOCVD is considered to be a viable alternative to MBE for many devices. See, for instance, Andre, et al.[16] There has been much recent progress in the development of this still relatively young process. Many structures that at one time were only considered possible using MBE have recently been fabricated using MOCVD. See Takakuwa, et al.,[17] and Razeghi, et al.[18] Interestingly, the advent of low pressure MOCVD and metal-organic MBE (MOMBE) is bringing both process regimes closer together.

Atomic layer epitaxy (ALE) by hydride[19] and metallorganics[20] and molecular layer epitaxy (MLE)[21] are recent variations of the VPE process that allow sufficient growth control for superlattice structures. While MBE is still superior in terms of growth control, MOCVD has good potential to provide high throughput.[22] However, there are serious safety considerations associated with adopting any process requiring arsine and/or phosphine.

MOCVD is not confined to III-V compounds. Chemistries exist for the deposition of II-VI and IV-VI compounds as well. A review of MOCVD is included in Ch. 4 of this handbook. Further references are presented in *Gallium Arsenide Technology,* Ch. 3, (D. K. Ferry, ed.) Howard W. Sams & Co. (1985) and in *Semiconductors and Semimetals* (W. T. Tsang, ed.), Vol. 22, Part A, Ch. 3, Academic Press (1985).

## 3.0 MBE-GROWN DEVICES

Although much of the initial MBE research was directed toward the study of surface film growth kinetics, the driving force today is the fabrication of advanced electronic and optoelectronic devices. As the film growth capabilities of MBE became clear, researchers began producing a wide variety of heretofore impossible and unimagined devices. Some of these devices have subsequently been fabricated using other epitaxial techniques, but many were initially conceived in MBE systems. The advantages of generally lower growth temperature and growth rate allow MBE to produce atomically abrupt heterojunctions and doping profiles. The ability to produce these composition variations with material systems of inherently high electron mobility (i.e., GaAs, InP, InGaAs) has permitted the fabrication of very fast devices. Microwave devices with operating frequencies near 100 GHz[23] and high speed digital switching near 5 picoseconds[24] have been achieved. Also, the control of contact layers has reduced parasitic resistances, significantly improving FET performance (e.g., MAG and NF). The ability of MBE to deposit epitaxial metal layers in situ promises to permit the construction of a metal base transistor.[25] The fact that several material systems (e.g., GaAs/AlGaAs) are also optically active allows for the possibility of integrating high speed digital and optical circuits. Recent progress in the growth of GaAs on silicon further increases the options by promising to combine the virtues of these two semiconductor technologies in a monolithic device. MBE silicon devices are discussed in an article by K. L. Wang.[26]

Since it is not the intent of the authors to discuss devices per se, we limit ourselves to three examples relevant to MBE growth: the high electron mobility transistor (HEMT), the heterojunction bipolar transistor (HJBT or HBT), and the multiquantum well (MQW) laser. Tables 2 through 5 catalog many of the MBE grown devices and circuits.

**Table 2.** MBE Grown Transistors

HEMT, MODFET, SDHT, TEGFET, HFET[31]
- Inverted HEMT[32]
- Low-noise HEMT[33]
- GeSi MODFET[34]
- MIS-HFET[35]

HBT[36][49]
- Strained-Layer[37]
- GaAs on Si[38]

HET, MGT[39][40]

MESFET; LOW NOISE[41]–[43]
- POWER[41][44][45]

BIFET (Buried-Interface FET)[46]

TEBT (Tunneling Emitter BT)[47]

BICFET (Bipolar Inversion Channel FET)[48]

**Table 3.** MBE Grown Microwave Devices

IMPATT[52]–[54]

MIXER[55]–[57]

GUNN[58]

VARACTOR[51][56]

**Table 4.** MBE-Grown Optoelectronic Devices*

LASER**

- DFB: Distributed Feedback
- DH: Double Heterostructure
- DBDH: Double Barrier DH
- GRINSCH: Graded-Index Separate Confinement Heterojunction
  - BH: Buried Heterostructure
- MQW: Multi-Quantum Well
- TJS: Transverse Junction Stripe
- SCH: Separate-Confinement Heterostructure

LED:

PHOTODETECTOR:

- APD: Avalanche:
  - Superlattice
    - Ge(x)Si(1-x)/Si Strained-Layer[62]
  - Graded-gap
  - Channeling
- GeSi Waveguide:[63]

SEED: Self Electro-optic Effect Devices[64]

SOLAR CELL:[65]

* A comprehensive review of MBE and III-V optoelectronic devices is given by Tsang, in: *Semiconductors and Semimetals* (W. T. Tsang, ed.), Vol. 22, Part A, Ch. 2, Academic Press (1985).

** See Norton, et al.,[66] and Partin, et al.,[67][68] for IV-VI lasers.

**Table 5.** MBE Based Integrated Devices/Circuits

Analog ICs

- 115 GHz Oscillator[71]
- HBT Voltage Comparator[72]

Digital ICs

- HEMT Ring Oscillator[24][73][74]
- I-HEMT Ring Oscillator[75]
- HBT ICs[76]
- 2-Stage Complementary Inverter[77]
- Quantum-Well CCD[78]
- 1 kb SRAM[79]
- 4 kb SRAM[80]

OEICs

- LED/Amplifier[81]
- Photoreceiver[82]–[84]
- Transmitter/receiver[85]
- Laser/FET[86]

Optical IC*

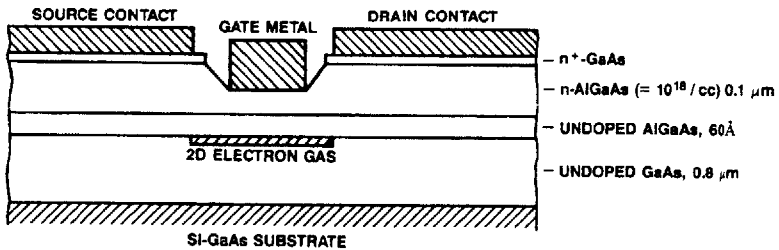
- Optical Switch[87]
- Laser Taper Coupler[88]
- Laser/waveguide[89]

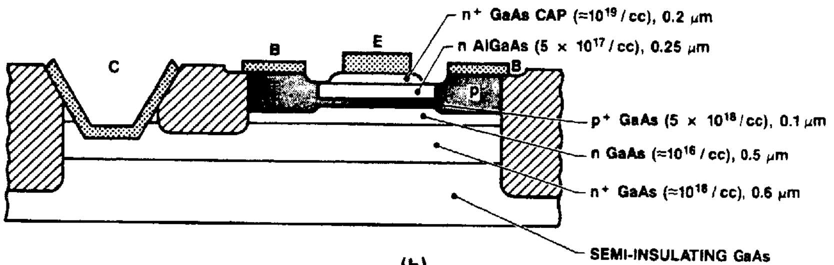
* See Burnham, R. D., and Scifres, D. R., Integrated Optical Devices Fabricated by MBE, in: *Prog. Crystal Growth Charact.,* 2:95 (1979); and Conwell, E. M., and Burnham, R. D., Materials for Integrated Optics: GaAs, *Ann. Rev. Mater. Sci.,* 8:135 (1978).

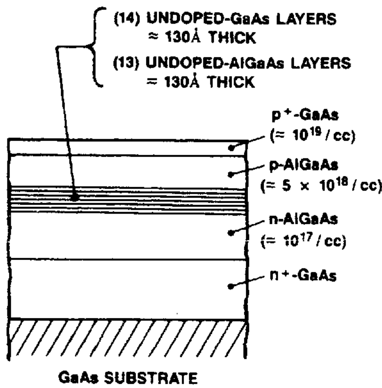
## 3.1 Transistors

The transistor, both as a digital switch and as an amplifier, has been key to the development of MBE. Table 2 summarizes the variety of MBE grown transistors. Of particular significance is the high electron mobility transistor (HEMT) The HEMT is often referred to by a number of synonyms such as: MODFET (modulation doped FET), SDHT (selectively-doped heterojunction transistor), and TEGFET (two-dimensional electron gas FET). It is a major force behind making MBE a production-worthy process because of its extremely fast switching speed and potential use in supercomputers.[27] Switching speeds near 5 picoseconds and speed-power products of 10 femtojoules have been demonstrated.[24] The HEMT is responsible in large part for the dwindling interest in Josephson junction devices. Its foundations are an outgrowth of superlattice and modulation doping structures made by Dingle, et al.,[28] and later evolved into the first practical device by Mimura[29] and Hiyamizu.[30] Its performance advantage is due to the separation of ionized donors and charge carriers. Electrons (holes) diffuse from a setback doped layer and are captured in the narrow potential well created at the heterojunction (see Fig. 4a). Room temperature mobilities in this two-dimensional layer can approach $10^4$ $cm^2$/Vsec for electrons. HEMT performance is also assisted by in situ MBE grown contact layers which contribute to reduced source and drain parasitic resistances. Reproducible structures require clean, atomically smooth heterojunctions, accurate setbacks, and repeatable doping levels. Several variations of the HEMT have been explored: the inverted HEMT, the double heterojunction HEMT, and the superlattice HEMT.

Another important transistor is the heterojunction bipolar transistor (HBT). A cross section is shown in Fig. 4b. Since the charge carriers flow vertically in the HBT, device speed is controlled by layer thickness, unlike the FET where the flow is lateral and critical distances are lithographically determined. This fundamental difference implies a potentially higher frequency operating limit for HBTs. HBTs also possess the very desirable characteristic of greater process margins, because turn-on voltages are determined almost entirely by the base material bandgap. Thickness uniformity is thus less critical than compositional reproducibility. In the case of the graded-base HBT, MBE allows the bandgap energy (composition) to vary continuously. MBE's potential to accurately control composition, layer thickness, and doping with superior across-the-wafer uniformity makes it ideally suitable for heterojunction bipolar transistor and IC production. MBE



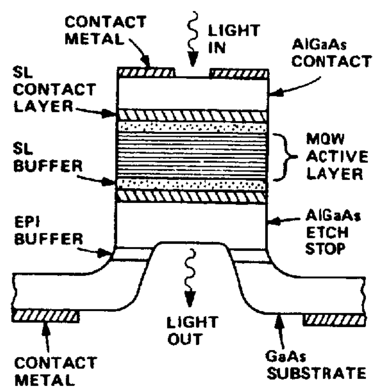




**Figure 4.** Schematic cross-sections of some MBE-grown devices: (*a*) high electron mobility transistor, (*b*) heterojunction bipolar transistor, (*c*) multi-quantum well laser, and (*d*) QCSE modulator.

HBTs with an $f_t$ of 40 GHz and an $F_{max}$ above 25 GHz have been grown by Asbeck, et al.[49] Other MBE grown transistors of potential significance, such as the hot-electron transistor, are referenced in Table 2, but will not be discussed here.

A discussion of MBE grown heterojunction bipolar transistors and selectively doped heterostructure transistors is given in Chs. 5 and 6, respectively, of *VLSI Electronics Microstructure Science,* Vol. 11, *GaAs Microelectronics* (N. G. Einspruch and W. R. Wisseman, eds.), Academic Press (1985). Also important is the article by Kroemer.[50]

### 3.2 Microwave and Millimeter Wave Devices

The first MBE grown device was a varactor diode[51] followed by the IMPATT diode.[52] These devices demonstrated the relative ease with which MBE could control doping profiles and thickness. High performance mixer and Gunn diodes have also been produced by MBE (see Table 3). In addition to two terminal devices, both low-noise and high power FETs have been successfully fabricated using MBE. Several manufacturers now produce MBE-grown IMPATTs and low noise FETs for commercial use.

### 3.3 Optoelectronic Devices

Optoelectronic devices require many of the same growth control capabilities (i.e., uniformity, abrupt heterojunctions, doping level and reproducibility) needed for transistors, but in addition there are strict limitations on the levels of deep traps. These traps, acting as recombination centers, can fatally impact the optical properties of LEDs, lasers, photodiodes, etc. Control of grown-in defects, dislocations and unintentional contaminants, all of which can serve as recombination centers, is critical. Considerable progress has been made in the past few years in the quality of MBE grown optoelectronic material. Room temperature CW AlGaAs DH lasers have been demonstrated with threshold currents as low as the best LPE material.[59][60] Tsang[61] had also shown that MBE can produce high quality DH lasers at growth rates near 10 microns per hour with excellent yield and reproducibility. DH lasers with projected mean CW lifetimes of greater than $10^6$ hours have been grown. The advantages of MBE are not limited to DH lasers. Table 4 lists some of the many different optoelectronic devices grown by MBE.

One optical device which exemplifies the growth control of the MBE process is the multiquantum well (MQW) heterostructure laser. A cross-sectional sketch is shown in Fig. 4(*c*). The MQW structure is composed of approximately 30 alternating layers of two materials (e.g., GaAs and AlGaAs) with layer thicknesses of about 100 nm each. The challenge is to grow this structure with uniform, repeatable layer thickness, repeatable compositions and atomically smooth interfaces free of alloy clusters. Laser Spectra has indicated that MBE can achieve this with thickness control near the monolayer level. Mean lifetimes near 5,000 hours at 70°C have been obtained making MBE grown MQW lasers the longest lived. Saku, et al.,[69] have reported the lowest $J_{th}$ for AlGaAs MQW lasers operating below 700 nm and the shortest wavelength room temperature operation of any AlGaAs MQW laser using MBE grown material. Also, Ohmori, et al.,[70] have achieved the first room temperature cw operation of a GaSb/AlGaSb MQW laser. These results attest to the material quality and growth control capabilities of MBE.

One final class of optoelectronic devices requires mention because of its potential contribution to the long-sought optical computer. This class of devices, based on quantum well structures, uses the Quantum Confined Stark Effect[64] and operates at room temperature. Optical modulators and voltage-tunable detectors can be made and combined into a single device called a SEED (self-electrooptic effect device). SEEDs have been made into linearized optical modulators, optically bistable devices, optical level shifters and OE oscillators. A QCSE modulator is shown in Fig. 4(*d*). The device was grown with MBE and has a transparent superlattice buffer layer on either side of a MQW structure.

### 3.4 Integrated Circuits

MBE-grown devices have progressed into digital, monolithic microwave, electro-optical and optical circuits at various levels of integration. Table 5 lists some integrated circuits fabricated from MBE-grown material. OEICs (optoelectronic ICs) have reached the SSI level,[85] optical ICs are at a somewhat lower level of integration, and both HEMT and HBT based LSI ICs have been successfully demonstrated. Texas Instruments[90] has made a MSI HBT 1K gate array and HEMT LSI 1K,[79] and 4K[80] SRAMs have been fabricated by Fujitsu (see Fig. 5). The 2-ns access time at 77 K is the highest ever reported for a 4K RAM. Miller[91] and Andre, et al.,[16] have addressed the specific MBE equipment

challenges presented by HEMT IC requirements. Threshold voltage control to within 30 mV is required across-the-wafer and wafer-to-wafer for LSI RAM HEMT circuits. Abrokwah, et al.,[92] achieved a MODFET threshold voltage standard deviation of 15% ($\langle V_t \rangle = -2.61\ V$) across a three-inch wafer while values of 16 mV for E-HEMTs and 24 mV for D-HEMTs have been reported over 2-inch wafers by Mimura, et al.[93] Kuroda, et al.,[80] obtained threshold voltage standard deviations of 12 mV and 20 mV, respectively, for DCFL E- and D-HEMTs with 1.5 micron gates. These values are about 2.5% of the DCFL logic swing. Current generation MBE systems are capable of meeting the thickness, composition, and doping specifications required for IC material growth on three-inch wafers. Further progress must be made in reducing defect levels, however.

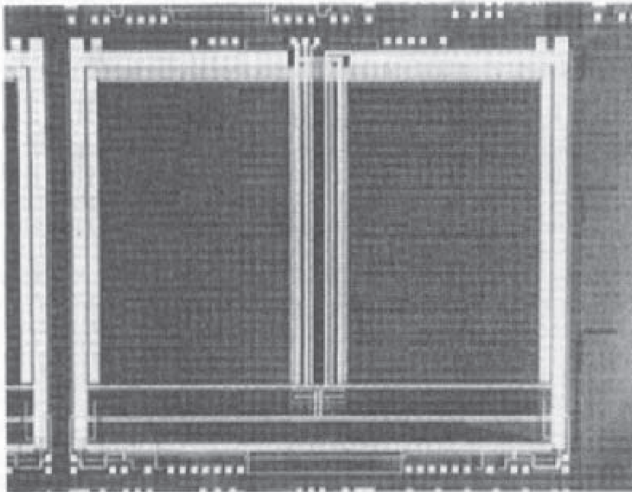


**Figure 5.** A 4K SRAM made from MBE-grown material.[80]

## 4.0 MBE DEPOSITION EQUIPMENT

Our attention in this section will focus on III-V MBE equipment. Discussions relevant to silicon and II-VI MBE will be made where appropriate. A system for II-VI MBE is shown in Fig. 6.

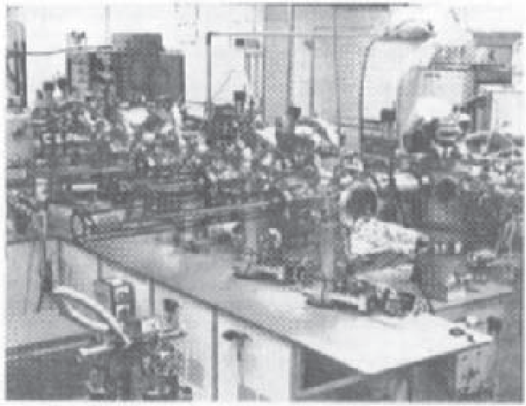


**Figure 6.** Photograph of a II-VI MBE system. *(Courtesy of J. P. Faurie, University of Illinois, Chicago.)*

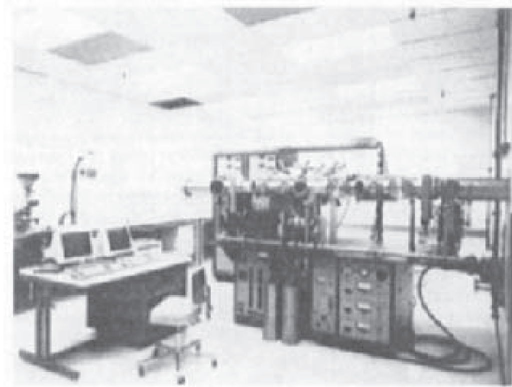
## 4.1 Vacuum System Construction

Vacuum system construction practices closely follow those of surface analysis equipment. Standard ultrahigh vacuum (UHV) practices are employed (see Dushman,[94] Guthrie,[95] or O'Hanlon,[96] for example). All internal materials are carefully selected for minimal background gas contribution and 200°C bakeout temperature compatibility. Materials like stainless steel, quartz and alumina are used where operating temperatures do not exceed 200°C. High purity refractory metals and pyrolytic boron nitride (PBN) are commonly used where temperatures exceed 200°C. Moving parts are typically dry-lubricated with very low vapor pressure molybdenum or tungsten disulfide.

**Construction Practices.** System chambers are normally fabricated from either 304 or 316 stainless steel using TIG welding techniques. These are the metals of choice for strength, vacuum compatibility and relative ease of fabrication. Following fabrication, chambers are often electropolished and passivated to improve the surface outgassing. Several techniques are practiced and properly prepared stainless surfaces will have an outgassing rate below $5 \times 10^{-11}$ Torr l/cm$^2$sec. Post bake levels in the $4 \times 10^{-12}$ Torr l/cm$^2$sec range are nominal.[97] There has been some recent success constructing MBE systems from aluminum,[98] but aluminum may not be compatible with all source materials. Nevertheless, base pressures one to two orders below stainless following a 25 hour bake at 156°C are claimed. System chambers are usually isolated by gate valves of

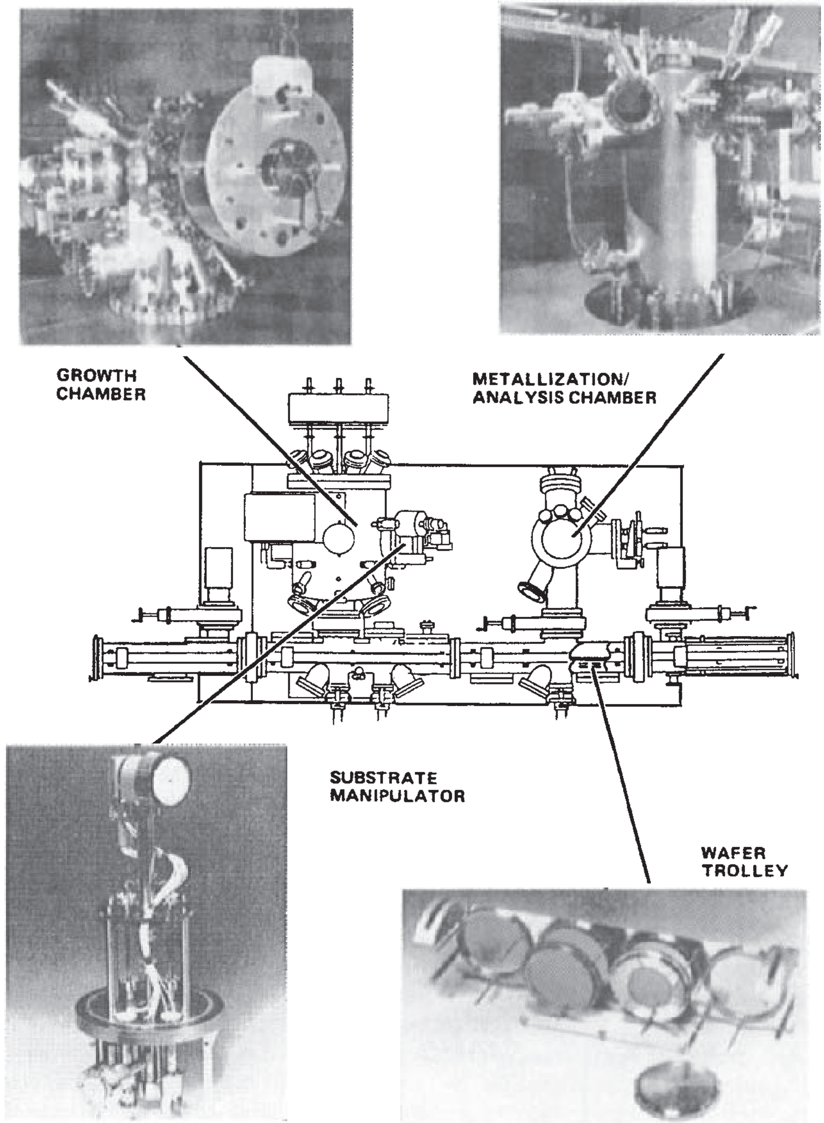
various types and sizes. These may be either all-metal valves or Viton sealed. Viton is compatible with repeated 200°C bakeouts if it is not baked under compression. O-rings of other fluorocarbon elastomers with higher temperature limits have been considered. Viton sealed valves have a cost advantage and about ten times the lifetime when compared to all-metal valves. All chamber ports are sealed with metal gaskets.

**Multi-Chamber Systems.** A typical current generation MBE system will be composed of four separate vacuum chambers: a load-lock for substrate entry and exit, a growth chamber, an auxiliary chamber for analysis or metallization and an intermediate or "buffer" chamber for pregrowth processing (see Figs. 7, *a* and *b*). The load-lock typically achieves base pressures of around $10^{-8}$ Torr while the auxiliary and buffer chambers reach $5 \times 10^{-10}$ Torr or better and the growth chamber reaches $5 \times 10^{-11}$ Torr or better after baking. Multichamber systems allow increased flexibility in configuration and operation. Present loadlock designs allow for the entry of 10 to 16 wafers (or samples) at a time to increase system throughput. Newly introduced wafers can be heated under vacuum to desorb water vapor before proceeding into the intermediate chamber. The separation of growth and analytical instrumentation, which appeared with second generation equipment, was prompted by a need to keep the analytical instrumentation clean and to allow film growth independent of analytical studies. The modular design of current generation MBE systems allows two or more systems to be connected, further increasing the in situ processing capabilities and throughput.



(a)

**Figure 7.** (*a*) Varian modular MBE system. (*b*) Key components of Varian modular MBE system.




(b)

**Figure 7.** *(Cont'd.)*

**Pumping Considerations.** MBE systems rely on a family of pumps depending on the film growth materials and on the purpose of the chamber(s) pumped. A typical III-V MBE system will use sorption pumps for roughing because they are clean, simple (reliable) and easily regenerated. After roughing, the chamber(s) are usually transitioned to a sputter ion pump. These pumps are also relatively simple and reliable and capable of maintaining system base pressures in the $1 \times 10^{-11}$ Torr range for a well-baked system. Titanium sublimation pumping is commonly used to assist the ion pump during initial pumpdown. Closed loop helium cryopumps frequently augment ion pumps on the growth chamber, where they pump gases such as hydrogen and helium somewhat more effectively. Cryopumps are mechanically more complex than ion pumps and, therefore, have reliability and cost considerations. The growth region is typically surrounded with liquid nitrogen-cooled cryopanels to minimize background gas contaminants. Turbomolecular pumps and trapped diffusion pumps are occasionally found on MBE systems intended for special applications. Such applications arise, for instance, when source elements with high vapor pressures (e.g., phosphorus and mercury) or gas sources (e.g., organometallics and hydrides) are used. These pumps have their drawbacks: turbopumps are less efficient with light element gases and diffusion pumps may backstream oil vapors if operated improperly. Cryopumps have also been used to pump these gases with varying degrees of success. Regardless of the pumping method, high vapor pressure materials such as phosphorus and mercury require a method of collection during bakeout.[99] This exhaust is frequently cryotrapped in a special container which can be removed without venting the system to the ambient. In addition, MBE systems using hydrides are frequently faced with large hydrogen loads and are most commonly evacuated with turbopumps or $LN_2$ trapped diffusion pumps.

**Sample Transfer Techniques.** One challenge for any piece of UHV processing equipment is sample handling. Techniques commonly used at atmospheric pressure such as a vacuum pik and air track are obviously impossible. All existing methods of vacuum transfer are variations of "pick and place." The most common means for bridging the vacuum interface are mechanical feedthroughs and magnetic couplings. Mechanisms using extended metal bellows are undesirable for reliability and cost factors. Rotary motion feedthroughs based on the Scotch yoke mechanism are common. The rotary motion can also be transformed into linear motion through a sprocket and chain. Magnetically coupled linear and rotary motion feedthroughs are equally common. The MBE system

shown in Fig. 7(*a*) uses magnetic coupling to operate "transfer rods" and "trolleys." A trolley, which can transfer up to 16 wafers at a time between chambers, is shown in Fig. 7(*b*). The transfer rods pick individual wafers from the trolley and move them to static stations or manipulators for growth or analysis. Wafer transfer mechanisms will evolve into another generation as automated production systems requiring minimal operator expertise and intervention are developed.

### 4.2 Sources

Sources are key elements of any MBE system. They must be designed to supply the needed uniformity and material purity. They can often be a source of background gas contaminants. The wide variety of source elements and compounds requires an equally broad assortment of sources.

**Thermal Evaporation Sources**. ***Knudsen Cells.*** Knudsen or K-cells are the standard evaporation source for most MBE systems. A typical K-cell is shown in Fig. 8. It consists of a heating element, surrounding heat shield and a crucible thermocouple assembly mounted on a port flange. Some cells include an integral water jacket in addition to heat shields. Construction materials are usually refractory metals such as tantalum and molybdenum and insulators like alumina and PBN. Lower temperature applications allow alumina, but due to the outgassing of contaminants, temperatures above a few hundred degrees usually mandate the use of PBN. The heating elements are wound either non-inductively or operated from DC power supplies to minimize stray B-field contributions that might interfere with analytical instrumentation. Source evaporants are contained inside crucibles which fit into the furnace assembly. Higher vapor pressure materials (e.g., arsenic) may use graphite or quartz crucibles, but PBN is more common particularly at higher temperatures.

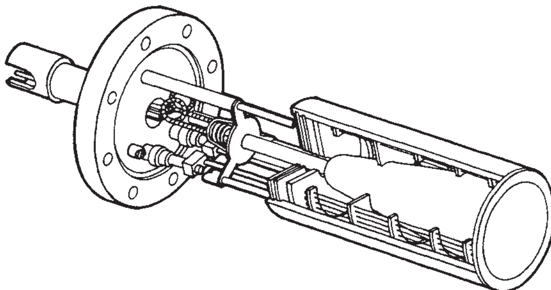


**Figure 8.** Large capacity K-cell (60 cm$^3$) for high uniformity across 3-inch wafers.

In an effort to improve the uniformity of deposition, several studies of K-cell effusion have been made.[100]–[103] The accepted geometry for molten sources (e.g., gallium, indium, and aluminum) involves a tapered crucible that will allow the entire melt surface to expose the substrate as the source is depleted. Large diameter sources may not require a taper depending on melt surface-to-substrate separation and sample size. In any event, wafer rotation during growth is also necessary for maximum uniformity. Effusion flux is determined by K-cell temperature which is controlled by a tungsten-rhenium thermocouple feeding a 3-term (PID) temperature controller. The standard thermocouple pair is tungsten-rhenium at either 5% and 26% or 3% and 25% rhenium. The former is somewhat less brittle after repeated high temperature excursions. K-cell flux density is related to temperature as

Eq. (1) $$d^2N/\mathrm{dwdt} \sim p(T)/(T)^{1/2}$$

In order to achieve gallium flux control within ±1%, cell temperature must be held to better than ±0.5°C. This is routinely obtained with existing PID controllers.[9]

It is often desirable to vary film composition in a controlled but rapid manner. Large magnitude, abrupt composition changes (e.g., heterojunctions and certain dopant profiles) can be produced by shuttering two or more K-cells of the appropriate flux. A graded layer of thickness greater than approximately 100 Å can be obtained by using the pulsed MBE technique (see Sec. 5.2) or by varying K-cell temperature. Thin layers or programmed doping profiles (e.g., exponential) require a source with fast thermal response. This can be achieved with a solid, Joule heated source (see Sec. 4.2) or with a modified K-cell. Construction of a fast response cell is similar to a standard cell except that the thermal mass is minimized. Since dopant fluxes are normally quite small, the major thermal mass is the source itself. The small dopant material required allows the cell size to be scaled down relative to the available power thereby decreasing the source response time. Figure 9 shows a typical fast-response dopant source.

***Solid Source Cracking Cells.*** Some materials, arsenic and phosphorus, for example, will evaporate in more than one molecular form. Often the larger molecule will have a higher vapor pressure and a lower sticking coefficient for a given substrate temperature than the smaller molecules. In this example, $As_4(P_4)$ has a maximum sticking coefficient of one half,

while that for $As_2(P_2)$ is near 1. Consequently the efficiency of source material utilization can be improved by cracking the tetramer into two dimers at the source. There is also evidence that the dimer incorporation results in fewer site defects and better material quality.[104][105] Source construction follows standard K-cell design with the addition of a secondary heat zone at the source exit.[106]–[108] See Fig. 10. Sufficient thermal isolation between the source furnace and the cracking furnace is required to minimize any interaction. The source zone is temperature controlled via a thermocouple and PID controller just as in the K-cell. The cracking zone may not be feedback controlled. Typically, the cracking efficiency will reach a maximum and level off beyond a critical temperature. It is enough to supply constant power somewhat beyond the critical value. Cracking sources often include a large source capacity (about 200 cm$^3$) to extend the period between refills. Crucible material for the high vapor pressure sources are frequently pyrolytic graphite. Graphite is relatively inexpensive and easily machined and the outgassing of the graphite is acceptably low after vacuum firing. The cracking end of the crucible is generally baffled to improve the cracking efficiency. An efficiency of greater than 90% is typical for arsenic or phosphorus.

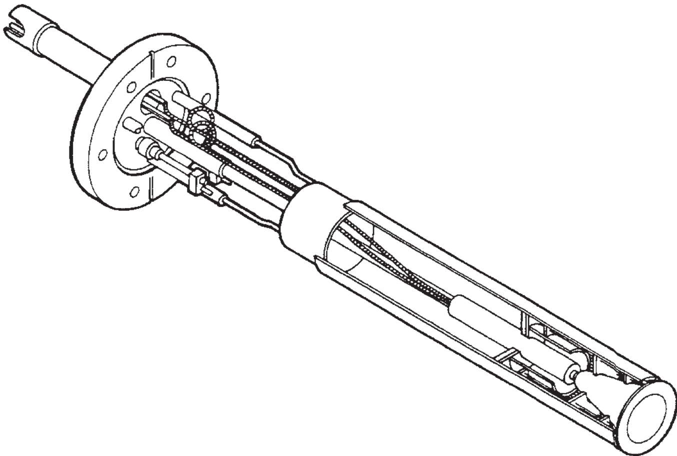


**Figure 9.** Dopant source designed for fast thermal response.

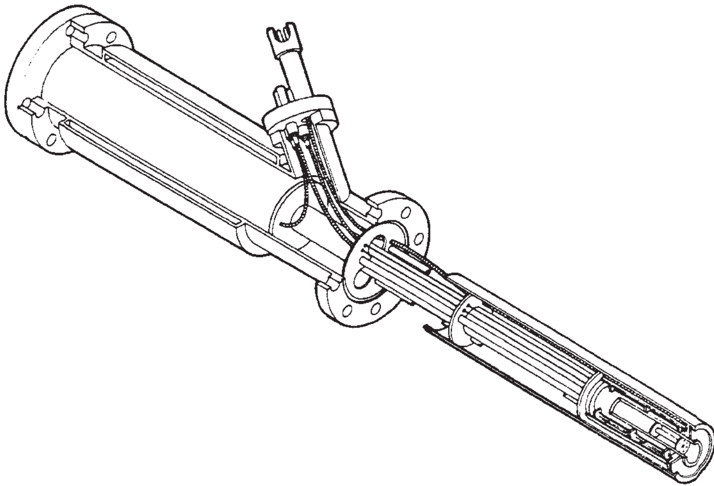


**Figure 10.** Solid source cracking cell.

***Solid Sources Using Direct Heating.*** Joule heating of materials for evaporation is not a new technique, but it has been appropriately reconsidered by T. N. Jackson, et al.,[109] to achieve silicon doping. A segmented wafer serves as the source until each leg is open. The wafer is easily replaced when expended. The advantages accrue from the small thermal mass which allows for a more rapid variation of flux and greater heating efficiency. See Fig. 11.

***Ionizing Sources.*** We discriminate between ionizing and implantation sources which are mentioned in Sec. 4.2. Naganuma and Takahashi[110] used electron impact ionization at the exit mouth of a K-cell to accelerate zinc atoms to energies near 1 keV. In this way, they increased the sticking coefficient sufficiently to incorporate this p-type dopant into GaAs. Gases have been similarly ionized. Takahashi[111] has introduced ionized hydrogen during the MOMBE growth of GaAs to control doping. Ionized hydrogen yielded p-type material, un-ionized n-type and no hydrogen yielded n+ GaAs. It was proposed that this technique be used to grow nipi superlattice structures.

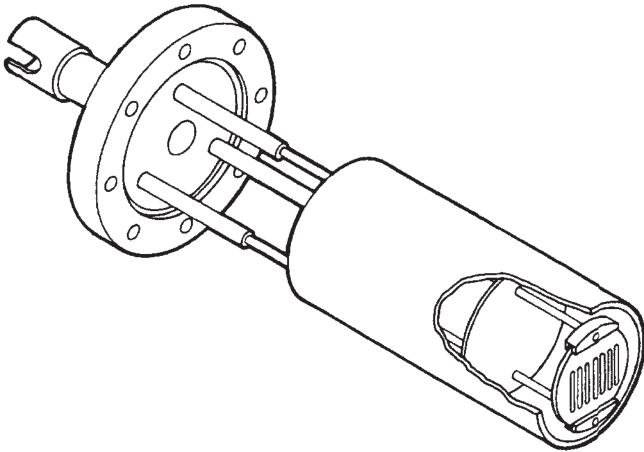


**Figure 11.** Solid silicon source using Joule healing. *(Following the method of I. N. Jackson, et al.)*[109]

***Load-Locked Sources.*** One attempt to solve the problem created by finite source lifetime is the load-locked source. In its simplest form, the source must be retracted behind a valve which is then sealed, allowing the source to be removed and refilled. The difficulty is finding a valve which can maintain adequate growth chamber vacuum integrity during source bakeout and is suitably long-lived. Two valves with differential pumping is better, but then cost and reliability factors increase. Since most systems require some periodic maintenance, an accepted alternative is to employ more than one, large volume source of the high expenditure materials (e.g., arsenic). These sources are often capable of running for four to six months without refill allowing other issues to trigger system downtime.

***Continuous Sources (Mercury).*** Sources which can be maintained in a liquid state (e.g., mercury) allow for continuous operation simply by adjusting the reservoir quantity and height.[112][113] (See Fig. 12.) This can be a fortunate solution to the relatively short source life of high vapor pressure, low sticking coefficient materials. Unfortunately, the number of materials amenable to this technique is quite limited.

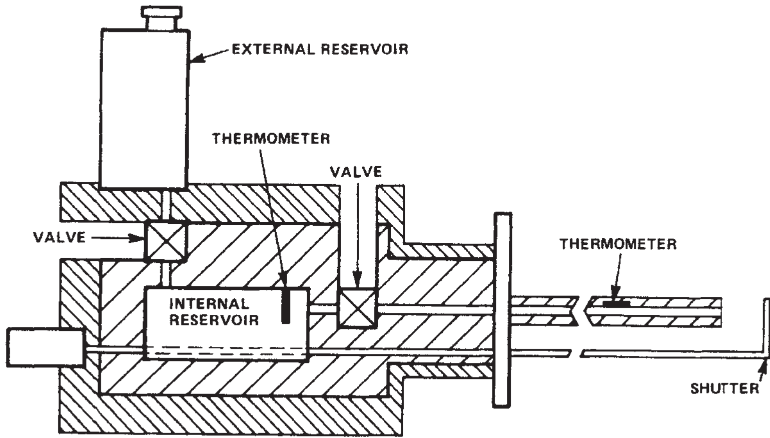



**Figure 12.** A continuous feed mercury source. *(K. A. Harris, et al.)*[113]

**Electron Beam Heated Sources.** Materials with very high melting temperatures are often evaporated using electron beam heating. Such sources are common in silicon MBE. Commercially available sources typically use magnetic deflection to direct an intense electron beam into a water-cooled hearth. The evaporant charge is shaped to fit the hearth. Scanning allows the beam to sweep over the charge surface. This improves material usage and extends source life. Materials commonly evaporated in this manner are tungsten, cobalt, nickel, silicon, and germanium. Metal silicides deposited by coevaporation require two e-gun sources. The high temperatures involved often result in significant radiant heating of the substrate which may aggravate substrate temperature control. Flux control may be accomplished by a quartz crystal monitor or electron excited emission spectroscopy (i.e., Inficon Sentinel). Using optimized geometries, excellent uniformity over a rotating substrate can be obtained.[114][115]

**Implantation Sources.** Implantation sources are differentiated from simple ionizing sources (in this work) by the existence of mass separation. Implantation sources are considerably larger (by virtue of the bending magnets) and more complex than the ionizing sources of Sec. 4.2. Some of the earliest applications were made by Bean and Dingle[116] who increased the sticking coefficient of Zn in GaAs; and Ota[117] who implanted arsenic

in silicon during MBE. Shimizu, et al.,[118][119] have used mass selection with low-energy (100–200 eV) Group-V implantation to grow GaAs, InP and InGaAsP. De Jong, et al.,[120] have used 10 keV As implantation to make silicon modulation doping structures.

**Gas Sources.** Gas sources are not new to MBE. Arsine was employed by Calawa[121] to improve the material quality of gallium arsenide. Later, Chow and Chai[122] using phosphine also experimented with gas sources. Serious consideration of gas sources has accompanied the successes of Panish, et al.,[123] and Tsang.[124] These processes are discussed in Sec. 6.4. There are two broad approaches. In one case, the gas or gases are cracked at the source orifice. This is common for the hydrides: arsine and phosphine. In the other case, the gases are simply directed toward the heated substrate where pyrolysis occurs. Any heating of this latter source is only sufficient to prevent condensation at the source. Refractory materials or quartz are used in the source construction depending on the gas and temperature range of operation. Gas sources are amenable to flux distribution manifolds and are likely candidates for multiple wafer processing. In addition, there is the possibility that large area uniformity can be achieved without wafer rotation.

**Source Shutters and The Source Flange.** One of the main virtues of MBE originates from the fact that fast acting shutters coupled with a slow growth rate allow for monolayer film growth control. Shutter motion may be either the flipping or rotating of a refractory metal blade between the source exit orifice and the substrate. Shutter actuation times below 0.1 second are nominal. Refractory metal shutters, once outgassed, maintain relatively clean outer surfaces in the closed position since they are heated by the source radiation. Source temperature transients can occur when the radiation losses are changed upon shutter opening and closing. These transients have been minimized by source modification[125] and by positioning the shutter blade obliquely to the source axis. It is common practice to mount 6 to 10 sources and their shutter mechanisms on a large vacuum flange. The sources are usually surrounded by a cooled baffle filled with either a water-alcohol mixture or liquid nitrogen to thermally isolate the sources from one another and minimize the consequent outgassing. A photograph of a typical source flange assembly is shown in Fig 13.

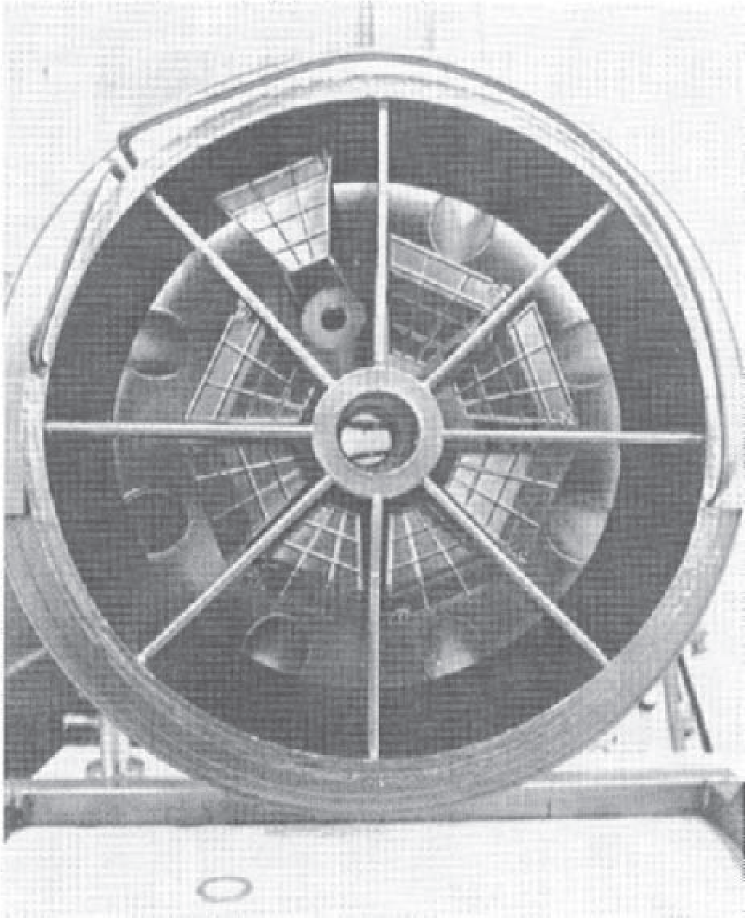


**Figure 13.** A source flange showing shutters and chilled, surrounding baffle.

## 4.3 Sample Manipulation

Proper sample (substrate) manipulation during growth is critical to producing high quality, uniform epitaxial layers. The substrate manipulator is responsible for holding, orienting, heating and rotating the sample (or wafer). A typical substrate manipulator is shown in Fig. 7b.

**Sample Mounting.** Traditionally, MBE samples have been mounted to molybdenum holders using indium solder. At film growth temperatures, the indium is liquid and provides adequate attractive force and good thermal conduction. Bonding free of voids maintains a minimal temperature gradient between the block and sample. Initial sample mounting is often done on a hot plate inside a glove box. This technique is difficult with large size samples, especially when they are brittle III-V materials. Post-deposition processing difficulties caused by the roughened back surface are common. Precoating the sample back surface with silicon nitride has been one solution.[126] Samples not amenable to this technique have been mechanically held (e.g., refractory metal retaining clips). The success of mechanical holders has largely eliminated these concerns.[127]–[130] Direct, free substrate heating is preferred and capable of ±5°C uniformity across an undoped 3-inch GaAs wafer at 750°C. Proper sample holding will produce minimal mechanical damage at temperatures over 850°C.

**Sample Temperature Control.** Sample temperature can be set and maintained by either thermocouple or pyrometer feedback.[131] Thermocouples are most commonly used because they are inexpensive and fairly reproducible. Although they do not provide accurate absolute sample temperature, they allow adequate maintenance of sample temperature. Calibration is achieved using fixed points such as alloy eutectic temperatures and sometimes the oxide desorption temperature of gallium arsenide. Pyrometer emissivities are also set using these points. Two-color pyrometers can, in principle, avoid this calibration and accommodate changes in viewport transmittance. Sample emissivity may vary with material and doping level and large variations must be adjusted for individually. Heater power input is regulated by a PID controller as with source furnaces.

**Sample Rotation Control.** Standard practice with large substrates (>2 inches diameter) is to rotate the wafer during film deposition. Rotational speeds of 5 to 20 RPM are typical for layers greater than about 100 Å and growth rates around one micron per hour. Very thin or single plane uniform layers require higher speeds possibly over 100 RPM. Most

MBE systems are equipped with a sample manipulator that allows the substrate to be continuously oriented about two axes. Remote, small angle positioning is provided to assist RHEED pattern adjustment.

### 4.4 System Automation

The complexities of MBE grown devices have made some amount of automation mandatory.[3][132][133] Extended superlattices, for example, would be virtually impossible without the accurate sequencing of source shutters. The reproducibility of structures, run-to-run would likewise be fortuitous. MBE system automation revolves around film growth control and the monitoring of certain functions (i.e., chamber pressures). Material structures are typically controlled from a "recipe" program that sets the sample temperature and rotation speed, the source temperatures and shutter sequencing from a given material structure.[134] Pregrowth calibration provides the proper constants to relate thickness and doping level to shutter timing and source temperature. The control or monitoring of other system facilities can vary greatly depending on the users' needs. The system controller can range from a small microprocessor to a mini-mainframe. More sophisticated systems allow several databases to be established: wafer recipe and growth history; system pressure history and RGA signature; source flux versus temperature history; and RHEED oscillation profiles, for example. A typical system configuration is shown in Fig. 14. Basic system software is usually supplied by the MBE equipment manufacturer, but specific applications may be written by the user.

### 4.5 Performance Parameters

Typical performance parameters for current generation MBE equipment are shown in Table 6. In addition to absolute performance specifications, there is a need for repeatability: the ability to maintain these specifications wafer-to-wafer and run-to-run over the system operating cycle. This is an especially important criteria for production systems. It is not uncommon for specifications to vary over this period, but they must remain within an allowed window. Normally, specifications with respect to thickness uniformity, growth originated defect levels, doping and composition uniformity are valid throughout the maximum specified uptime cycle.

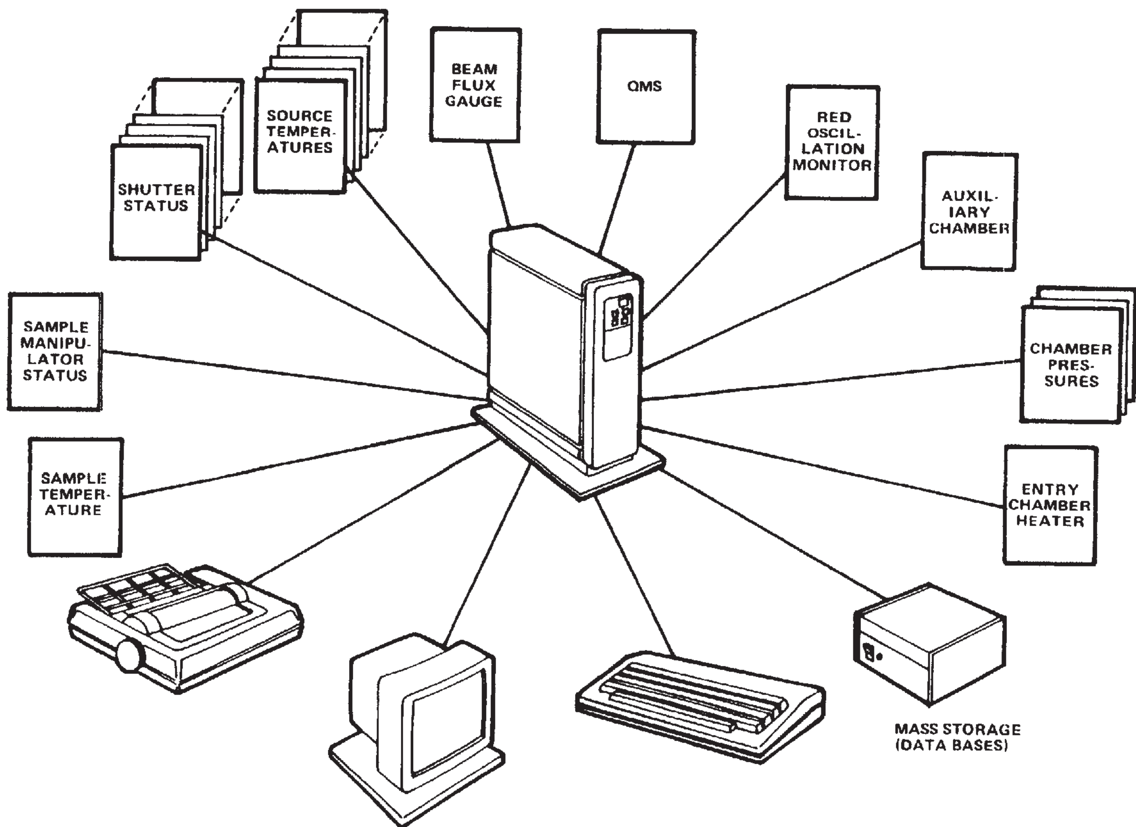



**Figure 14.** Functional diagram of computer controlled MBE system.

**Table 6.** Typical Performance Parameters

| | |
|---|---|
| Thickness Uniformity[a] (3-inch dia. wafer) | $<\pm 2\%$ |
| Composition Control[b] ($Al_xGa_{1-x}As$) | $\pm 1\%$ |
| Doping Control[a, c] (3-inch dia. wafer) | $<\pm 2\%$ |
| Defect density[d] (oval defects) | $<500/cm^2$ |
| Throughput[e] | 75/week |

[a] Saito and Shibatomi[135] at Fujitsu have obtained thickness and carrier concentration (doping uniformities of less than ±1% over a 3-inch wafer with optimized geometry).

[b] The composition of III-V binary compound semiconductors is largely controlled by surface reaction kinetics. Stoichiometry will be achieved given the minimum III/V flux ratio for a given growth temperature. Higher order alloys are more difficult to control in general because of incorporation competition between the Group-V elements

[c] Control of the absolute doping level depends largely on the accuracy of the monitoring method. Once a correlation between source temperature and dopant flux is established from Hall measurements, for example, repeatability is excellent due to the slow expenditure of source material.

[d] Dislocation density is excluded. Oval defects can be reduced by careful sample, system and source material preparation. Levels below $500/cm^2$ are routinely achievable with K-cell gallium sources if particulates are controlled.

[e] Throughput has become more important as more MBE systems fill device production roles. Current single wafer MBE equipment is capable of producing five 3-inch wafers per eight hour shift for one micron of material. Assuming full operation five days per week will result in 75 wafers per week maximum. Few systems produce more than half this number per week. Actual throughput depends on many factors such as device structure, asset utilization and operator skill. Future production equipment will reduce the number of uncontrolled variables (see Sec. 7.1).

## 5.0 PRINCIPLES OF OPERATION

A large number of films have been grown by MBE as listed in Table 7. This section covers the process portion of MBE growth, concentrating on GaAs, and Si and II-VI compounds to a lesser degree. The common analytical techniques to achieve and maintain high quality epitaxy are mentioned. A major concern of any MBE user is safety, of which the preliminaries will be included also in this section. For more specific process details, the readers may reference MBE reviews on III-V compounds,[4][8][167] Si[168]–[171] II-VI compounds,[172]–[174] Zn-chalcogenides[175] and IV-VI compounds,[176] and specific papers on GaAs[177] and AlGaAs.[178]

**Table 7.** MBE Grown Materials (Film: Substrate)

| | |
|---|---|
| **III-V** | |
| | AlGaAs: GaAs |
| | AlGaAs: GaAs, Si |
| | AlGaSb: GaAs |
| | AlSb: GaSb |
| | GaAs: GaAs, Ge,[136] Si[137] |
| | GaAsSb: GaAs,[138] InP, InAs,[139] GaSb[139] |
| | GaP: Si, GaP |
| | GaSb: GaAs, GaSb[140] |
| | InAlAs: InP |
| | InAlP: InGaP |
| | InAs: GaAs, GaSb |
| | InAsSb: GaSb, InSb, GaAs |
| | InGaAs: InP, InAs, GaAs,[139] GaSb[139] |
| | InGaAlAs: InP[141] |
| | InGaAlP: GaAs[142] |
| | InGaAsP: InP |
| | InGaAsSb: GaSb, GaAs[143] |
| | InGaP: InAlP |

*(Cont'd.)*

**Table 7.** *(Cont'd.)*

| | |
|---|---|
| | InGaSb: GaAs[144] |
| | InP: InP |
| | InSb: GaAs |
| **IV** | |
| | Si: Si |
| | Ge: Si |
| | GeSi: Si[145] |
| **II–VI** | |
| | CdMnTe: CdTe, GaAs[148] |
| | CdS: InP |
| | CdTe: GaAs,[146] InP, InSb[147] |
| | CdZnS: GaAs |
| | CdZnTe: GaAs[146] |
| | HgCdTe: CdTe, GaAs,[146] InSb, ZnCdTe |
| | HgMnTe: GaAs[146] |
| | HgTe: CdTe |
| | HgZnTe: GaAs[146] |
| | ZnMnSe: ZnSe, GaAs[149] |
| | ZnS: GaP |
| | ZnSe: GaAs,[133][151][152] InP, Si[153] |
| | ZnSeTe: GaAs[150] |
| | ZnTe: InP |
| **IV-VI** | |
| | PbEuSeTe: PbTe[68] |
| | PbSnSe: $BaF_2$, PbSe, $CaF_2$ |
| | PbS: $BaF_2$, PbSe |
| | PbSe: $BaF_2$, PbSe |
| | PbTe: $BaF_2$ |
| | PbYbSnTe: $BaF_2$,[154] PbTe[154] |

*(Cont'd.)*

**Table 7.** *(Cont'd.)*

**Insulators**

BN: Si

$BaF_2$: InP,[155] CdTe[155]

$CaF_2$: Si,[156] GaAs,[157] InP[158]

$CaSrF_2$: GaAs[159]

$LaF_3$: Si[160]

$SrBaF_2$: InAs,[161] InP[158]

$SrF_2$: GaAs[157]

**Metals**

Al: GaAs, InP[162]

Ag: InP[166]

Au: GaAs

$CoSi_2$: Si[165]

Fe: GaAs[164]

Mo: GaAs[163]

$NiSi_2$: Si[25]

Sn: GaAs

W: GaAs[163]

### 5.1 Substrate Preparation

The intent of substrate cleaning preparations is to create a suitable surface for epitaxial growth. The initial growth surface must be relatively free of contaminants and atomic imperfections. There are two reasons why such a surface is difficult to create for MBE samples. First, there is no easy manner to remove the top three or four atomic layers of the surface immediately prior to epitaxial growth as is done in VPE. MBE cleaning preparations are combinations of chemical steps done in a low particulate, noncontaminating and atmospheric environment, with the final cleaning steps done in vacuum. Second, a clean MBE sample must be transferred from an atmospheric situation to the UHV growth chamber. During this transfer period, the clean reactive surface may pick up contaminants. Nevertheless, many cleaning preparations have been developed for

substrates of a variety of materials which repeatedly yield device-quality epitaxial layers. Naturally, the simplest surface cleaning preparations are tried before progressing to more involved and complex preparations (i.e., chemical cleaning to sputter cleaning to high temperature desorption).

**III-V Substrate Cleaning.** Many detailed investigations for optimizing cleaning preparations for MBE III-V substrates were done on GaAs[4][179] although variations of these preparations are applied successfully towards other III-V substrates such as: InP,[180] InAs,[181] InSb,[181][182] GaSb,[140] etc. A generic cleaning preparation consists of the following steps:

1. A degrease step to remove residual waxes from the polishing step.
2. A chemical etch in concentrated acid, such as HCl or $H_2SO_4$, to remove other surface contaminants.
3. Immersion in a stagnant solution ($H_2SO_4$:$H_2O_2$:$H_2O$ and Br:$CH_3OCH_3$ are just two examples) to etch back the surface of the substrate.
4. A rinse in deionized (18 Mohm) water to form a thin and protective oxide cap on the etched substrate.
5. Thermal desorption of the oxide layer in UHV.

The fourth reoxidation step is critical. Munoz-Yague, et al.,[183] demonstrated that the proportions of $H_2SO_4$:$H_2O_2$:$H_2O$ can be optimized for the specific substrate orientation and dopant concentration. Massies, et al.,[184] propose that for step 4, immersing the substrate in static deionized water or drying the substrate in an oxygen environment produces a more consistent oxide rather than just rinsing.

Carbon is the residual contaminant most difficult to remove and keep off a clean surface. Another cleaning preparation exposes the substrates to UV radiation and ozone as an alternative for the third and fourth cleaning steps.[180][185][186] Two types of lamps are used, one which emits frequencies for exciting and dissociating the residual C-contamination and the other which creates ozone and atomic oxygen. The atomic oxygen reacts with the excited molecules, producing more volatile molecular species such as $CO_2$. Additional exposure time to these lamps regrows an oxide layer.

**Silicon Substrate Cleaning.** A generic cleaning preparation of Si substrates for molecular beam homo- and heteroepitaxy is less definitive. The literature contains a number of cleaning preparations which etch off

and regrow the $SiO_2$ in various wet chemical solutions. The purpose of these investigations is to regrow an $SiO_2$ layer which thermally desorbs in situ at a low temperature. Lower temperatures are desirable because slip lines form during the high temperature cleaning of Si surfaces.[187] There has been significant progress since the original work[188][190] which report a thermal desorption temperature time of 1200°C, 1 minute. Recent work[191] reports thermal desorption temperature times of about 750°C, 45 minutes.

Alternative cleaning preparations of Si substrates include reactive beam desorption, Si-radiation and sputtering. Wright, et al.,[192] originally demonstrated reactive beam desorption by aiming a molecular beam of Ga at the $SiO_2$ layer. Two reactions occur at a 800°C substrate temperature which convert the $SiO_2$ layer into more volatile oxides of the metal and SiO. Wang[193] has since used Al and Yang, et al.,[194] have proposed the use of In as the reactive beam. In Si-radiation, a Si beam is used to etch the $SiO_2$ at 800°C.[195] Sputter-cleaning of Si substrates is not recommended because the 1200°C anneal typically introduces slip lines.[187]

**II-VI Substrate Cleaning.** In general, sputter-cleaning and annealing the substrate has been successfully applied by those who grow the II-VI class of materials by MBE. The substrate preparation of II-VI homoepitaxial growths are described by Faurie, et al.,[196] for CdTe and Park for ZnSe.[197] In both cases, the substrates were first degreased, the CdTe substrate then went through a $BrCH_2OCH_3$ etch, whereas the ZnSe substrate bypassed this etch; both were then sputter-cleaned and annealed in situ.

Heteroepitaxy of CdTe on III-V substrates has also been demonstrated. To grow CdTe on InSb, the reported cleaning preparation is a hot isopropyl alcohol rinse followed by sputter-cleaning and annealing in situ.[198] In a TEM study of CdTe grown on InSb, thermal cleaning of the InSb substrate was compared to sputter-cleaning. The results showed thermally induced In precipitation at the interface.[182] The generic cleaning preparation was used on GaAs for heteroepitaxy of CdTe on GaAs. However, the thermal desorption of the oxide does not take place in an $As_4$ beam.[199]

## 5.2 Growth Procedure

Prior to the initiation of the III-V growth, it is common practice to thermally outgas all the sources (except for Group V materials) at temperatures greater than their eventual operating temperatures. After a period of time, the sources are reset to their operating temperature. Beam flux

measurements are taken with either a beam flux monitor (ion gauge), quartz crystal monitor, or a residual gas analyzer when the Group III sources equilibrate at the operating temperature. The beam flux measurement procedure using an ion gauge is as follows. Position an ion gauge at or near the substrate growth position. With all other shutters closed, open and close the shutter on the source in question, noting the pressure readings. The beam flux measurement is the difference between the pressure readings with the shutter opened and closed. The beam flux readings (beam equivalent pressure) indicate the arrival rate of the Group III species, and thus are a measure of the growth rate at a given substrate temperature.

After the Group V flux is set about 10–20 times greater than the Group III flux, the thermal desorption of the passivating oxide may commence. Growth is initiated by exposing the clean, heated sample to the Groups III and V beams via opening of the shutters.

Dopants are incorporated similarly by shutter actuation of the dopant source. Calibration of the dopant concentration as a function of source temperature may be done empirically.

**Thermal Transient.** MBE K-cell assemblies consist of a crucible of charge and an externally controlled shutter closing over the mouth of the crucible. Initially, thermal equilibrium is obtained prior to growth with the shutter closed. However, the initiation of growth by opening the shutter introduces a temperature perturbation onto the charge because now, the effusion furnace radiates energy out an open instead of a closed end. Typically, the exposed surface of the charge regains thermal equilibrium within a minute. This shutter-induced thermal transient affects directly the amount of material flux from the charge. In superlattice structures, where some layers require less than one minute of deposition time, the thermal transients are obstacles to growing a constant composition of the Group III metals within a single superlattice period.

Thermal transients have been reduced by a variety of methods. One simple method is to increase the separation distance between the mouth of the crucible and the shutter, or to vary the angle of the shutter with respect to the plane of the crucible opening. Another method is to increase the separation distance between the top surface of the charge and the shutter by not charging the crucible fully. A second concentric crucible is then used to shape the beam for uniformity and to retain some of the energy. The third method employs a computer which compensates for the thermal transients with prespecified amounts of power to the effusion cell.

**Doping Control.** A number of dopant sources have been used for MBE of GaAs. C. E. C. Wood[201] has reviewed these dopants and describes the incorporation mechanisms as currently understood. The dopants are thermally evaporated or sublimated from an effusion cell, unless otherwise noted. Briefly, Si, Ge, Sn, Te,[202][203] Se,[204] and SnTe[205] are n-type dopants for GaAs, where Si is the most common. P-type dopants for GaAs are Be,[206] Mg,[207] Mn,[208] implanted $Mg^+$,[209] implanted $Mn^+$,[210] and implanted $Zn^+$,[211] where Be is the most common. Gas sources containing Sn[212] and Si[213] molecules were also studied.

In MBE of Si, the Group V species which are used as n-type dopants are As and Sb. The technique to dope Si with As is by low energy (0.5 to 1.0 keV) ion implantation.[117] Evaporation,[214][215] low energy ion implantation,[216] and secondary implantation with Si[217] have been used to dope Si by Sb. In addition, low energy ion implantation is used to obtain large area dopant uniformity. Increased Sb doping control and concentration level has been demonstrated by negatively biasing the Si substrate during growth,[218][219] a technique named "potential enhanced doping."

The Group III species used for acceptors in Si-MBE are In, Ga, Al and B. The former three dopants are thermally evaporated from an effusion cell.[188][220] Boron may be deposited during growth by low energy ion implantation,[221] evaporated from a $B_2O_3$ source or sublimated from a saturated B-doped Si charge.[222]

The doping type and concentrations of MBE-HgCdTe compounds are critically related to the growth conditions. For example, a 6% temperature change or an increase in the Hg flux by a factor of two converts the doping from n-type to p-type.[196] HgCdTe may be conventionally doped n-type with In from an effusion cell.[223]

A study of various doping profiles predicted that a rectangular step doping profile results in an FET with linear I-V characteristics when the width becomes infinitesimally small.[224] MBE offers the capability of incorporating various doping profiles, and was suited for this particularly stringent requirement. Planar doping was demonstrated by interrupting the MBE growth briefly and depositing Ge on GaAs at the appropriate time in the growth sequence.[225][226]

Malik, et al.,[227][228] applied planar doping techniques to create new types of rectifying diodes. A $p^+$ planar doped layer was grown between two $n^+$ regions, separated by insulating layers of thickness $L_1$ and $L_2$. The barrier height, $V_{BO}$, at zero bias is calculated from:

Eq. (2) $$V_{BO} = [(L_1 + L_2)/(L_1L_2)]\ [eNx/E]$$

where eNx is the charge density of the planar doped region and E is the permittivity. The barrier height may be adjusted from zero to the semiconductor bandgap. The asymmetry in the I-V characteristics may be independently varied by the position of the thin $p^+$ layer between the $n^+$ layers.

Subharmonic mixer diodes with symmetric and asymmetric I-V characteristics were grown and characterized.[229][230] Other device structures which used planar doping techniques are a 3-terminal switch with a variable threshold voltage independent of bias voltage[231] and an HEMT for reduced persistent photoconductivity.[232]

**Compositional Control.** Compositional control in MBE is a function of flux ratios, substrate temperature and chemical species, since all these factors affect the surface incorporation kinetics on a substrate. In many cases, the fluxes are controlled via the source temperature to grow the desired composition. Beam flux monitoring prior to growth establishes reference points for future growths. In III-V alloy growths, the Group-III species have sticking coefficients of one at substrate temperatures below 600°C. The beam flux of the Group-III species, corrected for instrument-induced errors such as ionization efficiencies, are proportional to the desired atomic composition.

Stoichiometric control of x in $III_xIII_{1-x}V$ alloys results in control of the bandgap. For instance, choosing an x between zero to one in $Al_xGa_{1-x}As$, a material with a room temperature bandgap from 2.16 eV to 1.35 eV may be grown. Other examples are given in Fig. 15 where specific compositions may be grown lattice-matched to suitable substrates.[233]

A heterojunction transistor was proposed which takes advantage of a bandgap induced electric field.[234] A phototransistor based on this principle was grown by MBE with a graded bandgap structure.[235] Reviews of bandgap engineering and graded bandgap devices have been written.[236][237]

Bandgap grading may also be applied advantageously for contact layers. An $In_xGa_{1-x}As$ layer was grown on an n-type GaAs from $0 < x < 1$, and then the final InAs surface was metallized, creating ohmic contacts.[238]

When multilayered structures of various III-V alloy compositions are needed, a set of sources are dedicated to a particular layer composition. However, the fixed number of source ports limits the number of compositions which may be grown in a multilayered structure. This is especially true for thin layers, where the short growth times do not allow a set of sources to reach thermal equilibrium for the succeeding layer composition.

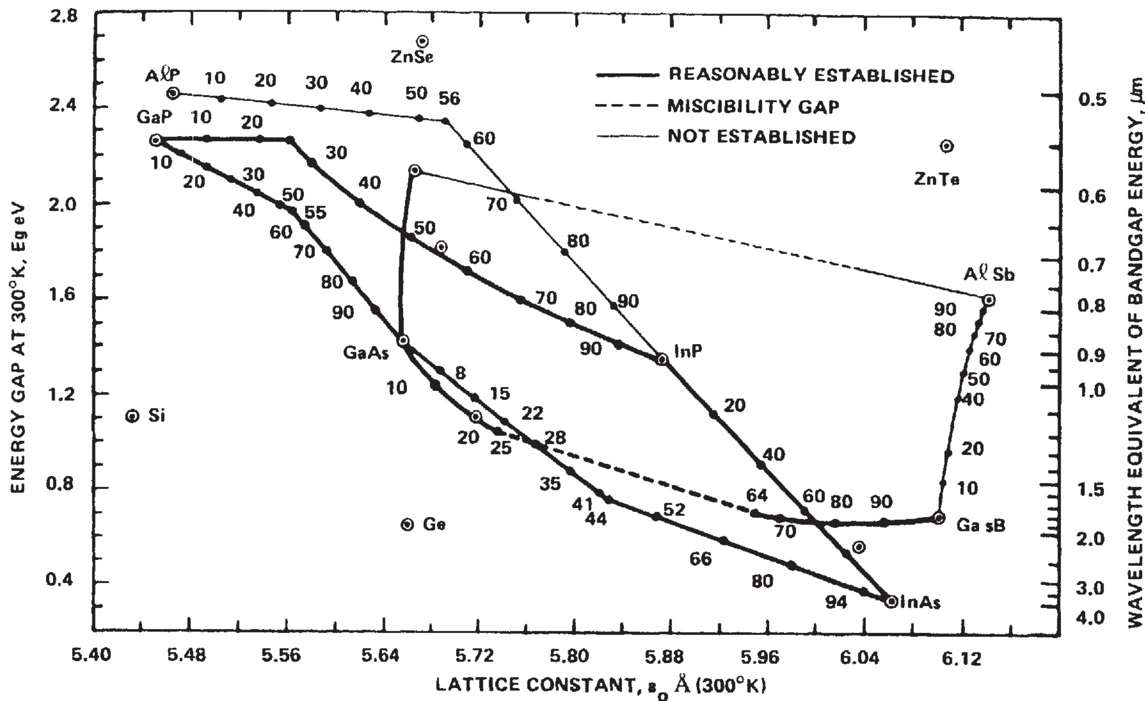



**Figure 15.** Energy gap versus lattice constant for some III-V materials at 300°K. *(R. Sahaj, et al.)*[233]

A novel solution was proposed called "pulsed molecular beam epitaxy."[239] The Group III beams are mechanically chopped such that the beam arrives at the substrate in pulses. The number of pulses are coordinated, say between Al and Ga, summing up atomically to the correct composition in one monolayer. The beam chopping time periods are chosen to be less than the time to grow one monolayer. Multilayered structures of AlGaAs[240] and InGaAlAs[241] have been grown successfully.

**Interrupted Growth.** High quality heterojunctions were attained when the growth was interrupted prior to the succeeding epitaxial layer, allowing time for the growth front to smooth over. In contrast, traditional heterojunction structures were grown in a continuous mode to avoid excessive impurity incorporation. The growth interruption technique utilizes RHEED to monitor the surface smoothness. During continuous growth, the RHEED intensity of a given spot oscillates with the period of a monolayer growth time.[242]–[244] The RHEED intensity maximum occurs when the surface growth front is smoothest. These RHEED intensity oscillations were also correlated to an MBE growth mechanism on GaAs[245] via computer simulations.[246] The growth conditions for the heterojunctions were optimized through computer-simulated results. To date, GaAs/AlGaAs[247][248] and GaAs/InAs[249] interfaces have been studied.

**In Situ Metallization.** Although other aspects of MBE metallization are of interest to researchers, we limit ourselves to metallization with respect to device structures in this treatment.

The benefits of in situ metallization accrue from a clean, well-ordered interface. This produces reproducible Schottky barriers and low resistance nonalloyed contacts. Reduced contact resistance is critical to low noise microwave performance. Stable contacts are especially important for InP devices where the barrier height is inherently low resulting in higher leakage currents. DiLorenzo, et al.,[250] were the first to demonstrate in situ nonalloyed ohmic subsequent in situ AuGe/AgAu top metallization. Reproducible low resistance contacts resulted. Cho, et al.,[251] have been able to reduce the noise temperature of microwave mixer diodes by growing epitaxial Al Schottky barriers. Ohno, et al.,[252] were able to produce an Al gate InGaAs MESFET by depositing epitaxial Al over 600 Å of $Al_{0.48}In_{0.52}As$ lattice matched to $Ga_{0.47}In_{0.53}As$. This created an 0.8 eV gate barrier height reducing the gate-to-drain leakage. Finally, McLean, et al.,[253] have successfully grown in situ epitaxial Al on GaAsSb. The ability of MBE to grow low resistance ohmic contacts and reproducible Schottky barriers is an important element of IC development.

MBE metallization has also contributed to the successful demonstration of new metal base devices. Cobalt and nickel silicide metallic layers have been grown epitaxially between Si allowing the first practical application of an epitaxial metal-base transistor (Rosencher, et al.)[254] Similarly, Rosencher, et al.,[255] have demonstrated the first permeable-base transistor (PBT) with an epitaxial $CoSi_2$ grating. Derkits, et al.,[256] have observed transistor action from W-GaAs metal gate transistors following the work of Harbison, et al.[257] The 80–150 Å thick W was grown nonepitaxially on the single crystal GaAs. These devices are distinct from PBTs because the pore size is smaller than the depletion length.

## 5.3 In Situ Analysis

Growing epitaxial films in UHV is advantageous because a number of analytical techniques may be used in situ which yield information on crystal structure, chemical bonding and composition. The physical mechanisms of reflection high energy electron diffraction (RHEED), x-ray photoelectron spectroscopy (XPS), Auger electron spectroscopy (AES), and secondary ion mass spectroscopy (SIMS) will be described briefly. A description of residual gas analysis (RGA) will also be included in this section.

**Reflection High Energy Electron Diffraction.** In reflection high energy electron diffraction (RHEED), a high energy beam of electrons aimed at a glancing angle, with respect to the sample, reflects off the surface-most layers of atoms. The reflected beam is scattered and impinges onto a visual monitor (fluorescent screen or camera). If the top surface is periodic with a period greater than the wavelength of the beam (i.e., lattice spacing is greater than the wavelength of the electron beam), diffraction occurs. The well-known Bragg law, $\lambda = 2d \sin\theta$, relates the wavelength, $\lambda$, surface periodicity, $d$, and diffraction angle, $\theta$, for achieving constructive interference (diffraction). The electron energy is related to the wavelength by the de Broglie equation: $\lambda = h/p = 12.25/(V^{1/2})$A, where $V$ is in eV.

RHEED patterns displayed on the visual monitor range from diffuse rings to spots to streaks. A diffuse ring usually indicates the presence of an amorphous layer, i.e., an oxide on the surface. A pattern of spots indicates thermal faceting, pitting, and/or a rough surface. When streaks appear, the general interpretation is the surface is smooth and of good crystalline perfection. The intensities and position of the streaks also yield crystal structure. As the growth proceeds on the substrate, the top surface becomes smoother and the RHEED streaks narrow. A more

detailed discussion on the application of RHEED to MBE is given by Cho, et al.,[4] and Ploog, et al.[258]

**X-ray Photoelectron Spectroscopy.** X-ray photoelectron spectroscopy (XPS) is also known as electron spectroscopy for chemical analysis, ESCA. A review of this surface analytical technique has been described by Riggs, et al.[259] Briefly, monoenergetic x-ray photons with energy $h\nu$ are aimed towards a sample. The spatial resolution is coarse with respect to AES because of the difficulty in focusing x-rays. The atoms within the first 25 Å absorb these photons and emit excited electrons with a characteristic binding energy, $E_b$. An electron energy spectrometer is used to measure the kinetic energy, $KE$, of the emitted electrons. The energies are related by $E_b = h\nu - KE + WF$, where $WF$ is the spectrometer work function. The XPS sensitivities are comparable to that of AES, and XPS identifies all elements except for H. In addition to obtaining elemental information, an atom residing in a molecule has forces acting upon its electron density. The changes in electron density induce a shift in the binding energy, enabling the determination of chemical information. Classically, XPS utilized these chemically induced shifts in the binding energy to observe various oxidation states of metals.[260] In MBE, XPS was similarly used to evaluate cleaning procedures on GaAs and InP substrates.[261]

**Auger Electron and Secondary Ion Mass Spectroscopy.** Auger electron spectroscopy (AES) is a quick technique for determining thin film composition. Sensitivities range from 0.05 to 5.0 atomic % across the Periodic Table.[262] The sampling depths of 5–20 Å may be combined with sputtering to obtain composition depth profiles. Spatial resolution of 0.03 micron to 30 microns are obtained. In MBE, the common application is to determine residual amounts of oxygen and carbon after the last in situ surface cleaning step.

The three step sequence of energy transitions leading to the emission of an Auger electron initiate with an incoming electron beam knocking out a core electron, say in the K shell for example. The resultant vacancy is filled by an electron from a higher orbited shell ($L_1$ or other higher orbital shells). The electron transition from the $L_1$ orbit releases an amount of energy ($E_k - E_{L1}$) to another electron in the $L_2$ shell. If the energy is sufficiently high, the $L_2$ electron is emitted as an Auger electron. The three electron process results in measured energies characteristic of each particular element. The Auger electron energy, $E$, is related to the transition according to $E = E_k - E_{L1} - E_{L2} + \phi$, where $\phi$ is the work function of the spectrometer. Hydrogen and helium are obviously not detectable by the

Auger process. A general review article on AES has been written[263] and one specific to MBE by Ploog, et al.[258]

Secondary ion mass spectroscopy (SIMS) can be more sensitive than AES by 2 to 3 orders of magnitude. SIMS is, therefore, applicable for determining contamination and dopant levels.[258] Sputtering may also be used with SIMS to determine concentration depth profiles of specific elements. Otherwise, the top 10 Å of the surface is sampled.

The physical mechanism of SIMS involves a primary ion beam (typically $O^+$ or $Cs^+$) to sputter a sample, generating a flux of secondary neutral and ionized species. The secondary ions are accelerated through a mass spectrometer and counted. A general review on SIMS is given by McHugh.[264]

**Residual Gas Analysis.** Residual gas analysis (RGA) is performed by mass spectrometry. Although RGA does not directly analyze the epitaxial layers, it does indicate the type of epitaxial environment and the composition of the beam flux. The RGA spectra can show the presence of air, water, or nitrogen leaks, and the presence of oxide in the source flux. Quantifying the RGA signals into partial pressures may be done with calibrated leak rates, or by accounting for the effects of ionization efficiency, filter transmission efficiency, and electron multiplier gain for various gases.[265] However, the hot filament of the RGA ionizer may alter the concentration of various molecular species and give misleading concentrations.

## 5.4 Materials Evaluation

The materials characterization techniques for MBE films are those commonly used for high purity semiconductor films. These techniques help in maintaining the film quality and identifying impurities. The control of impurities, desired and unwanted, is of utmost importance for developing new materials with unique properties. The techniques which will be described below are optical microscopy, Hall effect, capacitance-voltage, photoluminescence and deep level transient spectroscopy.

**Optical Microscopy.** At times, impurities or crystal defects may cause microscopic defects, such as oval defects. A Normarski (differential interference contrast option) optical microscope is an excellent tool for the initial and rapid evaluation of these defects. Also, optical microscopy gives morphological information which may be related to various growth conditions. There are chemical solutions for etching GaAs[266][267] which selectively etch various types of crystalline defects.

**Hall Effect.** The average transport properties of semiconductors are determined using the Hall effect. The measured parameters of Hall coefficient, $R_H$, and Hall resistivity, $\rho$, are related to the free carrier concentration, $n$, by:

Eq. (3) $$n = r_H/eR_H$$

where $r_H$ is the Hall coefficient scattering factor and assumed to be unity, and to the mobility by

Eq. (4) $$\mu = R_H/\rho$$

For n-type GaAs, the concentration of acceptors, $N_a$, and donors, $N_d$, may be derived from solving

Eq. (5) $$n_{77} = N_d - N_a$$

and

Eq. (6) $$N_d + N_a = f(\mu_{77})\,[\ln_e(6.94 \times 10^{17}/n_{77}) - 1]$$

where $\mu_{77}$ and $n_{77}$ are the mobility and free carrier concentrations at 77°K, and $f(\mu_{77})$ is from Fig. 9 of Stillman, et al.[268]

The Hall effect measurements were simplified by van der Pauw. By keeping the contacts small and at the circumference of the sample, and the sample thickness uniform and without geometric holes, a sample of arbitrary shape may be used for the Hall effect measurement.[269] With only four sample contacts, $\rho$ may be determined from a single resistance measurement and $R_H$ from a magnetically induced change in resistivity.[270] A review which discusses the Hall effect has been written by Blood, et al.[271] In addition to measuring transport properties in single epitaxial layers, high mobility structures such as HEMTs are also characterized by the Hall effect.

**Capacitance-Voltage.** From the capacitance-voltage (C-V) method, a dopant profile may be obtained. The method requires a Schottky barrier to be made by a small area, $A$, contact on the sample. A reverse bias voltage, $V$, is applied to the barrier and the capacitance is measured. The depletion depth $X_d$ is derived from:

Eq. (7) $$X_d = \varepsilon A/C$$

where $\varepsilon$ is the dielectric constant. The dopant concentration, $n$, at $X_d$ is derived from:

Eq. (8) $$n(X_d) = \frac{C_3}{\varepsilon e A^2}(dC/dy)^{-1}$$

where $e$ is the electronic charge. However, the maximum depth is limited by electrical breakdown at the surface of the sample. For n-type GaAs, $X_d$ equals 20 microns and 0.02 micron for dopant concentrations of $1 \times 10^{15}$ $cm^{-3}$ and $1 \times 10^{18}$ $cm^{-3}$, respectively. Also, there are resolution trade-offs between $X_d$ and $n$.[272]

Because of the problems mentioned above, a C-V technique was developed to contact and etch the sample in an electrochemical cell.[273] The etch depth, $X_e$, is determined by the amount of material removed according to Faraday's law of electrolysis:

Eq. (9) $$X_e = \frac{M}{ZFDA}\int I\,dt$$

where $M$ is the molecular weight of the sample, $D$ is the density of the sample, $Z$ is the atomic charge transferred and equals 6 for GaAs, $F$ is Faraday's constant, $A$ is the dissolution area, $I$ is the current, and $t$ is the time. The actual depth is the sum of $X_d$ and $X_e$. In addition to depth profiling the sample, the electrochemical C-V technique may be expanded with a laser source to study the photovoltage characteristics of the sample. Concentration profiles of AlGaAs/GaAs layers and the Al alloy content may be determined by this technique.[272]

**Photoluminescence Spectroscopy.** Photoluminescence spectroscopy (PL) is a nondestructive optical technique, ideally suited for evaluating high purity semiconductors because electrical contacts are not required for these high resistivity materials. In PL, a laser beam with a photon energy greater than the bandgap energy of the sample excites electron-hole pairs (excitons) within the sample. The optical emission from the resultant recombination of these excitons with shallow defect centers is scanned with a monochromator and detected by a photomultiplier. The samples may be cooled to 4.2°K for high resolution (0.1 meV) studies.

PL is used to determine molar concentrations in ternary III-V compounds because of the near bandgap energy information. Whereas Hall and C-V techniques give impurity transport and distribution information, PL has been used to empirically identify certain shallow acceptors in GaAs[274] and InP.[275] Concentrations of donors in the $1 \times 10^{15}$ $cm^{-3}$ and

acceptors in the $1 \times 10^{14}$ cm$^{-3}$ range are resolvable by PL.[274] A section on PL, in the study of GaAs and InP, is included in a review article on high purity III-V semiconductor materials.[276] A review on high resolution PL was written by Reynolds, et al.,[277] on MBE grown multiquantum well structures.

**Deep Level Transient Spectroscopy.** Deep level transient spectroscopy (DLTS) is a fast and sensitive transient capacitance technique.[278] A Schottky barrier is prepared on the sample. At a given temperature, a pulse generator applies a bias voltage onto the barrier, injecting carriers across the barrier and filling deep level traps. The capacitance, $C$, of the barrier is monitored as the barrier returns to thermal equilibrium and the traps empty. The deep trap concentration, $N_T$, is determined by:

Eq. (10) $$\Delta C/C = N_T/2N_B$$

where $N_B$ is the background doping concentration. A typical value of $\Delta C/C$ is about $1 \times 10^{-6}$ and of $N_B$ is about $1 \times 10^{15}$ cm$^{-3}$, giving a resolvable $N_T$ of $1 \times 10^{9}$ cm$^{-3}$.[262] Judicious selections of the time window over which $\Delta C$ is measured facilitates the emission rate data interpretation of a given trap. The emission rate, $e$, varies exponentially with the inverse temperature:

Eq. (11) $$e = K \exp(-\Delta E/T)$$

where the preexponential factor $K$ is assumed to be independent of temperature and $\Delta E$ is the enthalpic activation energy. By varying the pulse height, the deep trap concentration distribution may be profiled. By varying the pulse duration, the capture rates of the traps may be derived. Presently, there are commercial DLTS units available.[279][282]

In the initial DLTS study of MBE GaAs, nine traps were identified and labeled M0 through M8.[283] Since then, the four traps, M1 through M4, have been identified as related to MBE of GaAs epitaxy and are possibly impurity defect complexes.[284] In the same study, Fe and Cu induced deep traps were identified in MBE of GaAs. Another trap, labeled M00, was recently found.[285]

The deep level traps found in MBE grown AlGaAs bear little correlation to those of GaAs.[286] The major trap is the one with $\Delta E = 0.78$ eV, which had strong concentration dependence on the substrate growth temperature[287] and is also identified in VPE material.[286] In the latter study, four of the six traps found in AlGaAs had a concentration

dependence on the Al alloy composition, indicating that the deep traps are some sort of Al-contributing impurity. Another study was done on deep levels in MBE grown AlGaAs as a function of growth parameters, Si doping concentration and Al alloy composition from $0 < x < 1$. Two major traps were identified as ME6, prominent at $x < 0.2$, and ME3, prominent at $x < 0.2$. The authors proposed that the ME6 trap is created by a donor-vacancy complex (DX) center responsible for persistent photoconductivity.[288] The ME3 trap is thought to originate from a Group-III vacancy or an antisite defect.[289]

### 5.5 Safety

In the MBE process, toxic materials are used as the source evaporants and also created during growth. Specifically in GaAs growths, inorganic As and the Be dopant material are known to be carcinogenic for humans. Toxicity levels of these and other materials may be found in Sax.[290] A study of GaAs toxicity on rats was published in 1984.[291] The data suggest that GaAs dust should be considered as a source of As exposure. MBE operators and service personnel should consult industrial hygienists for the appropriate respirators, protective clothing and handling techniques for As and GaAs. The U.S. Department of HEW[292] has a recommended standard for handling As in an industrial environment.

Air, surface wipes and biological monitoring should be done to insure that the As levels are below OSHA recommendations.[290] All the monitoring should at least be performed in conjunction with potentially hazardous operations, such as recharging of the As source at the source flange. Air and wipe samples may be done more frequently, for example, during sample loading at the loadlock area. Biological monitoring is typically performed with an urine analysis for levels of As and its metabolized compounds. The urine analysis becomes more complex if the personnel had eaten shellfish within 48 hours of the test.[293]

## 6.0 RECENT ADVANCES

MBE is an incredibly fertile process. Its evolution into materials engineering and advanced device production is exceptional. Some current areas of research, relevant to the future viability of MBE, deserve mentioning.

## 6.1 RHEED Oscillation Control

Although intensity oscillations in RHEED patterns were recorded over six years ago by C. E. C. Wood, their nature was not well understood at that time and consequently their potential use was not perceived. The first published explanation is credited to Harris, et al.,[294] who observed pattern oscillations when GaAs growth was resumed on a tin-rich surface, and to Wood.[295] Since then RHEED oscillations have been observed with AlGaAs and Ge[296] and InGaAs[297] on GaAs substrates and recently RHEED oscillations for silicon on silicon[298][299] have been reported.

Two approaches to measuring intensity variations are shown in Fig. 16a. Examination of the specular beam in an off-Bragg condition reveals an increased sensitivity to the step density (and terrace width). A minimum in intensity corresponds to a maximum density of surface steps. The oscillations damp with time at a rate depending on the initial surface conditions and the final step density. One period of oscillation corresponds to the growth of one monolayer (Ga + As). An illustration of specular beam intensity versus time when the gallium beam is exposed is shown in Fig. 16b. Since the gallium flux determines the growth rate under As-stabilized growth, the period of oscillation allows the gallium flux to be determined. Growth under Ga-stabilized conditions allows the arsenic incorporation rate to be measured and thus the As/Ga ratio.[300] RHEED oscillations can also be used to determine the Al mol fraction in the growth of AlGaAs. Thus, the technique can be used to calibrate source fluxes without resorting to the beam flux gauge thereby avoiding difficulties associated with determining the gauge sensitivity.

## 6.2 GaAs on Silicon

There are several potential advantages to growing GaAs on silicon. For example, the speed and optical properties of GaAs can be combined with the superior thermal conductivity of silicon. In addition, one can imagine silicon logic circuits with GaAs optoisolators for interconnect simplification and noise immunity. Recent results have fueled enthusiasm for the monolithic integration of GaAs and silicon devices. Initial attempts to grow GaAs devices on Si involved the use of a thin nucleating layer of germanium.[301][302] Wang[303] was the first to show that the antiphase disorder could be suppressed without using a Ge buffer. Despite the relatively large lattice mismatch (~4%) and the probability of antiphase domains, considerable success has been achieved growing directly on

(100) silicon substrates cut between 3 and 4 degrees off-axis toward (110). GaAs MESFETs,[304] MODFETs,[305] lasers[306][307] and HBTs[38] have been successfully grown on silicon. Although there is considerable debate over the mechanism which allows the strain accommodation, many researchers are reporting positive results. Superlattice buffer layers are often employed to accommodate the mismatch and retard the outdiffusion of impurities and dislocation threading[308] from the substrate. A judicious scheduling of processing steps has allowed the production of silicon MOSFETs and GaAs MESFETs on the same wafer.[309] VLSI circuits with central HEMT logic elements and peripheral silicon I/O drivers are conceivable. If viable and economically competitive, GaAs on silicon will present immediate problems to MBE equipment vendors who will be required to supply very high uniformity over 4 inch and possibly 6 inch wafers. Besides the challenge this presents for conventional K-cell sources, there are also difficulties associated with heating and handling such wafer sizes in vacuum.

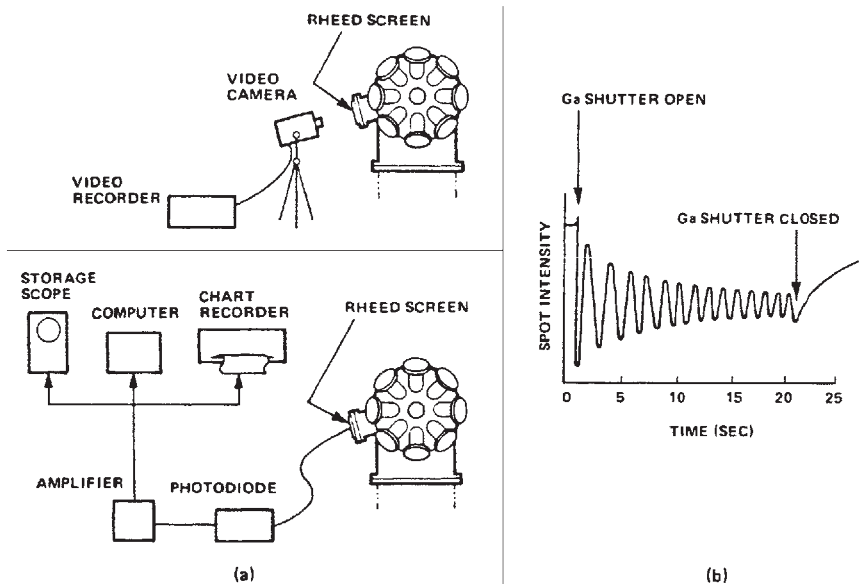



**Figure 16.** (*a*) Two possible arrangements for analyzing RHEED oscillations; (*b*) typical variation in spot intensity with gallium shutter opened.

## 6.3 Oval Defect Reduction

Morphological defects have been a serious concern since device-quality, low defect density films were sought. Surface defects can degrade the material electronic properties and present lithographic problems. III-V surface defects have many different origins: the substrate itself, pregrowth surface particulates, the film growth process, and postgrowth handling.[310] Careful substrate selection, preparation and handling have reduced defects to the point where those due to the growth itself are dominant.[311]–[315] The so-called "oval defect" has emerged as the principle defect contributor. A typical oval defect is shown in Fig. 17. Oval defects vary from 1 to 20 microns in length and are characterized by a major axis aligned along a <110> direction. Each defect appears to be bounded by (111) stacking faults that originate on a gallium-rich inclusion. Oval defect densities between $10^3$ and $10^4$ are not uncommon. Recent studies of oval defects have revealed two major sources: substrate surface particulates[316] and the film growth process. Careful substrate cleaning[317] and improved equipment design can greatly reduce the particulate contribution. It is the latter cause that has now gained the most attention. Oval defects originating during growth increase in density with film thickness and have been attributed to the presence of gallium oxides[318]–[320] and the spitting of gallium droplets from the source K-cell.[311][321] Neither mechanism can be differentiated on the basis of the observed increase in defect density with gallium source temperature. Various approaches that reduce the gallium oxides in the system have been shown to reduce the density of oval defects.[322][323] Defect densities down to 100 ±50 $cm^{-2}$ have been claimed using conventional K-cell sources. Tsang[324] has reported no oval defects using gas sources. The successful production of large area integrated circuits will require densities below 10 to 50 $cm^{-2}$ depending on the mean defect size.

## 6.4 Chemical Beam Epitaxy/Gas Source MBE

There is a growing interest in gas sources within the MBE community, especially among users contemplating production applications. Several approaches are under evaluation: mixed gas and conventional sources and all-gas processes using hydride and metallorganic sources or only organometallic sources. The high toxicity of the Group V hydrides is an issue of concern and the development of reduced toxicity alternatives is mentioned in Sec. 7.4. Some researchers have combined Group III alkyls

with conventional and cracked elemental Group V sources.[325][326][336] Gas sources have also been used for other reasons. An improvement in GaAs material quality has been found by Calawa[327] and Pao, et al.,[328] following the introduction of hydrogen during growth. Tokumitsu, et al.,[329] have added ionized hydrogen to trimethylgallium (TMG) and $As_4$ to reduce the carrier concentration by two orders of magnitude. Also, Briones, et al.,[330] have tried to use silane as a dopant source with limited success.

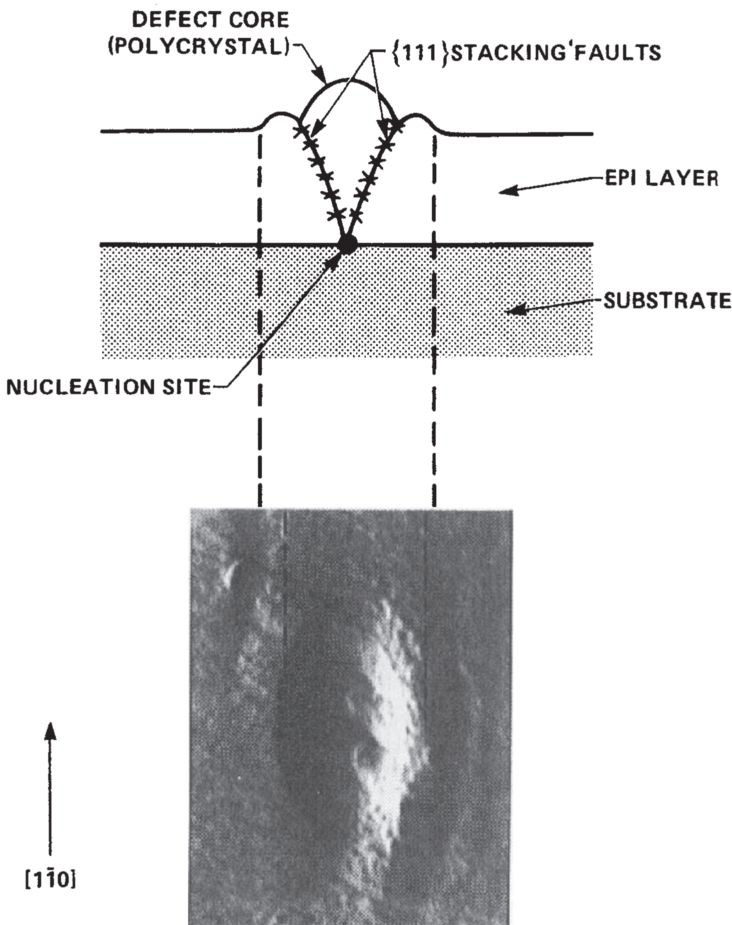



**Figure 17.** Typical oval defect and cross sectional drawing.

**Hydride MBE.** The introduction of gaseous sources into MBE systems dates back to Morris and Fukui,[331] who used arsine and phosphine to grow GaAs, GaP and GaAsP. Calawa[121] demonstrated material improvements with the substitution of cracked arsine for solid arsenic as the Group V source. Chow and Chai[332] reported on the cracking efficiency of phosphine under similar conditions. In each case, the Group V hydride was passed through a heated source section where it was decomposed according to the reaction:

Eq. (12) $4GH_3 \rightarrow G_4 + 6H_2$

Further heating results in the cracking:

Eq. (13) $G_4 \rightarrow 2G_2$

Within a given temperature range, G and $G_4$ are minor contributors to the total gas pressure when compared to $G_2$ and hydrogen. Significant progress has been made by Panish[333] who used "high" pressure (200–2000 Torr) sources to grow InGaAsP. Several types of laser heterostructures were successfully grown. More recently, Temkin, et al.,[334] and Vandenberg, et al.,[335] have grown GaInAs(P)/InP quantum well structures using a single high pressure hydride source. The Group V ratio was set by varying the individual hydride pressures. Panish refers to this technique as Gas Source MBE or GSMBE.

**Metallorganic MBE.** Another related approach has been taken by Tsang[124] at AT&T Labs. Tsang explored an all-alkyl gas process using TMG or triethylgallium (TEG) and trimethylarsine (TMAs) to grow GaAs, InP and InGaAs. The results of material quality analysis were disappointing probably due to the varying purity of the Group-V alkyls. Better results were obtained using arsine in place of TMAs. Tsang refers to this process as Chemical Beam Epitaxy or CBE. Combining TEG and $As_4$ has yielded some of the best MOMBE grown GaAs yet seen. Kondo, et al.,[336] obtained a background impurity concentration of $8 \times 10^{14}/cm^3$ at room temperature. AlGaAs has been grown by the addition of triethylaluminum (TEAl). Tsang and Miller[337] report material quality comparable to the best MBE and MOCVD. GaAs/AlGaAs single- and multi-quantum well structures were grown with superior quality PL line shape. Further, Kawaguchi, et al.,[338][339] have produced the highest quality MBE InP to date using TEIn and phosphine. A 77°K mobility of 105,000 $cm^2/Vsec$ at a carrier concentration of $9 \times 10^{13}/cm^3$ was achieved. This is comparable

to the best LPE and MOCVD material. Lastly, Tsang, et al.,[340] using TEG, TMIn and arsine, have grown InGaAs on InP with the highest quality epilayers of any technique.

Gas source MBE promises to solve two of the biggest roadblocks to production MBE: throughput and defect density. Gas sources offer the obvious advantage of being essentially inexhaustible thus reducing the downtime associated with conventional source replenishment. Also, there should be advantages in terms of large (<3 inch) diameter wafer uniformity that accrue from gas distribution designs. Although this has not yet been demonstrated, excellent compositional uniformity has been achieved without wafer rotation using gas sources.[341] Further, it appears that the growth rate can be increased from 1 micron per hour to somewhere between 3 and 6 microns per hour and possibly higher depending on the material system in use. Finally, the growth contribution to oval defects appears to be eliminated with gas sources. Tsang[324] has reported the absence of oval defects in GaAs and InGaAs grown with TMG or TEG and TMAs, whereas oval defects occurred when elemental gallium sources were used with either elemental $As_4$ or cracked TMAs. Assuming that satisfactory gas quality can be consistently supplied, the biggest drawback to gas source MBE would be the safety issues associated with the highly toxic hydrides and the pyrophoric alkyls. The required safety monitoring and protection equipment are nontrivial capital costs for many potential users.

## 6.5 Superlattice Structures

Superlattice structures were among the first MBE structures conceived.[342] Such structures exemplified the film growth capabilities of the MBE process and were virtually impossible to fabricate by any other technique at that time. Superlattice structures can be divided into two general classifications: compositional (or heterostructure, including modulation doped superlattices) and doping (or homostructure). Epitaxial superlattices of lattice mismatched materials have been grown when the layers are sufficiently thin and are known as strained-layer superlattices (SLSs).

**Strained-Layer Superlattices.** When materials of sufficiently large lattice mismatch are grown on top of one another, a dislocation network is formed at the interface to accommodate the resulting strain. If the overgrowth is sufficiently thin, however, the accommodation will be absorbed entirely by a variation from the bulk lattice constant. Alternating thin layers of two such materials will result in a superlattice whose electronic

properties can be adjusted within certain limits by pair choice and layer thickness.[343] For example, direct gap SLSs have been grown from the indirect-gap couple: GaP and $GaAs_{0.4}P_{0.6}$ and low current level optoelectronic devices have been proposed.

Several III-V SLSs have been grown: GaAsP/GaAs, GaAsP/GaP, and InGaAs/GaAs. Recently, $InSb/InAs_{0.26}Sb_{0.74}$ MBE SLSs have been successfully grown by Lee, et al.[344] $Ge_xSi_{1-x}/Si$ SLSs have been grown by Bean, et al.,[345] and investigated for their unique optical properties. A Sb modulation-doped $Si/Ge_{0.45}Si_{0.55}$ SLS grown by Jorke and Herzog[346] yielded a 5x enhancement in room temperature mobility. MBE HgTe/ZnTe SLSs were successfully fabricated for the first time by Faurie, et al.,[347] and CdTe/ZnTe SLSs have been grown by Monfroy, et al.[348]

**Superlattice Buffer Layers.** Superlattice layers have received considerable attention for their potential to improve device performance. It is proposed that the superlattice prevents the propagation of threading dislocations and substrate contaminants into the active overlayers. SL buffer layers may eliminate the need for a thick (about 1 micron) undoped GaAs layer. Fujii, et al.,[349] have reported GaAs/AlGaAs GRINSCH lasers with a 175 A/cm$^2$ minimum threshold current density, the lowest reported for a similar cavity length. The buffer layer consisted of 5 couples of 150 Å GaAs and 150 Å $Al_{0.7}Ga_{0.3}As$ spaced 1.5 microns below the quantum well active layer. Noda, et al.,[350] used a GaAs/AlAs superlattice buffer to improve the interface of a self-aligned structure laser, thus reducing the threshold current by 8–12%. Schaff and Eastman[351] have improved GaAs power FET performance using a 100 layer, 270 Å period AlGaAs/GaAs SL buffer layer. Morioka[352] has succeeded in growing GaAs on indium doped substrates using a 2 micron, 20 period superlattice of 100 Å GaAs and 100 Å AlAs. The PL improved substantially over that normally seen from material grown on 1% indium doped substrates and was comparable to chrome-doped substrates at 0.1% indium. Superlattice buffers have also been used to assist the growth of GaAs on silicon (see Sec. 6.2).

**Superlattice Device Structures.** Superlattice structures have played prominently in the development of new devices. MQW lasers, avalanche photo diodes and superlattice HEMTs have been mentioned earlier, for example. New devices exploiting the tunable electronic and optical properties afforded by doping superlattices have begun to emerge. Schubert, et al.,[353] and Vojak, et al.,[354] have reported on efforts to extend the useful optical limit of AlGaAs/GaAs above 0.9 micron. Other materials

have also been considered. InAsSb SLSs have been proposed for 8–12 micron detectors[344][355] because of the potential advantages of such devices over HgCdTe. Temkin, et al.,[356] and Pearsall, et al.,[357] have extended the spectral response of silicon photodetectors to 1.3 microns using a $Ge_xSi_{1-x}$/Si SLS. The approximately 6000 Å thick SL served both as the absorbing medium and to prevent the propagation of threading dislocations. Pearsall, et al.,[357] succeeded in showing an avalanche multiplication of 50 at 1.1 microns while Temkin, et al.,[356] have measured a photoconducting gain of 40 at 1.3 microns and projected a 200 Mb/s data rate over 25 km. Faurie, et al.,[358] have proposed new IR detector materials from HgTe/CdTe superlattices. These SLs should have a weaker energy gap temperature dependence than comparable HgCdTe detectors operating in the 8 to 12 micron range.

## 7.0 FUTURE DEVELOPMENTS

### 7.1 Production Equipment

The demand for production capable MBE equipment has developed naturally from device demand. Devices which were spawned in the research lab have become desirable and mass producible. The MBE equipment required to demonstrate such devices is considerably different from that needed to produce it in volume. Whereas, second generation MBE machines were designed to offer maximum versatility, a production machine can be defined more specifically since a particular material system or device is sought. The emphasis shifts from configurational flexibility to reliability, both of the process and the hardware. Production equipment, based on an established process, must maintain that process wafer-to-wafer. The justification for any piece of production equipment is a low ratio of the cost per device to the value added per device. Step yield, maintenance costs and downtime are contributors to the cost per device.

Some devices allow such a value added that MBE is without question the process of choice. In cases where the device structure relaxes process constraints, other approaches such as MOCVD may be competitive or superior to MBE on a cost per device basis. Current efforts among MBE equipment vendors are focused on increasing wafer throughhput and reducing system downtime and capital costs. At present, the major markets are for AlGaAs/GaAs analog (microwave) and digital devices. The next larger markets are for other III-V materials for microwave and

optoelectronic devices. Many of the devices in these markets require sophisticated processing and have a high added value. Second generation equipment was an attempt to address these markets and such machines are today producing device material for commercial use. Multichamber processing, multiple wafer load lock chambers with preprocessing capabilities, three-inch wafer compatibility and high uniformity have all contributed to demonstrating MBE's production worthiness.[92][126] Other advances are needed for the next generation of production MBE equipment.

The critical issues for production MBE are throughput and material quality. Batch processing, at least on the scale traditionally achieved using CVD, will probably never be attained by MBE, but small three to five wafer loads are certainly feasible. It is possible, in principle, to maintain the superior thickness and doping uniformity specifications over several wafers simultaneously. Compositional control should likewise be excellent across such a small batch. This may be accomplished using conventional sources, but it is likely that gas sources will be required. Recently, growth rates in the 3 to 5 microns per hour range have been reported using gas sources.[124] Excellent morphology is also claimed. The question of source gas purity remains an issue, however. There must be a reliable supply of high purity gases in order to maintain consistent material quality.

In order to reduce die costs, future production MBE equipment will be expected to meet critical uptime levels. Gas sources could further this goal by virtually eliminating the downtime associated with refilling conventional effusion cells. Load-locked, large volume cells are the only alternative where factors such as toxicity preclude the use of gas sources by certain device manufacturers. Combining the throughput advantages of gas sources with cassette-to-cassette automated wafer handling and real time in situ growth monitors should allow throughputs in the 20 to 50 wph range for one micron of material growth. Uptime requirements will also demand reliable hardware and advanced automation. Sophisticated system automation will monitor all aspects of the system, reducing the necessary operator skill level and providing diagnostics to assist service. Eventually, expert systems and robotics will eliminate operators entirely.[359] Third generation III-V production systems are currently under development by all major equipment manufacturers.[115][360] Although the market for silicon MBE is less well defined, production MBE equipment for large diameter silicon wafers has been developed.[361] A high-throughput production silicon MBE machine capable of handling 8-inch wafers is shown in Fig. 18.

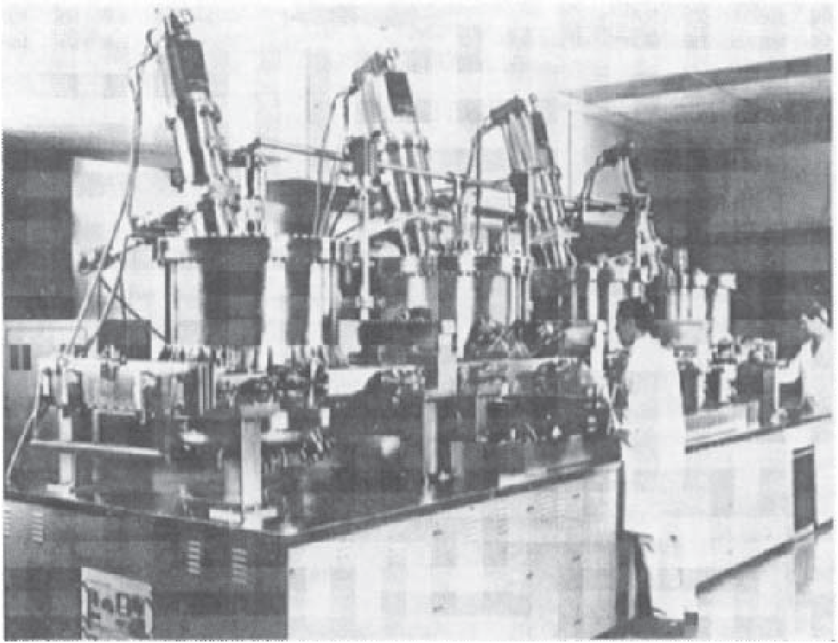


**Figure 18.** A silicon MBE production system with 200 mm wafer capability. *(Courtesty of J. C. Bean, AT&T Laboratories.)*

## 7.2 In Situ Processing

The UHV environment of MBE is considered by some to be the ultimate condition for processing microelectronic devices. For example, see Harbison.[362] Instead of surrounding all process steps with a clean environment, the ambient is contained within one piece of equipment. Such a scheme is a natural extension of existing efforts to control process conditions more tightly thereby increasing yield and reproducibility. Particulate contamination due to wafer handling and air exposure can be virtually eliminated with proper designs. An all-vacuum process could eliminate the need for Class 10 and better cleanrooms. Such an integrated process is still far in the future, but UHV deposition, etching, implantation, annealing and lithography have been demonstrated. Table 8 lists some examples. Current modular MBE systems lend themselves to the addition of additional processing (see Fig. 5). In situ cleaning, annealing, metallization and analysis (inspection) have, in fact, been common to second generation

equipment. There are current efforts to add laser and focused ion beam (FIB) processing. The joining of focused ion beam and MBE equipment has been put to practice by Miyauchi and Hashimoto.[363] They successfully demonstrated maskless FIB implantation of multilayer structures and showed that device quality was significantly improved by in situ versus interrupted growth of an imbedded stripe DH laser.

**Table 8.** In Situ Processing Elements

| In Situ Processing Elements |
|---|
| Metallization |
| Schottky contacts[251][253][364] |
| Non-alloyed contacts[250][365][366] |
| Shadow Masking[367]–[369] |
| Selective Epitaxy[370][371] |
| Ion Implantation[117][138][372] |
| Focused Ion Beam Processing[363] |
| Laser Annealing[383] |

## 7.3 Process Developments

Several epitaxial processes closely related to conventional MBE or MOMBE have been tried or suggested and are mentioned briefly below. These processes are rather less developed than MBE and it is unclear what their future role will be, but it is important to remember that at one time MBE was in a similar state.

**Ionized Cluster Beam Epitaxy.** An epitaxial growth technique with comparable hardware to MBE is ionized cluster beam epitaxy or ICBE. Film growth takes place on heated substrates in UHV using MBE-type source geometries. The fundamental difference is in the design of the effusion cells. First, the exit nozzle is restricted so that large aggregates of between 100 and 1,000 atoms are formed by adiabatic expansion of the source vapors into the vacuum. Second, some percentage of aggregates are charged by electron bombardment and accelerated toward the substrate (as with ionized sources, see Sec. 4.2) at 1–10 keV. The substrate is

bombarded by a mixture of ionized and neutral clusters. The virtues of this approach are higher surface mobility (lower growth temperatures) and higher sticking coefficients (higher maximum doping levels). Many metals and compound semiconductors have been epitaxially deposited on a variety of substrates. Much of the experimental work has occurred in Japan under Takagi and Yamada.[373]–[375] In the United States, work is underway at Rensselaer Polytechnic Institute with support from the Semiconductor Research Institute. Commercial ICBE equipment has been available, but in principle any MBE equipment could perform ICBE with a properly configured source.

**Vacuum Chemical Epitaxy.** Another epitaxial technique, vacuum chemical epitaxy (VCE), shares aspects of MOMBE and MOCVD. The process has been developed mainly by Fraas and co-workers at Chevron[376] and is shown schematically in Fig. 3d. Total pressure during growth is between 1 and 100 mTorr. This is in the region between MOMBE and low pressure MOCVD. System base pressures near $10^{-8}$ Torr are achieved with a turbo pump. Growth occurs through the pyrolysis of a Group-III alkyl and a hydride at the heated wafer. The hydride may be cracked at the gas inlet or a solid source cracker can be used (just as in MBE). Ternary and quaternary alloys can be deposited by premixing the alkyls and, separately, the hydrides. The reduced growth pressure results in an alkyl mean free path greater than the source-to-wafer distance (as in MBE). The hydride mean free path can vary depending on whether it is cracked, but it is generally in molecular flow across the wafer. The hot graphite reactor walls assist hydride decomposition and increase Group-V material incorporation efficiency. A typical growth rate is 5 microns per hour and Fraas has grown III-III-V and III-V-V alloys. A cold wall, diffusion pumped version of VCE has been used by Sugiura, et al.,[377] to grow InSb. The role of VCE relative to MOMBE and MOCVD has yet to be determined, but it is, in principle, a production capable technique.

**Irradiation Assisted MBE.** Several researchers are exploring the process advantages of assisting film growth by bombarding the substrate with either electrons, ions[378] or photons during deposition. Kondo and Kawashima[379] enhanced the lateral epitaxial growth of gallium arsenide over tungsten with hydrogen and gallium ion bombardment. Using gallium and hydrogen ions, they obtained single crystal layers at temperatures where polycrystalline growth normally occurs. The photo-assisted work follows similar ideas under development at higher pressures during CVD. If practical, benefits may arise from a lack of substrate heater (less

background contamination) and a tunable reaction chemistry using different laser frequencies. Takahashi[380] has reported photo-assisted MOMBE using an ArF excimer laser at 193 nm. A roughly linear relationship between pulse frequency and growth rate was found. Superlattice growth using switched lasers of different wavelength is proposed. Nishizawa, et al.,[381] have combined photoepitaxy and molecular layer epitaxy to grow GaAs using TEG and arsine. Elsner, et al.,[382] at IBM have proposed pulsed laser-assisted MBE of GaAs using a 694 nm ruby laser. The laser-assisted MBE growth of silicon has also been reported.[383] In this instance, the deposition was at room temperature and subsequently annealed with a 694 nm ruby laser. Films up to 4000 Å thick yielded a (2 × 1) LEED pattern on Si.[100]

## 7.4 Toxic Gases and Environmental Concerns

The use of hydrides and organometallics in MBE brings along the attendant hazards and requirements for safety. The hydrides of As and P are extremely toxic, and phosphine is additionally pyrophoric. The American Conference of Government-Industrial Hygienists have set threshold limit values (TLV) of 0.3 ppm and 0.05 ppm, averaged over an 8-hour period, for phosphine and arsine respectively. Although the metal organics are not considered as toxic, they are pyrophoric. Due to the pyrophoric nature of the metal organics and low TLVs of the hydrides, users must exercise engineering as well as administrative safety controls wherever these gases are stored, handled, used and disposed. Each area contains a potential toxic gas emergency. Engineering controls include designs to dilute potential gas leaks from fittings, cylinders, regulators, etc., and to incorporate adequate sensors and burn boxes. Administrative controls include the training of personnel and providing protective gear for personnel, instituting safety and emergency procedures and protecting the surrounding community from accidental gas releases. The latter includes toxic neutralization systems, such as burn boxes and scrubbers. Currently under study are less toxic sources of gaseous phosphorus[384] for OMVPE which may prove suitable for MBE.

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# 11

# Ion Beam Deposition

*John R. McNeil, James J. McNally, and Paul D. Reader*

## 1.0 INTRODUCTION

Ion bombardment of surfaces has been used in connection with thin film deposition for decades. The amount and type of ion bombardment greatly influences film structure and composition; this, in turn, determines optical, mechanical and electrical properties of the film. The bombardment can be achieved using a number of techniques, some of which are very simple. However, the highest degree of control of critical parameters (e.g., ion flux, energy, species, and angle of incidence) is provided by broad-beam Kaufman ion sources. This is because the gas discharge of the ion source is separate and removed from the rest of the deposition system. This is not the case with some other ion bombardment techniques used in film deposition. The discussion here is restricted to applications of the broad-beam Kaufman ion source. For discussion of other ion sources see Refs. 1–3.

The following material is consistent with the general nature of this volume in that application, or "how-to," aspects of ion beams for thin film deposition are emphasized. References are given to more in-depth technical treatments of several topics. For example, Harper et al.,[3] gave

an excellent review of modification of film properties provided by ion bombardment. The first two sections which follow are fairly general, while the section discussing applications is somewhat specific. This is a result of the backgrounds of two of the authors in optical materials. Also, the authors' approach is that it is more beneficial to discuss a few applications in detail rather than many applications in a cursory manner.

## 2.0 OVERVIEW OF ION BEAM APPLICATIONS

The general technology of broad-beam ion sources has been discussed adequately in the literature (see, for example, Ref. 1). This section covers a brief description of the construction of ion sources and cites specific examples of operational characteristics that impact the design of processing tasks.

The typical ion source consists of an enclosure containing electrodes, magnetic fields, ion accelerating grids, and emitters suitably arranged to sustain electron-bombardment ionization of a working gas. The arrangement of these components has been widely varied by many experimenters and analytically investigated by even more. The results invariably support the local mythology of what a "good" ion source should be. The many configurations and concepts incorporated in both commercially available and custom-built ion sources tend to overwhelm users upon initial exposure to the technology.

### 2.1 Categories of Kaufman Ion Sources

The following comments do not deal with the full range of ion source possibilities. They merely attempt to describe some of the design trends in an overview, using details only to illustrate extremes of the trends. Ion sources, like most apparatus, when highly optimized for a given process, tend to sacrifice performance in other areas. This tendency leads to grouping of types of sources that conform to the process parameters of interest.

Sputtering sources, those used to remove the maximum amount of material from a target in the minimum time, are one example. In general, beam uniformity is not of great importance. The source is usually operated at 1 to 2 kV. It is important that the beam strike the target and that the source not produce contaminants. The lower the gas flow rate, the better.

Frequently, operation with reactive gases is desirable—or even necessary—to control stoichiometry. These parameters usually dictate small to moderate diameter (2 to 15 cm) sources operating at close to maximum conditions. When large numbers of substrates need to be coated, larger diameter sources are used, and the source-to-target and target-to-substrate distances are increased. This geometric scaling results in inverse square losses, with a corresponding reduction in coating rate. Linear sources have been applied to this task to partially eliminate the losses associated with increasing distance. The linear sources permit reduced geometries. While the number of workpieces coated is also decreased, there can be a net gain in throughput in a significantly smaller working volume.

Another example is etching sources, which have significantly different characteristics. They generally operate at voltages below 1 kV, with some even optimized for voltages between 50 and 200 eV. Beam uniformity is normally critical, with a typical specification of ±5% across a significant fraction of the beam. Etching sources are characterized by highly developed grid systems which seek to present a high current-density beam of acceptable flatness to the workpiece. The workpiece is frequently mounted on a fixture which produces a complex, non-integer motion to compensate for the remaining non-uniformities of the beam. Etching sources are frequently required to operate with gases that react with the workpiece to enhance etch rate or selectivity.

Peculiar ion source shapes occasionally appear among etching sources because of the need to be consistent with the geometry of the workpiece or that swept by the fixturing. Beams and sources shaped to segments of circles or annular segments are available. Linear sources are used to sweep, in a push-broom fashion, around cylindrical fixtures or along continuous rolls of material (e.g., webs).

Similar to the etching sources are sources used for cleaning workpieces prior to deposition or used to simultaneously bombard coatings during the deposition process (enhancement sources). These sources usually have fewer uniformity requirements. For example, if approximately 50 Å of material is removed to clean the workpiece, then a large percentage variation in this amount can be tolerated. Relatively small sources can be used for the cleaning task, but they are generally operated at maximum performance to minimize cleaning time. The voltage and current density used for cleaning are sometimes determined by the material to be cleaned. As an example, a web of plastic materials passing under a high performance linear source moves at a rate such that the web is in the beam

for about one second. If the web motion is interrupted for three seconds, the web is melted. Further discussion of ion beam cleaning is given in a later section.

Enhancement sources provide ion bombardment to a surface being coated with material produced by magnetron, thermal, electron-gun, or ion sputter techniques. Enhancement sources are typically operated at low beam energies and current densities. This energy input into the growing film modifies the physical structure and growth characteristics of the film. It is possible to alter the crystalline phase of some films. Enhancement sources are frequently required to operate with reactive gas to control the stoichiometry of the film. Some arrangements permit constant exposure of the substrate to the beam, while other arrangements allow the substrate to pass through the beam occasionally, due to planetary rotation. The effects of the ion bombardment might not be the same for the two situations.

The point of this discussion is to make the reader aware of the wide variety of potential tasks that can be accomplished using broad-beam ion sources, and that the ion sources can be optimized for various tasks. Frequently, the optimization from one specialized task to another can be accomplished by something as simple as a grid change. Other optimization can require extensive hardware changes and include significant variations in control systems and operating procedure.

A good example of major change is the method of producing the ionizing electrons for ion source operation. The most popular method of producing ionizing electrons is by thermionic emission. One method to achieve this is the use of a bare refractory wire as an emitter. Another method makes use of a low work-function material dispersed through a tungsten slug that is heated inside an inert gas-buffered tube. The latter device is known as a *hollow cathode.* The simple thoriated tungsten wire has given good service as an emitter for many investigators. However, the wire is sputtered by the ions in the discharge, and this limits the cathode lifetime. The wire emitter also presents a problem when operated with reactive gases. In addition, some users find problems with both the heat and photon flux on sensitive workpieces, as well as contamination due to evaporated and sputtered filament material. The hollow-cathode emitter can be used for both the source discharge chamber emitter and the neutralizer emitter to solve these lifetime problems. Use of the hollow cathode does impose heat-up and cool-down constraints prior to venting the work chamber, but for long runs these factors become less critical. The hollow-cathode requires a supply of inert gas, usually argon or xenon, to buffer the

low work-function insert. Any gas may be used in the source discharge chamber, giving wide flexibility to the use of the hollow-cathode ion source.

Radio frequency discharges can be used to produce the ions that are accelerated to produce the beam; this has been under investigation since the early 1960s. Recent advances in efficient RF circuit components have allowed the control and impedance matching problems to be reduced such that reasonably reliable operation can be achieved. While the RF sources eliminate the hot emitter from the chamber, many electronic design, control, and stability problems remain to be investigated.

## 2.2 Operational Considerations

Ion sources that produce beams using electrostatic acceleration present certain potential problems. The beam is extracted and accelerated by significant DC potentials (200 to 2,000 V typically). The work chamber contains a moderate current ($\geq$ 1 A) beam and is filled with a dilute, conducting plasma. Care must be taken to electrostatically shield the high potential leads to the source. Electrical breakdown is possible between closely spaced leads, and this is enhanced by the dilute plasma.

Some ion sources are designed in which gas flow lines are isolated from ground potential near the ion source. Other sources have a conductive gas line at high voltage that passes through an insulator in the vacuum system wall and is electrically isolated outside the chamber. This line is often overlooked as a high voltage electrode.

The pressure inside the gas line goes from a few psi above atmospheric pressure at the gas bottle to approximately $10^{-3}$ torr in the ion source plasma region. Screens and metal wool pads are frequently used to provide large area surfaces on which ions can recombine. This prevents electrical breakdown in the gas feed tubes.

Oxidation can occur if a hot ion source is vented to atmosphere too soon after operation. The oxide films on the various electrodes can become sufficiently insulating to prevent source operation on a subsequent pump down. Similarly, sputtering or etching of materials in a reactive atmosphere can produce insulating coatings. To avoid problems due to this, regular cleaning of the ion source is important. This can be accomplished mechanically, for example, using bead blasting, or chemically, using acids to remove thin film material.

## 3.0 ION BEAM PROBING

The applications of ion beams to coating discussed below require knowledge of the ion flux at the target. In some applications, such as ion assisted deposition (IAD) in which the target is the substrates being coated, this is very important; knowing just the total beam current is not sufficient. In this section, probe construction and operation are first discussed, and then use of the probe as related to film deposition is discussed. Only applications of the probe to measure particle flux are addressed here.

Probes can also be used to determine charged particle energy. Typically ions from a Kaufman ion source are nearly monoenergetic; they have an energy spread of approximately 10 eV centered about the anode potential (i.e., beam energy) for the dual grid extraction arrangement.[3] Ion energy spread in the beam from a source with a single grid arrangement is somewhat larger.[3] However, because beam energy characteristics are fixed by discharge conditions and are rarely measured by the user, this probe technique will not be discussed in further detail.

The ions and neutralizing electrons in a beam can be considered a weakly ionized plasma, or gas discharge. Plasma probe technology can be applied to monitor the beam conditions. For details, many references on plasma probes are available.[4] Only the relevant technology will be discussed here. A simple arrangement which is widely used is the planar Faraday probe illustrated in Fig. 1(a). The probe is connected to an electrical vacuum feedthrough with a shielded conductor. The shield is connected to the part of the probe which encloses the probe element. Note that the back of the probe element is also shielded to avoid ion current contribution from this region. The probe element diameter is typically 5 to 10 mm, and it is recessed into the shield enclosure by approximately the same amount. This maintains approximately the same sheath dimensions and effective probe area with minor variations in probe bias voltage. Insulators of alumina can be used to separate the probe element and the shield enclosure. This separation should be as small as convenient, with approximately 0.5 mm being typical. An easily constructed, simpler, though perhaps less accurate, version of a probe is shown in Fig. 1(b). In this case, the probe element is mounted on a sheet of insulating material such as mica, and this is fastened to a piece of metal (e.g., Al) plate. Again, the back of the probe and the electrical conductor are shielded to avoid extraneous sources of ion current. The entire probe arrangement,

whichever form is used, should be constructed such that it is easily disassembled for cleaning.

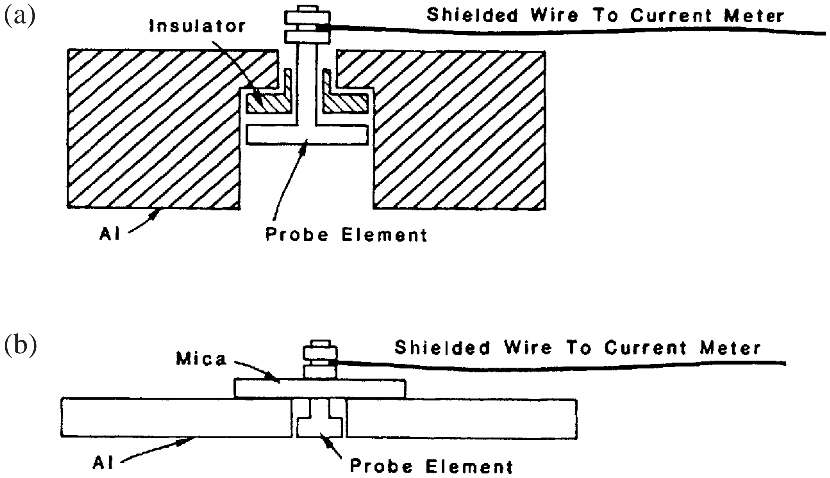



**Figure 1.** Two arrangements of a Faraday probe to monitor ion beam current; (*a*) more accurate version and (*b*) simple version. Note, in both arrangements the back side of the probe should be shielded (e.g., with Al foil) to prevent ion current contribution from this region.

Outside the vacuum system, the probe can be biased, and probe current can be measured with a meter connected in series with the arrangement. If the probe is to be used to measure ion current density, and therefore to calculate ion flux, the bias should be approximately -30 V. This potential repels electrons from the beam, and the measured current is primarily due to the ions. If the probe is perpendicular to the beam, then the ion current density is approximately equal to the measured probe current divided by the probe element area. The ion flux ($I'$) is calculated by dividing the current density by the ion charge $q$. For example, if the probe current is 25 μA and the probe element is 1 cm in diameter, the current density and ion flux are given by:

Eq. (1)
$$
\begin{aligned}
J &= I_p/A_p \\
&= 25/\pi(0.5)^2\ \mu\text{A/cm}^2 \\
&= 31.8\ \ \mu\text{A/cm}^2
\end{aligned}
$$

and

Eq. (2)

$$\begin{aligned}\Gamma &= J/q \\ &= 31.8 \times 10^{-6}/1.6 \times 10^{-19} \\ &= 19.9 \times 10^{13} \text{ ions/cm}^2\text{-sec}\end{aligned}$$

the latter could, for example, be used for comparison with the flux of thin film molecules at the substrate.

As Kaufman discusses,[3] there are two sources of error in the probe current measurements described above. First, ions striking the probe surface can cause secondary electrons to be emitted from the probe. Because the probe is biased negatively, the electrons are repelled, and this constitutes a current which is additive with that of incident ions. Because the probability of secondary electron emission from the metal surfaces involved (e.g., Al, stainless steel, etc.) at the ion energies employed is of the order of 0.1, there is little error introduced by this effect. The second source of error involves secondary (charge exchange) ions produced by the high energy ions of the beam. The probe will collect both types of ions, and therefore give an erroneously high current reading. Unless the background pressure in the vacuum chamber is abnormally high, this effect is generally negligible except at the outer edges of the ion beam. At this point, the density of the secondary ions can be relatively high compared to that of the beam ions, and one might think the extent of the beam is greater than it actually is.

When this arrangement is used while depositing conducting film materials, no special precautions are necessary. The probe element should remain insulated from the rest of the probe body, and the electrical characteristics of the probe element should remain constant. The probe might be moved into the ion beam just prior to substrate cleaning, sputtering, or whatever the application, in order to check the beam condition. The probe would then be moved out of the beam.

When insulating materials are being deposited, care should be exercised to prevent the probe element from becoming coated. This would change the probe characteristics to provide incorrect indications of ion beam current density. During coating, the probe might be moved to an area where it is shielded from coating material, or the probe might have a shield attached. If the beam is to be monitored during coating, some deposition on the probe element is inevitable, and the probe should be later cleaned.

## 4.0 SUBSTRATE CLEANING WITH ION BEAMS

Substrate condition prior to coating is extremely important for proper film adhesion; in addition, it has an influence on subsequent film growth characteristics. The general topic of substrate cleaning is very diverse and will not be treated here. What is discussed is the application of ion beam apparatus as the final step of cleaning a surface immediately before film deposition. Results of ion beam cleaning and the improved adhesion of films which this can provide, such as Au on BK-7 glass, are discussed in Ref. 5. For a general treatment of substrate cleaning techniques. (See, for example, Ref. 6.)

Bombardment with ions and electrons to clean a surface has been commonly used for many years, primarily by employing a glow discharge in the deposition system. However, with this so-called "glow discharge" technique, one has very little idea of what species is actually bombarding the substrate, or the energy and flux of the bombarding species. Use of the ion beam apparatus to provide the particle bombardment affords more control of the important system parameters such as ion species (reactive or inert), flux, and energy. The same parameters are not only known, they are in large part independently controllable. This, combined with proper beam probing techniques discussed previously, make the process very useful for cleaning and bombardment during early stages of film growth. With a neutralized beam, conducting and insulating substrates can be treated. Ion beam cleaning obviously represents no added equipment to the deposition system if ion assisted deposition (IAD) is employed. See a later section.

The processes which occur on the substrate due to ion and electron bombardment include a number of things. This includes desorption of adsorbed water vapor, hydrocarbons and other gas atoms. Adsorbed gases are very efficiently desorbed at low energies (~300 eV). Chemisorbed species and possible occluded gases are sputtered. If the bombarding ion is an oxygen species, chemical reactions with organic species on the surface can result in compounds which are more volatile and hence more easily removed.[6] For the levels of ion flux and energy employed, and for the small time required for cleaning, the substrate temperature rise is usually negligible, and this has little effect on substrate outgassing. Ion bombardment causes substrate defect production which, in general, is beneficial for subsequent film nucleation and adhesion.

Typically, the level of ion flux at the substrates used during precleaning is several tens of μA/cm$^2$. In this application, uniformity of current density is not as important as it is for other applications such as IAD. Because of this, small ion sources are useful provided they have sufficient total beam current. Relatively low energy (~300 eV) ions are preferable to higher energy ions to minimize substrate sputtering, while still being sufficiently energetic to produce the effects mentioned above. A mixture of Ar and $O_2$ can be used as the gas species in the ion sources. As an example, consider a 30 μA, 300 eV beam from a 2.5 cm diameter ion source which is directed at substrates approximately 30 cm away. At the substrates, depending somewhat upon the vacuum chamber pressure, the peak current density would be approximately 160 μA/cm$^2$; the width of the beam (FWHM beam current density) would be approximately 17 cm. If the deposition chamber dimensions permit, the ion source should be placed farther away to provide a larger, more uniform beam at the substrates. If there is only single-axis rotation of the substrates, the ion source might be placed directly below the center of the substrates; if it is not directly below the substrates, then the beam pattern is simply spread over a larger area. In either case, it might be advantageous to direct the beam off-center of the substrate fixturing if the fixturing is much larger than 17 cm in diameter. If the fixturing involves planetary rotation, then the beam should be directed to a region that will ultimately provide bombardment of all substrates. In this case, the ion beam is obviously not on a particular substrate continuously; it is "time-shared" between all substrates. This, however, does not present the potential problems that are discussed in connection with IAD of substrates in planetary arrangements.

To estimate the time required for cleaning substrates, one should consider the amount of material which is sputtered. This is determined in part by the sputter yield of the substrate material and that of the unknown species on the substrate. Sputter yields for many materials are well characterized for various incident ions and ion energies; typical values range from 0.1 to 3 atoms/ion for inert gas ions of approximately 0.5 to 2 keV energy.[7] If a sputter yield ($S$) of 0.1 atoms/ion is assumed, the thickness ($L$) of the layer of material removed in five minutes ($t$) due to a beam of 50 μA/cm$^2$ current density ($J$) is given by:

Eq. (3)
$$\begin{aligned} L &= SJVt/q \\ &= (0.1)(50 \times 10^{-6})(27)(300)(10^{-16})/1.6 \times 10^{-19} \\ &= 25 \text{ Å} \end{aligned}$$

here *V* is an assumed volume of the sputtered atoms, taken to be 27 Å,[3] and *q* is the charge of the ion in coulombs. The factor of $10^{-16}$ in the equation is included to express the layer thickness in angstroms. This calculation illustrates how several atomic layers of material can be quickly removed from the substrate to leave it atomically clean. This should actually be considered a maximum estimate of substrate material removal. The adsorbed species on the surface are, in general, much easier to remove and have a large effective sputter yield. If the beam is "time-shared" as described above in connection with planetary fixturing, then one must estimate the fraction of time *F* the substrates are in the ion beam; in the expression above, *t* would become *t/F*.

There are four considerations one should be aware of in applying ion bombardment, regardless of the technique, to clean substrates. The first has to do with the influence of ion bombardment on the substrate microroughness. If the substrate is polycrystalline and composed of relatively large crystallites, the microroughness of the substrate might increase significantly if the substrate is ion-bombarded for a very long time. This is due to the crystals in the substrate sputtering at different rates and therefore different amounts being removed, depending upon their orientation to the incident ions. See Fig. 2. For example, Cu substrates have demonstrated an increase in rms roughness from approximately 25 Å to nearly 50 Å when 1200 Å of the substrate was removed using ion beam sputtering.[5] This amount of material removal is somewhat severe in terms of substrate cleaning, but it illustrates the point. On the other hand, amorphous or very small-grained polycrystalline substrates, as well as single crystalline materials, do not present a problem. For example, glass substrates (e.g., fused silica, Zerodur, and BK-7) have been ion-beam milled several microns deep with no noticeable increase in roughness, starting with substrates as smooth as 7 Å rms roughness.[8] Electroless Ni films have been examined in this same manner, and they do not display an increase in roughness with ion milling.

The second consideration when applying ion precleaning is that the stoichiometry of the top few atomic layers of substrates composed of molecular species, can be altered. This is due to the ions preferentially sputtering one atomic species from the top molecules, leaving the surface rich in the other atomic species. The extent of this altered layer production is naturally minimum with minimum ion energy (for energies less than approximately 2 keV) and flux, while the impact of it depends upon the application of the coated substrate. In the case of fused silica and other

glass substrates, the effect is not noticeable in optics used in routine, as well as severe, applications such as high energy laser optics.[9] Similarly, fused silica samples which were ion milled several microns and examined with an ellipsometer displayed no change in optical constants. In this case, the effects of the altered layer were either negligible or exposure to atmosphere made them so. The situation in the case of other substrate materials might not be as favorable as that for glass materials, and one should be aware of potential problems.

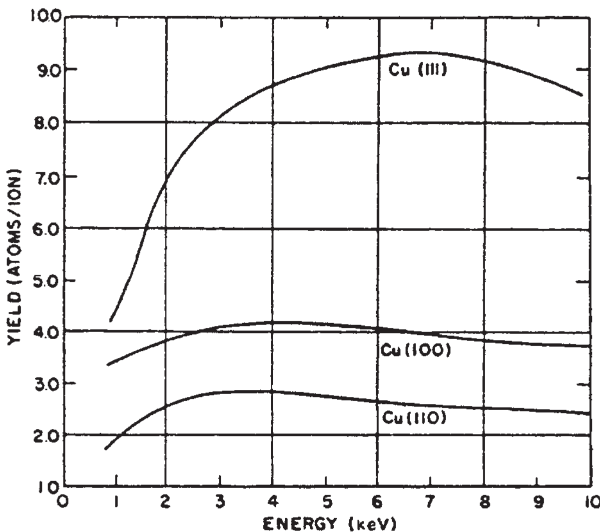



**Figure 2.** Sputter yield, *S*, of three planes of Cu bombarded by normal-incidence $Ar^+$ ions.[7]

A third consideration when applying ion beam precleaning involves the potential damage to crystalline substrate surfaces such as semiconductor materials. It is very difficult to obtain a clean semiconductor surface and maintain the bulk properties at the surface; atoms in the crystal lattice structure are dislocated due to the ion bombardment. A general guideline is to reduce the ion energy to the lowest level possible if substrate damage is a concern. The dislocation energy of an atom is typically a few tens of eV. The sputter yield of adsorbed molecules should be sufficient at the reduced ion energy to provide the desired cleaning with minimal substrate damage.

A fourth consideration in applying ion precleaning involves contaminating the surface of the substrate being cleaned with the material from the fixture holding the substrate. Slight contamination, especially around the periphery of the substrate, is unavoidable. When possible, the fixturing should be constructed of material which is compatible with the coating. For example, in deposition of oxides for optical applications in which a high background pressure of $O_2$ is present, the fixturing might be constructed of Al. In this case, the contaminant from the fixturing could be present in the form of $Al_2O_3$ which is harmless in most cases.

## 5.0 APPLICATIONS

Two general arrangements are most popular for application of the ion source to thin film coating. First, ions from the source can be directed at a target which is sputtered, and the sputtered material is deposited as a thin film. This is termed *ion beam sputter deposition* (IBS). Second, ions from the source can be directed to the substrate which is being coated with material generated by some independent technique. This is termed *ion assisted deposition* (IAD). In both cases, the intent is to provide the thin film adatoms on the substrate with increased energy and therefore more mobility prior to nucleation. This leads to the modifications in film properties mentioned previously. Two or more ion sources can be used simultaneously to provide both IBS and IAD. These two processes are discussed in detail in this section.

### 5.1 Ion Beam Sputtering

Aspects of ion beam sputtering which are described here first include a brief review of sputtering parameters and results. This is necessary, for example, to describe some of the advantages and disadvantages of ion beam sputtering compared to other forms of sputtering. Detailed treatments of sputtering are given in Refs. 1, 7 and 10. Next, several aspects of ion beam apparatus and other experimental details are described. Last, a summary of film properties provided by ion beam sputtering is given.

**Aspects of Sputtering.** When an energetic ion or neutral atom strikes a surface, many processes can occur. One of these is the ejection of atoms of the surface target material, and this is known as *sputtering*. Of primary concern in sputtering is the sputter yield *(S)*, in atoms/ion, and the relation of

*S* to parameters such as ion and target species, ion energy, ion incident angle, and target condition. In addition, it is very important to have an idea of the average ejection energy of sputtered atoms, as this has a significant influence on resulting thin film properties. Similarly, the angular distribution of the sputtered atoms is important in determining film deposition rate and uniformity. The following is a summary of relevant aspects of sputter yield and sputtered particle properties taken from Refs. 1, 7 and 10.

*Sputter Yield*

*(a)* *S* has a threshold level of approximately 10 to 30 eV for most ion/target combinations. It increases exponentially with ion energy up to 200 or 300 eV (see Fig. 3) and increases approximately as $E^x$, where $0.5 \leq x \leq 1$ for ion energies up to several keV.[1] At higher ion energies, *S* decreases, most likely due to implantation.

*(b)* *S* increases for many target elements with increasing mass of rare gas ions. For example, for 500 eV ions incident on Ta, *S* is 0.01, 0.28, 0.57, 0.87 and 0.88, respectively, for He, Ne, Ar, Kr, and Xe.[11]

*(c)* *S* increases with ion angle of incidence to the target, up to angles of approximately 45 to 60 degrees. The increase can be as great as a factor of two or more; at larger angles of incidence, *S* decreases. See Fig. 4.[1][10]

*(d)* *S* can be different for different crystal orientations of the same material.

*Sputtered Particle Energy*

*(a)* Average ejection energies increase with incident ion energy up to roughly 0.5 to 1.0 keV, above which the energy of the sputtered particle increases little.

*(b)* For the same incident ion species, materials with lower sputter yield tend to have higher ejection energies.

*(c)* For the same target material, average ejection energies tend to increase for heavier bombarding ions.

*(d)* Average ejection energy tends to increase with ion angle of incidence.

*(e)* There is not a significant dependence of the sputtered atom ejection energy upon crystal orientation of the target.

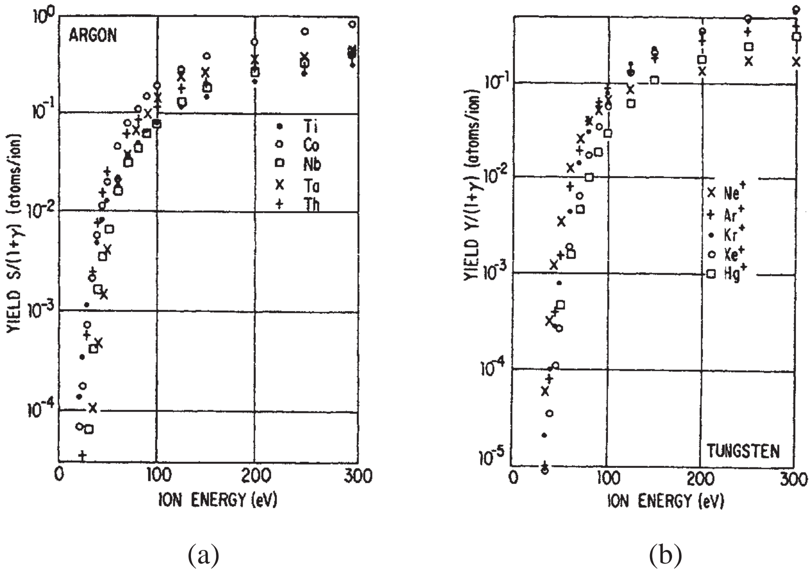



**Figure 3.** Sputter yield, *S,* vs ion energy; (*a*) shown for several materials with $Ar^+$ bombardment, and (*b*) for W bombarded by different ion species.[10] *(Reproduced with permission from Maissel and Glang,* Handbook of Thin Film Technology, *McGraw-Hill, 1970.)*

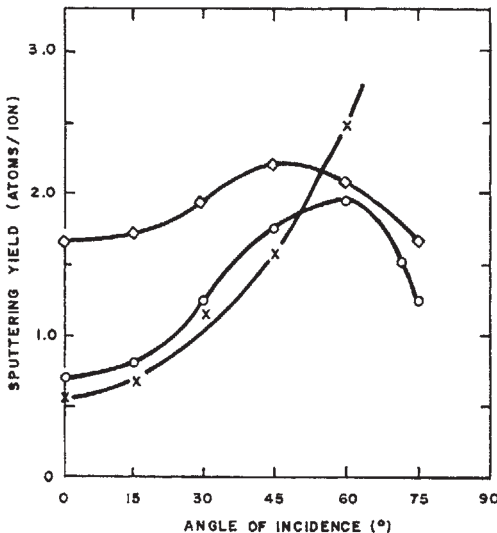



**Figure 4.** Effect of angle of incidence on sputter yield; ◊: gold, O: aluminum, and ×: photoresist.[30] *(Reproduced with permission from Vossen and Kern,* Thin Film Processor, *Academic Press, 1978.)*

***Angular Distribution of Sputtered Atoms.*** In general, the angular distribution of sputtered particles is peaked in a forward direction, at an angle roughly comparable to that of the incident ions. A cosine distribution has been used to describe this, although several factors have an influence. In particular, the target condition is very important. For example, the target can be single crystal or polycrystalline, and there will be different effects on the distribution pattern. In addition, the distribution changes in the case of a new target that is being used for the first few hours. A target of solid material will provide a distribution pattern different from that of one made of pressed powder. In addition, if the target is arranged at a different angle with respect to the ion beam, the distribution pattern would be different as well. Energy of the incident ions has been observed to have an effect on the sputtered particle distribution.

From what has been described, it is apparent that the best approach to characterize the distribution pattern in applications in which it is critical is to directly measure it. For example, sample substrates might be located at various positions relative to the target and then coated. Film deposition rate and uniformity could be determined from coating thickness measurements using a spectrophotometer or other types of interferometry.

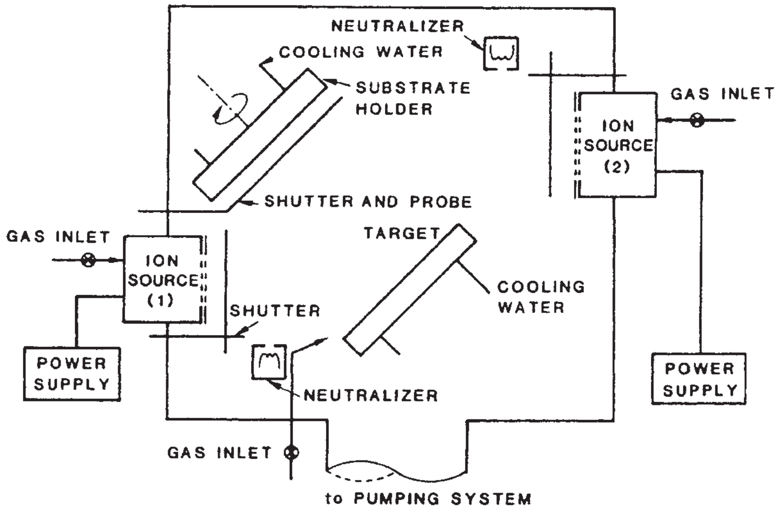
**Advantages/Disadvantages of Ion Beams for Sputtering.** In sputter applications, ion beams provide control of ion energy, flux, species, and angle of incidence. These parameters are not only controllable over a wide range, they can be controlled nearly independently of each other. This represents significant advantages compared to other forms of sputtering. In addition, the gas discharge of the ion source is contained and separate from the rest of the deposition system. From the discussion above, it can be seen that having an ion energy of 1 to 2 keV is desirable for higher sputter yield and higher sputtered atom energy. In the case of magnetron sputtering, for example, the incident ion energy is, at most, equal to the energy provided by the cathode fall voltage (typically 600 V), and it could be less due to charge transfer collisions in the region above the cathode. In addition, the ion energy can not be controlled over a wide range, and it is closely coupled to the magnetron discharge current. Being able to arrange the sputter target at an angle to the incident ion beam is advantageous both in terms of sputter yield and sputtered atom energy, as well as allowing flexibility in the experimental arrangement. In the case of magnetron sputtering or other processes in which the sputter target is in

contact with the gas discharge, there is no control of the ion incident angle. Ion beam sputtering allows greater flexibility in target material and composition than in other forms of sputtering. This is discussed below in connection with targets. In addition, the species in the ion beam can be easily and accurately controlled by adjusting the flow of one or more types of gas through the source; reactive (e.g., $O_2$, $N_2$ etc.) or inert ion species can be present in practically any ratio desired. This is not the case with other forms of sputtering. The low background pressure present during ion beam sputtering might lead to less gas inclusion compared to other processes. However, the deposition geometry should be such that the substrates are not bombarded with energetic neutralized ions which are reflected from the target. In this case, the incorporation could increase significantly due to a larger sticking coefficient of the energetic atom.

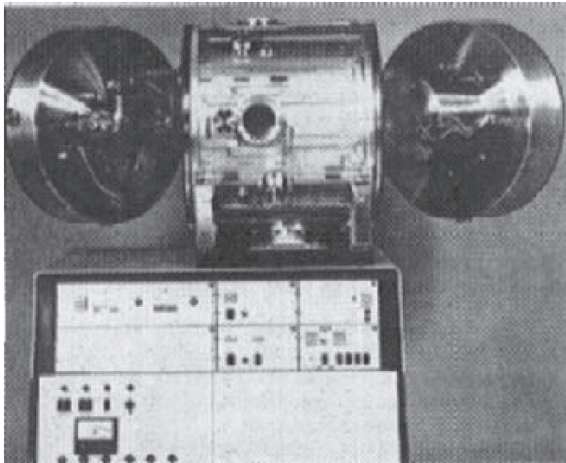
An obvious disadvantage of the application of ion beams in general is the added expense and complexity of the coating process. However, neither of these is severe. Another disadvantage is that it is more difficult to scale the ion beam sputter process compared to magnetron or some other sputter process. Geometries of the ion beam sputter arrangement must sometimes be small in order to provide reasonable deposition rates, and this might be a problem.

**Aspects of Ion Beam Sputter Apparatus.** Figure 5 illustrates the apparatus used in ion beam sputtering. Two ion sources are shown in the figure; one is used for sputtering and the other is used for bombarding the substrate prior to coating or during deposition (i.e., IAD). Also shown is a probe to characterize the beam in the vicinity of the target, as well as the other shutters typically found in a deposition system.

***Vacuum Chamber.*** Chamber size requirements are influenced little by the addition of a small ion source; more elaborate arrangements such as illustrated in Fig. 5 require a specially designed system. Typical size of the arrangement shown in the figure is roughly 50 cm in diameter. Similarly, vacuum pumping requirements are not influenced greatly by the addition of a small ion source; typical added gas load is 2 to 4 $cm^3$/min for a 2.5 cm diameter ion beam source. A 6-inch diffusion-pumped or cryogenically-pumped system will typically operate in the $10^{-5}$ to low $10^{-4}$ torr region with this gas load. Incorporating large ion sources into a system may require additional pump capability.




(a)



(b)

**Figure 5.** Ion beam sputter apparatus. Although the vacuum system shown here is designed specifically for IBS, the same ion beam apparatus could be added to an existing vacuum system.

The arrangement of the sputter target and the substrates is often as illustrated in Fig. 5. A typical separation between the ion source and the target is 30 cm. The target is arranged at an angle of approximately 45 degrees to the ion beam to optimize the sputter process as discussed above. The energetic neutralized ions which are reflected from the target can, in some situations, be detrimental to the film if they are allowed to bombard the substrate. This is the case, for example, when high quality oxide films are being deposited using Ar ions to sputter a target and with an $O_2$ partial background pressure.[12] To minimize this effect, the substrates are arranged as shown in Fig. 5. Although the neutralized ions do not all reflect in a specular sense, it is believed they are predominantly directed in this direction.

***Ion Sources.*** For ion beam sputtering, it is usually desirable to deliver as much ion current to the sputter target as possible, and this dictates the use of large ion sources (e.g., 10 to 15 cm diameter). Wire filament cathodes and neutralizer can be used which are made of W or Ta, and typically 0.010 to 0.015 inches in diameter. Both have lifetime limits of several (one to over ten) hours. Lifetime of the neutralizer is increased if it is placed near the edge of the ion beam and not through the center. This can be tedious to achieve, as the beam profile and, therefore the position of the neutralizer, are somewhat dependent on operating conditions (pressure, beam energy, etc.). Both the cathode and neutralizer lifetime are greatly reduced if a reactive gas is used in the ion source. In addition, the W or Ta material can contaminate the target and be deposited in the film at a low level. In place of the wire cathode, a hollow cathode discharge device can be used to supply electrons to the main discharge of the ion source. Although this operates very well with inert gas, operation with $O_2$ has not been satisfactory. Similarly, the wire neutralizer can be replaced with an auxiliary discharge device, a plasma bridge neutralizer, to supply neutralizing electrons to the beam. This must remain outside of the beam to avoid being sputtered and contaminating the target material. Another approach is to construct the housing of the plasma bridge neutralizer of a material which is compatible with the target and film.

***Targets.*** Target size should be sufficient to insure that none of the beam passes the target and sputters other material. In optical coating arrangements in which large ion sources are used, target size is typically 20 cm wide and 30 cm long. Placement of the target and the influence of this on the distribution of sputtered atoms has been discussed previously.

In the case of optical coatings, elemental targets of Si, Ti, Ta, etc., are often preferred because of the higher sputter yields and therefore large deposition rates provided, compared to targets composed of the oxide materials. In this particular situation, Ar ions are often used to sputter the target; a second ion source, possibly with a single-grid arrangement to provide low energy ions, is often used with $O_2$ to improve film stoichiometry by IAD. Deposition rates of 1 to 2 Å/sec can be achieved.[12] Similar techniques can be used in the case of nitride film deposition. This arrangement is illustrated in Fig. 5.

In general, there is no restriction placed on a target used in ion beam sputtering; the target can be an insulator since the ion beam can be neutralized. Sputter targets are often water-cooled due to the incident power (e.g., 0.25 A at 1,500 V in vacuum).

A technique which has been used to ion-beam sputter compounds of materials involves placing pieces of one target material on a second target material. The film composition depends on the relative sputter yields, the relative areas of the targets which are sputtered, and the relative sticking coefficients of the atoms at the substrate.

**Properties of Ion Beam Sputtered Films.** Harper[1] has described the properties of thin films deposited by ion beam sputtering. These include superior adhesion and denser film structure, both attributed to the higher energy of the sputtered particles. The improved adhesion was observed for films produced with and without ion precleaning. The superconducting transition temperature, $T_c$, of ion-beam deposited transition materials has been found to increase over bulk values for some metals and decrease for others. The effects were correlated with the size of the sputtering ion used and attributed to the influence on lattice expansion.

More recently, ion-beam sputtered oxides have been found to exhibit optical properties which are superior to those of films of the same material deposited using e-beam evaporation. This is illustrated in Fig. 6[12] which shows the refractive indices of several film materials deposited using ion-beam sputtering as described above. The total losses (absorptance, scatter, and transmittance) from high reflectance mirrors constructed from these films is 100 parts per million or less, as determined by performance in a ringdown laser arrangement. The films are stable with temperature cycling to 300°C in atmosphere for several hours. The internal stress of ion-beam sputtered films is compressive, and it is generally greater than that of evaporated films of the same material In the case of some oxide materials, the compressive stress is sufficient to cause film

delamination from the substrate.[12] The amount of film stress changes with the location of the substrates relative to the sputter target. This suggests the dependence might be related to substrate bombardment during film deposition.

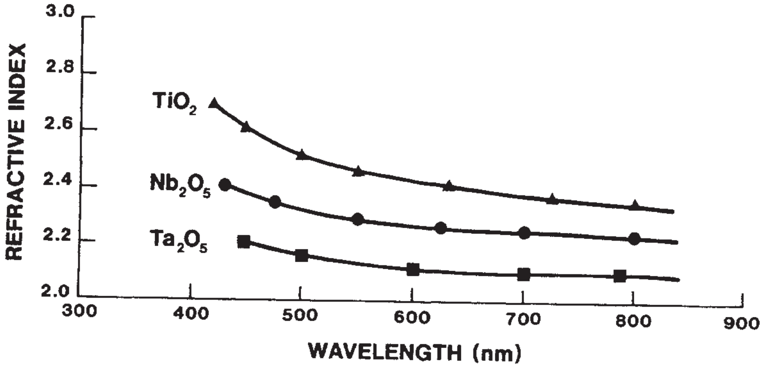



**Figure 6.** Values of refractive index obtained from examining thin film materials which were ion-beam sputtered.[12]

## 5.2 Ion Assisted Deposition

Ion-assisted deposition (IAD) employs an ion source to direct a beam of ions at the substrates during deposition. The source of film material could be an evaporation source or a sputter arrangement, such as the dual ion beam deposition arrangement mentioned in the previous section. An obvious advantage to utilizing IAD is that the process can be easily incorporated into an existing vacuum deposition system.

In this section, we describe the equipment used to deposit thin films using IAD, the advantages inherent in using IAD, and the limitations in applying IAD to deposit thin films. This technique has been employed in the fabrication of multilayer optical coatings, in the deposition of compound thin films at reduced substrate temperature, and to modify film properties during deposition. We review results of employing IAD and illustrate how control of the ion energy and flux can be utilized to tailor the properties of thin films.

**Equipment.** A schematic of a vacuum deposition system configured for IAD is shown in Fig. 7.[9] The operation of the source of thin film material is totally independent from the ion source. The Kaufman ion

source provides a monoenergetic, neutralized ion beam which is directed at the substrates being coated. This configuration has a number of advantages over conventional plasma configurations used to provide ion bombardment of the substrate. Three advantages provided by ion beams include the independence of the bombardment process from the deposition process, the inherent control provided by the ion beam, and the ability to accurately measure all critical deposition parameters. An additional feature concerning IAD is that substrate cleaning can be readily accomplished prior to deposition by controlling the appropriate gas species through the ion source.

As illustrated in Fig. 7, the gas is introduced through the ion source into the deposition chamber. IAD is inherently a low pressure process ($10^{-5}$ to $10^{-4}$ torr) that permits a great deal of flexibility in deposition configuration. Any number of gas species can be introduced, depending upon the complexity of the gas manifold. Neutral background gas can also be introduced into the vacuum chamber through another inlet if desired.

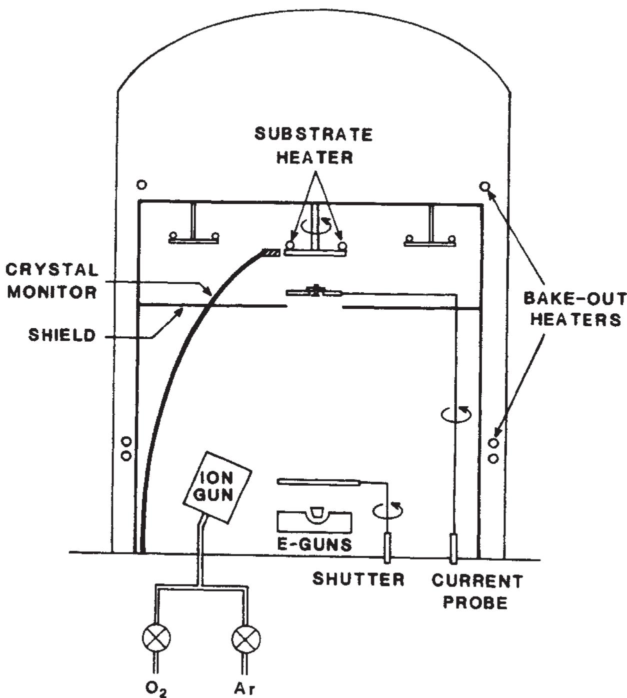



**Figure 7.** Schematic of an IAD deposition system.

As described in a previous section, it is essential that the ion beam is properly probed prior to deposition. For some materials, film properties are sensitive to bombarding ion flux levels; examples are given later in this section. As illustrated in Fig. 7, an ion current probe is located just below the substrate. The probe platform is mounted on an aluminum rod that is attached to a rotary vacuum feedthrough. The probe is rotated into position immediately below the substrates to be cleaned or coated. After the ion flux value is measured, the probe is rotated away from the substrate area to minimize coating of the probe. Not shown in Fig. 7 is a shield attached to the probe platform which protects the probe from film material during deposition. This shield prolongs the lifetime of the probe when depositing insulating film materials.

An important parameter in depositing thin films using IAD is the ratio of the ion-to-molecule arrival rates. Proper beam probing allows accurate determination of the ion flux. In the case where substrates are continuously exposed to the ion beam, modification of film properties occurs on a continual basis. One method of determining the flux of arriving thin film molecules is measurement of the film deposition rate using a crystal monitor. In the data presented below, film properties are plotted versus ion beam current density and for a constant deposition rate. Thus the ratio of ion-to-molecule arrival rates is a variable. As illustrated in Fig. 7, the monitor can be located very close to the substrates. The monitor must be calibrated to determine an accurate tooling factor for different film materials and for various ion source conditions.

If the substrate fixturing involves planetary rotation, the monitor cannot be located immediately adjacent to the substrates. In this arrangement, determining the proper flux of ions and film molecules is more difficult. Usually the substrates are exposed to the ion beam for only a fraction of time, $F$. The effect of the ion bombardment during the fraction of time $F$ may not be the same as if the substrate were bombarded continuously. This might be the case even if the average levels of ion flux are kept constant, for example, by increasing the ion current density by a factor of $1/F$. Therefore, when using IAD with a planetary rotation geometry, care must be exercised in selecting the ion beam parameters which result in the desired thin film properties. This is best achieved by first coating sample substrates with single layer films (if multiple layered structures are ultimately desired). For each film material, optimal ion beam current density and energy can be determined by examining samples deposited under different conditions.

Another important consideration when applying IAD is the respective arrival directions of the bombarding ions and the film molecules. As illustrated in Fig. 7, when employing a fixed-position substrate geometry with an ion source located off-axis, it is important that substrate rotation be employed. The rotation of the substrates is necessary to minimize anisotropic properties in the films due to the different arrival directions of the ions and the molecular species.

Proper selection of the discharge voltage is important. The value should be high enough to sustain an appropriate discharge in the source, but not too high a value, which will cause an increased production of doubly ionized ions. The doubly ionized species will accelerate to twice the beam energy, and this reduces the level of control the operator has over the ion beam parameters. In addition, high values of discharge voltage decrease the lifetime of the cathode filament in the source. For a 10 cm source, cathode filament lifetime for typical IAD conditions (500 eV, 30 $\mu A/cm^2$) operating in oxygen is approximately 4 hours for a 0.015 inch diameter tungsten wire. The lifetime for a 0.020 inch diameter tantalum wire is only 1 to 1.5 hours under similar conditions.

As mentioned in a previous section, it is necessary to provide an equal number of electrons to neutralize the ion beam, especially when bombarding an insulating target. This is often accomplished using a thermionic neutralizer filament which emits the appropriate electron current into the beam. The value of this neutralizer current is made approximately equal to that of the beam current. Note that the ions are not each neutralized, but rather the net charge flux to the target is zero. When using this simple arrangement for beam neutralization, consideration must be given to problems arising due to neutralizer filament sputtering. Another technique for beam neutralization is the use of a plasma bridge neutralizer arrangement (see a previous section).

**Procedures.** The thin film material can be preheated prior to coating and, as illustrated in Fig. 7, a shutter can be employed to shield the chamber from the vapor material. Immediately upon completion of the cleaning process, film deposition can commence. The time between the two processes is limited to the delay, if any, associated with changing the gas species flowing through the ion source.

It is critical that the ion flux is stable and accurately measured before deposition begins. The gas discharge of the ion source should be established and the desired beam parameters (ion energy, flux, and neutralizer

current) set at the ion source power supply. When the ion flux is measured by the probe, an accurate record of its value and all ion source parameters should be made. When the probe is rotated out of position, deposition can commence. During deposition, the beam energy and current must be monitored on the power supply to ensure stable ion source operation. At the completion of deposition, the ion flux should be checked by rotating the probe back to the original measurement position.

**Examples of Applications of IAD to Optical Coatings.** Early work utilizing a separate ion source to bombard evaporated SiO with 5 keV oxygen ions during deposition was examined by Dudonis and Prannevicius.[14] They investigated the effects of ion flux on film stoichiometry and found that for increasing flux values, the O/Si ratio approached two. They also simultaneously bombarded with oxygen ions during the evaporation of aluminum and measured changes in film resistivity as function of ion flux; resistivity changes for $10^{17}$ were obtained using the ion bombardment. Changes in resistivity are an extremely sensitive measure of film stoichiometry. Cuomo, et al.,[15] obtained superconducting NbN films by bombarding evaporated Nb with $N_2^+$ during deposition. They also reported a change in stress from tensile to compressive for evaporated Nb films bombarded with 100 to 800 eV $Ar^+$ during deposition. Hoffman and Gaerttner[16] bombarded evaporated Cr films during deposition with 11.5 keV $Ar^+$. They reported changes in stress from tensile to compressive and attributed the results to modifications in film microstructure. In these studies, an important parameter affecting film properties was the ion-to-atom arrival rate ratio. This ratio can be used to normalize results from various experiments and is discussed in more detail later in this section.

Recently, IAD has been applied in the production of optical coatings. Netterfield and Martin have studied the effects on the properties of $ZrO_2$ and $CeO_2$ films bombarded with $O_2^+$ and $Ar^+$ during deposition.[17]–[19] They reported increased packing densities, reduced permeability to water and changes in film crystal structure. Bombardment with $Ar^+$ produced changes in film stoichiometry. Allen applied IAD to obtain increased values of refractive index in $TiO_2$ films.[20] The increase was larger at 300 eV bombardment than at 500 eV. McNeil, et al.,[21][22] examined the effects of 30 and 500 eV oxygen ion bombardment on the properties of $TiO_2$ and $SiO_2$ films deposited using TiO and SiO starting materials. They reported improvements in film properties were obtained with 30 eV bombardment in the

case of ambient substrate temperatures. In particular, they obtained films with improved stoichiometry. Al-Jumaily, McNally and McNeil[23]–[25] examined the effects of ion energy and flux on optical scatter and crystalline phase in Cu, $TiO_2$, and $SiO_2$ films. They reported reduction in optical scatter and crystal phase transitions for bombarded films. The modifications in Cu films were obtained with 500 eV $Ar^+$ bombardment. McNally, et al.,[26][27] reported on the effects of oxygen ion bombardment on the properties of $Ta_2O_5$, $Al_2O_3$, $TiO_2$, and $SiO_2$ films. Increases in the values of refractive index were reported for 200, 300, 500, and 1,000 eV bombardment. The increase was found to be directly dependent on the ion flux, which is consistent with the comments in a previous section regarding the importance of proper beam probing. Changes in film stoichiometry and crystal phase were also reported.

As a final example of recent IAD work, the deposition of protective coatings on sensitive substrates at low temperatures has been demonstrated.[28] Films of $MgF_2$ were successfully deposited on heavy metal fluoride glass substrates at 100°C temperature. The films were bombarded with 300 eV $Ar^+$ during deposition. Conventionally evaporated $MgF_2$ films are soft when deposited at this substrate temperature, while the IAD $MgF_2$ films were hard and robust. This represents a significant advantage in using IAD to deposit films.

**IAD Results.** Some sample results from applying IAD to produce coatings are given in this section. McNally, et al.,[9] produced $Ta_2O_5$ coatings which were electron-beam evaporated at a rate of 0.30 nm sec$^{-1}$ with oxygen backfill pressure of $1.0 \times 10^{-4}$ torr. The coatings were deposited onto heated substrates (275°C), and were bombarded with oxygen ions during deposition. The transmittance spectra for two $Ta_2O_5$ coatings are given in Fig. 8. The curve labeled $J = 0$ corresponds to a coating deposited with no ion bombardment; the curve labeled $J = 5$ is for a coating bombardment during deposition with 500 eV $O_2^+$ current density of 5 μA cm$^{-2}$. The curve for the ion assisted coating contains larger differences in transmittance extrema than the curve for the conventional e-beam evaporated coating. These larger differences indicate a larger value of refractive index *(n)* for the ion assisted coating. Good film stoichiometry was obtained for the ion bombardment conditions employed, as indicated by an absence of measurable absorption at wavelengths for which the film is multiple half-wave in optical thickness down to 340 nm. Examination of the reflectance spectra for these coatings indicated an absence of any refractive index inhomogeneity.

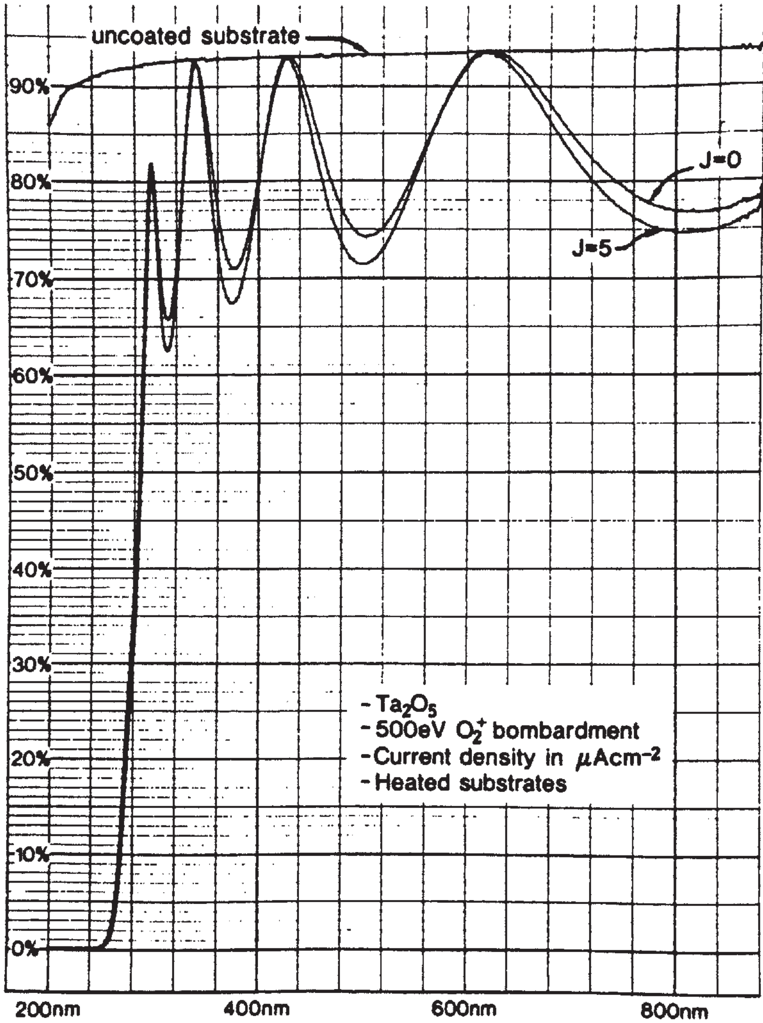



**Figure 8.** Transmittance spectra of two $Ta_2O_5$ coatings, one deposited without ion bombardment ($J = 0$) and the other deposited with ion bombardment ($J = 5$ μA/cm$^2$).

The values of $n$ (at $\lambda = 400$ nm) for $Ta_2O_5$ coatings bombarded with 200, 300 and 500 eV oxygen ions are plotted in Fig. 9 as a function of $O_2^+$ current density. The error bars indicate the uncertainty in the index measurements. The values increase from 2.16 for the coating deposited without bombardment to maximum values of 2.25. 2.28 and 2.19 for films bombarded with 500, 300 and 200 eV $O_2^+$, respectively.

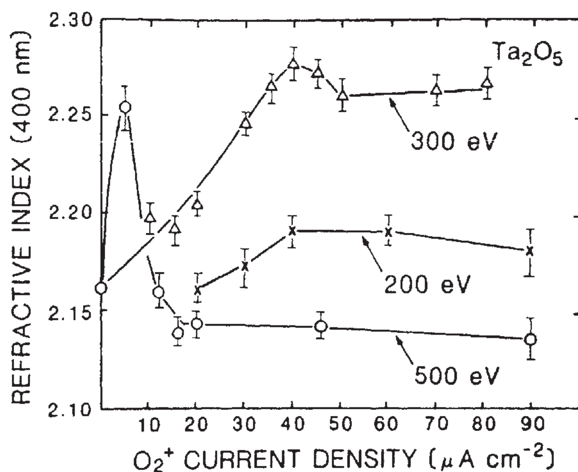



**Figure 9.** Values of refractive index for $Ta_2O_5$ coatings deposited under different levels of $O_2^+$ current density and energy.

The increase in the values of $n$ with increasing $O_2^+$ current density indicates that ion bombardment during deposition modifies the growth of film columnar microstructure resulting in film densification. The results indicate that the coatings bombarded with 300 eV $O_2^+$ had larger values of $n$ than those bombarded with 500 eV $O_2^+$. The results in Fig. 9 indicate that only minor densification occurred for coatings bombarded with 200 eV oxygen ions during deposition. A similar dependence of refractive index on bombarding ion energy has been reported for ion assisted $CeO_2$ films.[19]

The current density value (for a fixed ion energy) at which the maximum $n$ occurs is termed the *critical value.* The results in Fig. 9 illustrate that film index values decrease for ion current densities greater than the critical values. The decrease in index may be explained as a result

of degradation in film stoichiometry, creation of closed isolated voids, or oxygen incorporation into the films. The decrease was largest for bombardment with 500 eV ions and least for 200 eV ions in the case of $Ta_2O_5$. This energy dependent decrease is consistent with the dependence on ion energy of the average ion penetration depth and preferential sputtering yield. Similar results for which the values of refractive index decrease for current densities greater than the critical values have been reported for ion assisted $ZrO_2$ films[18] and $CeO_2$ films.[19]

The coatings bombarded during deposition at oxygen ion current densities up to approximately the critical values exhibit good optical characteristics. For higher levels of bombardment, the optical absorption of the coatings increase. In Fig. 10, values of extinction coefficient *(k)* for $Ta_2O_5$ coatings (300 nm thick) bombarded with 500, 300, and 200 eV oxygen ions are plotted as a function of $O_2^+$ current density. The values of $k$ were calculated at $\lambda = 400$ nm. The error bars indicate the uncertainty in the measurements. The dashed line across the bottom at $k = 2.0 \times 10^{-4}$ indicates the level below which the values of $k$ were too small to be regarded as reliable due to the minimum sensitivity of the measurement technique.

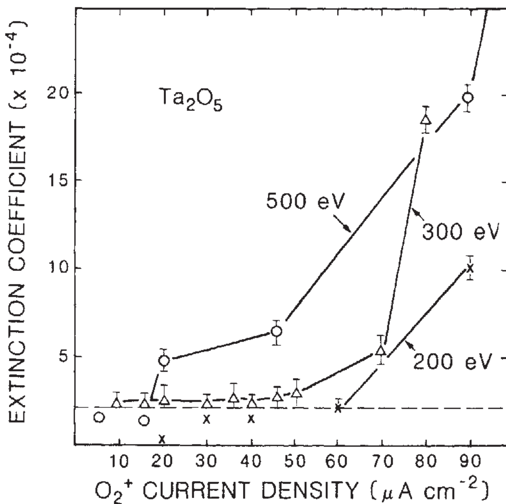



**Figure 10.** Values of extinction coefficient of the same $Ta_2O_5$ coatings represented by Fig. 9.

As illustrated in Fig. 10, film optical absorption increased with higher levels of oxygen bombardment. The most probable mechanism for this is the preferential sputtering of oxygen in the $Ta_2O_5$ molecule. Preferential sputtering would result in oxygen-deficient layers continuously integrated into the coatings as deposition occurs. Values of $k$ for coatings bombarded at a fixed current density were the lowest for 200 eV $O_2^+$, higher for 300 eV, and highest for 500 eV $O_2^+$. This result is consistent with increasing preferential sputtering yields for higher energy ions. This damage mechanism has been observed in other IAD films.[18] This highlights the requirement for proper beam probing to avoid compositional change by preferential sputtering.

The environmental stability of optical coatings is in large part limited by the porosity of the film microstructure. Figures 11 and 12 are the transmittance curves for two $Ta_2O_5$ coatings exposed to humidity testing. The spectra in Fig. 11 are for a coating deposited onto a heated silica substrate with no ion bombardment ($J = O$). The spectra in Fig. 12 are for a coating bombarded during deposition with 300 eV $O_2^+$ at a current density of 20 μA $cm^{-2}$. The curve labeled "AIR" is the spectrum measured after the coating has been removed from the vacuum chamber and exposed to the ambient atmosphere. The curve labeled "POST HUMIDITY" is the spectrum for the same coating remeasured after exposure to 97% relative humidity at 35°C for 6 hours.

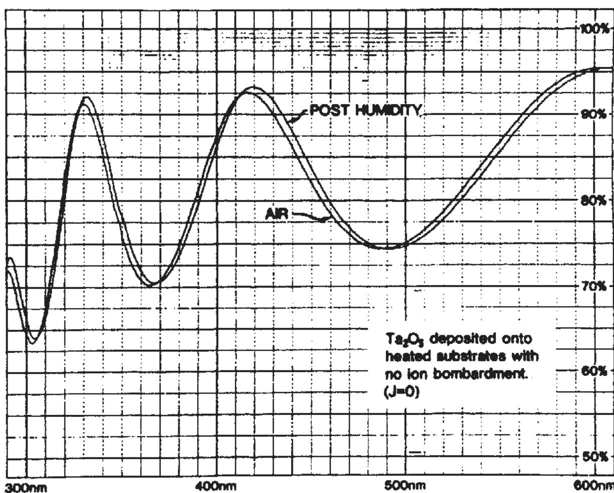



**Figure 11.** Transmittance spectra of a $Ta_2O_5$ coating deposited without ion bombardment subjected to humidity test.

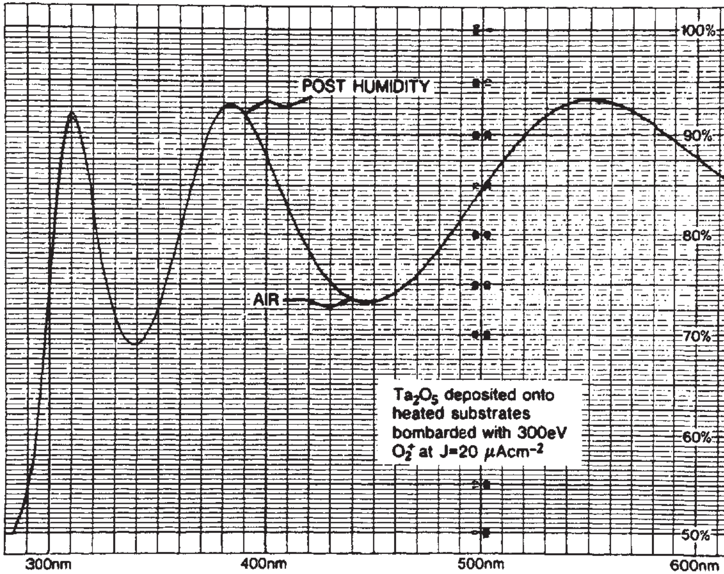



**Figure 12.** Transmittance spectra of a $Ta_2O_5$ coating bombarded during deposition with 300 eV $O_2^+$ at $J = 20$ mA cm$^{-2}$ subjected to humidity test.

The curves in Fig. 11 illustrate a spectral shift of 1% to longer wavelengths for the coating deposited without bombardment. The shift is most likely due to water adsorption into the microvoids in the film microstructure. This increases the effective index value of the coating and, in turn, increases the optical thickness (*nt*). Figure 12 is typical of the results obtained for IAD coatings. No spectral shifts within the measurement precision of the spectrophotometer are observed. Similar results have been reported for IAD $ZrO_2$ and $TiO_2$ coatings.[17][18]

IAD can affect intrinsic stress in films. Changes in stress for $Ta_2O_5$ coatings have been reported.[9] The stress was measured interferometrically. The stress was computed from measured substrate bending, and because film thickness was much less (factor of 1000) than the substrate thickness, the elastic constants of the coating were not required.

Figure 13 illustrates the values of film stress plotted versus oxygen ion current density. The triangles and circles represent stress values for coatings bombarded during deposition with 300 and 500 eV $O_2^+$, respectively. The results indicate film stress was compressive and increased for increasing levels of ion bombardment.

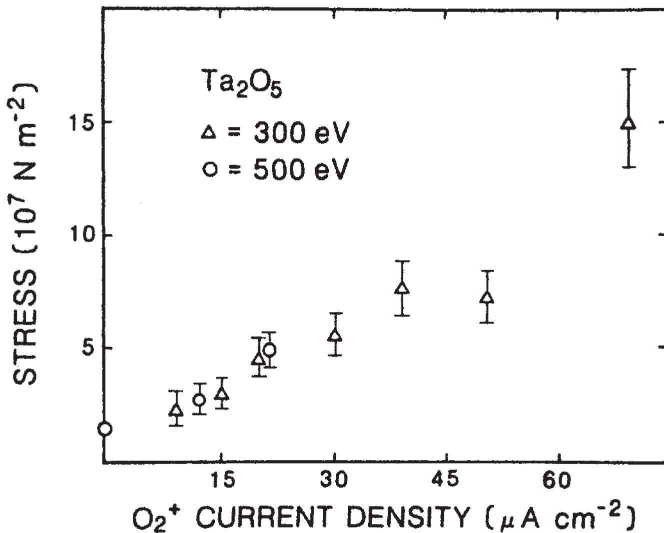



**Figure 13.** Values of stress of $Ta_2O_5$ coatings for films deposited with different levels of $O_2^+$ current density and energy.

There have been a number of studies in which the effects of ion bombardment on stress in metal films were examined. Cuomo, et al.,[15] reported a change in stress from tensile to compressive for evaporated Nb films bombarded with 100 to 800 eV $Ar^+$ during deposition. They attributed the changes in stress to modifications in film microstructure and incorporation of argon. Hirsh and Varga[29] measured stress relief in evaporated Ge films bombarded with 100 to 300 eV $Ar^+$ during deposition. The stress changed toward compressive values. Hoffman and Gaerttner[16] bombarded evaporated Cr films during deposition with 11.5 keV $Ar^+$ They reported changes in stress from tensile to compressive and attributed the results to modification in film microstructure. Thus, the results illustrated in Fig. 13 are consistent with the trend toward increasing compressive stress for increasing ion bombardment.

IAD has also been used to produce $Al_2O_3$ optical coatings.[9] The $Al_2O_3$ coatings were electron-beam evaporated at a rate of 0.40 nm sec$^{-1}$ with oxygen backfill pressure of $1.0 \times 10^{-4}$ torr. The coatings were deposited onto heated substrates (275°C), and were bombarded with oxygen ions during deposition.

The values of $n$ (at $\lambda = 350$ nm) for $Al_2O_3$ coatings bombarded with 300, 500, and 1,000 eV oxygen ions are plotted in Fig. 14 as a function of $O_2^+$ current density. The values increase from 1.64 for coatings deposited without bombardment to maximum values of 1.70, 1.68, and 1.68 for films bombarded with 100, 500, and 300 eV $O_2^+$, respectively.

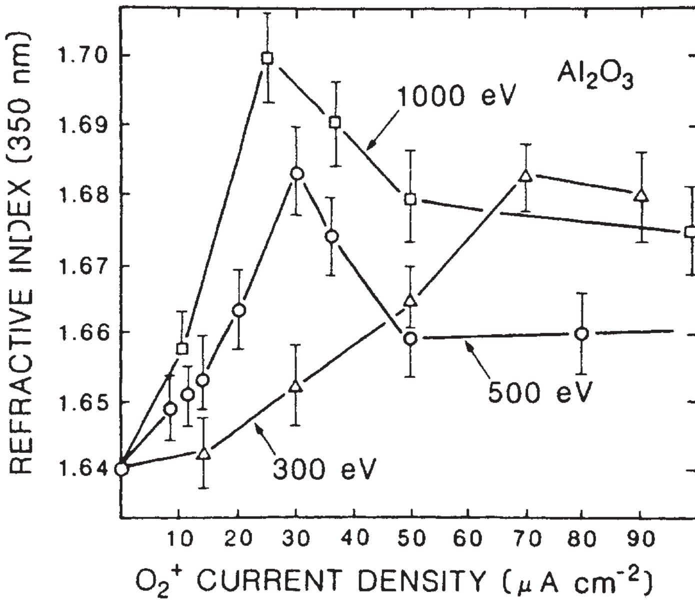



**Figure 14.** Values of refractive index of $Al_2O_3$ coatings deposited under different levels of $O_2^+$ current density and energy.

The increase in the values of $n$ for increasing levels of $O_2^+$ current density is similar to $Ta_2O_5$ results (Fig. 9) and indicates that ion bombardment during deposition results in film densification. The results indicate that the $Al_2O_3$ coatings bombarded with 1,000 eV $O_2^+$ had larger values of $n$ than those bombarded with 500 and 300 eV $O_2^+$. These results illustrate that the effects of ion bombardment on the values of $n$ are material dependent. The ion energy at which the largest value of $n$ occurred for $Ta_2O_5$ was 300 eV, yet for $Al_2O_3$ it was 1,000 eV.

The results in Fig. 14 illustrate that values of *n* decreased for ion current densities larger than the critical values. The decrease was largest for bombardment with 1,000 eV ions and least for 300 eV ions. This energy dependent decrease is consistent with the results for IAD $Ta_2O_5$ coatings (Fig. 9).

Attempts to measure the values of extinction coefficient for the $Al_2O_3$ coatings (400 nm thick) were limited due to the minimum sensitivity of the measurement equipment. All computed values of $k$ were less than $2.0 \times 10^{-4}$. The low values of $k$ calculated for all the $Al_2O_3$ coatings indicate that, for the conditions examined, preferential oxygen sputtering is not a dominant mechanism for $Al_2O_3$ as was the case for $Ta_2O_5$ (Fig. 10). This result again illustrates that the effects of ion bombardment on film properties are material dependent.

## 5.3 Application Summary

The two configurations for using ion beams for thin film deposition (Figs. 5, 7) each contain their distinct advantages and disadvantages. Direct comparison of the two configurations to determine which provides the "best" coatings is difficult. The decision as to which configuration to employ must be made with consideration of the end application, the existing deposition system (if any), total costs, and the issues discussed in previous sections. In this section, a discussion summarizing the advantages and disadvantages of IBS and IAD is given with the emphasis on listing information to aid the users in deciding which configuration would better serve their needs.

The improvements in the properties of thin films produced using IBS are detailed in a previous section. Similar improvements in the properties of IAD films are given in a previous section. It appears that each technique results in thin films of similar quality. Thus, a decision based on film quality would need to be made on a case-by-case basis.

A direct advantage of IAD is that the technique is readily implemented with the addition of an ion source apparatus to an existing vacuum deposition system. This offers significant savings in both time and money. On the other hand, IBS may require more modifications to an existing deposition system, or the purchase of a totally dedicated one. Either choice requires a major investment. Another advantage of IAD is the ease in which the technique can be scaled to large geometries. Scaling the IBS process is more limited than the IAD process by the size of ion sources

available. A number of trade-offs among the deposition parameters (deposition rate, uniformity, etc.) exist, and they must be considered before choosing which technique would best achieve the desired results.

## 6.0 CONCLUDING COMMENTS

In this chapter, a general description and two specific applications of ion beams for thin film coating have been described. A common advantage of ion beam techniques is the degree of flexibility and control provided compared to other techniques that incorporate a gas discharge. Ion beam sources will continue to be incorporated into deposition arrangements and applied to other materials to provide films with improved properties.

## ACKNOWLEDGMENTS

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# 12

# Chemical Mechanical Polishing

*Kenneth C. Cadien*

## 1.0 INTRODUCTION

Polishing of materials has been known to many disciplines for many decades. For example, in astronomy, glass mirrors and lenses have been polished since at least the seventeenth century. In metallurgy, metal samples are routinely polished prior to metallographic examination. In the semiconductor field, lapping and polishing have been used for the preparation of single crystal substrates (wafers) during the last 40 years. The lapping process is used after sawing and prior to polishing. Lapping is performed on both sides of the wafer to insure flatness and parallelism. Polishing is used to remove surface damage and haze. All polishing processes described above refer to the surface finishing of bulk materials. During the past decade, a new application of polishing has occurred in integrated circuit manufacturing. This application involves the removal of thin metal, insulator, and semiconductor films. This new field is referred to as chemical mechanical polishing (CMP).

The primary driving force for CMP was the realization during the 1980s that shrinking feature size and the increased number of devices on a chip required additional layers of metallization (separated by *interlayer dielectrics*, ILD). Since the metal layers were etched into metal lines, and

the ILD layers were deposited by conformal CVD processes, additional metal layers meant that there would be a dramatic increase in topography within the die. This effect is illustrated in Fig. 1. This increase in topography was in direct opposition to trends in lithography where the printing of ever-smaller feature sizes meant that less topography was required, not more. The reason for this was that small features require improved resolution. Increasing resolution meant reduction in depth of focus. This trend is summarized in Fig. 2. The need for both additional metal layers and increased resolution lead to the development of many planarization strategies. The two predominant ones were *spin-on glass* (SOG) with or without etchback, and CMP. Following the development of CMP for planarization, it has also been used for tungsten polish and shallow trench polish, to name a few applications. This chapter will focus on these applications of CMP as well as a brief survey of polishing tools that are available; special tool features: endpoint, pad conditioning, retaining rings, and consumables.

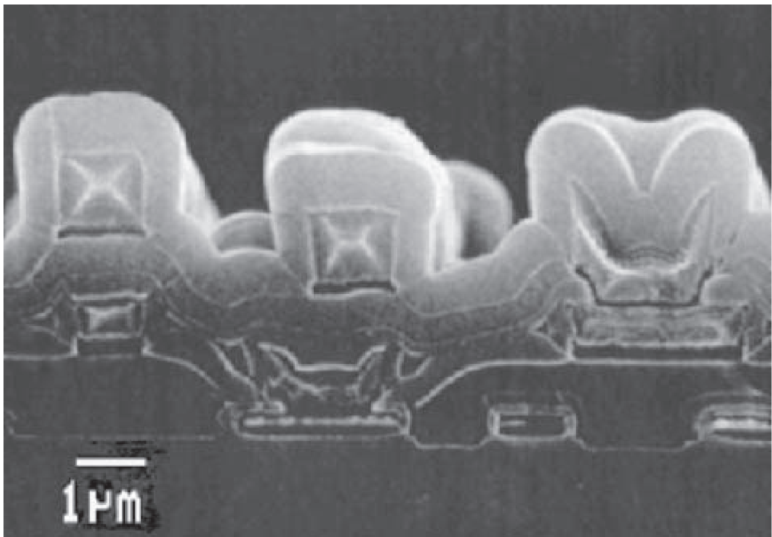



**Figure 1.** Photograph showing topography due to two metal layers.

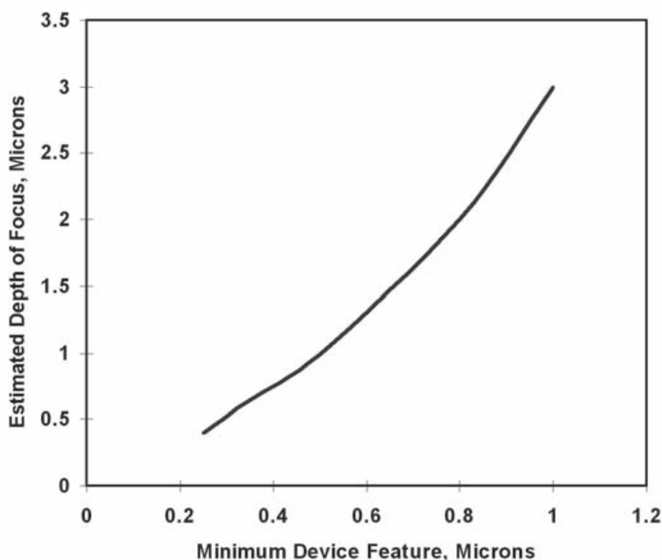



**Figure 2.** The effect of shrinking minimum device feature size on depth of focus.

## 2.0 PROCESSING

During CMP the wafer environment consists of the slurry and polishing pad, and the backing material behind the wafer. The wafer is pressed against the polishing pad with a known pressure. Typical polishing variables are polishing pressure, pad rotation rate, wafer rotation rate, slurry type and flow rate, backing pad and curvature, and polishing pad material. A schematic of the polishing process is shown in Fig. 3.

The polishing pad is mounted on a rigid base plate that is rotated about its center axis. Slurry is pumped onto the pad near the center and centripetal force spreads the slurry over the pads surface. The wafer is placed face down on the pad with a given pressure. The wafer is also rotated about its own axis. The wafer can also move in a radial motion on the pad in order to widen the track of the wafer over the pad and thereby improve the life of the pad.

In this section we discuss three different CMP processes: global planarization, shallow trench isolation polish, and tungsten polish.

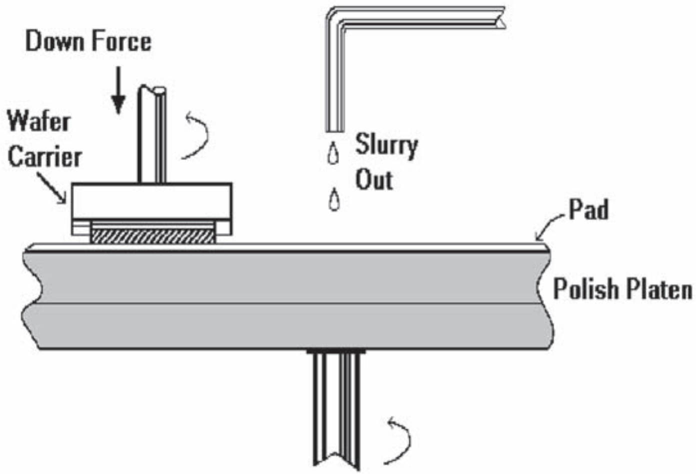



**Figure 3.** Schematic diagram of a polishing apparatus.

## 2.1 Oxide Polish

As mentioned earlier, during IC fabrication thick ILD layers are deposited over metal topography. The ILD layer must be thick enough so that during CMP enough oxide can be removed so that the topography can be eliminated, and enough oxide left behind to adequately isolate metal layers from each other. The planarization process sequence is summarized schematically in Fig. 4.

During polishing, elevated surfaces of the substrate are polished more rapidly than the lower regions, leading to a flattening of the surface. In addition there are pattern density effects during polishing. Large areas polish more slowly than small areas. Polish processes are optimized to minimize pattern density effects as well as polish rate and uniformity. Process conditions that are typically used are summarized below in Table 1.

In oxide polish, the slurries that are used typically consist of a fumed silica abrasive suspended in an ammonia or potassium hydroxide environment that is buffered to prevent pH drift. At high pH's, $SiO_2$ is softened and easier to remove.

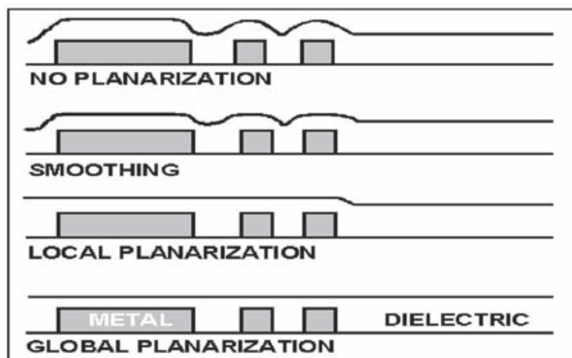



**Figure 4.** Schematic diagram of the global planarization process.

**Table 1.** Typical Process Conditions for Global Planarization

| PROCESS PARAMETER | RANGE OF VALUES |
|---|---|
| Polish pressure, psi | 7–9 |
| Relative velocity (pad-wafer), ft/min | 125–300 |
| Slurry and flow rate, sccm | Silica abrasive, pH = 10–11, 100–200 |
| Polishing pad | Hard pad on soft pad |
| Backing pad | Soft |

The biggest challenge for global planarization using CMP is the fact that in this process there is no endpoint. The process is complete when the surface is planarized and a specified thickness of oxide is remaining. This means that either an in situ oxide measurement tool is required, or the oxide CMP process must be very stable. Another strategy that is used is to target the process so that out-of-control (OOC) events leave the ILD too thick so that rework is possible. Then a post polish thickness measurement must be made of the polished wafers on the polishers (or an external tool) to verify that the ILD thickness is within specification. Commercial equipment is now available that is capable of making within-die thickness measurements

under water and communicating with the polisher so that OOC wafers can be sent back to the tool for rework.

## 2.2 STI Polish

Shallow trench isolation is a process that uses trenches in the silicon substrate filled with undoped polysilicon or silicon dioxide to isolate active regions. STI replaces the LOCOS process. During STI polish, the fill material is polished off to leave trenches filled with the fill material. Silicon nitride is often used on the planar silicon surfaces to act as a polish stop. While STI polish uses conditions similar to the oxide polish described above, the process is fundamentally different. Oxide polish is designed to stop in the middle of the oxide layer, while STI polish clears the fill off the stopping layer.

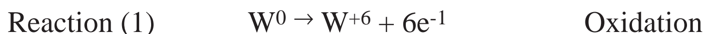
The thickness of the stopping layer, within die, within wafer, and wafer-to-wafer, is often used as the measure of success of this process. The process is very sensitive to pattern density variations within the die. Areas of the die with a high density of trenches tend to polish faster and the stopping layer is thinner than low density regions. Techniques such as *dummification* have been used to even out pattern fluctuations.

It is interesting to note that the pattern sensitivity noted for STI polish is also found at tungsten polish. A simple mechanical model proposed by Rutten, et al.,[1] explains both phenomena.

## 2.3 Tungsten Polish

Tungsten studs are used to connect different metal layers, or metal 1 to the diffusion layer. Vias or contacts are etched in the ILD, an adhesion layer is sputter deposited, and W is then deposited by CVD. The W/adhesion layer is then removed by a blanket polish process leaving behind tungsten studs.

Unlike global planarization, during W polish there is a clear stopping layer, the ILD. Several authors have reported endpoint systems and processes for W polish related to the different friction between W, the adhesion layer, and ILD. There is relatively good understanding of the phenomena that occur during W polish which is based on the seminal work published by Kaufman, et al., during 1991.[2] The role of the slurry during W polish is to have a redox potential such that in the presence of the chemistry, W is oxidized while the slurry chemistry is reduced. The reactions are summarized below using iron (Fe) as an example.



Reaction (1) $W^0 \rightarrow W^{+6} + 6e^{-1}$ Oxidation

Reaction (2) $Fe^{+3} + e^{-1} \rightarrow Fe^{+2}$ Reduction

In reaction (1), W is oxidized and forms a stable oxide film which is removed by the abrasive during the polish process. Areas of the wafer that are not in contact with the polish pad are protected from the chemistry by the oxide film.

The conditions under which these reactions are thermodynamically favorable are shown in Pourbaix diagrams.[3] These diagrams are calculated from thermodynamic data. Since there is usually only complete data for metal/water systems, Pourbaix diagrams typically do not exist for complex nonaqueous systems. The Pourbaix diagram for W in water at 25°C indicates that pH and electrochemical potential determine the condition under which the passive W oxide layer forms. For the W water system, the optimum pH range is below 4.

## 3.0 POLISH EQUIPMENT

There are three basic steps to CMP:

*i)* down force is applied to the wafer pressing it against the polishing pad

*ii)* slurry is pumped onto the pad

*iii)* the wafer and pad are rotated

This simplified view of CMP is shown schematically in Fig. 3. Polishing does not occur unless pressure forces the wafer against the polishing pad, and there is relative motion between the wafer and the polish pad. The uniformity of the pressure of the wafer against the pad is critical to obtaining polish rate uniformity. In fact, controlled polish non-uniformity can be used to correct systematic non-uniformity due to the pad/wafer interaction. Examples of this are curved carriers and back pressure. During polishing, both the pad and the wafer are rotated in the same or opposite directions. This applies large shear stresses to the wafers that tend to cause the wafer to slip out of the wafer carrier. A retaining ring made out of a wear-resistant material is used to hold the wafer in place. Traditionally, the ring was fixed to the carrier. Pumping of slurries is difficult. Slurries tend to be corrosive and contain very fine particles that destroy moving parts such as bearings. It has been found that the optimal method of pumping slurry is to

use a system that completely isolates the slurry from moving parts of the pump. Pumps such as peristaltic and dual diaphragm pumps work well. Polishers tend to have multiple pumps per pad which allows for two or more components to be pumped on to the pad for in situ mixing. This is especially useful when premixed slurry components are unstable, have short shelf life, or have some other difficulty. Since peristaltic pumps are positive displacement pumps they have difficulty pumping compressible fluids. Liquids are not compressible. However, liquids that entrap lots of gas such as foams or froth are compressible and cannot be pumped with peristaltic pumps. Most polishers deliver slurry onto the top surface of the pad where centripetal force spreads the slurry over the pad surface. There are new tools on the market today that deliver slurry through the pad right to the wafer surface. This leads to very effective consumption of the slurry. It may also have some positive impact on polish uniformity. Slurry is normally delivered to semiconductor fabs in 55 gallon drums or totes that have volumes in excess of 300 gallons. The fab slurry delivery system mixes the totes, dilutes the slurry and/or makes additions to the slurry, then distributes the slurry to the polishers. A detailed discussion of slurry delivery systems is beyond the scope of this chapter.

## 4.0 HISTORY

Although polishing has been done on blanket silicon wafers for many years, the first fabrication (fab) compatible polisher did not appear until the late 1980s. The key characteristic that made this polisher fab compatible was robotic cassette-to-cassette capability (C-to-C). The first production tool was delivered in 1989. It had a single polish platen and a single polishing head. Wafers were held in the head by a fixed retaining ring. The tool had inherent problems related to the large size of the machine and the relatively low throughput rate for long polish steps. As the number of polish steps have increased in submicron IC processes, the large number of polishers required for manufacturing has become a major issue. Other competitive machines began to arrive on the market in 1990. The first of these consisted of two polish heads on a single large polish platen. The system had inherently higher throughput but also had a larger foot print.

Today, most polishers are distinguishable by the number of polishing heads and the number of primary polish platens that each tool has. These features are summarized in Table 2 for several tools that are available

today. The number of polish heads tells us the number of wafers that can be in process simultaneously. It is also an indication of increasing throughput. Machines in the middle rows represent compromises between high throughput, size, and complexity.

**Table 2.** Examples of Polish Tools Available Today Based on Number of Polish Heads

| Number of polish heads | Number of polish platens | Tool |
|---|---|---|
| 1 | 1 | A |
| 2 | 1 | B |
| 3 | 3 | C |
| 4 | 4 | D |
| 5 | 1 | E |
| 6 | 1 | F |

## 5.0 INNOVATIONS

One innovation that these early tool vendors brought to CMP market was the use of pad conditioners. It had been discovered that during polishing the rate decreases due to pad glazing. Mechanically abrading the surface of the pad, either during polishing or between polishes, reduces the rate at which the polishing rate drops. There are several novel designs for pad conditioners exemplified by the design disclosed by Intel.[4]

There are several innovations on the current generation of tools. For example, a method has been invented[5] for applying differential pressure to the retaining ring to improve uniformity. Systems have been developed that deliver slurry through the pad instead of on top of the pad, and move the wafer in an orbital motion.[6] There are also polish systems where the polish table is not rigid, and an equal air pressure needs to be applied behind the pad and the wafer.[6] In addition, in situ endpoint systems have been developed that directly measure optical film thickness during polishing. Motor current techniques that measure friction at the wafer surface have also been used to endpoint polish.

## 6.0 AUTOMATION

There are different approaches to automation with respect to wafer motion within the tool. The major approaches are to use a load cup with single and multiple heads, and pick-and-place. In the load cup example, a robotic system delivers wafers from the load cassette to the load cup. The polish head either swings over the load cup or indexes in a rotary motion over the load cup. This approach means that the polishing head, in addition to having up and down motion, must also be able to move in the XY plane. With pick-and-place systems, a robot picks the wafer from a cassette and places it directly in the polishing head. The polishing head only has to have vertical motion.

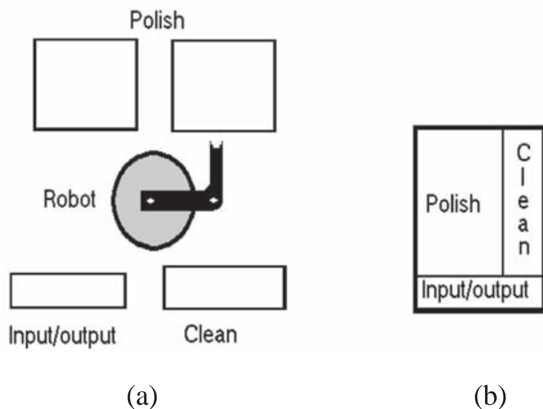
## 7.0 WAFER/PAD RELATIVE MOTION

In the simplified view of CMP that was shown earlier in Fig. 3, the wafer was rotated with respect to a large polish pad that was also rotated producing relative motion. Other methods of relative motion have been developed. In one instance, the wafer is subjected to an off-axis rotation of about 1 inch in diameter to produce a buffing type of motion. The pad is kept very small (2–4 inches larger than the wafer size). Slurry has to be delivered through the pad in order to reach the wafer surface.[7] In another case, a polishing pad is moved linearly in front of a rotating wafer.[8] This has a similar motion to a belt sander.

## 8.0 FUTURE CHALLENGES

There are several major challenges for the future generation of tools that will be emerging within the next year. These include automation, 300 mm wafers, and in-situ metrology. On the automation front, fully integrated dry-in/dry-out polishing systems that improve throughput and reduce footprints are being developed. Figure 5 shows schematically linked and integrated systems. In linked systems, discrete polishers, cleaners, and an input/output interface are linked by an external robot. The external robot moves cassettes of wafers between tools. While this system is large, it does reduce the number of people required to run the polish area, and eliminates possible ergonomic issues with polish and clean tools. In the

integrated system, a supplier delivers a total solution to their customers. Within the tool, either cassettes or single wafers are moved between the polish and clean modules.




(a) (b)

**Figure 5.** Schematic figure of linked (*a*) and integrated (*b*) polishing systems.

The transition from 150 to 200 mm wafers was fairly transparent to CMP tool suppliers, since existing tools could easily accommodate the larger wafer size. With 300 mm wafers, most machines will need to increase the frame of the polisher. Of particular concern will be wafer handling. Three-hundred (300) mm wafers are about four times heavier than 200 mm wafers.

One of the factors that impacts CMP throughput and floor space is the need for metrology tools. The drive in future tools is to incorporate in-situ metrology for device wafers into integrated tools with closed loop control. This will also limit process excursions to the wafers in process.

## CONCLUSION

CMP was developed to address a major roadblock to future IC manufacturing. It is now finding widespread acceptance. CMP tools are undergoing a rapid evolution from fairly simple machines, to very complex high throughput tools with enhanced capability. These capabilities include in situ clean and metrology capabilities.

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# 13

# Organic Dielectrics in Multilevel Metallization of Integrated Circuits

*Krishna Seshan, Dominic J. Schepis, and Laura B. Rothman*

## 1.0 GENERAL INTRODUCTION

We turn our attention now to the interlevel dielectrics used in multilevel metal interconnections, and in particular, organic dielectrics which have recently become the subject of much work due to their unique properties. Advances in integration and scaling have opened new opportunities for these materials. Let us examine this further.

Future scaling of silicon integrated circuits to submicron dimensions has three consequences. First, the major component of propagation delay will transfer from the device to the interconnection wires. Second, the increased circuit integration, together with scaling, will require more interconnections, and finally, the wires will have to carry higher current densities. Therefore multilevel interconnection technology will have to consider the use of new conductors, insulators, and planarized three dimensional structures to satisfy the demands of scaling and integration.[1]

One method of reducing the propagation delay is to use organic dielectrics with lower dielectric constants. Going hand in hand with this is the switch to lower resistivity materials, mainly copper-based alloys. This chapter concentrates on the properties and the processing of organic dielectric materials. In this introduction, we examine some of the reasons for the use of the "conventional" AlCu wiring with $SiO_2$ as the dielectric and the requirements that any new wiring scheme will have to meet.

Multilevel metal/dielectric interconnection technology (dimensional ground rules and electrical properties) strongly impacts chip size and performance, and plays an important part in chip cost, yield, and reliability. Therefore, several considerations are involved in changing from one wiring/dielectric scheme to another. Historically, the AlSi or AlCu metal conductor in a $SiO_2$ or glass interlevel dielectric evolved first and is the industry standard. This scheme generally uses AlCu sputtering for deposition and reactive ion etching (RIE) to etch the metal. The dielectric, oxide or glass, is deposited by one of several well known techniques including sputtering, plasma enhanced chemical vapor deposition (PECVD), or spin-on glass (SOG). Via holes are then etched in the dielectric by RIE, followed by deposition of the next layer of metal. This so called "conventional etch technique," where the conductor is deposited over oxide with open vias, patterned and etched, has dominated present interconnection technology. This scheme, however, has its performance limitations[1] and becomes difficult when used in VLSI/ULSI systems as will become evident with further reading.

The choice of AlCu metallurgy evolved primarily because Al is easy to deposit and etch, compared with Cu, Ag, or Au, which are other choices for low resistance conductors. It was found that Al, when carrying high current densities, is prone to electromigration. The most common metallurgy in the industry is Alx%Cu (where x is between 1 and 4%), a composition reached after extensive research, notably at Motorola by Jim Black and coworkers. It is believed that the Cu segregates to the Al grain boundaries and prevents electromigration.[2][3] Difficulties in changing to Cu-based metallurgy include the fact that Cu is not easily etched by RIE and is easily oxidized by residual moisture.

The choice of $SiO_2$ is also historical. The dielectric must be robust, free of pinholes, and one which can be patterned and etched with wet solutions or by plasma. It should also have a low dielectric constant, so that its capacitance is low and thus allows high speed signal propagation. $SiO_2$ satisfies all of these requirements. Thermally grown oxide for the

recessed oxide layer, as well as sputtered or CVD silicon dioxide for successive ILD layers, are robust insulators for MLM applications. More complex structures have been suggested using dual dielectrics such as oxide-nitride repeating layers which can offer reduced defect densities. New organic dielectrics must match and even surpass these properties to be considered as a replacement for these proven insulators. A change from this conventional process is required for several reasons.

First is the loss of planarity in the conventional process. Sequential deposition of multiple layers causes topology to develop which leads to difficulties in both reliability (step coverage) and lithography. Lithographically it is difficult to pattern a nonplanar surface due to depth of focus limitations. The topology also causes shadowing during metal deposition. Some form of planarization is necessary, requiring many additional processing steps, and a further complication is the difficulty in gap free deposition of dielectric between metal lines.

A second reason to change from $AlCu/SiO_2$ is the need for higher performance, which calls for low resistance and a reduced dielectric constant. The dielectric constants of $SiO_2$ and $Si_3N_4$ are 3.9 and 7.5, respectively. These are high compared with organic dielectrics which have dielectric constants ranging from about 2.5 to 3.5. The resistance of AlCu alloys is in the range of 3.2 μohm-cm, higher than copper-rich alloys which are less than 2.0 μohm-cm. Solomon[4] has argued for cryogenic operation which reduces metal resistance. Perhaps a more attractive alternative involves the use of Cu-rich alloys, with resistivity less than 2 μohm-cm,[5] and an organic dielectric insulator like polyimide with a lower dielectric constant of about 2.9. Such a structure has been demonstrated by Small and Pearson[1] for an experimental 64 kB SRAM chip.

A third reason for change is that density drives the requirement for a smaller line to line pitch. This unfortunately increases crosstalk between interconnections. This can be offset by the use of organic dielectrics with lower dielectric constants.

A planar Cu-polyimide wiring scheme described by Small and Pearson is shown in Fig. 1. The first tungsten contact is made in PECVD oxide. A trilayer insulator structure of $Si_3N_4$/polyimide/PECVD $Si_3N_4$ is then deposited. The organic dielectric constant is between 2.8 and 3.1. The $Si_3N_4$ layer acts as a Cu diffusion barrier, forms an adhesion layer between the polyimide layers, prevents Cu hillock formation, and prevents solvent absorption by the completed polyimide layer when the layer above is spun on. The metal described is 500 Å Ta/Cu/Ta, where the Ta helps adhesion

and prevents diffusion of Cu. Low contact resistances were reported with 90% yield on 64 kB SRAMs. Reliability was also good, demonstrated after the chips were treated for 12 thermal cycles (30 minutes at 400°C) and 100 cycles to 77 K. No effects of stress, such as change in line resistance, and diffusion effects, as measured by diode leakage measurements, were observed.

**Figure 1.** A planar Cu-polyimide wiring scheme. *(After Small, et al.[1] Reprinted with permission.)*

The change to an organic dielectric will call for a new process sequence. The design of such a sequence will require qualification of new materials. A judicious design reduces cost and maintains or improves reliability. Cost, complexity, reliability, and performance issues pose a conundrum.[6] One of the main attractions of organic dielectrics is their low cost; in fact, polyimides are used in many cost-performance offerings, as pointed out in Sec. 2. Photosensitive polyimides are particularly attractive, as several photoresist apply-and-remove steps may be eliminated.

This chapter talks specifically about the use of organic dielectrics in multilevel metallization. This section is meant as an overview of the emergence of organic dielectrics and as an introduction to some applications. These materials are reliable, inexpensive, defect free, and can withstand high (400°C) processing temperatures.

Section 2 of this chapter presents the reader with a historical introduction which describes the realization in the late 1970s of the need for planarity and low dielectric constant, and the search for high temperature organic dielectrics. Section 3 introduces the reader to some of the chemistry of polyimides. Sections 4 and 5 describe processing steps to build a multilevel metallization scheme, and Secs. 6 and 7 conclude with some reliability and performance issues. A discussion of some possible future trends for this technology is presented in Sec. 8.

This chapter is written as both a general introduction to the beginning engineer, as well as a reference for the experienced engineer. References are given to several companies actively involved in this growing field which the authors hope will increase the reader's interest in these new materials. Let us begin with a discussion of the historical evolution of organic dielectrics.

## 2.0 HISTORICAL PERSPECTIVE

The application of organic dielectrics to ICs began in the early 1970s when the use of polyimide for multilevel metal interconnections was reported by the Japanese.[7] The first publication talked about a completely new planar method permitting step-free multilevel interconnections. It was the desire to achieve some degree of planarization which provided the incentive to investigate polyimides as dielectric materials.

The need for planarity arose in the 1970s due to the need for multilevel metal. Initially just two levels of metal were required, and Hitachi introduced a material called PIQ which was incorporated into routine production in 1975. The PIQ material was described as a thermally stable polyimide resin specially synthesized for use on semiconductor devices.[8] For the via hole etch process, a hydrazine solution was utilized. The desirable properties which were noted were low residual stress (compared with CVD $SiO_2$), high temperature stability (450°C, compared with conventional polyimides at 400°C), good breakdown voltage strength, and low dielectric constant. The reliability tests reported showed excellent results.

Within the U. S., however, the use of hydrazine as an etchant was too hazardous for use in a manufacturing environment. Alternative via hole processes were developed for polyimide films. In 1975, Yen[9] described a technique where a partially cured polyimide film could be etched with a caustic positive photoresist developer solution. In 1978,

IBM introduced a new semiconductor memory technology called SAMOS which incorporated polyimide as part of the dual dielectric insulators between metal layers and as a top layer passivation coating.[10][11] The dual dielectric was composed of silicon dioxide and polyimide layers. The via holes were etched in the polyimide using one mask level where the photoresist developer additionally served as the polyimide etchant. After the photoresist strip, a second photoresist layer was applied to etch the vias through the silicon dioxide layer. Through the use of two dielectrics and two mask steps, an extraneous hole will occur only in the unlikely event that dielectric or photoresist random defects are coincident. This provided a significant reduction in defect density. The use of the polyimide cushion on the rigid silicon dioxide layer also provided improved mechanical properties, resulting in better integrity of metal lines and metal interconnections.

A cross-sectional diagram of the SAMOS multilevel metal structure is shown in Fig. 2. The two levels of polyimide can be seen, with the second layer being much thicker for passivation purposes. The lines terminate on lead-tin pads which are bonded by flip-chip technology onto the package.

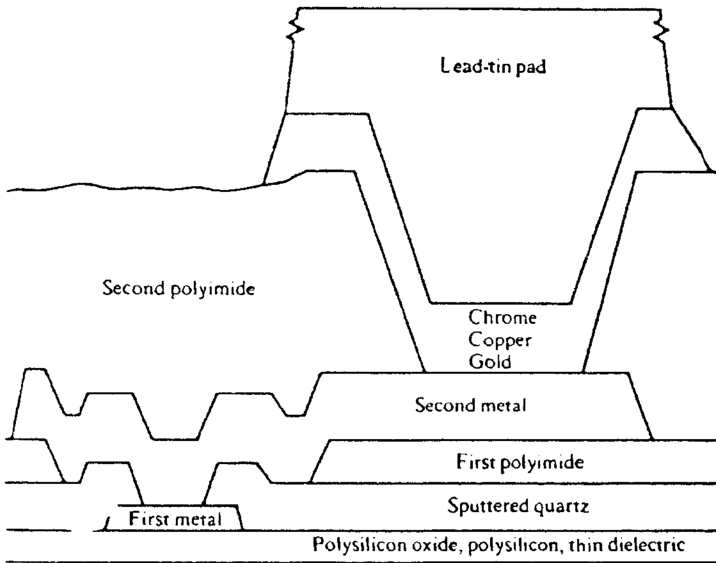



**Figure 2.** General view of metallization and passivation layers used in SAMOS. The structures are roughly to scale, with the exception of the much-reduced pad height. *(After Larsen.[11] Reprinted with permission.)*

One of the unique features of the SAMOS process was the built-in redundancy. After the second level of metallization, the wafers were tested for functionality. Chips which were non-perfect but repairable could have the failing addresses written into the second level metal by blowing the redundancy fuses. The final chip seal was provided by a second layer of polyimide, the thickness of which was sufficient to cover all metal exposed during the fuse-blowing operation. Only a polyimide layer could sufficiently cover the structure after the fuses were blown. This was one of the key aspects which kept polyimide in the process.

In the late 1970s and early 1980s, the need to go beyond two levels of metal was being recognized by many.[12][13] It was felt that the emerging techniques of VLSI would place increasing burdens on the technologies necessary to interconnect components of higher complexity and density on a single silicon surface. It was predicted that at least three levels of metal would be required with high resolution vias. The insulating layers should have reduced pinhole densities, superior dielectric properties, adhesive and temperature tolerant properties, and provide no contamination to the underlying silicon devices. Most important was the need to provide gradual changes in surface slope and some self leveling or planarization to permit good step coverage in overlying high resolution conductor lines. In addition, an inexpensive, low temperature, controllable batch operation was highly desirable. (These same statements could be applied today.) The need for a planarizing material was twofold: in order to attenuate the topography so that high resolution lithography can be done, and to provide reliability in the metal interconnections.

The first planar process, which was described by Sato,[7] involved using polyimide to supposedly planarize the underlying metal pattern, followed by an etchback of the polyimide to expose the "bumps" or metal interconnections. Later it was shown[14] that, due to the many geometry effects, it is not possible to completely planarize a typical metal pattern with a polyimide film. Good edge coverage, however, is obtained with all polyimide films even when full planarization is not achieved. By making use of certain geometry effects, such as providing narrow spaces that will be planarized by polyimide, a process was developed for fabricating a planar multilevel metal-insulator structure.[15][16] An example of the planarity achieved on a four level metal interconnection scheme using polyimide is shown in Fig. 3.

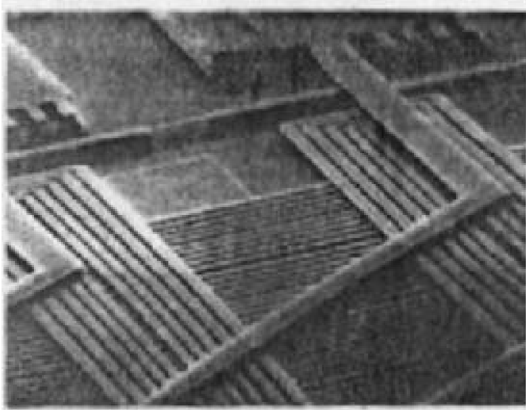


**Figure 3.** SEM after four layers of metal completed. The polyimide is removed to illustrate planarity. *(After Rothman.[15] Reprinted with permission).*

There were several ways to obtain the integration density that was being projected. Other alternatives to multilevel metal were smaller ground rules or larger chips. It is apparent from the literature that many companies decided to implement the latter of these alternatives rather than explore the use of polyimide.

Possible reasons for the cautiousness with the use of polyimide were concerns about polarization and water absorption.[17] However, reliability data amassed over several years and specifically addressing polarization, water absorption, and possible corrosion consequences in non-hermetic packages have not contradicted the viability of polyimide.[18]–[20]

Several polyimide investigators have asked the question as to why polyimide is not more widely implemented in the semiconductor industry. Eight years after the first paper by the Japanese, there were several publications on the use of polyimides but very little about their actual implementation. Part of this may be due to the resistance to make changes—evolutionary versus revolutionary practices within the semiconductor industry. Inhibitors to change include the skills available and the practices used in an organization. Change to new technologies is invariably resisted, particularly where the role of management has evolved into one of improving the efficiency of the existing systems rather than preparing and innovating for the "new." As a result, technologies are invariably introduced by newcomers to the industry. Despite the rapid advances in silicon

chip technology in the past twenty years, VLSI has really evolved through steady process improvements. Therefore, current skill levels and practices built up over the years in semiconductor fabrication discourage change to new technologies and new materials.[21]

The use of polyimide for packaging applications such as multichip modules started to appear in the 1980s. The people working on packaging technologies were already used to dealing with organic materials, so there was probably less of a barrier to its use compared with semiconductor technology. The multichip module technology borrows ideas from both the hybrid or printed circuit board and from the semiconductor areas.

In the late 1980s, some reports of polyimide applications started to appear in the literature.[18] IBM introduced the use of polyimide in a metallized ceramic package with an insulating layer of polyimide to allow for an additional wiring plane. Figures 3 through 6 show examples of some of the packaging applications of polyimides. The films used in the packaging were generally thicker and the ground rules were much larger, which made for relaxed tolerances on critical dimensions. Other articles appeared[20][22]–[27] which described the use of polyimide for high density thin film wiring on ceramic packages. The low dielectric constant of polyimide was the driving force behind its use. The excellent processing characteristics of polyimide coupled with its chemical resistance and high temperature stability were desirable.

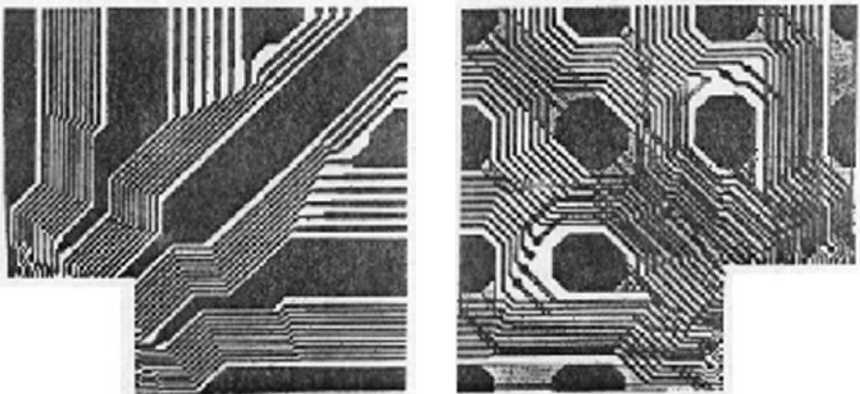


**Figure 4.** Photomicrograph of metal lines in polyimide on metallized ceramic. *(After Homma and Posocco.[18] Reprinted with permission.)*

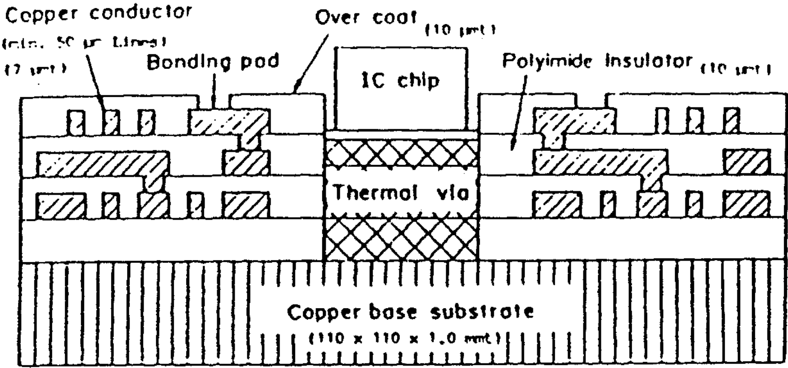



**Figure 5.** A schematic of the MCPM (Multilevel Copper- Polyimide-Module) structure. *(After Kimbara, et al.[24] Reprinted with permission.)*

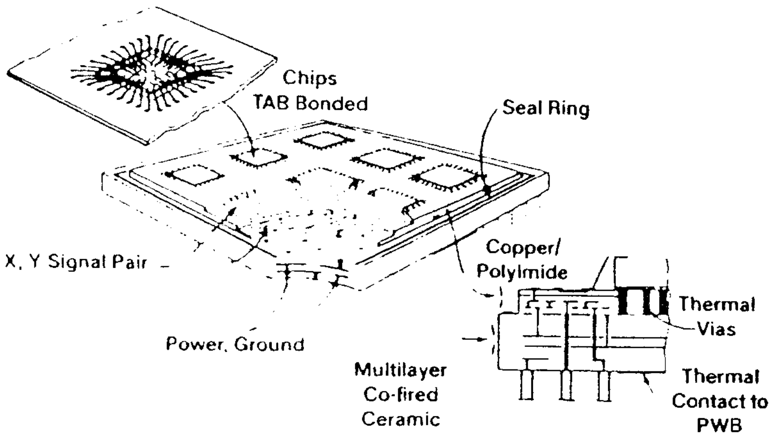



**Figure 6.** A multilayer thin film package structure showing the use of the copper polyimide wiring scheme. *(After Chao, et al.[27] Reprinted with permission.)*

Significant advances in the development of new polyimide materials designed specifically for the semiconductor applications also occurred in the '80s. Coefficients of thermal expansion (CTE) could be modified to match the CTE of metals or inorganic materials used in the fabrication of ICs. Resistance to moisture absorption could be achieved. Later, improved photosensitive polyimides became available. The list of advantages provided by polyimide included:

1. The use of a solution and the spin coating technique which allows:
   a) the possibility of cassette-to-cassette in-line processing
   b) planarization of underlying topography resulting in more reliable wiring
   c) lower defect levels (compared to vacuum processes)
   d) low cost process
   e) low temperature process without detrimental effects such as radiation damage or field enhanced contamination
2. Vias are easily patterned by wet or dry etching with good slope control.
3. Low dielectric constant (< 3.5).
4. Chemical resistance.
5. High temperature stability.
6. Versatility of chemical synthesis allows the optimization of polymer properties for specific applications.
7. Low stress allows for thicker films providing the ability to improve transmission line characteristics.

More applications of polyimide started to appear in the literature in the late 1980s. Polyimides are most popular as top passivation layers where they provide protection from moisture, corrosion, ion transport, and damage during packaging. Another type of passivation layer is the alpha particle barrier that is applied to high density memory devices to prevent soft errors. Polyimides are free of radioactive emitters and they effectively absorb alpha particles emitted by ceramics or other inorganic materials.[28]–[30] In addition, polyimide can be used as a stress buffer when applied at either the wafer level or at the packaging level. The

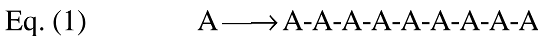
use of polyimide as an interlayer dielectric has been implemented mainly on high density multilayer packages. The Japanese are leading the industry in the use of photosensitive polyimides as interlayer dielectrics in high density interconnect applications. Hitachi, Mitsubishi, Toshiba, and NTT have all announced HDI packages using photosensitive polyimides.[23][24][31] The following sections will provide details on polyimides and other organic dielectrics, their processing and reliability. Hopefully the reader will find many applications for these versatile materials.

## 3.0 FUNDAMENTAL CHEMISTRY OF ORGANIC DIELECTRICS

Thus far in our discussions on organic dielectrics, we have discussed some of the advantages of these materials and their historical evolution. Let us now explore some of the chemical structures and physical properties that arise from these materials.

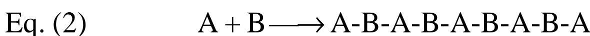
### 3.1 Materials Options

The class of materials that form these organic dielectrics are known as polymers. Polymers are composed of repeating units of smaller organic materials known as monomers. These monomers contain one or more reactive groups which under certain conditions react with one another to form long chains. For example, the schematic below shows a monomer A, which undergoes polymerization to form a chain of monomers.



Eq. (1) $$A \longrightarrow A\text{-}A\text{-}A\text{-}A\text{-}A\text{-}A\text{-}A\text{-}A\text{-}A$$

In other cases, two different monomers may react with one another to form a chain of monomers with an alternating structure as shown below:



Eq. (2) $$A + B \longrightarrow A\text{-}B\text{-}A\text{-}B\text{-}A\text{-}B\text{-}A\text{-}B\text{-}A$$

A polymer that is made of more than one component is called a copolymer. Most of the materials discussed in this section fall into this class. They generally form chains of very long length which can wrap around each other and add to the mechanical strength of the materials.

Most of these materials are high molecular weight polymers made from building blocks of aromatic organic monomers. The high temperature properties are generally obtained through a polymer cross-linking mechanism. This forms what is known as a class of compounds called network polymers. The materials begin as long chain polymers with reactive groups which can begin to cross-link at elevated temperatures and form 3-dimensional networks of polymers. Linear chain polymers such as Teflon do not contain these groups and will not cross-link upon further heat treatment.

The most common organic dielectrics used as multilevel metal dielectrics are materials that can withstand high processing temperatures, have low dielectric constants, and are easily integrated with semiconductor materials. A list of some of the more common organic dielectrics and some of their properties are shown in Table 1 below. While this is clearly not an exhaustive list of organic dielectrics, it describes some materials from several classes of polymers. For a more thorough treatment of high performance polymers, see Bureau, et al.[32]

**Table 1.** Glass Transition Temperature $T_g$, the Dielectric Constant, Solvent, and Dielectric Strength for Various Commonly Used Organic Dielectrics

| Polymer | $T_g$ °C | $\varepsilon_p$ | Solvent | Dielectric strength | Ref. |
|---|---|---|---|---|---|
| PMDA-ODA | 450 | 3.6 | NMP | 4.0E3 V/mil | 1 |
| BTDA-ODA | — | 3.5 | NMP | 4.0E3 V/mil | 1 |
| Teflon | <200 | 2.2 | — | — | 4 |
| Benzo-cyclobutene | <360 | 2.6 | Xylene | — | 5 |
| Polyquinoline | 288 | 2.8 | Cyclopent-anone | 7.3E6 V/cm | 6 |
| Thermid | 320 | 3.1 | NMP | — | 57 |
| PIQ | 450 | 3.5 | DMAC | 1.0E6 V/cm | 78 |
| PPQ | 365 | 2.7 | Toluene | 2.0E6 V/cm | 6 |
| Paralene | 70 | 2.7 | CVD | 7.0E3 V/mil | 2 |
| Polyimide Siloxanes | >200 | 2.9 | Diglyme | 1.2E6 V/cm | 3 |

Some materials which have the best dielectric properties exhibit certain undesirable properties. Teflon, for example, has a dielectric constant of about 2 at room temperature. Its melting point however, is in the range of only 260–280°C.[33] This provides certain limits to the type of processing that can be done after the dielectric layer is in place. In general, metal depositions which occur after the organic dielectric is in place cannot exceed the glass transition state temperature ($T_g$) of the polymer. These metals are usually sputtered or evaporated onto the polymers which requires the polymers to be compatible both chemically and mechanically to the deposition process.

To get a more general view of some of the temperatures involved in conventional semiconductor and metallization processing, several process steps and their temperatures are plotted in Fig. 7. As shown in the figure, only organic materials with reasonably high melting points are usable for today's multilevel metal interconnect schemes.

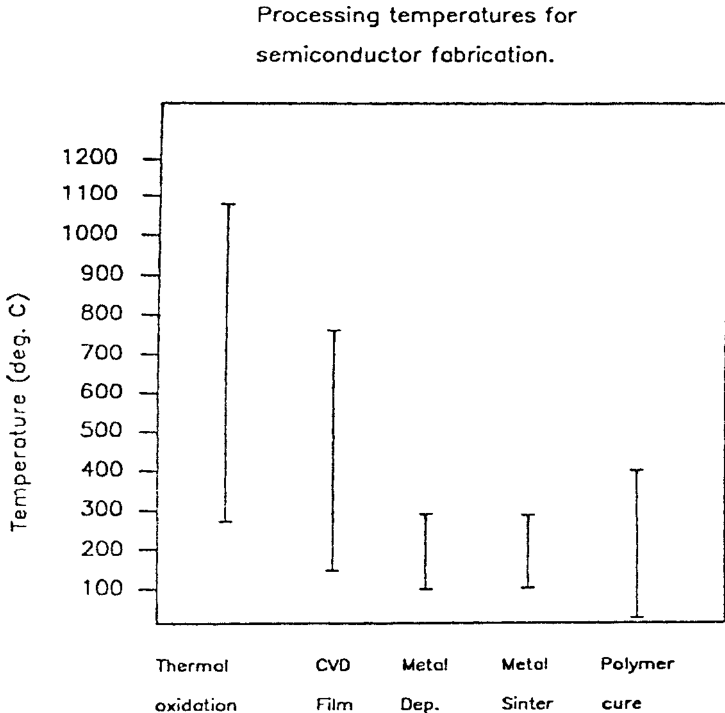



**Figure 7.** Examples of processing temperatures for various semiconductor processing operations. No process over 400°C can follow the polymer cure.

As shown in Table 1, several leading candidates for organic dielectrics have emerged due to their combinations of superior processability, thermal stability, and dielectric properties. Many of these polymers contain aromatic rings or heterocyclic structure. Chains made from these compounds tend to have more thermal stability than simple aliphatic (saturated) structures. As we have discussed earlier in the historical section, polyimides have emerged as the most common family of polymers studied for multilevel interconnect technology. More recently enhancements to these material have resulted in fluorinated polyimides (FPI) which have excellent thermal and dielectric properties. One fluorinated polyimide was evaluated at Motorola with an integrated tungsten via plug process.[34] Several new variations of polyquinolines are also gaining attention due to their relative moisture insensitivity.[35] Dupont is also publishing data on a new Teflon material called Teflon-AF.[36] This fluorinated polymer has one of the lowest dielectric constants (epsilon approx. 1.89) of any polymer described for microelectronics applications.

For the sake of example, let us examine the most widely used class of materials, polyimides, for their chemistry and processing properties.

## 3.2 Polyimide Structure

Polyimides are a general class of compounds which consist of a polyamic acid monomer. Upon polymerization, these compounds undergo condensation reactions to form the polyimide polymer chains. Figure 8 shows several dianhydride materials and a diamine. Pyromellitic dianhydride (PMDA) and benzophenone tetracarboxylic acid dianhydride (BTDA) are shown to react with the diamine oxydianiline to yield the polymers PMDA-ODA and BTDA-ODA respectively.

The process of the formation of the polyimide polymer is a condensation reaction. For the sake of clarity let us again look at the PMDA-ODA reaction in Fig. 9. Nucleophilic attack of the amine on the carbonyl group of the PMDA gives the amide intermediate. Upon further heating, the remaining acid moiety can react with another amine in solution or the amide on the adjacent leg of the molecule. Upon the loss of two molecules of water, the final condensed phase of polyimide is formed.

Upon continued heating of many of the polyimide films, it can be seen that cross-linking between adjacent polymer films can be achieved. This cross-linking is important in imparting many of the high temperature properties of these films. This baking of the polymer to achieve

the idealized film property is known as curing. Much work on curing has been done in the recent years to optimize the cure cycles with specific applications.

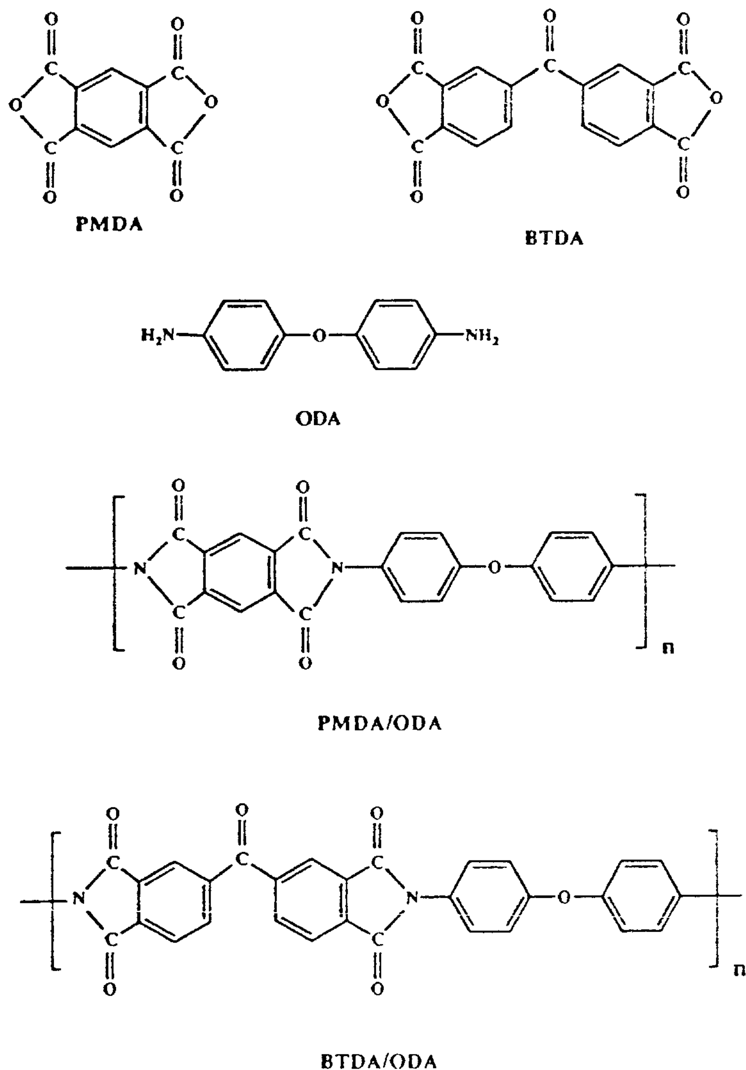



**Figure 8.** The chemical structures of various monomers and polymers used in the synthesis of commercial polyimides.

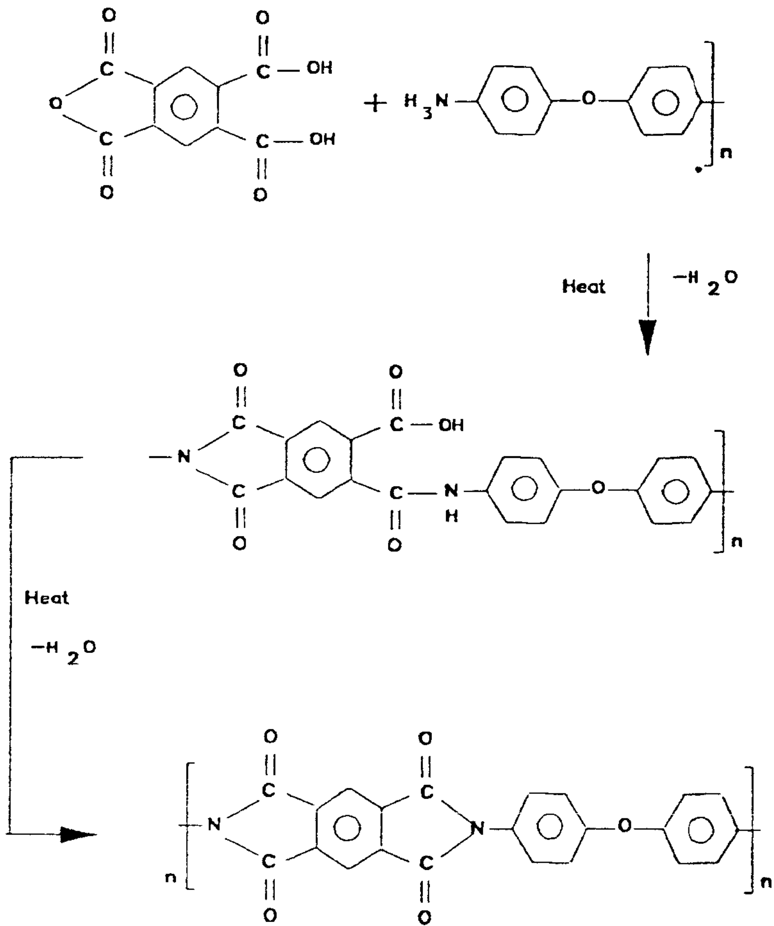



**Figure 9.** Diagram of the reaction sequence in the synthesis of polyimides.

Figure 10 shows an idealized cure cycle for several other polyimide structures. Here again, high temperatures are required both to insure complete imidization as well as to drive off the water formed as a reaction by-product. A more detailed discussion of curing will be discussed in Sec. 4 of this chapter, relating to specific process design.

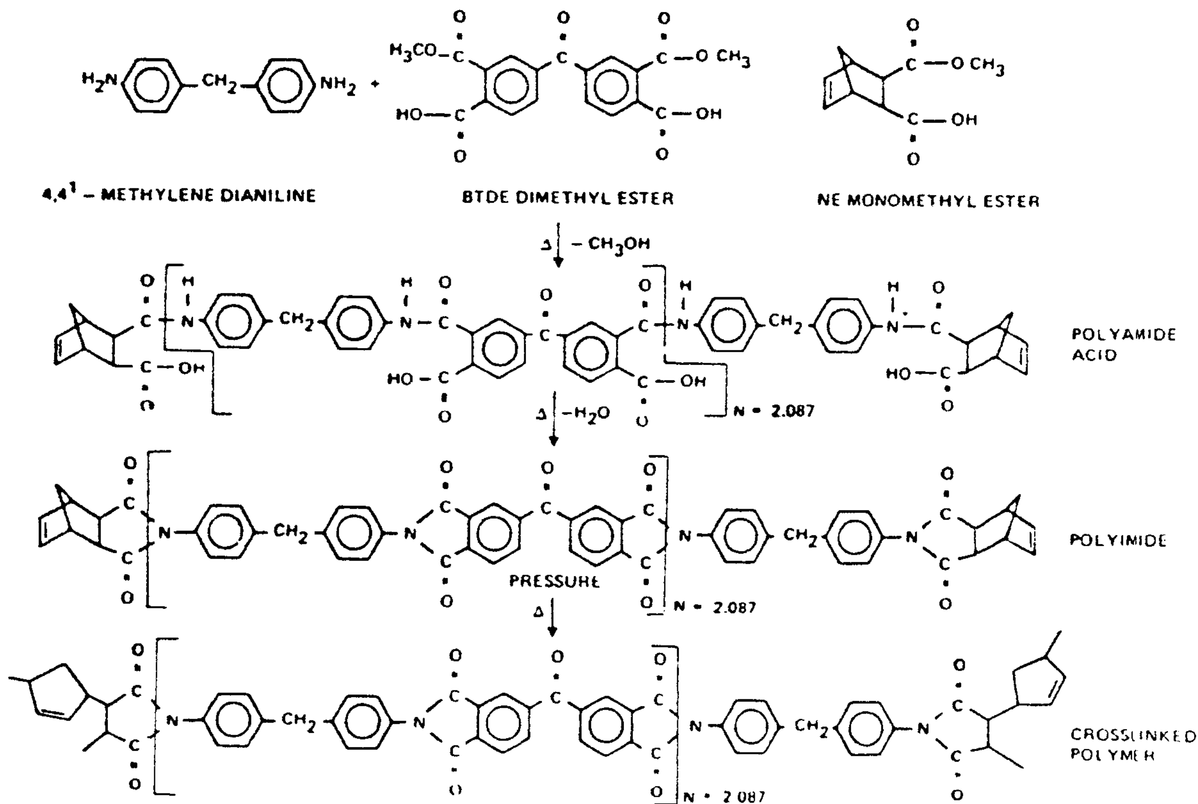



**Figure 10.** Shows the idealized cure sequences of PMR-15 resin.

## 3.3 Depositing Polyimides

The most common method of depositing polyimide films is spin casting or spraying from a polyamic acid solution. Here the choice of solvents, viscosity, and many other factors needs to be considered in order to choose the correct material for a specific application. The film is first baked at a temperature of about 120°C to evaporate off the solvent. The most commonly used solvent in many polyimide films is N-methyl, 2-pyrollidone (NMP). The cure cycle may be done in several steps at temperatures ranging from about 250–450°C for up to several hours. Here, the use of thermogravimetric analysis (TGA) is useful to determine the decomposition points for a particular polyimide film. A TGA curve for a typical polyimide is shown in Fig. 11.[37] The solid line in the diagram refers to the percent weight loss as a function of temperature. The dotted line represents the derivative of the weight loss curve. The derivative defines two major transitions at about 200°C and 250°C as shown by the vertical dotted lines. This is useful in determining volatile components of the organic dielectric. To ensure proper adhesion of the polyimide layer to the substrate, adhesion promoters are generally applied. Here, as with many photoresists, organosilanes are popular materials. The silyl or siloxane moiety of the adhesion promoter forms a good bond with the available hydroxyl groups on surfaces such as silicon dioxide. The organic ligands provide a good surface for the polymers, giving rise to strong adhesion between the films. A more thorough discussion of adhesion is discussed in a later section.

## 3.4 Moisture Absorption

One of the most critical properties in the use of polyimides in multilevel interconnect dielectrics is their ability to absorb water. The films tend to be hygroscopic after curing when allowed to come in contact with the atmosphere. Water itself is a by-product of the condensation reaction to form polyimides as mentioned earlier. Furthermore, the polymer contains many oxygen atoms which may impede the liberation of water due to hydrogen bonding. Usually, after sufficient curing, however, the films will contain very little water.

Water in the polyimide films affects several of the physical, material, and electrical properties of the film. The amount of water absorbed in polyimide dielectrics has been shown to be directly related to the dielectric constant.[38] A graph of the moisture content vs dielectric constant is shown in Fig. 12.

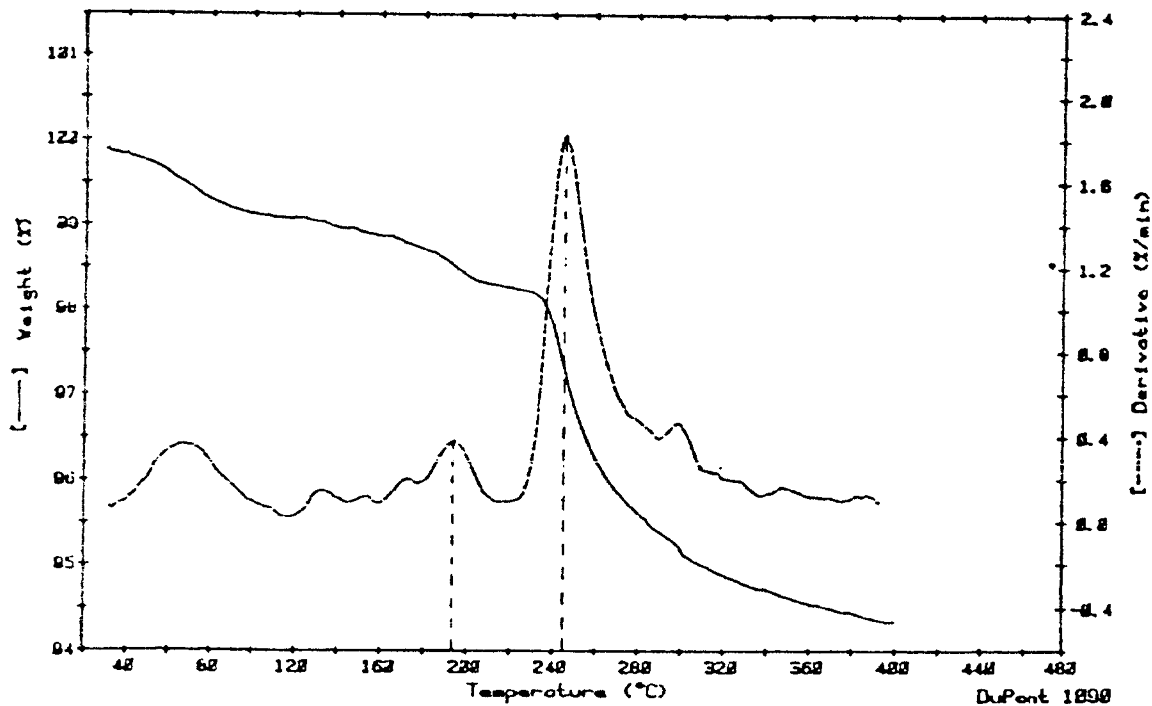



**Figure 11.** Shows the TGA analysis of a polyimide done in He from 40–400°C.

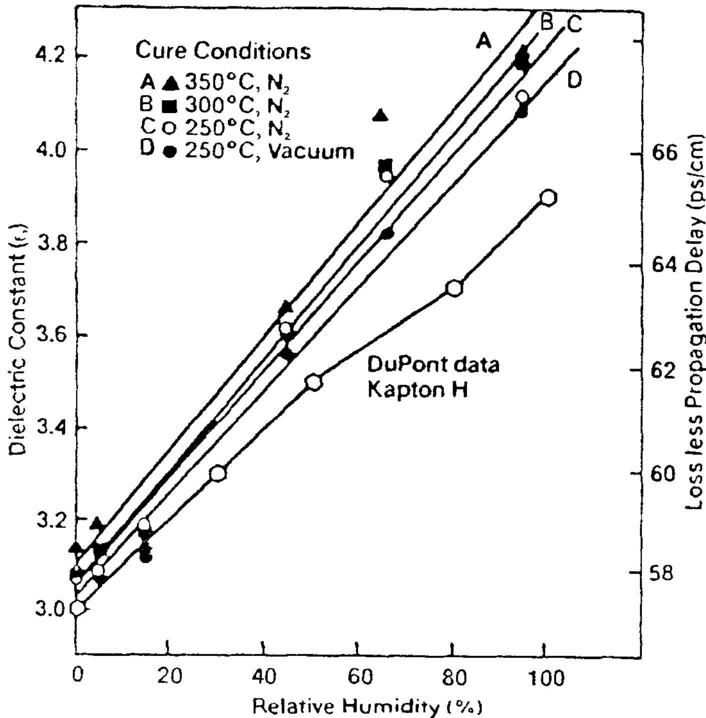



**Figure 12.** Shows the variation of dielectric constant with relative humidity.

Humidity affects many other properties of the polyimide films besides dielectric constants. The ac dielectric strength is decreased with increasing water content. Furthermore, the dissipation factor increases dramatically with increasing humidity. The dissipation factor, or tan delta as it is sometimes referred to, is a measure of the signal loss in the dielectric as a function of frequency. This loss factor is associated with the slower rate of change of polarization with respect to the electric field. Electronic and molecular polarization contribute to the dissipation factor in organic dielectrics.

As is shown in Table 2, humidity affects the dielectric properties of polyimide films tremendously. The dielectric strength drops precipitously with increasing humidity along with a considerable rise in the dielectric constant.

**Table 2.** Relative Humidity vs the Electrical Properties of Kapton

| % Relative Humidity | AC Dielectric Strength | | Dielectric Constant | Dissipation Factor |
|---|---|---|---|---|
| | V/µm | V/mil | | |
| 0 | 339 | 8600 | 3.0 | 0.0015 |
| 30 | 315 | 8000 | 3.3 | 0.0017 |
| 50 | 303 | 7700 | 3.5 | 0.0020 |
| 80 | 280 | 7100 | 3.7 | 0.0027 |
| 100 | 268 | 6800 | 3.8 | 0.0035 |

(For calculations involving absolute water content, 50% RH in our study is equal to 1.8% water in the film and 100% RH is equal to 2.8% water, the maximum adsorption possible regardless of the driving force.)

### 3.5 Solvent Effects

The solvents used in the various polymer films can have a major effect on the properties of the materials. For example, spin casting a film from a low boiling point solvent may cause striations in the film uniformity and a high degree of mechanical stress and thinning if the solvent is boiled off too quickly. High molecular weight polymers generally require a highly polar solvent to keep them in solution over a long time period. In the case of polyamic acids, the precursors to polyimides, the solvents even affect the rate of imidization. Solvents which have too high a boiling point may also be difficult to remove completely during the cure cycle, which makes them more likely to outgas during subsequent processing. This can be a major reliability impact on multilevel metal interconnection processes, especially when a cap of nonporous insulator is coated over the polyimides. Outgassing of solvents can exert pressure from within the matrix causing distortion or breakage of metal lines. Finally, if the solvent used can hydrogen bond to oxygen atoms in the organic dielectric, it can make the solvent much more likely to remain trapped inside the polyimide, even after full cure cycles.

## 3.6 Oxidation

Since the chemical bonds in the polyimide tend to be quite stable, very little oxidation or weight loss of the film is observed at temperatures below 300°C. With the exception of solvents, the film will begin to show weight loss at temperatures above 400°C, especially in an air ambient. When the film is processed in an inert gas, the temperature the film can withstand increases to more than 500°C. The isothermal weight loss can be seen for various temperatures and ambients in Fig. 13.

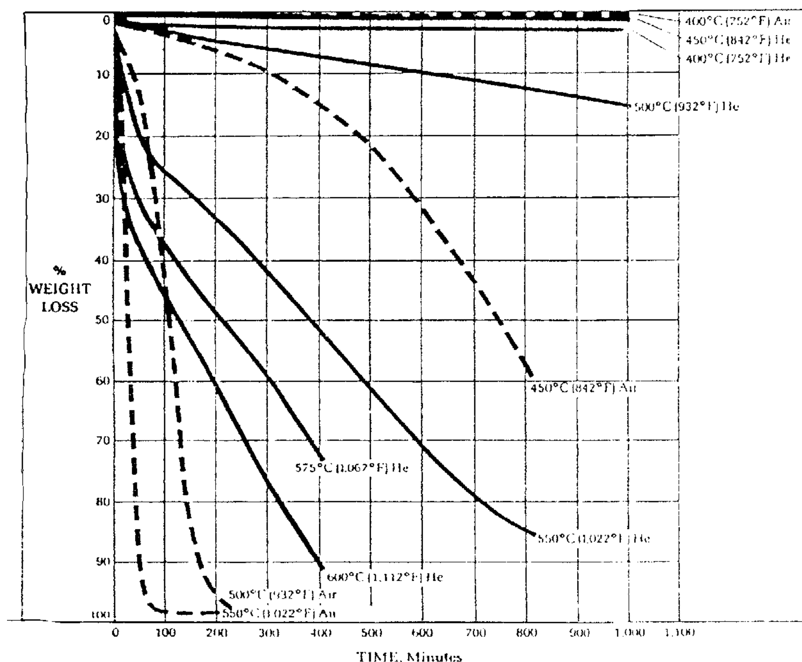



**Figure 13.** The isothermal weight loss vs time in different ambients.[33] *(Reprinted with permission.)*

## 3.7 Dimensional Stability

The dimensional stability of the film or shrinkage is dependent on several factors. The differences in the coefficients of thermal expansion between the film and substrate cause residual stresses to be placed on the films during manufacture. The shrinkage in a normal multilevel metallization scheme is also very critical. If the shrinkage causes the polymer to pull away from the metal lines, an air gap becomes available which can provide a channel for corrosive agents or moisture. The thermal coefficient of expansion varies from polymer to polymer but must be considered when dealing with reduced lithography tolerances. Some typical values for Kapton polyimide films are given in Table 3. The stresses put on the films and the wiring during curing can affect the overall reliability and integrity of the structure. These stresses may limit the overall dimensions of the multilevel metal structure. These same dimensional characteristics which affect the bulk films become important when dealing with photosensitive polyimides. This topic will be discussed in a later section.

**Table 3.** Shows the Thermal Expansion Coefficient of Kapton at Different Temperature Ranges

| Temperature Range | ppm/°C |
|---|---|
| 23–100°C (73–212°F) | 18 |
| 100–200°C (212–392°F) | 31 |
| 200–300°C (392–572°F) | 48 |
| 300–400°C (572–752°F) | 78 |
| 23–400°C (73–752°F) | 46 |

(Type HN film, 25 μm thermally exposed)

## 3.8 Metal-Polymer Interactions

A great deal of work has been done to understand the interactions between metal and polymer surfaces. Let us begin with a discussion of an ideal case where individual polymer molecules are free to interact with metal atoms. The field of organometallic chemistry is very complex and the literature is filled with cases of organometallic molecules, charge transfer complexes, and metallocenes. We do not have the time in this text to investigate all of the proposed structures; however, let us take a simple look at an ideal metal to polyimide surface.

It has been theorized by Chou[39] that the reaction of chromium metal with PMDA-ODA is a delocalized bonding between the Cr atom and the PMDA monomer. Figure 14 describes a condition whereby the d-orbitals of the chromium atom can overlap the pi-electrons on the PMDA molecule to form a stable charge transfer complex. Photoemission spectroscopy was used to obtain data which was analyzed using quantum chemical calculations of the lowest unoccupied molecular orbital for the PMDA molecule. Results show that the most energetically stable configuration comes from this d-orbital which overlaps constructively with the pi-orbital of the PMDA monomer.

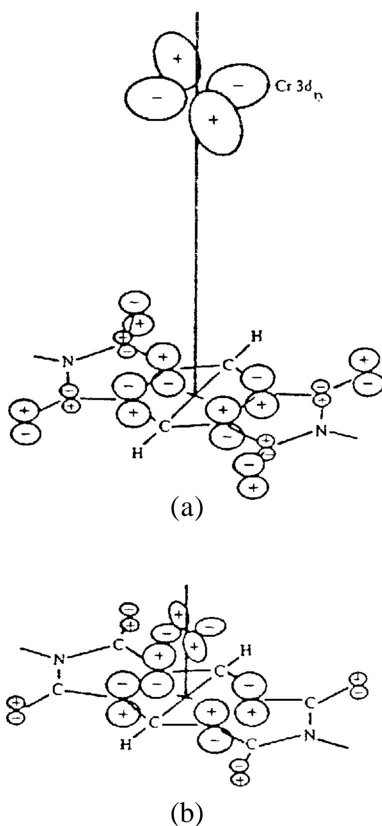



**Figure 14.** (*a*) Highest occupied molecular-orbital (HOMO) diagram for the lowest unoccupied molecular orbitals (LUMO) of the PMDA monomer when chromium atom is sufficiently distant to be non-interacting. (*b*) Chromium over the six-member central ring of the PMDA monomer. The phases of the d(*xy*) levels add constructively to the pi-levels of the monomer, giving rise to a stable bonding configuration. *(After Ho, et al.[40] Reprinted with permission.)*

If we extrapolate this understanding of these transition elements with unfilled d-orbitals for bonding, we can expect there to be similar complexes formed between polyimides and these metal surfaces. If we use a measurable property such as adhesion to examine the polymer-metal interface, we might expect these refractory metals to have a higher bonding energy than those of the noble metals, which have few or no unfilled d-orbitals available for these bonding interactions. Indeed, it has been observed[40] that the adhesion energy and peel strength for Ti and Cr are greater than for those of Al and Cu, which are traditional metals used in semiconductor metallurgy schemes. The observed trend for these metals is shown in Fig. 15 below.

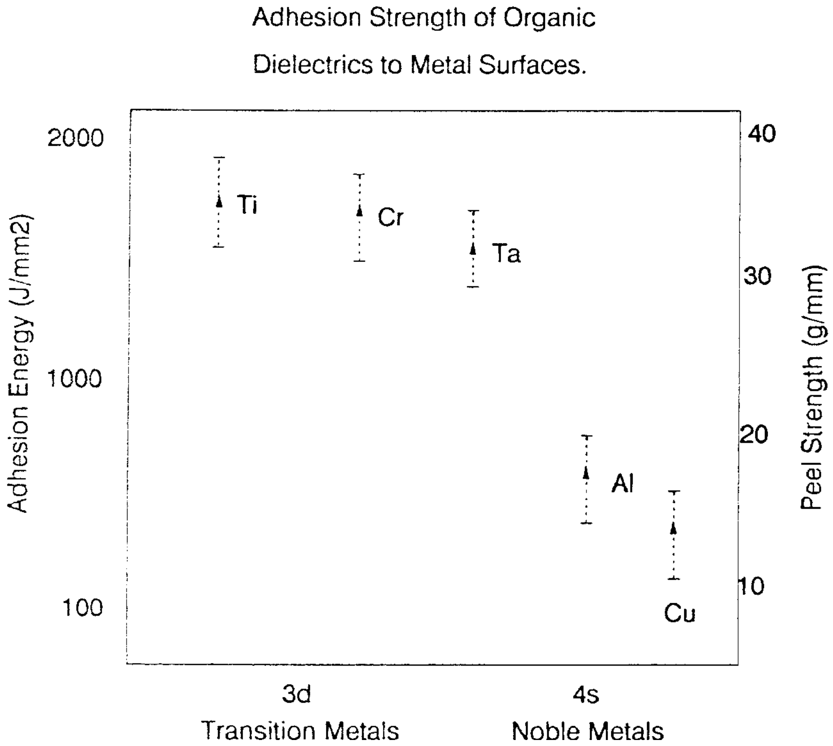



**Figure 15.** Shows the variation of adhesion energy and peel strength for 3d transition metals and 4s noble metals, data compiled from various sources.

If indeed this trend is observed for most dielectric polymers, then process design engineers need to develop a metallurgy which is consistent with all of the necessary properties of VLSI interconnects. In order to obtain the low resistivities of metals such as Cu and Al and also have the enhanced adhesion of some of the transition elements, several schemes have been suggested[41] which build on a layered structure of a chromium liner over and under the polymer for adhesion, with a sandwich of Al in between. This has been shown not only to improve the adhesion and conductivity of the lines, but also to improve the electromigration lifetime. These added benefits have led to a host of novel metallization schemes and alloys which can be used with both organic and inorganic dielectrics.

While the understanding of the bonding between metals and polymers is complex, it is important to note that the metal-polymer interface is very dependent on how the films are put down, in what order, at what temperature, and using what technique. Surely the case of coating an organic film over a metal surface produces one type of interface, while depositing a metal over an existing organic surface may produce another. It has been suggested that the deposition of a metal on a polymer film by sputtering can lead to a degradation of the polymer film surface which can be shown by spectroscopy to resemble a carbonized layer.[42] This organic-metal interface would clearly not resemble the idealized bonding structure proposed in Fig. 14. Therefore, the process design engineer must carefully consider not only the metals involved, but the method of integration which will produce an interface specific to their application.

### 3.9 Photosensitive Organic Dielectrics

In recent literature[43] there has been much discussion on photosensitive dielectrics. These materials have enormous potential since they can be selectively patterned, which leads to a reduction in the number of steps needed to build a multilevel metallization structure. In general, a photoactive component (PAC) is built into one of the arms of the monomers used to build the polymer. After illumination at the proper wavelength, the PAC is converted to a base-soluble material which can be removed by development in aqueous base solutions. This eliminates the need for an additional photoresist layer which is required to pattern conventional polyimides. The materials have certain limitations, however, such as control of the critical image dimensions. This is mainly caused by excess solvent in the photosensitive materials which cannot be baked out

without decomposition of the PAC. There are also the mechanical stresses in the films which must be factored into the final linewidth variation.

### 3.10 Summary

Organic dielectrics are just beginning to show promise in applications such as insulators for multilevel interconnections. A great deal has been learned about these novel materials over the past several years. We have seen that the driving force towards moving to organic dielectrics is their superior electrical characteristics. Furthermore, these materials are light-weight, easy to apply, and available from several commercial sources.[14]

While specific organic materials have been mentioned thus far in our discussions, we in no way have scratched the surface of describing the vast field of organic dielectrics. In the case of polyimides alone, we have only mentioned the condensation of several amines with electrophilic anhydrides. In reality, there are nearly infinite combinations of such materials which can he polymerized to yield thin films of this type. Unfortunately, many are not suitable due to their instability at high temperatures or their dielectric constants.

In summary, it has been suggested by many working in the field that the ideal organic dielectric is yet to be found. Much work in future years should yield a host of new candidates, each with their own improvements in dielectric characteristics, moisture sensitivity, and thermal budget. The next decade should be an exciting time for research in these fascinating materials.

Now that we have explored some of the basic material properties and discussed their strategic importance in semiconductor processing, let us now focus on specific applications and how these materials integrate with the substrate to form a complete metallized structure. In the next two sections, applications of organic dielectrics are described with respect to multilevel interconnection technology. Section 4 concentrates on isolated process steps, while Sec. 5 considers specific process integration issues.

## 4.0 PROCESSING OF POLYMER FILMS

The performance advantages that organic dielectrics offer make them attractive in designing advanced semiconductor chips and packages. In order to take full advantage of these materials, a process must be designed which fully integrates the metallization steps with the polymer.

Some of the difficulties of this integration come about from the inherent nature of the polymeric materials when exposed to the harsh chemical environment and elevated temperatures of semiconductor multilevel metal (MLM) processes.

Specialized equipment is used to apply polymer films, cure them, and incorporate metal wires and interconnects within them. As we shall see, certain processes must be developed which are specific to organic dielectrics where they differ from conventional inorganic materials.

In all processes, the polymer must be applied in a uniform and controllable fashion, with good adhesion to the substrate. Proper curing is critical, followed by process steps to deal with the problem of water absorption. The next few sections concentrate on these unit process steps and related issues.

### 4.1 Substrate Preparation and Polyimide Coating

Commercial polyimides come in various forms including thick films which may be applied by roll-on applicators such as Riston.[33] In addition, films are applied by spin-on methods as well as spray techniques. In some cases the films may also be screen-printed onto substrates. Spin coating is most often used and is done in the same fashion and using the same equipment as photolithography materials. Spin-on coatings are the method of choice since they produce films with excellent defect densities. Substrates are held to a spinning chuck with the aid of a vacuum and the polymer is applied.

A wafer is spun in the range of 3500–5000 rpm for a period of time approaching 60 seconds to give a uniform coating. After the initial coating, the wafers are baked at a moderate temperature to drive out the bulk of the solvent. Most modern day spin-coating equipment is integrated with spin and bake stations in the same enclosed environment. The tools allow for coating of adhesion promoters and multiple layers of polymers. This coating is then cured by a multistep anneal process.

In many cases, the polymer may not have good adhesion to the surface of the substrate unless an adhesion promoter is used prior to the polymer coating. These substances are often organosilanes such as A-1100 or other similar materials. Certain polymers, however, do not require these adhesion promoters since the polymer films may exhibit good wetting to the existing surface. Since the organic dielectric may be coated on both chip and packaging substrates as well as metals and other layers of dielectric, let us examine the topic of adhesion more closely.

## 4.2 Polyimide Adhesion

Adhesion of the polyimide films to the underlying substrate is of paramount importance. Since the polyimide dielectrics are generally applied to a metal surface underlayer, much work has been done on the adhesion of polyimides to metals. The adhesion of polyimide to copper-chromium systems has been studied as a function of surface pretreatment.[44] It was suggested that for a series of PMDA-ODA systems, that exposure of the substrate to low energy sputtering with Ar or $O_2$ ions improves adhesion, while for BPDA-PDA systems, $O_2$ sputtering is more effective than Ar. In general, a surface pretreatment is practiced when coating most polymers, either by physical surface modification or by the application of an adhesion promoter. In some cases, another polymer film can be used as a seed layer, providing the hydrophobic surface generally preferred by these films. Much work on polyimide surface modification has been performed by Shaw and Lee.[45] Some companies advertise organic polymers that themselves provide good adhesion to many surfaces so efficiently that no adhesion treatment is necessary.[35][46]

Adhesion to ceramic surfaces has been studied by Buchwalter.[47] In general, adhesion promoters of the organosilane type can be used on ceramic substrates or on silicon wafers[48] with good results, while on metal surfaces the situation is more complex. Since the adhesion of the polymer is extremely surface specific, it is necessary to adjust the adhesion process to those exact materials.

Adhesion in general is usually measured with a peel test. The film is pulled away from the substrate, and the force that is applied is measured by a peel strength apparatus. The force is generally measured in g/mm. This provides a relative measurement to compare various materials. No standard test for an absolute adhesion measurement has been developed. A discussion of the use of the peel test for reliability testing appears in Sec. 6. A schematic of a peel strength apparatus is shown below in Fig. 16.[14] A force transducer is fixed on a sliding stage which is connected to the test sample by a long rod. In this particular apparatus, the test sample consists of a strip of wafer of known width attached by two-sided tape to a glass slide. The wafer is then broken off leaving the film intact. The film is pulled at a consistent angle at a constant rate. This particular setup was enclosed in an environment of dry nitrogen. Several variations on this setup exist which perform the same basic functions.

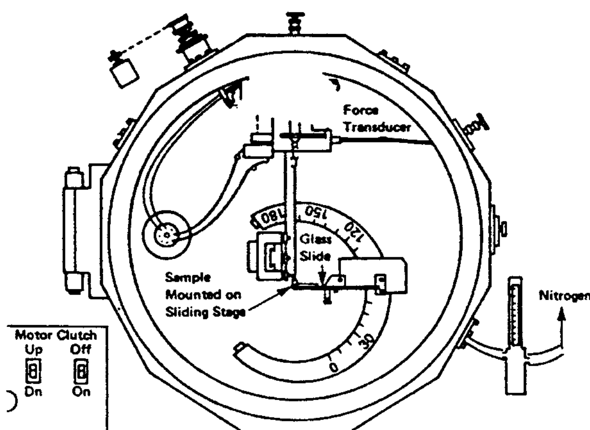



**Figure 16.** Schematic of a peel force test apparatus. In this apparatus, the polyimide film is peeled away from the substrate. *(After Rothman.[14] Reprinted with permission.)*

Many investigators have measured polymer adhesion on top of metal and ceramic substrates. Inversely, if polyimide is applied first and then subsequently coated with a metal film such as Cr, the polymer should first be rf-sputtered to improve the adhesion.[49] This is thought to improve the chemical bonding between the metal and the polymer. Additionally, the adhesion of the Cr-polyimide interface is significantly degraded by exposure to high temperature and humidity environments. It is suggested that the degradation results from hydrolysis of the polyimide or the metal-oxygen bond. This conclusion is further supported by Seshan,[50] who found that the isotope $O^{18}$ was trapped at the polymer-metal interface after allowing diffusion of water through the film. This buildup of tracer material was in direct correlation to the loss of adhesion at that interface.

Finally, the adhesion can be affected by the bake cycle or “curing” of the dielectric material. Let us examine this more closely.

## 4.3 Curing of Polyimides

After the application of organic dielectrics, the films are baked at high temperatures in a process known as curing. The curing of films is

important in order to impart the necessary properties of the organic dielectric. The cure cycle is generally done in several steps of increasing temperature, which drives out solvent and provides full imidization. The optimum cure conditions have been found experimentally and also have been modeled.[51] Commercial films of PIQ L100, for example, were modeled to find the optimum conditions for internal stress, imidization, and molecular orientation.

The type and duration of curing of polyimide films after spin coating is critical to the final film characteristics. The polyamic acids and the polymer backbones must be cured at a high enough temperature to affect cross-linking without decomposing them. The cure cycle also affects planarity. If the cure is done in a vacuum at a low enough temperature, a planarizing effect is achieved.[52] Alternately, the films may be cured in an inert ambient using carefully controlled furnaces. Curing is generally done over a wide range of temperatures with the final bake approaching the $T_g$ for the film. In many cases for polyimides, this final cure temperature is about 400°C. The curing is generally performed in a conventional furnace tube with a dry nitrogen ambient or in an integrated photolithography coating tool. Tight control on temperature, generally on the order of ±1°C, is important for reproducible film characteristics.

The length of time is also very important. The cure cycle dictates the amount of imidization which occurs and therefore the final film characteristics. Figure 17 demonstrates this for three different film thicknesses and two temperatures. As shown in the figure, the cure cycle can be extended such that, after a certain time, a constant degree of imidization is achieved where the data converges. This time can be adjusted for each polymer to ensure that a nearly complete imidization occurs. It is important to design the cure cycle toward the right of this curve where reproducible films can be realized.

## 4.4 Diffusion of Water

Diffusion coefficients for water in some polyimides have been measured by Chang at Motorola.[53] Diffusion of water through polyimide is fairly rapid, resulting in problems such as corrosion of metal surfaces as well as adhesion loss. The water content in the film also strongly affects the dielectric constant. The variation of the low frequency dielectric constant is directly proportional to the absorbed moisture.[54] These three negative affects of humidity make it imperative that the polyimide process

takes place in a well controlled environment and that the package be hermetically sealed after the chip or package is complete. A graph of the effect of relative humidity vs dielectric constant was shown earlier in Fig. 12. Moisture absorption can be a long term reliability issue as will be discussed in a later section. Catastrophic immediate damage will occur if polyimide multilayer systems with absorbed water are rapidly heated during processing.

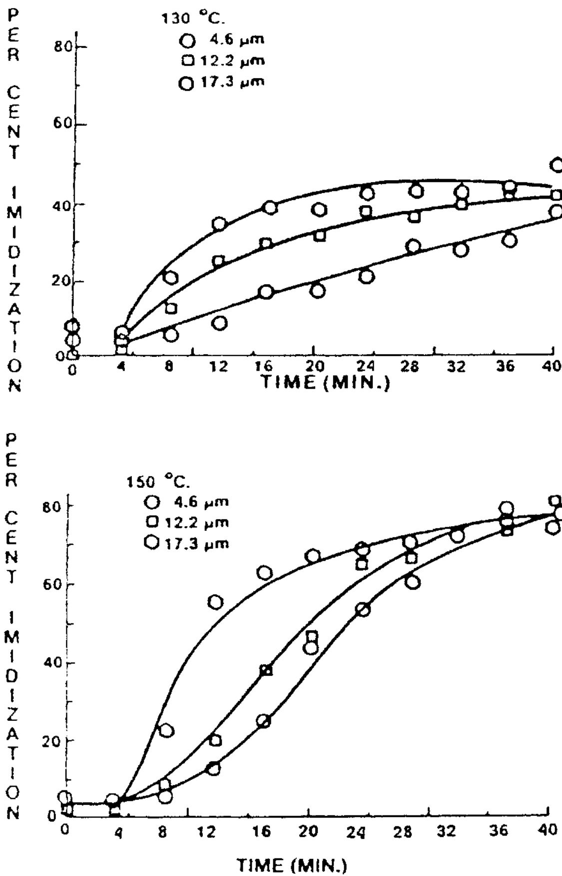



**Figure 17.** Shows the percent of imidization vs time for cure at 130 and 150°C.

## 4.5 Summary

We have examined some of the unit process steps and concerns that are part of using polymers to build multilevel metal structures. It will become apparent that incorporating these processes into a complete integrated structure is considerably more complicated and requires addressing interactions between the various layers of materials as the structure is vertically integrated.

In Sec. 5, some of these steps of process integration will be examined in more detail and examples of organic dielectrics in multilevel metal semiconductor structures will be described.

# 5.0 PROCESS INTEGRATION WITH ORGANIC DIELECTRICS

There are several possible ways to build a multilevel metal interconnect structure.[15] In one case, the metal lines are first fabricated and the organic dielectric is then applied. In an alternate procedure, a dielectric is deposited and patterned and the metal is deposited into the grooves etched in the dielectric. The process will clearly vary based on the individual substrate, thermal budget, and organic material. Therefore, the individual application will drive the thermal budget and the process limitations. Thus far, we have described generic techniques to build a structure with organic dielectrics. Assuming the first layer to be an $SiO_2$ based passivation layer, the first layer of organic material is deposited. If only a single layer is to be used, the processing would become simplified. Repeating this process to build multiple layers involves some additional considerations.

Numerous other details will affect the issues encountered during integration. In some applications, an inorganic RIE etch stop or passivation layers may be placed between organic dielectric layers. These thin films have little effect on the electrical performance but may ease the critical process integration steps. On the negative side, these thin inorganic etch stop layers are subject to cracking or delamination at later levels. The type of metallization will also drive the type of integration process that is used. For tungsten plugs, the polyimide vias may first be coated with a liner to provide a nucleation site for the tungsten deposition as well as to buffer the polymer from the compressive stress that is generally associated with metal deposition.

Let us examine some of the procedures involved in the fabrication process.

## 5.1 Processes for Forming MLM Structures

A cross-section of a multilevel metal structure that could be found as part of the wiring scheme on a semiconductor substrate is shown schematically in Fig. 18. It consists of several repeating alternating layers of metal and dielectric stacked upon one another to produce the final structure. In general, the layers closest to the semiconductor substrate contain the smallest wires with the upper layers used to distribute the input-output lines and provide power to various parts of the chip. Let us examine Fig. 18 starting at the layer labeled Metal 1 (M1).

This wiring level may contain many centimeters of metal, connecting contacts on a nonplanar surface which is generally built upon an inorganic dielectric, usually $SiO_2$.

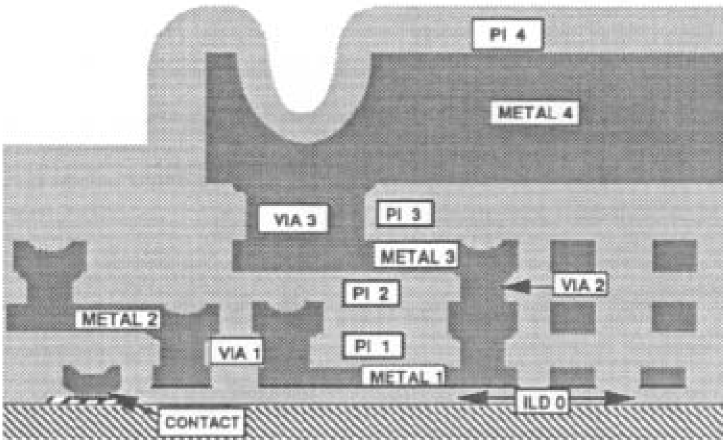



**Figure 18.** Shows the cross-section of a multilayer metal to polyimide structure. Notice that the ILD 0 is oxide.

This dielectric should act as a getter of impurities and also be noncorrosive to the metal contacts below. There is also a concern about metal ion contamination sometimes present in organic materials (e.g., Na, K, Ni, Fe) which could poison the semiconductor junctions if allowed to come in contact with the silicon. This is especially true of today's polysilicon

electronic devices, where metals diffuse quickly through the polysilicon grain boundaries into the junctions. For these reasons, polyimides have not been used as the primary insulator at the semiconductor surface. Generally, an oxide layer is used as the first dielectric layer, usually as a thin film. The oxide layer may be pure or doped with gettering ions such as phosphorus.

Upon this surface, the next levels of metal are fabricated and are isolated from one another and the substrate by organic dielectrics. A simple schematic of the process steps required to build a multilevel metal interconnect technology using organic dielectrics is shown in Fig. 19. It can be seen that the process consists of repeating basic building blocks of insulator and metal.

General process design is built around specific steps. Each step has specific effects which must be considered. The schematic that follows gives a generic process flow for a particular type of process known as lift-off.

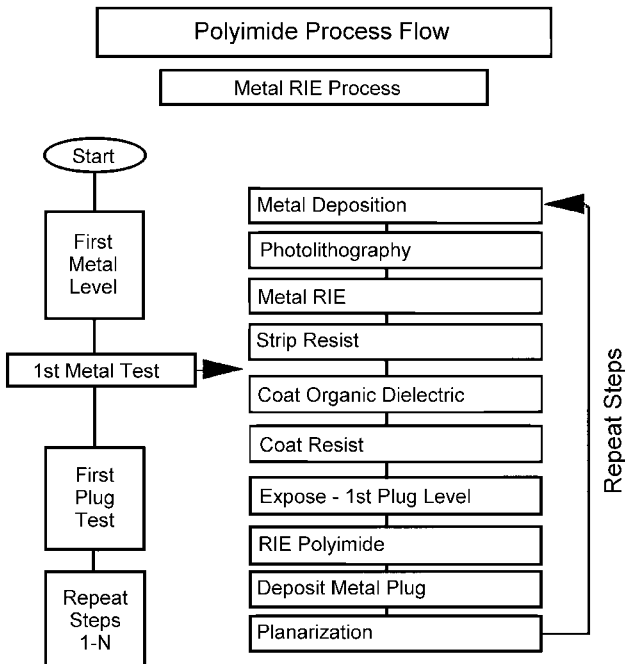
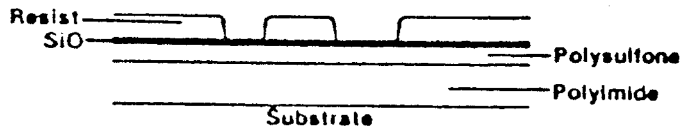



**Figure 19.** A process flow for a typical metal RIE process.

| | Steps which repeat | Comments |
|---|---|---|
| 1. | Apply adhesion layer | Preclean of surface required |
| 2. | Spin-on polyimide | May be multicoat film procedure |
| 3. | Multistep cure (100°C/200°C/300°C/400°C) | Multistep; optimize for specific process. Ambient effects, $N_2$ during final cure. Also stress. |
| 4. | Apply hardmask layer ($SiO_2$) | |
| 5. | Apply photoresist (bake) | |
| 6. | Expose | |
| 7. | RIE hardmask | Anisotropic RIE |
| 8. | RIE polyimide | Anisotropic RIE with undercut |
| 9. | Metal Deposition | Directional |
| 10. | Lift-off | |

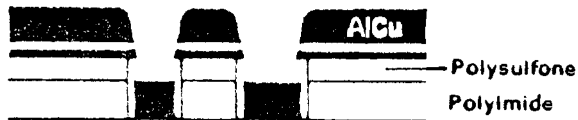
Initially, pillars of metal are formed over predetermined areas in the M1 metal line. The pillar is formed in a contact through the first polyimide layer. As mentioned earlier, this may be performed by the opening of a via hole in the dielectric using conventional photolithographic techniques. This is usually accomplished by the curing of a blanket polyimide layer over the substrate followed by an inorganic film such as $SiO_2$ which is used as a RIE hardmask. The substrate is then coated with conventional photoresist, and the pattern is transferred into the hardmask layer using plasma etching in a gas such as $CF_4$. The gas is then changed to oxygen to etch the polyimide layer below. Control of the RIE conditions can cause anisotropic etching of the film or intentional undercuts of the hardmask layer if desired. In general, an undercut profile is desired when a lift-off metal is evaporated in a directional manner. The excess metal is then lifted off by a release layer to form a pillar of metal which is brought to the surface of the organic dielectric for contact by Metal 2 (M2). The lift-off method has been used in recent years due to its planarity and relative ease of process. A schematic of the lift-off process is shown in Fig. 20. The process has been used with inorganic and organic films and for both semiconductor and packaging applications.

After the pillars have been created, the next level of metal is deposited and defined. The conducting metal lines can be defined by methods such as RIE or wet chemical etching. The metal layers will conformally cover the organic underlayer and replicate the topography already present in the structure. A structure that is as planar as possible is desirable for reliable metallization structures and lithography.




Apply Polyimide by Spin Coating and Cure
Apply Polysulfone by Spin Coating and Cure
Evaporate 1000 Å SiO
Define Pattern in Resist

Reactive Ion Etch
In $CF_4$ to Etch SiO
In $O_2$ to Etch Organics




Evaporate AlCu

Lift-off in NMP

**Figure 20.** Process description for forming the first level of metal via a lift-off process.[15] (*Reprinted with permission.*)

The process of patterning, etching, and deposition becomes more restricted as the number of levels increases. The metal lines sandwiched between multiple organic layers are subject to the stress and deformations imposed by the polymer material's physical characteristics.

The lift-off process is extendable down to submicron dimensions but becomes more difficult since the small lines are subject to falling over. For larger patterns, isotropic metal etching has been the method of choice due to simplicity. VLSI technologies, however, require anisotropic metal RIE or other well controlled selective deposition techniques.

## 5.2 Patterning of Organic Dielectrics

The polymer etching is generally performed using oxygen RIE in an anisotropic plasma etcher. At the first organic insulator level, the oxygen RIE provides a selective etch to the MI level, since both zero level dielectric and the metal are not etched by oxygen RIE. At subsequent levels, however, the etch becomes more complicated by the fact that vias which are not fully covering metal lines below may be overetched down below the metal line. The subsequent filling of these vias may cause shorting or reliability problems at later levels. This has led some investigators to incorporate thin "etch stop" layers in between the organic dielectrics. These thin films have little effect on electrical performance but may ease the critical process integration steps. Difficulties in these etch stop layers arise from the tendency for the organic layers to outgas during subsequent processing. This leads to cracked films or stresses affecting the planarity of the structure. The adhesion of the organic layers to the thin dielectric etch stop layers may also be subject to failure later on in processing.

More recently, an alternative approach for building multilevel metallurgy has been described, making use of photosensitive polyimides. The general basic structure is formed but uses a different process sequence. One of the attractive features of this system is the relative simplicity of processing steps. Figure 21 shows a comparison of the number of steps required to form a single layer of metal isolated by organic dielectrics. A description of some of the options employing these photosensitive materials will not be discussed here but has been described by others.[43] The photosensitive materials basically combine the photolithography and etching step into one process. Commercial photosensitive materials available today, however, do have their limitations. The photosensitive organic

films are cured at much lower temperatures to prevent damage to the photoactive component (PAC). They therefore contain more solvent and are at about twice their completely cured thickness. This causes aspect ratio problems and dimensional instability. If the developed image undergoes shrinkage over time, this will lead to difficulties in controlling critical dimensions required for VLSI. For this reason, the materials have thus far been used primarily in packaging and relaxed ground rule applications.[54]

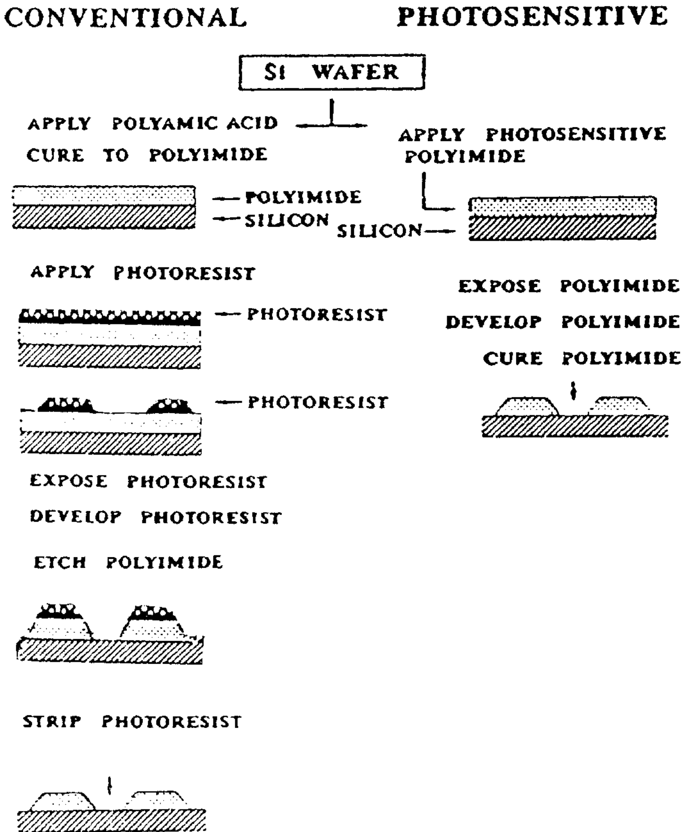



**Figure 21.** A comparison of the process steps using conventional and photosensitive polyimides.

## 5.3 Planarization

For several reasons, it is desirable that the multilevel metal insulator layers be as planar as possible. First, the film depositions of metal and insulator are most uniform when deposited as a planar thin film, as almost all deposition systems have a degree of non-conformality. This results in films on vertical surfaces being of different thicknesses than films on horizontal surfaces. In the removal of metal and insulator films, planarity is even more critical. Since the removal of films is usually performed with anisotropic plasma etching, a nonplanar surface results in rails or "stringers" around the highest objects which may result in short circuits.

More importantly, the step coverage of metals as they go over topography may cause reliability problems which may not show up as a time-zero fail. Electromigration fails could be expected to form in these regions of incomplete metal thickness.

Finally, today's lithography tooling is designed for small geometries with large numerical apertures. A by-product of this engineering is that the depth of focus for these tools becomes very small, in many cases less than 1000 nm. If the non-planarity of the multilevel metal stack exceeds this topography, the lines on the next lithography level may not print uniformly across the chip.

One of the advantages of spin-on layers is that they tend to have a planarizing effect when coated over topography. They also have a very low defect density as compared with CVD films. While planarization of the wafer surface appears to be uniform at the local level, the surface is never fully planar after a single thin coat of organic dielectric. It has been shown that coating several thin layers produces a more planar coating than one coat of equal thickness.[15] It is therefore important to adjust the coating thickness and cure to coincide with the particular structure being planarized. A curve showing the degree of planarity as a function of numbers of coatings is shown in Fig. 22.

The planarity of the structure is not only affected by the number of coatings but also by the dimensions of the structures themselves. In general, when the linewidth and the spaces between the lines are kept small, the planarization will be more complete as opposed to larger lines and spaces. Furthermore, a particular substrate may have an isolated line surrounded by organic dielectric in one area and many lines close together in another area. This can lead to localized planarization of the isolated line only. In this case, it is important to concentrate on the areas which are

most difficult to planarize on each particular chip layout. Figure 23 shows the effect of planarization as a function of linewidth and spaces for a particular polyimide film. In most cases, even multiple coats may not afford total planarized structures.

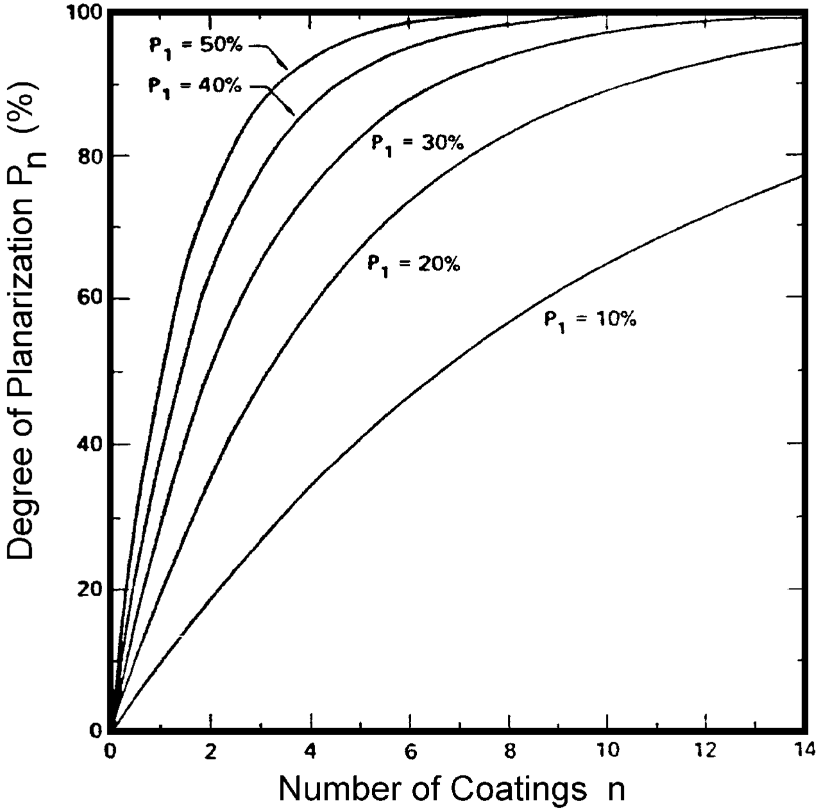



**Figure 22.** Diagram showing the degree of planarization vs. the number of coatings; P is the packing factor. As the structure becomes more dense, a larger number of coatings are required for planarization.

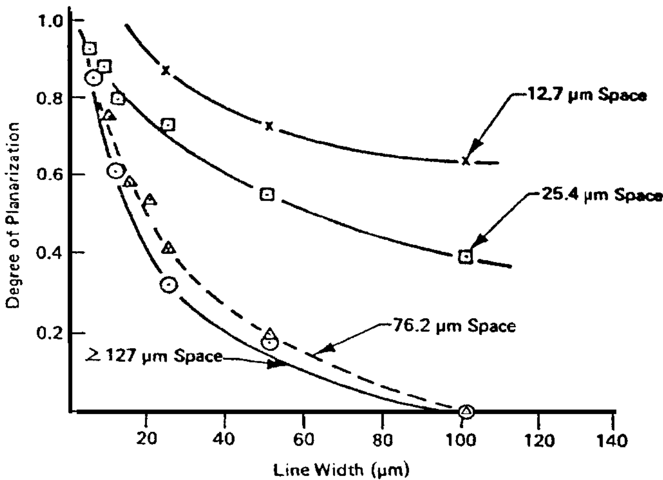



**Figure 23.** The degree of planarization vs. linewidth and line spaces.

Other factors affecting planarization relate to film characteristics, solvents, application techniques, and the film curing cycles. These need to be optimized for the individual user applications.

Thus, while local planarization is often achieved, complete global planarization is not achieved with polyimide coating. Several approaches have been used to address this. In the first approach, a photoresist is coated over the polyimide and exposed in the opposite density to the metal definition mask. The polyimide can then be removed over the metal lines by RIE etching, leaving a polyimide plug between the metal lines. This approach has been studied extensively by Chang, et al.[55] Another novel approach has been studied by Chakravorty,[56] who reports that uniform shrinkage of two polyimide layers leads to a planar structure.

As an alternate approach for producing structures with increased planarity, many engineers are investigating chemical-mechanical polishing as a method of planarization.[1][57] This method produces planar surfaces; however, organic materials may crack or become distorted under the stresses of the polishing process. The polishing process for organic dielectrics is much more difficult due to the mechanical properties of the cured films. Some of the effects caused by metal or polishing stresses are wrinkling, cracking, adhesion loss between layers, and blistering.

## 5.4 Thermal Budget Considerations

The thermal budget for multilevel metallization processes has always been limited, since metals such as aluminum have relatively low melting points. In the case of organic dielectrics, processes are even more constrained since many of these materials break down at temperatures much above 400°C.

Furthermore, when several metals are used in alternating layers, metal intermixing can become a problem. Since electromigration and adhesion concerns can be improved by using multiple layers of metallurgy to form the primary conducting wire, it is important to choose the right combinations of materials and thicknesses. Several multilayered metallurgy schemes have been proposed and summarized by Mattox.[58] Some examples of thin film metallurgy are shown in Fig. 24.

The metals are arranged in a 3-layer fashion, as shown in Fig. 25, with the adhesion layer being the Ti or Cr. Problems related to thermal budget begin to compound as the structure is built. The first layer of metal is annealed both after deposition and after subsequent repetitions of polyimide curing and metal anneals. This further influences metal mixing. To illustrate this principle, a temperature-time curve is shown in Fig. 26. It can be seen that the thermal budget issues define the material and process constraints for subsequent metal levels.

An Example of a Thin Film Multilayer Structure

| 2-layer | 3-layer | 4-layer |
|---|---|---|
| Au/Ti | Au/Pd/Ti | Au/Rh/Pt/Ti |
| Au/Cr | Au/Pt/Ti | Au/Ni/Cu/Ti |
| Au/Mo | Pd/Cu/Ti | etc. |
| Au/Nb | Au/W/Ti<br>Au/Mo/Ti | |

**Figure 24.** Table showing examples of various metallurgy composites used in multilevel metal wiring.

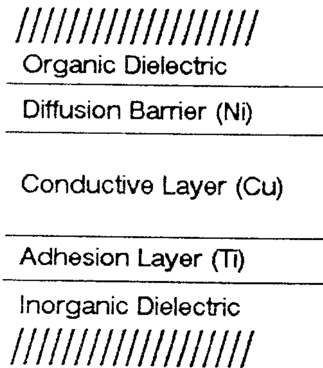



**Figure 25.** Schematic of the arrangement of the adhesion conduction and barrier layers commonly used in metallization schemes shown in Fig. 24.[58] (*Reprinted with permission.*)

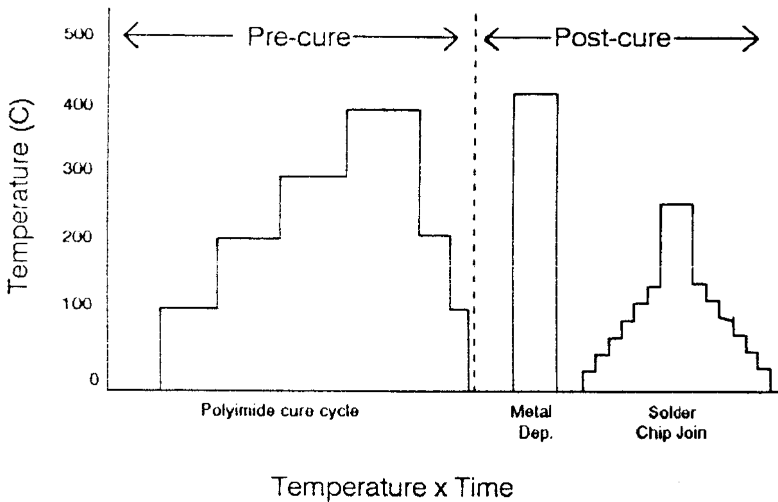



**Figure 26.** Temperature × time diagram for the thermal processes that the last layer of polyimide has to withstand.

## 5.5 Examples of Organic Dielectrics in Semiconductor Technologies

While a great deal of studies of organic dielectrics have occurred over the years, the use of these materials in actual products has been limited. One of the earliest uses of a polyimide passivated metallurgy in semiconductor memory products was the SAMOS process, developed by IBM in the 1978 time frame.[11] Here a silicon dioxide and polyimide dual dielectric was employed at the first level of metal to reduce defect densities and also help improve reliability. The polyimide also provided improved mechanical properties. After holes were etched down to the first level metal, a second layer of metal was deposited and patterned. A second polyimide layer was then deposited across the wafer to fully passivate the structure. In this case, the film was somewhat thicker than that used at the M1 level. The polyimide was then removed over the M2 pads and in between chips. The final contact metallurgy was then evaporated through a mask to form the chips' lead-tin pad connections. In the case of the SAMOS process a series of five metals was used. As discussed earlier, a thin chromium layer serves as a seal because of its excellent adhesion to both aluminum and polyimide. The chromium also provides good corrosion resistance from the solder connections. A copper conductor was then used as the primary conductor along with a gold passivation layer. The lead-tin pads were then deposited. The resulting structure is illustrated schematically in Fig. 2, Sec. 2.

It is interesting to note that a total of five metal evaporations were possible within the boundaries of the polyimide heat constraints. The thermal stability of the polyimide allowed the implementation of this advanced metallurgy into an LSI memory product. This technology was used to create a highly successful family of 18–64 K bit memory chips.

In 1987, IBM also reported the use of polyimide dielectrics in a triple layer bipolar chip.[59] Again, the resultant product was found to have high reliability and planar surfaces for metallization. The process is also low cost since it does not require CVD tools for the dielectric deposition.

Some more modern examples of polyimide integration in multilevel interconnection structures have been demonstrated by Chang.[34] This integrated structure demonstrates the use of organic dielectrics to fabricate a full four levels of metal in a VLSI product. The structure is shown in Fig. 27.

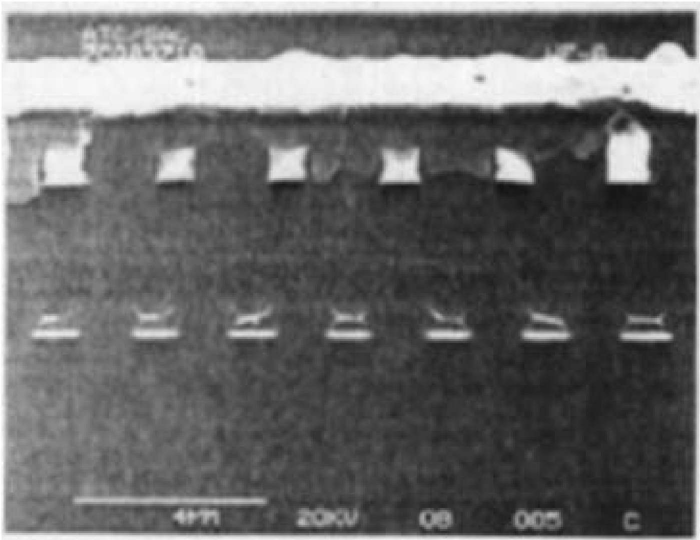



**Figure 27.** Cross section SEM showing four layers of metal and polyimide. (*Figure provided by Li Chang of Motorola, unpublished.*)

Small and Pearson[1] also describe the use of polyimides for advanced logic products to reduce wiring delay, as was shown schematically in Fig. 1 of Sec. 1.0 of this chapter. The general flavor suggests that organic dielectrics will be studied by all companies that have an eye on the future of semiconductor manufacturing. The examples above already have demonstrated that the technology is mature enough to move from the laboratory into the manufacturing line.

Polyimides have also successfully been integrated into multichip packages by Honeywell.[60] These packages offer the same advantages for signal propagation as semiconductor metallization structures.

Finally, more researchers are describing techniques and applications for organic dielectrics for microelectronics. The growing interest suggests that the advantages offered by these films is finally beginning to be recognized.

## 5.6 Summary

During this discussion methods of fabricating multilevel metal structures have been simplified in order to bring up the various parts of building such structures. In reality, the cross-section shown in Fig. 18 is highly idealized, showing no detail of the metal or insulator stack. In general, the metal layers are actually composites of alloys, adhesion layers, and passivation layers. The insulator stack may contain other dielectrics such as silicon oxides or nitrides for plasma etch stops or passivation.

The process design to build a multilevel metal-polyimide structure involves the details of metal-metal, metal to polyimide, and polyimide-oxide interactions and their environment. Features such as pillars, plugs, contacts, and lines can be put down by evaporation or sputtering and patterned with wet or dry (plasma) etching. We have seen that there is no unique set of steps to build a multilevel metal structure. The need for adhesion layers may complicate the integration by requiring additional depositions and process steps. Coating these films over topography also presents a challenge by requiring either multiple coatings, specific cure conditions, or planarization techniques. While creative solutions for most of these integration problems have been demonstrated, their complexity may have up to now limited the use of organic dielectrics. Several examples of organic dielectrics in device structures have now been reported by a increasing number of companies and universities. It is expected that as more of these products become commercialized, the use of organic dielectrics in future products will substantially increase.

As we conclude this section on process integration, it is fitting that we now discuss the reliability of these films in actual multilevel metal applications. Section 6 will discuss these issues.

# 6.0 RELIABILITY

The reliability of metal to polyimide multilayers falls into two broad categories: "during-build" design or reliability issues and "post-build" or "burn-in" reliability issues. This section discusses these aspects separately, although the basic mechanisms underlying the degradation of reliability are often the same.

"During-build" reliability testing and modeling is, and should be, concerned primarily with adhesion, adhesion monitoring, and the degradation of adhesion during the manufacturing cycle. Attention should be given to

stress generation and propagation. Stress modeling should be used for optimizing shapes and aspect ratios of posts, pillars, and lines. Special attention should be given to the role of moisture. Both moisture and thermal aging can have important effects upon the mechanical properties of the polymer. Trapped charge and dielectric breakdown related to processing needs to be studied.

"Burn-in" or long term reliability testing is concerned with long term temperature-humidity cycles, conformation to mil-specs (military specifications), or ASTM (American Society for Testing Materials) specifications for commercial products. In special applications specific ICs (ASICs), the customers may impose more stringent temperature and leakage requirements. Very often it is the electromigration of metal that limits the line lifetime; therefore, the electromigration testing of thin, narrow metal lines should be and is an area of intense study and concern. A review of the use of polyimides in the Japanese semiconductor industry is given by Makino.[19] It is often difficult to find extensive detailed reports of such testing as the data is often considered proprietary.

Developing new testing methods, understanding the significance of pull and peel testing, electrical characterization of electrical nets with narrow width and pitch at high frequency, and the development of new test methods can all be considered as being within the broad scope of general reliability testing and modeling. This discussion will be limited to some of the key issues, with Secs. 6.1 through 6.4 addressing "during-build" questions and Sec. 6.5 dealing with long term reliability.

## 6.1 Adhesion and Its Connection to Diffusion of Metal into Polyimide: The Interphase and Interface Stress

Pull and peel testing and wire bond pull testing have been used extensively to study adhesion degradation by Rothman[14] and, despite the micromechanical complexities, remain as the main vehicles to quantitatively study adhesion. Generally, the adhesion between metal and polymer degrades with temperature cycles during build. Cycling Ti-Cu-Ni-Au multilayers to 360°C in "factory nitrogen," with Ti as the adhesion layer, has been shown to degrade adhesion. Oxidizing ambients (like "factory nitrogen" which contains traces of oxygen) cause more degradation than reducing (forming gas) ambients.[61] There have also been extensive studies of modeling adhesion and the micromechanics of the peel test. For details, see Kim, et al.,[49] and related papers.

Much of early reliability deals with whether the metal polyimide stack will survive the heat cycles of the manufacturing process. The main topics of concern are:

1. Adhesion of the metal to the polyimide and the different layers of polyimide to each other.
2. Adhesion degradation during manufacture.
3. Role of ambient gases while processing.
4. Thermal cycles during manufacture.
5. Stress effects that occur; for example the shrinkage of the conductor metal after evaporation.

Adhesion depends critically on the state of the metal to polyimide interphase and on the amount of diffusion of metals into the polyimide. Therefore, an understanding of the diffusion of metals into polyimide forms a basis for understanding adhesion. Much work at IBM has concentrated on the understanding of the diffusion mechanism, and this is described next.

Diffusion of metals into interlayer dielectrics give rise to several related reliability concerns. These concerns are the same for both silicon dioxide and for organics. These concerns are:

1. Metal penetration from lines and change of dielectric constant.
2. Metal (Cu) diffusion into the device silicon.
3. Shorting of metal lines and pillars.
4. Adhesion degradation.
5. Thermal effects enhancing above mechanisms.

Cu and Al have been shown to diffuse into polyimide, and Gupta, Faupel, Ho, and co-workers have argued that the transition metals Cr and Ti may, in a complexed state, diffuse much more slowly in polyimide. However, since Cu diffuses readily into PI, structures which clad the Cu and protect the sidewalls have to be devised. Such structures have been described in the literature. For example, Cu interconnections with Cr-Cu-Cr at 0.8 and 0.5 μm line widths, defined using lift-off with Si templates and a trilayer resist stack, have been described by Rogers, et al.[62] Reliability requires complete cladding of Cu. Double level metal structures (0.8 μm) with the sidewalls protected by PECVD SiON deposition over lift-off Cr-Cu-Cr have been constructed and were shown to pass

the reliability tests. This paper shows that when the proper structure is achieved, the structures are reliable, passing the standard tests.

In order to study the penetration of metals into polyimides, tracers have been used and diffusion coefficients have been calculated. Some of the published results are shown in Fig. 28. The basic technique is to apply a coat of radioactive copper, microsection the sample using ion beams, and mass analyze the beam for the radioactive copper. This process produces plots of copper penetration as a function of time and temperature. This is then used to determine the diffusion constant.[63]

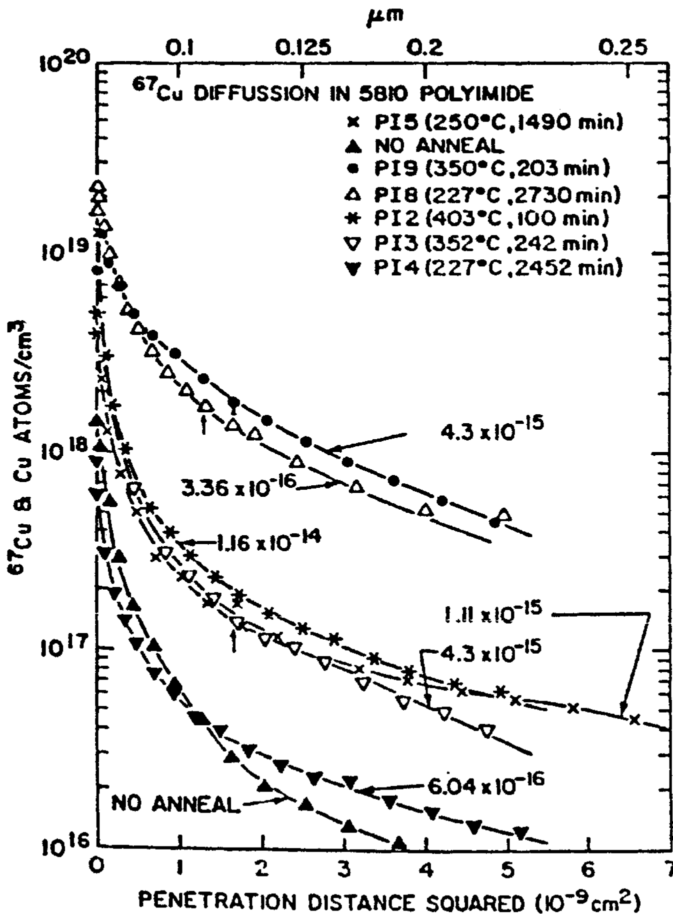



**Figure 28.** Shows the diffusion of isotopic copper into 5810 polyimide. *(After Gupta.[63] Reprinted with permission.)*

The diffusion of copper in polyimide and in inorganic dielectrics has been compared by Gupta (see Fig. 29)[63] and modeled by Faupel and co-workers.[64] It was found that Cu diffusion in polyimides is faster at the same temperature and that the diffusion of Cu in SiN:H is the least, followed by 4% PSG. Copper diffusion in PMDA-ODA is 10 x as compared to BPDA-PDA. Copper solubility in polyimide is 10x compared to 4% PSG. Copper diffusion in PMDA-PDA and 4% PSG at 400°C is about 1 μm in 70 hours.

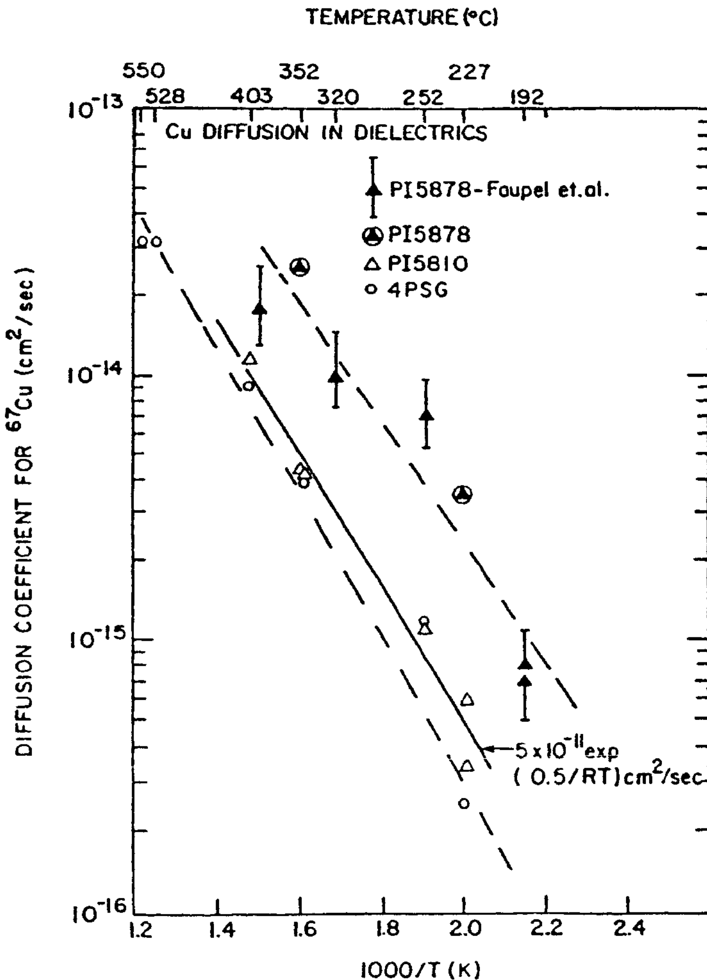



**Figure 29.** The diffusion of Cu into phosphosilicate glass (PSG) as compared with polyimide. *(After Gupta.[63] Reprinted with permission.)*

Monte Carlo calculations of the penetration process can be seen in Fig. 30.[64][65] These simulations provide corroborative evidence of the penetration discussed above. Notice especially the copper enriched layer below the metal. This layer plays an important part in adhesion.

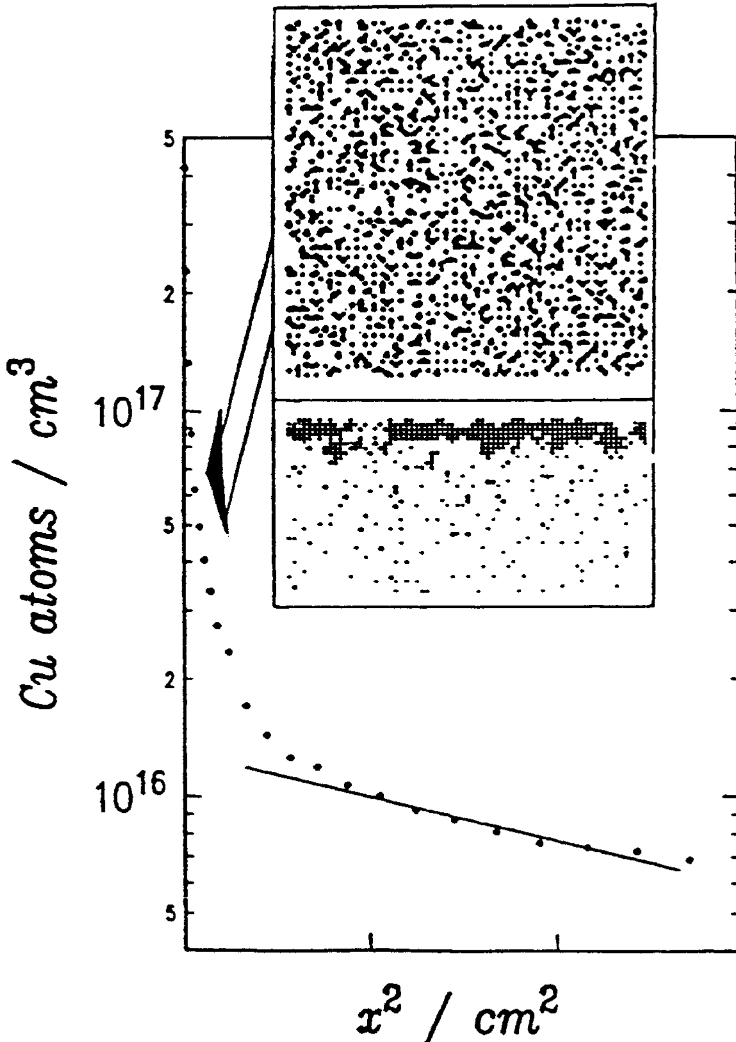



**Figure 30.** Monte Carlo simulation of copper diffusion into polyimide. *(After Silverman.[65] Reprinted with permission.)*

Das and Morris[66] have reported self-gettering behavior of ion-implanted Cu in polyimide. They attribute this to diffusant/diffusant interaction; this is further evidence in support of a cluster type mobility of Cu in polyimide. Silverman[65] has simulated metal atom cluster mobility in metal/polymer interfaces. This view of the diffused metal polyimide interface is also supported by Wool and Long,[67] and this point of view has been used as a basis for further modeling by Seshan and Lacombe.[50]

**The "Interphase" and Its Models.** The Cu diffusion experiments and the Monte Carlo simulations show that the penetration of metal into polyimide is an active, never ceasing process. This area just below the metal, we have chosen to call the "interphase," and a finite element rendering of it is shown in Fig. 31. It was modeled as having two mechanical "phases;"[61] it can change during the manufacturing process and during reliability test thermal cycling. This is the reason that we have chosen to call the layer between the metal and the polyimide a "transition" layer.[61]

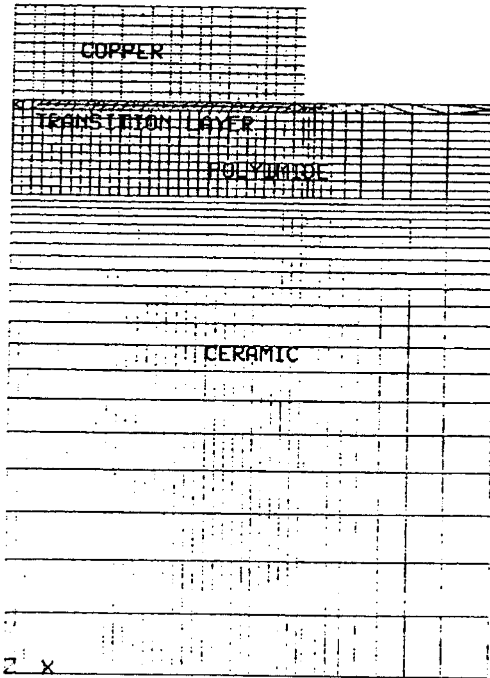



**Figure 31.** Shows a finite element model, based on Fig. 30, to calculate the local stress effects of the copper rich "transition" layer. *(After Seshan and Lacombe.[50] Reprinted with permission.)*

This interphase model can be used to understand changes in properties and help explain some testing results. This is particularly useful in understanding the effect of moisture, as discussed below.

**Modeling with the Metal-Polyimide "Interphase."** The results of finite element modeling of the interface, taking into account the transition layer are shown in Fig. 32. It is the thickness, the mechanical properties of the "transition" region and its change with time that dominates adhesion. An understanding of this transition layer will remain a major problem in the reliability arena. The more subtle problem is the change in the "local" dielectric properties and its impact on performance.

Figure 32 shows the stresses in the interphase region when the metal is deposited at temperature and cooled, and then the mismatch stresses are imposed. The resultant changes in normal and shear stresses were calculated.[50] The conclusion of that work was that at critical thicknesses, with sufficient loading of the metal particles, delamination can occur, as is observed in early reliability testing. This affect can be avoided by reducing the thermal cycles and avoiding an oxidizing ambient.

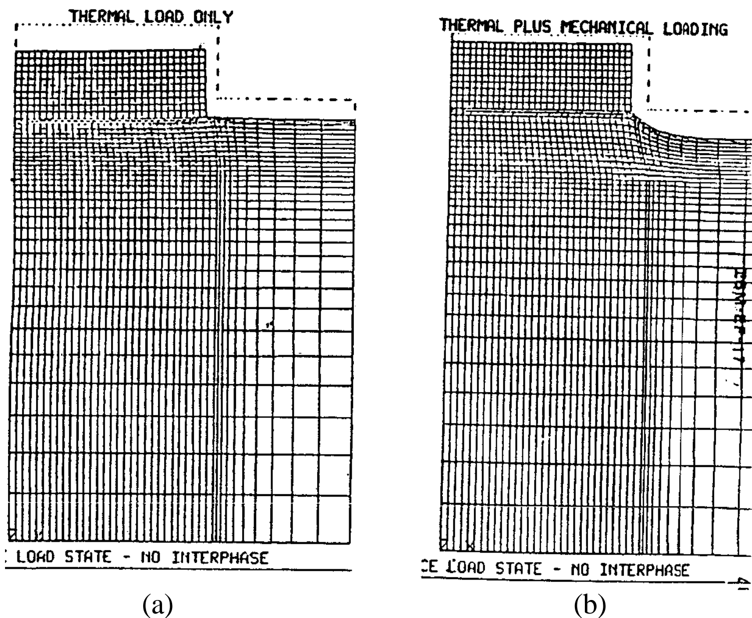



**Figure 32.** Shows the contraction calculated using the model in Fig. 31. *(a)* Shows the results, only of the contraction due to the cooling of the metal, and *(b)* shows the results of the differential contraction of the metal and the polyimide. *(After Seshan and Lacombe.*[50] *Reprinted with permission.)*

## 6.2 Effect of Moisture Ingress

Concepts from the "interphase" can be used to understand and model the adhesion when moisture is introduced. The effect of moisture ingress into polyimide/metal interfaces is an area of continuing concern. Adhesion tests of thin metal multilayer films to polyimide showed that both Cr and Ti, used as adhesion layers, degraded when exposed to an oxidizing ambient.[61] This degradation was attributed to the formation of $Cr_xO_y$ and $Ti_xO_y$, at the interface. It was shown that forming gas ($H_2$+$N_2$) was more benign than $N_2$ annealing, which is slightly oxidizing because "factory nitrogen" was found to be contaminated with oxygen. There also is a change in the failure mode.

Thus, two different failure modes were observed. When tested just after metal deposition, using peel testing, high strength (30–50 gm/mm) cohesive failures were observed. In this failure mode small pieces of the polyimide were torn out with the metal. When the interface was exposed to ambient, the adhesion strength dropped to 5–10 gm/mm, and low strength adhesive fails were seen. In this failure mode, a "new" low strength, "interphase" layer seemed to have formed. These failure modes are illustrated in Fig. 33.

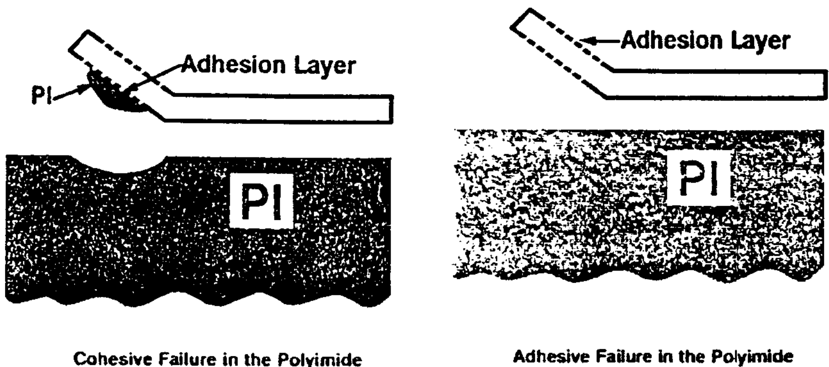
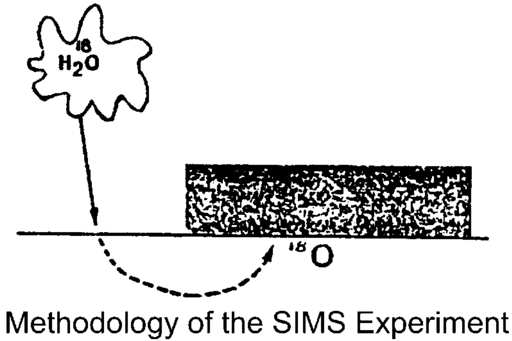
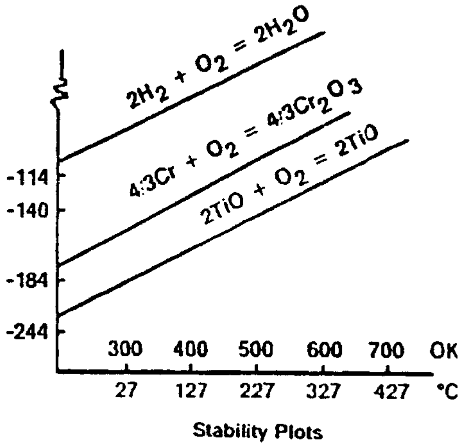



**Figure 33.** Shows the different failure modes observed when deposited metal is peeled off cured polyimide. Cohesive failure involves tearing out of the polyimide. Adhesive failure involves a "clean" separation between the metal and the polyimide, implying a "transition" layer as shown in Fig. 31.

A thermodynamic explanation was advanced, which depended on the penetration of moisture to the metal-polymer interface region. These hypotheses are supported by the data in Fig. 34. The polyimide-ingressed moisture would react with the metal clusters in the transition region. Ti would be more susceptible than Cr, because Ti has the added ability to dissolve hydrogen and expand and embrittle.[61] This seems to explain the observed experimental results that Ti adhesion layers failed faster than Cr layers. The mechanical modeling[61] also support this argument.




(a)




(b)

**Figure 34.** *(a)* Shows the methodology of the SIMS experiment where isotopic water containing $O^{18}$, was introduced into the metal/polyimide interface. SIMS showed an accumulation of $O^{18}$ near the interface. *(b)* Shows the stability plots relevant to Fig. 35; the interface adhesion layer, usually Ti or Cr, will be able to reduce the water and form oxides of Ti or Cr. *(From Seshan, et al..*[61] *Reprinted with permission.*)

The ingress of moisture into polyimides can be quantitatively measured. An optical technique to measure the refractive index of polyimide when exposed to water showed that, as humidity increased, the refractive index increased. This could be caused by swelling as a result of the incorporation of water, perhaps at a molecular level. The other argument is that there are micro-pores.[68] Using a laser technique, TM and TE modes were measured, these giving the refractive index for both parallel and perpendicular modes generated by coherent laser light. The micro-void model would cause the refractive index to increase. The swell model would cause the refractive index to decrease. Data suggested that both mechanisms are operative. When the amount of water is small, the swelling model applies; for larger amounts (over 1%), the void model appears to hold. This was considered important for the reliability of non-sealed low cost hybrid systems.[68]

## 6.3 Mechanical

Thermal aging, moisture ingress, and prolonged exposure to temperature and humidity cause the tensile strength to decrease, and the elongation to drop. The result is that films are prone to crack; these trends can be seen below. In the modeling work, data from Fig. 35 was found to be useful and is included here for the purpose of reference.[33]

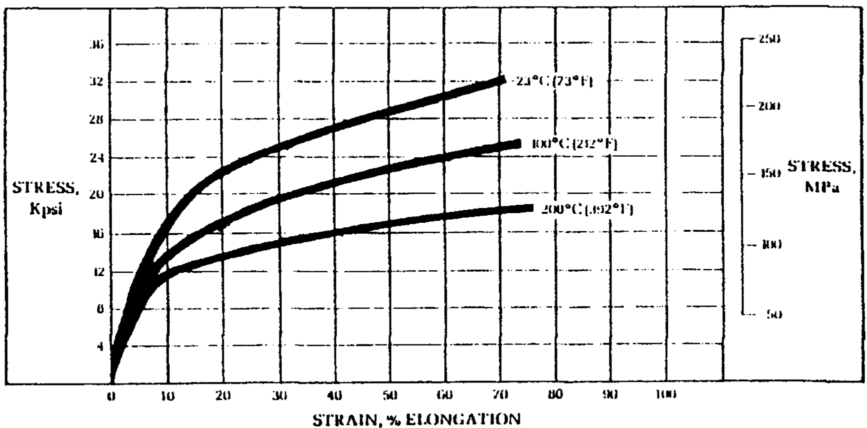



**Figure 35.** Shows the stress-strain curves for cured polyimide films.[33] (*Data from Dupont*).

In conjunction with a drop in strength, polyimides also creep; this is of concern when there are local stress raisers. Over time there is a possibility of dimensional changes; published data for polyimides are shown in Fig. 36.[33]

Homma[69] reports a deformation mechanism of polyimide insulated Al alloy lines, caused by shrinkage stresses of the resin on top of the chip. This caused the polyimide and the 1st level alloy line to deform, while the upper layers were unharmed. Reliability was improved by modeling, changing the adhesion, and optimizing the film thickness.

## 6.4 Electrical Properties

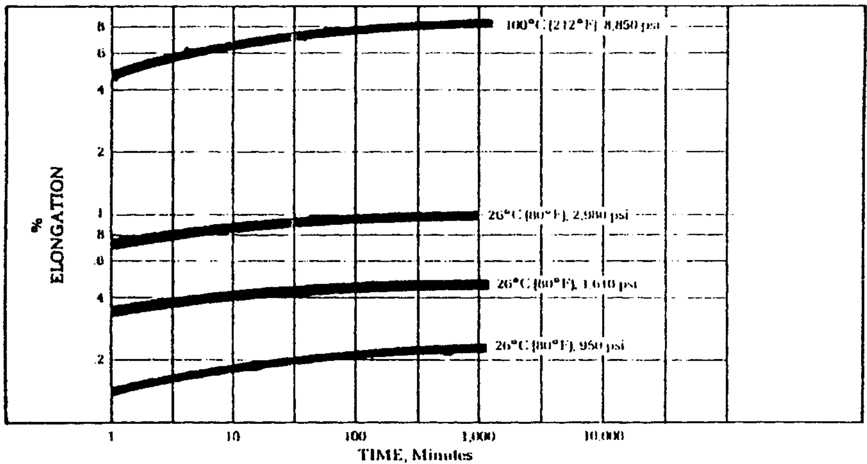



**Figure 36.** Tensile creep properties of cured polyimide films.[33] *(Reprinted with permission.)*

Many of the dielectric tests for oxides also apply to polyimides. Dielectric integrity tests for reliability include time zero dielectric breakdown (TZDB), time dependent dielectric breakdown (TDDB), and trapped charge measurements. Although the requirements on organic dielectrics are not as severe as on oxides, nevertheless questions about what values are to be used for extremely thin polyimide layers is becoming an issue.

The effect of temperature on ac dielectric strength, dielectric constant, dissipation factor, and volume resistance are shown in Figs. 37 and 38 from the properties compiled for Kapton by DuPont.[33] It must be remembered that both mechanical and electrical property changes occur.

Figure 39 shows some of the origins of dielectric integrity and reliability problems.

Some of the issues in dielectric integrity and reliability are shown in Table 4. These properties are measured by the usual CV/IV measurements used to test oxides. The breakdown of the dielectric and the effect of the trapped charge are important, depending on whether the application is in power or in performance.

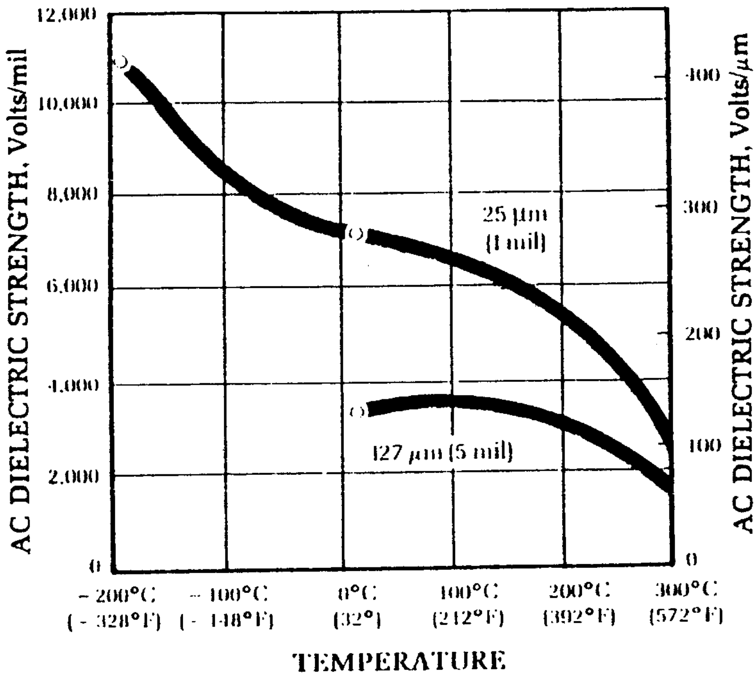



**Figure 37.** Shows the decrease of dielectric strength with temperature. The defects shown in Fig. 39 will enhance these effects.

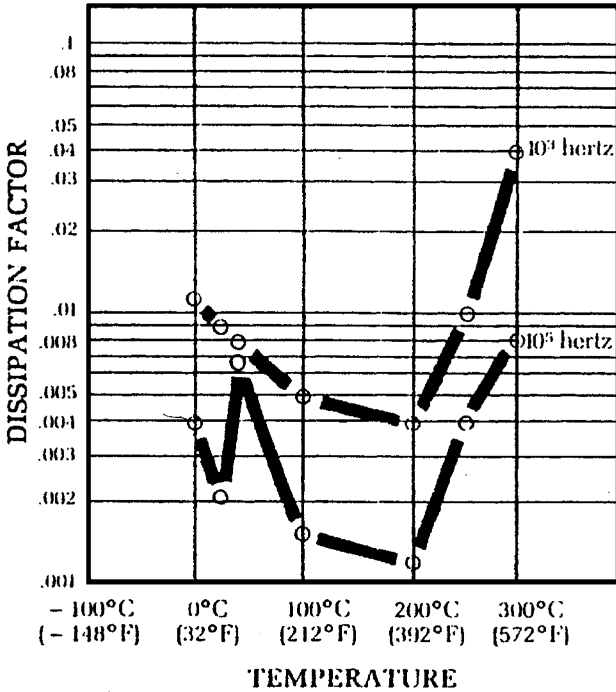



**Figure 38.** Shows the dissipation factor vs. temperature. Notice that the dissipation factor increases with temperature. This will adversely affect the performance of metal wiring in polyimide.

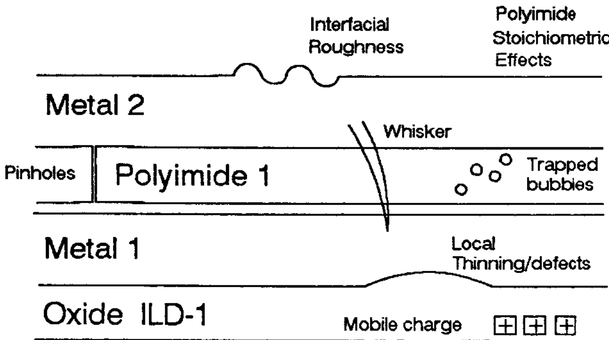



**Figure 39.** Shows the electrical defects that could reside between the metal/polyimide/ ceramic multilayer. As the metal line pitch decreases, or higher operating temperatures are used, these become more important for reliability. Diagram compiled from different sources including Bakoglu.[71] *(Reprinted with permission.)*

**Table 4.** Various Dielectric Properties That Must Be Monitored, That May Impact Dielectric Reliability

| DIELECTRIC INTEGRITY AND RELIABILITY BY CV/IV |
|---|
| Measurement of Dielectric Quality |
| • **Time zero dielectric breakdown (TZDB)**<br>Voltage-to-breakdown ($V_{BD}$)<br>Field-to-breakdown ($F_{BD}$)<br>Self Healing behavior ($V_{SB}$,K) |
| • **Time dependent dielectric breakdown (TDDB)**<br>Time-to-breakdown ($t_{BD}$)<br>Charge-to-breakdown ($Q_{BD}$)<br>Electric field acceleration (G, $\beta$) |
| • **Oxide trapped charge**<br>Oxide trapped charge centroid ($\bar{X}$)<br>Oxide cross section ($\sigma$)<br>Oxide trapped charge distribution [$n_{ot}(X)$] |
| • **Statistical data analysis**<br>Weibull plots<br>Process control charts |

## 6.5 Long Term Reliability

Long term reliability of multilayer metals in polyimide includes tests for:

1. Heat resistance.
2. Planarization and eventual viscous flow.
3. Withstanding wire bonding, die attach.
4. Withstanding the pressure cooker test (PCT).
5. Withstanding temperature/humidity (T/H) test.
6. Effect of incomplete imidization.
7. Effect of sodium on device performance.
8. Protection of devices from alpha particles.
9. Propagation of soft error rates (SER).
10. Effect of via chain resistance and its change.
11. Effect of electromigration.
12. Effects dealing with the absorption of water.
13. Effects of $Si_3N_4$ passivation.

There have been several papers dealing with various aspects of these issues, and in all of them polyimides compare very favorably with TEOS, PSG, and other conventional dielectrics.

The most extensive tests were carried out by A. W. Lin[20] of AT&T, who compared nine commercial polyimides for multilevel interconnection applications. In his tests, DuPont PI2555 performed the best. This was compared against other formulations which included PI2540, PI2545, PI2550, PI2560, PI2562, PI 2566, and PI2590. Photosensitive PIs were also included in the test; these included Hitachi's PIQ, PAL 1000 and photosensitive PI, Rhone-Poulenc Nolimid 32, Lat 10*, 50*, Kermid 601, Ciba Geigy, Upjohn Polyimide 2080, Epoxy Tech Epo Tech 390 3M Photosensitive PI, Siemens Photosensitive PI, and EM chemical HTR-2 photosensitive PI.

Lin subjected these materials to the Temperature Humidity Bias (THB) test 85°C, 85% RH, 180 vdc bias with 3 mil (75 μm) spacing. The following is a summary of the findings. Thermoplastic preimidized materials showed poor chemical resistance. Compared with RTV, considered the best encapsulant for ICs, with leakage of 10E-9 amps at the THB test, all the polyimides showed increased leakage with time, with currents in the 10E-9 to 10E-7 amps. The data for DuPont PI255 is compared with RTV in Fig. 40.

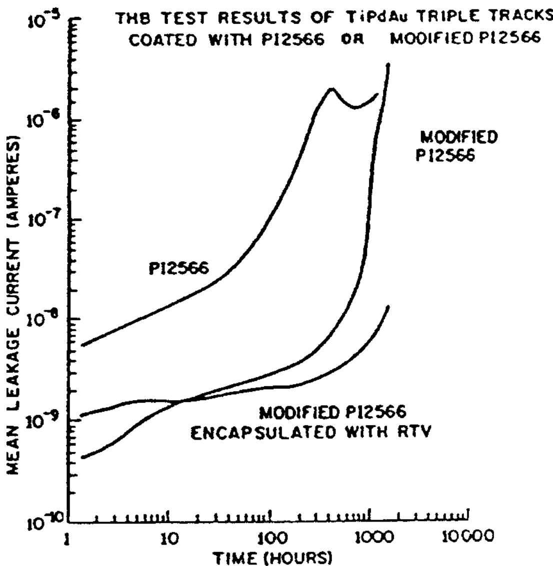



**Figure 40.** Encapsulated leakage current graph.

When the best polyimide is encapsulated with RTV, the leakage current is reduced to lower values at 100 hours. These tests showed that contaminants have a severe effect on increasing the leakage current. Mobile ions including sodium are possible suspects.

Degradation of metallized via chains with polyimide has been studied by Homa,[18] who developed a special test structure which allowed testing of wiring crossovers, which were subject to T/H testing and measured by four point probe for opens and shorts. They report that via resistance showed little or no change and the voltage bias test with 10 volts over a 675 × 72 crossover area showed no change in insulation resistance. Their conclusion from testing 236,000 vias with 10 V bias with 85/85 stress test showed no via and interlevel failures. It appears from this paper that if particular attention is paid to cleanliness and process detail, highly reliable structures can be obtained.

Although the uptake of moisture by the polyimide is always a concern, there have been a number of studies in the literature showing that it is possible to passivate the polyimide surface and achieve good reliability. Hefner, et al.,[70] compare PIQ-13 and $Si_3N_4$ moisture uptake. Taking conventional oxide dielectrics as standard, the pressure cooker test (PCT) showed that a passivating $Si_3N_4$ coating over the polyimide gave comparable moisture uptake to conventional oxide dielectrics. Low leakage currents of 1 pA were observed, and it was concluded that the $Si_3N_4$ can also act as an etch stop for subsequent layers. Other long term reliability tests have been reported in the literature. See Makino[19] and Lin.[20]

### 6.6 Summary

It can be seen that the reliability measurements for this technology are very important anytime a new material is introduced into the commercial market. Organic dielectrics have, thus far, shown great potential for the building of high reliability structures. Let us now move on to a discussion of the performance advantages of organic dielectrics in multilevel metal interconnects.

## 7.0 PERFORMANCE ADVANTAGES OF ORGANIC DIELECTRICS

A discussion of organic dielectrics would not be complete without the discussion of their performance advantages over conventional

dielectrics. This section will make some simple comparisons with more conventional dielectrics and conclude by discussing what the authors consider to be the ultimate limits in the use of polymers.

## 7.1 Performance Comparisons

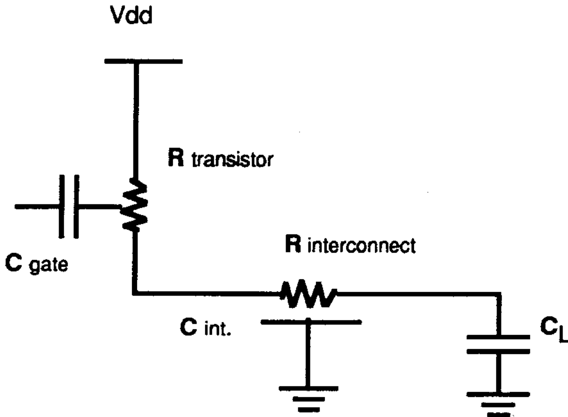
Organic dielectrics offer properties which make them desirable over many other inorganic dielectrics. One of the most important properties is the dielectric constant, which has a direct effect on the transmission of signals in the wiring levels. Simply stated, the lower the dielectric constant, the higher the performance that can be attained. Let us discuss this matter in a little more detail and compare some of the effects of lowering the dielectric constant in a metallized structure.

The importance of having low dielectric constants in chip and package wiring, in order to enhance performance, can be shown by a simple calculation of interconnection wiring capacitance. This is a simplification of a more complete treatment by Bakoglu[71] and Glasser.[72]

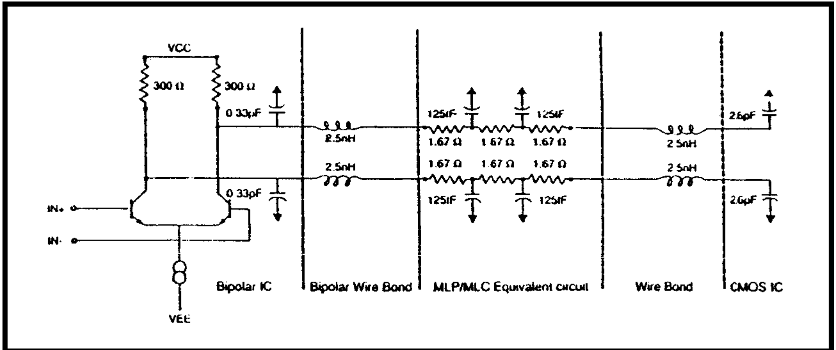
As chip dimensions increase, wiring capacitance of on-chip wires approaches the driver gate capacitance. At least at this point, wiring capacitance dominates the circuit delay. If chip sizes are increased beyond this critical size, larger global nets will not perform as fast as smaller nets. The same is true at the board level, where chip-to-chip capacitance is an order of magnitude higher than on-chip capacitances.

The chip level wiring capacitance can be modeled as shown in Fig. 41, where a driver is connected to a receiver via an interconnection of length $l_{int}$. The capacitance between the wire and ground includes the signal layer dielectric constant, here assumed to be oxide, with a dielectric constant of about 4 pF/cm. The driver in this example is a CMOS driver with a rise time of 500–2000 psec. The assumption is that the rise time $t_r$ is much larger than the time of flight, which is assumed to be about 2 psec. Under these conditions a simple lumped circuit is valid. Faster circuits will be treated later.

Figure 41(a) shows a simple equivalent circuit to illustrate the importance of capacitance in determining wiring delay. A more complete model would include distributed capacitances, inductances, reflections, etc. The gate delay increases with the on-resistance of the driver, the capacitance of the wire, $C_{int}$, and the capacitance of the receiver gate, $C_{gate}$. When $C_{int}$ is larger than $C_{gate}$, wiring capacitance dominates the delay.




(a)




(b)

**Figure 41.** (*a*) Shows the simple model of a driver and a receiver and the equivalent electrical circuit. (*b*) Shows a more complex and realistic driver-wire-MLM-to receiver in a typical IC. Under certain conditions the simple model in (*a*) can predict the behavior of (*b*).

Figure 41(b) shows a realistic model for an actual bipolar IC driver coupled via wires to an external circuit and then to a CMOS IC, which is given, to first order, as:

Eq. (3) $$T_{50\%} = R_{tr}(C_{int} + C_{gate})$$

where $C_{int}$ is the interconnection capacitance, $C_{gate}$ is the gate capacitance, and $R_{tr}$ is the driver resistance. The fifty percent delay, $T_{50\%}$, is defined as the delay from the time the input potential reached midway between $V_{dd}$ and ground to the time the output reached the same point. For the purpose of this argument we take a simple form of $C_{int}$ as:

Eq. (4) $$C_{int} = \frac{\varepsilon_{ox} W_{int} \, l_{int}}{t_{ox}}$$

with $W_{int}$ as the interconnect width and $t_{ox}$, the ILD thickness. Values of $C_{int}$ turn out to be about 2 pF/cm.[73]

The equivalent circuit shown in Fig. 41(a) is used to determine the $T_{50\%}$. Using these two formulae, we can reach some important conclusions about wiring delay. Suppose chip dimensions are increased. At some point the interconnection capacitance will equal the gate capacitance. The wire length at which this point is reached is given by:

Eq. (5) $$C_{gate} = 2.0 \frac{\text{pF}}{\text{cm}} l_{\text{int}}$$

For a $C_{\text{gate}}$ value of the order of 0.6 pF (typical number for a 2 µm channel 10 µ × 20 µ device), one calculates the critical length as 0.3 mm. This leads to several conclusions:

- First, the capacitance of a 0.3 mm long wire equals the input capacitance of a large CMOS inverter.
- Second, as the inverter is made smaller, this critical length will decrease. Therefore, neglecting other factors, as integration increases, larger chip sizes become increasingly slow.
- Third, the critical paths of large logic chips are usually dominated by wiring rather than device capacitance, in state-of-the-art device technology.
- When one is dealing with GaAs and fast logic technologies, the wiring designer has to force a compromise between several wiring layers, the interlevel dielectric constant, and wire size and shape.

There are several factors that go into optimizing the wiring delay. The choice of the dielectric is a significant one. It helps to choose a dielectric with as low a dielectric constant as possible. The second is the shape of the conductor, especially its width over height (*W/H*) ratio and the insulator thickness. The decrease of wiring capacitance with these factors is shown in Fig. 42, which shows the decrease of wire capacitance with geometry and with the dielectric constant fixed at 2 and 4, modified after Edelstein, et al.,[74] and Bakoglu and Meindl.[71] Wire capacitance decreases as *W* is decreased with respect to *H*. There must be a balance, however, between width and height to optimize the resistive and capacitive components. This relationship continues until *W* approaches the dielectric thickness, where the capacitance levels off at about 1 pF/cm.

Certainly other factors are involved in optimizing the wiring delay such as the resistance of the conductor, temperature, and other factors which for brevity will not be discussed here.

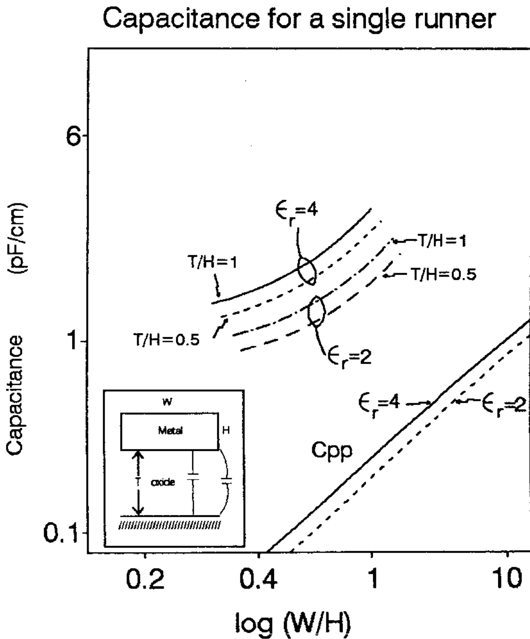



**Figure 42.** A calculation of the capacitance of a single runner, when it is placed in oxide and in polyimide; the graphs illustrate the effect of the decrease in the dielectric constant. *(Modified from a diagram for Bakoglu and Meindl.*[71])

With faster technologies, where much faster rise times are involved, like 20–100 psecs, transmission line analysis has to be used. Here the line inductances have to be considered, and the analysis becomes more complex. Nevertheless, the simple argument about using lower dielectric constant insulators still holds. In order to make a comparison, Table 5 showing on-chip rise times is useful.

**Table 5.** Rise Time of Different Semiconductor Technologies *(After Bakoglu)*[71]

| Technology | On Chip Rise Time | Off Chip Rise Times |
|---|---|---|
| CMOS | 500–2000 | 2000–4000 |
| Bipolar | 50–200 | 200–400 |
| GaAs | 20–100 | 100–250 |

Let us define the critical length $l_{crit}$ to be the propagation velocity $V_{prop}$ times the rise time $t_r$. It then can be shown that under the condition that the size of the package is larger than $l_{crit}$, time of flight arguments will still hold. This will predict that there is a direct advantage to the use of lower dielectric constant materials.

Used in the right regime, the propagation speed vs dielectric constant is given in Fig. 43. Clearly the propagation velocity increases as one reduces the dielectric constant.

Figure 44 shows $l_{crit}$ vs rise time $t_r$ for various technologies and one arbitrary value of propagation velocity. The numbers are derived from Bakoglu.[71] This graph shows the regimes where time of flight arguments can be used. Given a $t_r$ of 500 psecs, it will be seen that time of flight arguments can be used up to 3 cm. However, for a GaAs driver with a 10 psec rise time, $l_{crit}$ is only 6 mm. By using an ILD with a lower dielectric constant, one can shift the $l_{crit}$ line to higher values.

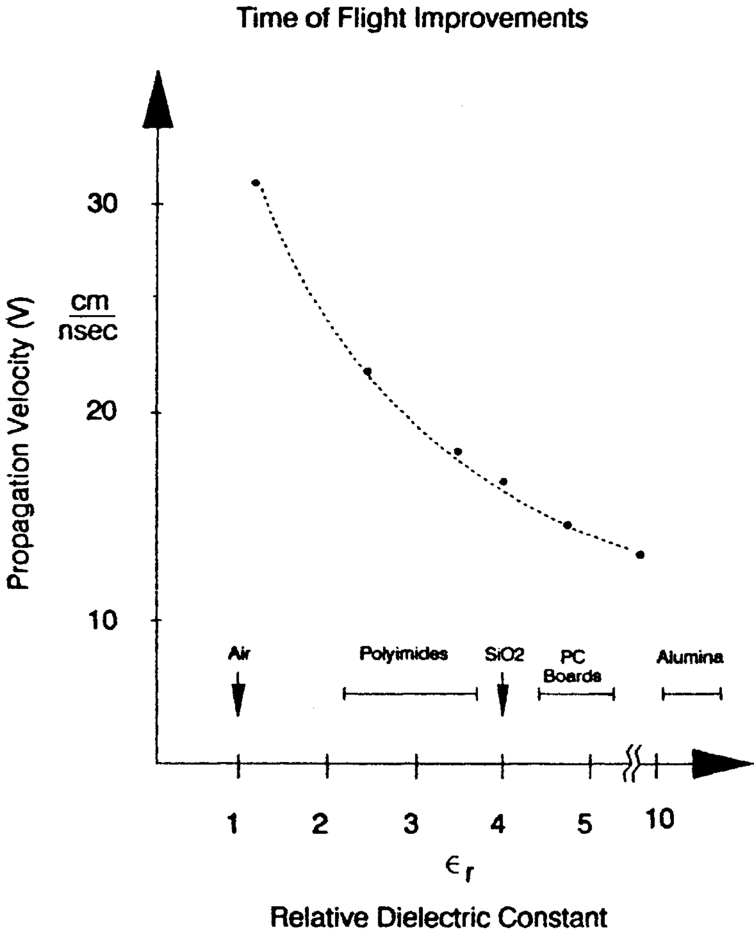
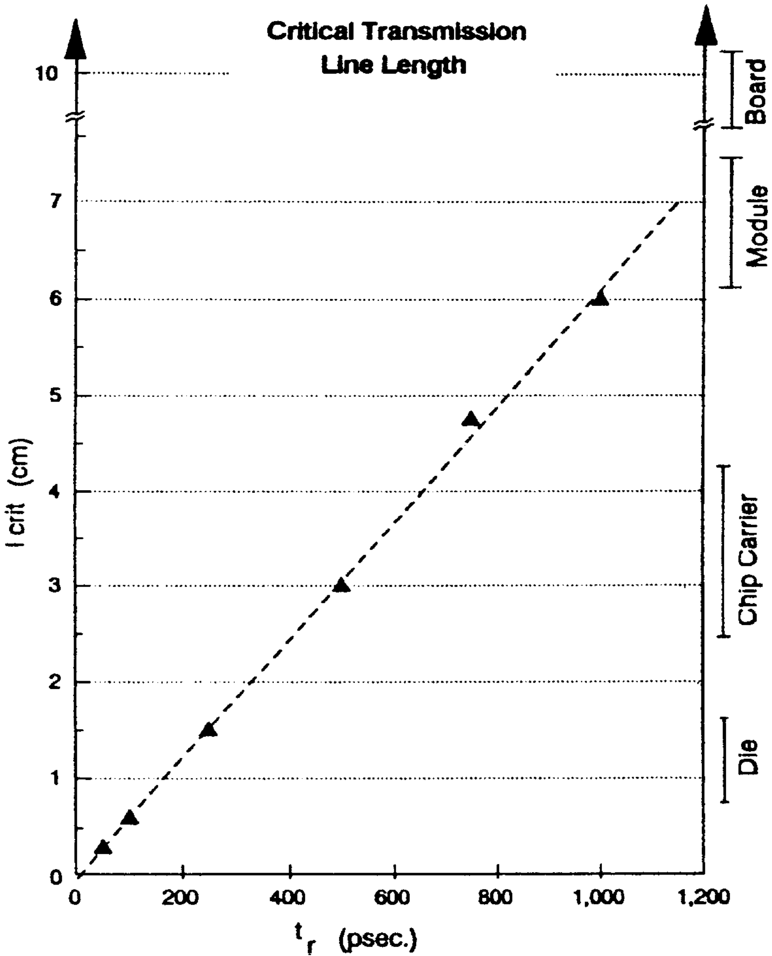



**Figure 43.** Shows the time of flight improvement as a function of the dielectric constant.




| Tech. | Chip | Package |
|---|---|---|
| CMOS | 200-500 | 2000-4000 |
| Bipolar | 50-200 | 200-400 |
| GaAs | 20-100 | 100-250 |

**Figure 44.** A diagram showing that for a certain rise time, the domain where the dielectric constant reduction achieves performance improvements. For a chip or a module with rise time over 1000 ps, it will be seen that dielectric constant and size reduction achieves performance improvements.

## 7.2 Performance Conclusions

In summary, the electrical interconnect designer is driven by several factors:

- Line resistance should be minimized. This is the motivation for using copper-based interconnections.
- Dielectric constant should also be minimized. This is the main motivation to implement organic dielectrics.
- Wiring dimensions, shapes, and spacing should be optimized to minimize crosstalk.
- Line length should be minimized and reflection matching considered. This is achieved by a judicious layout.

These factors often impose contradictory requirements; however, by a judicious application of these principles, a fully integrated multilevel metal structure can be evolved.

## 7.3 Factors in the Ultimate Limits to Performance

The ultimate performance of wiring structures for integrated circuits may depend on the scaling and conduction of nanometer dimension conductors.

Van Roggen and Meijer[75] have studied the conduction mechanisms in purified polyethylene single crystals. They have reported some very interesting nonlinear conduction in thin 100 Å, single crystals as shown in Fig. 45 from their 1962 and 1988 papers. More recently, this group has used a spring-loaded, etched wire contact and has reported the same observation in 2 to 3 layered structures. In some of the follow up papers the authors have suggested the use of such characteristics in FET type molecular electronic devices as described in Fig. 46. The interested reader is referred to the papers of Meijer and co-workers.

The important implication from the point of this chapter is as follows; as signal line pitch continues to scale to submicron dimensions, the anisotropy of organic polymer chain type structures will begin to manifest itself. The first property to come into question will be the dielectric constant; the fact that Meijer and co-workers have shown molecular conduction means that the "macroscopic" definition of the dielectric constant is itself in question. This, in turn, poses two challenges.

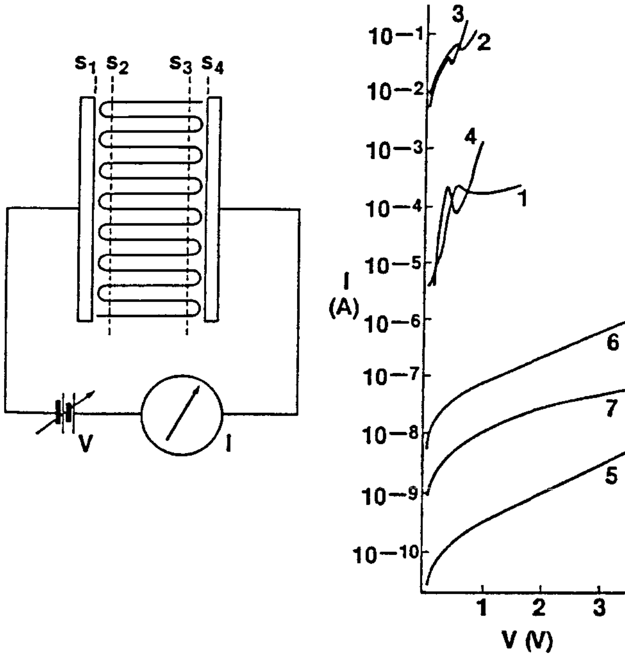



**Figure 45.** Experimental setup and electrical parameters of conduction in purified single crystal polyethylene.[75] *(Reprinted with permission.)*

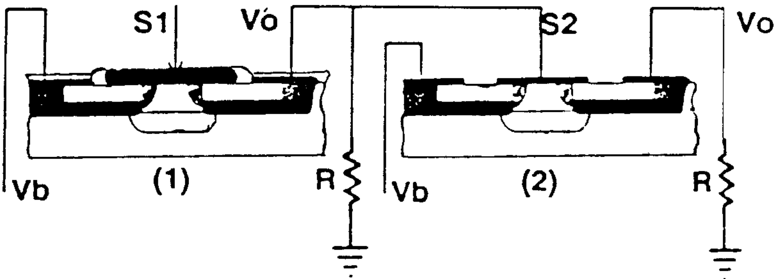



**Figure 46.** Two FET devices as conceived by Meijer for use in molecular electronics.

The first challenge is to define an "average" small dimension dielectric constant. This will affect and limit the performance of the interconnection scheme in a fundamental way; specifically it will result in a net increase in the dielectric constant, thus increasing the RC constant. This will work against the use of organic polymers as we have them now, unless new polymers are developed.

The second challenge is to measure the dielectric constant at such small dimensions. This will force the use of optical techniques to determine the refractive index and then derive the dielectric constant from the classical relation to the refractive index. However, it will be evident to the reader that this is making a "classical" compromise. We believe the papers of Meijer, et al., are important from these points of view towards the future.

It is anticipated that organic dielectrics will gain more popularity as these materials and processes improve. Our expectations of future trends are addressed in the following section.

## 8.0 FUTURE TRENDS

Now that we have examined the present state of organic dielectrics in multilevel metallization applications, we can attempt to make some predictions about future trends.

From the literature, it is clear that from the perspective of cost, performance, reliability, and low defect rate, organic dielectrics are of great interest.

The use of polyimides as we mentioned is driven by performance requirements, due to their low dielectric constants, or for cost-performance applications. We also stated that implementing more levels of metal in advanced metallization schemes requires some degree of planarization. Polishing layers with materials of very dissimilar mechanical properties is still a fundamental problem, but not specific to polyimides.

It is also shown in the literature that the utilization of polyimides has occurred to a larger extent in Japan than in the U.S., specifically in the cost-performance low end products.[19] From this position, there are not fundamental properties that limit the increased use of polyimides in both chip and package.

Finally, it can be said that the main reason that organic dielectrics are absent from many products is historical. Many device and process

designers do not yet feel comfortable with these nontraditional materials. This is probably due to the fact that electrical engineers and metallurgists are determining the processes. If we want to see more usage of organic dielectrics in the future, a shift towards hiring polymer chemists and chemical engineers will be required. The use of polymers will also occur if there is no inorganic material which can meet the design requirements. This may happen if a low dielectric constant (< 3) becomes mandatory.

Further developments in the treatment and the understanding of polyimide surface properties are also anticipated. Hiroyuki, et al.,[76] have shown that polyimides become highly hydrophilic upon irradiation by deep-UV or UV lasers in air. This laser exposure is efficient, and these authors have shown the possibility of direct image metallization. The metal does not nucleate on the laser-exposed regions, while unexposed surfaces showed uniform metal deposition. Such developments could stimulate the use of electro- and electroless deposition processes for the patterning of fine metal lines.

Activity in the CVD deposition of polyimides directly from the vapor phase is being investigated by Kowalczyk and others.[77] While this is an advanced application, it is not likely to be used in cost-sensitive packages.

Considerable work has concentrated on characterizing polyimides and other organic dielectrics. Many of the polymers in use today are trade-offs between materials with the best electrical properties and acceptable mechanical properties. In some cases, this combination is difficult to achieve. At the present time, polymers that are variations of Teflon are being examined seriously due to its low dielectric constant (< 2.5). Although Teflon does not have the required thermal and mechanical properties, we expect to see new organic materials which do meet these requirements.

It can be said with some confidence that the optimum dielectric for microelectronics applications has not yet been found. Polymers for the future will require decreasing dielectric constants while also providing improved moisture resistance, thermal and mechanical properties, and cost.

In conjunction with these materials, new classes of materials which are hybrids between organic and inorganic dielectrics are just beginning to be investigated. The art of solgel technology for glass formation is being explored where one of the silicon ligands is replaced by an organic group. This new class of "glasses" demonstrates new properties of low dielectric

strength and high temperature stability. The drive towards low dielectric constants has initiated a study on porous materials that would have lower dielectric constants due to the incorporation of tiny pockets of air. These organic solgel compounds contain large pores where a network of material is formed containing many air spaces in the structure. It is expected that these materials could be very useful if the mechanical properties are such that it survives semiconductor multilevel metal processing.

In the areas of process development, it is expected that photosensitive dielectrics will become more prevalent. With much simpler processing capability, these materials will be ideal for both chip and packaging applications where their simplicity and cost can be exploited. The limitations of these polymers today are generally in the form of critical dimension control due to solvents in the polymer which are not baked out during the restricted bake cycles. While this is a limitation in today's materials, rapid advances in photoresist technology has resolved many of these problems and it is expected that photosensitive organic dielectrics will follow close behind.

As dimensions of chips becomes smaller, device designers will be pushed to the limits of semiconductor physics to produce further gains in performance. It is expected that improvements in the multilevel metal process and materials offer the greatest potential for performance improvements. Given this reasoning and the proper paradigm shifts, it is expected that organic dielectrics should become more widespread in order to meet the growing demands in the electronics industry.

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# 14

# Performance, Processing, and Lithography Trends

*Krishna Seshan*

## 1.0 INTRODUCTION

Lithographically defined dimensions will continue to shrink as device scaling enables higher speeds and greater density of transistors. Lithography equipment, resist processes, and mask-making will change to meet the challenges. Gate oxides have to become thinner requiring changes in both growth and metrology equipment. As gate oxides become thinner, voltages must drop bringing about new material requirements. Lithography will call for highly planarized surfaces, causing higher demands on chemically-mechanically polished surfaces.

As transistor densities increase, the wiring levels providing interconnectivity will increase. This will increase the RC (resistance-capacitance) delay contribution of interconnections. The consequent drive to reduce resistance will drive the change from aluminum-based wiring metallurgy to copper-based metallurgy. In addition, the drive to decrease the dielectric constant will call for changes of the $SiO_2$-based dielectric to a class of "low-K" dielectrics.

Stringent demands will be made on contamination control, particle detection, and yield enhancement. One of the consequences will be the move from 8 inch to 12 inch wafers. This will drive consolidation of process steps.

These changing technologies will present new reliability challenges. This chapter discusses these trends and challenges.

## 2.0 SCALING THE TRANSISTOR

Gate oxide thickness, channel length, and power supply voltage scale along well-predicted trends as shown in Fig. 1. This figure is the basis for understanding the lithography challenges—where line patterning in the range of 100 nm (0.1 μm) and gate oxides of 30 nm (0.03 μm) will need to be grown and measured.

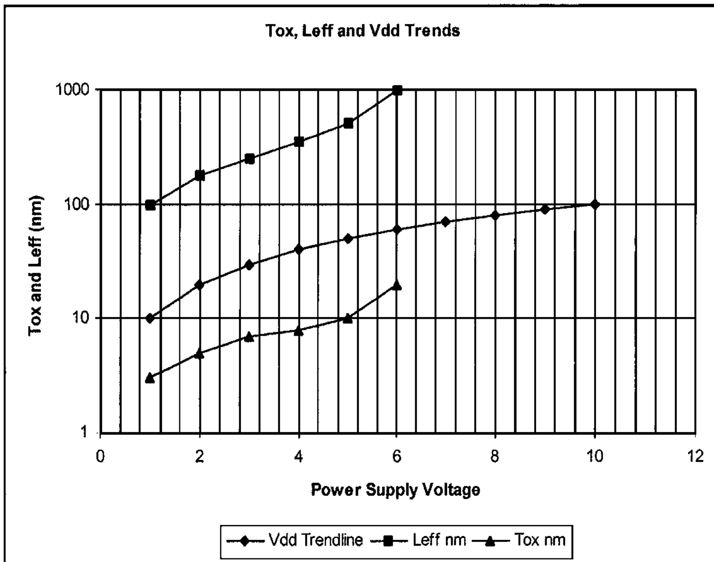


**Figure 1.** Gate oxide thickness, channel length, and power supply voltage scale along well-predicted trends.

As gate length decreases, the delay per gate decreases. This enables the transistor-based inverters to switch faster. However, there is a competing and slowing-down effect, referred to as interconnect delay.

Interconnections can be serious limiters of higher performance.[3] Figure 2 shows how the pitch decreases and the number of metal layers increase with scaling. The RC delay caused by this crowding of metal lines can be modeled using various capacitance-calculating models. The result is always the same: the back-end RC delay contribution increases.

The effect of the back-end delay is seen clearly when the *total* delay (gate delay + interconnect delay) is plotted for different generations. Figure 3 is a graph derived from the NTRS roadmap showing the total delay versus generation. This is only an estimate and is not real data. From this graph it should be clear that there is need to change the interconnect metallurgy to copper and to try to reduce the dielectric constant of the interlayer dielectric (see also Fig. 4). Many companies have announced processes and some are cited in the references.[1][2]

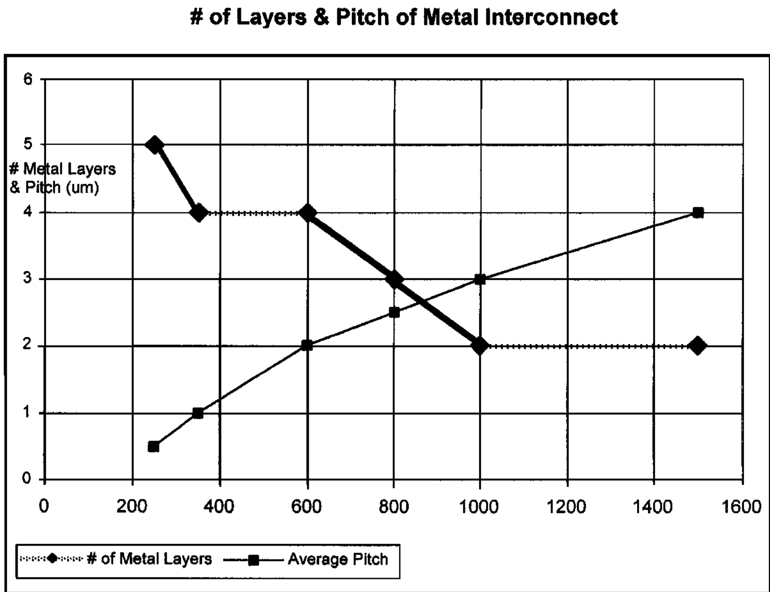


**Figure 2.** The pitch decreases and the number of metal layers increase with scaling.

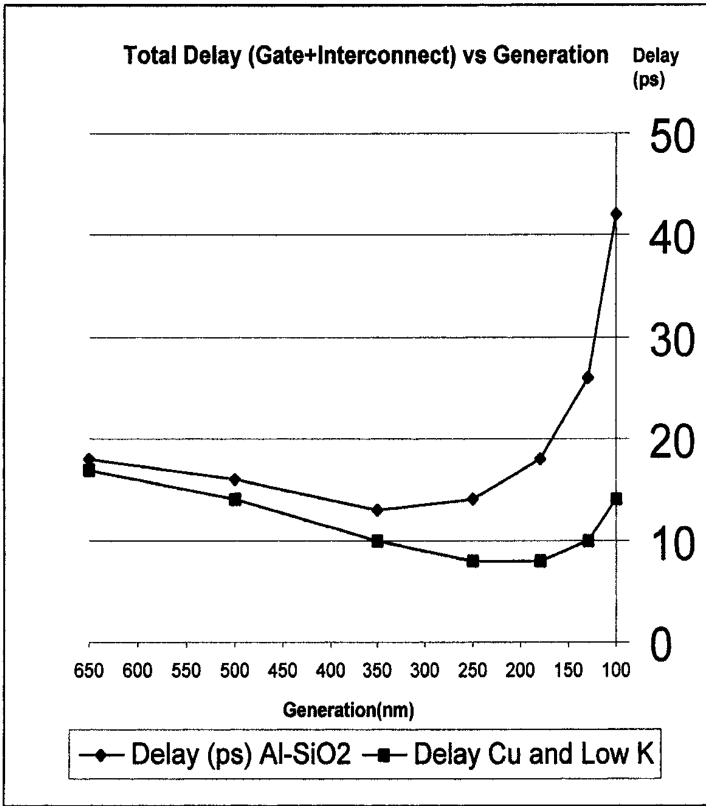


**Figure 3.** Graph shows the total delay vs device generation. This is only an estimate and is not real data.

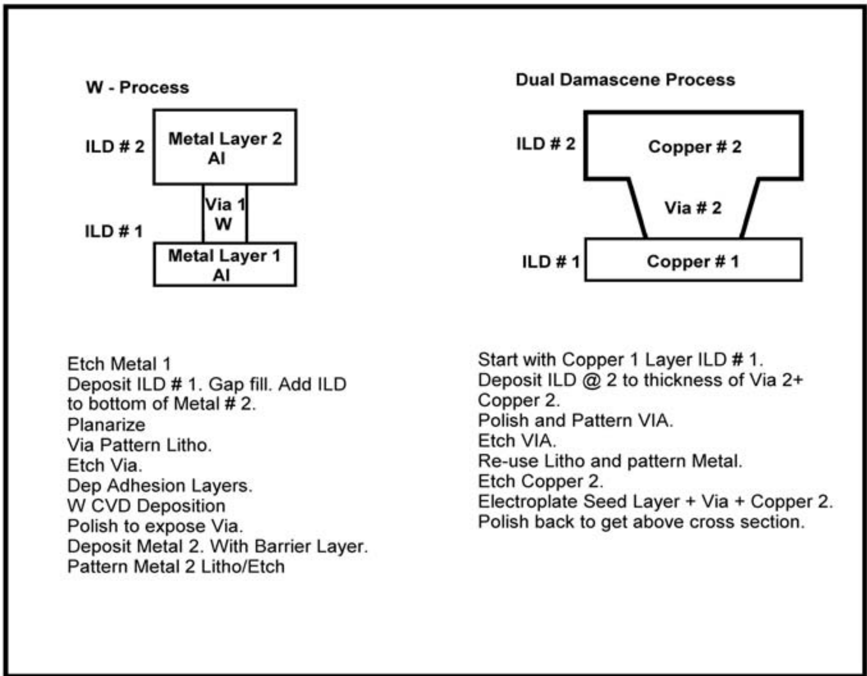


**Figure 4.** Changing to Cu-based metallurgy requires significant changes in the way the metal is deposited and patterned.

## 3.0 LOW RESISTANCE: CHANGE TO COPPER-BASED METALLURGY

Figure 4 shows how the tungsten via and Al-Si line are replaced with a copper via and a copper line. The challenge then is to change the interlayer dielectric. At this time several schemes are proposed by which the dielectric is controlled. One method includes introduction of fluorine into the deposited $SiO_2$.

The standard capacitance extraction method draws on a very simple approach that is shown in Fig. 5.

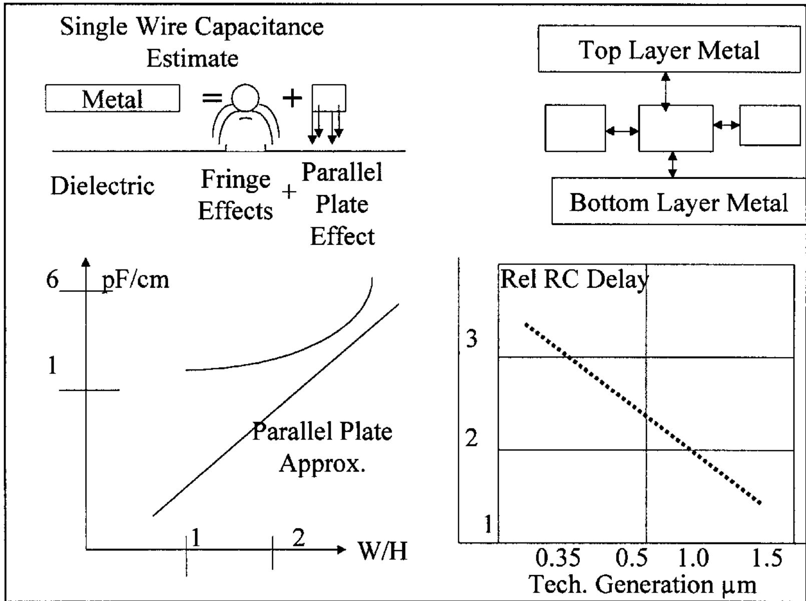


**Figure 5.** Capacitance extraction methodology and results.

The left top of the figure shows a metal "runner" modeled as a sum of a parallel plate plus a fringing capacitor. The result of such calculations (after Bakoglu, Ref. 6) is shown in the left bottom graph which indicates that as the lines are made narrow and tall, the capacitance decreases. The dielectric constant for oxide is taken to be 3.9. However, because of fringing effects, the capacitance asymptotically approaches 1 pf/µm.

On the right is a line surrounded by other metal lines, and here the graph shows how interconnect RC delay increases as lines are packed together.

From these graphs it is evident that reducing *R*, the line resistance, and *C*, the line-to-line capacitance, will be a central challenge for some time.

## 4.0 TREND TO LOW K MATERIALS

In order to obtain lower dielectric constants, the industry will have to evaluate several new materials. One simple method is to add fluorine to the deposited silicon dioxide. This is known as SiOF and has a dielectric constant of about 3.6, as shown in Fig. 6. Other spin-on materials are under evaluation, but it is too early to predict which materials may be widely used.

The combination of copper plus new low K materials provides many new challenges for the thin film industry including the development of deposition processes and equipment. Spin-on-glasses are candidates and these often need to be capped. Etching the glasses to deep aspect ratios may require the use of high density plasmas and modification of modern reactive ion etching methods. Filling the vias, and making this compatible with the copper dual Damascene process, may provide challenges for polishing and for lithography.

Table 1 shows some of the new materials that are currently available. This list is not exhaustive.

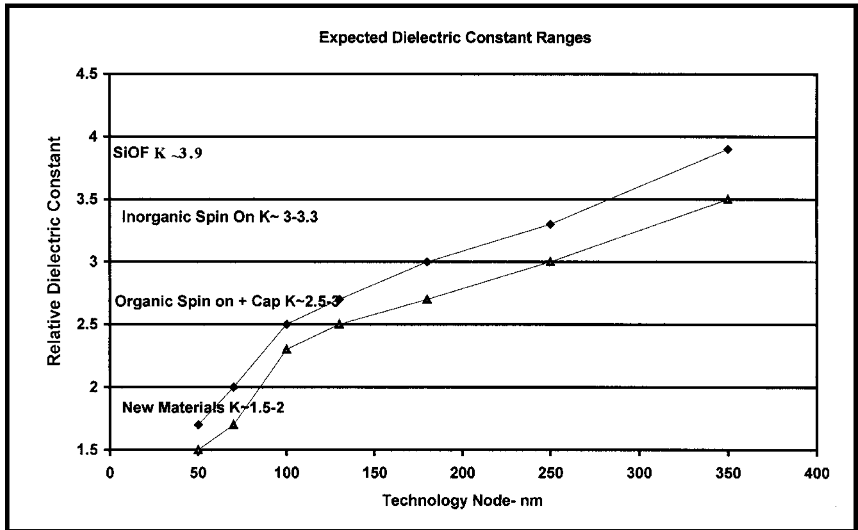


**Figure 6.** Dielectric constants of some materials.

**Table 1.** Various Dielectric Materials

| Dielectric Range | Material/Trade Name | Manufacturer or Process | Compatibility/Use |
|---|---|---|---|
| K ~7 | $Si_3N_4$ - Silicon Nitride | CVD- or HDP-nitride | Al metallurgy<br>Cu metallurgy<br>Use: moisture passivation |
| K ~4 | All forms of $SiO_2$, plasma TESO source oxides | Various sub-atmospheric, low pressure and HPD processes | In wide use with Al metallurgy, also with Cu metallurgy. Introduction of fluorine decreases K |
| K<3<br><br>K<3 | Fox™<br>SiLK-G™<br>FLARE™<br>Velox | Dow Chemical<br>Dow Chemical<br>Honywell<br>Schumacher Air Products & Chemicals | All compatible with Al and with Cu Damascene. Many processes are in development stage. |
| K <2.5 | FSG<br>Low K Flowfill<br>Black Diamond<br>Coral<br>3MS<br>HOSP™<br>Parylene AF -4 | <br>Trikon Technology<br>Applied Materials<br>Novellus<br>Dow Corning<br>Honywell<br>Parylene | Entirely in development stage at the time of writing of this book. |
| K<2.0 | Nanoglass™ | Honeywell | |

## 5.0 LITHOGRAPHY AND PLANARIZATION

Basic optical laws pertaining to lithography dictate the need for highly planarized surfaces.

Smaller dimensions make severe demands on lens designs for optical lithography equipment. Lenses have to be aberration free, shorter wavelengths must be used to expose lithography patterns, and high numerical apertures are necessary. The higher the numerical aperture, the smaller the depth of focus.

*Depth of focus* is defined as the distance range within which an image plane will still have the smallest features resolved. As the depth of focus of lenses decreases, imaging surfaces have to be more planar, placing additional demands on CMP.

## 6.0 CHALLENGES TO CONTAMINATION/CLEANING

This vast subject is discussed in Ch. 7 of this book. Here, the trends are considered from two points of view. First, Sec. 6.1 deals with the challenges to the detection of smaller and smaller particles. The second section (Sec. 6.2) deals with trends in equipment.

### 6.1 Detection/Types of Contamination

Some typical numbers describing limitations on defects are projected in Table 2. The main message from this table is that detection of small particles will be a challenge in enforcing and verifying cleanliness.

The costs of operating cleanrooms and keeping equipment clean will presumably increase, and equipment will become more sophisticated and expensive. Many laser light scattering methods for checking the state of cleanliness are currently in the development stage.

Sources of defects are airborne contamination, now containing increased amounts of molecular organic materials like amines and resist and resist cleaning materials. These are referred to as AMC (airborne molecular contamination). The detection of these contaminants and their effect on yield loss will remain a challenge to the industry.

The challenge to mask-making will be more stringent. See Ref. 8 for details.

**Table 2.** Defect Trends

| Technology Generation | 1997 | 1999 | 2001 | 2003 | 2006 | 2008 | 2012 |
|---|---|---|---|---|---|---|---|
| Wafer Handling (defects/meter$^2$) | 30 | 13 | 8 | 5 | *2* | *1* | *1* |
| Wafer Size (mm) | 200 | 300 | 300 | 300 | *300* | *450 ?* | *450 ?* |
| Critical Defect Size (nm) | 125 | 90 | 75 | 65 | *50* | *35* | *25* |
| Electrical Defect $D_o/m^2$ for 60% yield | 1940 | 1712 | 1512 | 1353 | *1119* | *939* | *776* |
| Chip Area Logic | 300 | 340 | 385 | 430 | *520* | *620* | *750* |
| Mask Levels | 22 | 23 | 23 | 24 | *25 ?* | *27 ?* | *28 ?* |
| Faults per Mask Level | 88 | 74 | 66 | 56 | *45* | *35* | *28* |

## 6.2 Trends in Integrated Processing

The concept of integrated processing is not new. It is intuitive. It is ease to show pictorially (Fig. 7), however, actually building equipment is difficult and expensive, and the practical details of how to keep the equipment clean and functioning become very complex.

A trend toward integrated processing includes mini-environments around tools so that locally clean areas near the tool and the wafer are maintained. The mini-environment can be extremely clean (Class 0.1) whereas the cleanroom can be in the Class 1 range (see Fig. 8). These will

be increasingly necessary as the wafer size increases. Actual tools based on the conceptual diagram in Fig. 7 are now available and in use.

Cleanroom technology needs increasing attention. Reduction of particulate contaminants needs sophisticated levels of understanding, measurements, and diagnostics with experimental and theoretical simulations. Contaminants may be particulate, organic or ionic, and their sources may be airborne, from chemicals used, from various processing steps, or from people, tools and equipment. Intrinsic tool processing like evaporation or sputtering may generate particles which are then released from the tool. This area will receive significant attention in the years ahead.

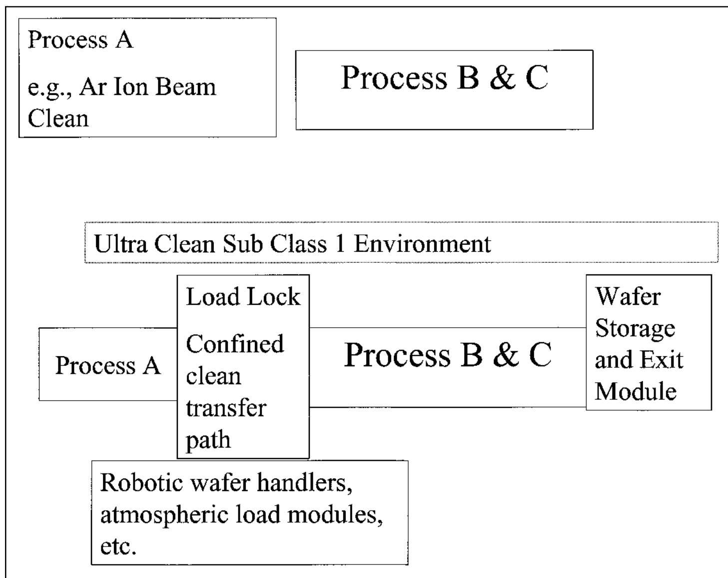


**Figure 7.** Conceptual diagram of integrated processing.

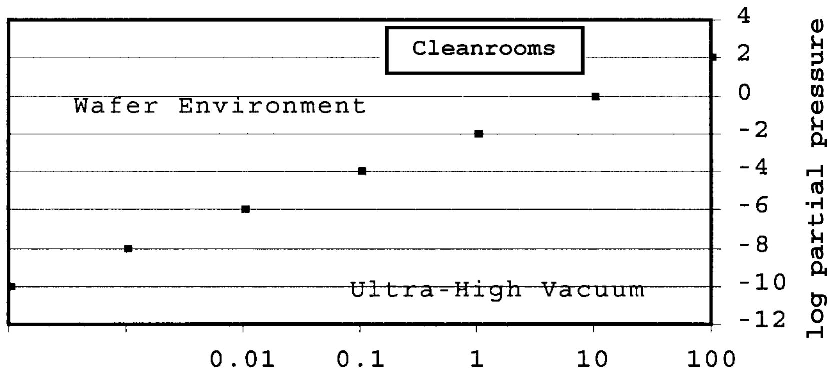


**Figure 8.** Cleanroom Class designations and associated partial pressures.

## 7.0 SUMMARY

In this industry it is difficult to be ever up-to-date and to assess trends accurately, but scaling occurs by rigorous laws so that we can relatively accurately predict where we need to be. It is more difficult to predict how we get there and what processes and materials will be in use. One thing is certain: the deposition of thin films will continue to be an enabling technology.

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