1 Fundamentals

1.1 Construction of a FinFET

1.1.1 General layout and mode of operation

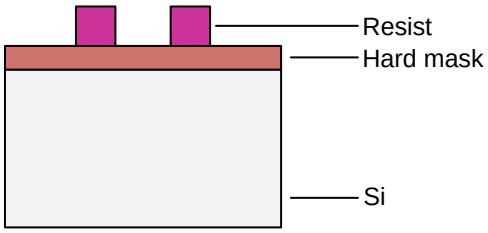
The basic electrical layout and the mode of operation of a FinFET does not differ from a traditional field effect transistor. There is one source and one drain contact as well as a gate to control the current flow.

In contrast to planar MOSFETs the channel between source and drain is build as a three dimensional bar on top of the silicon substrate, called fin. The gate electrode is then wrapped around the channel, so that there can be formed several gate electrodes on each side which leads to reduced leakage effects and an enhanced drive current.

The manufacture of a bulk silicon-based multi gate transistor with three gates (tri gate) is described below.

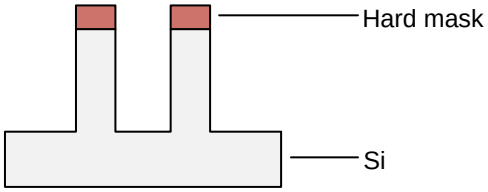
1.1.2 Construction of a bulk silicon-based FinFET

1. Substrate: Basis for a FinFET is a lightly p-doped substrate with a hard mask on top (e.g. silicon nitride) as well as a patterned resist layer.

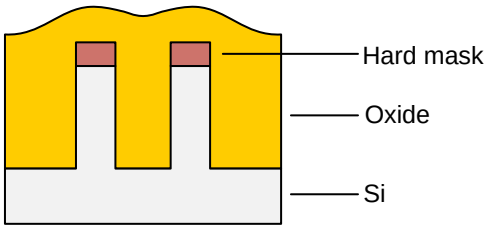


2. Fin etch: The fins are formed in a highly anisotropic etch process. Since there is no stop layer on a bulk wafer as it is in SOI, the etch process has to be time based. In a

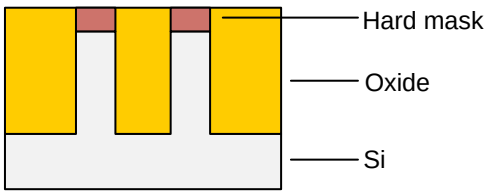
22 nm process the width of the fins might be 10 to 15 nm, the height would ideally be twice that or more.



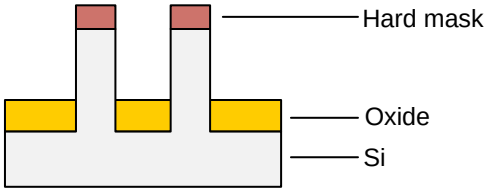
3. Oxide deposition: To isolate the fins from each other a oxide deposition with a high aspect ratio filling behavior is needed.



4. Planarization: The oxide is planarized by chemical mechanical polishing. The hard mask acts as a stop layer.

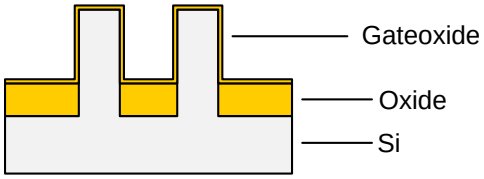


5. Recess etch: Another etch process is needed to recess the oxide film to form a lateral isolation of the fins.



6. Gate oxide: On top of the fins the gate oxide is deposited via thermal oxidation to isolate the channel from the gate elctrode. Since the fins are still connected underneath

the oxide, a high-dose angled implant at the base of the fin creates a dopant junction and completes the isolation (not illstrated).



7. Deposition of the gate: Finally a highly n^+-doped poly silicon layer is deposited on top of the fins, thus up to three gates are wrapped around the channel: one on each side of the fin, and - depending on the thickness of the gate oxide on top - a third gate above.

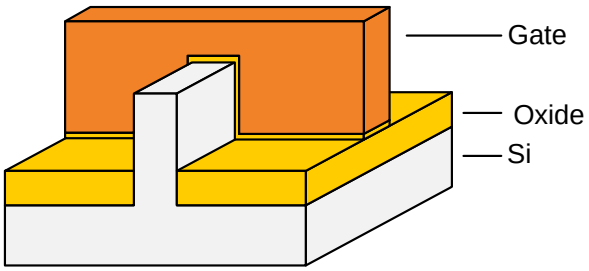


Fig. 1.1: FinFET in bulk process

The influence of the top gate can also be inhibited by the deposition of a nitride layer on top of the channel.

Since there is an oxide layer on an SOI wafer, the channels are isolated from each other anyway. In addition the etch process of the fins is simplified as the process can be stopped on the oxide easily.

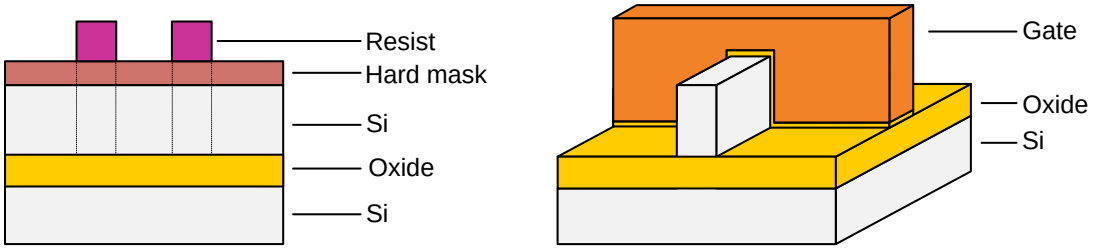


Fig. 1.2: FinFET on SOI