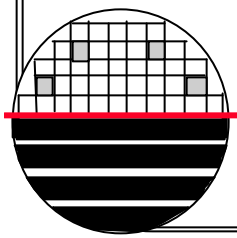
ROCHESTER INSTITUTE OF TECHNOLOGY
MICROELECTRONIC ENGINEERING

RIT's Advanced CMOS Process
(L_{poly}= 0.5 µm l=0.25 µm)

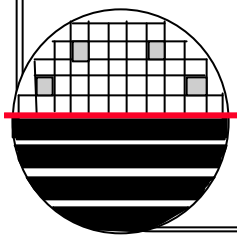
Dr. Lynn Fuller
Branislav Curanovic, Donald Hamilton, Chris Harvey, Neal Lafferty, Matt Malloy, Keith Tabakman

Microelectronic Engineering
Rochester Institute of Technology
82 Lomb Memorial Drive
Rochester, NY 14623-5604
Tel (585) 475-2035
Fax (585) 475-5041
LFFEEE@rit.edu
http://www.microe.rit.edu



OUTLINE

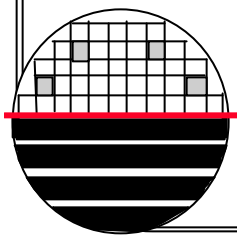
Introduction
Advanced CMOS Process Details



INTRODUCTION - FACTORY PROCESSES

RIT is supporting three different CMOS process technologies. The older p-well CMOS has been phased out. The SMFL-CMOS process is used for standard 5 Volt Digital and Analog integrated circuits. This is the technology of choice for teaching circuit design and fabricating CMOS circuits at RIT. The SUB-CMOS and ADV-CMOS processes are intended to introduce our students to process technology that is close to industry state-of-the-art. These processes are used to build test structures and develop new technologies at RIT.

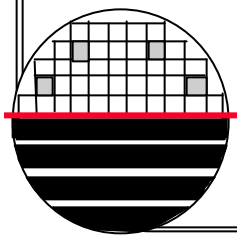
RIT p-well CMOS (1995)	$\lambda = 4\ \mu m$	Lmin = 8 µm
RIT SMFL-CMOS (2004)	$\lambda = 1\ \mu m$	Lmin = 2 µm
RIT Subµ-CMOS (2000)	$\lambda = 0.5\ \mu m$	Lmin = 1.0 µm
RIT Advanced-CMOS (2003)	$\lambda = 0.25\ \mu m$	Lmin = 0.5 µm



INTRODUCTION

Advanced Processes:

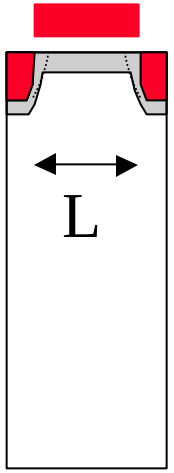
Shallow Trench Etch with Endpoint
Trench PECVD TEOS fill and CMP
Silicide TiSi2, Recipes for Rapid Thermal Processor
Dual Doped Gate, Ion Implant and Mask Details
Anisotropic Poly Etch
100 Å Gate Oxide Recipe with N2O
Nitride Spacer, New Anisotropic Nitride Etch
Aluminum Metal, W Plugs Deposition, CMP of Oxide
New Test Chip
New Masks, Canon and ASML
New Stepper Jobs, Canon and ASML
Create MESA Process, Products, Instructions, Parameters



RIT ADVANCED CMOS VER 150

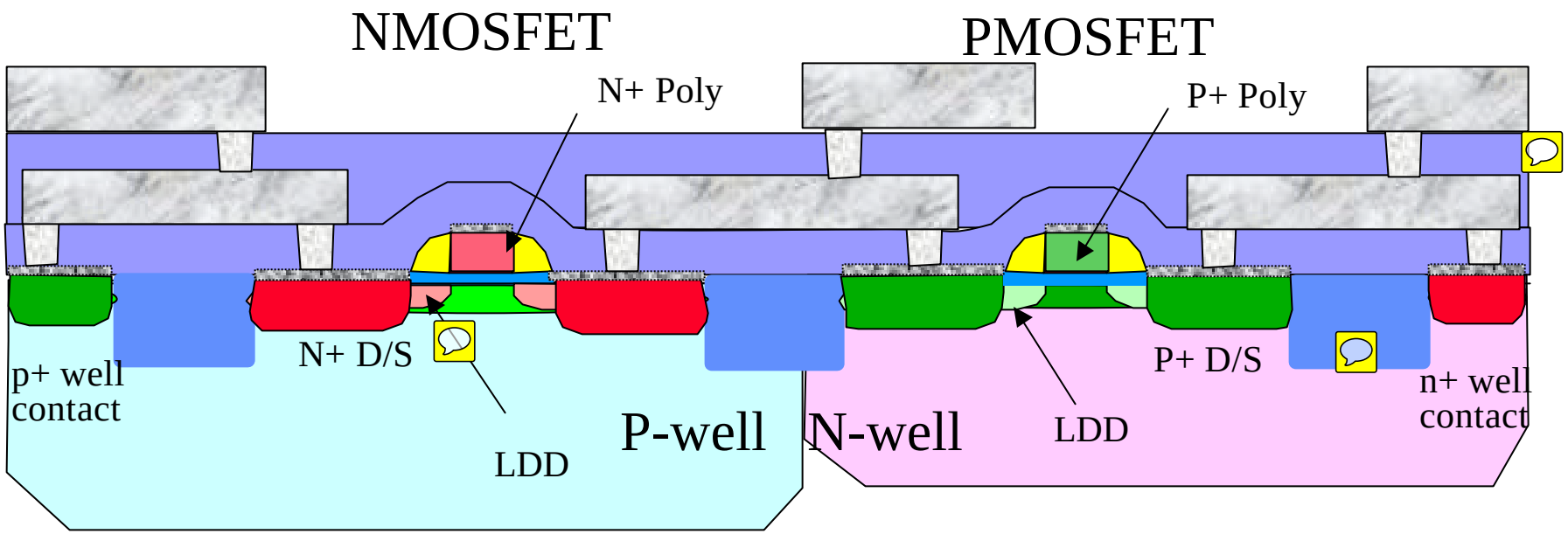
RIT Advanced CMOS

150 mm Wafers
Nsub = 1E15 cm-3 or 10 ohm-cm, n or p
Nn-well = 1E17 cm-3
Xj = 2.5 µm
Np-well = 1E17 cm-3
Xj = 2.5 µm
Shallow Trench Isolation
Field Ox = 4000 Å
Dual Doped Gate n+ and p+
Xox = 100 Å
Lmin= 0.5 µm
LDD/Nitride Side Wall Spacers
TiSi2 Silicide
Tungsten Plugs, CMP, 2 Layers Aluminum



Long Channel Behavior

RIT ADVANCED CMOS



ASML 5500/90 STEPPER

KrF Excimer Laser Stepper

λ = 248 nm

NA = 0.52, σ = 0.6

Resolution = 0.7 λ / NA = ~0.3 µm

20 x 20 mm Field Size

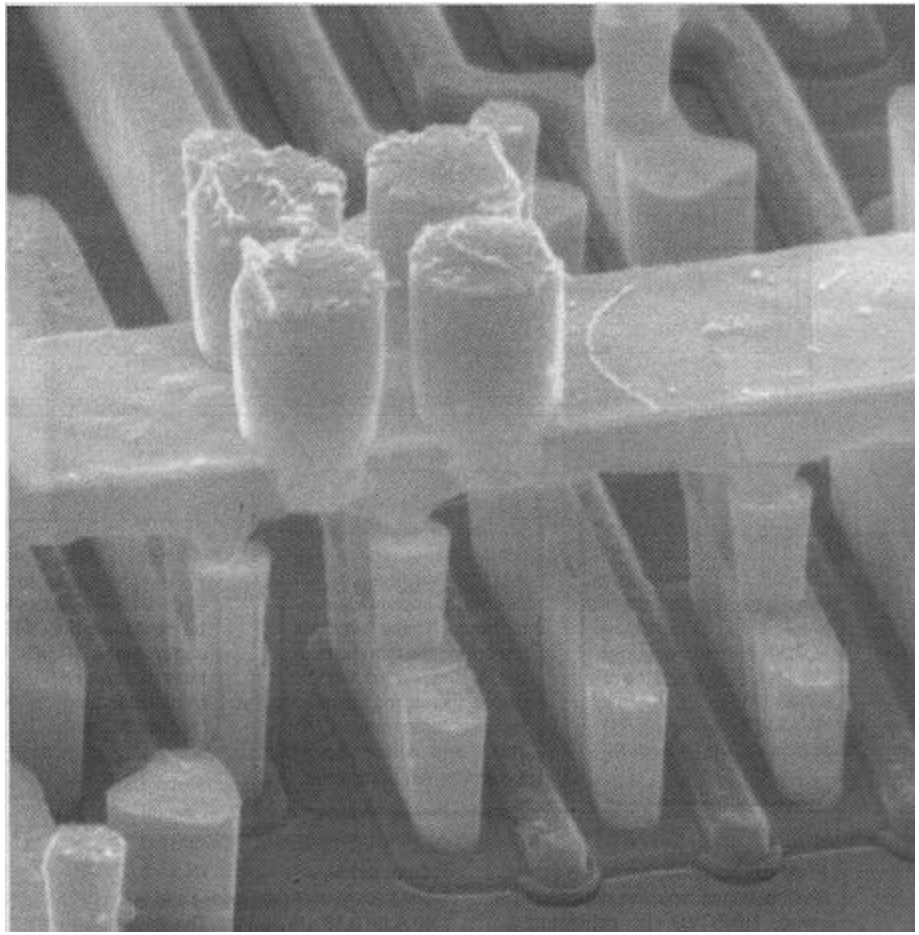
Depth of Focus = $k_2 \lambda/(NA)^2$

~ 0.64 µm

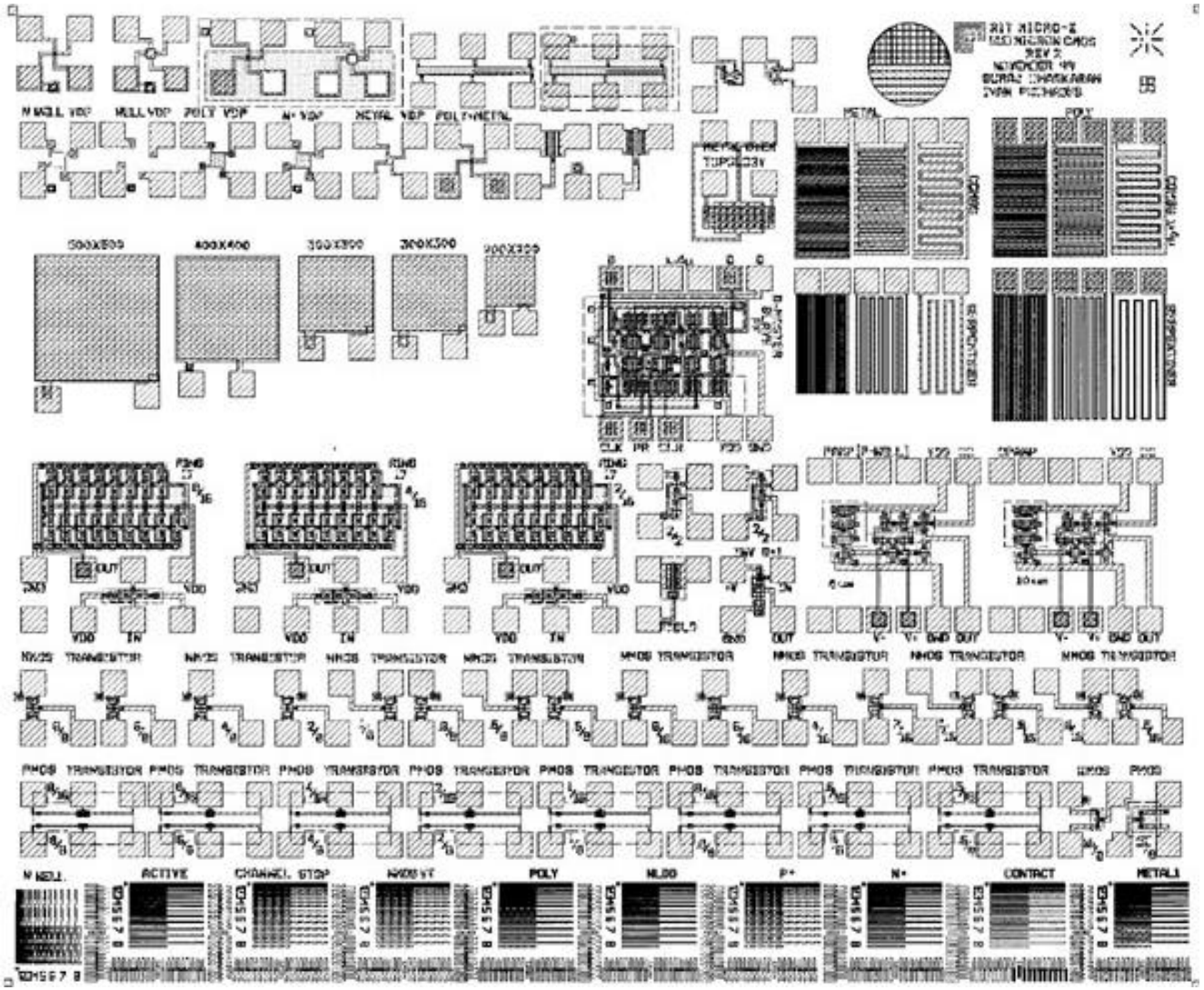
6"x6" Masks

MULTI- LAYER ALUMINUM, W PLUGS, CMP, DAMASCENE OF LOCAL W INERCONNECT

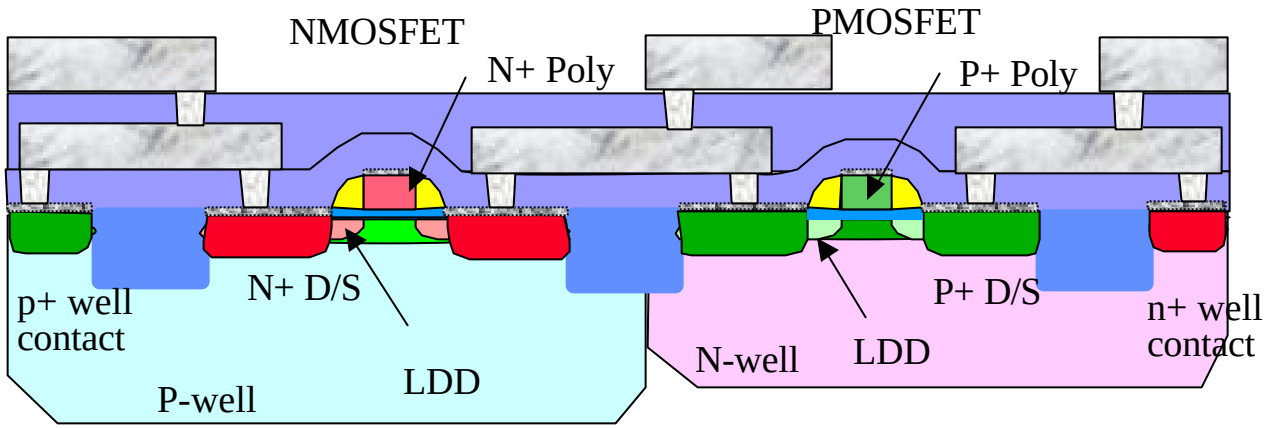
Multi-layer aluminum interconnect with tungsten plugs, CMP, and damascene of local tungsten interconnect.

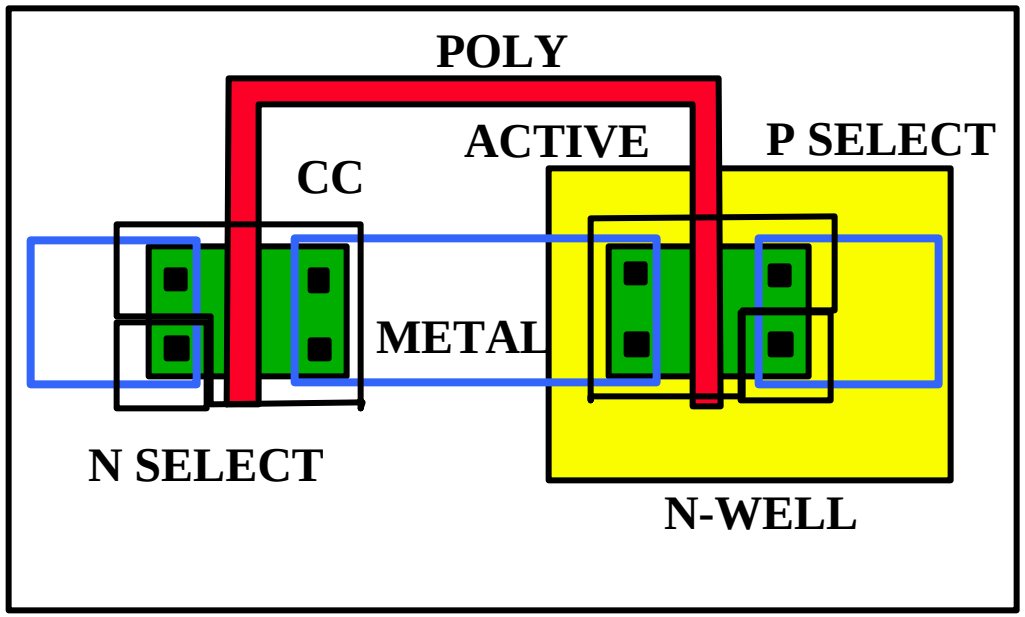


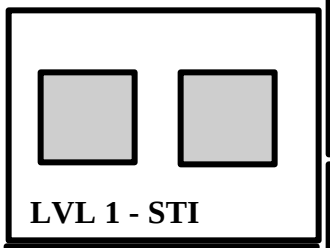
ADVANCED CMOS TEST STRUCTURES

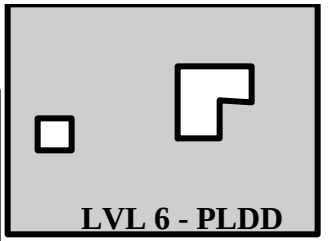


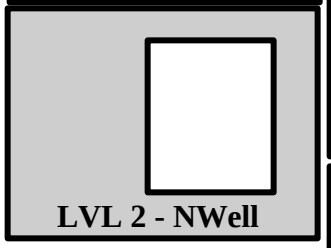
RIT ADVANCED CMOS PROCESS

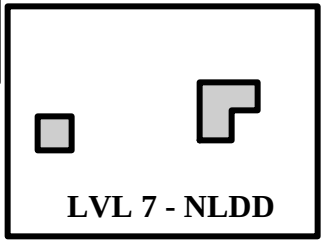


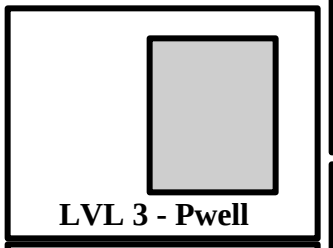


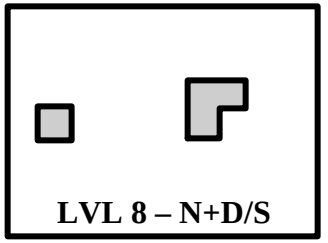


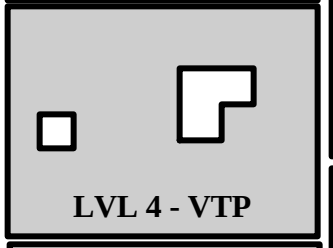


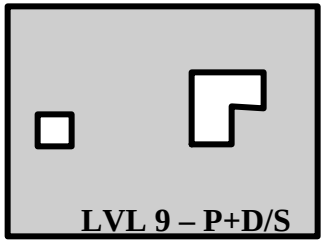


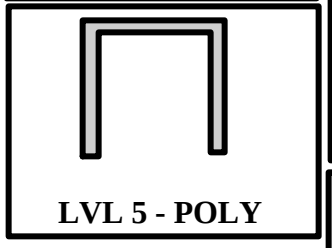


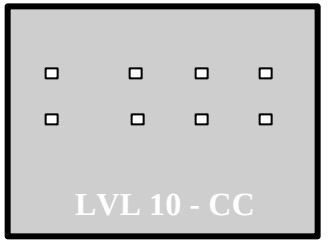




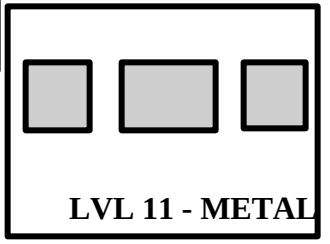








11 PHOTO LEVELS



MASK ORDER

Rochester Institute of Technology
Semiconductor & Microsystems Fabrication Laboratory

Mask Making
Order Request

Customer Information

Name: Dr. Lynn Fuller
Company / Department: Microelectronic Engineering
Street Address:
City, State and Zip Code:
Phone Number: ( ) - 475-2035
Project Code:
E-mail Address:

Order Date: 4/1/03 March 31, 2003
Order Due Date: 1st Mask by 4/8/03, 2ND Mask by 4/15/03

Mask Information

SEE PAGE 2 FOR INSTRUCTIONS ON CREATING YOUR GDS FILE!

Design Name: adv cmos04b1e3.gds
Number of Design Layers in Layout:
Number of Mask Levels:
Cell Layout Size: X: µm Y: µm
Alignment Key (Center of Die is Origin): X: µm Y: µm

Fracture Resolution: ☐ 0.5µm ☐ µm
Scale Factor: 5X
Orientation: ☒ Mirror135 ☐
Rotation: ☐ None ☐
Plate Size: 5 inch square
Number of Levels on Plate: 1
Array: ☐ None ☐ Array with rows and columns

Details for Each Mask Layer

Mask Level Name	Mask Level #	Design Layer Name(s)	Design Layer #('s)	Boolean Function	Field Type	Bias (µm)	CD (µm)
STI	1	Active-area.I	3	OR	clear		
		(INV) N-well.e	51	OR			
		P-well.e	52	OR			
NWELL	2	N-well.I	1	OR	Dark		
		Active-area.e	53	OR			
PWELL	3	(INV) N-well.I	1	OR	Dark		
		N-implant.e	54	OR			
VTP	4	P-implant.I	5	OR	Dark		
		P-implant.e	55	OR			

Comments: Other masks will be ordered later

ALL FIELDS OF THIS ORDER FORM MUST BE FILLED OUT ENTIRELY OR YOUR MASK WILL NOT BE MADE. NO EXCEPTIONS!

ADV-CMOS 150 PROCESS

CMOS Versions 150, one level Metal

1. ID01
2. DE01
3. CL01
4. OX05--- pad oxide 500 A
5. CV02- 1500 Å
6. PH03 –1- STI
7. ET29 etch shallow trench, 4000A
8. ET07-ash
9. CL01
10. OX05 – pad oxide, 500 A
11. CV03 – CVD oxide trench fill

11.1 OX07 - Anneal

12. CM01 – Trench CMP
13. CL02 - CMP_Clean
14. CL01-rca clean
15. ET19 hot phos
16. PH03-2-n-well
17. IM01 3E13, P31, 180 KeV
18. ET07-ash
19. PH03 – 3 – p-well
20. IM01 – 3E13, B11, 150KeV
21. ET07 -ash
22. CL01
23. OX06 well drive, 6hr 1100C
24. IM01 blanket implant
25. PH03 – 4 - VT adjust
26. IM01 adjust
27. ET07
28. CL01
29. ET06 oxide etch
30. OX06 gate oxide
31. CV01 poly dep
32. PH03 - 5 - poly
33. ET08 poly etch
34. ET07

35 CL01

36 OX05 pad oxide

37. PH03 –6- p LDD
38. IM01 p LDD
39. ET07
40. PH03 –7- n LDD
41. IM01 n LDD
42. ET07
43. CL01
44. CV02 nitride spacer dep
45. ET39 spacer etch
46. PH03 – 8 - N+D/S
47. IM01 – N+D/S
48. ET07
49. PH03 – 9- P+ D/S
50. IM01 – P+ D/S
51. ET07
52. CL01
53. OX08 – DS Anneal
54. ME03 HF dip & Co/Ti
55. RT01
56. ET11 Ti Etch
57. RT02
58. CV03 – LTO
59. PH03 – 10 CC
60. ET10
61. ET07
62. CL01

62.1 CV04 W Plugs

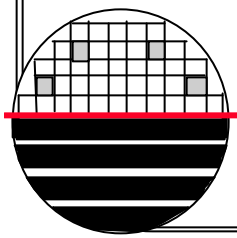
63 ME01 Aluminum

64. PH03 -11- metal
65. ET15 plasma Al Etch
66. ET07
67. SI01
68. SEM1
69. TE01
70. TE02
71. TE03
72. TE04

(Revision 9-20-04)

STARTING WAFER

N-type or P-type Substrate 10 ohm-cm



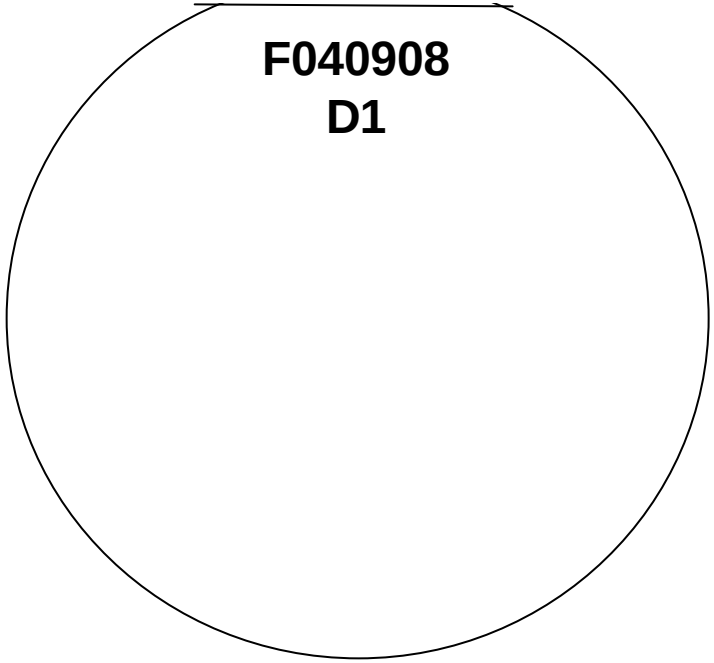
SCRIBE WAFERS WITH LOT AND WAFER NUMBER

Lot Numbers are: XYYMMDD
Where X is

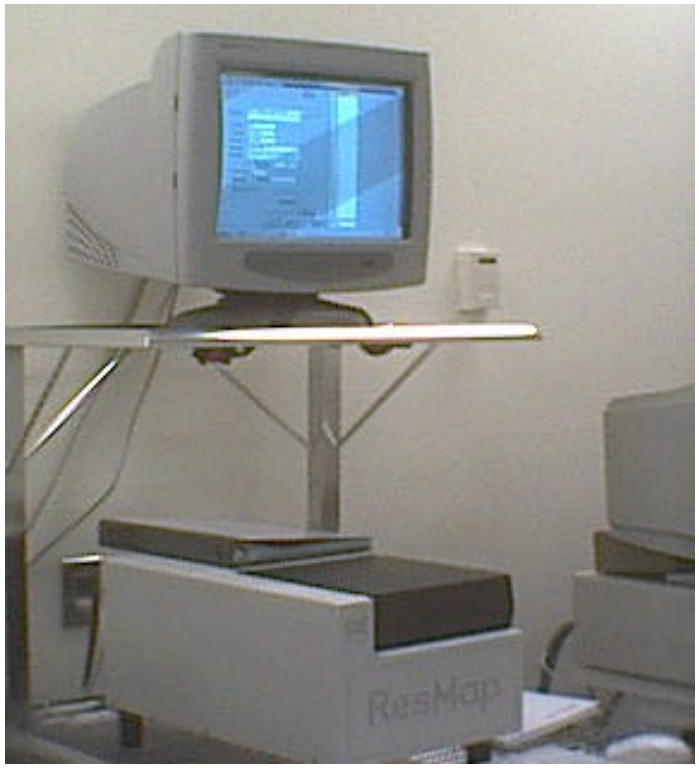
R for Research
L for Laboratory
F for Student Factory
S for Scrap or Shipped

YY is year
MM is month
DD is day

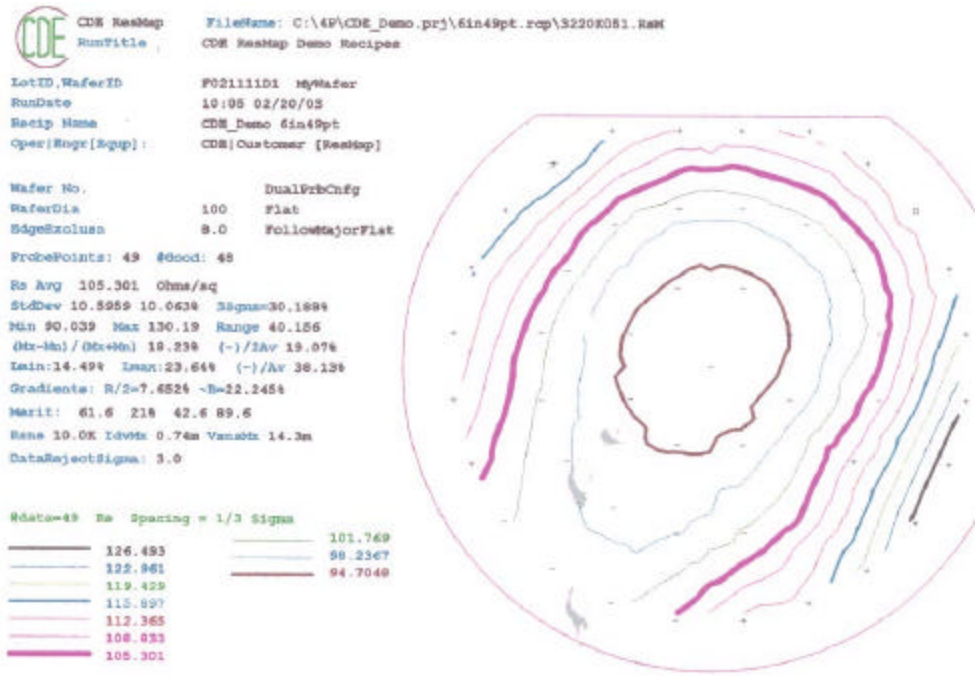
The wafer number is D1, D2, D3, etc. for device wafers or C1, C2, C3, etc. for control wafers, X1,X2 for extra wafers to replace broken D wafers

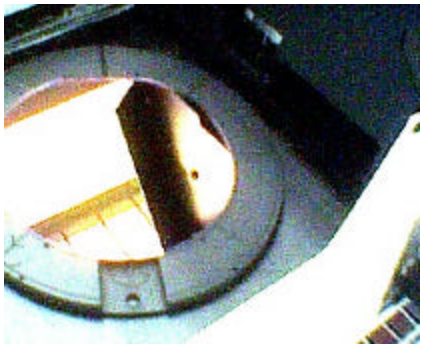


MEASURE WAFER SHEET RESISTANCE



CDE Resistivity Mapper



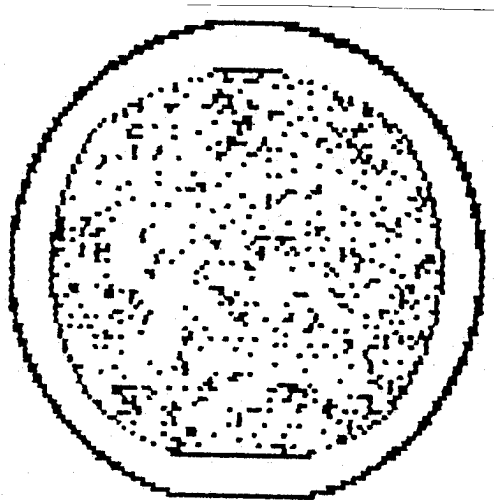


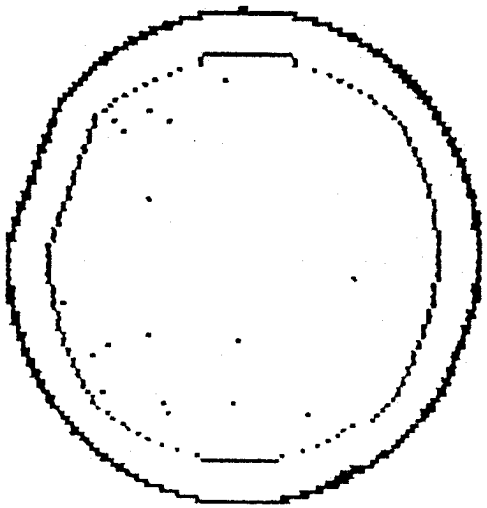
Rho=Rhos x t

TENCORE SURF SCAN

Gives total surface particle count and count in 4 bins <0.5, 0.5 to 2.0, 2.0-10, >10. Bin boundary can be selected. Edge exclusion eliminated count from near the edge of the wafer.

EXAMPLE SURFACE PARTICLE COUNT DATA





Before Cleaning (75 mm)

Size Range (µm)	Count
0.2 - 0.5	104
0.5 - 2.0	562
2.0 - 10	19
>10	2

After Cleaning (75 mm)

Size Range (µm)	Count
0.2 - 0.5	10
0.5 - 2.0	4
2.0 - 10	3
>10	0

RCA CLEAN

APM

NH_4OH - 1part
H_2O_2 - 3parts
H_2O - 15parts
70 °C, 15 min.

DI water
rinse, 5 min.

H_20 - 50
HF - 1
60 sec.

DI water
rinse, 5 min.

HPM

HCL - 1part
H_2O_2 - 3parts
H_2O - 15parts
70 °C, 15 min.

DI water
rinse, 5 min.

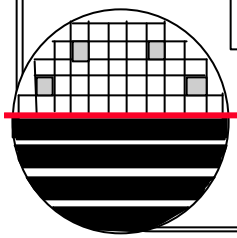
SPIN/RINSE
DRY

What does RCA stand for?

ANSWER

PLAY

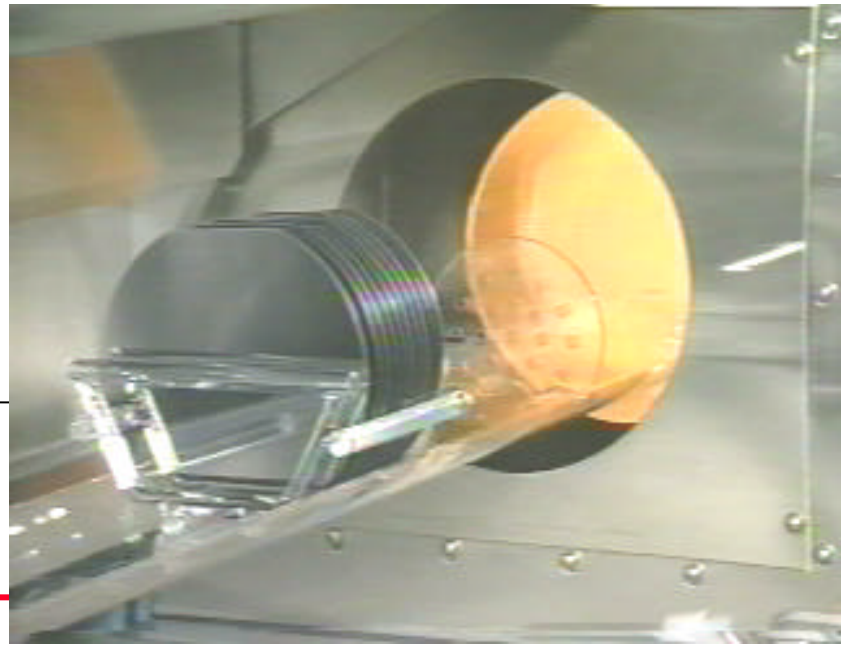
Explain the Process



RCA CLEAN AND PAD OXIDE GROWTH

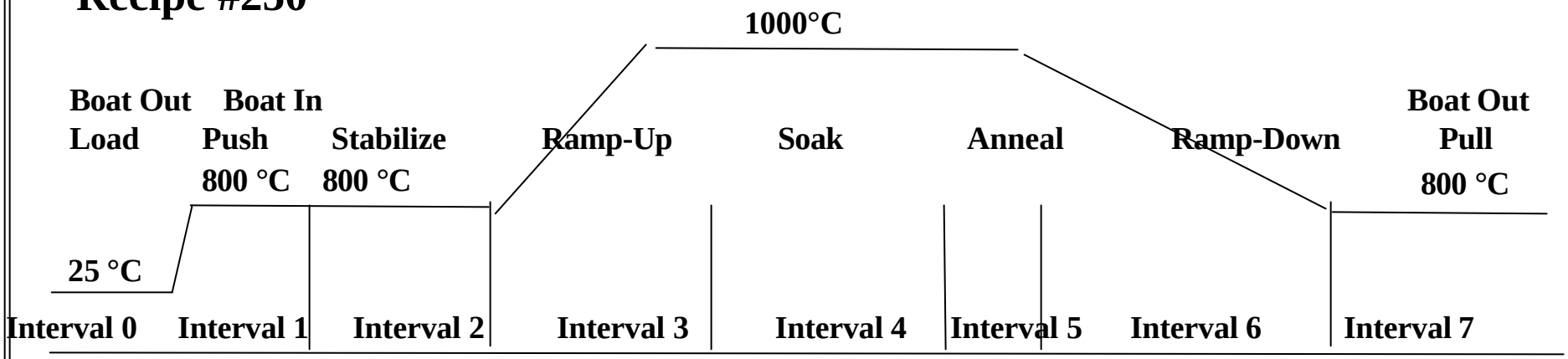
Pad Oxide, 500A
Bruce Furnace 04 Recipe 250
~45 min at 1000 °C

Substrate 10 ohm-cm



BRUCE FURNACE RECIPE 250 500Å DRY OXIDE

Recipe #250



Any	12 min	15 min	20 min	40min	5min	40 min	12 min
0 lpm	10 lpm	10 lpm	5 lpm	10 lpm	15 lpm	10 lpm	5 lpm
none	N2	N2	O2	O2	N2	N2	N2

At the end of a run the furnace returns to Interval 0 which is set for boat out, 25 °C and no gas flow. The furnace waits in that state until someone aborts the current recipe or loads a new recipe.

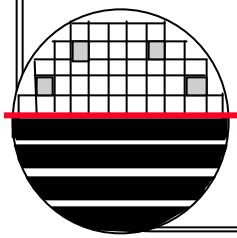
DEPOSIT SILICON NITRIDE

Recipe Nitride 810
Nitride, 1500A
LPCVD, 810C, ~30min

Substrate 10 ohm-cm

LEVEL 1 PHOTO - STI

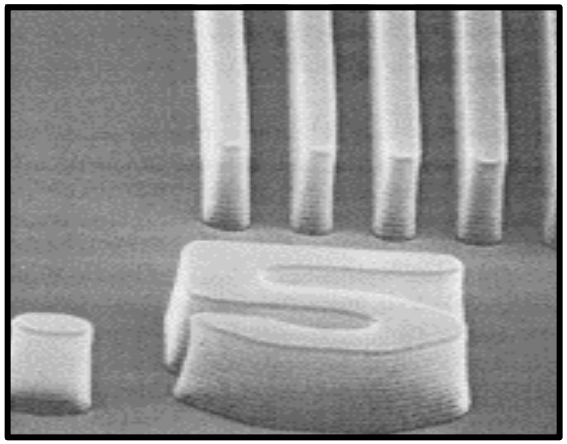
Substrate 10 ohm-cm



SSI COAT AND DEVELOP TRACK FOR 6" WAFERS

SSI coat and develop track

CANON FPA-2000 i1 STEPPER



i-Line Stepper $\lambda = 365$ nm

NA = 0.52, $\sigma = 0.6$

Resolution = $0.7\ \lambda$ / NA = ~0.5 µm

20 x 20 mm Field Size

Depth of Focus = $k_2\ \lambda/(NA)^2$

= 0.8 µm

ASML 5500/90 STEPPER

KrF Excimer Laser Stepper

λ = 248 nm

NA = 0.52, σ = 0.6

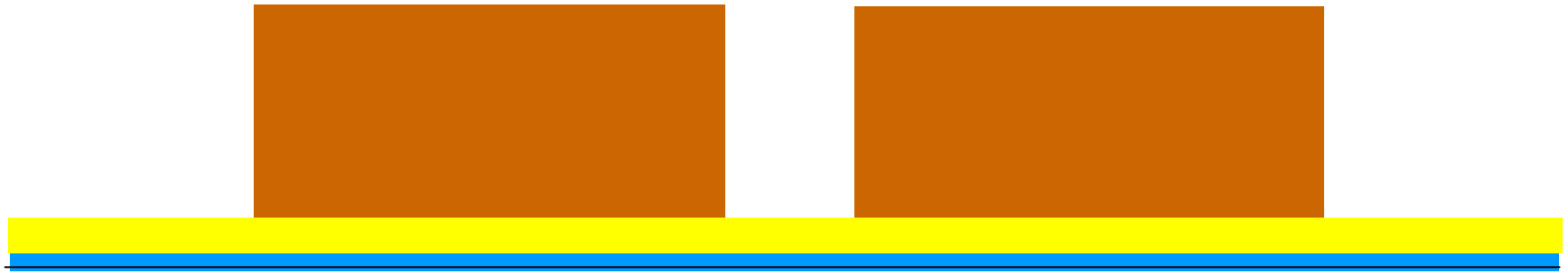
Resolution = 0.7 λ / NA = ~0.3 µm

20 x 20 mm Field Size

Depth of Focus = $k_2 \lambda/(NA)^2$

~ 0.64 µm

PLASMA ETCH NITRIDE/OXIDE/SILICON



STI Etch: SF_6 plasma

LAM 490 Etcher, Etch Rate ~1000 Å/min for Nitride

~ 500 Å/min for Oxide

~ 5000 Å/min for silicon

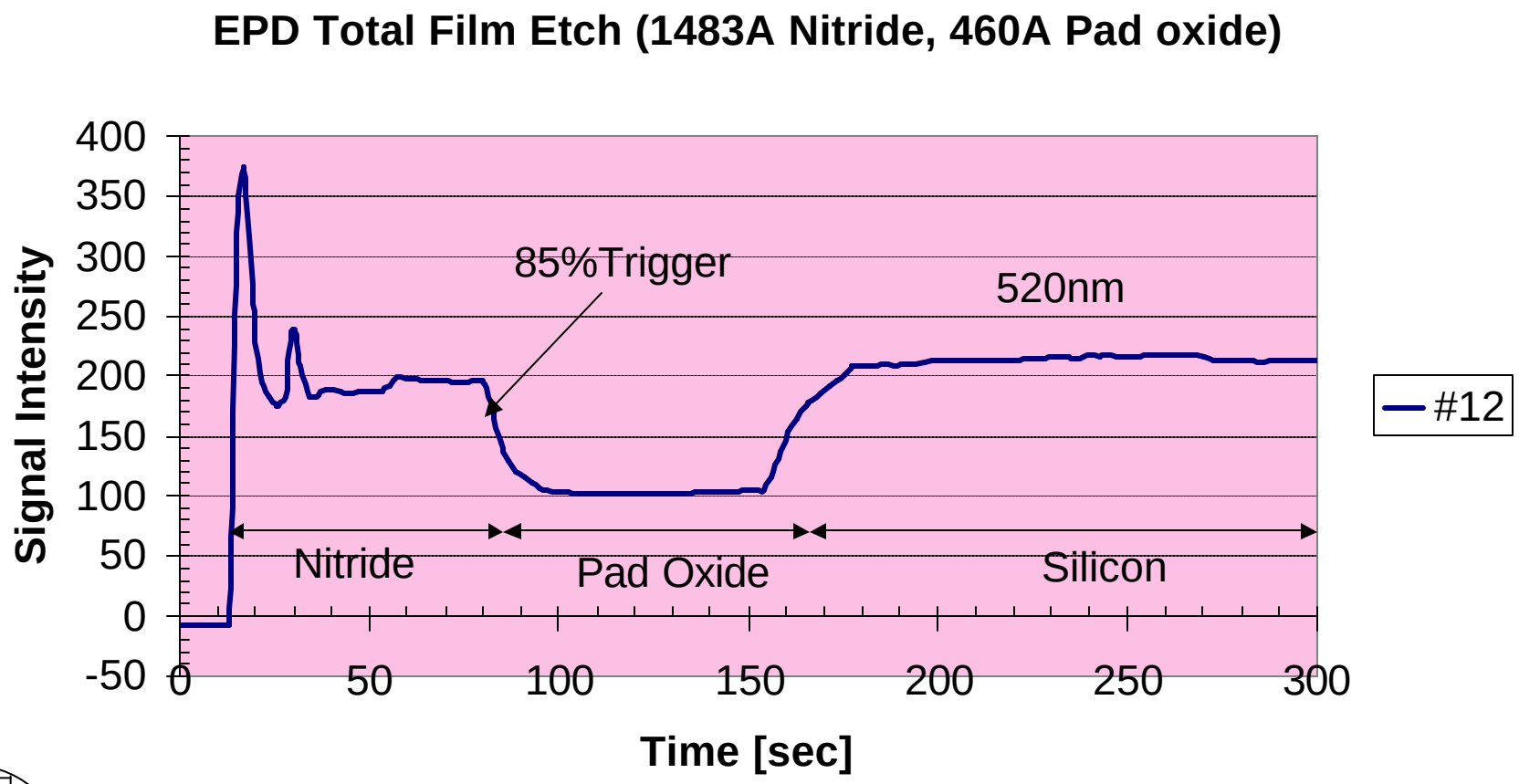
Substrate 10 ohm-cm

PLASMA ETCH TOOL

Lam 490 Etch Tool
Plasma Etch Nitride (~ 1500 Å/min)
SF6 flow = 200 sccm
Pressure= 260 mTorr
Power = 125 watts
Time=thickness/rate

Use end point detection capability
This system has filters at 520 nm and 470 nm. In any case the color of the plasma goes from pink/blue to white/blue once the nitride is removed.

LAM 490 END POINT



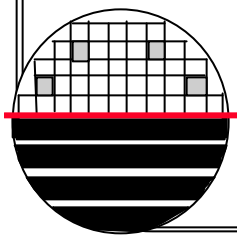
APPROACH FOR STI END POINT DETECTION

Step 1
Flow Gas
Set Pressure
No RF Power

Step 2
RF Power On
Nitride
Endpoint

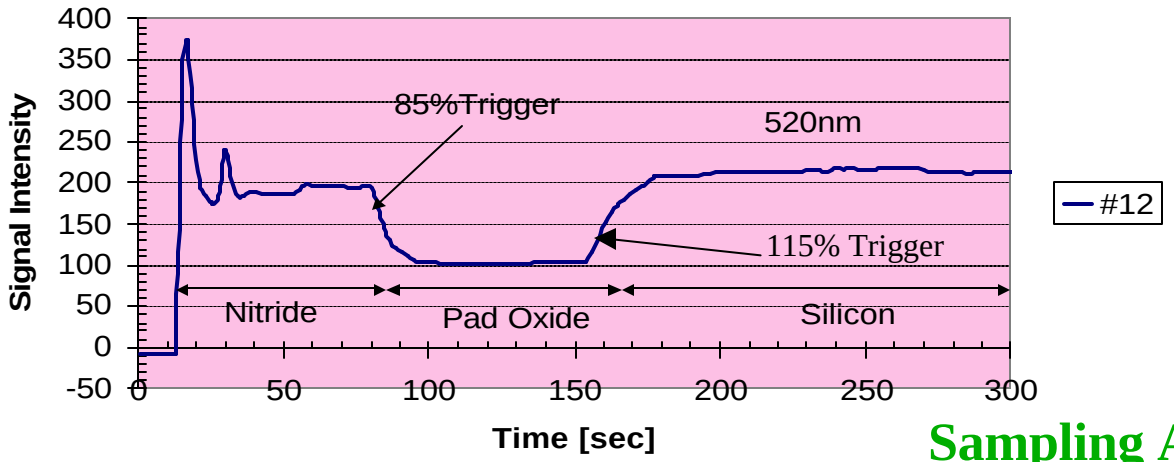
Step 3
RF Power On
Oxide
Endpoint

Step 3
RF Power On
Timed
Silicon Etch



SELECTING LAM 490 END POINT PARAMETERS

EPD Total Film Etch (1483A Nitride, 460A Pad oxide)



Nitride Etch (Step 2)
If no Endpoint is found then
Max Etch Time 100 sec

Sampling A only [520nm ch 12]
Active during Step 2
Delay 50 sec before normalizing
Normalize for 10 sec
Trigger @ 85% of normalized value

Oxide Etch (Step 3)
If no Endpoint is found then
Max Etch Time 50 sec

Sampling A only [520nm ch 12]
Active during Step 3
Delay 30 sec before normalizing
Normalize for 10 sec
Trigger @ 115% of normalized value

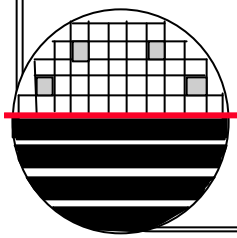
FINALIZE STI ETCH RECIPE

Process: Step 1 –
260mTorr; 0 watts
200sccm SF6,
Max Time = 2 min
Time Only

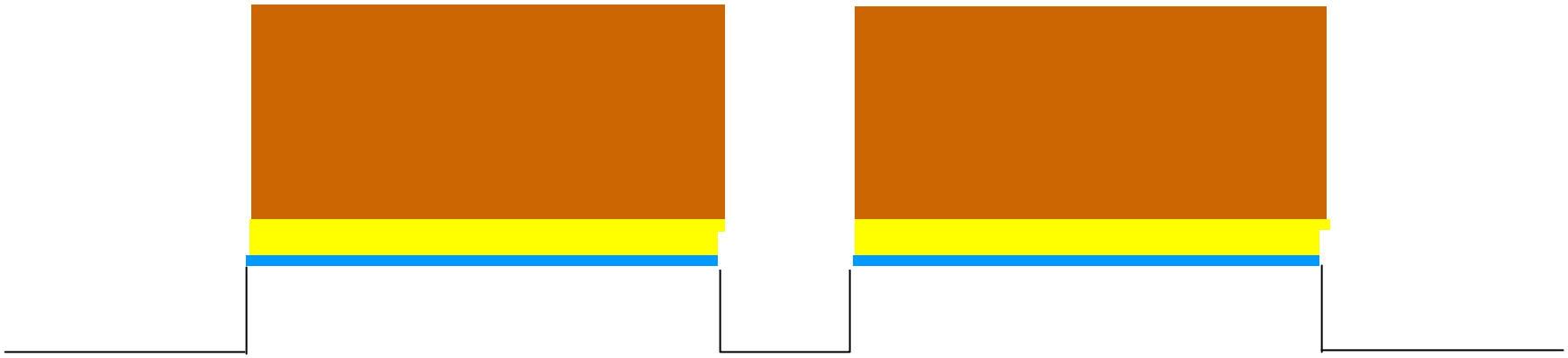
Process: Step 2 –
260mTorr; 125 watts,
200sccm SF6,
Max Time = 1min 40sec
Endpoint and Time
Sampling A (ch12 @ 520nm)
Active during step 02
Delay 50sec before normalizing
Normalize for 10sec
Trigger at 85%

Process: Step 3 –
260mTorr; 125 watts,
200sccm SF6,
Max Time = 50sec
Endpoint and Time
Sampling A (ch12 @ 520nm)
Active during step 03
Delay 30sec before normalizing
Normalize for 10sec
Trigger at 115%

Process: Step 4 –
260mTorr; 125W,
200sccm SF6,
Time Only,
Max Time = 50 sec



CONTINUE THE ETCH THRU PAD OXIDE AND INTO THE SILICON



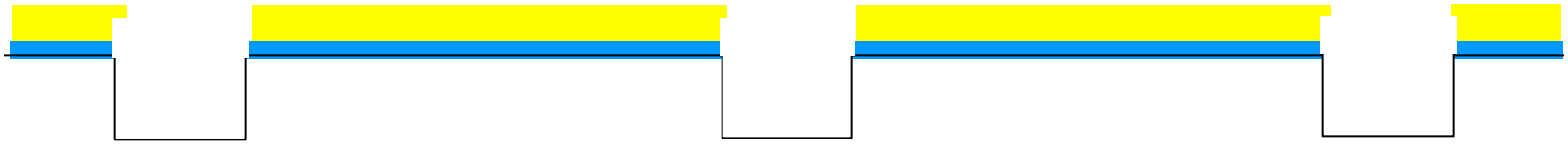
Substrate 10 ohm-cm

MEGASONIC RCA CLEAN, SRD & ASHER

RCA Clean Bench

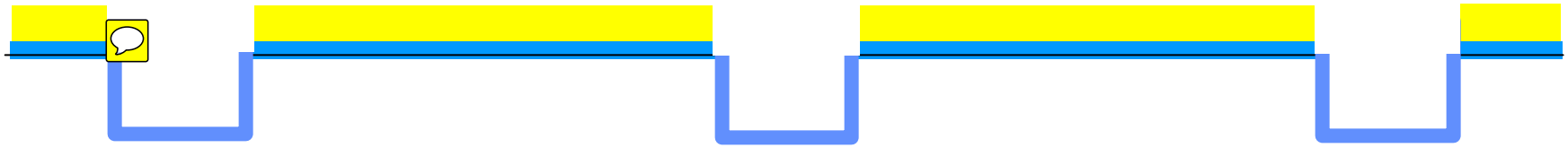
Asher

STRIP RESIST AND RCA CLEAN



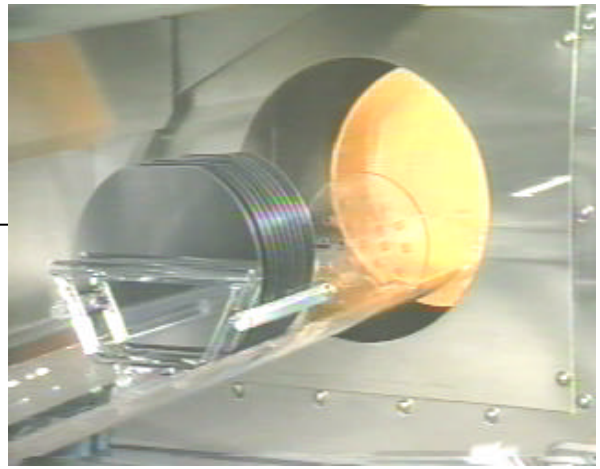
Substrate 10 ohm-cm

GROW TRENCH LINER OXIDE



Pad Oxide, 500A
Bruce Furnace 04 Recipe 250

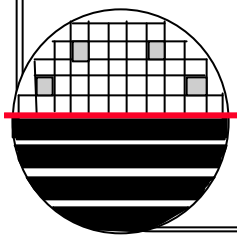
Substrate 10 ohm-cm



DEPOSIT LTO TRENCH FILL

Substrate 10 ohm-cm

Fill 4000 Å trench
Deposit 6000 Å LTO



PECVD OXIDE FROM TEOS

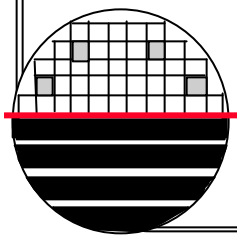
TEOS Program: (Chamber A)
Step 1
- Setup Time = 15 sec
- Pressure = 9 Torr
- Susceptor Temperature= 390 C
- Susceptor Spacing= 220 mils
- RF Power = 0 watts
- TEOS Flow = 400 scc
- O2 Flow = 285 scc

Step 2 – Deposition
- Dep Time = 55 sec (5000 Å)
- Pressure = 9 Torr
- Susceptor Temperature= 390 C
- Susceptor Spacing= 220 mils
- RF Power = 205 watts
- TEOS Flow = 400 scc
- O2 Flow = 285 scc

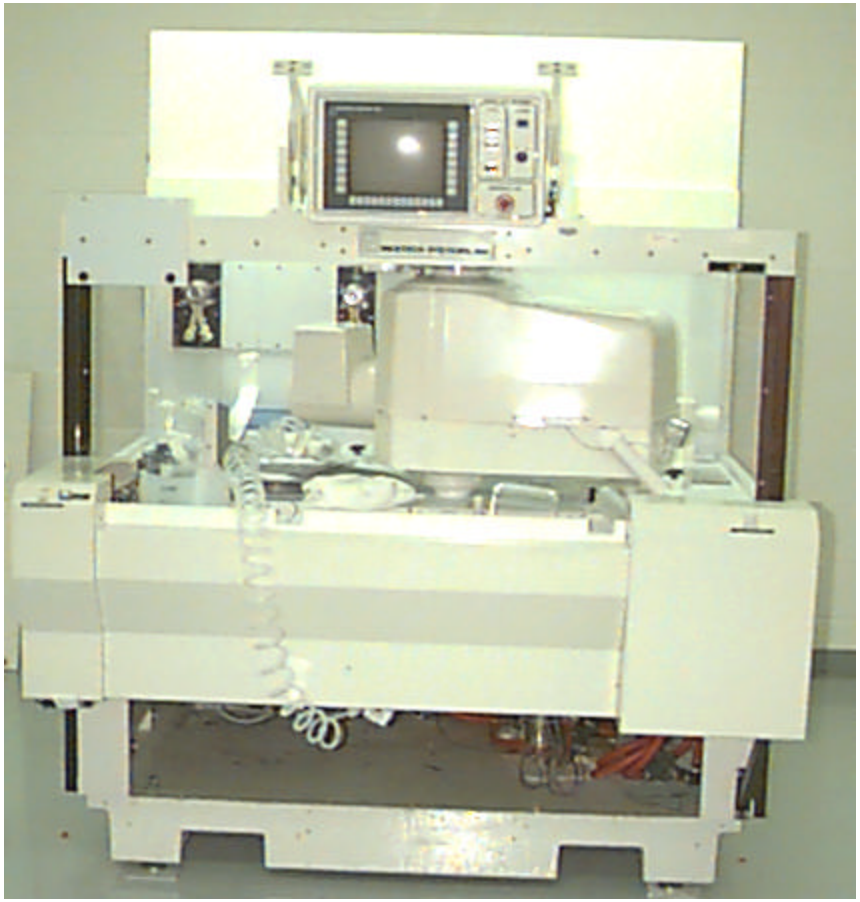
Step 3 – Clean
- Time = 10 sec
- Pressure = Fully Open
- Susceptor Temperature= 390 C
- Susceptor Spacing= 999 mils
- RF Power = 50 watts
- TEOS Flow = 0 scc
- O2 Flow = 285 scc

CMP

Substrate 10 ohm-cm



CMP TOOL

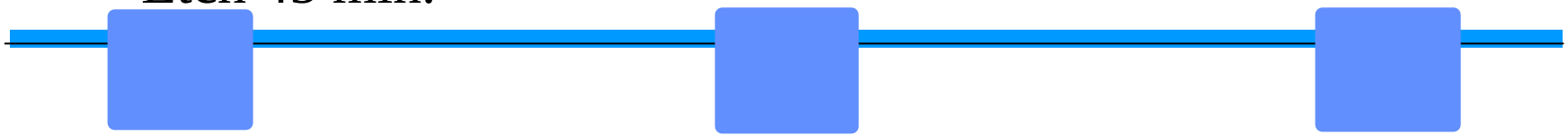


CMP CLEAN

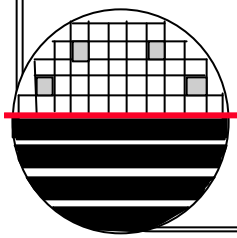
Substrate 10 ohm-cm

HOT PHOSPHORIC ACID NITRIDE ETCH

30 Dip in BHF, Rinse
Hot Phosphoric Acid
Wet Nitride Etch.
Etch Rate ~80 Å/min
Etch 45 min.



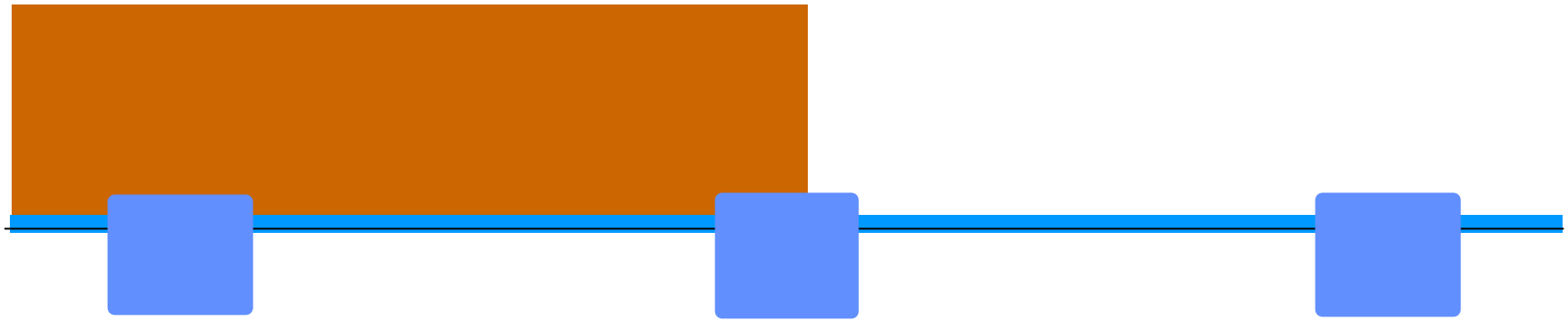
Substrate 10 ohm-cm



HOT PHOSPHORIC ACID ETCH BENCH

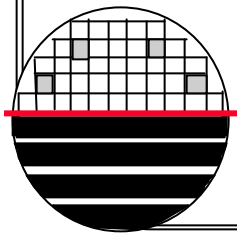
- Include D1-D3
- Warm up Hot Phos pot to 175º
- Use Teflon boat to place wafers in acid bath
  - 3500Å +/-500 → 90 minutes
  - 1500Å +/- 500 → 45 minutes
  - Etch rate of ~80 Å/min
- Rinse for 5 minutes in Cascade Rinse
- SRD wafers

PHOTO 2 N-WELL

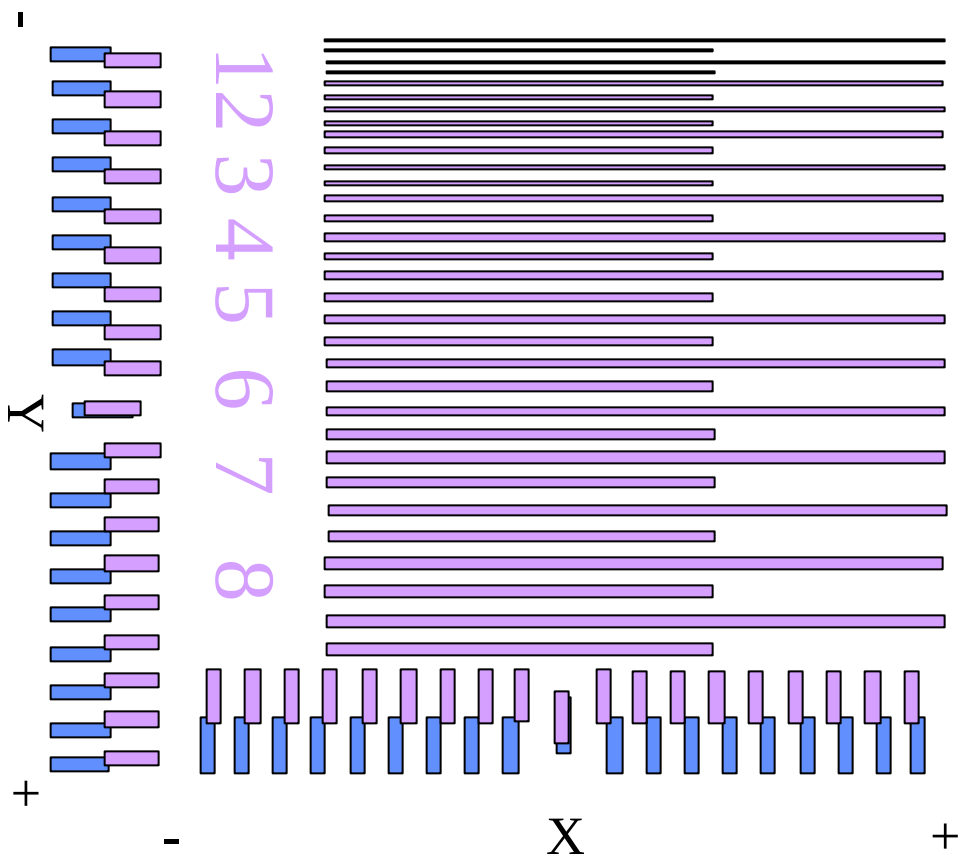


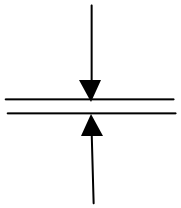
Need thicker resist

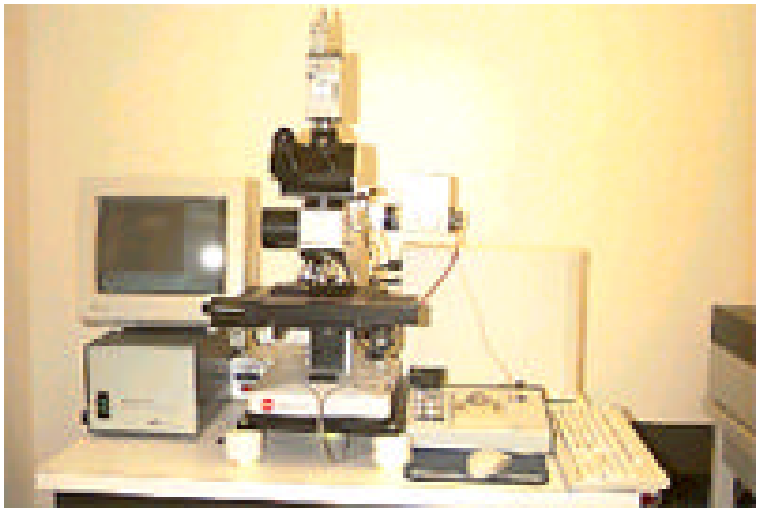
Use COATMTL.RCP (2000rpm, 30 sec gives 1.3µm)
and DEVMTL.RCP (~75 seconds)



ALIGNMENT VERNIERS
CRITICAL DIMENSION (CD) STRUCTURES

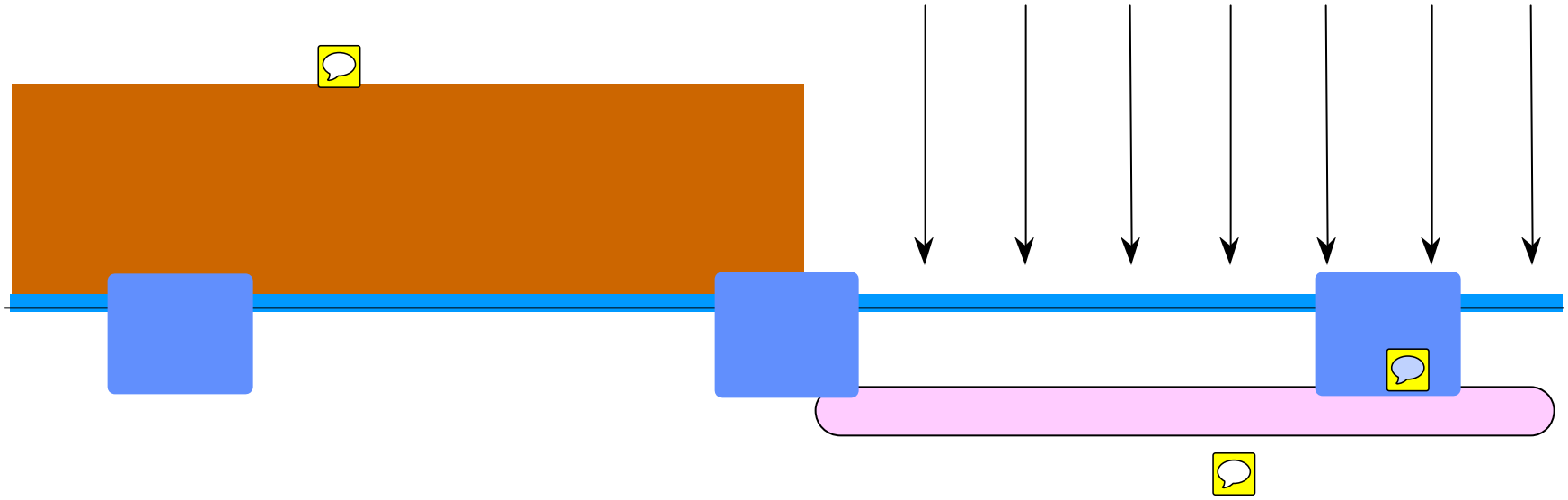






PLAY

N-WELL IMPLANT

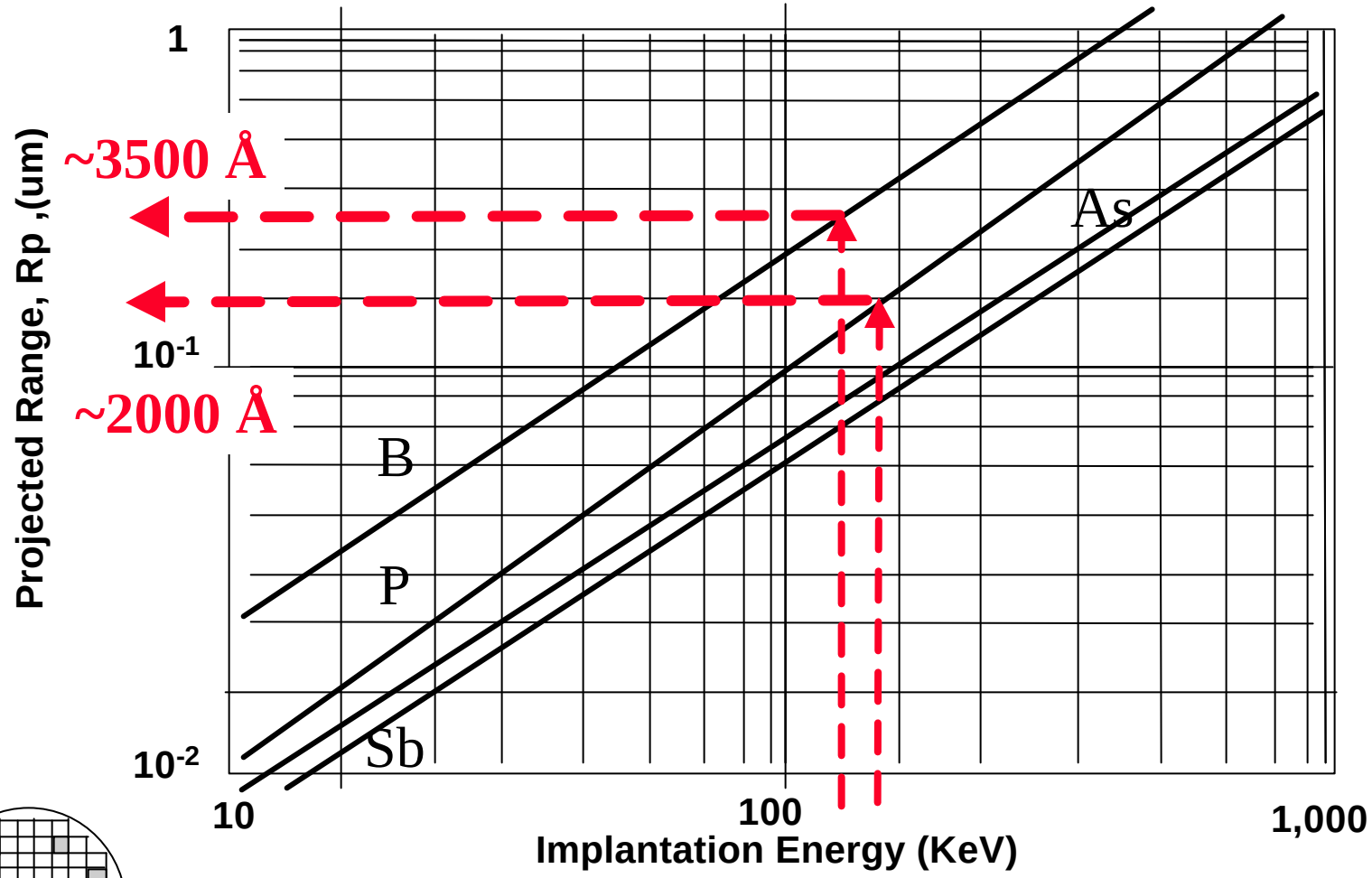


3e13, 180keV, P_{31}

Substrate 10 ohm-cm

VARIAN 350 D ION IMPLANTER (4" AND 6" WAFERS)

ION IMPLANT RANGE CHART



IMPLANT MASKING THICKNESS CALCULATOR

Rochester Institute of Technology					Lance Barron		
Microelectronic Engineering					Dr. Lynn Fuller		
11/20/04							

IMPLANT MASK CALCULATOR **Enter 1 - Yes 0 - No in white boxes**

DOPANT SPECIES

B11	0
BF2	0
P31	1

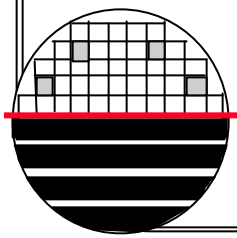
MASK TYPE

Resist	0
Poly	0
Oxide	1
Nitride	0

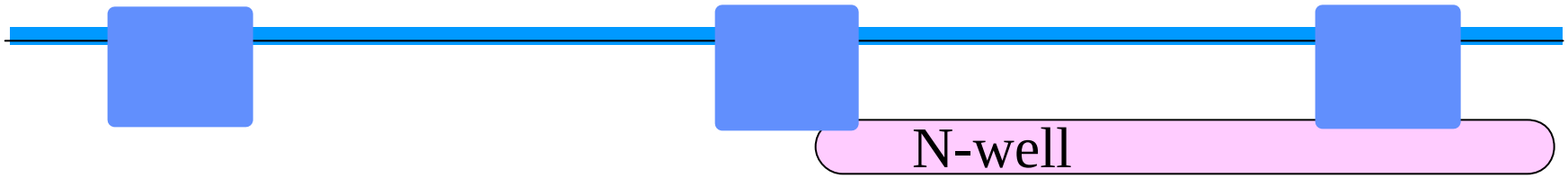
ENERGY

180 KeV

Thickness to Mask >1E15/cm3 Surface Concentration 5396.537 Angstroms

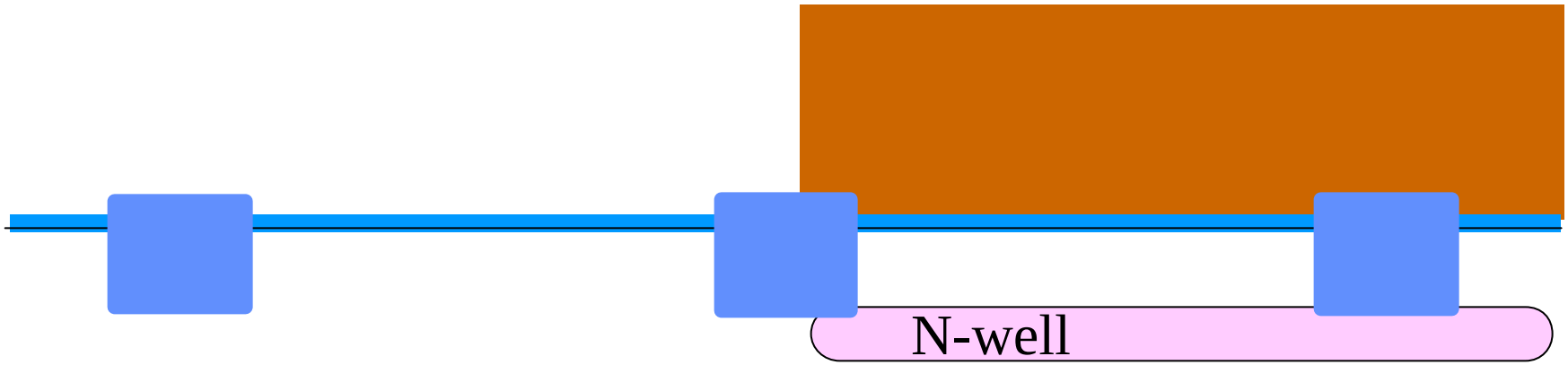


STRIP RESIST



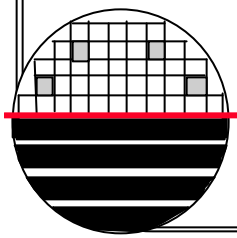
Substrate 10 ohm-cm

PHOTO 3 P-WELL

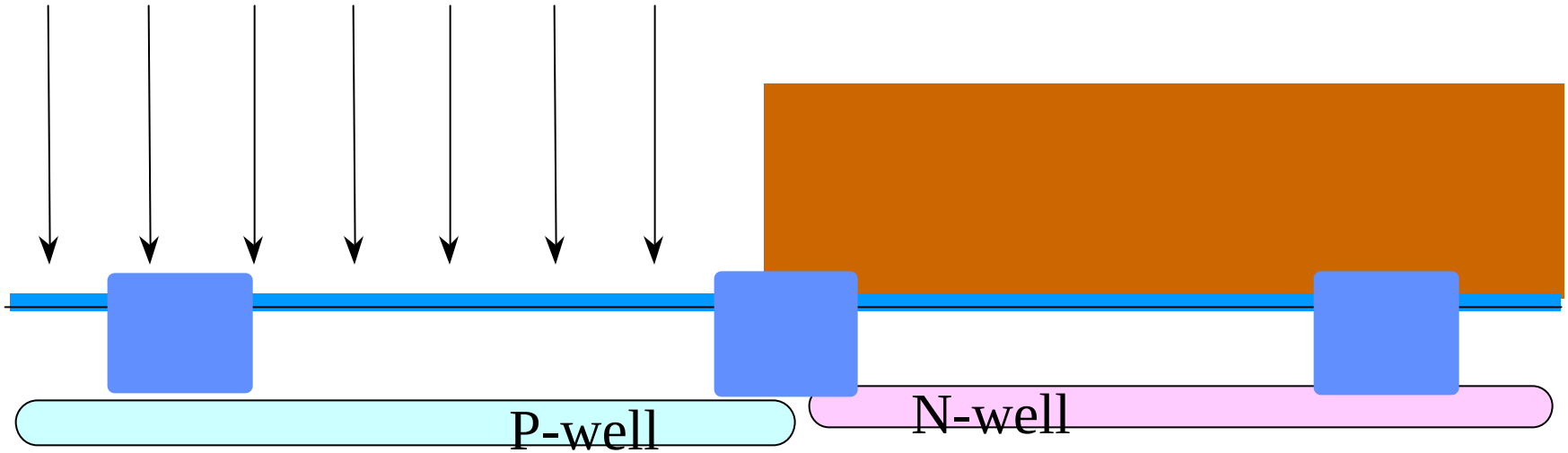


Need thicker resist

Use COATMTL.RCP (2000rpm, 30 sec gives 1.3µm)
and DEVMTL.RCP (~75 seconds)



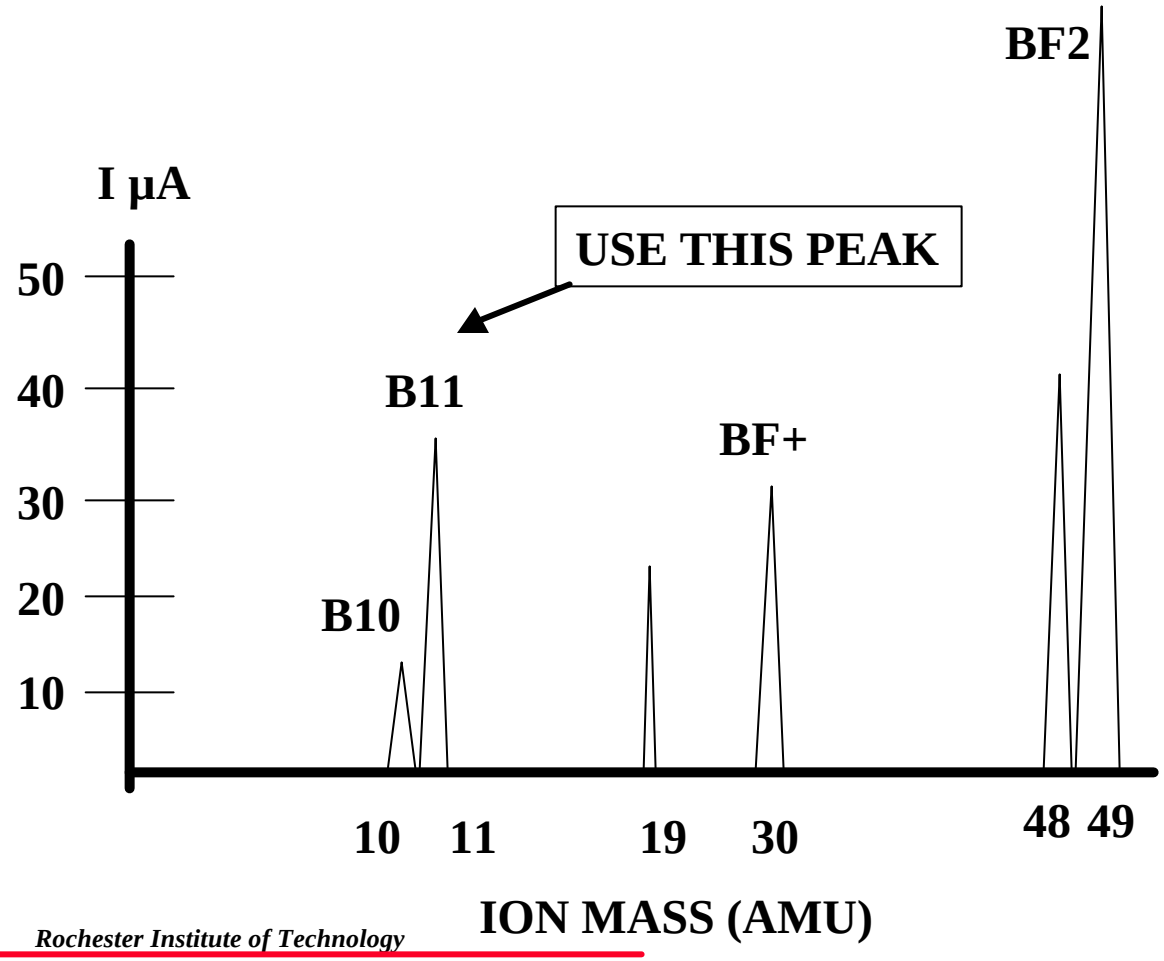
ION IMPLANT P-WELL



3e13, 125keV, B_{11}

Substrate 10 ohm-cm

B_{11} IMPLANT FOR BORON THRESHOLD ADJUSTS, STOP, P-WELL



PLAY

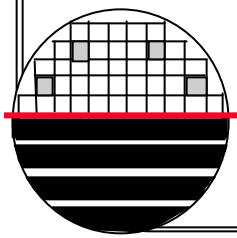
IMPLANT MASKING THICKNESS CALCULATOR

Rochester Institute of Technology				Lance Barron	
Microelectronic Engineering				Dr. Lynn Fuller	
11/20/04					

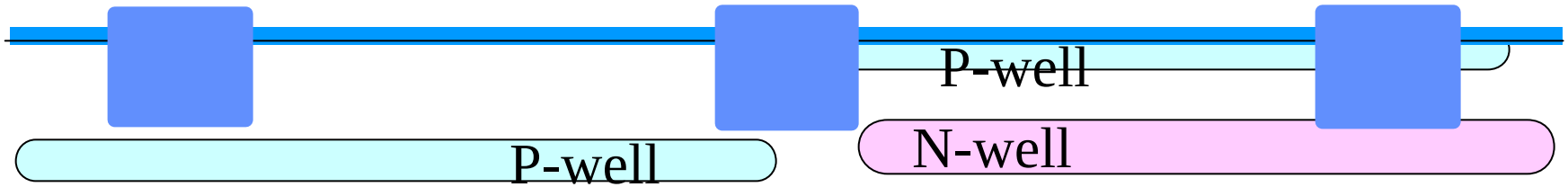
IMPLANT MASK CALCULATOR **Enter 1 - Yes 0 - No in white boxes**

DOPANT SPECIES		**MASK TYPE**		**ENERGY**	
B11	1	Resist	0	125	KeV
BF2	0	Poly	0		
P31	0	Oxide	1		
		Nitride	0		

Thickness to Mask >1E15/cm3 Surface Concentration 5371.71 Angstroms



STRIP RESIST AND RCA CLEAN



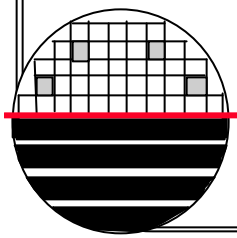
3e13, 150keV, B_{11}

Substrate 10 ohm-cm

Big Problem

ALTERNATIVE APPROACH FOR WELL FORMATION IN ADVANCED CMOS PROCESS

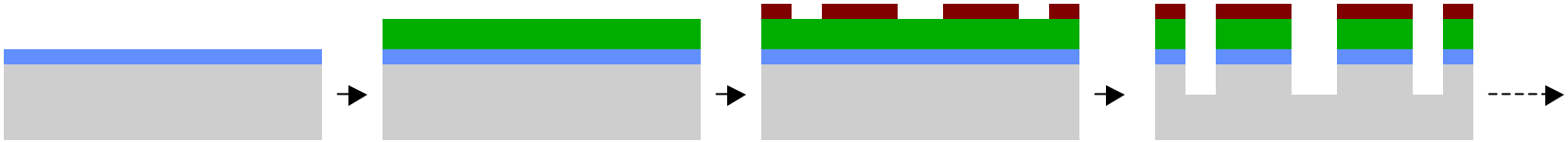
The current Adv-CMOS process calls for ion implanting the well through the filled trenches. This requires exact trench depths, exact CMP stop, and high energy implants. The normal photoresist is not thick enough to block these high energy implans, 180KeV for P31 and 150KeV for B11. This project investigated implanting the wells prior to trench fill and CMP. Using SILVACO ATHENA simulations a set of implant conditions was determined to give a well with the correct surface concentration, well junction depth and sheet resistance. The wells also need to be continuous under the trench isolation so that several devices can be placed in a single well with a single well potential. In addition our ion implanter has difficulty at high energy so lower energy implants would be useful.



Jonathan Reese

February 22, 2005

ORIGINAL ADV-CMOS PROCESS FLOW

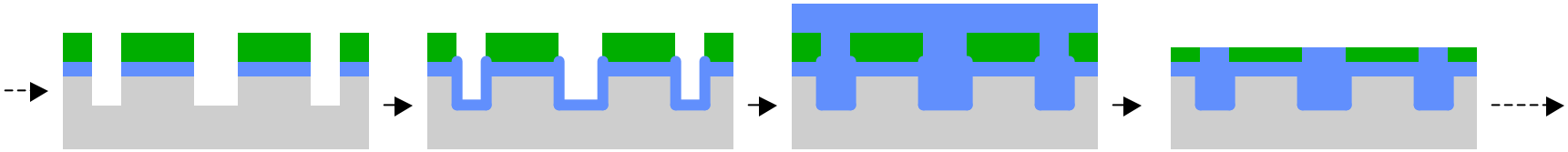


500Å Pad Ox.
-Bruce Tube 4

1500Å CVD Nitride
-LPCVD

STI Litho- level 1

4000Å Plasma etch
-Lam 490

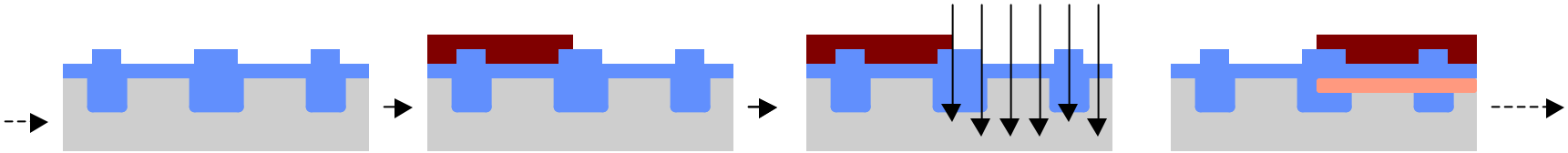


PR Ash
RCA Clean

500Å Pad Oxide
-Bruce Tube 1

CVD Trench fill- P-5000
Anneal –Bruce Tube 1

Trench CMP
CMP Clean

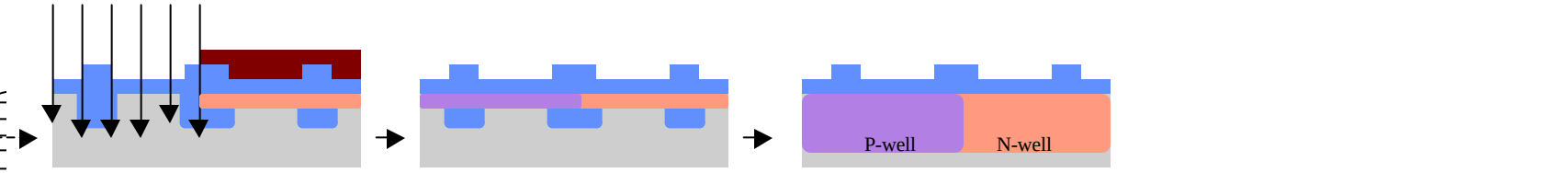


RCA Clean
Hot Phos. Nitirde strip

N-well Litho
-Level 2

N-well implant
-P31, 3E13 cm^{-2} E=180KeV

Ash
P-well Litho - level 3

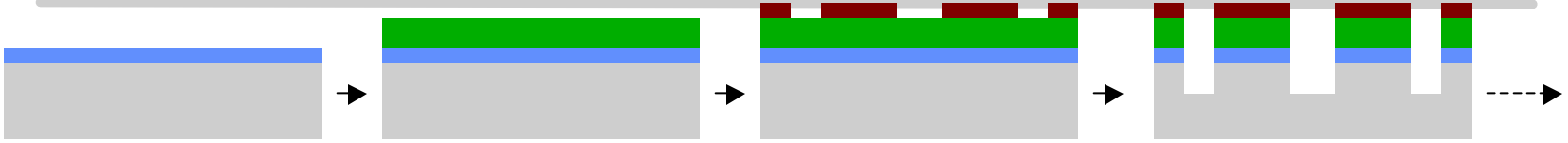


P-well implant
-B11, 3E13 cm^{-2} E=150KeV

Ash, RCA clean
Drive in- 6hr 1100C-Tube 1

X_j approx. 3 µm

PROPOSED ADV-CMOS PROCESS FLOW



500Å Pad Ox.

-Bruce Tube 4

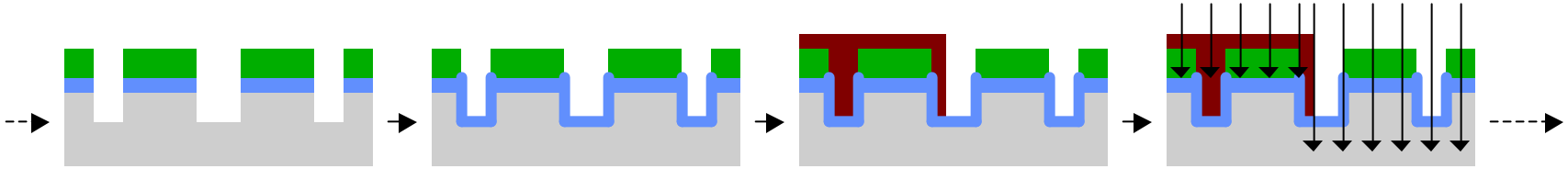
1500Å CVD Nitride

-LPCVD

STI Litho- level 1

4000Å Plasma etch

-Lam 490



PR Ash

RCA Clean

500Å Pad Oxide

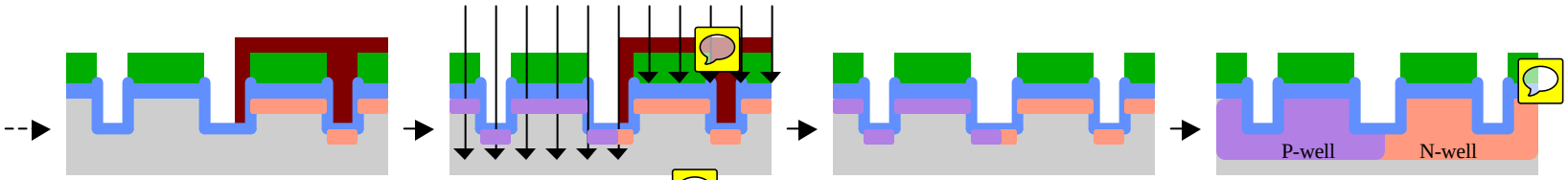
-Bruce Tube 1

N-well Litho

-Level 2

N-well implant

-P31, 8e13 cm^{-2} E=80 KeV



P-well Litho

-Level 3

P-well implant

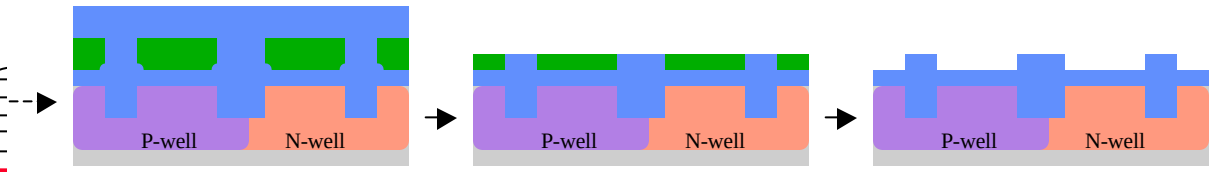
-B11, 3e13 cm^{-2} E=170 KeV

PR Ash

RCA Clean

Drive in- 6hr 1100℃-Tube 1

X_j approx. 3 µm



CVD Trench fill- P-5000

Anneal –Bruce Tube 1

Trench CMP

CMP Clean

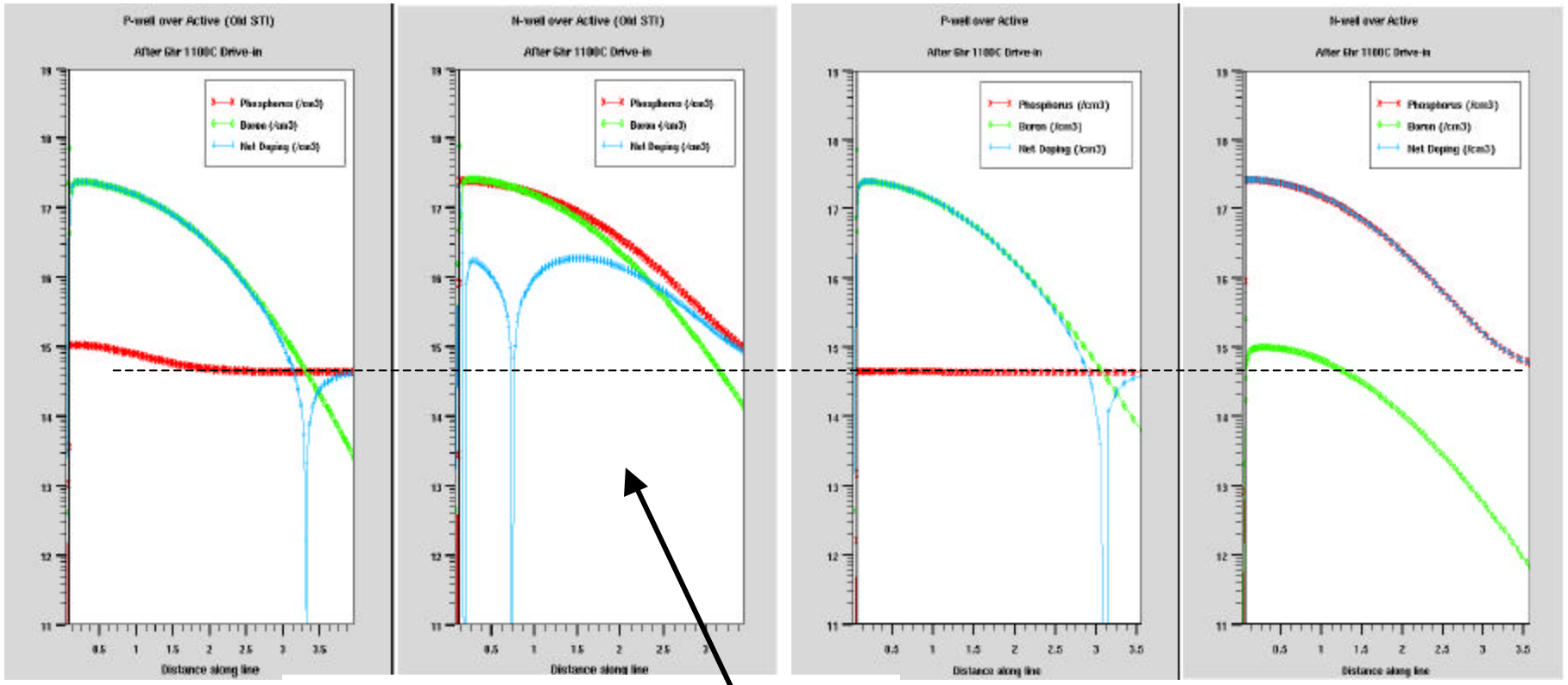
RCA Clean

Hot Phos. Nitirde strip

SIMULATION: ORIGINAL PROCESS WELL PROFILES

Current Process

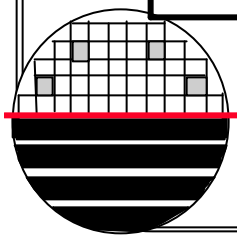
Proposed Process



Problems with Boron Penetration of Masking Resist

WELL PARAMETERS

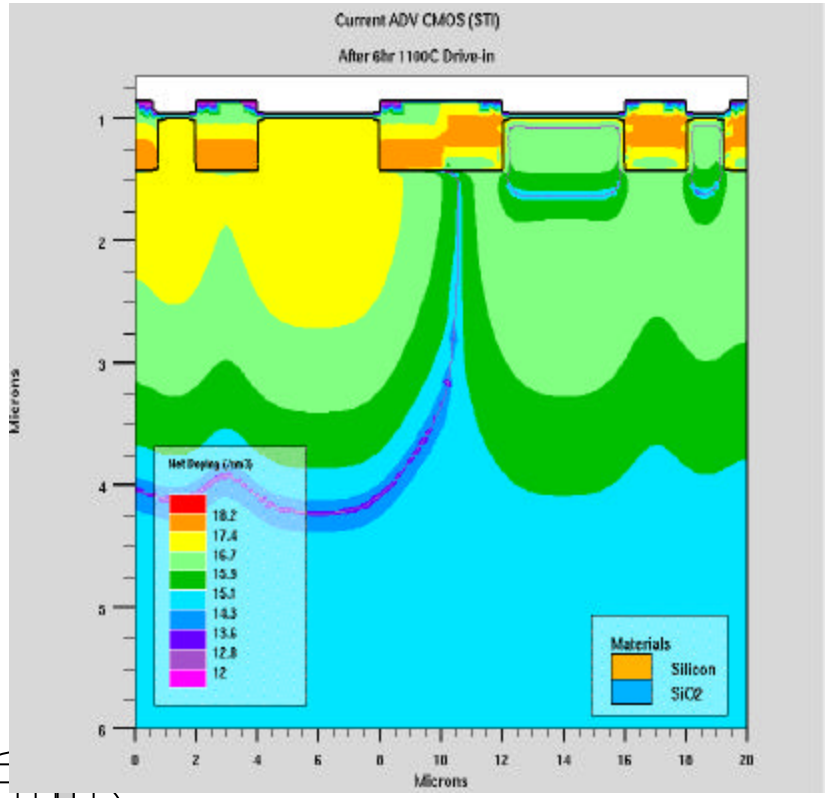
	Design Parameters	Old Process Simulation	New Process Simulation	
N well				
Dose	3E13	3E13	3E13	
Energy		180	170	Lower
Surface Conc.	~1E17	2.4E17	1.08E17	Better
N well Xj	~3.0	4.0#	3.5	Better
P well				
Dose	3E13	3E13	8E13	
Energy		150	80	Lower
Surface Conc.	~1E17	3.6E16	1.0E17	Better
P well Xj	~3.0	3.3	3.1	Better



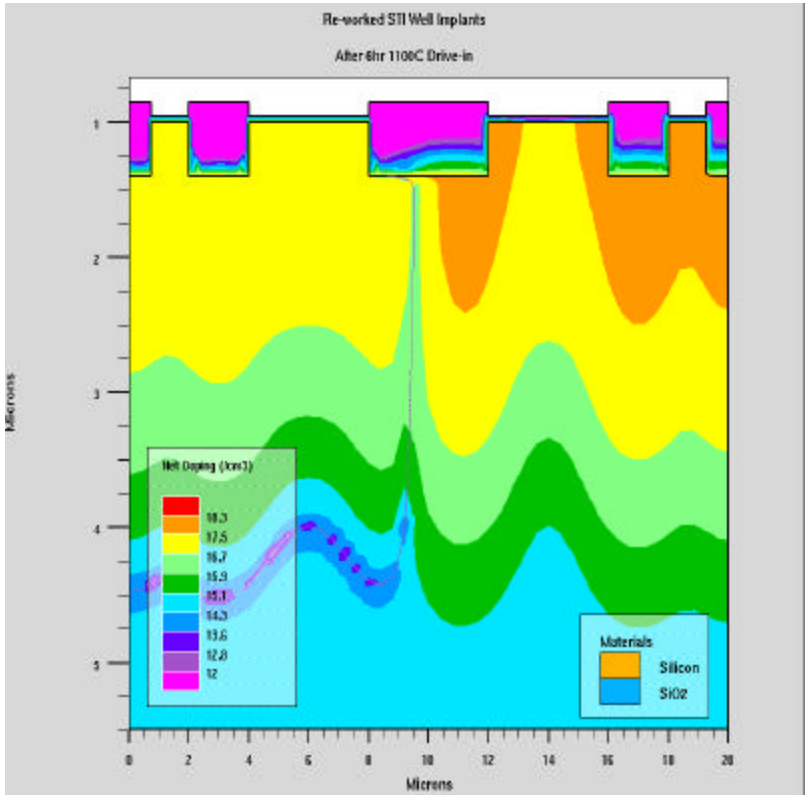
If Boron penetration into N-well can be eliminated

SIMULATION: PROCESS CROSS-SECTION

Current Process

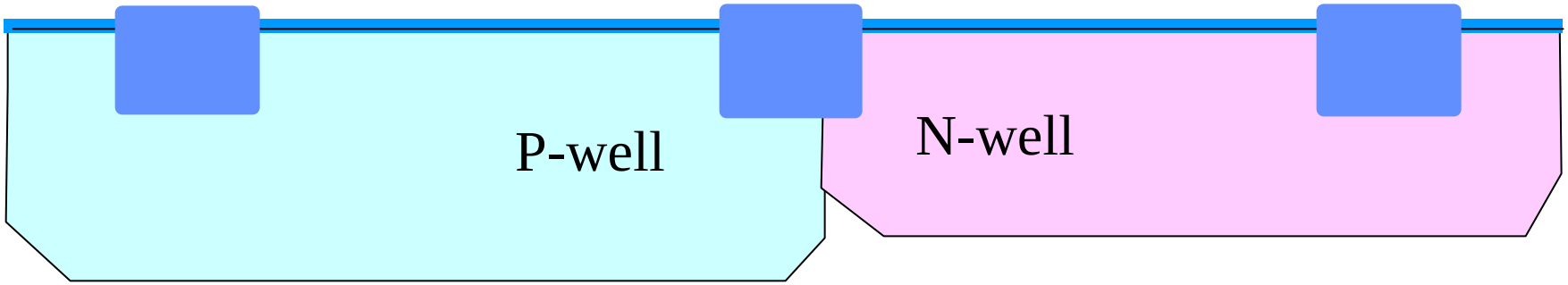


Proposed Process



WELL DRIVE

6 hrs, 1100 °C

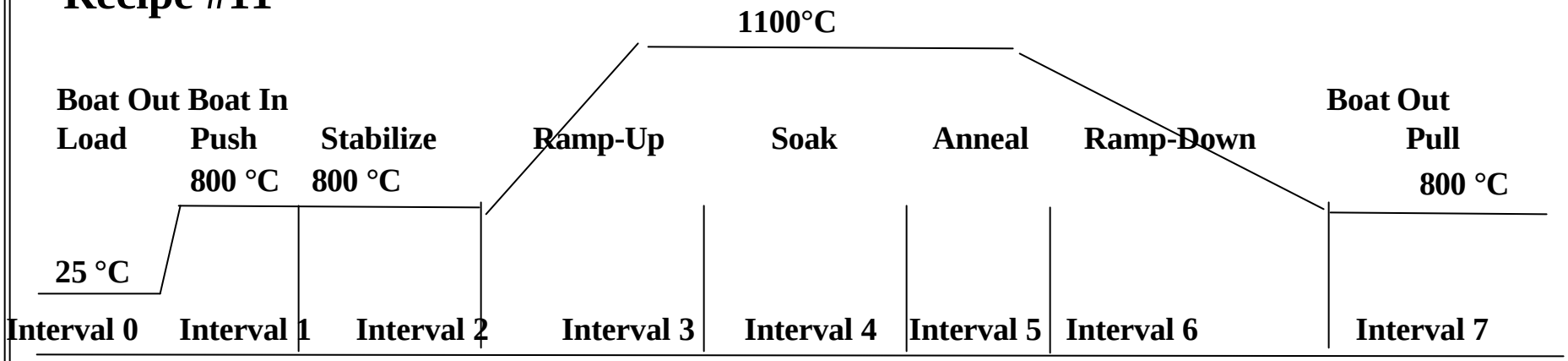


Substrate 10 ohm-cm

BRUCE FURNACE RECIPE 11 ADV-CMOS WELL DRIVE

Verified:12-8-04

Recipe #11

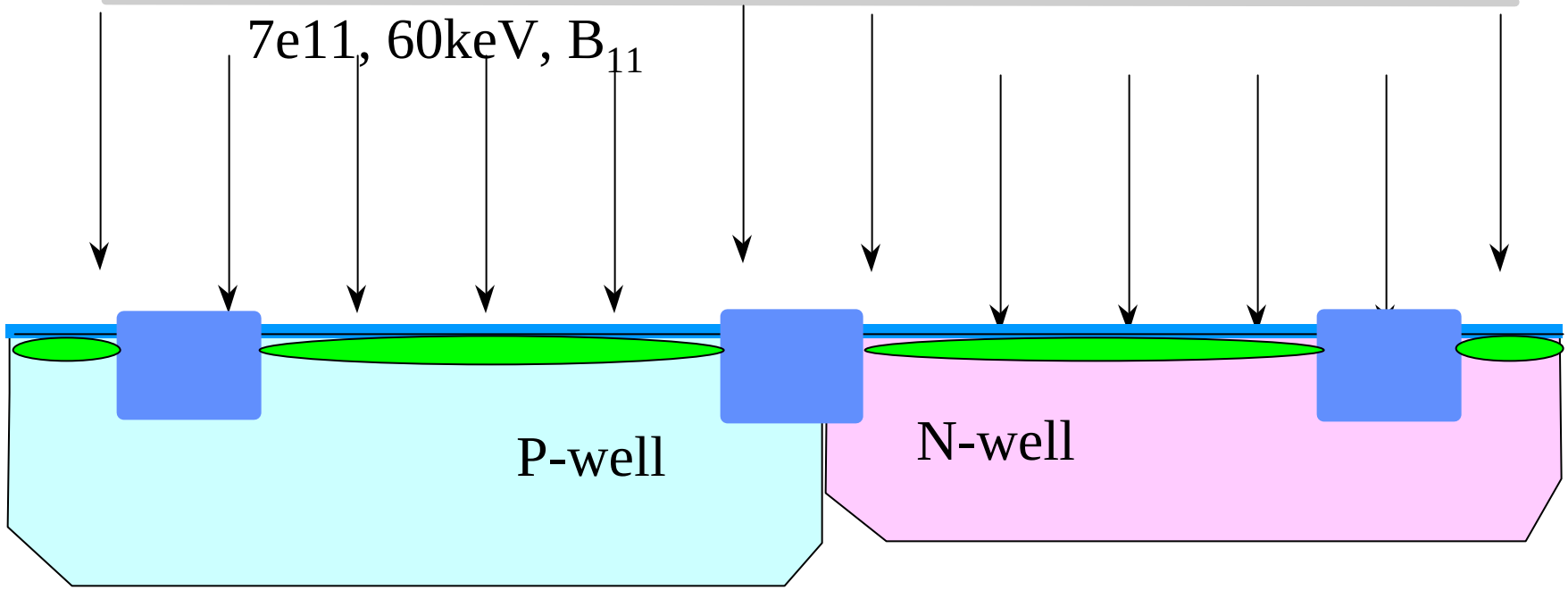


Any	12 min	15 min	30 min	360 min	5 min	60 min	12 min
0 lpm	10 lmp	10 lpm	10 lpm	10 lpm	10 lpm	10 lpm	5 lpm
none	N2	N2	N2	N2	N2	N2	N2

At the end of a run the furnace returns to Interval 0 which is set for boat out, 25 °C and no gas flow. The furnace waits in that state until someone aborts the current recipe or loads a new recipe.

Sub-CMOS Well Drive, No Oxide Growth, Tube 1

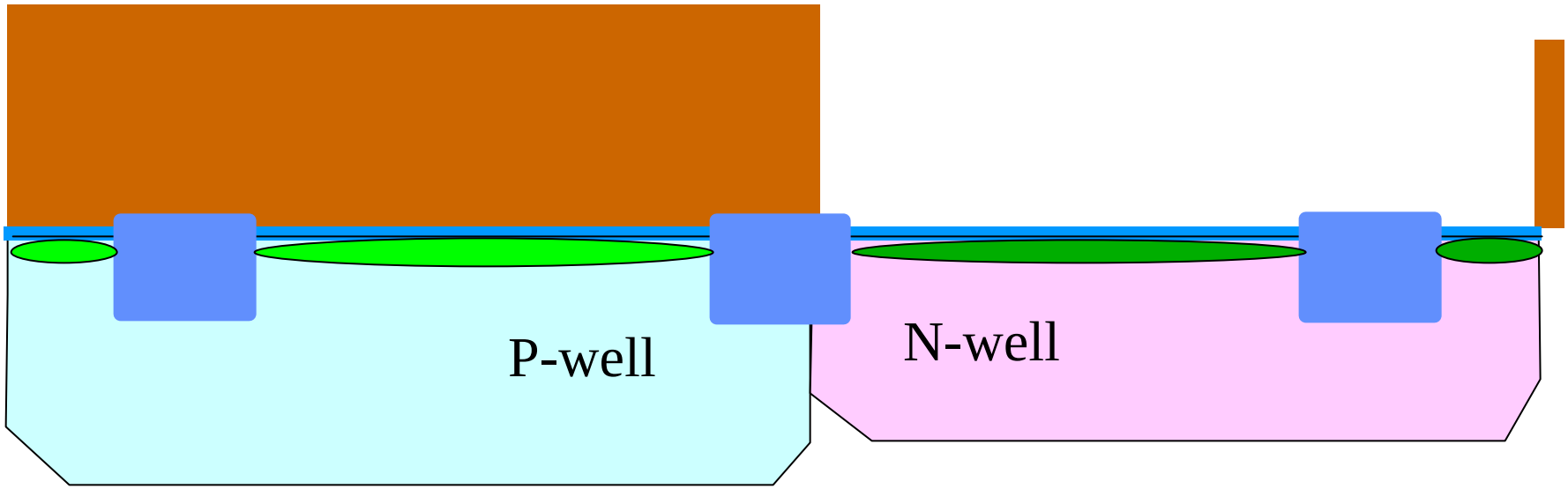
BLANKET PMOS & NMOS VT ADJUST IMPLANT



Substrate 10 ohm-cm

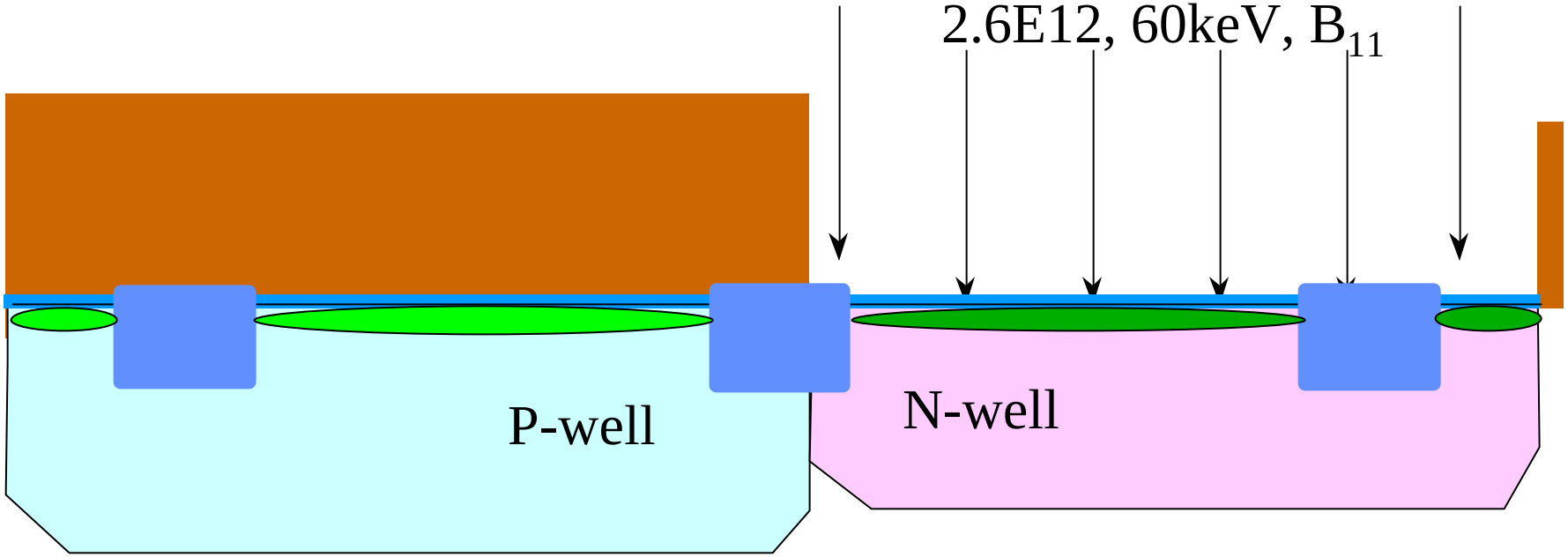
Note: This implant may be omitted

PHOTO 4 PMOS VT



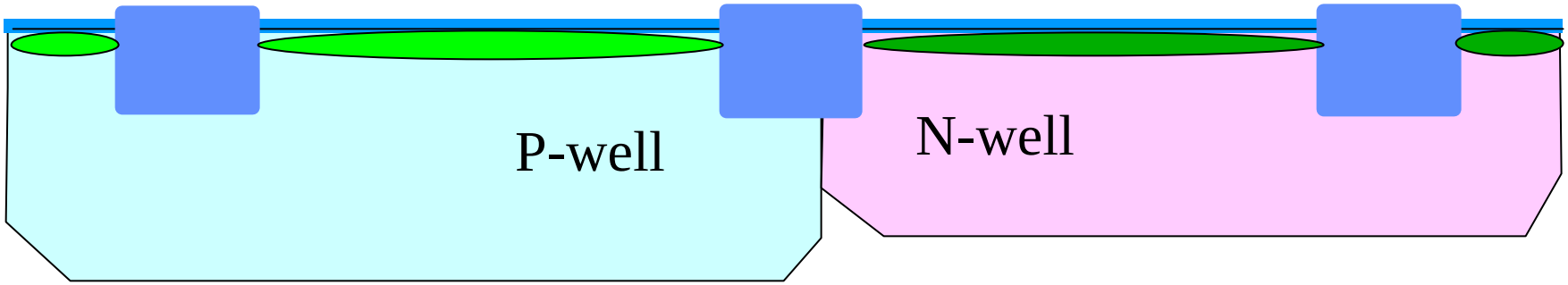
Substrate 10 ohm-cm

PMOS VT IMPLANT



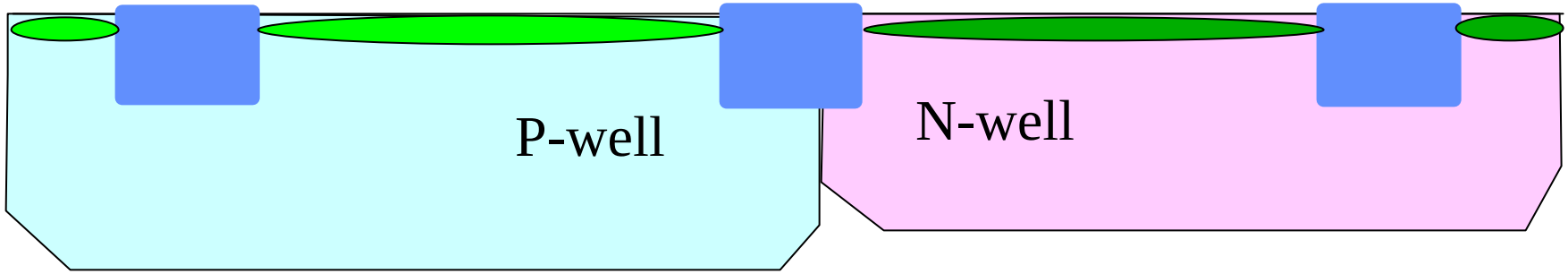
Substrate 10 ohm-cm

STRIP RESIST AND RCA CLEAN

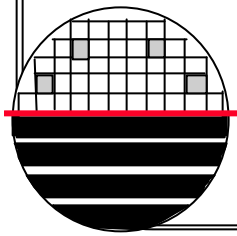


Substrate 10 ohm-cm

OXIDE ETCH

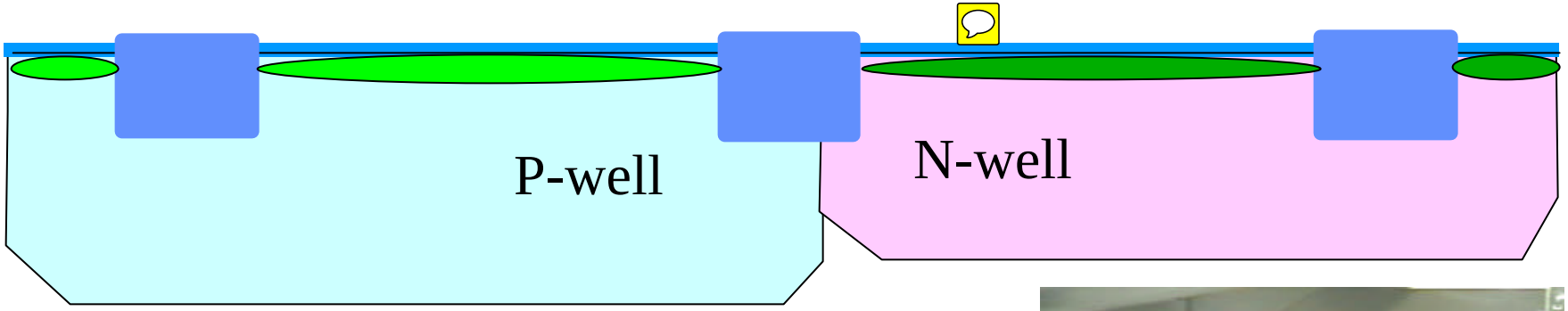


Substrate 10 ohm-cm

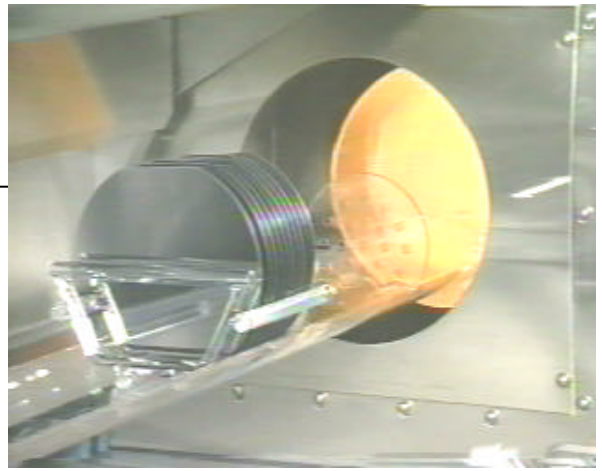


GROW GATE OXIDE

Oxide, 100A, Dry O_2
Bruce Furnace04 Recipe 214



Substrate 10 ohm-cm



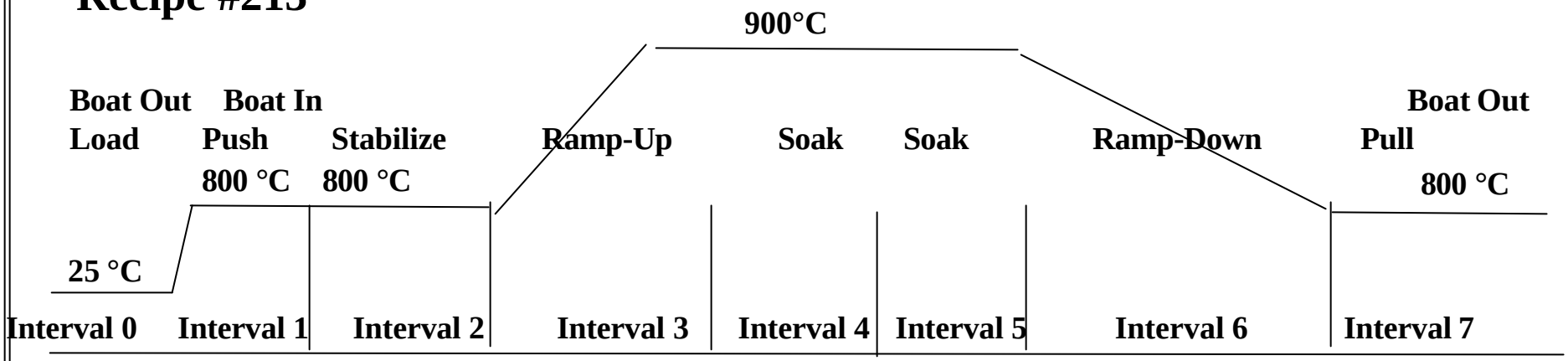
INCORPORATING NITROGEN IN THIN GATE OXIDES

In todays deep sub-micron transistors the pMOSFET normally has p+Poly for the gate material. The gate oxide is 100Å or less. The p+ dopant is normally Boron and Boron diffuses quickly (compared to Phosphorous) through oxides. Since the gate oxides are thin this could allow Boron to diffuse through the gate oxide and dope the channel causing the transistors to not function correctly. If some nitrogen is incorporated in the gate oxide the diffusion of Boron is much lower. This project involved developing a gate oxide recipe that will result in nitrogen incorporation in the gate oxide. The recipe included 30 min anneal in N2, 30 min oxynitride growth in N2O and 30 min oxide growth in O2, all at 900 °C. The gate oxides were evaluated at RIT using the ellipsometer (looking for index of refraction in between 1.45 (oxide) and 2.00 (nitride) and thickness near 100Å. The same wafers were also sent to Kodak for XPS analysis to give information on nitrogen content in the oxide.

BRUCE FURNACE RECIPE 213

Verified:2-24-04

Recipe #213



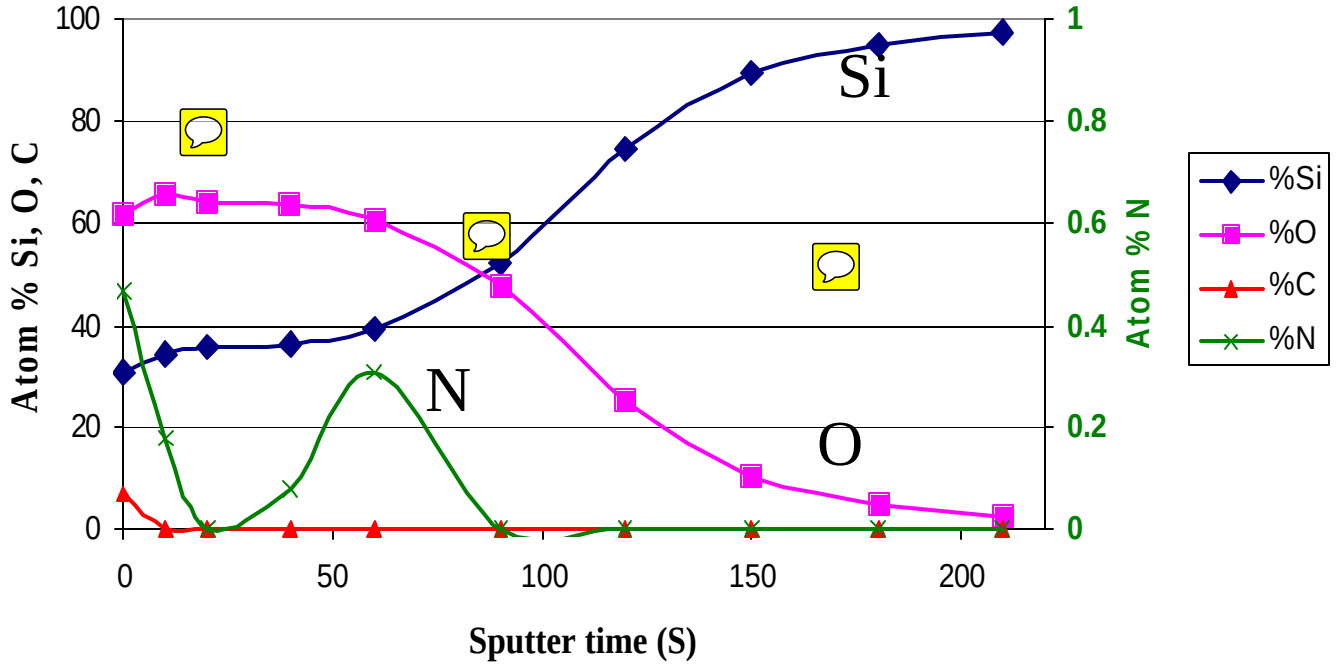
Any	12 min	30 min	30 min	30min	30 min	30 min	15 min
0 lpm	5 lpm	5 lmp	10 lpm	10 lpm	10 lpm	10 lpm	5 lpm
none	N2	N2	O2	N2O	O2	N2	N2

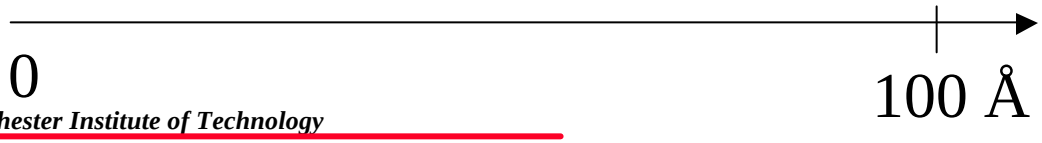
At the end of a run the furnace returns to Interval 0 which is set for boat out, 25 °C and no gas flow. The furnace waits in that state until someone aborts the current recipe or loads a new recipe.

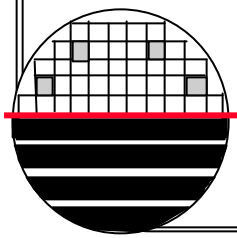
Dry Oxide Growth with N2O, Target 100 Å

INCORPORATING NITROGEN IN THIN GATE OXIDES

XPS Compositional Depth Profiles of SiO_XN_Y

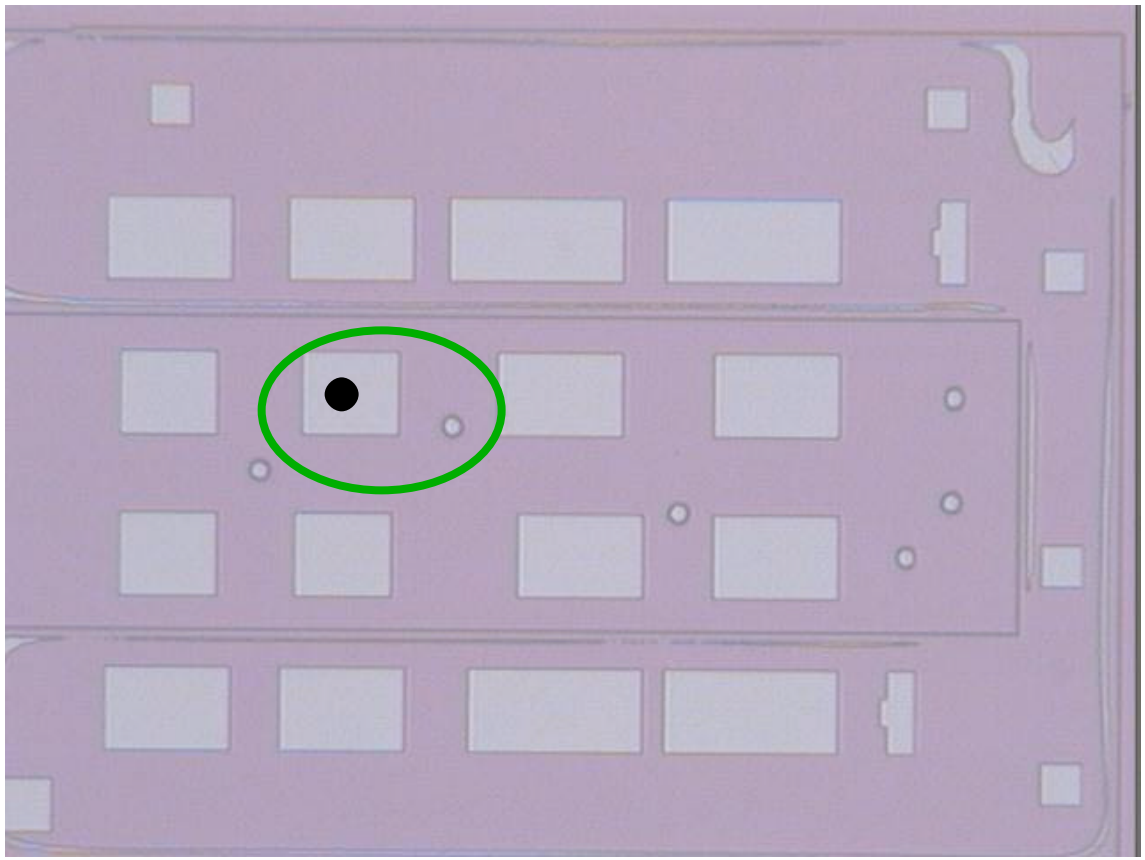






LOCATION FOR MEASUREMENT OF GATE OXIDE

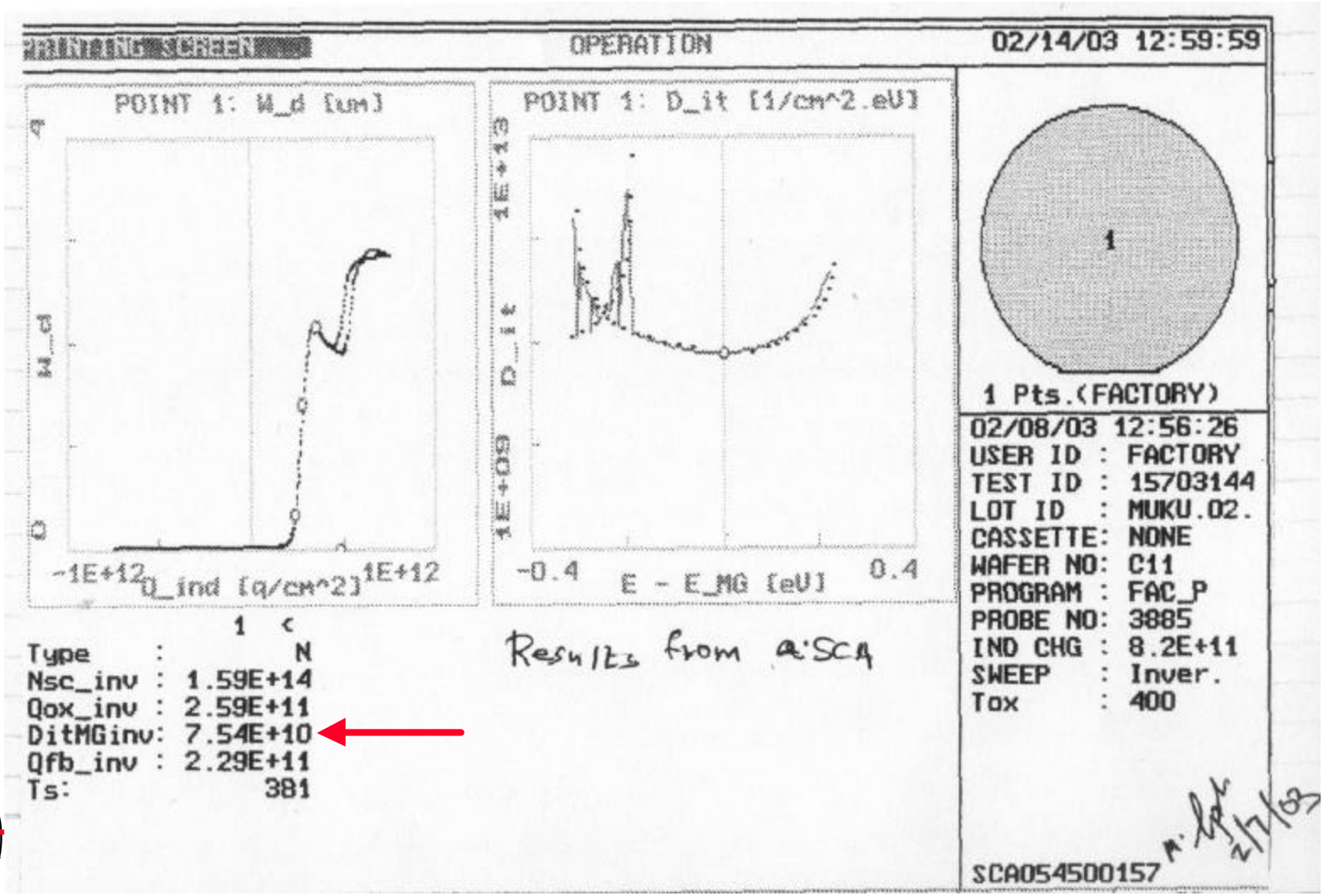
Measure gate oxide thickness (~100A) in any white active area



MEASURE C1 AND C2 ON SCA-2500

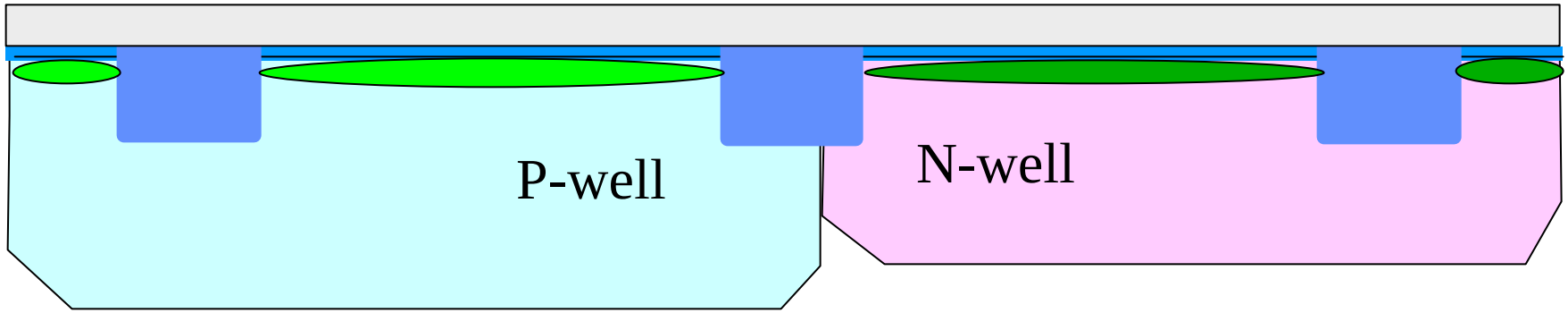
Login: FACTORY
Password: OPER
<F1> Operate
<F1> Test **Center the wafer on the stage**
Select (use arrow keys on the numeric pad (far right on the keyboard)
space bar, page up, etc)
PROGRAM = FAC-P or FAC-N
LOT ID = HAWAII
WAFER NO. = C1
TOX = 250 (from nanospec)
<F12> start test and wait for measurement
<Print Screen> print results
<F8> exit and log off
<ESC> can be used anytime, but wait for current test to be completed

SCA MEASUREMENT OF GATE OXIDE

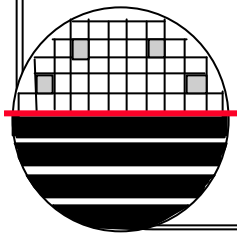


LPCVD POLY

Polysilicon, 4000A
LPCVD, 610C, ~53min



Substrate 10 ohm-cm



LOCATION FOR POLY THICKNESS MEASUREMENT

Measure poly thickness within any active area using thin film stack #4 on nanospec at 40X magnification

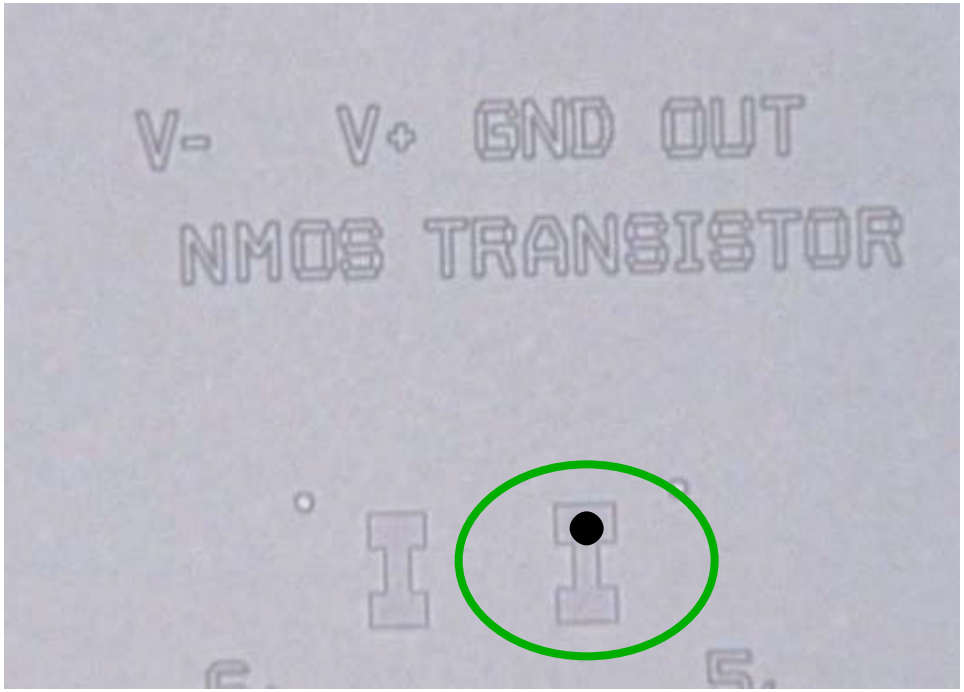
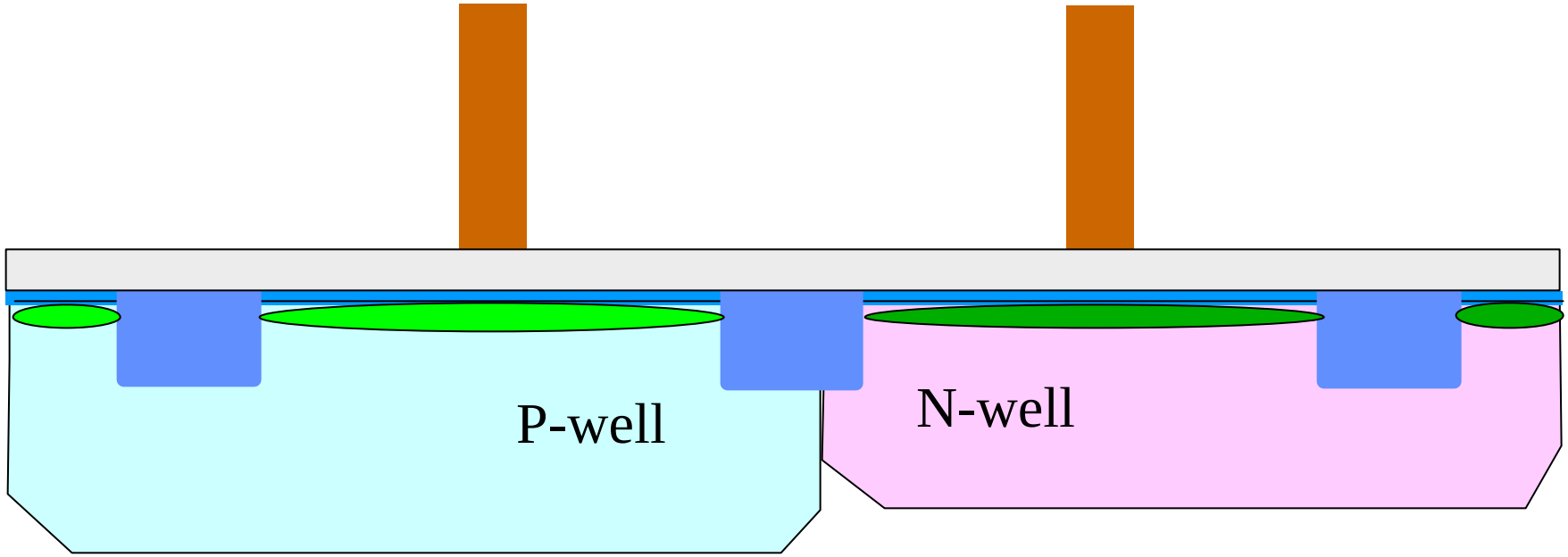
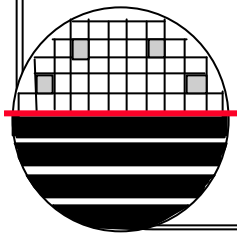


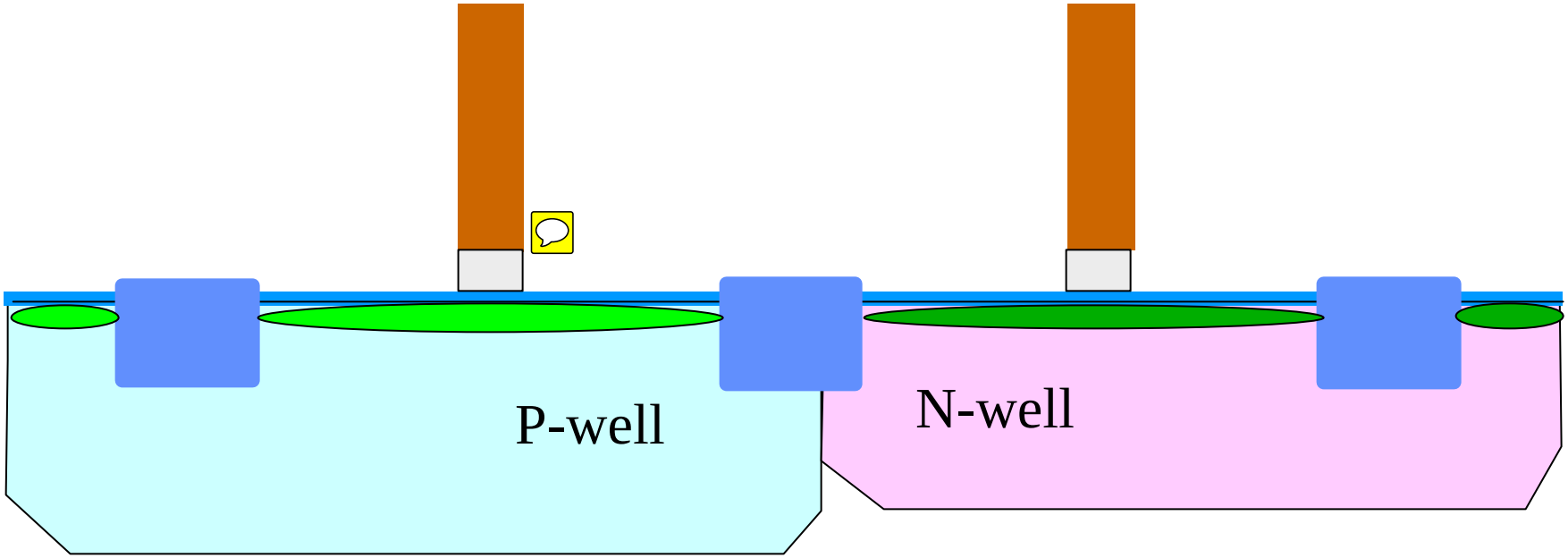
PHOTO 5 POLY GATE



Substrate 10 ohm-cm



POLY ETCH



Substrate 10 ohm-cm

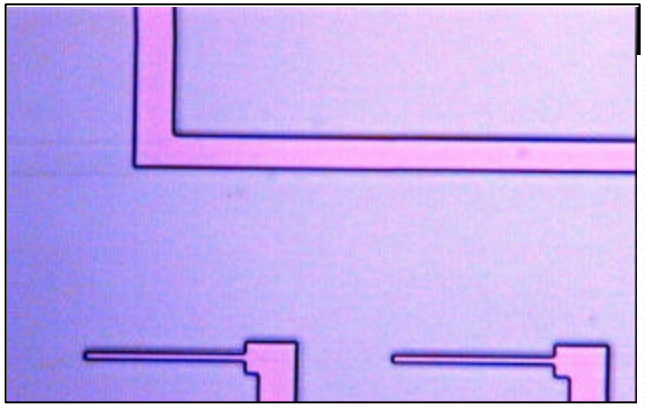
POLY ETCH WITH END POINT

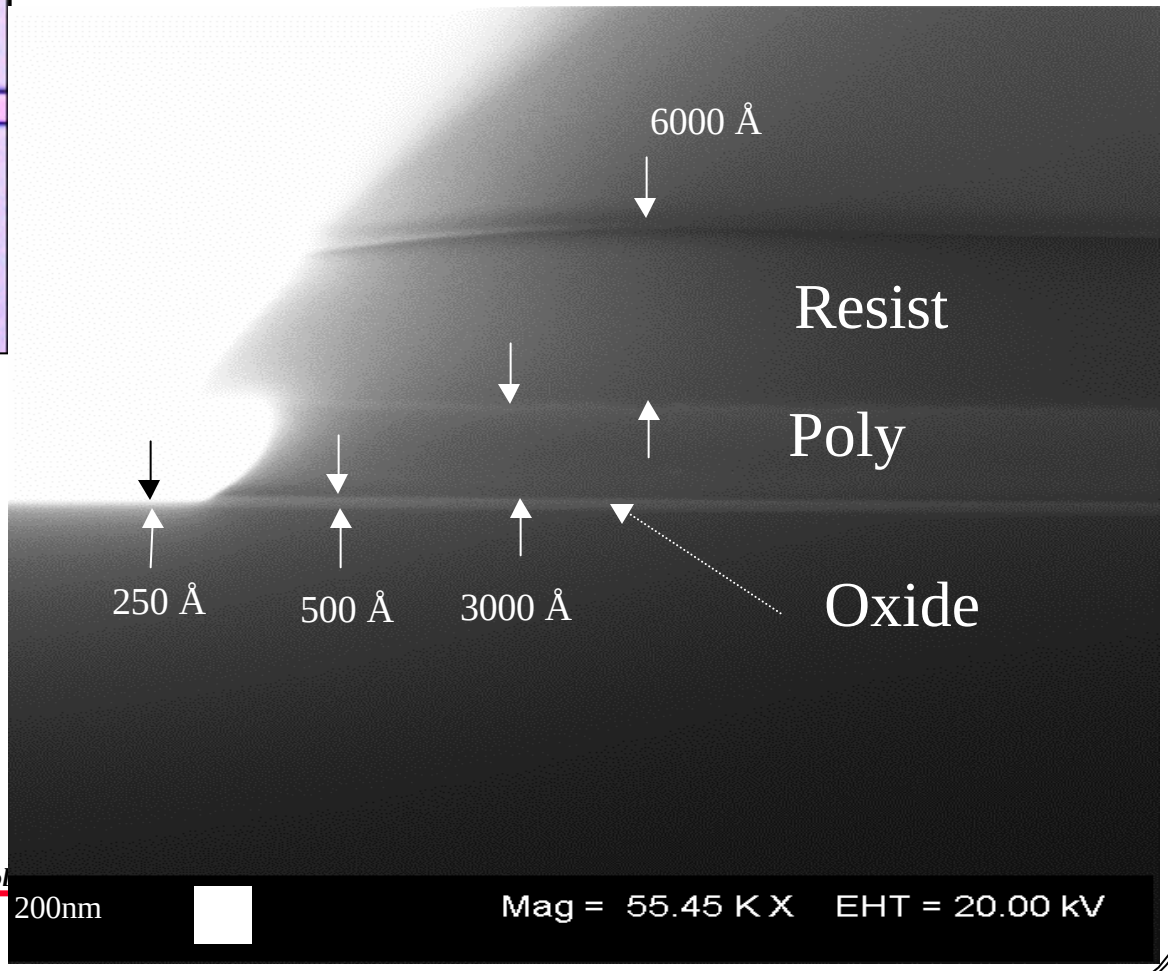
Process: Step 1 – 325mTorr; 0 watts
Gap = 1.5 cm
140sccm SF6, 15 sccm O2
Max Time = 2 min.
Time Only

Process: Step 2 – 325mTorr; 140 watts,
Gap = 1.5 cm
140sccm SF6, 15 sccm O2
Max Time = 1 min. 15 sec
Time or Endpoint
Endpoint and Time
Sampling A (ch12 @ 520nm)
Active during step 02
Delay 15sec before normalizing
Normalize for 10sec
Trigger at 90%

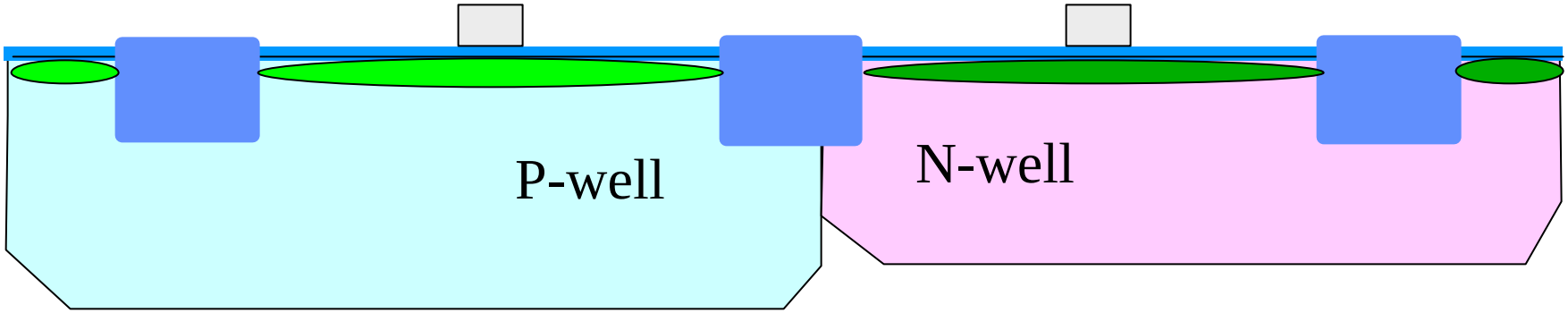
Process: Step 3 – 325mTorr; 140W,
Gap = 1.5 cm
140sccm SF6, 15 sccm O2
Overetch – 10%

VERIFICATION



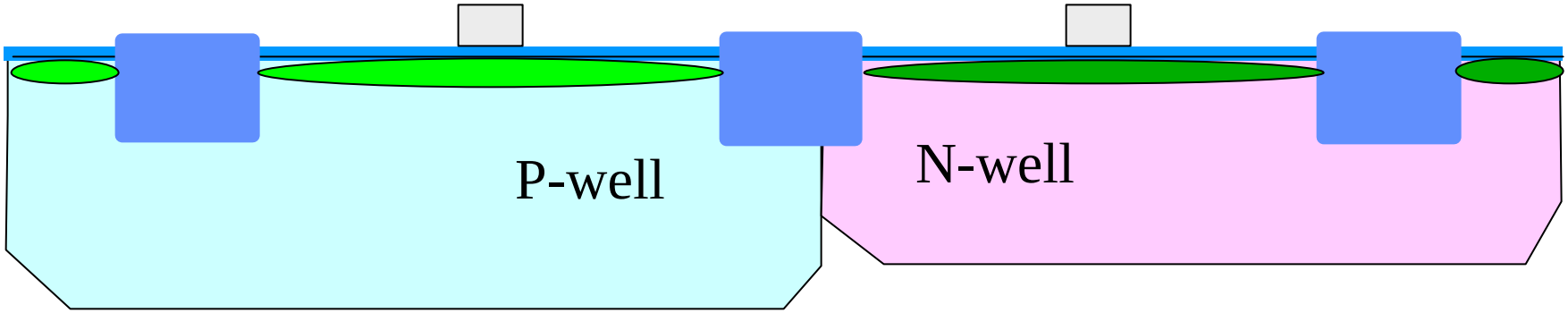


STRIP RESIST



Include D1-D3
Strip Photresist in Branson Asher

RCA CLEAN



GROW OXIDE

Oxide, 500A
Bruce Furnace 04 Recipe 250
~45 min at 1000 °C

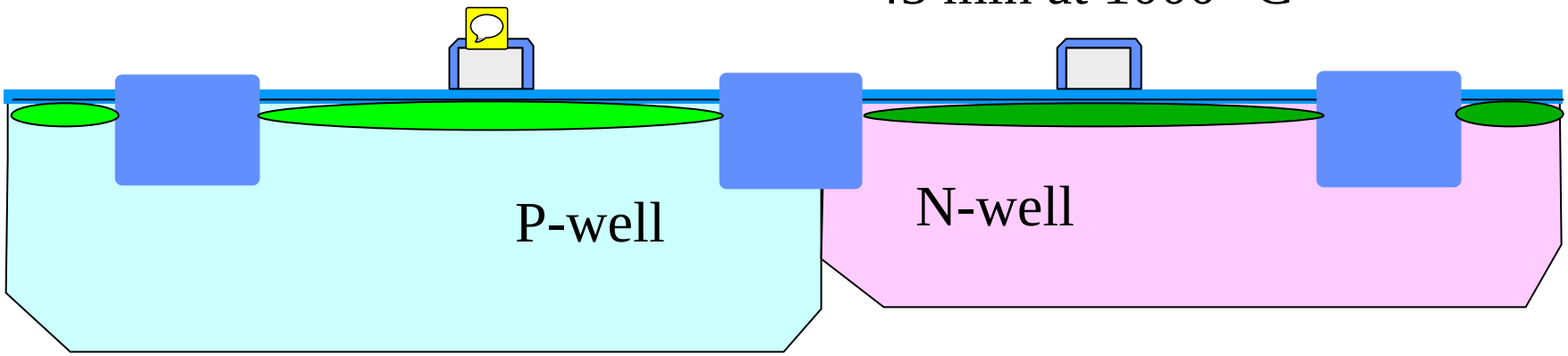
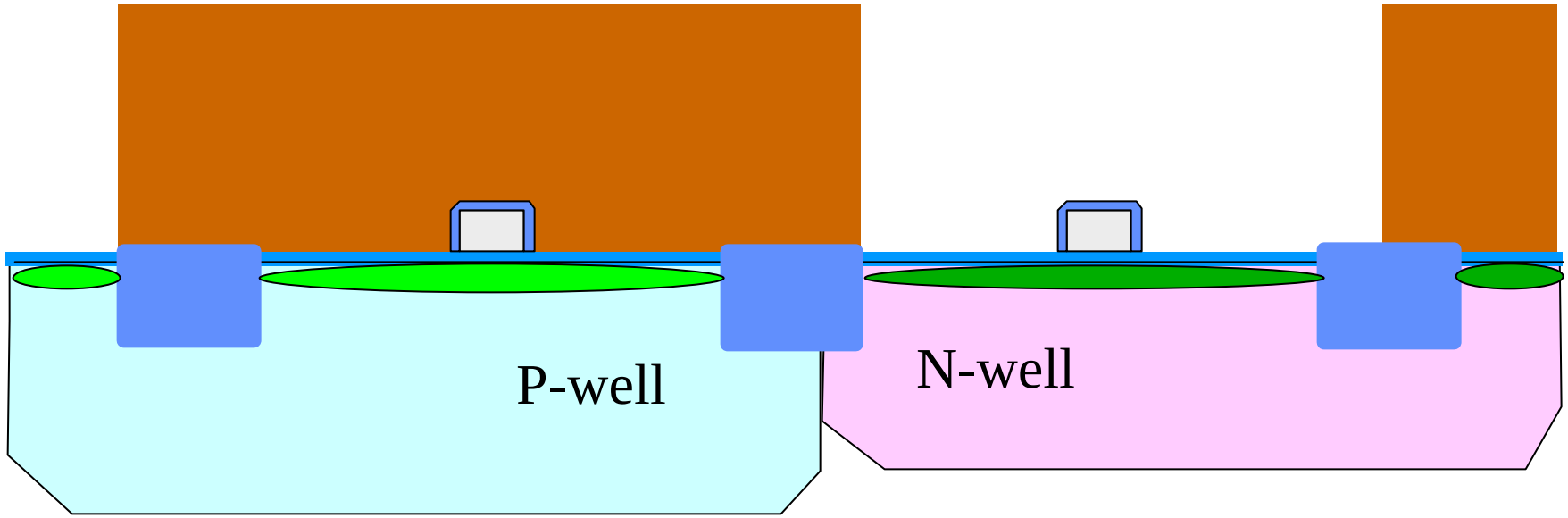
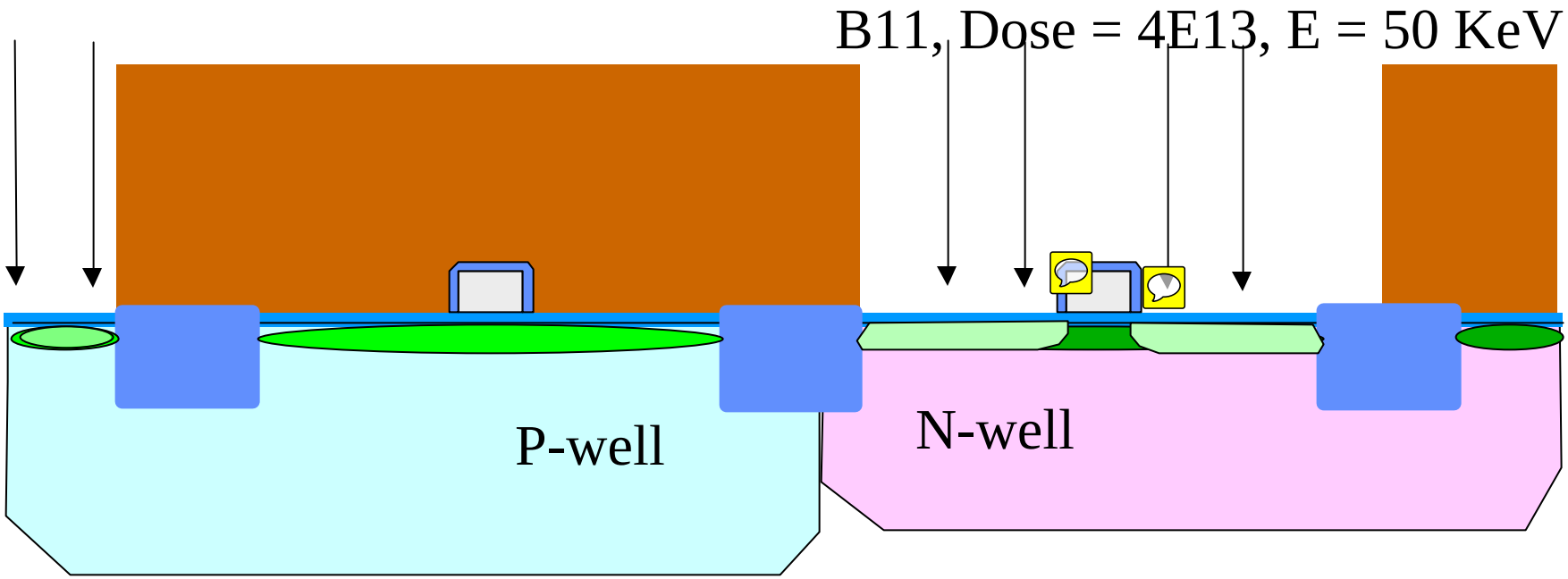


PHOTO 6 LDD P-TYPE IMPLANT



Substrate 10 ohm-cm

IMPLANT P-LDD



Substrate 10 ohm-cm

IMPLANT MASKING THICKNESS CALCULATOR

Rochester Institute of Technology					Lance Barron		
Microelectronic Engineering					Dr. Lynn Fuller		
11/20/04							

IMPLANT MASK CALCULATOR **Enter 1 - Yes 0 - No in white boxes**

DOPANT SPECIES

B11	1
BF2	0
P31	0

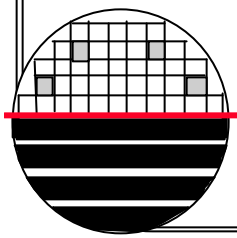
MASK TYPE

Resist	0
Poly	1
Oxide	0
Nitride	0

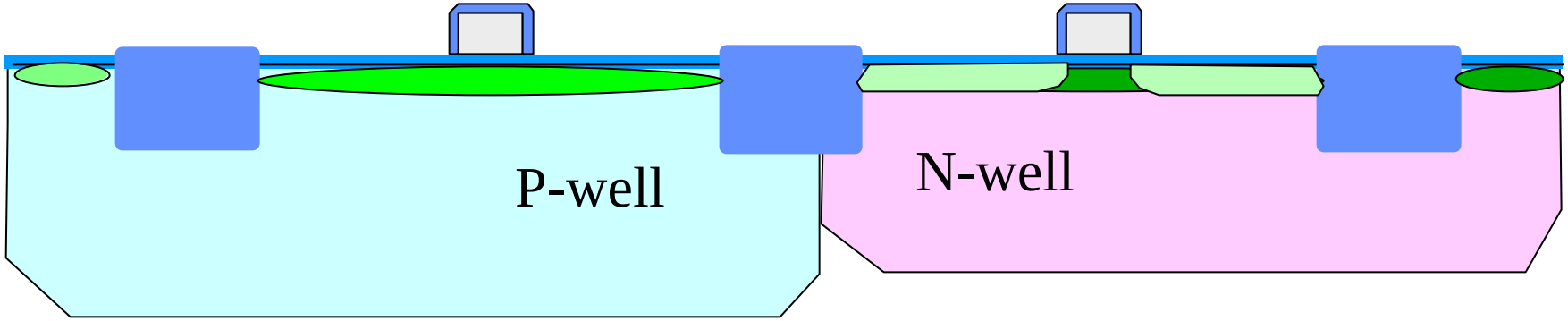
ENERGY

50 KeV

Thickness to Mask >1E15/cm3 Surface Concentration 3529.481 Angstroms



STRIP RESIST



Include D1-D3
Strip Photresist in Branson Asher

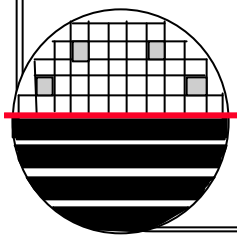
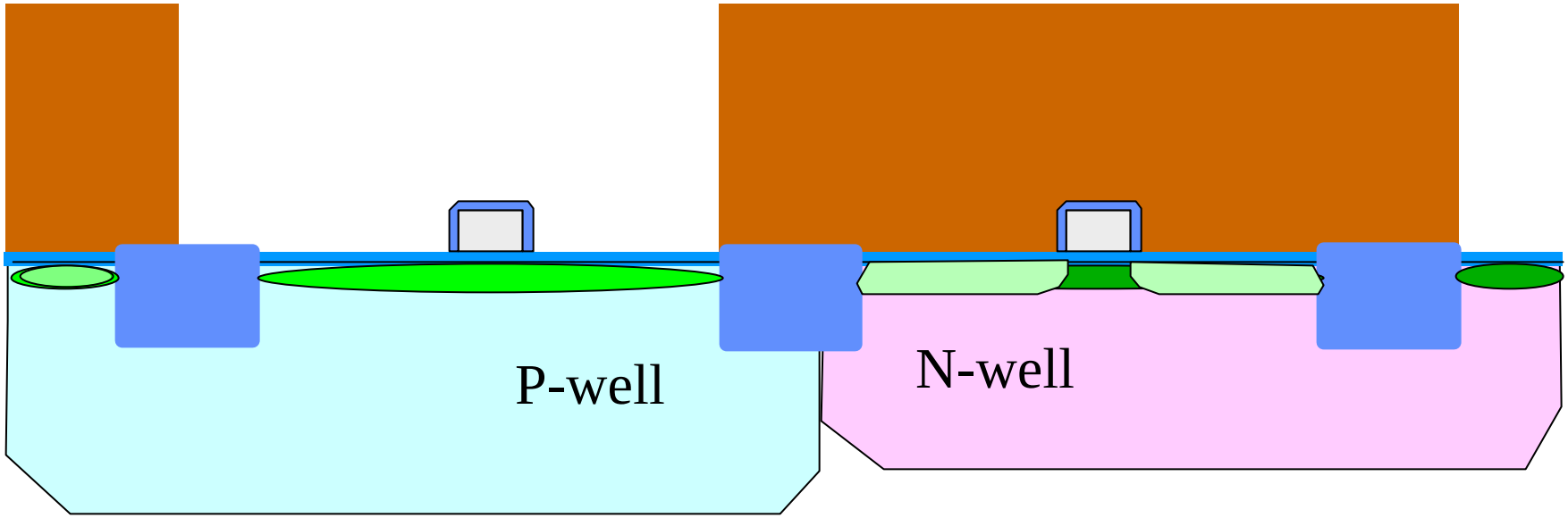


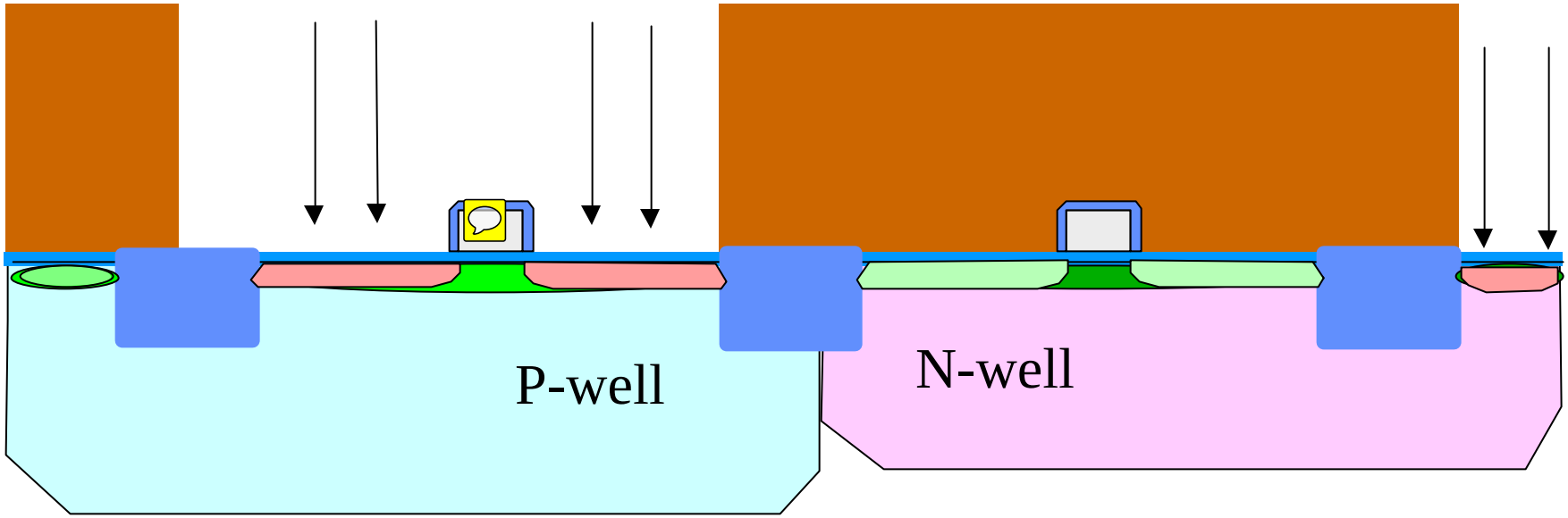
PHOTO 7 LDD N-TYPE IMPLANT



Substrate 10 ohm-cm

IMPLANT N-LDD

P31, Dose = 4E13, E = 60 KeV



Substrate 10 ohm-cm

IMPLANT MASKING THICKNESS CALCULATOR

Rochester Institute of Technology					Lance Barron		
Microelectronic Engineering					Dr. Lynn Fuller		
11/20/04							

IMPLANT MASK CALCULATOR **Enter 1 - Yes 0 - No in white boxes**

DOPANT SPECIES

B11	0
BF2	0
P31	1

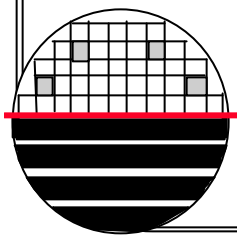
MASK TYPE

Resist	0
Poly	1
Oxide	0
Nitride	0

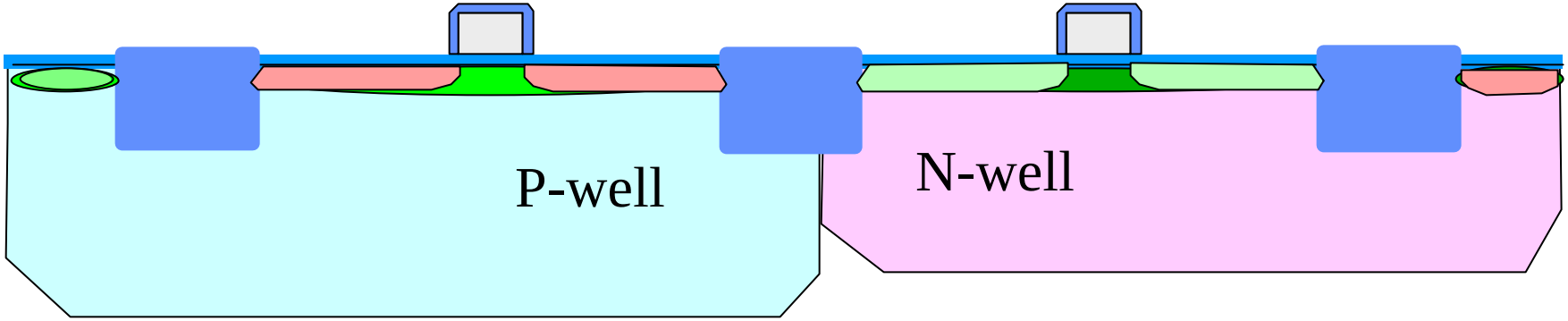
ENERGY

60 KeV

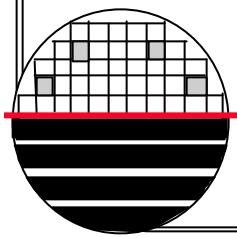
Thickness to Mask >1E15/cm3 Surface Concentration 2798.861 Angstroms



STRIP RESIST

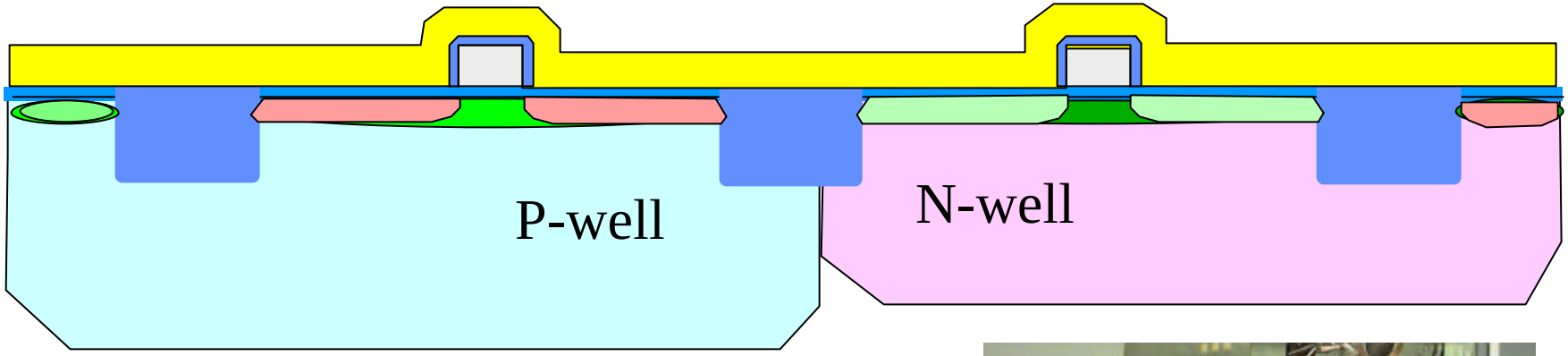


Include D1-D3
Strip Photresist in Branson Asher

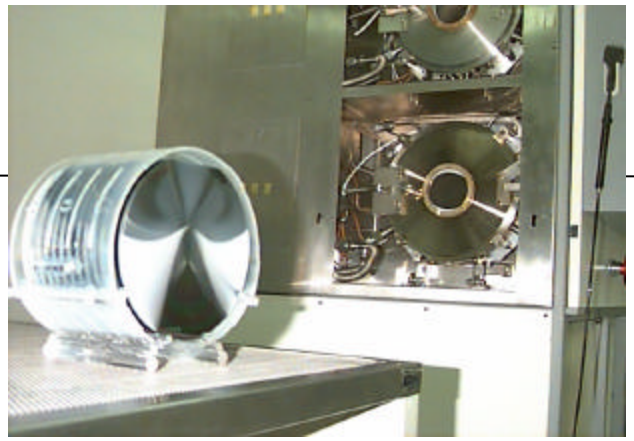


RCA CLEAN AND LPCVD NITRIDE

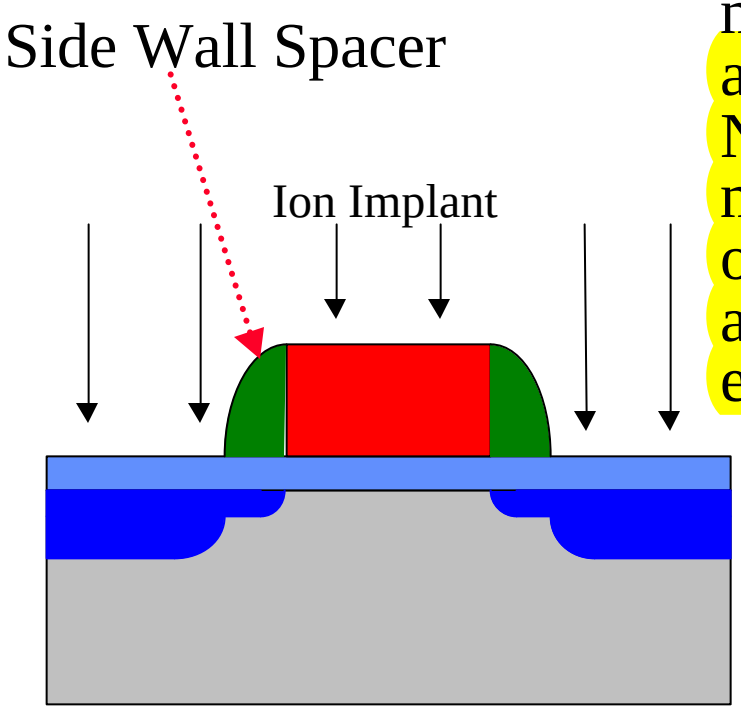
Target 4000 Å



ASM 6" LPCVD Tool



NITRIDE SIDE WALL SPACERS

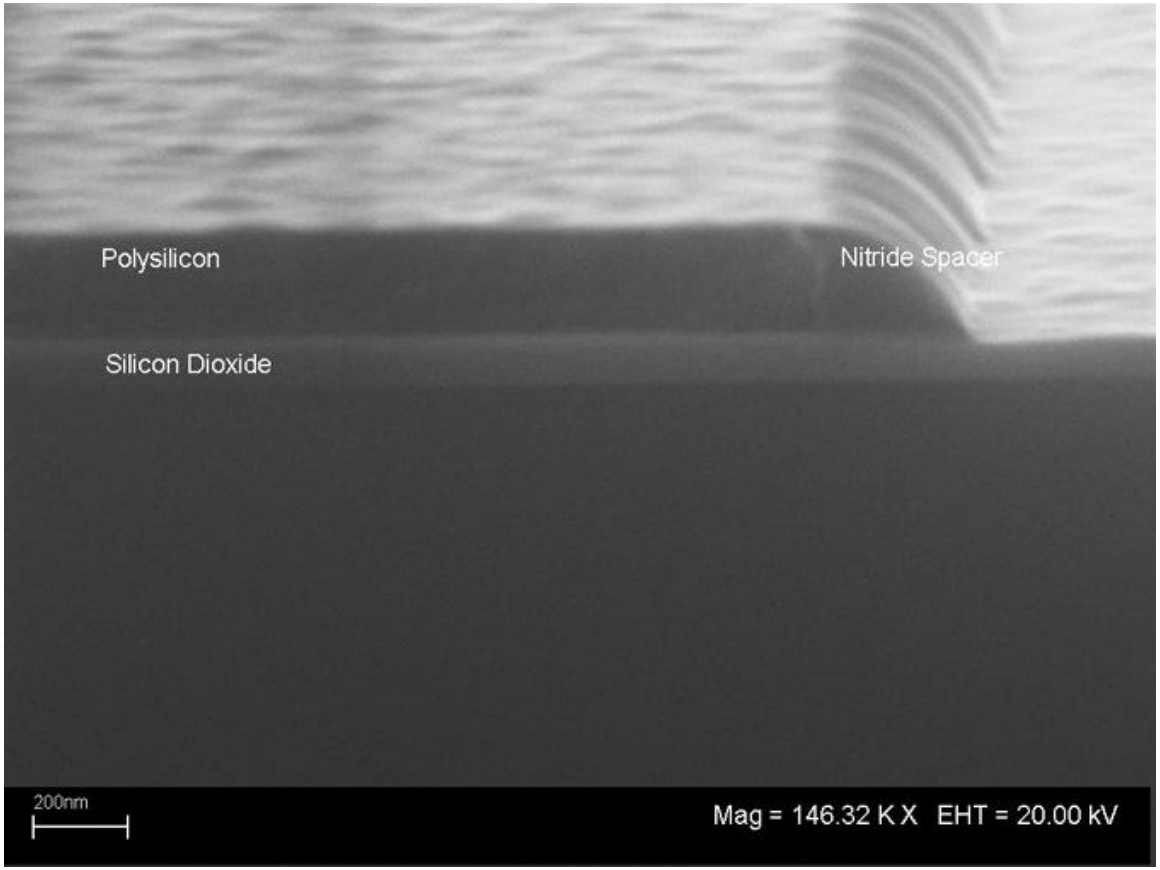


Nitride as a side wall spacer in deep sub micron transistor fabrication has some advantages over oxide side wall spacers. Nitride LPCVD is a more uniform and more conformal film than LTO. Nitride offers the possibility of end-point detection and higher selectivity during the plasma etch, while an oxide spacer does not.

Power	**250 Watts**
Pressure	**40 mTorr**
SF6	**30 sccm**
CHF3	**30 sccm**
Nitride Etch Rate	**1250 A/min**
Nitride Etch %NU	**~ 4% ***
Oxide Etch Rate	**~ 950 A/min ***
Oxide Etch %NU	**~ 10% ***
Selectivity Nitride:Oxide	**1.3:1**

Drytek Quad

NITRIDE SIDE WALL SPACERS



Poly thickness = 2300 A
Oxide thickness = 1000A
Spacer Height = 2300 A
Spacer Width = 0.3 um

Special thanks to
Dr. Sean Rommel for
help in using the new
LEO SEM

SIDE WALL SPACER ETCH IN DRYTEK QUAD

Anisotropic Nitride Etch
Drytek Quad
Recipe FACSPCR
30 sccm SF6
30 sccm CHF3
Power = 250 watts
Pressure = 40 mTorr
Etch Rate = 125 nm/min

ETCH NITRIDE TO FORM SIDE WALL SPACERS

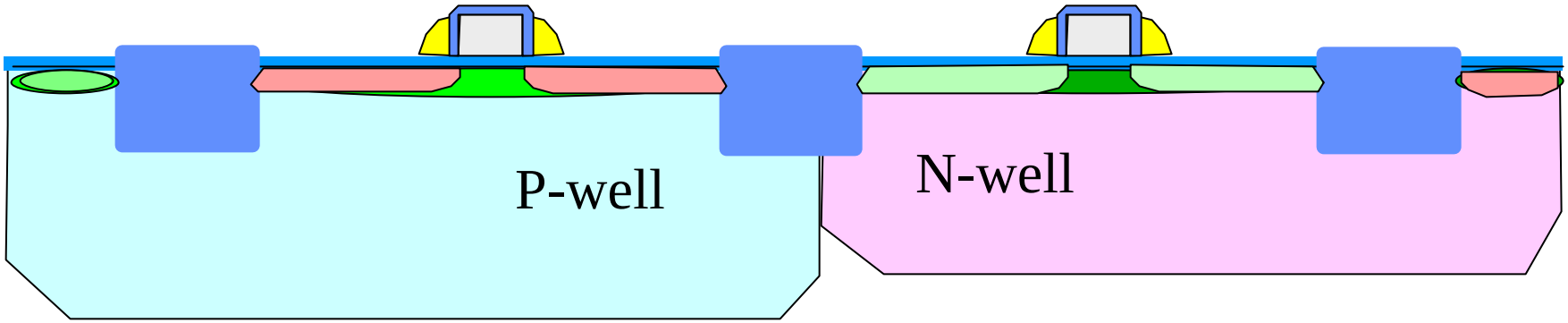
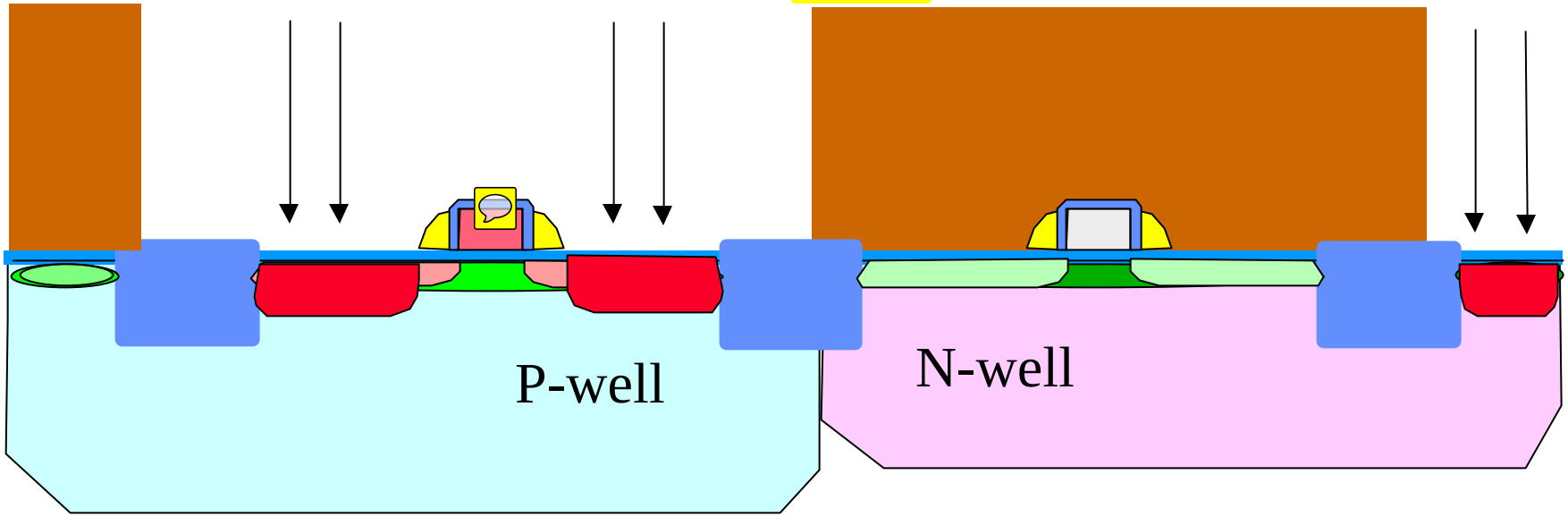


PHOTO 8 N+ D/S

P31, Dose = 2 E15, E = 60 KeV



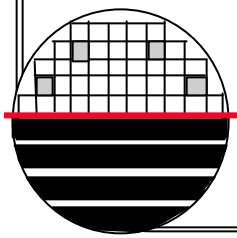
IMPLANT MASKING THICKNESS CALCULATOR

Rochester Institute of Technology				Lance Barron	
Microelectronic Engineering				Dr. Lynn Fuller	
11/20/04					

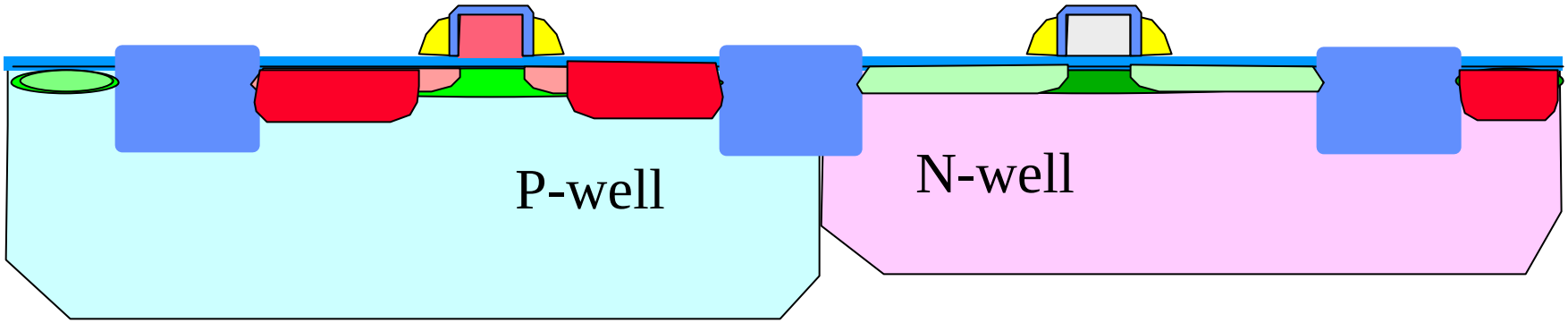
IMPLANT MASK CALCULATOR **Enter 1 - Yes 0 - No in white boxes**

DOPANT SPECIES		MASK TYPE		ENERGY	
B11	0	Resist	0	60	KeV
BF2	0	Poly	1		
P31	1	Oxide	0		
		Nitride	0		

Thickness to Mask >1E15/cm3 Surface Concentration 2798.861 Angstroms



STRIP RESIST



Include D1-D3
Strip Photresist in Branson Asher

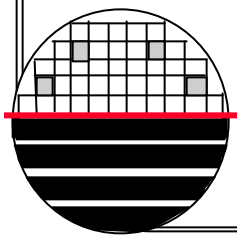
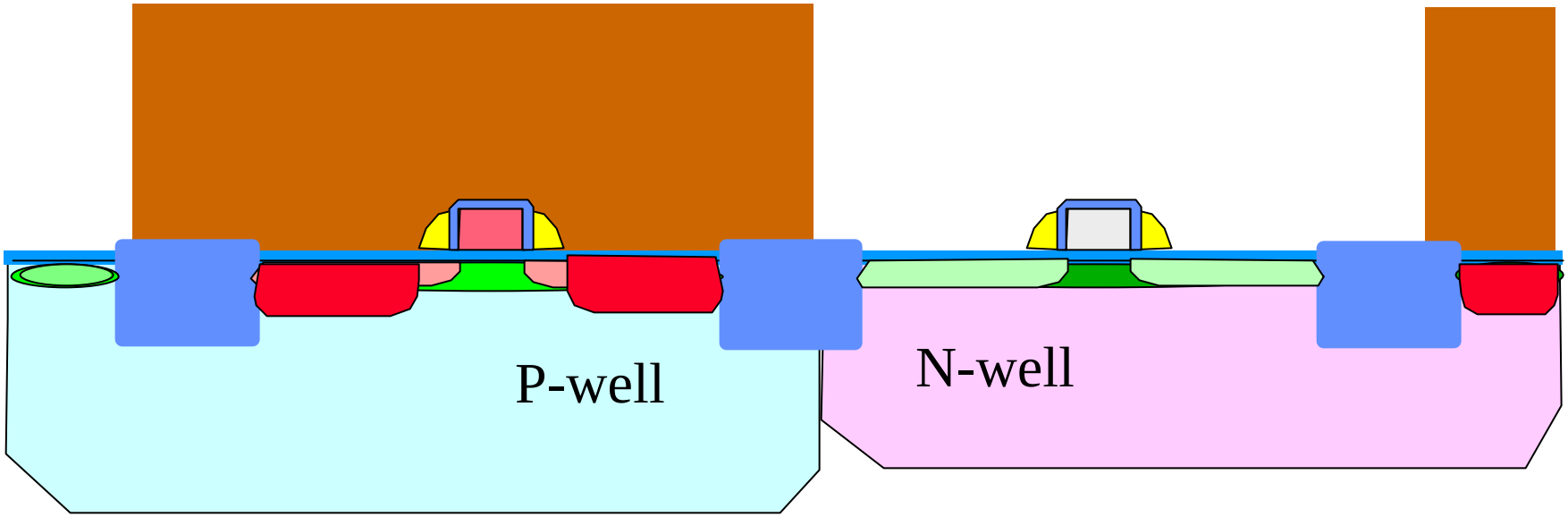
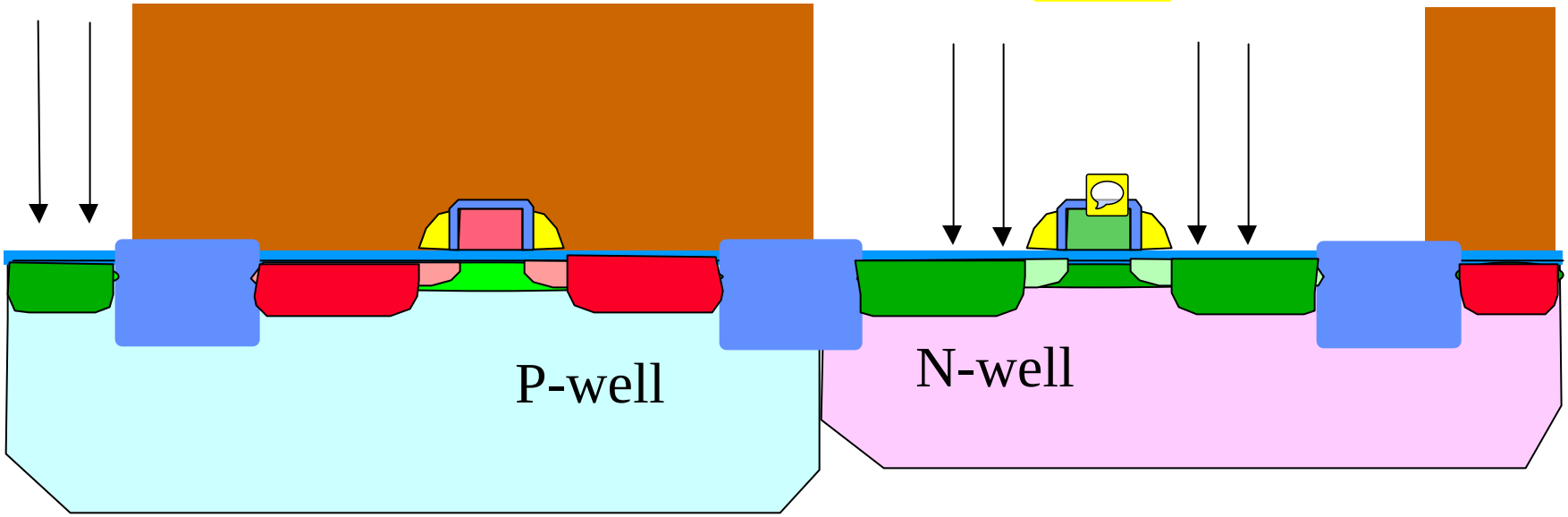


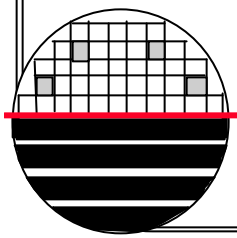
PHOTO 9 P+ D/S



IMPLANT P+ D/S

B11, Dose = 2 E15, E = 50 KeV





IMPLANT MASKING THICKNESS CALCULATOR

Rochester Institute of Technology					Lance Barron		
Microelectronic Engineering					Dr. Lynn Fuller		
11/20/04							

IMPLANT MASK CALCULATOR **Enter 1 - Yes 0 - No in white boxes**

DOPANT SPECIES

B11	1
BF2	0
P31	0

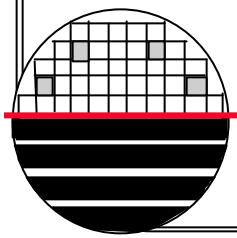
MASK TYPE

Resist	0
Poly	1
Oxide	0
Nitride	0

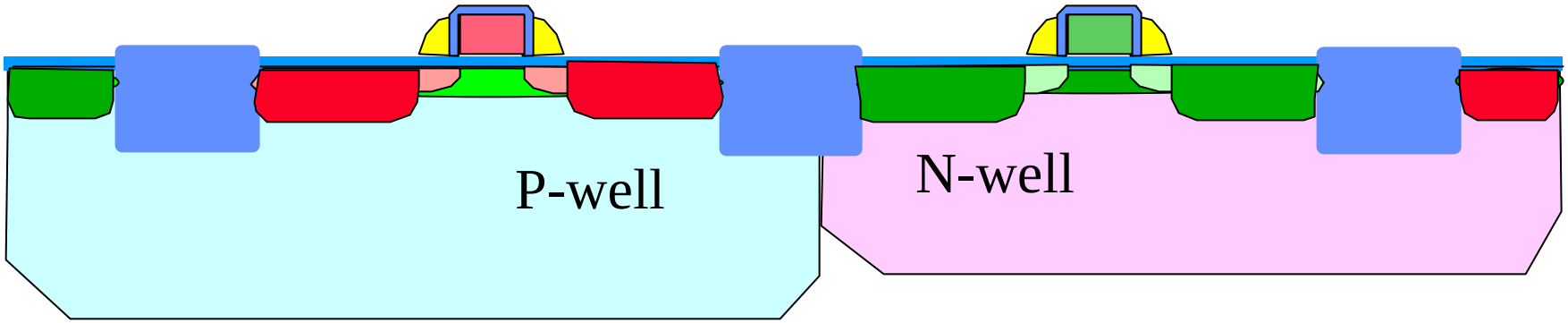
ENERGY

40 KeV

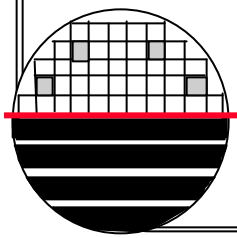
Thickness to Mask >1E15/cm3 Surface Concentration 2961.954 Angstroms



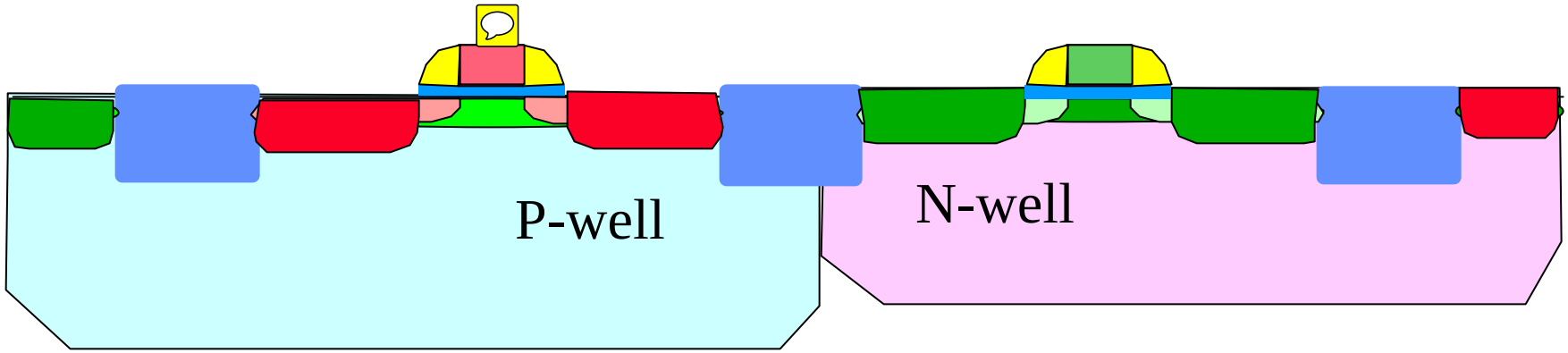
STRIP RESIST, RCA CLEAN

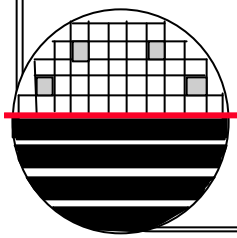


Include D1-D3
Strip Photresist in Branson Asher



ETCH OXIDE





TiSi SALACIDE PROCESS

Forming a metal silicide helps reduce the resistance of the polysilicon interconnects and reduces the sheet resistance of the drain/source areas of the transistor. In deep sub-micron CMOS the nMOSFET transistor has n+ poly and the pMOSFET has p+ poly. Normally the poly is doped by ion implantation at the same time the drain and sources is implanted. In this case it is essential to form a silicide to reduce the sheet resistance of the poly and to connect n+ and p+ poly where ever they meet. SALICIDE is an acronym for self-aligned silicide and can be achieved with the following process. Ti (or some other metal) is sputtered on the wafer. It is heated in vacuum or N2 atmosphere to form TiSi where ever the Ti metal is in contact with silicon but not where it is in contact with silicon dioxide. The wafer is etched in sulfuric acid and hydrogen peroxide mixture which removes the metal from the oxide regions leaving TiSi self aligned on the silicon areas. Further heat treating at a higher temperature can convert TiSi to TiSi2 which is lower sheet resistance.

TiSi SALACIDE PROCESS

Sputtering of Titanium:

4" Target, 350 watts, 5 mTorr, 10 min pre-sputter, 10 min sputter, Rate = 100Å/min

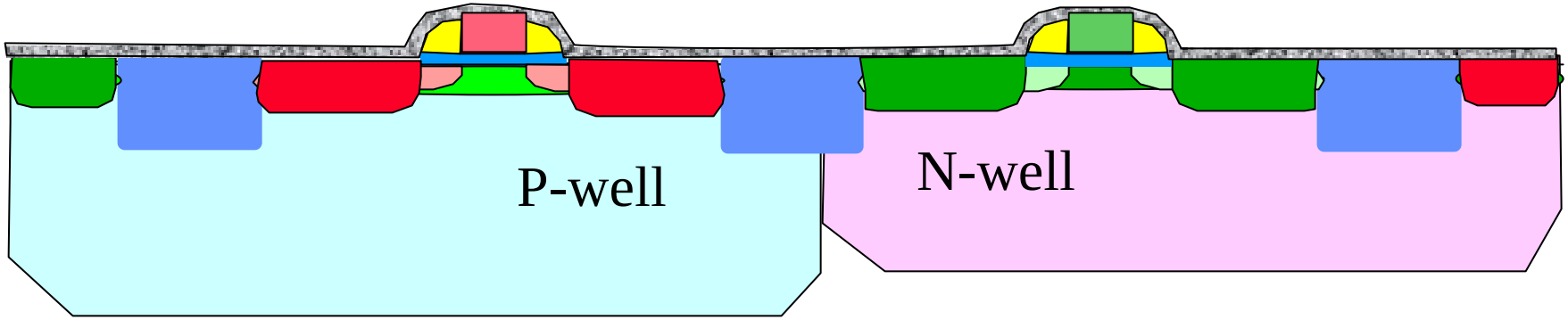
8" Target, 750 watts, 5 mTorr, 10 min pre-sputter, 10 min sputter, Rate = 176 Å/min

SPUTTER OF Co AND Ti FOR CoSi2 SALACIDE

Total Thickness = 700 Å
Dilute HF dip (50:1) 30 sec
Spin Rinse Dry
Sputter in CVC601
Heater time, 20 min., 300 C
Base Pressure <5E-6 Torr
Presputter Co 5 min at 250 watts
Sputter Co at 5 mTorr of Ar
Time = 6 min.
Presputter Ti 5 min at 1000 watts
Sputter Ti at 5 mTorr of Ar
Time = 17 min

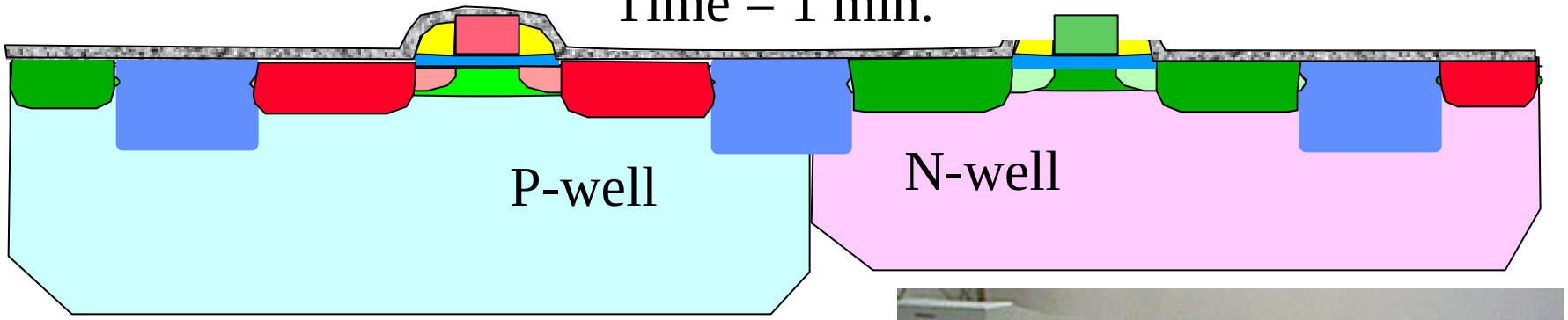
CVC 601 Sputter Tool

SPUTTER Co AND/OR Ti

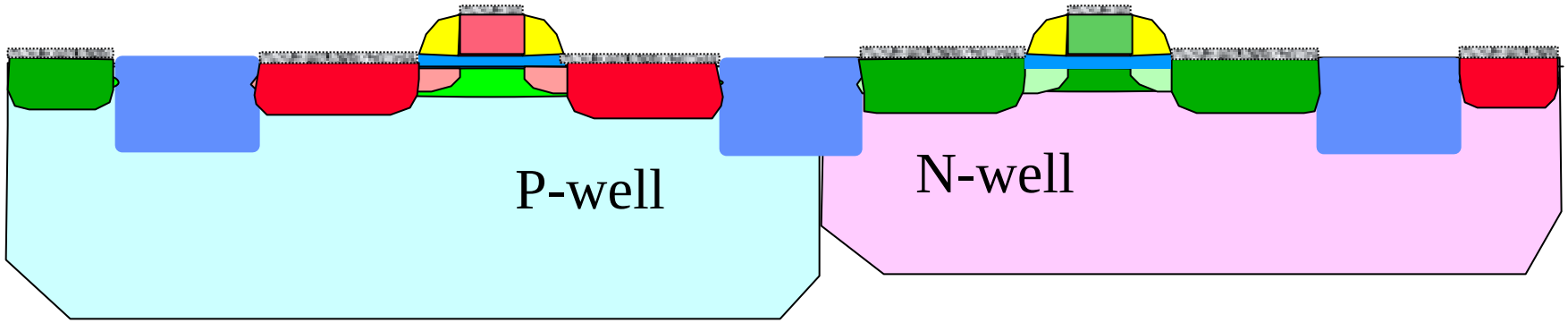


RTP TO FORM SILICIDE

AG Associates 610
N2
Recipe TISI1.RCP
Temp = ~350 C
Time = 1 min.



ETCH REMOVE Co/Ti



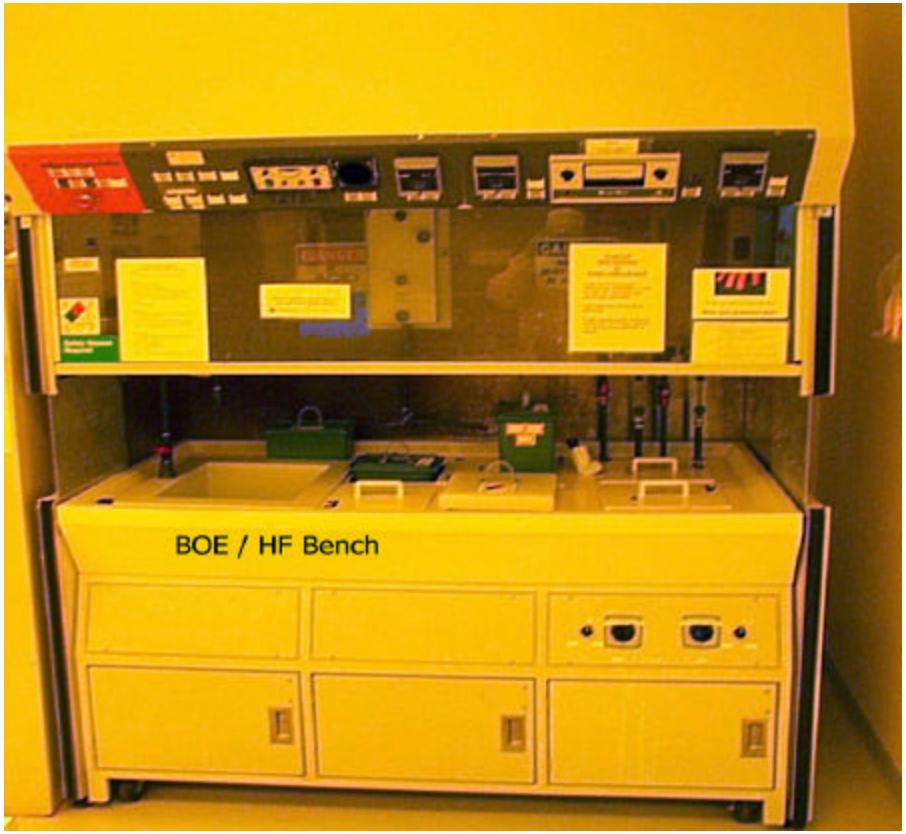
Mix new chemicals in 9"x9" Pyrex Dish
H2S04:H2O2 (1:2), Temp ~90C (self heating)
Etch Time = 2 min
Rinse, 5 min., Spin-Rinse Dry

TiSi SALACIDE PROCESS

Etching of Ti Metal:

Heat the Sulfuric Acid:Hydrogen Peroxide (1:2) mixture on a hotplate to 100°C (set plate temperature to 150°C)

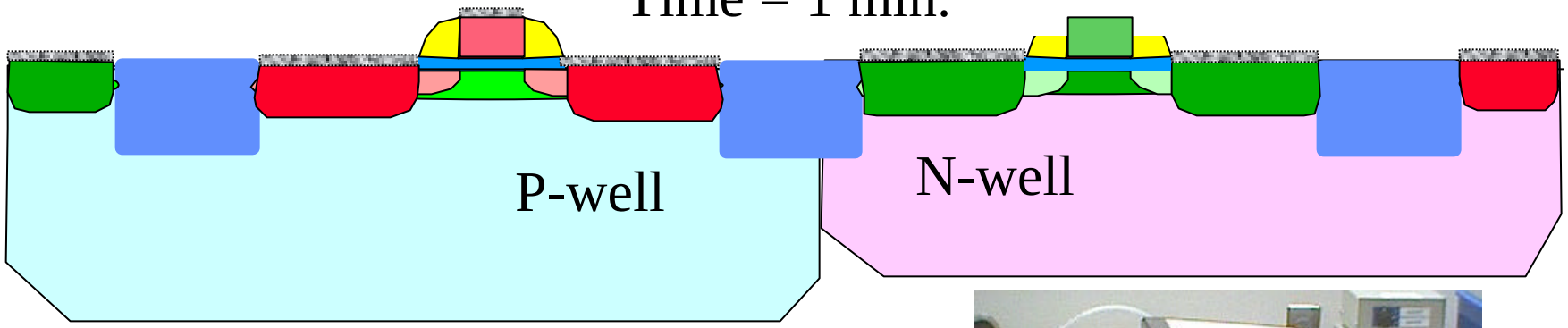
Etch for 1 min 30 sec. This should remove the Ti that is on top of the silicon dioxide but not remove TiSi that was formed on the polysilicon and D/S regions. It also removes unreacted Ti metal over the TiSi on the poly and D/S regions.



Courtesy of SMFL

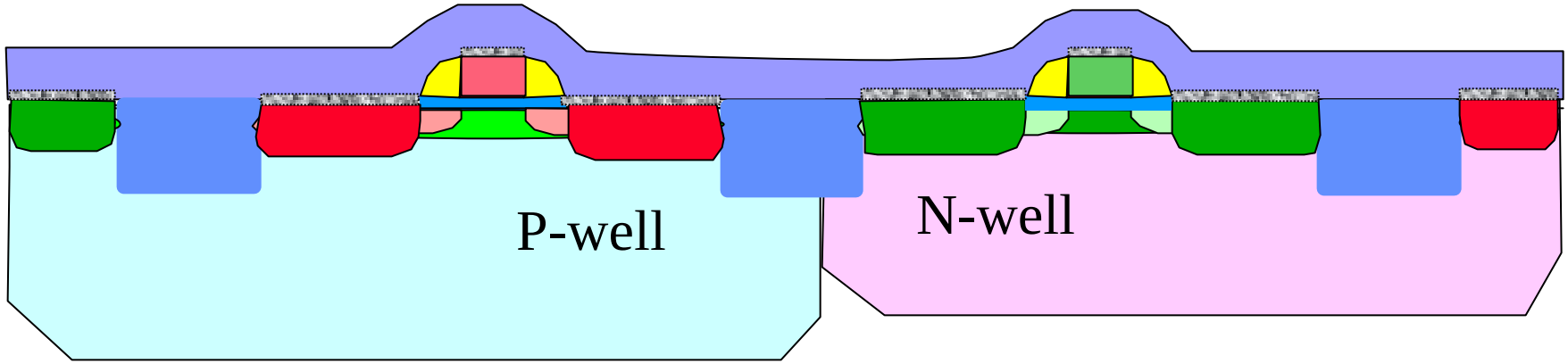
RTP TO FORM SILICIDE (CoSi2)

AG Associates 610
N2
Recipe TiSi2.RCP
Temp = ~750 C
Time = 1 min.



RCA CLEAN AND DEPOSIT LPCVD OXIDE

Target 4000 Å



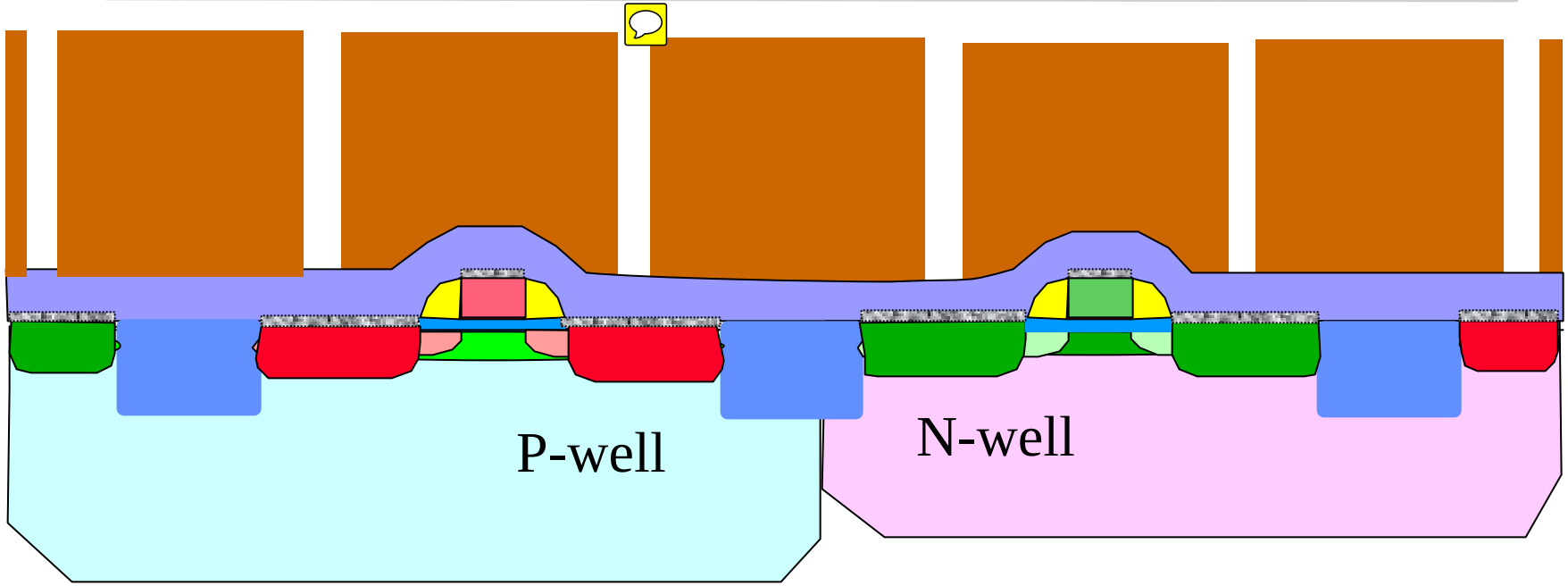
PECVD OXIDE FROM TEOS

TEOS Program: (Chamber A)
Step 1
- Setup Time = 15 sec
- Pressure = 9 Torr
- Susceptor Temperature= 390 C
- Susceptor Spacing= 220 mils
- RF Power = 0 watts
- TEOS Flow = 400 scc
- O2 Flow = 285 scc

Step 2 – Deposition
- Dep Time = 55 sec (5000 Å)
- Pressure = 9 Torr
- Susceptor Temperature= 390 C
- Susceptor Spacing= 220 mils
- RF Power = 205 watts
- TEOS Flow = 400 scc
- O2 Flow = 285 scc

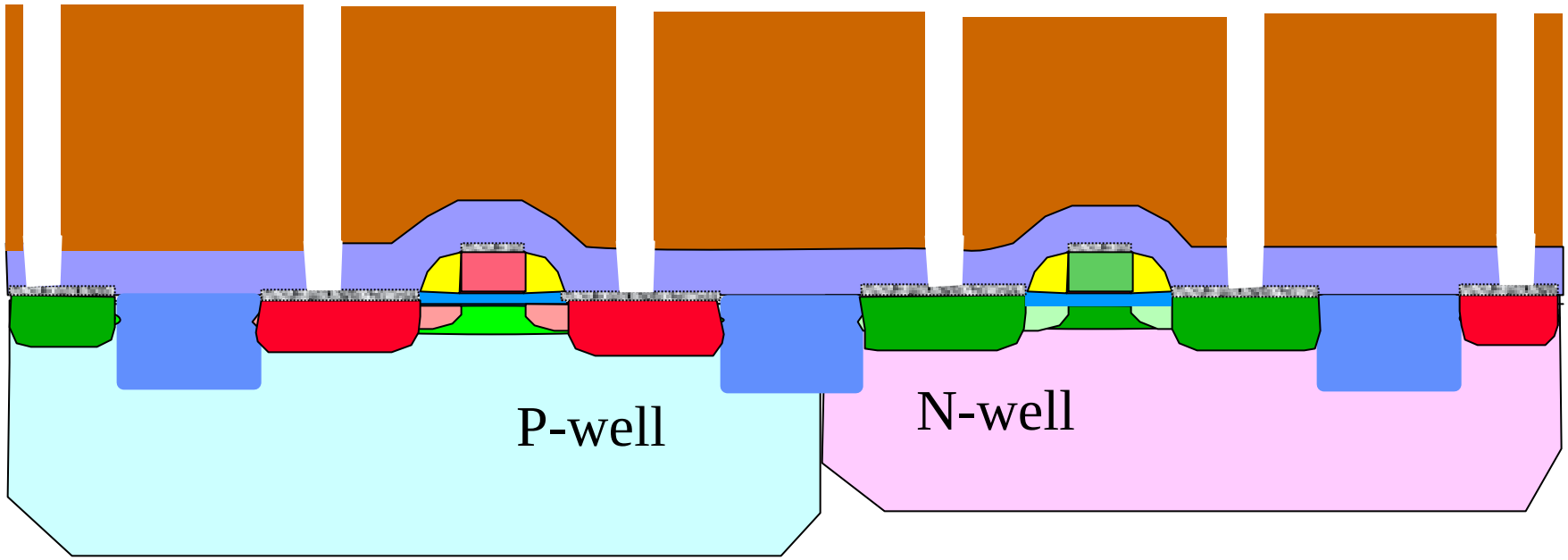
Step 3 – Clean
- Time = 10 sec
- Pressure = Fully Open
- Susceptor Temperature= 390 C
- Susceptor Spacing= 999 mils
- RF Power = 50 watts
- TEOS Flow = 0 scc
- O2 Flow = 285 scc

PHOTO 10 CONTACT CUTS

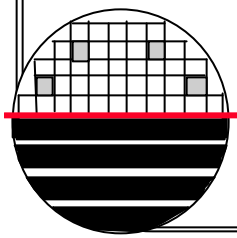


Increase Dose and Develop Time
Exposure Dose 185 mj/cm2
Use DEVFAC.RCP

ETCH CONTACT CUTS



Wet Etch in BHF, 5 min, SRD



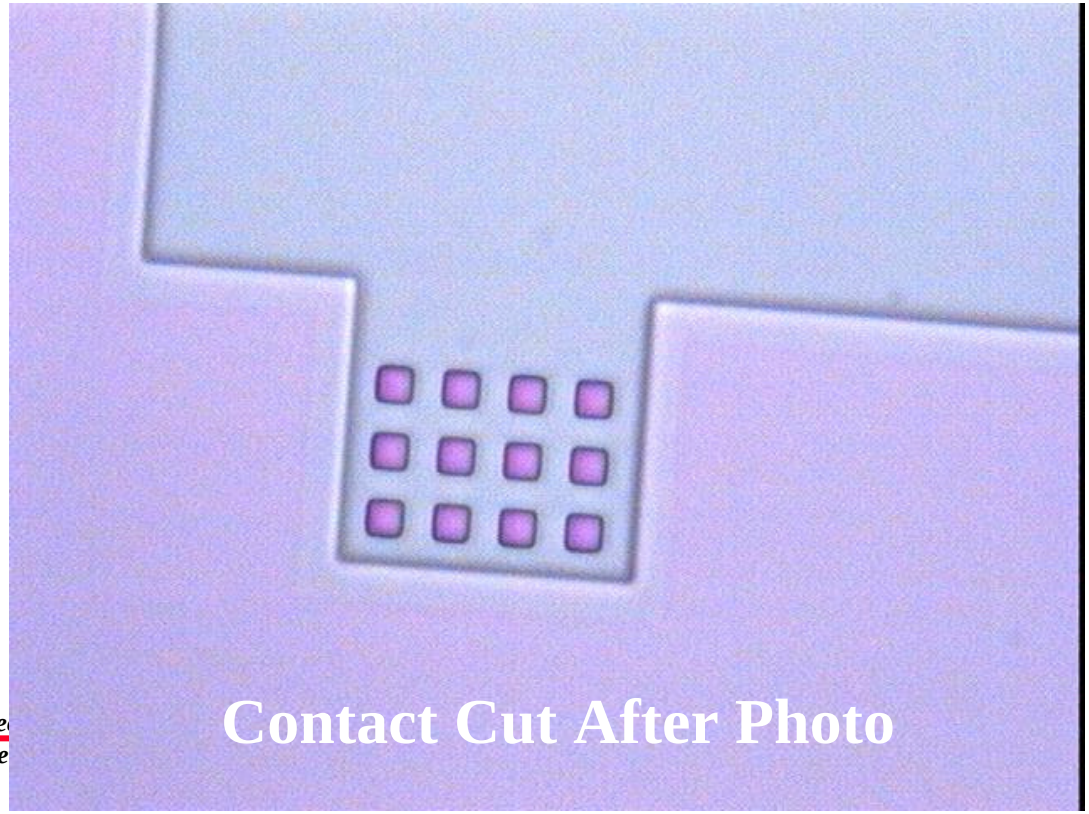
MAKING SMALL (2µm x 2µm) CONTACT CUT BY WET ETCH

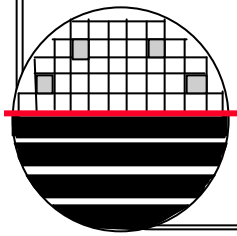
Contact Cut Lithography is difficult because of the complicated film stack. The contacts are through 4000Å TEOS oxide on thermal oxide on poly on gate oxide. The poly has a silicide layer in the Advanced CMOS process. The poly thickness might be 4000Å or 6000Å. The TEOS may be annealed. Other contacts are to drain and source through 4000Å TEOS on thermally grown oxide of ~500Å (from poly reox step) plus gate oxide. The gate oxides are 330Å, 150Å, or 100Å depending on the exact process.

Contact cut etch is also difficult. Plasma etch is difficult because of the different oxide layers and thickness and the poor selectivity between etching oxide and the underlying poly or drain/source silicon. Wet etch has problems with blocking. That is where the BOE can not get into the small contact cut openings. Blocking depends on surface tension as measured by the wetting angle which depends on the type of photoresist used.

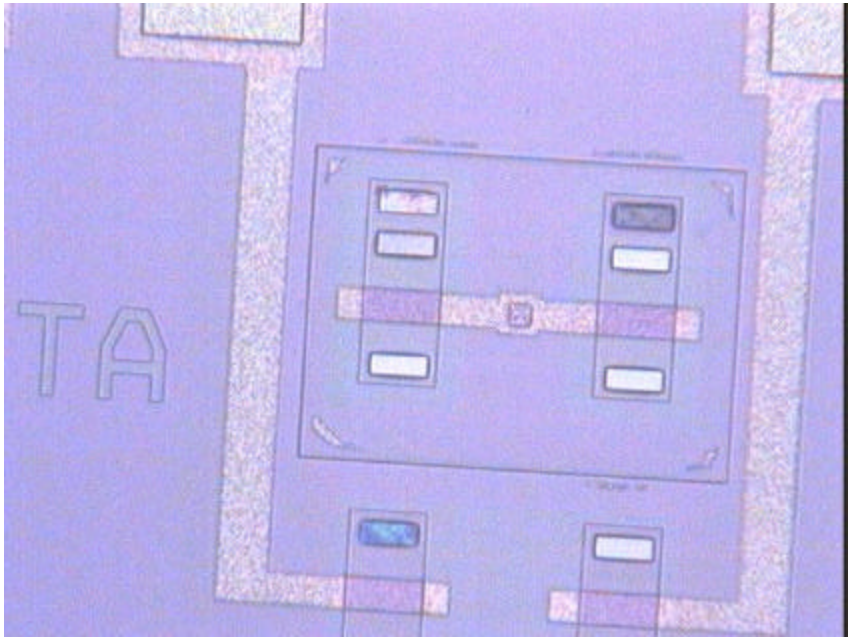
MAKING SMALL (2µm x 2µm) CONTACT CUT BY WET ETCH

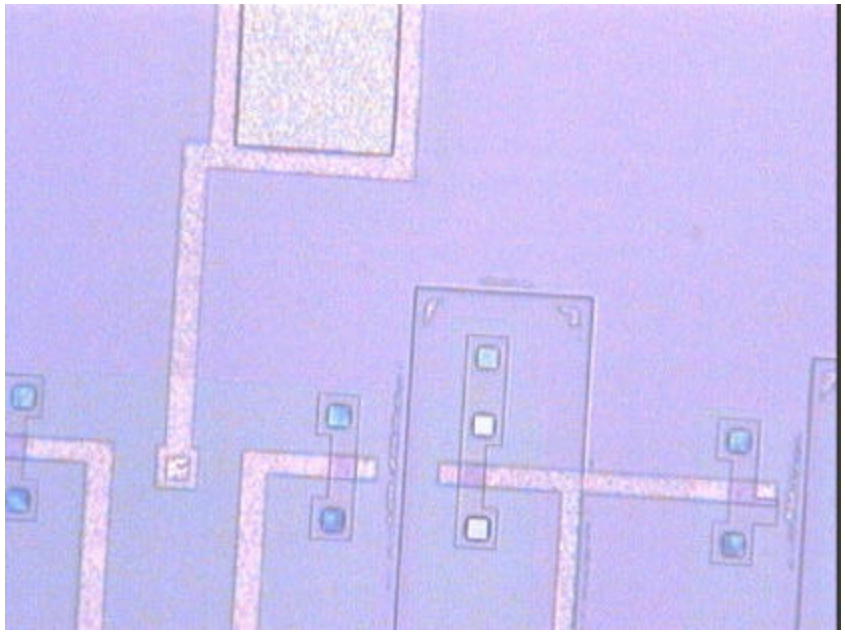
To ensure that the photoresist is cleared in the bottom of all the contact cuts the exposure dose is increased to 285 mj/cm2 and track develop time is increased to 3 min. This makes the 2µm x 2µm contacts a little larger ~2.2µm by ~2.2µm but they are clear regardless of the underlying film stack.





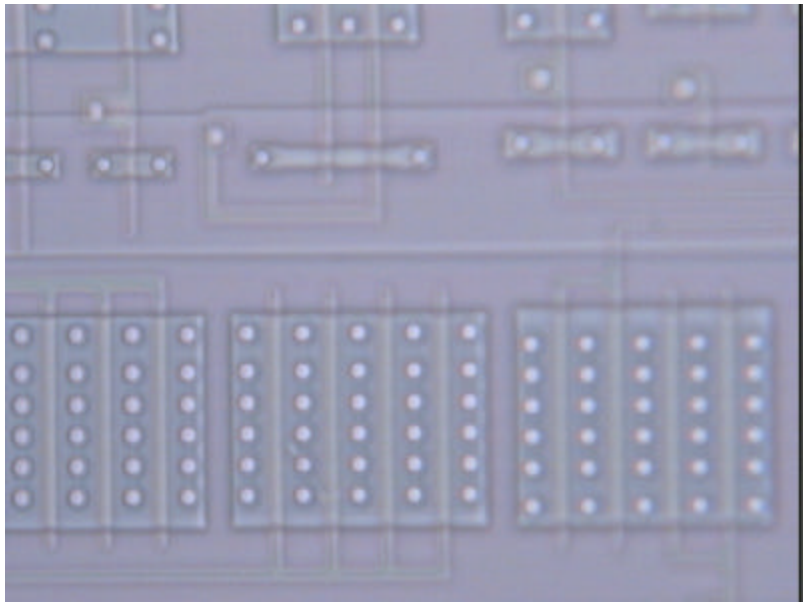
MAKING SMALL (2µm x 2µm) CONTACT CUT BY WET ETCH

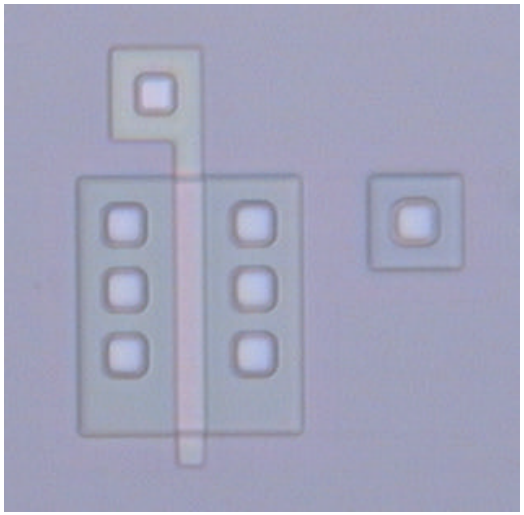




Wet etch has problems with blocking. That is where the BOE can not get into the small contact cut openings. Blocking depends on surface wetting angle. If blocking occurs some contact cuts will etch and clear while others will not etch as illustrated in the pictures above.

MAKING SMALL (2µm x 2µm) CONTACT CUT BY WET ETCH

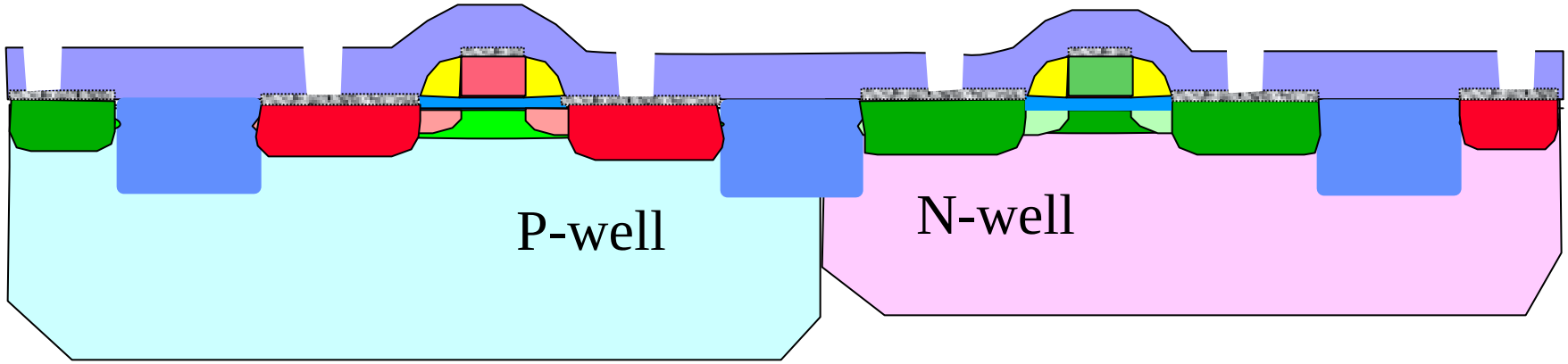




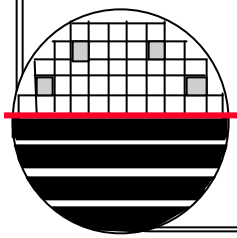
To overcome the blocking problem we raised the boat completely out of the BOE every 15 seconds throughout the entire etch. To be sure to clear all the contacts the etch time was extended to 5 minutes (approximately twice the expected etch time based on etch rates and approximate film thicknesses) This approach gave excellent results for all the various film stacks as shown in the pictures above.

Microelectronic Engineering

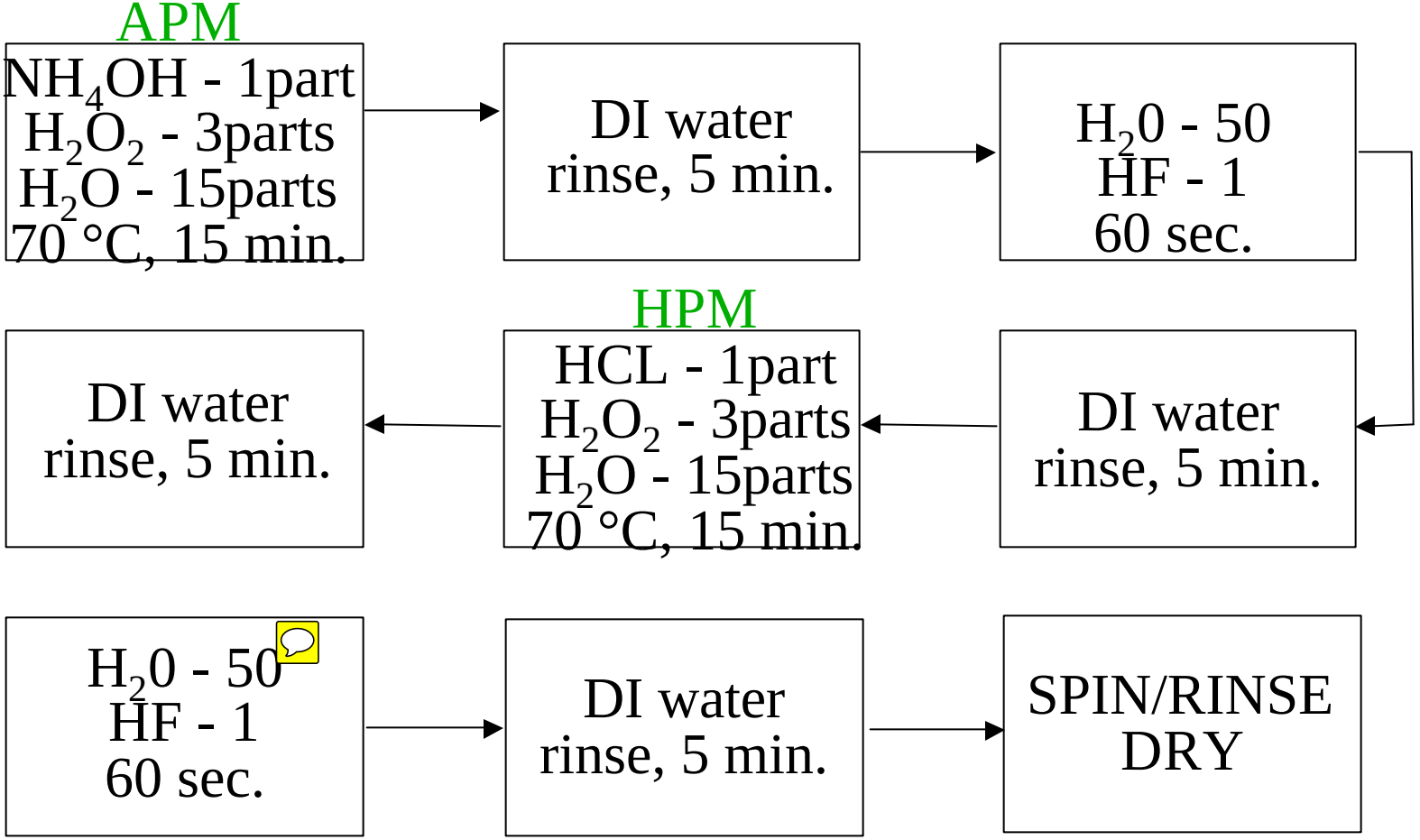
STRIP RESIST



Include D1-D3
Strip Photresist in Branson Asher

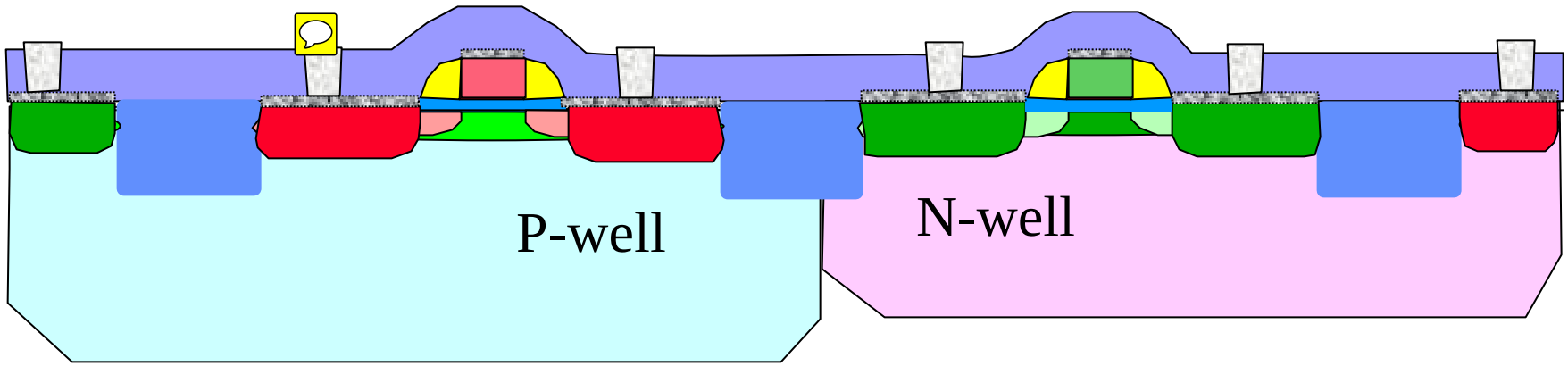


RCA CLEAN



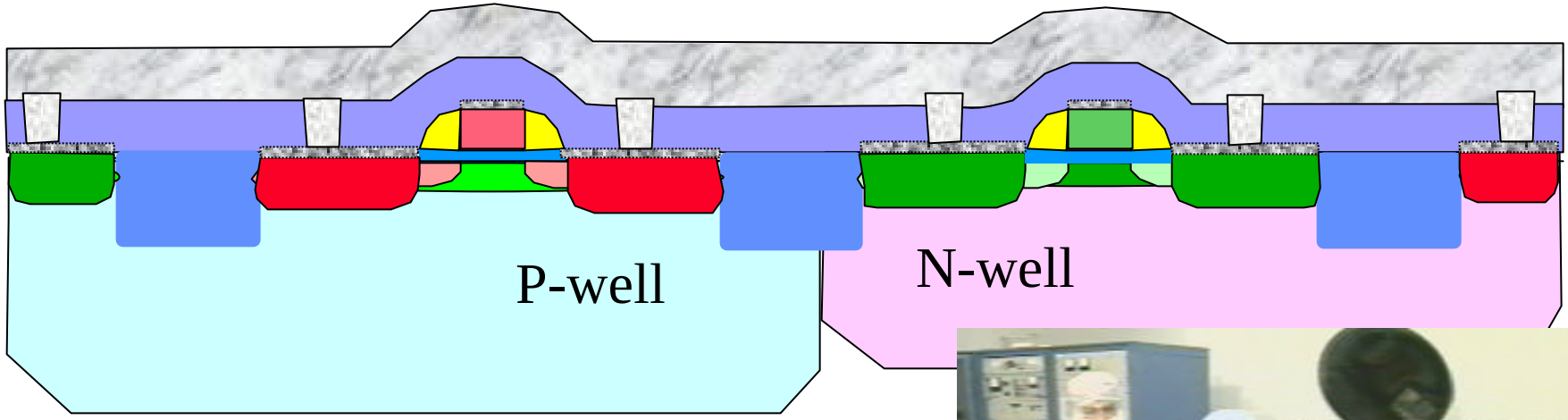
Clean includes 50:1 HF Dip twice once after each bath to remove chemically grown oxide

LPCVD TUNGSTEN PLUGS



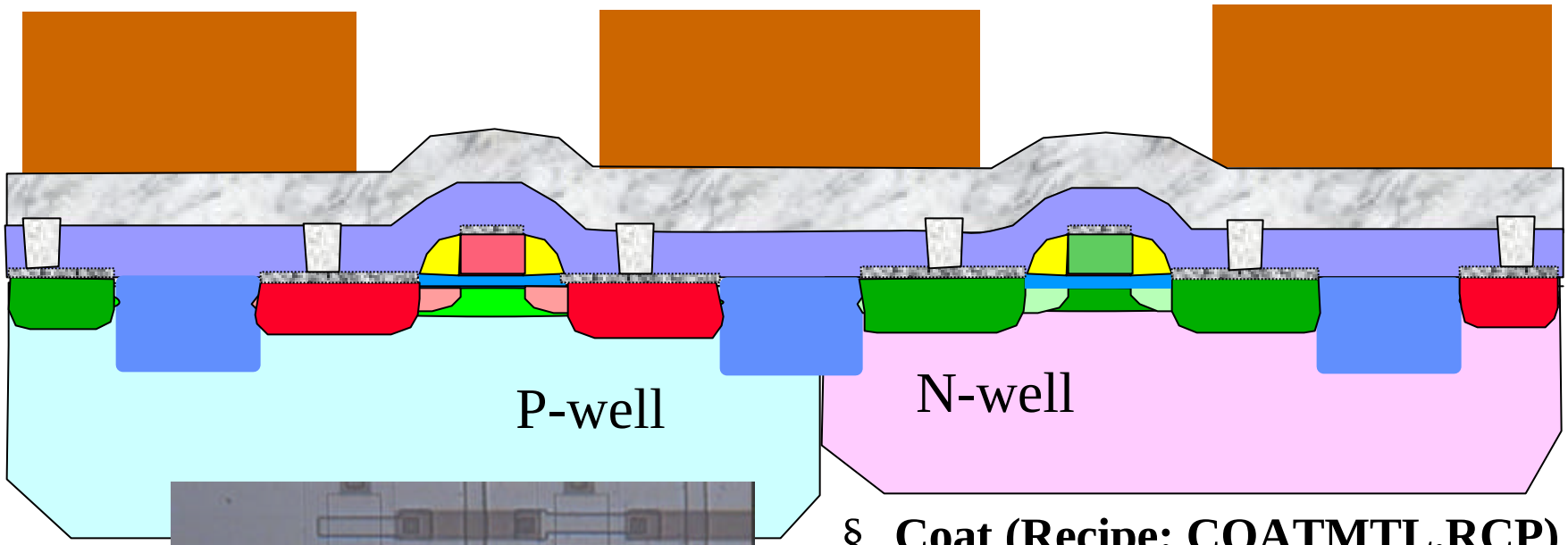
DEPOSIT ALUMINUM

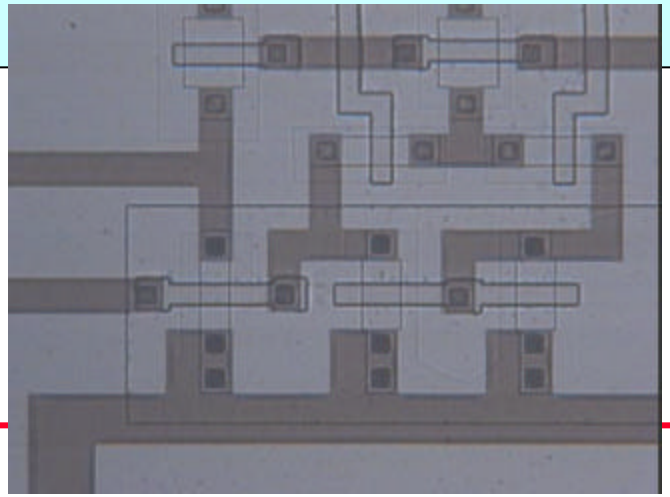
0.75 µm Aluminum



CVC 601 Sputter Tool

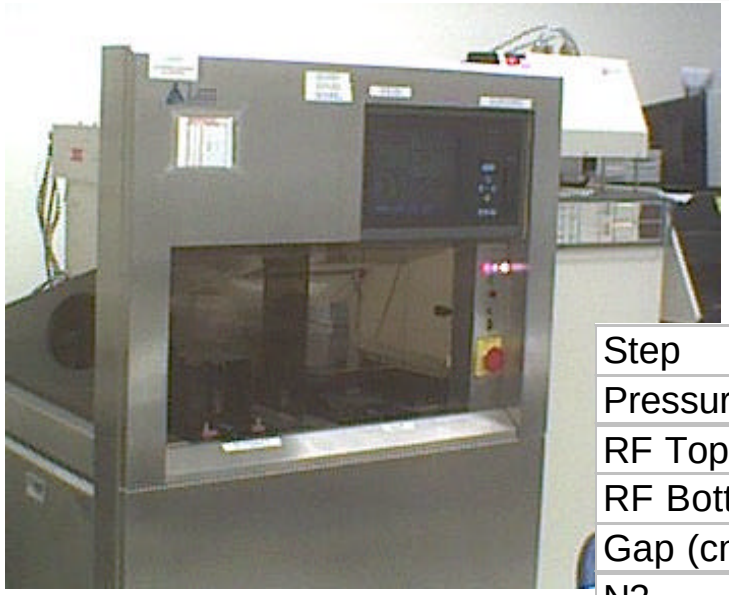
PHOTO 11 METAL ONE





- **Coat (Recipe: COATMTL.RCP)**
  - 400RPM for 2 seconds
  - 2000RPM for 30 seconds
  - Thickness of 13127A
- **Exposure**
  - Energy: 140mJ/cm2
  - Focus: 0.24um
- **Develop (Recipe: DEVMTL.RCP)**
  - Dispense 7 seconds
  - Wait 68 seconds
  - Hard Bake 2 min.

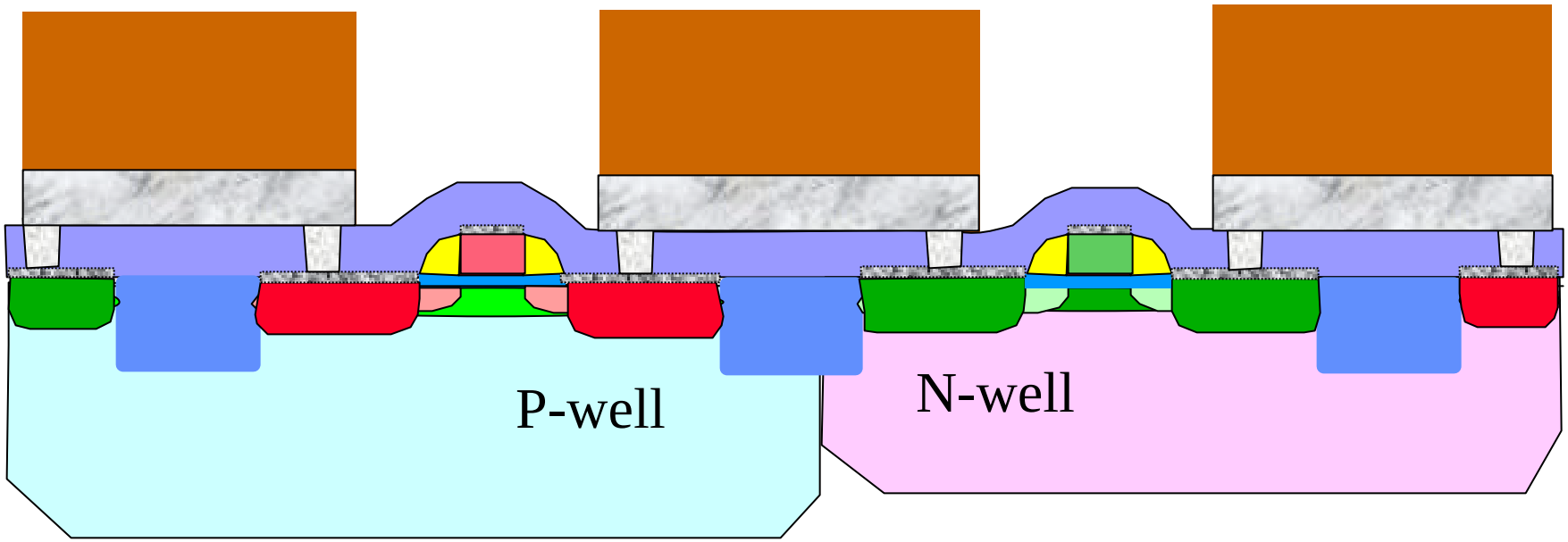
ALUMINUM ETCH



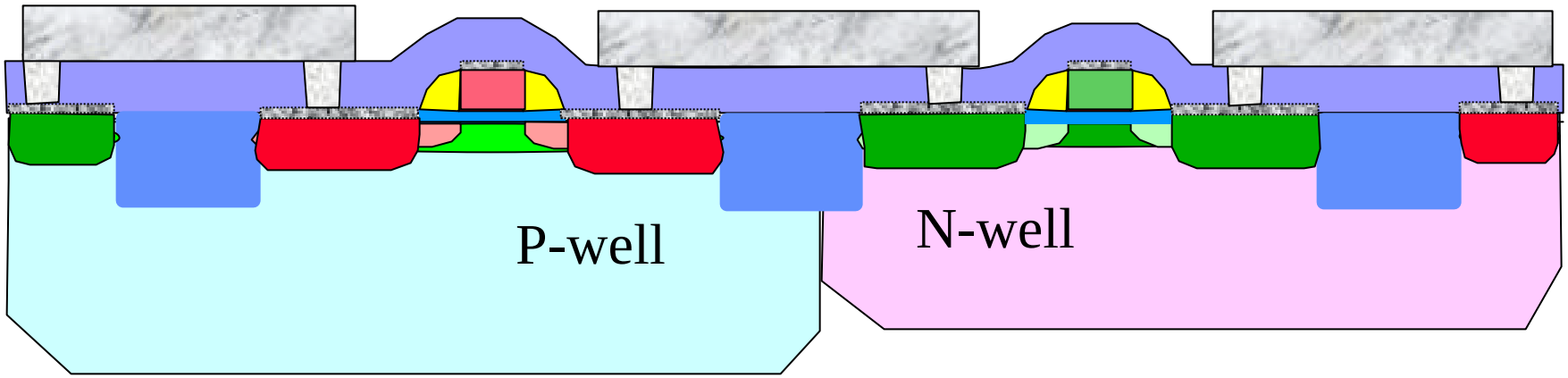
LAM 4600 Aluminum Etch Tool

Step	1	2	3	4	5
Pressure (mtorr)	300	300	300	300	0
RF Top (W)	0	0	0	0	0
RF Bottom (W)	0	250	125	125	0
Gap (cm)	3	3	3	3	5.3
N2	25	25	40	50	50
BCl3	100	100	50	50	0
Cl2	10	10	60	45	0
Ar	0	0	0	0	0
CFORM	15	15	15	15	15
Complete	Stabl	Time	endpoint	Oetch	time
time (s)	15	8	120	25%	15

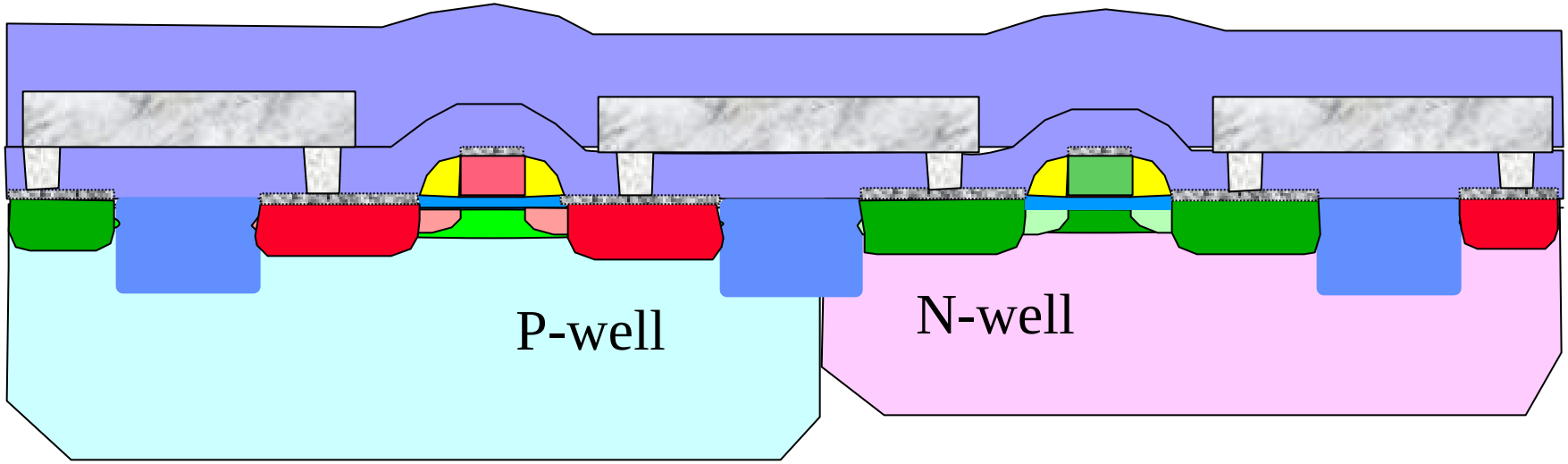
ALUMINUM ETCH



RESIST STRIP



LTO



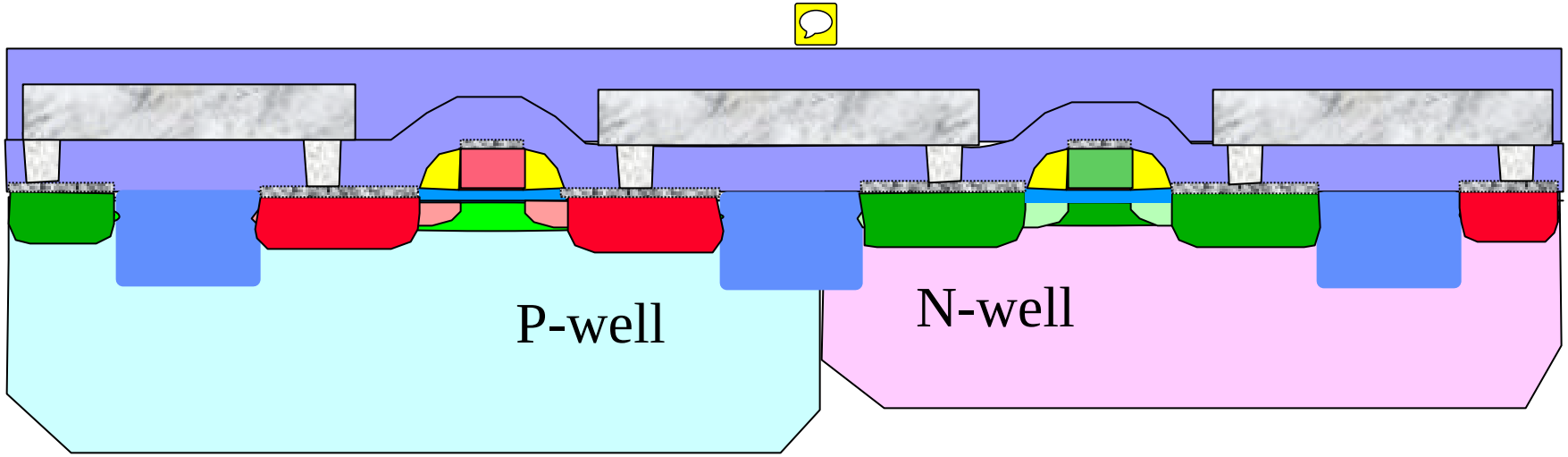
PECVD OXIDE FROM TEOS

TEOS Program: (Chamber A)
Step 1
- Setup Time = 15 sec
- Pressure = 9 Torr
- Susceptor Temperature= 390 C
- Susceptor Spacing= 220 mils
- RF Power = 0 watts
- TEOS Flow = 400 scc
- O2 Flow = 285 scc

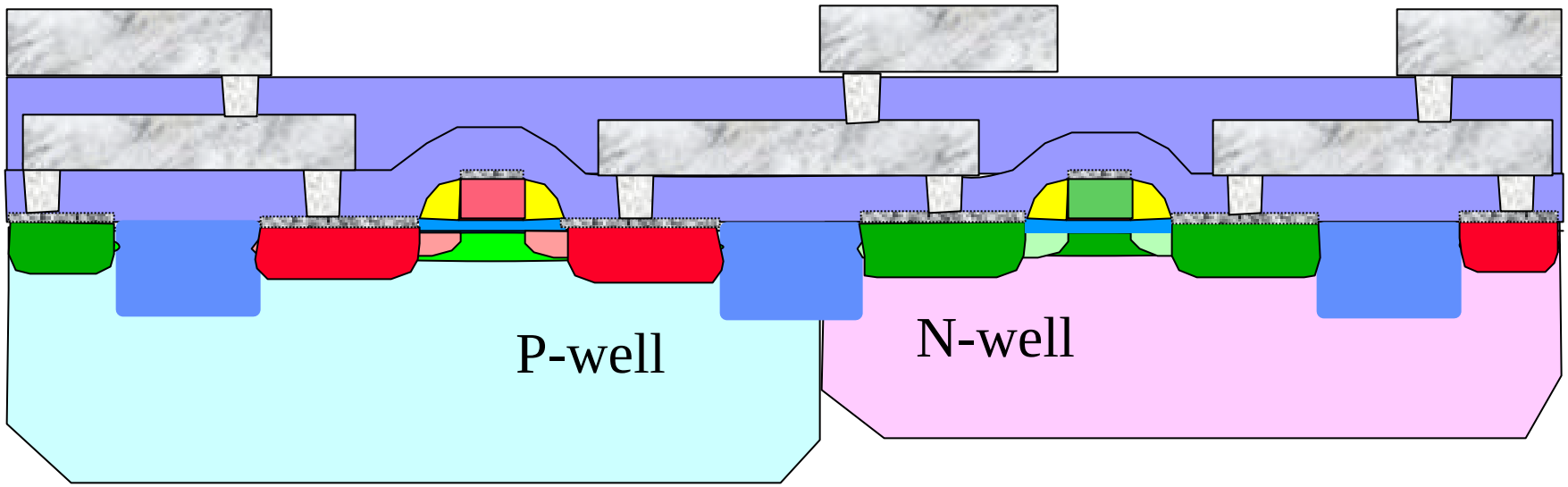
Step 2 – Deposition
- Dep Time = 55 sec (5000 Å)
- Pressure = 9 Torr
- Susceptor Temperature= 390 C
- Susceptor Spacing= 220 mils
- RF Power = 205 watts
- TEOS Flow = 400 scc
- O2 Flow = 285 scc

Step 3 – Clean
- Time = 10 sec
- Pressure = Fully Open
- Susceptor Temperature= 390 C
- Susceptor Spacing= 999 mils
- RF Power = 50 watts
- TEOS Flow = 0 scc
- O2 Flow = 285 scc

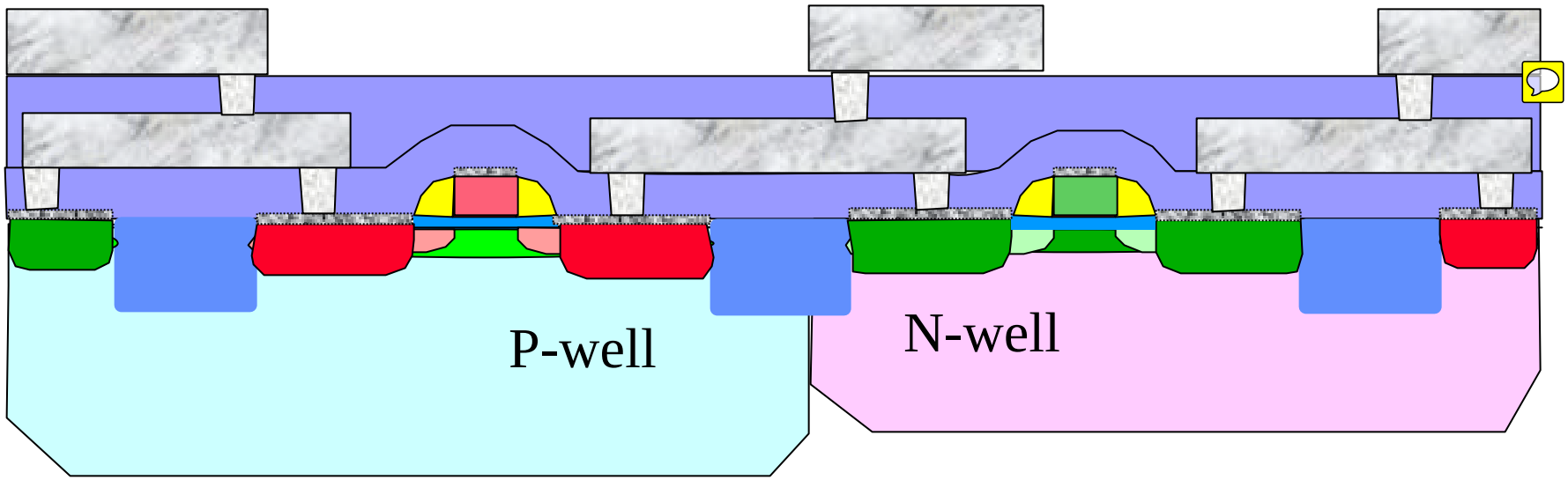
CMP



VIA, TUNGSTEN PLUGS, ALUMINUM, AL ETCH



SINTER



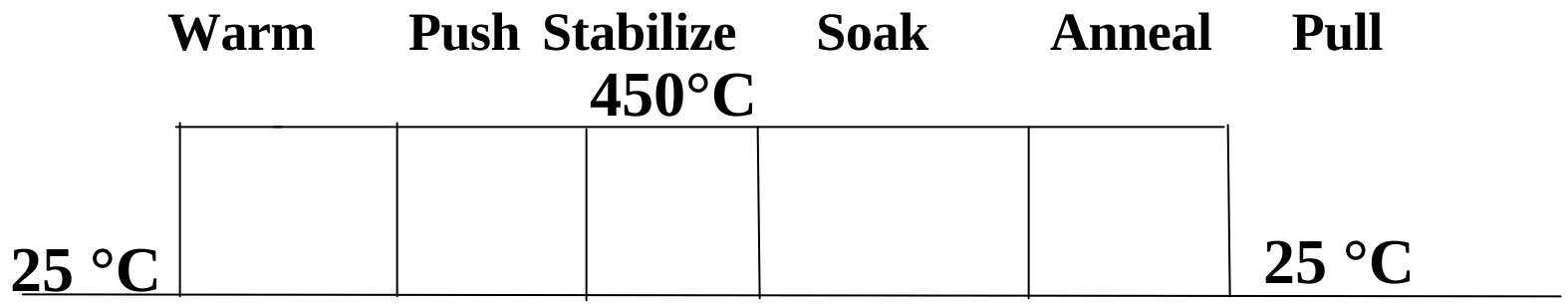
Bruce Furnace 02

Recipe 101: 450C, H_2N_2, 30min

BRUCE FURNACE RECIPE 101 SINTER

SINTER Recipe #101

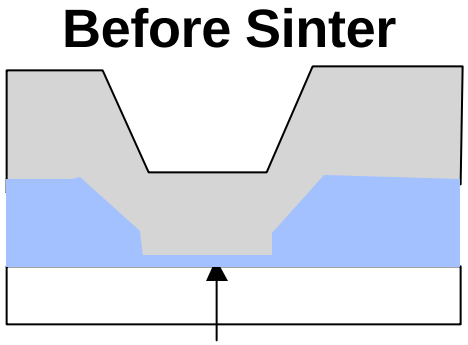
Verified:2-24-04



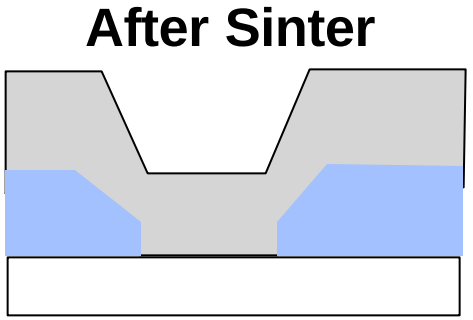
Interval	0	1	2	3	4	5	6	
Any`		90	12	15	30	5	15	min
0 lmp		10	10	10	5	10	5	lpm
None		N2	N2/H2	N2/H2	N2/H2	N2	N2	

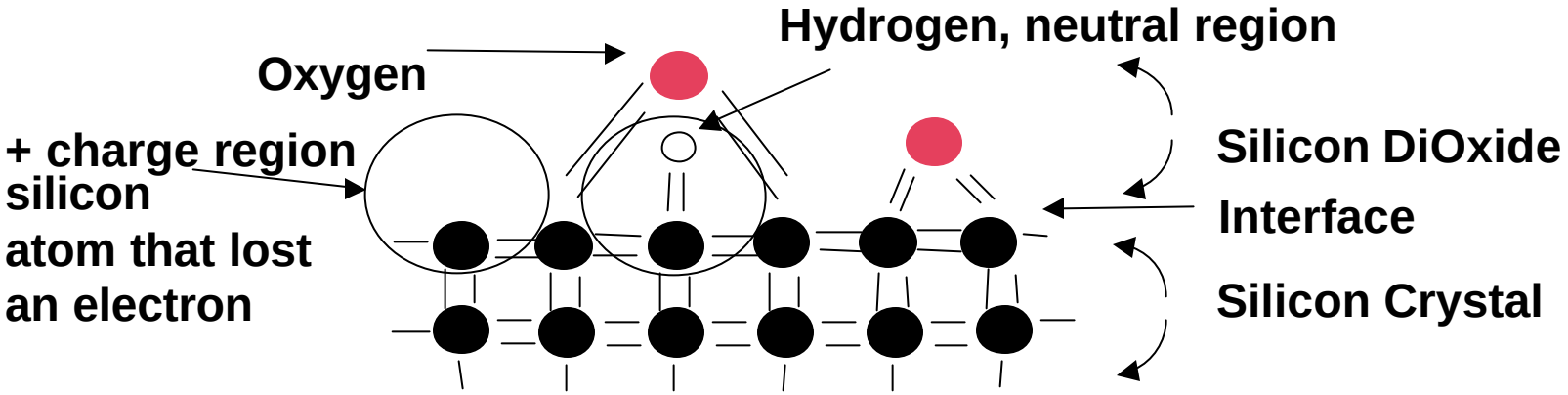
At the end of a run the furnace returns to Interval 0 which is set for boat out, 25 °C and no gas flow. The furnace waits in that state until someone aborts the current recipe or loads a new recipe.

SINTER



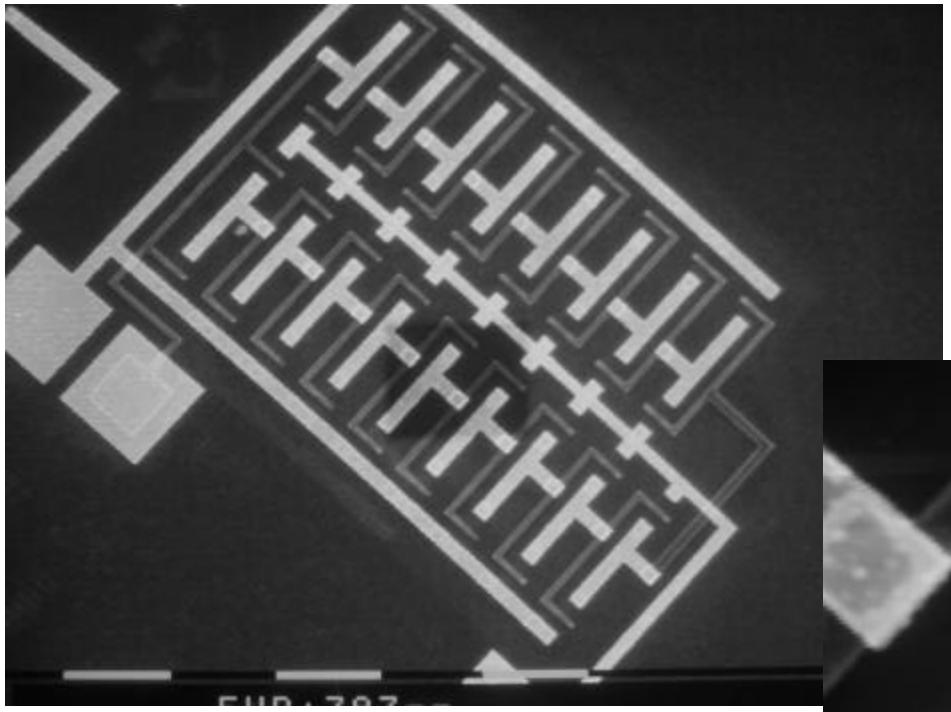
Reduce Contact Resistance

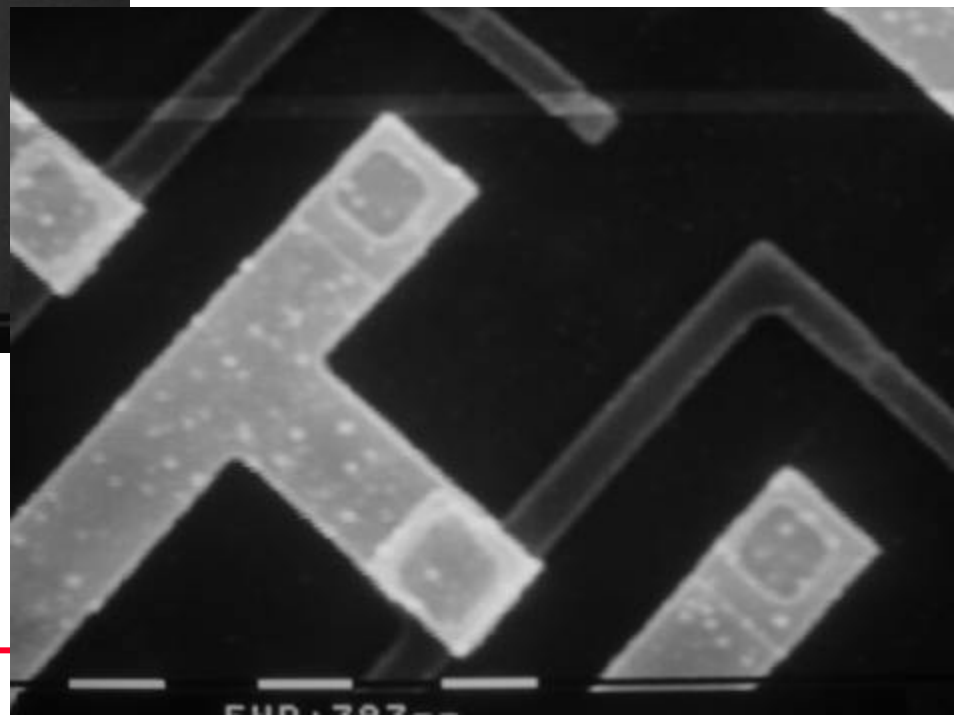


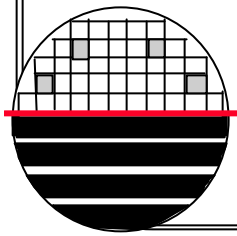


Reduce Surface States

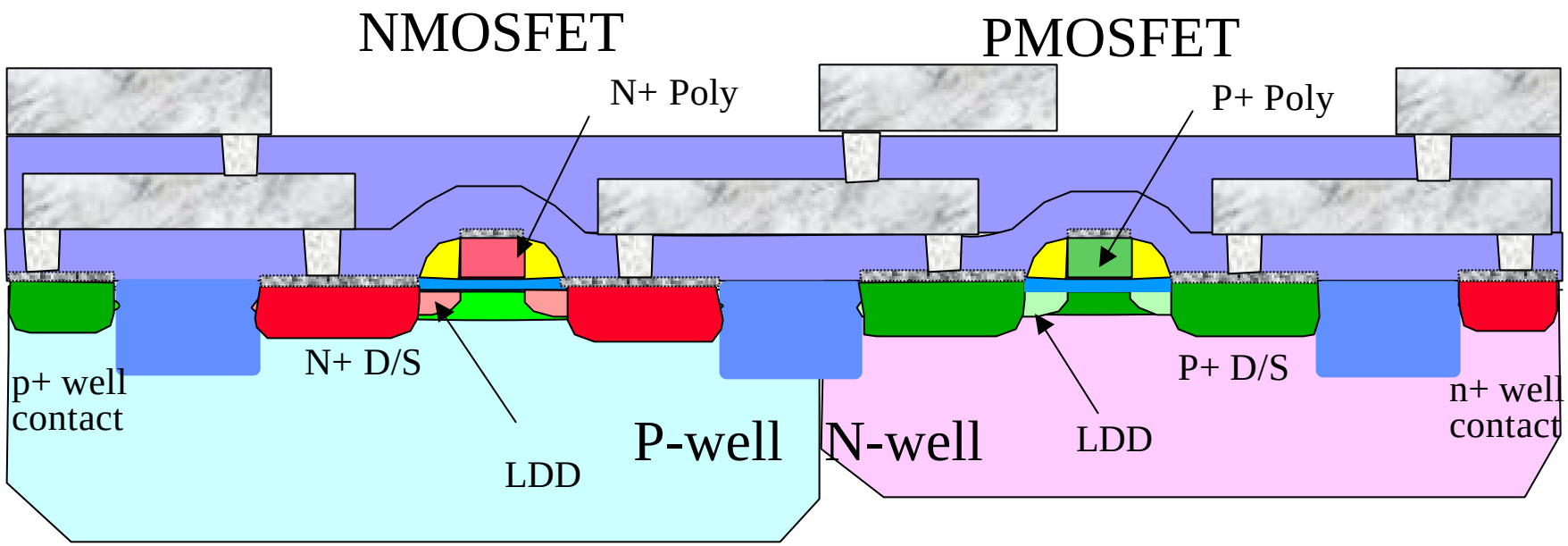
TAKE SEM PICTURES OF RING OSCILLATOR







ADV-CMOS 150



MESA WIPTRACKING SYSTEM

The process is long and complicated and will take many months to complete each lot. A computerized record keeping system is required to provide instructions and collect data. MESA (Manufacturing Execution System Application) from Camstar, Inc. runs on our AS/400 computer.

SUB MICRON CMOS PROCESS

```
  5/10/01                              MESA                    PCMSINQ    S35401
 14:01:59                      Process Master Inquiry          MICROGURU    RIT

Type information.  Then Enter, or use Roll keys to page.

  Plant  . . . . . :   RIT
  Process/rev  . . . . .   SUB-CMOS   1.0  SUB-MICRON TWIN WELL CMOS 4 INCH WAF

  5=Display                VI=View instructions     VO=View operation
  VS=View spec             VP=View parameters       VM=View move-in ...
                                                Position to  . . . . .  ________
  Opt Seq#     Operation       Spec ID              Rev  Spec description
  __    61.00  ET10 LTO ETCH   SUB-CMOS-ET10-CC     1.0  SUB-CMOS ETCH CC
  __    62.00  ET07 STRIP      SUB-CMOS-ET07-CC     1.0  SUB-CMOS ASH RESIST
  __    63.00  CL01 RCA CLEAN  SUB-CMOS-CL01-METAL  1.0  SUB-CMOS CL01 METAL
  __    64.00  ME01 AL DEPOSIT SUB-CMOS-ME01        1.0  SUB-CMOS ME01 AL DEP
  __    65.00  PH03 PHOTOLITH  SUB-CMOS-PH03-METAL  1.0  SUB-CMOS PH03 METAL
  __    66.00  ET05 AL ETCH    SUB-CMOS-ET05        1.0  SUB-CMOS AL ETCH
  __    67.00  ET07 STRIP      SUB-CMOS-ET07-METAL  1.0  SUB-CMOS ASH RESIST
  __    68.00  SI01 SINTER     SUB-CMOS-SI01        1.0  SUB-CMOS SI01 SINTER
  __    69.00  TE01 TEST RES   SUB-CMOS-TE01        1.0  SUB-CMOS TE01
  __    70.00  TE02 TEST XTR   SUB-CMOS-TE02        1.0  SUB-CMOS TE02       +
F2=Fold   F3=Exit   F4=Prompt   F12=Cancel   F23=More options   F24=More keys
```

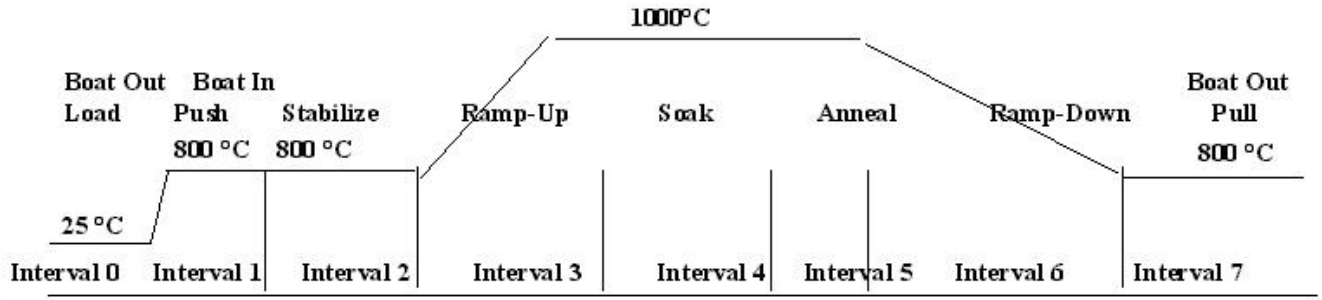
INSTRUCTIONS

```
    5/10/01                          MESA                    IGMSINQ    S36801
   14:05:05                 Instruction Group Inquiry        MICROGURU    RIT

Type information.  Then Enter.
  1=Display document, 5=Display detail

  Plant  . . . . . :   RIT
  Instruction group  . .   CMOS-OX04-ALIGNMENT   CMOS OX04 ALIGNMENT OXIDE
    Revision . . . . .   3.0

  Opt Subgroup  Text
   _            1.0 Include D1-D3
   _            2.0 Use resource FURNACE01 BRUCE TUBE 01  (see OX04.pps)
   _            3.0 Xox desired = 5000 A (see WellOx.pps)
   _            4.0 See SPC chart for operation (align_ox.pps)- execute step
   _            5.0 XRF warm up recipe 888, check gas & hydrogen supply
   _            6.0 When furnace stabilizes at 800 C
   _            7.0 XRF 5000 A wet O2 recipe 350, load wafers, press start
   _                P/P 800C, RU 20min, 120 min soak wet O2 1000C, RD 40 min
   _            8.0 When wafers complete, abort 350 and XRF idle recipe 999
   _            9.0 Record 3-zone temp, soak time, oxide thickness on D1 (se
                                                                      More...
F3=Exit    F4=Prompt    F5=Refresh    F10=View 2    F12=Cancel

MA    a                                                          12/005
```

IMAGE DOCUMENTS

BRUCE FURNACE RECIPES

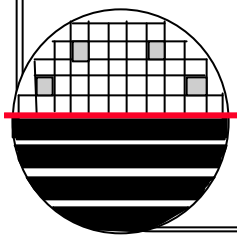
Recipe #350



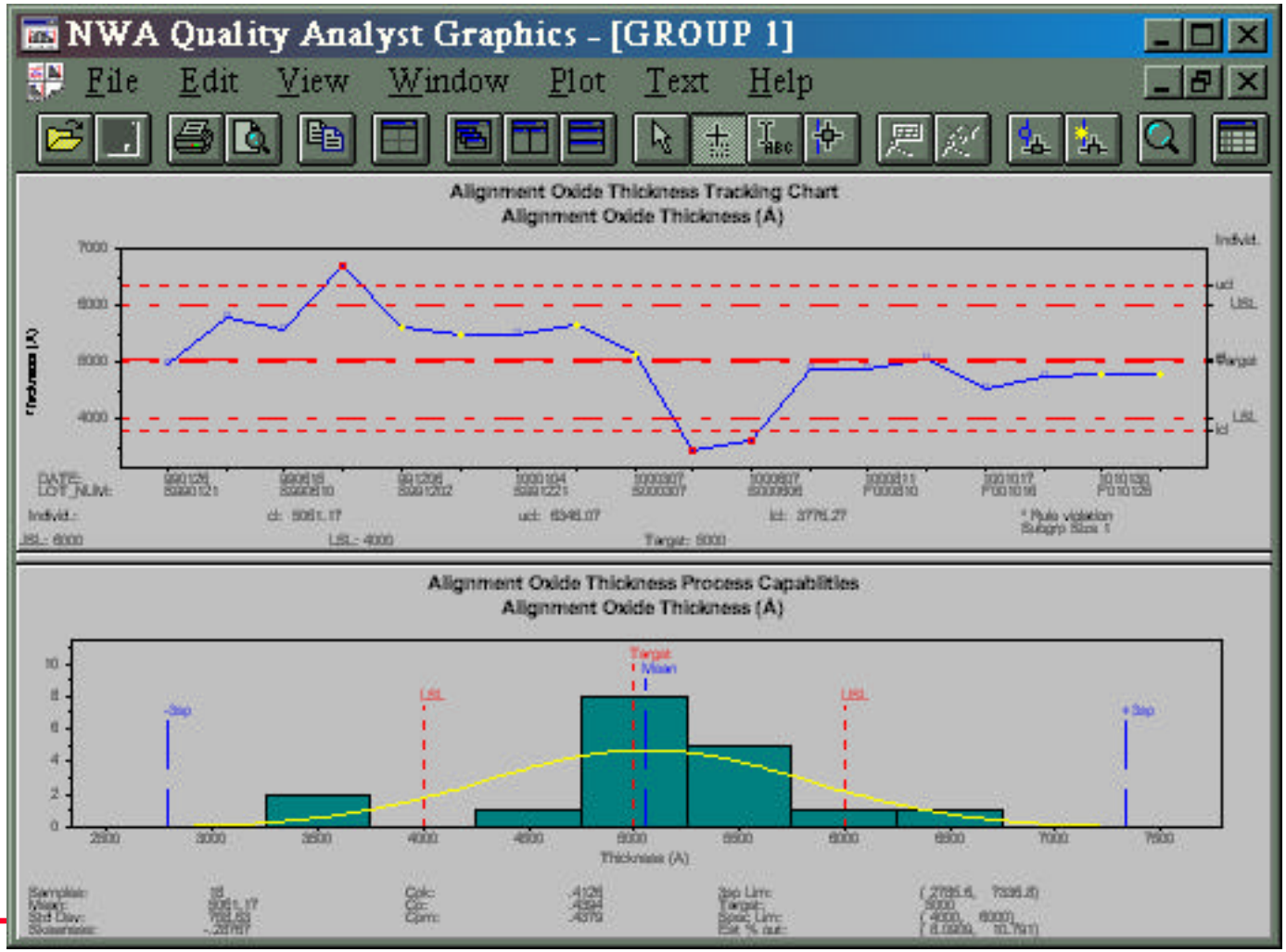
Any	12 min	15 min	20 min	120min	5 min	40 min	12 min
0 lpm	15 lpm	15 lmp	10 lpm	10 lpm	15 lpm	10 lpm	15 lpm
none	N2	N2	O2	O2	N2	N2	N2

At the end of a run the furnace returns to Interval 0 which is set for boat out, 25 °C and no gas flow. The furnace waits in that state until someone aborts the current recipe or loads a new recipe.

WIPTRACKING

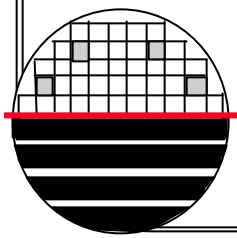


SPC CHARTS


NWA Quality Analyst Graphics - [GROUP 1]
File Edit View Window Plot Text Help
Alignment Oxide Thickness Tracking Chart
Alignment Oxide Thickness (A)
Alignment Oxide Thickness Process Capabilities
Alignment Oxide Thickness (A)

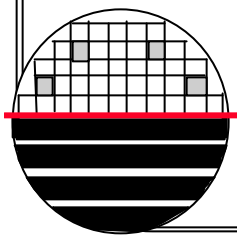
SUMMARY

The process described can be used down to ~0.5 µm gate length.



REFERENCES

- Silicon Processing for the VLSI Era, Volume 1 – Process Technology, 2nd, S. Wolf and R.N. Tauber, Lattice Press.
- The Science and Engineering of Microelectronic Fabrication, Stephen A. Campbell, Oxford University Press, 1996.



HOMEWORK – RIT ADVCMOS2003

1. Why do we want the surface concentration under the shallow trench in the p-well to be above some given value?
2. Why are the well implant energies greater than 150 KeV?
3. When checking material thickness for the ability to block D/S implant, which implant type and which material is the most critical.
4. Why is a nitride spacer (instead of oxide) used.
5. What are the two main purposes of the silicide in this process?
6. Why is the gate doped N-type on the NMOS and P-type on the PMOS devices?
7. What is the poly sheet resistance?
8. What is the purpose of the N2O in the gate oxide growth recipe?