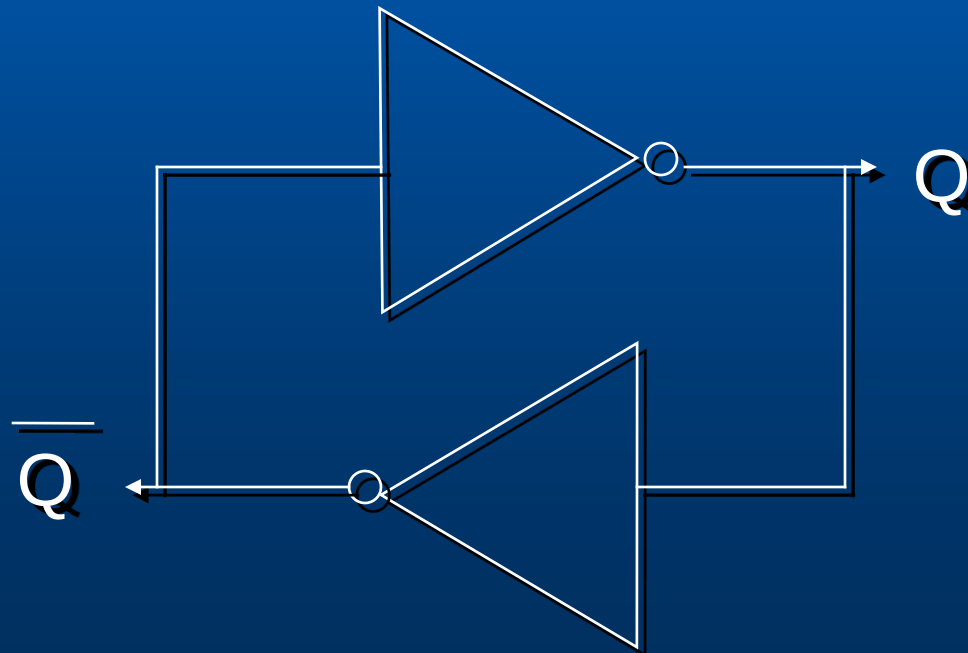


CIRCUITOS BIESTÁVEIS

Sel 414 - Sistemas Digitais

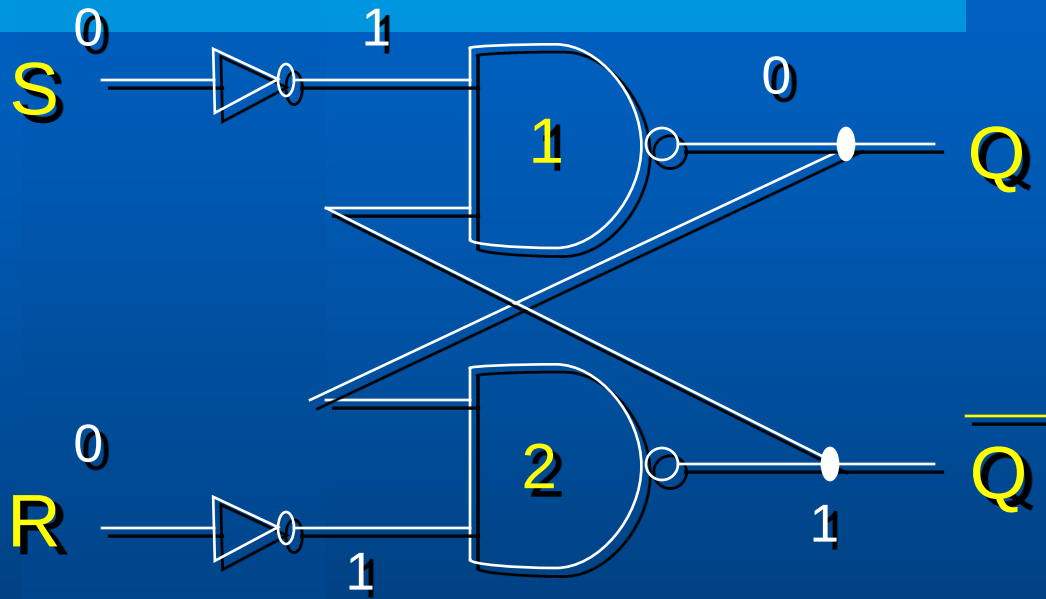
Prof. Homero Schiabel

LATCH RS



Latch RS

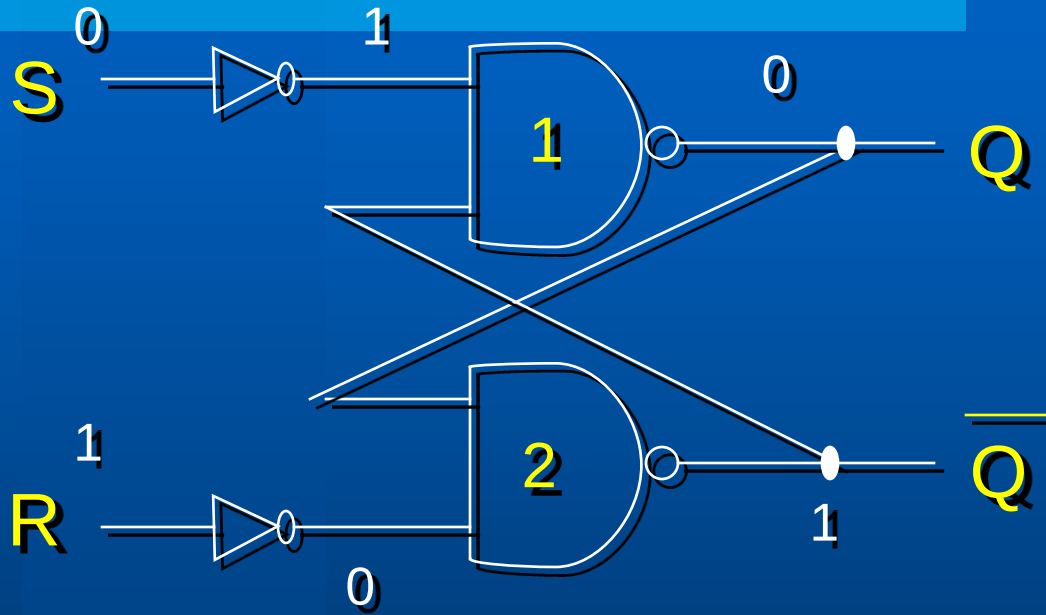
Condição Inicial → $Q = 0$



S	R	1	2	Q	$\overline{Q}$
0	0	1 1	0 1	0	1

Latch RS

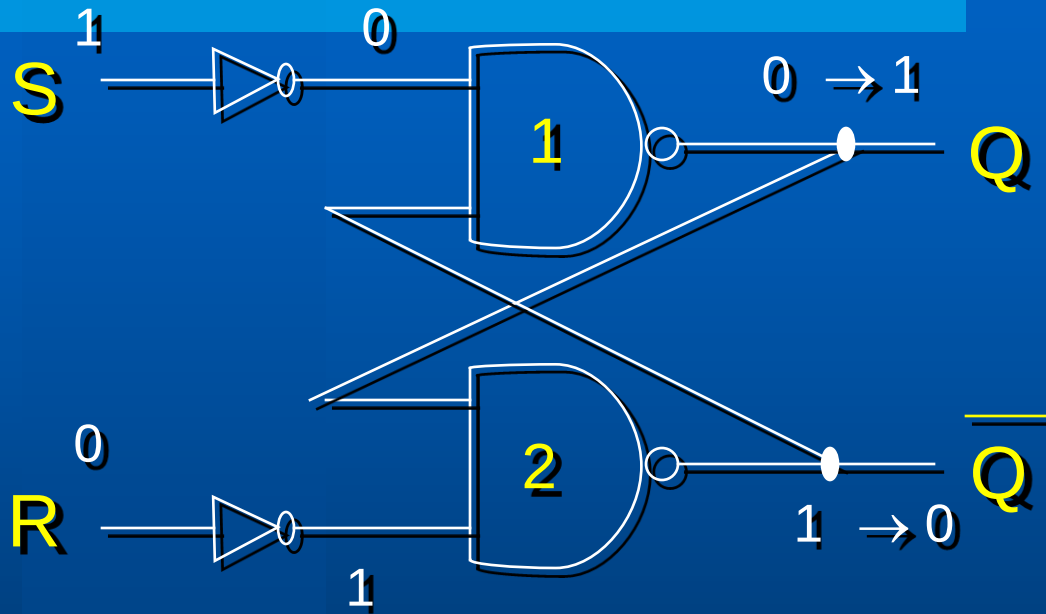
Condição Inicial → $Q = 0$



S	R	1	2	Q	$\overline{Q}$
0	0	1	0	0	1
0	1	1	0	0	1

Latch RS

Condição Inicial $\rightarrow Q = 0$

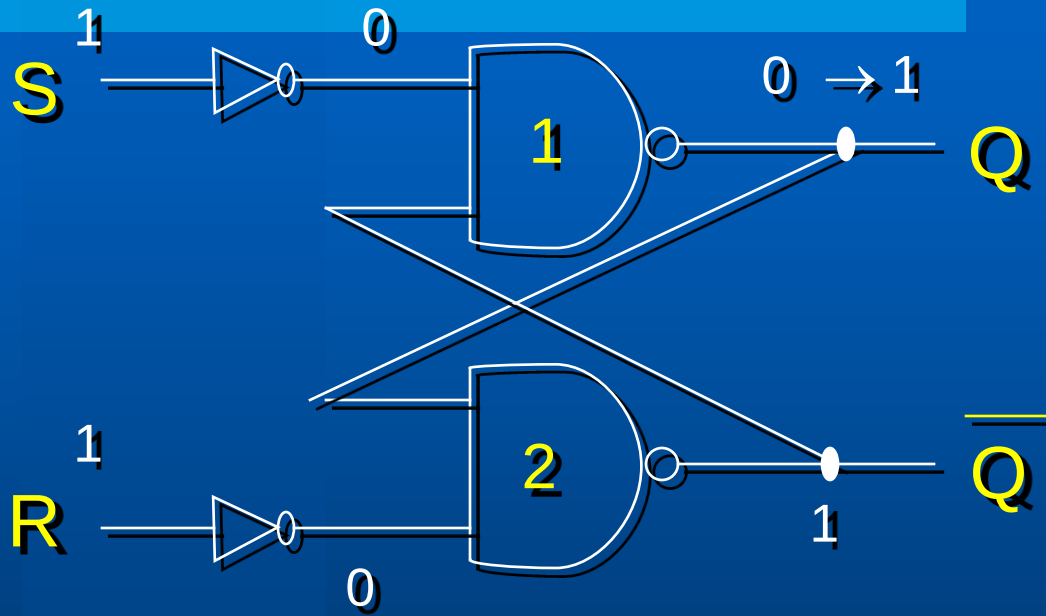


S	R	1	2	Q	$\overline{Q}$
0	0	1 1	0 1	0	1
0	1	1 1	0 0	0	1
1	0	0 1	0 1	1	1 *
		0 1	1 1	1	0

* Estado instável

Latch RS

Condição Inicial → $Q = 0$



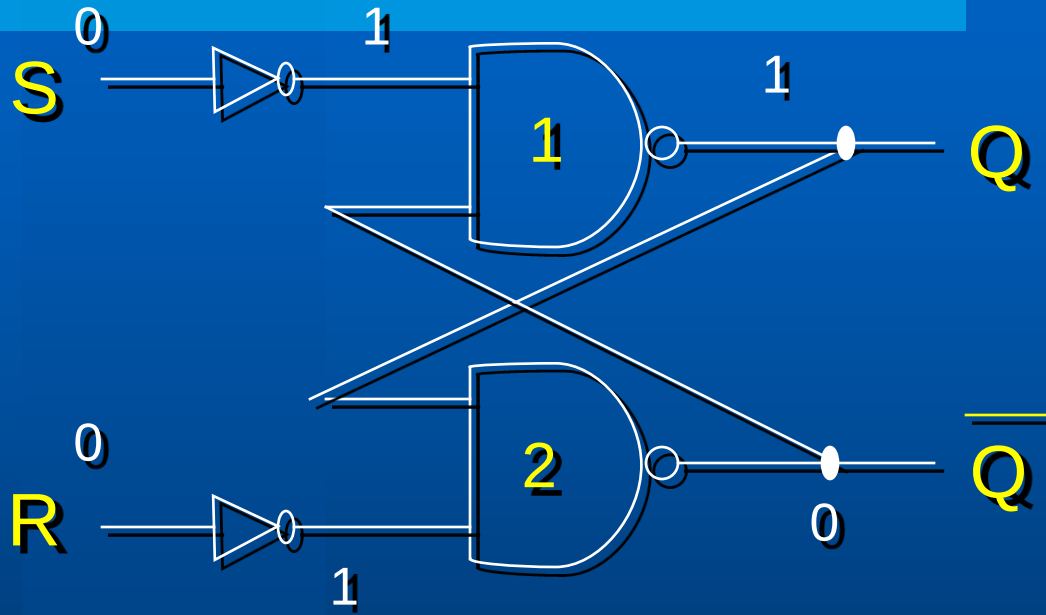
S	R	1	2	Q	$\overline{Q}$
0	0	1 1	0 1	0	1
0	1	1 1	0 0	0	1
1	0	0 1	0 1	1	1 *
		0 1	1 1	1	0
1	1	0 1	0 0	1	1
		0 1	1 0	1	1 **

* Estado instável

** “Incompatibilidade”
(Est. “proibido”)

Latch RS

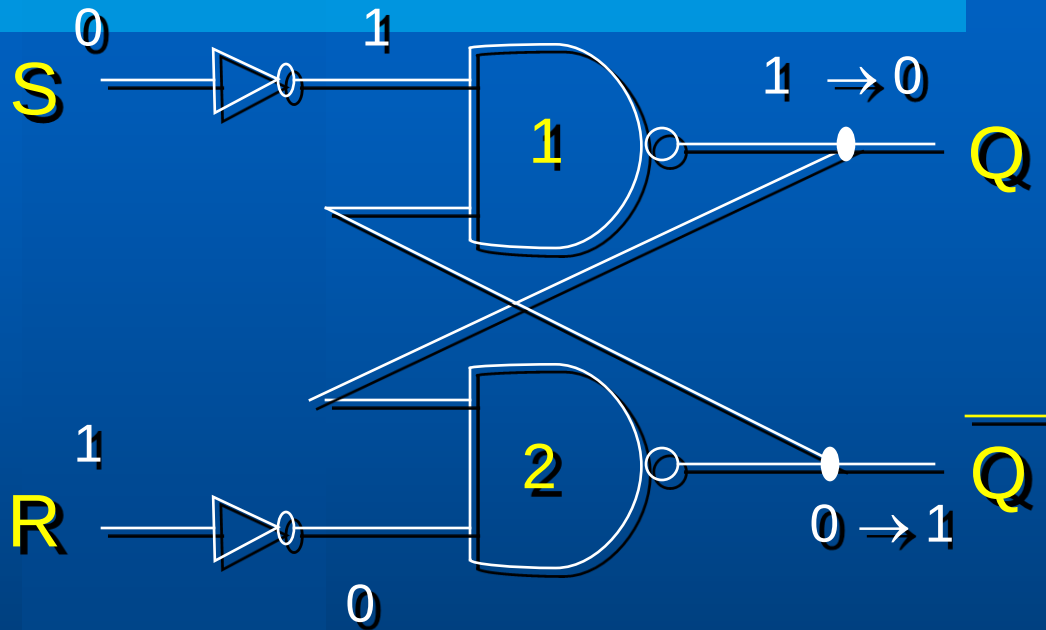
Condição Inicial → $Q = 1$



S	R	1	2	Q	$\overline{Q}$
0	0	1	0	1	0

Latch RS

Condição Inicial → $Q = 1$

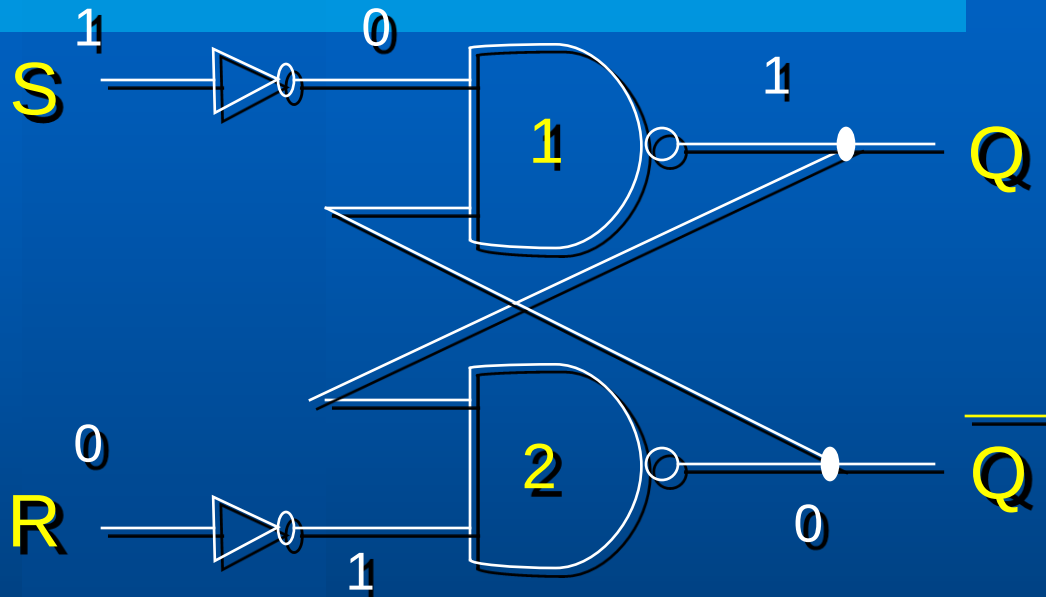


S	R	1	2	Q	$\overline{Q}$
0	0	1 0	1 1	1	0
0	1	1 0	1 0	1	1 *
		1 1	1 0	0	1

* Estado instável

Latch RS

Condição Inicial → $Q = 1$

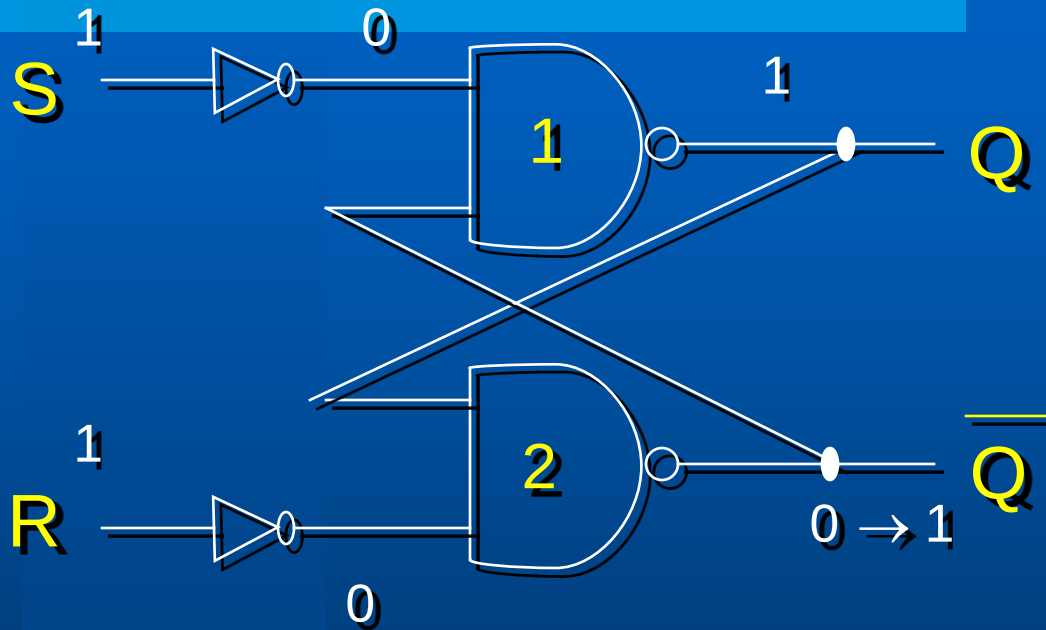


S	R	1	2	Q	$\overline{Q}$
0	0	1 0	1 1	1	0
0	1	1 0	1 0	1	1 *
		1 1	1 0	0	1
1	0	0 0	1 1	1	0

* Estado instável

Latch RS

Condição Inicial → $Q = 1$



S	R	1	2	Q	$\overline{Q}$
0	0	1 0	1 1	1	0
0	1	1 0	1 0	1	1 *
		1 1	1 0	0	1
1	0	0 0	1 1	1	0
1	1	0 0	1 0	1	1
		0 1	1 0	1	1 **

* Estado instável

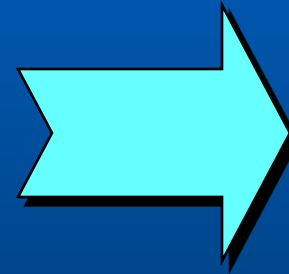
** “Incompatibilidade”
(Est. “proibido”)

Tabela da verdade:

 $Q = 0$
 $Q = 1$

S	R	Q	$\overline{Q}$
0	0	0	1
0	1	0	1
1	0	1	0
1	1	1	1**

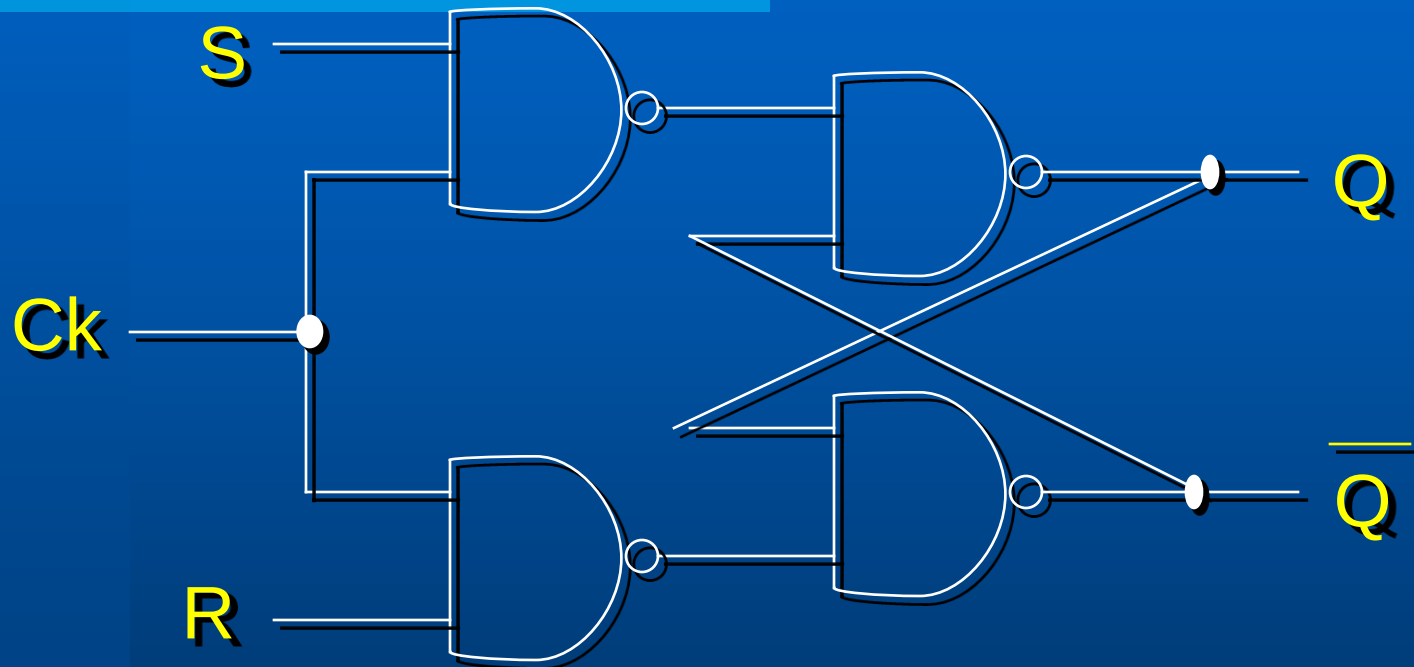
S	R	Q	$\overline{Q}$
0	0	1	0
0	1	0	1
1	0	1	0
1	1	1	1**



S	R	Q*
0	0	Q
0	1	0
1	0	1
1	1	1**

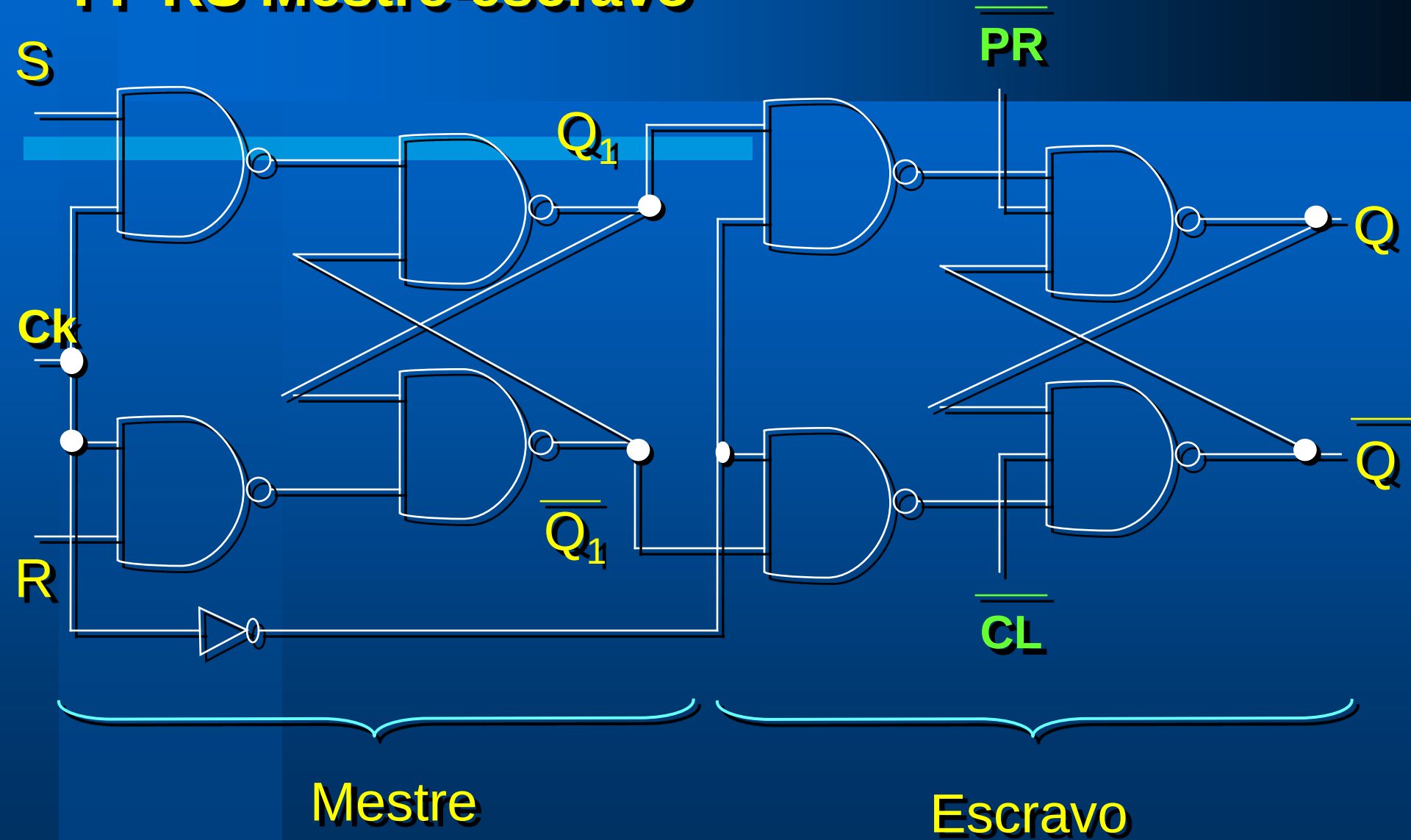
** “Incompatibilidade”
(Est. “proibido”)

RS Síncrono



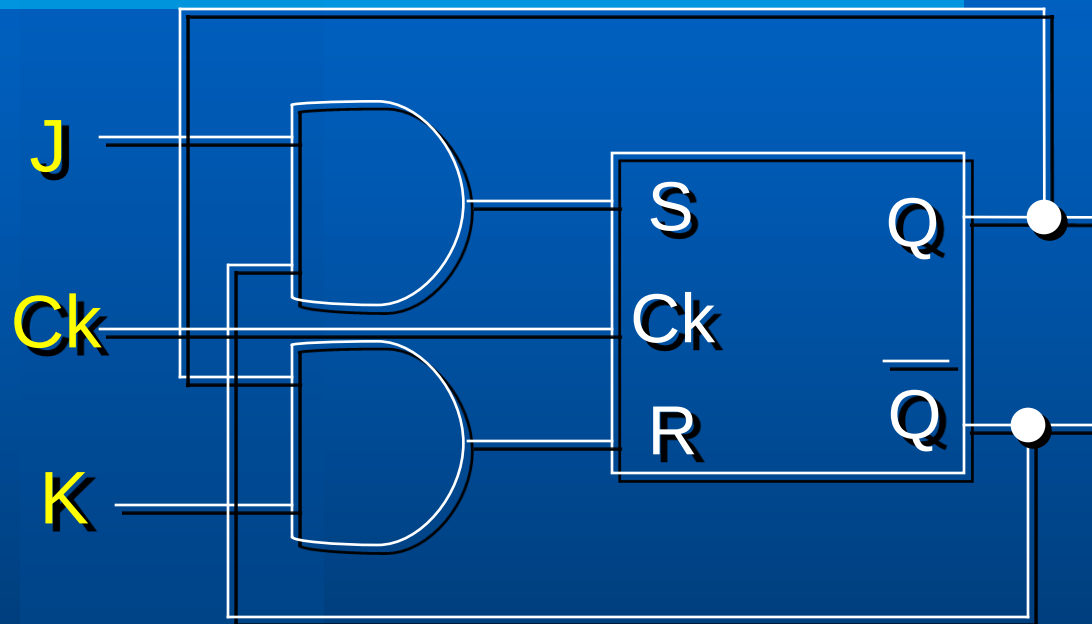
- Para $Ck=0 \rightarrow Q$ e $\overline{Q}$ não “sentirão” eventuais variações nas entradas
- Para $Ck=1 \rightarrow$ funcionamento normal (portas de entrada habilitadas)

FF RS Mestre-escravo



FLIP-FLOP JK

Flip-flop JK

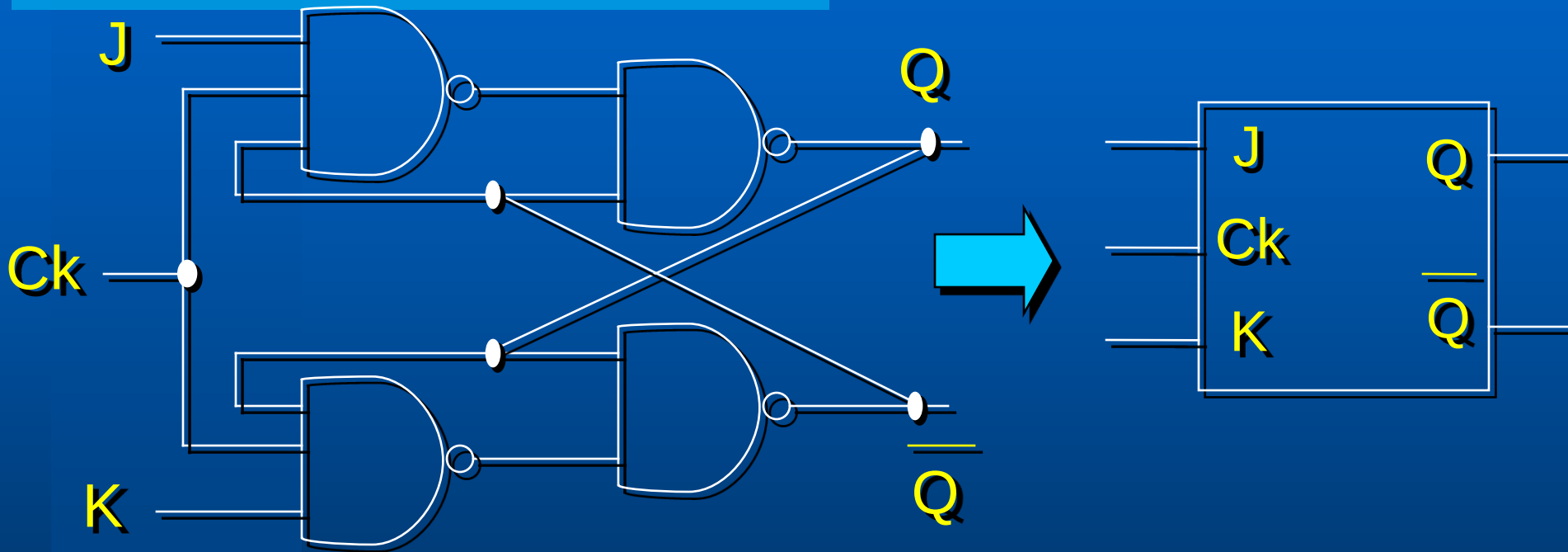


J	K	Q *
0	0	Q
0	1	0
1	0	<u>1</u>
1	1	$\overline{Q}$

* Após o pulso do Ck

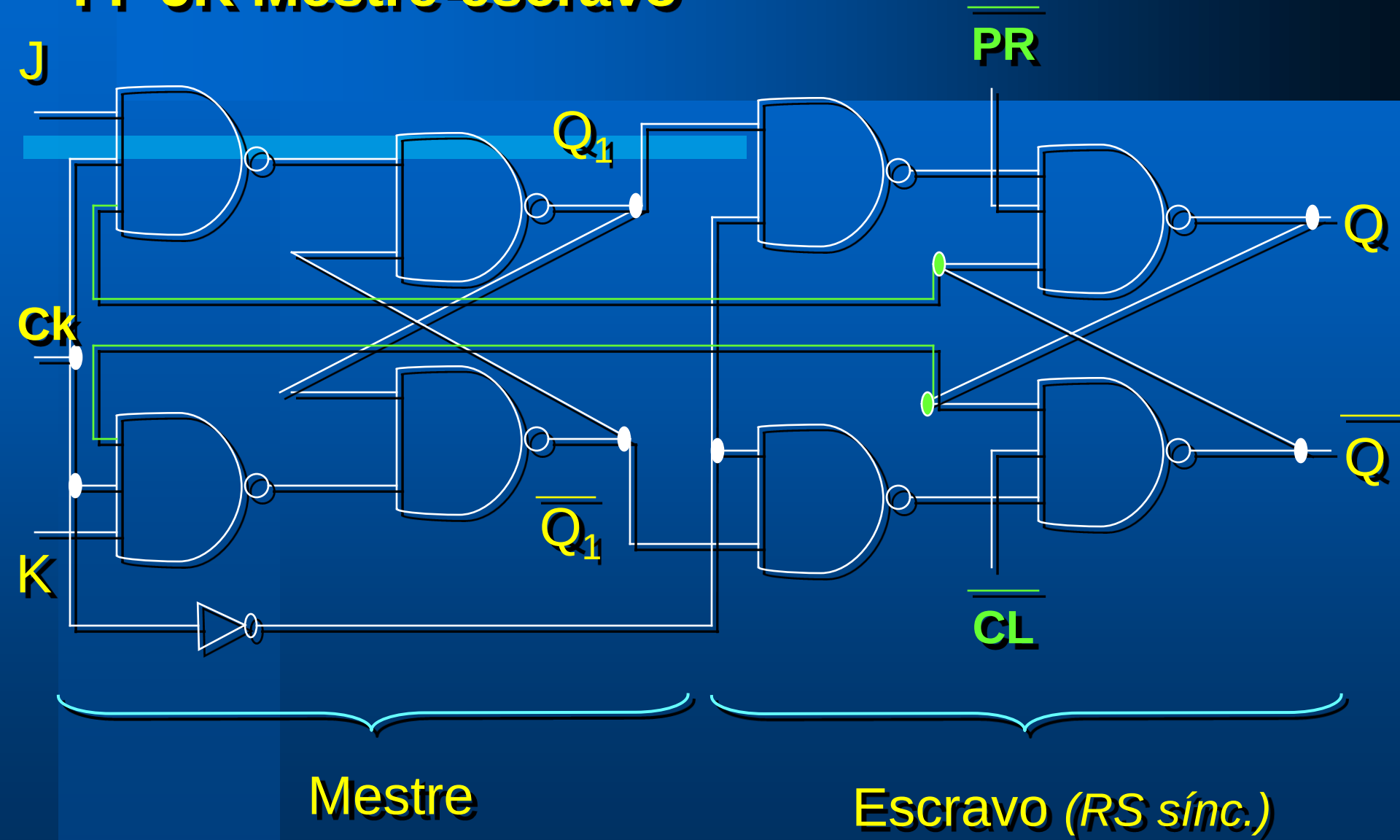
Resolve o problema da indeterminação quando as duas entradas são iguais a 1

Circuito básico real

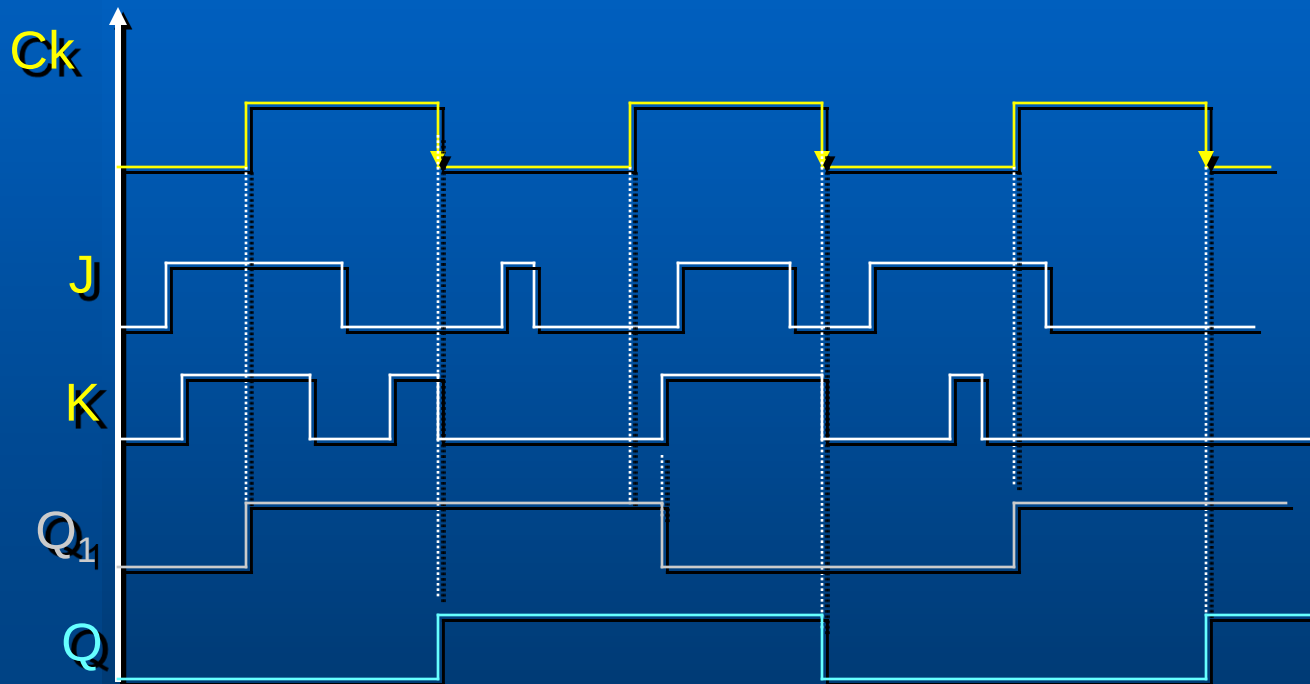


Problema do JK comum: quando o $Ck=1$, há passagem das entradas e realimentações; se, nesse instante, houver mudança de J e/ou K, haverá nova saída → comutação para outro estado mais de uma vez durante o mesmo pulso de Ck

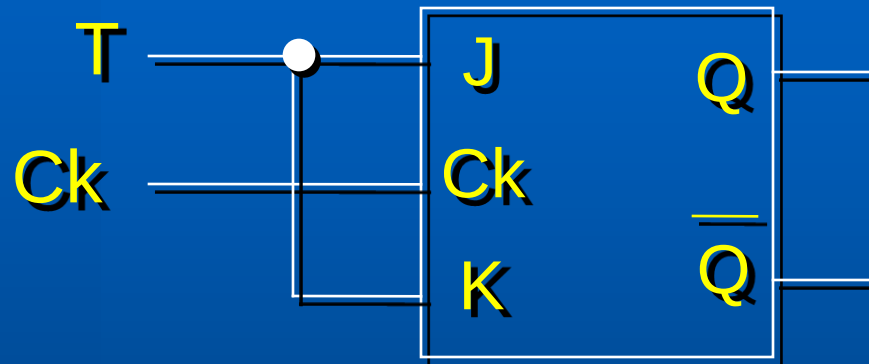
FF JK Mestre-escravo



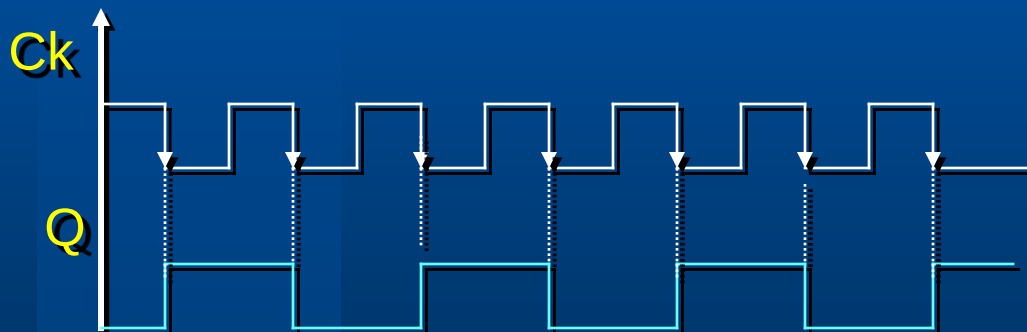
FF JK Mestre-escravo: comportamento



FF Tipo T



T	Q
0	$\overline{Q}$
1	Q

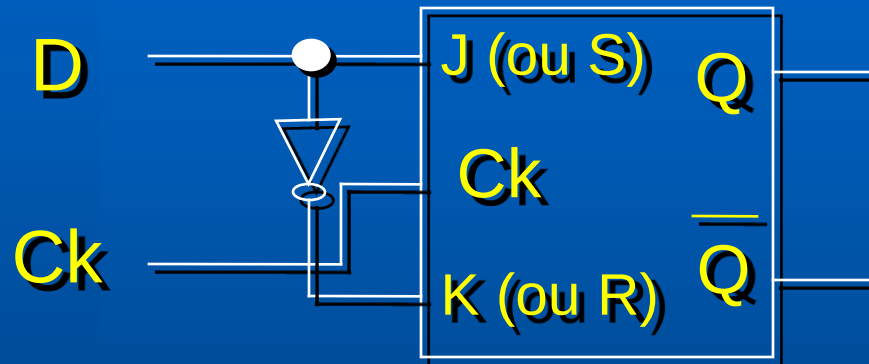


$$T = 1$$

$$f_Q = f_{Ck} / 2$$

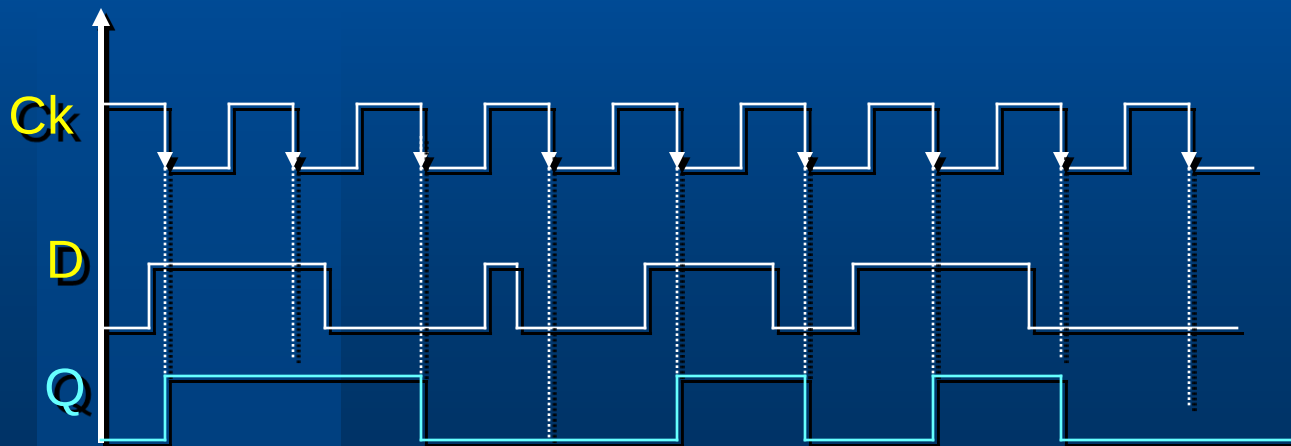
Divisor por 2

FF Tipo D

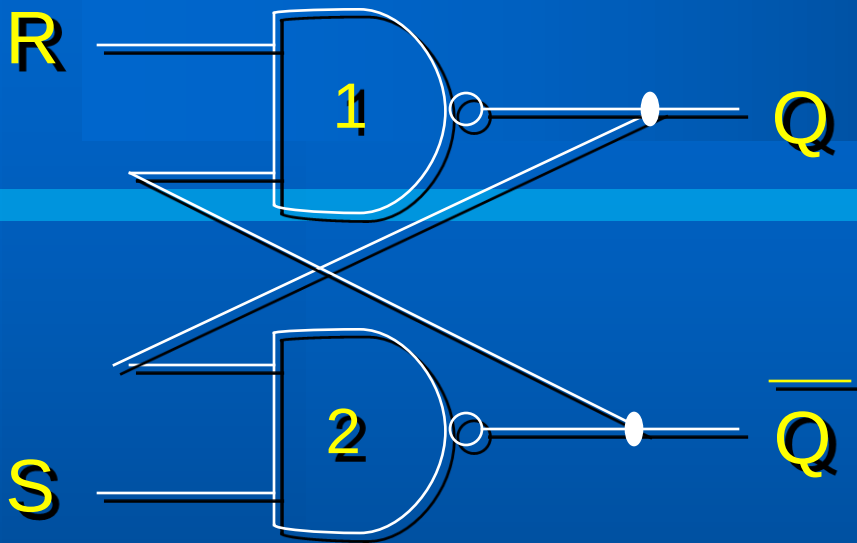


D	Q
0	0
1	1

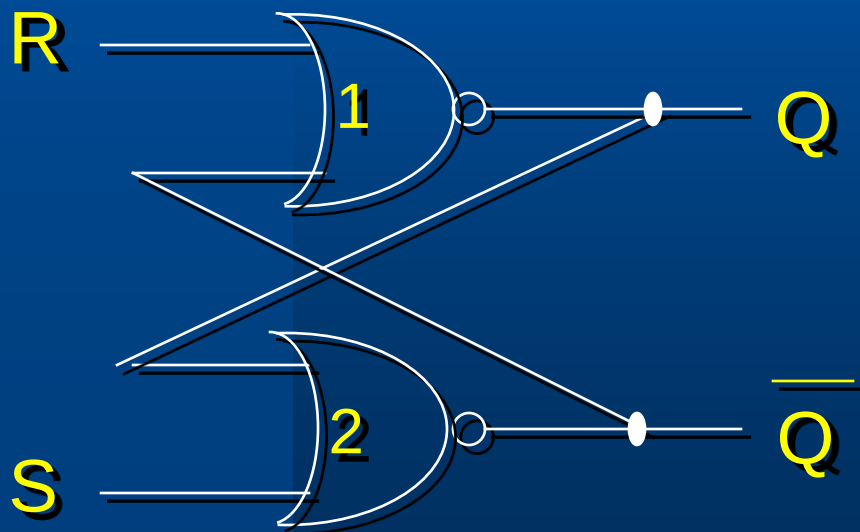
Ck = $\uparrow$, $\downarrow$ ou nível







R	S	Q
0	0	1 **
0	1	1
1	0	0
1	1	Q_a



R	S	Q
0	0	Q_a
0	1	1
1	0	0
1	1	1 **