```
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 */

#ifndef _PIC16F886_H_
#define _PIC16F886_H_

/*
 * C Header file for the Microchip PIC Microcontroller
 * PIC16F886
 */
#ifndef __XC8
#warning Header file pic16f886.h included directly. Use #include <xc.h>
    instead.
#endif

/*
 * Register Definitions
 */
```

```
// Register: INDF
extern volatile unsigned char           INDF                @ 0x000;
#ifndef _LIB_BUILD
asm("INDF equ 00h");
#endif

// Register: TMR0
extern volatile unsigned char           TMR0                @ 0x001;
#ifndef _LIB_BUILD
asm("TMR0 equ 01h");
#endif

// Register: PCL
extern volatile unsigned char           PCL                 @ 0x002;
#ifndef _LIB_BUILD
asm("PCL equ 02h");
#endif

// Register: STATUS
extern volatile unsigned char           STATUS              @ 0x003;
#ifndef _LIB_BUILD
asm("STATUS equ 03h");
#endif
// bitfield definitions
typedef union {
    struct {
        unsigned C                      :1;
        unsigned DC                     :1;
        unsigned Z                      :1;
        unsigned nPD                    :1;
        unsigned nTO                    :1;
        unsigned RP                     :2;
        unsigned IRP                    :1;
    };
    struct {
        unsigned                        :5;
        unsigned RP0                    :1;
        unsigned RP1                    :1;
    };
    struct {
        unsigned CARRY                  :1;
    };
    struct {
        unsigned                        :2;
        unsigned ZERO                   :1;
    };
} STATUSbits_t;
extern volatile STATUSbits_t STATUSbits @ 0x003;
// bitfield macros
#define _STATUS_C_POSN                                  0x0
#define _STATUS_C_POSITION                              0x0
#define _STATUS_C_SIZE                                  0x1
#define _STATUS_C_LENGTH                                0x1
#define _STATUS_C_MASK                                  0x1
#define _STATUS_DC_POSN                                 0x1
#define _STATUS_DC_POSITION                             0x1
#define _STATUS_DC_SIZE                                 0x1
#define _STATUS_DC_LENGTH                               0x1
#define _STATUS_DC_MASK                                 0x2
```

```
#define _STATUS_Z_POSN                  0x2
#define _STATUS_Z_POSITION              0x2
#define _STATUS_Z_SIZE                  0x1
#define _STATUS_Z_LENGTH                0x1
#define _STATUS_Z_MASK                  0x4
#define _STATUS_nPD_POSN                0x3
#define _STATUS_nPD_POSITION            0x3
#define _STATUS_nPD_SIZE                0x1
#define _STATUS_nPD_LENGTH              0x1
#define _STATUS_nPD_MASK                0x8
#define _STATUS_nTO_POSN                0x4
#define _STATUS_nTO_POSITION            0x4
#define _STATUS_nTO_SIZE                0x1
#define _STATUS_nTO_LENGTH              0x1
#define _STATUS_nTO_MASK                0x10
#define _STATUS_RP_POSN                 0x5
#define _STATUS_RP_POSITION             0x5
#define _STATUS_RP_SIZE                 0x2
#define _STATUS_RP_LENGTH               0x2
#define _STATUS_RP_MASK                 0x60
#define _STATUS_IRP_POSN                0x7
#define _STATUS_IRP_POSITION            0x7
#define _STATUS_IRP_SIZE                0x1
#define _STATUS_IRP_LENGTH              0x1
#define _STATUS_IRP_MASK                0x80
#define _STATUS_RP0_POSN                0x5
#define _STATUS_RP0_POSITION            0x5
#define _STATUS_RP0_SIZE                0x1
#define _STATUS_RP0_LENGTH              0x1
#define _STATUS_RP0_MASK                0x20
#define _STATUS_RP1_POSN                0x6
#define _STATUS_RP1_POSITION            0x6
#define _STATUS_RP1_SIZE                0x1
#define _STATUS_RP1_LENGTH              0x1
#define _STATUS_RP1_MASK                0x40
#define _STATUS_CARRY_POSN              0x0
#define _STATUS_CARRY_POSITION          0x0
#define _STATUS_CARRY_SIZE              0x1
#define _STATUS_CARRY_LENGTH            0x1
#define _STATUS_CARRY_MASK              0x1
#define _STATUS_ZERO_POSN               0x2
#define _STATUS_ZERO_POSITION           0x2
#define _STATUS_ZERO_SIZE               0x1
#define _STATUS_ZERO_LENGTH             0x1
#define _STATUS_ZERO_MASK               0x4

// Register: FSR
extern volatile unsigned char           FSR             @ 0x004;
#ifndef _LIB_BUILD
asm("FSR equ 04h");
#endif

// Register: PORTA
extern volatile unsigned char           PORTA           @ 0x005;
#ifndef _LIB_BUILD
asm("PORTA equ 05h");
#endif
// bitfield definitions
typedef union {
    struct {
```

```
        unsigned RA0                    :1;
        unsigned RA1                    :1;
        unsigned RA2                    :1;
        unsigned RA3                    :1;
        unsigned RA4                    :1;
        unsigned RA5                    :1;
        unsigned RA6                    :1;
        unsigned RA7                    :1;
    };
} PORTAbits_t;
extern volatile PORTAbits_t PORTAbits @ 0x005;
// bitfield macros
#define _PORTA_RA0_POSN                                         0x0
#define _PORTA_RA0_POSITION                                     0x0
#define _PORTA_RA0_SIZE                                         0x1
#define _PORTA_RA0_LENGTH                                       0x1
#define _PORTA_RA0_MASK                                         0x1
#define _PORTA_RA1_POSN                                         0x1
#define _PORTA_RA1_POSITION                                     0x1
#define _PORTA_RA1_SIZE                                         0x1
#define _PORTA_RA1_LENGTH                                       0x1
#define _PORTA_RA1_MASK                                         0x2
#define _PORTA_RA2_POSN                                         0x2
#define _PORTA_RA2_POSITION                                     0x2
#define _PORTA_RA2_SIZE                                         0x1
#define _PORTA_RA2_LENGTH                                       0x1
#define _PORTA_RA2_MASK                                         0x4
#define _PORTA_RA3_POSN                                         0x3
#define _PORTA_RA3_POSITION                                     0x3
#define _PORTA_RA3_SIZE                                         0x1
#define _PORTA_RA3_LENGTH                                       0x1
#define _PORTA_RA3_MASK                                         0x8
#define _PORTA_RA4_POSN                                         0x4
#define _PORTA_RA4_POSITION                                     0x4
#define _PORTA_RA4_SIZE                                         0x1
#define _PORTA_RA4_LENGTH                                       0x1
#define _PORTA_RA4_MASK                                         0x10
#define _PORTA_RA5_POSN                                         0x5
#define _PORTA_RA5_POSITION                                     0x5
#define _PORTA_RA5_SIZE                                         0x1
#define _PORTA_RA5_LENGTH                                       0x1
#define _PORTA_RA5_MASK                                         0x20
#define _PORTA_RA6_POSN                                         0x6
#define _PORTA_RA6_POSITION                                     0x6
#define _PORTA_RA6_SIZE                                         0x1
#define _PORTA_RA6_LENGTH                                       0x1
#define _PORTA_RA6_MASK                                         0x40
#define _PORTA_RA7_POSN                                         0x7
#define _PORTA_RA7_POSITION                                     0x7
#define _PORTA_RA7_SIZE                                         0x1
#define _PORTA_RA7_LENGTH                                       0x1
#define _PORTA_RA7_MASK                                         0x80

// Register: PORTB
extern volatile unsigned char           PORTB                   @ 0x006;
#ifndef _LIB_BUILD
asm("PORTB equ 06h");
#endif
// bitfield definitions
typedef union {
```

```
    struct {
        unsigned RB0                    :1;
        unsigned RB1                    :1;
        unsigned RB2                    :1;
        unsigned RB3                    :1;
        unsigned RB4                    :1;
        unsigned RB5                    :1;
        unsigned RB6                    :1;
        unsigned RB7                    :1;
    };
} PORTBbits_t;
extern volatile PORTBbits_t PORTBbits @ 0x006;
// bitfield macros
#define _PORTB_RB0_POSN                                 0x0
#define _PORTB_RB0_POSITION                             0x0
#define _PORTB_RB0_SIZE                                 0x1
#define _PORTB_RB0_LENGTH                               0x1
#define _PORTB_RB0_MASK                                 0x1
#define _PORTB_RB1_POSN                                 0x1
#define _PORTB_RB1_POSITION                             0x1
#define _PORTB_RB1_SIZE                                 0x1
#define _PORTB_RB1_LENGTH                               0x1
#define _PORTB_RB1_MASK                                 0x2
#define _PORTB_RB2_POSN                                 0x2
#define _PORTB_RB2_POSITION                             0x2
#define _PORTB_RB2_SIZE                                 0x1
#define _PORTB_RB2_LENGTH                               0x1
#define _PORTB_RB2_MASK                                 0x4
#define _PORTB_RB3_POSN                                 0x3
#define _PORTB_RB3_POSITION                             0x3
#define _PORTB_RB3_SIZE                                 0x1
#define _PORTB_RB3_LENGTH                               0x1
#define _PORTB_RB3_MASK                                 0x8
#define _PORTB_RB4_POSN                                 0x4
#define _PORTB_RB4_POSITION                             0x4
#define _PORTB_RB4_SIZE                                 0x1
#define _PORTB_RB4_LENGTH                               0x1
#define _PORTB_RB4_MASK                                 0x10
#define _PORTB_RB5_POSN                                 0x5
#define _PORTB_RB5_POSITION                             0x5
#define _PORTB_RB5_SIZE                                 0x1
#define _PORTB_RB5_LENGTH                               0x1
#define _PORTB_RB5_MASK                                 0x20
#define _PORTB_RB6_POSN                                 0x6
#define _PORTB_RB6_POSITION                             0x6
#define _PORTB_RB6_SIZE                                 0x1
#define _PORTB_RB6_LENGTH                               0x1
#define _PORTB_RB6_MASK                                 0x40
#define _PORTB_RB7_POSN                                 0x7
#define _PORTB_RB7_POSITION                             0x7
#define _PORTB_RB7_SIZE                                 0x1
#define _PORTB_RB7_LENGTH                               0x1
#define _PORTB_RB7_MASK                                 0x80

// Register: PORTC
extern volatile unsigned char           PORTC               @ 0x007;
#ifndef _LIB_BUILD
asm("PORTC equ 07h");
#endif
// bitfield definitions
```

```
typedef union {
    struct {
        unsigned RC0                    :1;
        unsigned RC1                    :1;
        unsigned RC2                    :1;
        unsigned RC3                    :1;
        unsigned RC4                    :1;
        unsigned RC5                    :1;
        unsigned RC6                    :1;
        unsigned RC7                    :1;
    };
} PORTCbits_t;
extern volatile PORTCbits_t PORTCbits @ 0x007;
// bitfield macros
#define _PORTC_RC0_POSN                                         0x0
#define _PORTC_RC0_POSITION                                     0x0
#define _PORTC_RC0_SIZE                                         0x1
#define _PORTC_RC0_LENGTH                                       0x1
#define _PORTC_RC0_MASK                                         0x1
#define _PORTC_RC1_POSN                                         0x1
#define _PORTC_RC1_POSITION                                     0x1
#define _PORTC_RC1_SIZE                                         0x1
#define _PORTC_RC1_LENGTH                                       0x1
#define _PORTC_RC1_MASK                                         0x2
#define _PORTC_RC2_POSN                                         0x2
#define _PORTC_RC2_POSITION                                     0x2
#define _PORTC_RC2_SIZE                                         0x1
#define _PORTC_RC2_LENGTH                                       0x1
#define _PORTC_RC2_MASK                                         0x4
#define _PORTC_RC3_POSN                                         0x3
#define _PORTC_RC3_POSITION                                     0x3
#define _PORTC_RC3_SIZE                                         0x1
#define _PORTC_RC3_LENGTH                                       0x1
#define _PORTC_RC3_MASK                                         0x8
#define _PORTC_RC4_POSN                                         0x4
#define _PORTC_RC4_POSITION                                     0x4
#define _PORTC_RC4_SIZE                                         0x1
#define _PORTC_RC4_LENGTH                                       0x1
#define _PORTC_RC4_MASK                                         0x10
#define _PORTC_RC5_POSN                                         0x5
#define _PORTC_RC5_POSITION                                     0x5
#define _PORTC_RC5_SIZE                                         0x1
#define _PORTC_RC5_LENGTH                                       0x1
#define _PORTC_RC5_MASK                                         0x20
#define _PORTC_RC6_POSN                                         0x6
#define _PORTC_RC6_POSITION                                     0x6
#define _PORTC_RC6_SIZE                                         0x1
#define _PORTC_RC6_LENGTH                                       0x1
#define _PORTC_RC6_MASK                                         0x40
#define _PORTC_RC7_POSN                                         0x7
#define _PORTC_RC7_POSITION                                     0x7
#define _PORTC_RC7_SIZE                                         0x1
#define _PORTC_RC7_LENGTH                                       0x1
#define _PORTC_RC7_MASK                                         0x80

// Register: PORTE
extern volatile unsigned char           PORTE               @ 0x009;
#ifndef _LIB_BUILD
asm("PORTE equ 09h");
#endif
```

```
// bitfield definitions
typedef union {
    struct {
        unsigned                        :3;
        unsigned RE3                    :1;
    };
} PORTEbits_t;
extern volatile PORTEbits_t PORTEbits @ 0x009;
// bitfield macros
#define _PORTE_RE3_POSN                                         0x3
#define _PORTE_RE3_POSITION                                     0x3
#define _PORTE_RE3_SIZE                                         0x1
#define _PORTE_RE3_LENGTH                                       0x1
#define _PORTE_RE3_MASK                                         0x8

// Register: PCLATH
extern volatile unsigned char           PCLATH              @ 0x00A;
#ifndef _LIB_BUILD
asm("PCLATH equ 0Ah");
#endif

// Register: INTCON
extern volatile unsigned char           INTCON              @ 0x00B;
#ifndef _LIB_BUILD
asm("INTCON equ 0Bh");
#endif
// bitfield definitions
typedef union {
    struct {
        unsigned RBIF                   :1;
        unsigned INTF                   :1;
        unsigned T0IF                   :1;
        unsigned RBIE                   :1;
        unsigned INTE                   :1;
        unsigned T0IE                   :1;
        unsigned PEIE                   :1;
        unsigned GIE                    :1;
    };
    struct {
        unsigned                        :2;
        unsigned TMR0IF                 :1;
        unsigned                        :2;
        unsigned TMR0IE                 :1;
    };
} INTCONbits_t;
extern volatile INTCONbits_t INTCONbits @ 0x00B;
// bitfield macros
#define _INTCON_RBIF_POSN                                       0x0
#define _INTCON_RBIF_POSITION                                   0x0
#define _INTCON_RBIF_SIZE                                       0x1
#define _INTCON_RBIF_LENGTH                                     0x1
#define _INTCON_RBIF_MASK                                       0x1
#define _INTCON_INTF_POSN                                       0x1
#define _INTCON_INTF_POSITION                                   0x1
#define _INTCON_INTF_SIZE                                       0x1
#define _INTCON_INTF_LENGTH                                     0x1
#define _INTCON_INTF_MASK                                       0x2
#define _INTCON_T0IF_POSN                                       0x2
#define _INTCON_T0IF_POSITION                                   0x2
#define _INTCON_T0IF_SIZE                                       0x1
```

```
#define _INTCON_T0IF_LENGTH                             0x1
#define _INTCON_T0IF_MASK                               0x4
#define _INTCON_RBIE_POSN                               0x3
#define _INTCON_RBIE_POSITION                           0x3
#define _INTCON_RBIE_SIZE                               0x1
#define _INTCON_RBIE_LENGTH                             0x1
#define _INTCON_RBIE_MASK                               0x8
#define _INTCON_INTE_POSN                               0x4
#define _INTCON_INTE_POSITION                           0x4
#define _INTCON_INTE_SIZE                               0x1
#define _INTCON_INTE_LENGTH                             0x1
#define _INTCON_INTE_MASK                               0x10
#define _INTCON_T0IE_POSN                               0x5
#define _INTCON_T0IE_POSITION                           0x5
#define _INTCON_T0IE_SIZE                               0x1
#define _INTCON_T0IE_LENGTH                             0x1
#define _INTCON_T0IE_MASK                               0x20
#define _INTCON_PEIE_POSN                               0x6
#define _INTCON_PEIE_POSITION                           0x6
#define _INTCON_PEIE_SIZE                               0x1
#define _INTCON_PEIE_LENGTH                             0x1
#define _INTCON_PEIE_MASK                               0x40
#define _INTCON_GIE_POSN                                0x7
#define _INTCON_GIE_POSITION                            0x7
#define _INTCON_GIE_SIZE                                0x1
#define _INTCON_GIE_LENGTH                              0x1
#define _INTCON_GIE_MASK                                0x80
#define _INTCON_TMR0IF_POSN                             0x2
#define _INTCON_TMR0IF_POSITION                         0x2
#define _INTCON_TMR0IF_SIZE                             0x1
#define _INTCON_TMR0IF_LENGTH                           0x1
#define _INTCON_TMR0IF_MASK                             0x4
#define _INTCON_TMR0IE_POSN                             0x5
#define _INTCON_TMR0IE_POSITION                         0x5
#define _INTCON_TMR0IE_SIZE                             0x1
#define _INTCON_TMR0IE_LENGTH                           0x1
#define _INTCON_TMR0IE_MASK                             0x20

// Register: PIR1
extern volatile unsigned char           PIR1                @ 0x00C;
#ifndef _LIB_BUILD
asm("PIR1 equ 0Ch");
#endif
// bitfield definitions
typedef union {
    struct {
        unsigned TMR1IF                 :1;
        unsigned TMR2IF                 :1;
        unsigned CCP1IF                 :1;
        unsigned SSPIF                  :1;
        unsigned TXIF                   :1;
        unsigned RCIF                   :1;
        unsigned ADIF                   :1;
    };
} PIR1bits_t;
extern volatile PIR1bits_t PIR1bits @ 0x00C;
// bitfield macros
#define _PIR1_TMR1IF_POSN                               0x0
#define _PIR1_TMR1IF_POSITION                           0x0
#define _PIR1_TMR1IF_SIZE                               0x1
```

```
#define _PIR1_TMR1IF_LENGTH                     0x1
#define _PIR1_TMR1IF_MASK                       0x1
#define _PIR1_TMR2IF_POSN                       0x1
#define _PIR1_TMR2IF_POSITION                   0x1
#define _PIR1_TMR2IF_SIZE                       0x1
#define _PIR1_TMR2IF_LENGTH                     0x1
#define _PIR1_TMR2IF_MASK                       0x2
#define _PIR1_CCP1IF_POSN                       0x2
#define _PIR1_CCP1IF_POSITION                   0x2
#define _PIR1_CCP1IF_SIZE                       0x1
#define _PIR1_CCP1IF_LENGTH                     0x1
#define _PIR1_CCP1IF_MASK                       0x4
#define _PIR1_SSPIF_POSN                        0x3
#define _PIR1_SSPIF_POSITION                    0x3
#define _PIR1_SSPIF_SIZE                        0x1
#define _PIR1_SSPIF_LENGTH                      0x1
#define _PIR1_SSPIF_MASK                        0x8
#define _PIR1_TXIF_POSN                         0x4
#define _PIR1_TXIF_POSITION                     0x4
#define _PIR1_TXIF_SIZE                         0x1
#define _PIR1_TXIF_LENGTH                       0x1
#define _PIR1_TXIF_MASK                         0x10
#define _PIR1_RCIF_POSN                         0x5
#define _PIR1_RCIF_POSITION                     0x5
#define _PIR1_RCIF_SIZE                         0x1
#define _PIR1_RCIF_LENGTH                       0x1
#define _PIR1_RCIF_MASK                         0x20
#define _PIR1_ADIF_POSN                         0x6
#define _PIR1_ADIF_POSITION                     0x6
#define _PIR1_ADIF_SIZE                         0x1
#define _PIR1_ADIF_LENGTH                       0x1
#define _PIR1_ADIF_MASK                         0x40

// Register: PIR2
extern volatile unsigned char           PIR2                @ 0x00D;
#ifndef _LIB_BUILD
asm("PIR2 equ 0Dh");
#endif
// bitfield definitions
typedef union {
    struct {
        unsigned CCP2IF                 :1;
        unsigned                        :1;
        unsigned ULPWUIF                :1;
        unsigned BCLIF                  :1;
        unsigned EEIF                   :1;
        unsigned C1IF                   :1;
        unsigned C2IF                   :1;
        unsigned OSFIF                  :1;
    };
} PIR2bits_t;
extern volatile PIR2bits_t PIR2bits @ 0x00D;
// bitfield macros
#define _PIR2_CCP2IF_POSN                       0x0
#define _PIR2_CCP2IF_POSITION                   0x0
#define _PIR2_CCP2IF_SIZE                       0x1
#define _PIR2_CCP2IF_LENGTH                     0x1
#define _PIR2_CCP2IF_MASK                       0x1
#define _PIR2_ULPWUIF_POSN                      0x2
#define _PIR2_ULPWUIF_POSITION                  0x2
```

```
#define _PIR2_ULPWUIF_SIZE                      0x1
#define _PIR2_ULPWUIF_LENGTH                    0x1
#define _PIR2_ULPWUIF_MASK                      0x4
#define _PIR2_BCLIF_POSN                        0x3
#define _PIR2_BCLIF_POSITION                    0x3
#define _PIR2_BCLIF_SIZE                        0x1
#define _PIR2_BCLIF_LENGTH                      0x1
#define _PIR2_BCLIF_MASK                        0x8
#define _PIR2_EEIF_POSN                         0x4
#define _PIR2_EEIF_POSITION                     0x4
#define _PIR2_EEIF_SIZE                         0x1
#define _PIR2_EEIF_LENGTH                       0x1
#define _PIR2_EEIF_MASK                         0x10
#define _PIR2_C1IF_POSN                         0x5
#define _PIR2_C1IF_POSITION                     0x5
#define _PIR2_C1IF_SIZE                         0x1
#define _PIR2_C1IF_LENGTH                       0x1
#define _PIR2_C1IF_MASK                         0x20
#define _PIR2_C2IF_POSN                         0x6
#define _PIR2_C2IF_POSITION                     0x6
#define _PIR2_C2IF_SIZE                         0x1
#define _PIR2_C2IF_LENGTH                       0x1
#define _PIR2_C2IF_MASK                         0x40
#define _PIR2_OSFIF_POSN                        0x7
#define _PIR2_OSFIF_POSITION                    0x7
#define _PIR2_OSFIF_SIZE                        0x1
#define _PIR2_OSFIF_LENGTH                      0x1
#define _PIR2_OSFIF_MASK                        0x80

// Register: TMR1
extern volatile unsigned short          TMR1            @ 0x00E;
#ifndef _LIB_BUILD
asm("TMR1 equ 0Eh");
#endif

// Register: TMR1L
extern volatile unsigned char           TMR1L           @ 0x00E;
#ifndef _LIB_BUILD
asm("TMR1L equ 0Eh");
#endif

// Register: TMR1H
extern volatile unsigned char           TMR1H           @ 0x00F;
#ifndef _LIB_BUILD
asm("TMR1H equ 0Fh");
#endif

// Register: T1CON
extern volatile unsigned char           T1CON           @ 0x010;
#ifndef _LIB_BUILD
asm("T1CON equ 010h");
#endif
// bitfield definitions
typedef union {
    struct {
        unsigned TMR1ON             :1;
        unsigned TMR1CS             :1;
        unsigned nT1SYNC            :1;
        unsigned T1OSCEN            :1;
        unsigned T1CKPS             :2;
```

```
        unsigned TMR1GE                 :1;
        unsigned T1GINV                 :1;
    };
    struct {
        unsigned                        :2;
        unsigned T1INSYNC               :1;
        unsigned                        :1;
        unsigned T1CKPS0                :1;
        unsigned T1CKPS1                :1;
        unsigned                        :1;
        unsigned T1GIV                  :1;
    };
    struct {
        unsigned                        :2;
        unsigned T1SYNC                 :1;
    };
} T1CONbits_t;
extern volatile T1CONbits_t T1CONbits @ 0x010;
// bitfield macros
#define _T1CON_TMR1ON_POSN                                      0x0
#define _T1CON_TMR1ON_POSITION                                  0x0
#define _T1CON_TMR1ON_SIZE                                      0x1
#define _T1CON_TMR1ON_LENGTH                                    0x1
#define _T1CON_TMR1ON_MASK                                      0x1
#define _T1CON_TMR1CS_POSN                                      0x1
#define _T1CON_TMR1CS_POSITION                                  0x1
#define _T1CON_TMR1CS_SIZE                                      0x1
#define _T1CON_TMR1CS_LENGTH                                    0x1
#define _T1CON_TMR1CS_MASK                                      0x2
#define _T1CON_nT1SYNC_POSN                                     0x2
#define _T1CON_nT1SYNC_POSITION                                 0x2
#define _T1CON_nT1SYNC_SIZE                                     0x1
#define _T1CON_nT1SYNC_LENGTH                                   0x1
#define _T1CON_nT1SYNC_MASK                                     0x4
#define _T1CON_T1OSCEN_POSN                                     0x3
#define _T1CON_T1OSCEN_POSITION                                 0x3
#define _T1CON_T1OSCEN_SIZE                                     0x1
#define _T1CON_T1OSCEN_LENGTH                                   0x1
#define _T1CON_T1OSCEN_MASK                                     0x8
#define _T1CON_T1CKPS_POSN                                      0x4
#define _T1CON_T1CKPS_POSITION                                  0x4
#define _T1CON_T1CKPS_SIZE                                      0x2
#define _T1CON_T1CKPS_LENGTH                                    0x2
#define _T1CON_T1CKPS_MASK                                      0x30
#define _T1CON_TMR1GE_POSN                                      0x6
#define _T1CON_TMR1GE_POSITION                                  0x6
#define _T1CON_TMR1GE_SIZE                                      0x1
#define _T1CON_TMR1GE_LENGTH                                    0x1
#define _T1CON_TMR1GE_MASK                                      0x40
#define _T1CON_T1GINV_POSN                                      0x7
#define _T1CON_T1GINV_POSITION                                  0x7
#define _T1CON_T1GINV_SIZE                                      0x1
#define _T1CON_T1GINV_LENGTH                                    0x1
#define _T1CON_T1GINV_MASK                                      0x80
#define _T1CON_T1INSYNC_POSN                                    0x2
#define _T1CON_T1INSYNC_POSITION                                0x2
#define _T1CON_T1INSYNC_SIZE                                    0x1
#define _T1CON_T1INSYNC_LENGTH                                  0x1
#define _T1CON_T1INSYNC_MASK                                    0x4
#define _T1CON_T1CKPS0_POSN                                     0x4
```

```
#define _T1CON_T1CKPS0_POSITION                         0x4
#define _T1CON_T1CKPS0_SIZE                             0x1
#define _T1CON_T1CKPS0_LENGTH                           0x1
#define _T1CON_T1CKPS0_MASK                             0x10
#define _T1CON_T1CKPS1_POSN                             0x5
#define _T1CON_T1CKPS1_POSITION                         0x5
#define _T1CON_T1CKPS1_SIZE                             0x1
#define _T1CON_T1CKPS1_LENGTH                           0x1
#define _T1CON_T1CKPS1_MASK                             0x20
#define _T1CON_T1GIV_POSN                               0x7
#define _T1CON_T1GIV_POSITION                           0x7
#define _T1CON_T1GIV_SIZE                               0x1
#define _T1CON_T1GIV_LENGTH                             0x1
#define _T1CON_T1GIV_MASK                               0x80
#define _T1CON_T1SYNC_POSN                              0x2
#define _T1CON_T1SYNC_POSITION                          0x2
#define _T1CON_T1SYNC_SIZE                              0x1
#define _T1CON_T1SYNC_LENGTH                            0x1
#define _T1CON_T1SYNC_MASK                              0x4

// Register: TMR2
extern volatile unsigned char           TMR2                @ 0x011;
#ifndef _LIB_BUILD
asm("TMR2 equ 011h");
#endif

// Register: T2CON
extern volatile unsigned char           T2CON               @ 0x012;
#ifndef _LIB_BUILD
asm("T2CON equ 012h");
#endif
// bitfield definitions
typedef union {
    struct {
        unsigned T2CKPS                 :2;
        unsigned TMR2ON                 :1;
        unsigned TOUTPS                 :4;
    };
    struct {
        unsigned T2CKPS0                :1;
        unsigned T2CKPS1                :1;
        unsigned                        :1;
        unsigned TOUTPS0                :1;
        unsigned TOUTPS1                :1;
        unsigned TOUTPS2                :1;
        unsigned TOUTPS3                :1;
    };
} T2CONbits_t;
extern volatile T2CONbits_t T2CONbits @ 0x012;
// bitfield macros
#define _T2CON_T2CKPS_POSN                              0x0
#define _T2CON_T2CKPS_POSITION                          0x0
#define _T2CON_T2CKPS_SIZE                              0x2
#define _T2CON_T2CKPS_LENGTH                            0x2
#define _T2CON_T2CKPS_MASK                              0x3
#define _T2CON_TMR2ON_POSN                              0x2
#define _T2CON_TMR2ON_POSITION                          0x2
#define _T2CON_TMR2ON_SIZE                              0x1
#define _T2CON_TMR2ON_LENGTH                            0x1
#define _T2CON_TMR2ON_MASK                              0x4
```

```
#define _T2CON_TOUTPS_POSN                      0x3
#define _T2CON_TOUTPS_POSITION                  0x3
#define _T2CON_TOUTPS_SIZE                      0x4
#define _T2CON_TOUTPS_LENGTH                    0x4
#define _T2CON_TOUTPS_MASK                      0x78
#define _T2CON_T2CKPS0_POSN                     0x0
#define _T2CON_T2CKPS0_POSITION                 0x0
#define _T2CON_T2CKPS0_SIZE                     0x1
#define _T2CON_T2CKPS0_LENGTH                   0x1
#define _T2CON_T2CKPS0_MASK                     0x1
#define _T2CON_T2CKPS1_POSN                     0x1
#define _T2CON_T2CKPS1_POSITION                 0x1
#define _T2CON_T2CKPS1_SIZE                     0x1
#define _T2CON_T2CKPS1_LENGTH                   0x1
#define _T2CON_T2CKPS1_MASK                     0x2
#define _T2CON_TOUTPS0_POSN                     0x3
#define _T2CON_TOUTPS0_POSITION                 0x3
#define _T2CON_TOUTPS0_SIZE                     0x1
#define _T2CON_TOUTPS0_LENGTH                   0x1
#define _T2CON_TOUTPS0_MASK                     0x8
#define _T2CON_TOUTPS1_POSN                     0x4
#define _T2CON_TOUTPS1_POSITION                 0x4
#define _T2CON_TOUTPS1_SIZE                     0x1
#define _T2CON_TOUTPS1_LENGTH                   0x1
#define _T2CON_TOUTPS1_MASK                     0x10
#define _T2CON_TOUTPS2_POSN                     0x5
#define _T2CON_TOUTPS2_POSITION                 0x5
#define _T2CON_TOUTPS2_SIZE                     0x1
#define _T2CON_TOUTPS2_LENGTH                   0x1
#define _T2CON_TOUTPS2_MASK                     0x20
#define _T2CON_TOUTPS3_POSN                     0x6
#define _T2CON_TOUTPS3_POSITION                 0x6
#define _T2CON_TOUTPS3_SIZE                     0x1
#define _T2CON_TOUTPS3_LENGTH                   0x1
#define _T2CON_TOUTPS3_MASK                     0x40

// Register: SSPBUF
extern volatile unsigned char           SSPBUF              @ 0x013;
#ifndef _LIB_BUILD
asm("SSPBUF equ 013h");
#endif

// Register: SSPCON
extern volatile unsigned char           SSPCON              @ 0x014;
#ifndef _LIB_BUILD
asm("SSPCON equ 014h");
#endif
// bitfield definitions
typedef union {
    struct {
        unsigned SSPM                   :4;
        unsigned CKP                    :1;
        unsigned SSPEN                  :1;
        unsigned SSPOV                  :1;
        unsigned WCOL                   :1;
    };
    struct {
        unsigned SSPM0                  :1;
        unsigned SSPM1                  :1;
        unsigned SSPM2                  :1;
```

```
        unsigned SSPM3                  :1;
    };
} SSPCONbits_t;
extern volatile SSPCONbits_t SSPCONbits @ 0x014;
// bitfield macros
#define _SSPCON_SSPM_POSN                                       0x0
#define _SSPCON_SSPM_POSITION                                   0x0
#define _SSPCON_SSPM_SIZE                                       0x4
#define _SSPCON_SSPM_LENGTH                                     0x4
#define _SSPCON_SSPM_MASK                                       0xF
#define _SSPCON_CKP_POSN                                        0x4
#define _SSPCON_CKP_POSITION                                    0x4
#define _SSPCON_CKP_SIZE                                        0x1
#define _SSPCON_CKP_LENGTH                                      0x1
#define _SSPCON_CKP_MASK                                        0x10
#define _SSPCON_SSPEN_POSN                                      0x5
#define _SSPCON_SSPEN_POSITION                                  0x5
#define _SSPCON_SSPEN_SIZE                                      0x1
#define _SSPCON_SSPEN_LENGTH                                    0x1
#define _SSPCON_SSPEN_MASK                                      0x20
#define _SSPCON_SSPOV_POSN                                      0x6
#define _SSPCON_SSPOV_POSITION                                  0x6
#define _SSPCON_SSPOV_SIZE                                      0x1
#define _SSPCON_SSPOV_LENGTH                                    0x1
#define _SSPCON_SSPOV_MASK                                      0x40
#define _SSPCON_WCOL_POSN                                       0x7
#define _SSPCON_WCOL_POSITION                                   0x7
#define _SSPCON_WCOL_SIZE                                       0x1
#define _SSPCON_WCOL_LENGTH                                     0x1
#define _SSPCON_WCOL_MASK                                       0x80
#define _SSPCON_SSPM0_POSN                                      0x0
#define _SSPCON_SSPM0_POSITION                                  0x0
#define _SSPCON_SSPM0_SIZE                                      0x1
#define _SSPCON_SSPM0_LENGTH                                    0x1
#define _SSPCON_SSPM0_MASK                                      0x1
#define _SSPCON_SSPM1_POSN                                      0x1
#define _SSPCON_SSPM1_POSITION                                  0x1
#define _SSPCON_SSPM1_SIZE                                      0x1
#define _SSPCON_SSPM1_LENGTH                                    0x1
#define _SSPCON_SSPM1_MASK                                      0x2
#define _SSPCON_SSPM2_POSN                                      0x2
#define _SSPCON_SSPM2_POSITION                                  0x2
#define _SSPCON_SSPM2_SIZE                                      0x1
#define _SSPCON_SSPM2_LENGTH                                    0x1
#define _SSPCON_SSPM2_MASK                                      0x4
#define _SSPCON_SSPM3_POSN                                      0x3
#define _SSPCON_SSPM3_POSITION                                  0x3
#define _SSPCON_SSPM3_SIZE                                      0x1
#define _SSPCON_SSPM3_LENGTH                                    0x1
#define _SSPCON_SSPM3_MASK                                      0x8

// Register: CCPR1
extern volatile unsigned short          CCPR1               @ 0x015;
#ifndef _LIB_BUILD
asm("CCPR1 equ 015h");
#endif

// Register: CCPR1L
extern volatile unsigned char           CCPR1L              @ 0x015;
#ifndef _LIB_BUILD
```

```
asm("CCPR1L equ 015h");
#endif

// Register: CCPR1H
extern volatile unsigned char           CCPR1H              @ 0x016;
#ifndef _LIB_BUILD
asm("CCPR1H equ 016h");
#endif

// Register: CCP1CON
extern volatile unsigned char           CCP1CON             @ 0x017;
#ifndef _LIB_BUILD
asm("CCP1CON equ 017h");
#endif
// bitfield definitions
typedef union {
    struct {
        unsigned CCP1M                  :4;
        unsigned DC1B                   :2;
        unsigned P1M                    :2;
    };
    struct {
        unsigned CCP1M0                 :1;
        unsigned CCP1M1                 :1;
        unsigned CCP1M2                 :1;
        unsigned CCP1M3                 :1;
        unsigned DC1B0                  :1;
        unsigned DC1B1                  :1;
        unsigned P1M0                   :1;
        unsigned P1M1                   :1;
    };
    struct {
        unsigned                        :4;
        unsigned CCP1Y                  :1;
        unsigned CCP1X                  :1;
    };
} CCP1CONbits_t;
extern volatile CCP1CONbits_t CCP1CONbits @ 0x017;
// bitfield macros
#define _CCP1CON_CCP1M_POSN                             0x0
#define _CCP1CON_CCP1M_POSITION                         0x0
#define _CCP1CON_CCP1M_SIZE                             0x4
#define _CCP1CON_CCP1M_LENGTH                           0x4
#define _CCP1CON_CCP1M_MASK                             0xF
#define _CCP1CON_DC1B_POSN                              0x4
#define _CCP1CON_DC1B_POSITION                          0x4
#define _CCP1CON_DC1B_SIZE                              0x2
#define _CCP1CON_DC1B_LENGTH                            0x2
#define _CCP1CON_DC1B_MASK                              0x30
#define _CCP1CON_P1M_POSN                               0x6
#define _CCP1CON_P1M_POSITION                           0x6
#define _CCP1CON_P1M_SIZE                               0x2
#define _CCP1CON_P1M_LENGTH                             0x2
#define _CCP1CON_P1M_MASK                               0xC0
#define _CCP1CON_CCP1M0_POSN                            0x0
#define _CCP1CON_CCP1M0_POSITION                        0x0
#define _CCP1CON_CCP1M0_SIZE                            0x1
#define _CCP1CON_CCP1M0_LENGTH                          0x1
#define _CCP1CON_CCP1M0_MASK                            0x1
#define _CCP1CON_CCP1M1_POSN                            0x1
```

```
#define _CCP1CON_CCP1M1_POSITION                0x1
#define _CCP1CON_CCP1M1_SIZE                    0x1
#define _CCP1CON_CCP1M1_LENGTH                  0x1
#define _CCP1CON_CCP1M1_MASK                    0x2
#define _CCP1CON_CCP1M2_POSN                    0x2
#define _CCP1CON_CCP1M2_POSITION                0x2
#define _CCP1CON_CCP1M2_SIZE                    0x1
#define _CCP1CON_CCP1M2_LENGTH                  0x1
#define _CCP1CON_CCP1M2_MASK                    0x4
#define _CCP1CON_CCP1M3_POSN                    0x3
#define _CCP1CON_CCP1M3_POSITION                0x3
#define _CCP1CON_CCP1M3_SIZE                    0x1
#define _CCP1CON_CCP1M3_LENGTH                  0x1
#define _CCP1CON_CCP1M3_MASK                    0x8
#define _CCP1CON_DC1B0_POSN                     0x4
#define _CCP1CON_DC1B0_POSITION                 0x4
#define _CCP1CON_DC1B0_SIZE                     0x1
#define _CCP1CON_DC1B0_LENGTH                   0x1
#define _CCP1CON_DC1B0_MASK                     0x10
#define _CCP1CON_DC1B1_POSN                     0x5
#define _CCP1CON_DC1B1_POSITION                 0x5
#define _CCP1CON_DC1B1_SIZE                     0x1
#define _CCP1CON_DC1B1_LENGTH                   0x1
#define _CCP1CON_DC1B1_MASK                     0x20
#define _CCP1CON_P1M0_POSN                      0x6
#define _CCP1CON_P1M0_POSITION                  0x6
#define _CCP1CON_P1M0_SIZE                      0x1
#define _CCP1CON_P1M0_LENGTH                    0x1
#define _CCP1CON_P1M0_MASK                      0x40
#define _CCP1CON_P1M1_POSN                      0x7
#define _CCP1CON_P1M1_POSITION                  0x7
#define _CCP1CON_P1M1_SIZE                      0x1
#define _CCP1CON_P1M1_LENGTH                    0x1
#define _CCP1CON_P1M1_MASK                      0x80
#define _CCP1CON_CCP1Y_POSN                     0x4
#define _CCP1CON_CCP1Y_POSITION                 0x4
#define _CCP1CON_CCP1Y_SIZE                     0x1
#define _CCP1CON_CCP1Y_LENGTH                   0x1
#define _CCP1CON_CCP1Y_MASK                     0x10
#define _CCP1CON_CCP1X_POSN                     0x5
#define _CCP1CON_CCP1X_POSITION                 0x5
#define _CCP1CON_CCP1X_SIZE                     0x1
#define _CCP1CON_CCP1X_LENGTH                   0x1
#define _CCP1CON_CCP1X_MASK                     0x20

// Register: RCSTA
extern volatile unsigned char           RCSTA               @ 0x018;
#ifndef _LIB_BUILD
asm("RCSTA equ 018h");
#endif
// bitfield definitions
typedef union {
    struct {
        unsigned RX9D                   :1;
        unsigned OERR                   :1;
        unsigned FERR                   :1;
        unsigned ADDEN                  :1;
        unsigned CREN                   :1;
        unsigned SREN                   :1;
        unsigned RX9                    :1;
```

```
        unsigned SPEN                   :1;
    };
    struct {
        unsigned RCD8                   :1;
        unsigned                        :5;
        unsigned RC9                    :1;
    };
    struct {
        unsigned                        :6;
        unsigned nRC8                   :1;
    };
    struct {
        unsigned                        :6;
        unsigned RC8_9                  :1;
    };
} RCSTAbits_t;
extern volatile RCSTAbits_t RCSTAbits @ 0x018;
// bitfield macros
#define _RCSTA_RX9D_POSN                                    0x0
#define _RCSTA_RX9D_POSITION                                0x0
#define _RCSTA_RX9D_SIZE                                    0x1
#define _RCSTA_RX9D_LENGTH                                  0x1
#define _RCSTA_RX9D_MASK                                    0x1
#define _RCSTA_OERR_POSN                                    0x1
#define _RCSTA_OERR_POSITION                                0x1
#define _RCSTA_OERR_SIZE                                    0x1
#define _RCSTA_OERR_LENGTH                                  0x1
#define _RCSTA_OERR_MASK                                    0x2
#define _RCSTA_FERR_POSN                                    0x2
#define _RCSTA_FERR_POSITION                                0x2
#define _RCSTA_FERR_SIZE                                    0x1
#define _RCSTA_FERR_LENGTH                                  0x1
#define _RCSTA_FERR_MASK                                    0x4
#define _RCSTA_ADDEN_POSN                                   0x3
#define _RCSTA_ADDEN_POSITION                               0x3
#define _RCSTA_ADDEN_SIZE                                   0x1
#define _RCSTA_ADDEN_LENGTH                                 0x1
#define _RCSTA_ADDEN_MASK                                   0x8
#define _RCSTA_CREN_POSN                                    0x4
#define _RCSTA_CREN_POSITION                                0x4
#define _RCSTA_CREN_SIZE                                    0x1
#define _RCSTA_CREN_LENGTH                                  0x1
#define _RCSTA_CREN_MASK                                    0x10
#define _RCSTA_SREN_POSN                                    0x5
#define _RCSTA_SREN_POSITION                                0x5
#define _RCSTA_SREN_SIZE                                    0x1
#define _RCSTA_SREN_LENGTH                                  0x1
#define _RCSTA_SREN_MASK                                    0x20
#define _RCSTA_RX9_POSN                                     0x6
#define _RCSTA_RX9_POSITION                                 0x6
#define _RCSTA_RX9_SIZE                                     0x1
#define _RCSTA_RX9_LENGTH                                   0x1
#define _RCSTA_RX9_MASK                                     0x40
#define _RCSTA_SPEN_POSN                                    0x7
#define _RCSTA_SPEN_POSITION                                0x7
#define _RCSTA_SPEN_SIZE                                    0x1
#define _RCSTA_SPEN_LENGTH                                  0x1
#define _RCSTA_SPEN_MASK                                    0x80
#define _RCSTA_RCD8_POSN                                    0x0
#define _RCSTA_RCD8_POSITION                                0x0
```

```
#define _RCSTA_RCD8_SIZE                        0x1
#define _RCSTA_RCD8_LENGTH                      0x1
#define _RCSTA_RCD8_MASK                        0x1
#define _RCSTA_RC9_POSN                         0x6
#define _RCSTA_RC9_POSITION                     0x6
#define _RCSTA_RC9_SIZE                         0x1
#define _RCSTA_RC9_LENGTH                       0x1
#define _RCSTA_RC9_MASK                         0x40
#define _RCSTA_nRC8_POSN                        0x6
#define _RCSTA_nRC8_POSITION                    0x6
#define _RCSTA_nRC8_SIZE                        0x1
#define _RCSTA_nRC8_LENGTH                      0x1
#define _RCSTA_nRC8_MASK                        0x40
#define _RCSTA_RC8_9_POSN                       0x6
#define _RCSTA_RC8_9_POSITION                   0x6
#define _RCSTA_RC8_9_SIZE                       0x1
#define _RCSTA_RC8_9_LENGTH                     0x1
#define _RCSTA_RC8_9_MASK                       0x40

// Register: TXREG
extern volatile unsigned char           TXREG           @ 0x019;
#ifndef _LIB_BUILD
asm("TXREG equ 019h");
#endif

// Register: RCREG
extern volatile unsigned char           RCREG           @ 0x01A;
#ifndef _LIB_BUILD
asm("RCREG equ 01Ah");
#endif

// Register: CCPR2
extern volatile unsigned short          CCPR2           @ 0x01B;
#ifndef _LIB_BUILD
asm("CCPR2 equ 01Bh");
#endif

// Register: CCPR2L
extern volatile unsigned char           CCPR2L          @ 0x01B;
#ifndef _LIB_BUILD
asm("CCPR2L equ 01Bh");
#endif

// Register: CCPR2H
extern volatile unsigned char           CCPR2H          @ 0x01C;
#ifndef _LIB_BUILD
asm("CCPR2H equ 01Ch");
#endif

// Register: CCP2CON
extern volatile unsigned char           CCP2CON         @ 0x01D;
#ifndef _LIB_BUILD
asm("CCP2CON equ 01Dh");
#endif
// bitfield definitions
typedef union {
    struct {
        unsigned CCP2M                  :4;
        unsigned DC2B0                  :1;
        unsigned DC2B1                  :1;
```

```
    };
    struct {
        unsigned CCP2M0                 :1;
        unsigned CCP2M1                 :1;
        unsigned CCP2M2                 :1;
        unsigned CCP2M3                 :1;
        unsigned CCP2Y                  :1;
        unsigned CCP2X                  :1;
    };
} CCP2CONbits_t;
extern volatile CCP2CONbits_t CCP2CONbits @ 0x01D;
// bitfield macros
#define _CCP2CON_CCP2M_POSN                                     0x0
#define _CCP2CON_CCP2M_POSITION                                 0x0
#define _CCP2CON_CCP2M_SIZE                                     0x4
#define _CCP2CON_CCP2M_LENGTH                                   0x4
#define _CCP2CON_CCP2M_MASK                                     0xF
#define _CCP2CON_DC2B0_POSN                                     0x4
#define _CCP2CON_DC2B0_POSITION                                 0x4
#define _CCP2CON_DC2B0_SIZE                                     0x1
#define _CCP2CON_DC2B0_LENGTH                                   0x1
#define _CCP2CON_DC2B0_MASK                                     0x10
#define _CCP2CON_DC2B1_POSN                                     0x5
#define _CCP2CON_DC2B1_POSITION                                 0x5
#define _CCP2CON_DC2B1_SIZE                                     0x1
#define _CCP2CON_DC2B1_LENGTH                                   0x1
#define _CCP2CON_DC2B1_MASK                                     0x20
#define _CCP2CON_CCP2M0_POSN                                    0x0
#define _CCP2CON_CCP2M0_POSITION                                0x0
#define _CCP2CON_CCP2M0_SIZE                                    0x1
#define _CCP2CON_CCP2M0_LENGTH                                  0x1
#define _CCP2CON_CCP2M0_MASK                                    0x1
#define _CCP2CON_CCP2M1_POSN                                    0x1
#define _CCP2CON_CCP2M1_POSITION                                0x1
#define _CCP2CON_CCP2M1_SIZE                                    0x1
#define _CCP2CON_CCP2M1_LENGTH                                  0x1
#define _CCP2CON_CCP2M1_MASK                                    0x2
#define _CCP2CON_CCP2M2_POSN                                    0x2
#define _CCP2CON_CCP2M2_POSITION                                0x2
#define _CCP2CON_CCP2M2_SIZE                                    0x1
#define _CCP2CON_CCP2M2_LENGTH                                  0x1
#define _CCP2CON_CCP2M2_MASK                                    0x4
#define _CCP2CON_CCP2M3_POSN                                    0x3
#define _CCP2CON_CCP2M3_POSITION                                0x3
#define _CCP2CON_CCP2M3_SIZE                                    0x1
#define _CCP2CON_CCP2M3_LENGTH                                  0x1
#define _CCP2CON_CCP2M3_MASK                                    0x8
#define _CCP2CON_CCP2Y_POSN                                     0x4
#define _CCP2CON_CCP2Y_POSITION                                 0x4
#define _CCP2CON_CCP2Y_SIZE                                     0x1
#define _CCP2CON_CCP2Y_LENGTH                                   0x1
#define _CCP2CON_CCP2Y_MASK                                     0x10
#define _CCP2CON_CCP2X_POSN                                     0x5
#define _CCP2CON_CCP2X_POSITION                                 0x5
#define _CCP2CON_CCP2X_SIZE                                     0x1
#define _CCP2CON_CCP2X_LENGTH                                   0x1
#define _CCP2CON_CCP2X_MASK                                     0x20

// Register: ADRESH
extern volatile unsigned char           ADRESH              @ 0x01E;
```

```
#ifndef _LIB_BUILD
asm("ADRESH equ 01Eh");
#endif

// Register: ADCON0
extern volatile unsigned char           ADCON0              @ 0x01F;
#ifndef _LIB_BUILD
asm("ADCON0 equ 01Fh");
#endif
// bitfield definitions
typedef union {
    struct {
        unsigned ADON                   :1;
        unsigned GO_nDONE               :1;
        unsigned CHS                    :4;
        unsigned ADCS                   :2;
    };
    struct {
        unsigned                        :1;
        unsigned GO                     :1;
        unsigned CHS0                   :1;
        unsigned CHS1                   :1;
        unsigned CHS2                   :1;
        unsigned CHS3                   :1;
        unsigned ADCS0                  :1;
        unsigned ADCS1                  :1;
    };
    struct {
        unsigned                        :1;
        unsigned nDONE                  :1;
    };
    struct {
        unsigned                        :1;
        unsigned GO_DONE                :1;
    };
} ADCON0bits_t;
extern volatile ADCON0bits_t ADCON0bits @ 0x01F;
// bitfield macros
#define _ADCON0_ADON_POSN                                   0x0
#define _ADCON0_ADON_POSITION                               0x0
#define _ADCON0_ADON_SIZE                                   0x1
#define _ADCON0_ADON_LENGTH                                 0x1
#define _ADCON0_ADON_MASK                                   0x1
#define _ADCON0_GO_nDONE_POSN                               0x1
#define _ADCON0_GO_nDONE_POSITION                           0x1
#define _ADCON0_GO_nDONE_SIZE                               0x1
#define _ADCON0_GO_nDONE_LENGTH                             0x1
#define _ADCON0_GO_nDONE_MASK                               0x2
#define _ADCON0_CHS_POSN                                    0x2
#define _ADCON0_CHS_POSITION                                0x2
#define _ADCON0_CHS_SIZE                                    0x4
#define _ADCON0_CHS_LENGTH                                  0x4
#define _ADCON0_CHS_MASK                                    0x3C
#define _ADCON0_ADCS_POSN                                   0x6
#define _ADCON0_ADCS_POSITION                               0x6
#define _ADCON0_ADCS_SIZE                                   0x2
#define _ADCON0_ADCS_LENGTH                                 0x2
#define _ADCON0_ADCS_MASK                                   0xC0
#define _ADCON0_GO_POSN                                     0x1
#define _ADCON0_GO_POSITION                                 0x1
```

```
#define _ADCON0_GO_SIZE                                 0x1
#define _ADCON0_GO_LENGTH                               0x1
#define _ADCON0_GO_MASK                                 0x2
#define _ADCON0_CHS0_POSN                               0x2
#define _ADCON0_CHS0_POSITION                           0x2
#define _ADCON0_CHS0_SIZE                               0x1
#define _ADCON0_CHS0_LENGTH                             0x1
#define _ADCON0_CHS0_MASK                               0x4
#define _ADCON0_CHS1_POSN                               0x3
#define _ADCON0_CHS1_POSITION                           0x3
#define _ADCON0_CHS1_SIZE                               0x1
#define _ADCON0_CHS1_LENGTH                             0x1
#define _ADCON0_CHS1_MASK                               0x8
#define _ADCON0_CHS2_POSN                               0x4
#define _ADCON0_CHS2_POSITION                           0x4
#define _ADCON0_CHS2_SIZE                               0x1
#define _ADCON0_CHS2_LENGTH                             0x1
#define _ADCON0_CHS2_MASK                               0x10
#define _ADCON0_CHS3_POSN                               0x5
#define _ADCON0_CHS3_POSITION                           0x5
#define _ADCON0_CHS3_SIZE                               0x1
#define _ADCON0_CHS3_LENGTH                             0x1
#define _ADCON0_CHS3_MASK                               0x20
#define _ADCON0_ADCS0_POSN                              0x6
#define _ADCON0_ADCS0_POSITION                          0x6
#define _ADCON0_ADCS0_SIZE                              0x1
#define _ADCON0_ADCS0_LENGTH                            0x1
#define _ADCON0_ADCS0_MASK                              0x40
#define _ADCON0_ADCS1_POSN                              0x7
#define _ADCON0_ADCS1_POSITION                          0x7
#define _ADCON0_ADCS1_SIZE                              0x1
#define _ADCON0_ADCS1_LENGTH                            0x1
#define _ADCON0_ADCS1_MASK                              0x80
#define _ADCON0_nDONE_POSN                              0x1
#define _ADCON0_nDONE_POSITION                          0x1
#define _ADCON0_nDONE_SIZE                              0x1
#define _ADCON0_nDONE_LENGTH                            0x1
#define _ADCON0_nDONE_MASK                              0x2
#define _ADCON0_GO_DONE_POSN                            0x1
#define _ADCON0_GO_DONE_POSITION                        0x1
#define _ADCON0_GO_DONE_SIZE                            0x1
#define _ADCON0_GO_DONE_LENGTH                          0x1
#define _ADCON0_GO_DONE_MASK                            0x2

// Register: OPTION_REG
extern volatile unsigned char           OPTION_REG          @ 0x081;
#ifndef _LIB_BUILD
asm("OPTION_REG equ 081h");
#endif
// bitfield definitions
typedef union {
    struct {
        unsigned PS                     :3;
        unsigned PSA                    :1;
        unsigned T0SE                   :1;
        unsigned T0CS                   :1;
        unsigned INTEDG                 :1;
        unsigned nRBPU                  :1;
    };
    struct {
```

```
        unsigned PS0                    :1;
        unsigned PS1                    :1;
        unsigned PS2                    :1;
    };
} OPTION_REGbits_t;
extern volatile OPTION_REGbits_t OPTION_REGbits @ 0x081;
// bitfield macros
#define _OPTION_REG_PS_POSN                                     0x0
#define _OPTION_REG_PS_POSITION                                 0x0
#define _OPTION_REG_PS_SIZE                                     0x3
#define _OPTION_REG_PS_LENGTH                                   0x3
#define _OPTION_REG_PS_MASK                                     0x7
#define _OPTION_REG_PSA_POSN                                    0x3
#define _OPTION_REG_PSA_POSITION                                0x3
#define _OPTION_REG_PSA_SIZE                                    0x1
#define _OPTION_REG_PSA_LENGTH                                  0x1
#define _OPTION_REG_PSA_MASK                                    0x8
#define _OPTION_REG_T0SE_POSN                                   0x4
#define _OPTION_REG_T0SE_POSITION                               0x4
#define _OPTION_REG_T0SE_SIZE                                   0x1
#define _OPTION_REG_T0SE_LENGTH                                 0x1
#define _OPTION_REG_T0SE_MASK                                   0x10
#define _OPTION_REG_T0CS_POSN                                   0x5
#define _OPTION_REG_T0CS_POSITION                               0x5
#define _OPTION_REG_T0CS_SIZE                                   0x1
#define _OPTION_REG_T0CS_LENGTH                                 0x1
#define _OPTION_REG_T0CS_MASK                                   0x20
#define _OPTION_REG_INTEDG_POSN                                 0x6
#define _OPTION_REG_INTEDG_POSITION                             0x6
#define _OPTION_REG_INTEDG_SIZE                                 0x1
#define _OPTION_REG_INTEDG_LENGTH                               0x1
#define _OPTION_REG_INTEDG_MASK                                 0x40
#define _OPTION_REG_nRBPU_POSN                                  0x7
#define _OPTION_REG_nRBPU_POSITION                              0x7
#define _OPTION_REG_nRBPU_SIZE                                  0x1
#define _OPTION_REG_nRBPU_LENGTH                                0x1
#define _OPTION_REG_nRBPU_MASK                                  0x80
#define _OPTION_REG_PS0_POSN                                    0x0
#define _OPTION_REG_PS0_POSITION                                0x0
#define _OPTION_REG_PS0_SIZE                                    0x1
#define _OPTION_REG_PS0_LENGTH                                  0x1
#define _OPTION_REG_PS0_MASK                                    0x1
#define _OPTION_REG_PS1_POSN                                    0x1
#define _OPTION_REG_PS1_POSITION                                0x1
#define _OPTION_REG_PS1_SIZE                                    0x1
#define _OPTION_REG_PS1_LENGTH                                  0x1
#define _OPTION_REG_PS1_MASK                                    0x2
#define _OPTION_REG_PS2_POSN                                    0x2
#define _OPTION_REG_PS2_POSITION                                0x2
#define _OPTION_REG_PS2_SIZE                                    0x1
#define _OPTION_REG_PS2_LENGTH                                  0x1
#define _OPTION_REG_PS2_MASK                                    0x4

// Register: TRISA
extern volatile unsigned char           TRISA               @ 0x085;
#ifndef _LIB_BUILD
asm("TRISA equ 085h");
#endif
// bitfield definitions
typedef union {
```

```
    struct {
        unsigned TRISA0                 :1;
        unsigned TRISA1                 :1;
        unsigned TRISA2                 :1;
        unsigned TRISA3                 :1;
        unsigned TRISA4                 :1;
        unsigned TRISA5                 :1;
        unsigned TRISA6                 :1;
        unsigned TRISA7                 :1;
    };
} TRISAbits_t;
extern volatile TRISAbits_t TRISAbits @ 0x085;
// bitfield macros
#define _TRISA_TRISA0_POSN                                      0x0
#define _TRISA_TRISA0_POSITION                                  0x0
#define _TRISA_TRISA0_SIZE                                      0x1
#define _TRISA_TRISA0_LENGTH                                    0x1
#define _TRISA_TRISA0_MASK                                      0x1
#define _TRISA_TRISA1_POSN                                      0x1
#define _TRISA_TRISA1_POSITION                                  0x1
#define _TRISA_TRISA1_SIZE                                      0x1
#define _TRISA_TRISA1_LENGTH                                    0x1
#define _TRISA_TRISA1_MASK                                      0x2
#define _TRISA_TRISA2_POSN                                      0x2
#define _TRISA_TRISA2_POSITION                                  0x2
#define _TRISA_TRISA2_SIZE                                      0x1
#define _TRISA_TRISA2_LENGTH                                    0x1
#define _TRISA_TRISA2_MASK                                      0x4
#define _TRISA_TRISA3_POSN                                      0x3
#define _TRISA_TRISA3_POSITION                                  0x3
#define _TRISA_TRISA3_SIZE                                      0x1
#define _TRISA_TRISA3_LENGTH                                    0x1
#define _TRISA_TRISA3_MASK                                      0x8
#define _TRISA_TRISA4_POSN                                      0x4
#define _TRISA_TRISA4_POSITION                                  0x4
#define _TRISA_TRISA4_SIZE                                      0x1
#define _TRISA_TRISA4_LENGTH                                    0x1
#define _TRISA_TRISA4_MASK                                      0x10
#define _TRISA_TRISA5_POSN                                      0x5
#define _TRISA_TRISA5_POSITION                                  0x5
#define _TRISA_TRISA5_SIZE                                      0x1
#define _TRISA_TRISA5_LENGTH                                    0x1
#define _TRISA_TRISA5_MASK                                      0x20
#define _TRISA_TRISA6_POSN                                      0x6
#define _TRISA_TRISA6_POSITION                                  0x6
#define _TRISA_TRISA6_SIZE                                      0x1
#define _TRISA_TRISA6_LENGTH                                    0x1
#define _TRISA_TRISA6_MASK                                      0x40
#define _TRISA_TRISA7_POSN                                      0x7
#define _TRISA_TRISA7_POSITION                                  0x7
#define _TRISA_TRISA7_SIZE                                      0x1
#define _TRISA_TRISA7_LENGTH                                    0x1
#define _TRISA_TRISA7_MASK                                      0x80

// Register: TRISB
extern volatile unsigned char           TRISB                   @ 0x086;
#ifndef _LIB_BUILD
asm("TRISB equ 086h");
#endif
// bitfield definitions
```

```
typedef union {
    struct {
        unsigned TRISB0                 :1;
        unsigned TRISB1                 :1;
        unsigned TRISB2                 :1;
        unsigned TRISB3                 :1;
        unsigned TRISB4                 :1;
        unsigned TRISB5                 :1;
        unsigned TRISB6                 :1;
        unsigned TRISB7                 :1;
    };
} TRISBbits_t;
extern volatile TRISBbits_t TRISBbits @ 0x086;
// bitfield macros
#define _TRISB_TRISB0_POSN                                      0x0
#define _TRISB_TRISB0_POSITION                                  0x0
#define _TRISB_TRISB0_SIZE                                      0x1
#define _TRISB_TRISB0_LENGTH                                    0x1
#define _TRISB_TRISB0_MASK                                      0x1
#define _TRISB_TRISB1_POSN                                      0x1
#define _TRISB_TRISB1_POSITION                                  0x1
#define _TRISB_TRISB1_SIZE                                      0x1
#define _TRISB_TRISB1_LENGTH                                    0x1
#define _TRISB_TRISB1_MASK                                      0x2
#define _TRISB_TRISB2_POSN                                      0x2
#define _TRISB_TRISB2_POSITION                                  0x2
#define _TRISB_TRISB2_SIZE                                      0x1
#define _TRISB_TRISB2_LENGTH                                    0x1
#define _TRISB_TRISB2_MASK                                      0x4
#define _TRISB_TRISB3_POSN                                      0x3
#define _TRISB_TRISB3_POSITION                                  0x3
#define _TRISB_TRISB3_SIZE                                      0x1
#define _TRISB_TRISB3_LENGTH                                    0x1
#define _TRISB_TRISB3_MASK                                      0x8
#define _TRISB_TRISB4_POSN                                      0x4
#define _TRISB_TRISB4_POSITION                                  0x4
#define _TRISB_TRISB4_SIZE                                      0x1
#define _TRISB_TRISB4_LENGTH                                    0x1
#define _TRISB_TRISB4_MASK                                      0x10
#define _TRISB_TRISB5_POSN                                      0x5
#define _TRISB_TRISB5_POSITION                                  0x5
#define _TRISB_TRISB5_SIZE                                      0x1
#define _TRISB_TRISB5_LENGTH                                    0x1
#define _TRISB_TRISB5_MASK                                      0x20
#define _TRISB_TRISB6_POSN                                      0x6
#define _TRISB_TRISB6_POSITION                                  0x6
#define _TRISB_TRISB6_SIZE                                      0x1
#define _TRISB_TRISB6_LENGTH                                    0x1
#define _TRISB_TRISB6_MASK                                      0x40
#define _TRISB_TRISB7_POSN                                      0x7
#define _TRISB_TRISB7_POSITION                                  0x7
#define _TRISB_TRISB7_SIZE                                      0x1
#define _TRISB_TRISB7_LENGTH                                    0x1
#define _TRISB_TRISB7_MASK                                      0x80

// Register: TRISC
extern volatile unsigned char           TRISC               @ 0x087;
#ifndef _LIB_BUILD
asm("TRISC equ 087h");
#endif
```

```
// bitfield definitions
typedef union {
    struct {
        unsigned TRISC0                 :1;
        unsigned TRISC1                 :1;
        unsigned TRISC2                 :1;
        unsigned TRISC3                 :1;
        unsigned TRISC4                 :1;
        unsigned TRISC5                 :1;
        unsigned TRISC6                 :1;
        unsigned TRISC7                 :1;
    };
} TRISCbits_t;
extern volatile TRISCbits_t TRISCbits @ 0x087;
// bitfield macros
#define _TRISC_TRISC0_POSN                                      0x0
#define _TRISC_TRISC0_POSITION                                  0x0
#define _TRISC_TRISC0_SIZE                                      0x1
#define _TRISC_TRISC0_LENGTH                                    0x1
#define _TRISC_TRISC0_MASK                                      0x1
#define _TRISC_TRISC1_POSN                                      0x1
#define _TRISC_TRISC1_POSITION                                  0x1
#define _TRISC_TRISC1_SIZE                                      0x1
#define _TRISC_TRISC1_LENGTH                                    0x1
#define _TRISC_TRISC1_MASK                                      0x2
#define _TRISC_TRISC2_POSN                                      0x2
#define _TRISC_TRISC2_POSITION                                  0x2
#define _TRISC_TRISC2_SIZE                                      0x1
#define _TRISC_TRISC2_LENGTH                                    0x1
#define _TRISC_TRISC2_MASK                                      0x4
#define _TRISC_TRISC3_POSN                                      0x3
#define _TRISC_TRISC3_POSITION                                  0x3
#define _TRISC_TRISC3_SIZE                                      0x1
#define _TRISC_TRISC3_LENGTH                                    0x1
#define _TRISC_TRISC3_MASK                                      0x8
#define _TRISC_TRISC4_POSN                                      0x4
#define _TRISC_TRISC4_POSITION                                  0x4
#define _TRISC_TRISC4_SIZE                                      0x1
#define _TRISC_TRISC4_LENGTH                                    0x1
#define _TRISC_TRISC4_MASK                                      0x10
#define _TRISC_TRISC5_POSN                                      0x5
#define _TRISC_TRISC5_POSITION                                  0x5
#define _TRISC_TRISC5_SIZE                                      0x1
#define _TRISC_TRISC5_LENGTH                                    0x1
#define _TRISC_TRISC5_MASK                                      0x20
#define _TRISC_TRISC6_POSN                                      0x6
#define _TRISC_TRISC6_POSITION                                  0x6
#define _TRISC_TRISC6_SIZE                                      0x1
#define _TRISC_TRISC6_LENGTH                                    0x1
#define _TRISC_TRISC6_MASK                                      0x40
#define _TRISC_TRISC7_POSN                                      0x7
#define _TRISC_TRISC7_POSITION                                  0x7
#define _TRISC_TRISC7_SIZE                                      0x1
#define _TRISC_TRISC7_LENGTH                                    0x1
#define _TRISC_TRISC7_MASK                                      0x80

// Register: TRISE
extern volatile unsigned char           TRISE               @ 0x089;
#ifndef _LIB_BUILD
asm("TRISE equ 089h");
```

```
#endif
// bitfield definitions
typedef union {
    struct {
        unsigned                        :3;
        unsigned TRISE3                 :1;
    };
} TRISEbits_t;
extern volatile TRISEbits_t TRISEbits @ 0x089;
// bitfield macros
#define _TRISE_TRISE3_POSN                                      0x3
#define _TRISE_TRISE3_POSITION                                  0x3
#define _TRISE_TRISE3_SIZE                                      0x1
#define _TRISE_TRISE3_LENGTH                                    0x1
#define _TRISE_TRISE3_MASK                                      0x8

// Register: PIE1
extern volatile unsigned char           PIE1                    @ 0x08C;
#ifndef _LIB_BUILD
asm("PIE1 equ 08Ch");
#endif
// bitfield definitions
typedef union {
    struct {
        unsigned TMR1IE                 :1;
        unsigned TMR2IE                 :1;
        unsigned CCP1IE                 :1;
        unsigned SSPIE                  :1;
        unsigned TXIE                   :1;
        unsigned RCIE                   :1;
        unsigned ADIE                   :1;
    };
} PIE1bits_t;
extern volatile PIE1bits_t PIE1bits @ 0x08C;
// bitfield macros
#define _PIE1_TMR1IE_POSN                                       0x0
#define _PIE1_TMR1IE_POSITION                                   0x0
#define _PIE1_TMR1IE_SIZE                                       0x1
#define _PIE1_TMR1IE_LENGTH                                     0x1
#define _PIE1_TMR1IE_MASK                                       0x1
#define _PIE1_TMR2IE_POSN                                       0x1
#define _PIE1_TMR2IE_POSITION                                   0x1
#define _PIE1_TMR2IE_SIZE                                       0x1
#define _PIE1_TMR2IE_LENGTH                                     0x1
#define _PIE1_TMR2IE_MASK                                       0x2
#define _PIE1_CCP1IE_POSN                                       0x2
#define _PIE1_CCP1IE_POSITION                                   0x2
#define _PIE1_CCP1IE_SIZE                                       0x1
#define _PIE1_CCP1IE_LENGTH                                     0x1
#define _PIE1_CCP1IE_MASK                                       0x4
#define _PIE1_SSPIE_POSN                                        0x3
#define _PIE1_SSPIE_POSITION                                    0x3
#define _PIE1_SSPIE_SIZE                                        0x1
#define _PIE1_SSPIE_LENGTH                                      0x1
#define _PIE1_SSPIE_MASK                                        0x8
#define _PIE1_TXIE_POSN                                         0x4
#define _PIE1_TXIE_POSITION                                     0x4
#define _PIE1_TXIE_SIZE                                         0x1
#define _PIE1_TXIE_LENGTH                                       0x1
#define _PIE1_TXIE_MASK                                         0x10
```

```
#define _PIE1_RCIE_POSN                                 0x5
#define _PIE1_RCIE_POSITION                             0x5
#define _PIE1_RCIE_SIZE                                 0x1
#define _PIE1_RCIE_LENGTH                               0x1
#define _PIE1_RCIE_MASK                                 0x20
#define _PIE1_ADIE_POSN                                 0x6
#define _PIE1_ADIE_POSITION                             0x6
#define _PIE1_ADIE_SIZE                                 0x1
#define _PIE1_ADIE_LENGTH                               0x1
#define _PIE1_ADIE_MASK                                 0x40

// Register: PIE2
extern volatile unsigned char           PIE2                @ 0x08D;
#ifndef _LIB_BUILD
asm("PIE2 equ 08Dh");
#endif
// bitfield definitions
typedef union {
    struct {
        unsigned CCP2IE                 :1;
        unsigned                        :1;
        unsigned ULPWUIE                :1;
        unsigned BCLIE                  :1;
        unsigned EEIE                   :1;
        unsigned C1IE                   :1;
        unsigned C2IE                   :1;
        unsigned OSFIE                  :1;
    };
} PIE2bits_t;
extern volatile PIE2bits_t PIE2bits @ 0x08D;
// bitfield macros
#define _PIE2_CCP2IE_POSN                               0x0
#define _PIE2_CCP2IE_POSITION                           0x0
#define _PIE2_CCP2IE_SIZE                               0x1
#define _PIE2_CCP2IE_LENGTH                             0x1
#define _PIE2_CCP2IE_MASK                               0x1
#define _PIE2_ULPWUIE_POSN                              0x2
#define _PIE2_ULPWUIE_POSITION                          0x2
#define _PIE2_ULPWUIE_SIZE                              0x1
#define _PIE2_ULPWUIE_LENGTH                            0x1
#define _PIE2_ULPWUIE_MASK                              0x4
#define _PIE2_BCLIE_POSN                                0x3
#define _PIE2_BCLIE_POSITION                            0x3
#define _PIE2_BCLIE_SIZE                                0x1
#define _PIE2_BCLIE_LENGTH                              0x1
#define _PIE2_BCLIE_MASK                                0x8
#define _PIE2_EEIE_POSN                                 0x4
#define _PIE2_EEIE_POSITION                             0x4
#define _PIE2_EEIE_SIZE                                 0x1
#define _PIE2_EEIE_LENGTH                               0x1
#define _PIE2_EEIE_MASK                                 0x10
#define _PIE2_C1IE_POSN                                 0x5
#define _PIE2_C1IE_POSITION                             0x5
#define _PIE2_C1IE_SIZE                                 0x1
#define _PIE2_C1IE_LENGTH                               0x1
#define _PIE2_C1IE_MASK                                 0x20
#define _PIE2_C2IE_POSN                                 0x6
#define _PIE2_C2IE_POSITION                             0x6
#define _PIE2_C2IE_SIZE                                 0x1
#define _PIE2_C2IE_LENGTH                               0x1
```

```
#define _PIE2_C2IE_MASK                                 0x40
#define _PIE2_OSFIE_POSN                                0x7
#define _PIE2_OSFIE_POSITION                            0x7
#define _PIE2_OSFIE_SIZE                                0x1
#define _PIE2_OSFIE_LENGTH                              0x1
#define _PIE2_OSFIE_MASK                                0x80

// Register: PCON
extern volatile unsigned char           PCON                @ 0x08E;
#ifndef _LIB_BUILD
asm("PCON equ 08Eh");
#endif
// bitfield definitions
typedef union {
    struct {
        unsigned nBOR                   :1;
        unsigned nPOR                   :1;
        unsigned                        :2;
        unsigned SBOREN                 :1;
        unsigned ULPWUE                 :1;
    };
    struct {
        unsigned nBO                    :1;
    };
} PCONbits_t;
extern volatile PCONbits_t PCONbits @ 0x08E;
// bitfield macros
#define _PCON_nBOR_POSN                                 0x0
#define _PCON_nBOR_POSITION                             0x0
#define _PCON_nBOR_SIZE                                 0x1
#define _PCON_nBOR_LENGTH                               0x1
#define _PCON_nBOR_MASK                                 0x1
#define _PCON_nPOR_POSN                                 0x1
#define _PCON_nPOR_POSITION                             0x1
#define _PCON_nPOR_SIZE                                 0x1
#define _PCON_nPOR_LENGTH                               0x1
#define _PCON_nPOR_MASK                                 0x2
#define _PCON_SBOREN_POSN                               0x4
#define _PCON_SBOREN_POSITION                           0x4
#define _PCON_SBOREN_SIZE                               0x1
#define _PCON_SBOREN_LENGTH                             0x1
#define _PCON_SBOREN_MASK                               0x10
#define _PCON_ULPWUE_POSN                               0x5
#define _PCON_ULPWUE_POSITION                           0x5
#define _PCON_ULPWUE_SIZE                               0x1
#define _PCON_ULPWUE_LENGTH                             0x1
#define _PCON_ULPWUE_MASK                               0x20
#define _PCON_nBO_POSN                                  0x0
#define _PCON_nBO_POSITION                              0x0
#define _PCON_nBO_SIZE                                  0x1
#define _PCON_nBO_LENGTH                                0x1
#define _PCON_nBO_MASK                                  0x1

// Register: OSCCON
extern volatile unsigned char           OSCCON              @ 0x08F;
#ifndef _LIB_BUILD
asm("OSCCON equ 08Fh");
#endif
// bitfield definitions
typedef union {
```

```
        struct {
            unsigned SCS                    :1;
            unsigned LTS                    :1;
            unsigned HTS                    :1;
            unsigned OSTS                   :1;
            unsigned IRCF                   :3;
        };
        struct {
            unsigned                        :4;
            unsigned IRCF0                  :1;
            unsigned IRCF1                  :1;
            unsigned IRCF2                  :1;
        };
    } OSCCONbits_t;
    extern volatile OSCCONbits_t OSCCONbits @ 0x08F;
    // bitfield macros
    #define _OSCCON_SCS_POSN                                        0x0
    #define _OSCCON_SCS_POSITION                                    0x0
    #define _OSCCON_SCS_SIZE                                        0x1
    #define _OSCCON_SCS_LENGTH                                      0x1
    #define _OSCCON_SCS_MASK                                        0x1
    #define _OSCCON_LTS_POSN                                        0x1
    #define _OSCCON_LTS_POSITION                                    0x1
    #define _OSCCON_LTS_SIZE                                        0x1
    #define _OSCCON_LTS_LENGTH                                      0x1
    #define _OSCCON_LTS_MASK                                        0x2
    #define _OSCCON_HTS_POSN                                        0x2
    #define _OSCCON_HTS_POSITION                                    0x2
    #define _OSCCON_HTS_SIZE                                        0x1
    #define _OSCCON_HTS_LENGTH                                      0x1
    #define _OSCCON_HTS_MASK                                        0x4
    #define _OSCCON_OSTS_POSN                                       0x3
    #define _OSCCON_OSTS_POSITION                                   0x3
    #define _OSCCON_OSTS_SIZE                                       0x1
    #define _OSCCON_OSTS_LENGTH                                     0x1
    #define _OSCCON_OSTS_MASK                                       0x8
    #define _OSCCON_IRCF_POSN                                       0x4
    #define _OSCCON_IRCF_POSITION                                   0x4
    #define _OSCCON_IRCF_SIZE                                       0x3
    #define _OSCCON_IRCF_LENGTH                                     0x3
    #define _OSCCON_IRCF_MASK                                       0x70
    #define _OSCCON_IRCF0_POSN                                      0x4
    #define _OSCCON_IRCF0_POSITION                                  0x4
    #define _OSCCON_IRCF0_SIZE                                      0x1
    #define _OSCCON_IRCF0_LENGTH                                    0x1
    #define _OSCCON_IRCF0_MASK                                      0x10
    #define _OSCCON_IRCF1_POSN                                      0x5
    #define _OSCCON_IRCF1_POSITION                                  0x5
    #define _OSCCON_IRCF1_SIZE                                      0x1
    #define _OSCCON_IRCF1_LENGTH                                    0x1
    #define _OSCCON_IRCF1_MASK                                      0x20
    #define _OSCCON_IRCF2_POSN                                      0x6
    #define _OSCCON_IRCF2_POSITION                                  0x6
    #define _OSCCON_IRCF2_SIZE                                      0x1
    #define _OSCCON_IRCF2_LENGTH                                    0x1
    #define _OSCCON_IRCF2_MASK                                      0x40

    // Register: OSCTUNE
    extern volatile unsigned char           OSCTUNE             @ 0x090;
    #ifndef _LIB_BUILD
```

```
asm("OSCTUNE equ 090h");
#endif
// bitfield definitions
typedef union {
    struct {
        unsigned TUN                    :5;
    };
    struct {
        unsigned TUN0                   :1;
        unsigned TUN1                   :1;
        unsigned TUN2                   :1;
        unsigned TUN3                   :1;
        unsigned TUN4                   :1;
    };
} OSCTUNEbits_t;
extern volatile OSCTUNEbits_t OSCTUNEbits @ 0x090;
// bitfield macros
#define _OSCTUNE_TUN_POSN                                       0x0
#define _OSCTUNE_TUN_POSITION                                   0x0
#define _OSCTUNE_TUN_SIZE                                       0x5
#define _OSCTUNE_TUN_LENGTH                                     0x5
#define _OSCTUNE_TUN_MASK                                       0x1F
#define _OSCTUNE_TUN0_POSN                                      0x0
#define _OSCTUNE_TUN0_POSITION                                  0x0
#define _OSCTUNE_TUN0_SIZE                                      0x1
#define _OSCTUNE_TUN0_LENGTH                                    0x1
#define _OSCTUNE_TUN0_MASK                                      0x1
#define _OSCTUNE_TUN1_POSN                                      0x1
#define _OSCTUNE_TUN1_POSITION                                  0x1
#define _OSCTUNE_TUN1_SIZE                                      0x1
#define _OSCTUNE_TUN1_LENGTH                                    0x1
#define _OSCTUNE_TUN1_MASK                                      0x2
#define _OSCTUNE_TUN2_POSN                                      0x2
#define _OSCTUNE_TUN2_POSITION                                  0x2
#define _OSCTUNE_TUN2_SIZE                                      0x1
#define _OSCTUNE_TUN2_LENGTH                                    0x1
#define _OSCTUNE_TUN2_MASK                                      0x4
#define _OSCTUNE_TUN3_POSN                                      0x3
#define _OSCTUNE_TUN3_POSITION                                  0x3
#define _OSCTUNE_TUN3_SIZE                                      0x1
#define _OSCTUNE_TUN3_LENGTH                                    0x1
#define _OSCTUNE_TUN3_MASK                                      0x8
#define _OSCTUNE_TUN4_POSN                                      0x4
#define _OSCTUNE_TUN4_POSITION                                  0x4
#define _OSCTUNE_TUN4_SIZE                                      0x1
#define _OSCTUNE_TUN4_LENGTH                                    0x1
#define _OSCTUNE_TUN4_MASK                                      0x10

// Register: SSPCON2
extern volatile unsigned char           SSPCON2             @ 0x091;
#ifndef _LIB_BUILD
asm("SSPCON2 equ 091h");
#endif
// bitfield definitions
typedef union {
    struct {
        unsigned SEN                    :1;
        unsigned RSEN                   :1;
        unsigned PEN                    :1;
        unsigned RCEN                   :1;
```

```
        unsigned ACKEN                  :1;
        unsigned ACKDT                  :1;
        unsigned ACKSTAT                :1;
        unsigned GCEN                   :1;
    };
} SSPCON2bits_t;
extern volatile SSPCON2bits_t SSPCON2bits @ 0x091;
// bitfield macros
#define _SSPCON2_SEN_POSN                                       0x0
#define _SSPCON2_SEN_POSITION                                   0x0
#define _SSPCON2_SEN_SIZE                                       0x1
#define _SSPCON2_SEN_LENGTH                                     0x1
#define _SSPCON2_SEN_MASK                                       0x1
#define _SSPCON2_RSEN_POSN                                      0x1
#define _SSPCON2_RSEN_POSITION                                  0x1
#define _SSPCON2_RSEN_SIZE                                      0x1
#define _SSPCON2_RSEN_LENGTH                                    0x1
#define _SSPCON2_RSEN_MASK                                      0x2
#define _SSPCON2_PEN_POSN                                       0x2
#define _SSPCON2_PEN_POSITION                                   0x2
#define _SSPCON2_PEN_SIZE                                       0x1
#define _SSPCON2_PEN_LENGTH                                     0x1
#define _SSPCON2_PEN_MASK                                       0x4
#define _SSPCON2_RCEN_POSN                                      0x3
#define _SSPCON2_RCEN_POSITION                                  0x3
#define _SSPCON2_RCEN_SIZE                                      0x1
#define _SSPCON2_RCEN_LENGTH                                    0x1
#define _SSPCON2_RCEN_MASK                                      0x8
#define _SSPCON2_ACKEN_POSN                                     0x4
#define _SSPCON2_ACKEN_POSITION                                 0x4
#define _SSPCON2_ACKEN_SIZE                                     0x1
#define _SSPCON2_ACKEN_LENGTH                                   0x1
#define _SSPCON2_ACKEN_MASK                                     0x10
#define _SSPCON2_ACKDT_POSN                                     0x5
#define _SSPCON2_ACKDT_POSITION                                 0x5
#define _SSPCON2_ACKDT_SIZE                                     0x1
#define _SSPCON2_ACKDT_LENGTH                                   0x1
#define _SSPCON2_ACKDT_MASK                                     0x20
#define _SSPCON2_ACKSTAT_POSN                                   0x6
#define _SSPCON2_ACKSTAT_POSITION                               0x6
#define _SSPCON2_ACKSTAT_SIZE                                   0x1
#define _SSPCON2_ACKSTAT_LENGTH                                 0x1
#define _SSPCON2_ACKSTAT_MASK                                   0x40
#define _SSPCON2_GCEN_POSN                                      0x7
#define _SSPCON2_GCEN_POSITION                                  0x7
#define _SSPCON2_GCEN_SIZE                                      0x1
#define _SSPCON2_GCEN_LENGTH                                    0x1
#define _SSPCON2_GCEN_MASK                                      0x80

// Register: PR2
extern volatile unsigned char           PR2                     @ 0x092;
#ifndef _LIB_BUILD
asm("PR2 equ 092h");
#endif

// Register: SSPADD
extern volatile unsigned char           SSPADD                  @ 0x093;
#ifndef _LIB_BUILD
asm("SSPADD equ 093h");
#endif
```

```
// Register: SSPMSK
extern volatile unsigned char           SSPMSK              @ 0x093;
#ifndef _LIB_BUILD
asm("SSPMSK equ 093h");
#endif
// aliases
extern volatile unsigned char           MSK                 @ 0x093;
#ifndef _LIB_BUILD
asm("MSK equ 093h");
#endif
// bitfield definitions
typedef union {
    struct {
        unsigned MSK0                   :1;
        unsigned MSK1                   :1;
        unsigned MSK2                   :1;
        unsigned MSK3                   :1;
        unsigned MSK4                   :1;
        unsigned MSK5                   :1;
        unsigned MSK6                   :1;
        unsigned MSK7                   :1;
    };
} SSPMSKbits_t;
extern volatile SSPMSKbits_t SSPMSKbits @ 0x093;
// bitfield macros
#define _SSPMSK_MSK0_POSN                                   0x0
#define _SSPMSK_MSK0_POSITION                               0x0
#define _SSPMSK_MSK0_SIZE                                   0x1
#define _SSPMSK_MSK0_LENGTH                                 0x1
#define _SSPMSK_MSK0_MASK                                   0x1
#define _SSPMSK_MSK1_POSN                                   0x1
#define _SSPMSK_MSK1_POSITION                               0x1
#define _SSPMSK_MSK1_SIZE                                   0x1
#define _SSPMSK_MSK1_LENGTH                                 0x1
#define _SSPMSK_MSK1_MASK                                   0x2
#define _SSPMSK_MSK2_POSN                                   0x2
#define _SSPMSK_MSK2_POSITION                               0x2
#define _SSPMSK_MSK2_SIZE                                   0x1
#define _SSPMSK_MSK2_LENGTH                                 0x1
#define _SSPMSK_MSK2_MASK                                   0x4
#define _SSPMSK_MSK3_POSN                                   0x3
#define _SSPMSK_MSK3_POSITION                               0x3
#define _SSPMSK_MSK3_SIZE                                   0x1
#define _SSPMSK_MSK3_LENGTH                                 0x1
#define _SSPMSK_MSK3_MASK                                   0x8
#define _SSPMSK_MSK4_POSN                                   0x4
#define _SSPMSK_MSK4_POSITION                               0x4
#define _SSPMSK_MSK4_SIZE                                   0x1
#define _SSPMSK_MSK4_LENGTH                                 0x1
#define _SSPMSK_MSK4_MASK                                   0x10
#define _SSPMSK_MSK5_POSN                                   0x5
#define _SSPMSK_MSK5_POSITION                               0x5
#define _SSPMSK_MSK5_SIZE                                   0x1
#define _SSPMSK_MSK5_LENGTH                                 0x1
#define _SSPMSK_MSK5_MASK                                   0x20
#define _SSPMSK_MSK6_POSN                                   0x6
#define _SSPMSK_MSK6_POSITION                               0x6
#define _SSPMSK_MSK6_SIZE                                   0x1
#define _SSPMSK_MSK6_LENGTH                                 0x1
```

```
#define _SSPMSK_MSK6_MASK                                0x40
#define _SSPMSK_MSK7_POSN                                0x7
#define _SSPMSK_MSK7_POSITION                            0x7
#define _SSPMSK_MSK7_SIZE                                0x1
#define _SSPMSK_MSK7_LENGTH                              0x1
#define _SSPMSK_MSK7_MASK                                0x80
// alias bitfield definitions
typedef union {
    struct {
        unsigned MSK0                   :1;
        unsigned MSK1                   :1;
        unsigned MSK2                   :1;
        unsigned MSK3                   :1;
        unsigned MSK4                   :1;
        unsigned MSK5                   :1;
        unsigned MSK6                   :1;
        unsigned MSK7                   :1;
    };
} MSKbits_t;
extern volatile MSKbits_t MSKbits @ 0x093;
// bitfield macros
#define _MSK_MSK0_POSN                                   0x0
#define _MSK_MSK0_POSITION                               0x0
#define _MSK_MSK0_SIZE                                   0x1
#define _MSK_MSK0_LENGTH                                 0x1
#define _MSK_MSK0_MASK                                   0x1
#define _MSK_MSK1_POSN                                   0x1
#define _MSK_MSK1_POSITION                               0x1
#define _MSK_MSK1_SIZE                                   0x1
#define _MSK_MSK1_LENGTH                                 0x1
#define _MSK_MSK1_MASK                                   0x2
#define _MSK_MSK2_POSN                                   0x2
#define _MSK_MSK2_POSITION                               0x2
#define _MSK_MSK2_SIZE                                   0x1
#define _MSK_MSK2_LENGTH                                 0x1
#define _MSK_MSK2_MASK                                   0x4
#define _MSK_MSK3_POSN                                   0x3
#define _MSK_MSK3_POSITION                               0x3
#define _MSK_MSK3_SIZE                                   0x1
#define _MSK_MSK3_LENGTH                                 0x1
#define _MSK_MSK3_MASK                                   0x8
#define _MSK_MSK4_POSN                                   0x4
#define _MSK_MSK4_POSITION                               0x4
#define _MSK_MSK4_SIZE                                   0x1
#define _MSK_MSK4_LENGTH                                 0x1
#define _MSK_MSK4_MASK                                   0x10
#define _MSK_MSK5_POSN                                   0x5
#define _MSK_MSK5_POSITION                               0x5
#define _MSK_MSK5_SIZE                                   0x1
#define _MSK_MSK5_LENGTH                                 0x1
#define _MSK_MSK5_MASK                                   0x20
#define _MSK_MSK6_POSN                                   0x6
#define _MSK_MSK6_POSITION                               0x6
#define _MSK_MSK6_SIZE                                   0x1
#define _MSK_MSK6_LENGTH                                 0x1
#define _MSK_MSK6_MASK                                   0x40
#define _MSK_MSK7_POSN                                   0x7
#define _MSK_MSK7_POSITION                               0x7
#define _MSK_MSK7_SIZE                                   0x1
#define _MSK_MSK7_LENGTH                                 0x1
```

```
#define _MSK_MSK7_MASK                                  0x80

// Register: SSPSTAT
extern volatile unsigned char           SSPSTAT         @ 0x094;
#ifndef _LIB_BUILD
asm("SSPSTAT equ 094h");
#endif
// bitfield definitions
typedef union {
    struct {
        unsigned BF                     :1;
        unsigned UA                     :1;
        unsigned R_nW                   :1;
        unsigned S                      :1;
        unsigned P                      :1;
        unsigned D_nA                   :1;
        unsigned CKE                    :1;
        unsigned SMP                    :1;
    };
    struct {
        unsigned                        :2;
        unsigned R                      :1;
        unsigned                        :2;
        unsigned D                      :1;
    };
    struct {
        unsigned                        :2;
        unsigned I2C_READ               :1;
        unsigned I2C_START              :1;
        unsigned I2C_STOP               :1;
        unsigned I2C_DATA               :1;
    };
    struct {
        unsigned                        :2;
        unsigned nW                     :1;
        unsigned                        :2;
        unsigned nA                     :1;
    };
    struct {
        unsigned                        :2;
        unsigned nWRITE                 :1;
        unsigned                        :2;
        unsigned nADDRESS               :1;
    };
    struct {
        unsigned                        :2;
        unsigned R_W                    :1;
        unsigned                        :2;
        unsigned D_A                    :1;
    };
    struct {
        unsigned                        :2;
        unsigned READ_WRITE             :1;
        unsigned                        :2;
        unsigned DATA_ADDRESS           :1;
    };
} SSPSTATbits_t;
extern volatile SSPSTATbits_t SSPSTATbits @ 0x094;
// bitfield macros
#define _SSPSTAT_BF_POSN                                0x0
```

```
#define _SSPSTAT_BF_POSITION                    0x0
#define _SSPSTAT_BF_SIZE                        0x1
#define _SSPSTAT_BF_LENGTH                      0x1
#define _SSPSTAT_BF_MASK                        0x1
#define _SSPSTAT_UA_POSN                        0x1
#define _SSPSTAT_UA_POSITION                    0x1
#define _SSPSTAT_UA_SIZE                        0x1
#define _SSPSTAT_UA_LENGTH                      0x1
#define _SSPSTAT_UA_MASK                        0x2
#define _SSPSTAT_R_nW_POSN                      0x2
#define _SSPSTAT_R_nW_POSITION                  0x2
#define _SSPSTAT_R_nW_SIZE                      0x1
#define _SSPSTAT_R_nW_LENGTH                    0x1
#define _SSPSTAT_R_nW_MASK                      0x4
#define _SSPSTAT_S_POSN                         0x3
#define _SSPSTAT_S_POSITION                     0x3
#define _SSPSTAT_S_SIZE                         0x1
#define _SSPSTAT_S_LENGTH                       0x1
#define _SSPSTAT_S_MASK                         0x8
#define _SSPSTAT_P_POSN                         0x4
#define _SSPSTAT_P_POSITION                     0x4
#define _SSPSTAT_P_SIZE                         0x1
#define _SSPSTAT_P_LENGTH                       0x1
#define _SSPSTAT_P_MASK                         0x10
#define _SSPSTAT_D_nA_POSN                      0x5
#define _SSPSTAT_D_nA_POSITION                  0x5
#define _SSPSTAT_D_nA_SIZE                      0x1
#define _SSPSTAT_D_nA_LENGTH                    0x1
#define _SSPSTAT_D_nA_MASK                      0x20
#define _SSPSTAT_CKE_POSN                       0x6
#define _SSPSTAT_CKE_POSITION                   0x6
#define _SSPSTAT_CKE_SIZE                       0x1
#define _SSPSTAT_CKE_LENGTH                     0x1
#define _SSPSTAT_CKE_MASK                       0x40
#define _SSPSTAT_SMP_POSN                       0x7
#define _SSPSTAT_SMP_POSITION                   0x7
#define _SSPSTAT_SMP_SIZE                       0x1
#define _SSPSTAT_SMP_LENGTH                     0x1
#define _SSPSTAT_SMP_MASK                       0x80
#define _SSPSTAT_R_POSN                         0x2
#define _SSPSTAT_R_POSITION                     0x2
#define _SSPSTAT_R_SIZE                         0x1
#define _SSPSTAT_R_LENGTH                       0x1
#define _SSPSTAT_R_MASK                         0x4
#define _SSPSTAT_D_POSN                         0x5
#define _SSPSTAT_D_POSITION                     0x5
#define _SSPSTAT_D_SIZE                         0x1
#define _SSPSTAT_D_LENGTH                       0x1
#define _SSPSTAT_D_MASK                         0x20
#define _SSPSTAT_I2C_READ_POSN                  0x2
#define _SSPSTAT_I2C_READ_POSITION              0x2
#define _SSPSTAT_I2C_READ_SIZE                  0x1
#define _SSPSTAT_I2C_READ_LENGTH                0x1
#define _SSPSTAT_I2C_READ_MASK                  0x4
#define _SSPSTAT_I2C_START_POSN                 0x3
#define _SSPSTAT_I2C_START_POSITION             0x3
#define _SSPSTAT_I2C_START_SIZE                 0x1
#define _SSPSTAT_I2C_START_LENGTH               0x1
#define _SSPSTAT_I2C_START_MASK                 0x8
#define _SSPSTAT_I2C_STOP_POSN                  0x4
```

```
#define _SSPSTAT_I2C_STOP_POSITION                      0x4
#define _SSPSTAT_I2C_STOP_SIZE                          0x1
#define _SSPSTAT_I2C_STOP_LENGTH                        0x1
#define _SSPSTAT_I2C_STOP_MASK                          0x10
#define _SSPSTAT_I2C_DATA_POSN                          0x5
#define _SSPSTAT_I2C_DATA_POSITION                      0x5
#define _SSPSTAT_I2C_DATA_SIZE                          0x1
#define _SSPSTAT_I2C_DATA_LENGTH                        0x1
#define _SSPSTAT_I2C_DATA_MASK                          0x20
#define _SSPSTAT_nW_POSN                                0x2
#define _SSPSTAT_nW_POSITION                            0x2
#define _SSPSTAT_nW_SIZE                                0x1
#define _SSPSTAT_nW_LENGTH                              0x1
#define _SSPSTAT_nW_MASK                                0x4
#define _SSPSTAT_nA_POSN                                0x5
#define _SSPSTAT_nA_POSITION                            0x5
#define _SSPSTAT_nA_SIZE                                0x1
#define _SSPSTAT_nA_LENGTH                              0x1
#define _SSPSTAT_nA_MASK                                0x20
#define _SSPSTAT_nWRITE_POSN                            0x2
#define _SSPSTAT_nWRITE_POSITION                        0x2
#define _SSPSTAT_nWRITE_SIZE                            0x1
#define _SSPSTAT_nWRITE_LENGTH                          0x1
#define _SSPSTAT_nWRITE_MASK                            0x4
#define _SSPSTAT_nADDRESS_POSN                          0x5
#define _SSPSTAT_nADDRESS_POSITION                      0x5
#define _SSPSTAT_nADDRESS_SIZE                          0x1
#define _SSPSTAT_nADDRESS_LENGTH                        0x1
#define _SSPSTAT_nADDRESS_MASK                          0x20
#define _SSPSTAT_R_W_POSN                               0x2
#define _SSPSTAT_R_W_POSITION                           0x2
#define _SSPSTAT_R_W_SIZE                               0x1
#define _SSPSTAT_R_W_LENGTH                             0x1
#define _SSPSTAT_R_W_MASK                               0x4
#define _SSPSTAT_D_A_POSN                               0x5
#define _SSPSTAT_D_A_POSITION                           0x5
#define _SSPSTAT_D_A_SIZE                               0x1
#define _SSPSTAT_D_A_LENGTH                             0x1
#define _SSPSTAT_D_A_MASK                               0x20
#define _SSPSTAT_READ_WRITE_POSN                        0x2
#define _SSPSTAT_READ_WRITE_POSITION                    0x2
#define _SSPSTAT_READ_WRITE_SIZE                        0x1
#define _SSPSTAT_READ_WRITE_LENGTH                      0x1
#define _SSPSTAT_READ_WRITE_MASK                        0x4
#define _SSPSTAT_DATA_ADDRESS_POSN                      0x5
#define _SSPSTAT_DATA_ADDRESS_POSITION                  0x5
#define _SSPSTAT_DATA_ADDRESS_SIZE                      0x1
#define _SSPSTAT_DATA_ADDRESS_LENGTH                    0x1
#define _SSPSTAT_DATA_ADDRESS_MASK                      0x20

// Register: WPUB
extern volatile unsigned char           WPUB                @ 0x095;
#ifndef _LIB_BUILD
asm("WPUB equ 095h");
#endif
// bitfield definitions
typedef union {
    struct {
        unsigned WPUB                   :8;
    };
```

```
    struct {
        unsigned WPUB0                  :1;
        unsigned WPUB1                  :1;
        unsigned WPUB2                  :1;
        unsigned WPUB3                  :1;
        unsigned WPUB4                  :1;
        unsigned WPUB5                  :1;
        unsigned WPUB6                  :1;
        unsigned WPUB7                  :1;
    };
} WPUBbits_t;
extern volatile WPUBbits_t WPUBbits @ 0x095;
// bitfield macros
#define _WPUB_WPUB_POSN                                         0x0
#define _WPUB_WPUB_POSITION                                     0x0
#define _WPUB_WPUB_SIZE                                         0x8
#define _WPUB_WPUB_LENGTH                                       0x8
#define _WPUB_WPUB_MASK                                         0xFF
#define _WPUB_WPUB0_POSN                                        0x0
#define _WPUB_WPUB0_POSITION                                    0x0
#define _WPUB_WPUB0_SIZE                                        0x1
#define _WPUB_WPUB0_LENGTH                                      0x1
#define _WPUB_WPUB0_MASK                                        0x1
#define _WPUB_WPUB1_POSN                                        0x1
#define _WPUB_WPUB1_POSITION                                    0x1
#define _WPUB_WPUB1_SIZE                                        0x1
#define _WPUB_WPUB1_LENGTH                                      0x1
#define _WPUB_WPUB1_MASK                                        0x2
#define _WPUB_WPUB2_POSN                                        0x2
#define _WPUB_WPUB2_POSITION                                    0x2
#define _WPUB_WPUB2_SIZE                                        0x1
#define _WPUB_WPUB2_LENGTH                                      0x1
#define _WPUB_WPUB2_MASK                                        0x4
#define _WPUB_WPUB3_POSN                                        0x3
#define _WPUB_WPUB3_POSITION                                    0x3
#define _WPUB_WPUB3_SIZE                                        0x1
#define _WPUB_WPUB3_LENGTH                                      0x1
#define _WPUB_WPUB3_MASK                                        0x8
#define _WPUB_WPUB4_POSN                                        0x4
#define _WPUB_WPUB4_POSITION                                    0x4
#define _WPUB_WPUB4_SIZE                                        0x1
#define _WPUB_WPUB4_LENGTH                                      0x1
#define _WPUB_WPUB4_MASK                                        0x10
#define _WPUB_WPUB5_POSN                                        0x5
#define _WPUB_WPUB5_POSITION                                    0x5
#define _WPUB_WPUB5_SIZE                                        0x1
#define _WPUB_WPUB5_LENGTH                                      0x1
#define _WPUB_WPUB5_MASK                                        0x20
#define _WPUB_WPUB6_POSN                                        0x6
#define _WPUB_WPUB6_POSITION                                    0x6
#define _WPUB_WPUB6_SIZE                                        0x1
#define _WPUB_WPUB6_LENGTH                                      0x1
#define _WPUB_WPUB6_MASK                                        0x40
#define _WPUB_WPUB7_POSN                                        0x7
#define _WPUB_WPUB7_POSITION                                    0x7
#define _WPUB_WPUB7_SIZE                                        0x1
#define _WPUB_WPUB7_LENGTH                                      0x1
#define _WPUB_WPUB7_MASK                                        0x80

// Register: IOCB
```

```
extern volatile unsigned char           IOCB                @ 0x096;
#ifndef _LIB_BUILD
asm("IOCB equ 096h");
#endif
// bitfield definitions
typedef union {
    struct {
        unsigned IOCB                   :8;
    };
    struct {
        unsigned IOCB0                  :1;
        unsigned IOCB1                  :1;
        unsigned IOCB2                  :1;
        unsigned IOCB3                  :1;
        unsigned IOCB4                  :1;
        unsigned IOCB5                  :1;
        unsigned IOCB6                  :1;
        unsigned IOCB7                  :1;
    };
} IOCBbits_t;
extern volatile IOCBbits_t IOCBbits @ 0x096;
// bitfield macros
#define _IOCB_IOCB_POSN                                     0x0
#define _IOCB_IOCB_POSITION                                 0x0
#define _IOCB_IOCB_SIZE                                     0x8
#define _IOCB_IOCB_LENGTH                                   0x8
#define _IOCB_IOCB_MASK                                     0xFF
#define _IOCB_IOCB0_POSN                                    0x0
#define _IOCB_IOCB0_POSITION                                0x0
#define _IOCB_IOCB0_SIZE                                    0x1
#define _IOCB_IOCB0_LENGTH                                  0x1
#define _IOCB_IOCB0_MASK                                    0x1
#define _IOCB_IOCB1_POSN                                    0x1
#define _IOCB_IOCB1_POSITION                                0x1
#define _IOCB_IOCB1_SIZE                                    0x1
#define _IOCB_IOCB1_LENGTH                                  0x1
#define _IOCB_IOCB1_MASK                                    0x2
#define _IOCB_IOCB2_POSN                                    0x2
#define _IOCB_IOCB2_POSITION                                0x2
#define _IOCB_IOCB2_SIZE                                    0x1
#define _IOCB_IOCB2_LENGTH                                  0x1
#define _IOCB_IOCB2_MASK                                    0x4
#define _IOCB_IOCB3_POSN                                    0x3
#define _IOCB_IOCB3_POSITION                                0x3
#define _IOCB_IOCB3_SIZE                                    0x1
#define _IOCB_IOCB3_LENGTH                                  0x1
#define _IOCB_IOCB3_MASK                                    0x8
#define _IOCB_IOCB4_POSN                                    0x4
#define _IOCB_IOCB4_POSITION                                0x4
#define _IOCB_IOCB4_SIZE                                    0x1
#define _IOCB_IOCB4_LENGTH                                  0x1
#define _IOCB_IOCB4_MASK                                    0x10
#define _IOCB_IOCB5_POSN                                    0x5
#define _IOCB_IOCB5_POSITION                                0x5
#define _IOCB_IOCB5_SIZE                                    0x1
#define _IOCB_IOCB5_LENGTH                                  0x1
#define _IOCB_IOCB5_MASK                                    0x20
#define _IOCB_IOCB6_POSN                                    0x6
#define _IOCB_IOCB6_POSITION                                0x6
#define _IOCB_IOCB6_SIZE                                    0x1
```

```
#define _IOCB_IOCB6_LENGTH                              0x1
#define _IOCB_IOCB6_MASK                                0x40
#define _IOCB_IOCB7_POSN                                0x7
#define _IOCB_IOCB7_POSITION                            0x7
#define _IOCB_IOCB7_SIZE                                0x1
#define _IOCB_IOCB7_LENGTH                              0x1
#define _IOCB_IOCB7_MASK                                0x80

// Register: VRCON
extern volatile unsigned char           VRCON               @ 0x097;
#ifndef _LIB_BUILD
asm("VRCON equ 097h");
#endif
// bitfield definitions
typedef union {
    struct {
        unsigned VR                     :4;
        unsigned VRSS                   :1;
        unsigned VRR                    :1;
        unsigned VROE                   :1;
        unsigned VREN                   :1;
    };
    struct {
        unsigned VR0                    :1;
        unsigned VR1                    :1;
        unsigned VR2                    :1;
        unsigned VR3                    :1;
    };
} VRCONbits_t;
extern volatile VRCONbits_t VRCONbits @ 0x097;
// bitfield macros
#define _VRCON_VR_POSN                                  0x0
#define _VRCON_VR_POSITION                              0x0
#define _VRCON_VR_SIZE                                  0x4
#define _VRCON_VR_LENGTH                                0x4
#define _VRCON_VR_MASK                                  0xF
#define _VRCON_VRSS_POSN                                0x4
#define _VRCON_VRSS_POSITION                            0x4
#define _VRCON_VRSS_SIZE                                0x1
#define _VRCON_VRSS_LENGTH                              0x1
#define _VRCON_VRSS_MASK                                0x10
#define _VRCON_VRR_POSN                                 0x5
#define _VRCON_VRR_POSITION                             0x5
#define _VRCON_VRR_SIZE                                 0x1
#define _VRCON_VRR_LENGTH                               0x1
#define _VRCON_VRR_MASK                                 0x20
#define _VRCON_VROE_POSN                                0x6
#define _VRCON_VROE_POSITION                            0x6
#define _VRCON_VROE_SIZE                                0x1
#define _VRCON_VROE_LENGTH                              0x1
#define _VRCON_VROE_MASK                                0x40
#define _VRCON_VREN_POSN                                0x7
#define _VRCON_VREN_POSITION                            0x7
#define _VRCON_VREN_SIZE                                0x1
#define _VRCON_VREN_LENGTH                              0x1
#define _VRCON_VREN_MASK                                0x80
#define _VRCON_VR0_POSN                                 0x0
#define _VRCON_VR0_POSITION                             0x0
#define _VRCON_VR0_SIZE                                 0x1
#define _VRCON_VR0_LENGTH                               0x1
```

```
#define _VRCON_VR0_MASK                                 0x1
#define _VRCON_VR1_POSN                                 0x1
#define _VRCON_VR1_POSITION                             0x1
#define _VRCON_VR1_SIZE                                 0x1
#define _VRCON_VR1_LENGTH                               0x1
#define _VRCON_VR1_MASK                                 0x2
#define _VRCON_VR2_POSN                                 0x2
#define _VRCON_VR2_POSITION                             0x2
#define _VRCON_VR2_SIZE                                 0x1
#define _VRCON_VR2_LENGTH                               0x1
#define _VRCON_VR2_MASK                                 0x4
#define _VRCON_VR3_POSN                                 0x3
#define _VRCON_VR3_POSITION                             0x3
#define _VRCON_VR3_SIZE                                 0x1
#define _VRCON_VR3_LENGTH                               0x1
#define _VRCON_VR3_MASK                                 0x8

// Register: TXSTA
extern volatile unsigned char           TXSTA               @ 0x098;
#ifndef _LIB_BUILD
asm("TXSTA equ 098h");
#endif
// bitfield definitions
typedef union {
    struct {
        unsigned TX9D                   :1;
        unsigned TRMT                   :1;
        unsigned BRGH                   :1;
        unsigned SENDB                  :1;
        unsigned SYNC                   :1;
        unsigned TXEN                   :1;
        unsigned TX9                    :1;
        unsigned CSRC                   :1;
    };
    struct {
        unsigned TXD8                   :1;
        unsigned                        :5;
        unsigned nTX8                   :1;
    };
    struct {
        unsigned                        :6;
        unsigned TX8_9                  :1;
    };
} TXSTAbits_t;
extern volatile TXSTAbits_t TXSTAbits @ 0x098;
// bitfield macros
#define _TXSTA_TX9D_POSN                                0x0
#define _TXSTA_TX9D_POSITION                            0x0
#define _TXSTA_TX9D_SIZE                                0x1
#define _TXSTA_TX9D_LENGTH                              0x1
#define _TXSTA_TX9D_MASK                                0x1
#define _TXSTA_TRMT_POSN                                0x1
#define _TXSTA_TRMT_POSITION                            0x1
#define _TXSTA_TRMT_SIZE                                0x1
#define _TXSTA_TRMT_LENGTH                              0x1
#define _TXSTA_TRMT_MASK                                0x2
#define _TXSTA_BRGH_POSN                                0x2
#define _TXSTA_BRGH_POSITION                            0x2
#define _TXSTA_BRGH_SIZE                                0x1
#define _TXSTA_BRGH_LENGTH                              0x1
```

```
#define _TXSTA_BRGH_MASK                        0x4
#define _TXSTA_SENDB_POSN                       0x3
#define _TXSTA_SENDB_POSITION                   0x3
#define _TXSTA_SENDB_SIZE                       0x1
#define _TXSTA_SENDB_LENGTH                     0x1
#define _TXSTA_SENDB_MASK                       0x8
#define _TXSTA_SYNC_POSN                        0x4
#define _TXSTA_SYNC_POSITION                    0x4
#define _TXSTA_SYNC_SIZE                        0x1
#define _TXSTA_SYNC_LENGTH                      0x1
#define _TXSTA_SYNC_MASK                        0x10
#define _TXSTA_TXEN_POSN                        0x5
#define _TXSTA_TXEN_POSITION                    0x5
#define _TXSTA_TXEN_SIZE                        0x1
#define _TXSTA_TXEN_LENGTH                      0x1
#define _TXSTA_TXEN_MASK                        0x20
#define _TXSTA_TX9_POSN                         0x6
#define _TXSTA_TX9_POSITION                     0x6
#define _TXSTA_TX9_SIZE                         0x1
#define _TXSTA_TX9_LENGTH                       0x1
#define _TXSTA_TX9_MASK                         0x40
#define _TXSTA_CSRC_POSN                        0x7
#define _TXSTA_CSRC_POSITION                    0x7
#define _TXSTA_CSRC_SIZE                        0x1
#define _TXSTA_CSRC_LENGTH                      0x1
#define _TXSTA_CSRC_MASK                        0x80
#define _TXSTA_TXD8_POSN                        0x0
#define _TXSTA_TXD8_POSITION                    0x0
#define _TXSTA_TXD8_SIZE                        0x1
#define _TXSTA_TXD8_LENGTH                      0x1
#define _TXSTA_TXD8_MASK                        0x1
#define _TXSTA_nTX8_POSN                        0x6
#define _TXSTA_nTX8_POSITION                    0x6
#define _TXSTA_nTX8_SIZE                        0x1
#define _TXSTA_nTX8_LENGTH                      0x1
#define _TXSTA_nTX8_MASK                        0x40
#define _TXSTA_TX8_9_POSN                       0x6
#define _TXSTA_TX8_9_POSITION                   0x6
#define _TXSTA_TX8_9_SIZE                       0x1
#define _TXSTA_TX8_9_LENGTH                     0x1
#define _TXSTA_TX8_9_MASK                       0x40

// Register: SPBRG
extern volatile unsigned char           SPBRG               @ 0x099;
#ifndef _LIB_BUILD
asm("SPBRG equ 099h");
#endif
// bitfield definitions
typedef union {
    struct {
        unsigned BRG0                   :1;
        unsigned BRG1                   :1;
        unsigned BRG2                   :1;
        unsigned BRG3                   :1;
        unsigned BRG4                   :1;
        unsigned BRG5                   :1;
        unsigned BRG6                   :1;
        unsigned BRG7                   :1;
    };
} SPBRGbits_t;
```

```
extern volatile SPBRGbits_t SPBRGbits @ 0x099;
// bitfield macros
#define _SPBRG_BRG0_POSN                                0x0
#define _SPBRG_BRG0_POSITION                            0x0
#define _SPBRG_BRG0_SIZE                                0x1
#define _SPBRG_BRG0_LENGTH                              0x1
#define _SPBRG_BRG0_MASK                                0x1
#define _SPBRG_BRG1_POSN                                0x1
#define _SPBRG_BRG1_POSITION                            0x1
#define _SPBRG_BRG1_SIZE                                0x1
#define _SPBRG_BRG1_LENGTH                              0x1
#define _SPBRG_BRG1_MASK                                0x2
#define _SPBRG_BRG2_POSN                                0x2
#define _SPBRG_BRG2_POSITION                            0x2
#define _SPBRG_BRG2_SIZE                                0x1
#define _SPBRG_BRG2_LENGTH                              0x1
#define _SPBRG_BRG2_MASK                                0x4
#define _SPBRG_BRG3_POSN                                0x3
#define _SPBRG_BRG3_POSITION                            0x3
#define _SPBRG_BRG3_SIZE                                0x1
#define _SPBRG_BRG3_LENGTH                              0x1
#define _SPBRG_BRG3_MASK                                0x8
#define _SPBRG_BRG4_POSN                                0x4
#define _SPBRG_BRG4_POSITION                            0x4
#define _SPBRG_BRG4_SIZE                                0x1
#define _SPBRG_BRG4_LENGTH                              0x1
#define _SPBRG_BRG4_MASK                                0x10
#define _SPBRG_BRG5_POSN                                0x5
#define _SPBRG_BRG5_POSITION                            0x5
#define _SPBRG_BRG5_SIZE                                0x1
#define _SPBRG_BRG5_LENGTH                              0x1
#define _SPBRG_BRG5_MASK                                0x20
#define _SPBRG_BRG6_POSN                                0x6
#define _SPBRG_BRG6_POSITION                            0x6
#define _SPBRG_BRG6_SIZE                                0x1
#define _SPBRG_BRG6_LENGTH                              0x1
#define _SPBRG_BRG6_MASK                                0x40
#define _SPBRG_BRG7_POSN                                0x7
#define _SPBRG_BRG7_POSITION                            0x7
#define _SPBRG_BRG7_SIZE                                0x1
#define _SPBRG_BRG7_LENGTH                              0x1
#define _SPBRG_BRG7_MASK                                0x80

// Register: SPBRGH
extern volatile unsigned char           SPBRGH              @ 0x09A;
#ifndef _LIB_BUILD
asm("SPBRGH equ 09Ah");
#endif
// bitfield definitions
typedef union {
    struct {
        unsigned SPBRGH                 :8;
    };
    struct {
        unsigned BRG8                   :1;
        unsigned BRG9                   :1;
        unsigned BRG10                  :1;
        unsigned BRG11                  :1;
        unsigned BRG12                  :1;
        unsigned BRG13                  :1;
```

```
        unsigned BRG14                  :1;
        unsigned BRG15                  :1;
    };
} SPBRGHbits_t;
extern volatile SPBRGHbits_t SPBRGHbits @ 0x09A;
// bitfield macros
#define _SPBRGH_SPBRGH_POSN                                     0x0
#define _SPBRGH_SPBRGH_POSITION                                 0x0
#define _SPBRGH_SPBRGH_SIZE                                     0x8
#define _SPBRGH_SPBRGH_LENGTH                                   0x8
#define _SPBRGH_SPBRGH_MASK                                     0xFF
#define _SPBRGH_BRG8_POSN                                       0x0
#define _SPBRGH_BRG8_POSITION                                   0x0
#define _SPBRGH_BRG8_SIZE                                       0x1
#define _SPBRGH_BRG8_LENGTH                                     0x1
#define _SPBRGH_BRG8_MASK                                       0x1
#define _SPBRGH_BRG9_POSN                                       0x1
#define _SPBRGH_BRG9_POSITION                                   0x1
#define _SPBRGH_BRG9_SIZE                                       0x1
#define _SPBRGH_BRG9_LENGTH                                     0x1
#define _SPBRGH_BRG9_MASK                                       0x2
#define _SPBRGH_BRG10_POSN                                      0x2
#define _SPBRGH_BRG10_POSITION                                  0x2
#define _SPBRGH_BRG10_SIZE                                      0x1
#define _SPBRGH_BRG10_LENGTH                                    0x1
#define _SPBRGH_BRG10_MASK                                      0x4
#define _SPBRGH_BRG11_POSN                                      0x3
#define _SPBRGH_BRG11_POSITION                                  0x3
#define _SPBRGH_BRG11_SIZE                                      0x1
#define _SPBRGH_BRG11_LENGTH                                    0x1
#define _SPBRGH_BRG11_MASK                                      0x8
#define _SPBRGH_BRG12_POSN                                      0x4
#define _SPBRGH_BRG12_POSITION                                  0x4
#define _SPBRGH_BRG12_SIZE                                      0x1
#define _SPBRGH_BRG12_LENGTH                                    0x1
#define _SPBRGH_BRG12_MASK                                      0x10
#define _SPBRGH_BRG13_POSN                                      0x5
#define _SPBRGH_BRG13_POSITION                                  0x5
#define _SPBRGH_BRG13_SIZE                                      0x1
#define _SPBRGH_BRG13_LENGTH                                    0x1
#define _SPBRGH_BRG13_MASK                                      0x20
#define _SPBRGH_BRG14_POSN                                      0x6
#define _SPBRGH_BRG14_POSITION                                  0x6
#define _SPBRGH_BRG14_SIZE                                      0x1
#define _SPBRGH_BRG14_LENGTH                                    0x1
#define _SPBRGH_BRG14_MASK                                      0x40
#define _SPBRGH_BRG15_POSN                                      0x7
#define _SPBRGH_BRG15_POSITION                                  0x7
#define _SPBRGH_BRG15_SIZE                                      0x1
#define _SPBRGH_BRG15_LENGTH                                    0x1
#define _SPBRGH_BRG15_MASK                                      0x80

// Register: PWM1CON
extern volatile unsigned char           PWM1CON             @ 0x09B;
#ifndef _LIB_BUILD
asm("PWM1CON equ 09Bh");
#endif
// bitfield definitions
typedef union {
    struct {
```

```
        unsigned PDC                    :7;
        unsigned PRSEN                  :1;
    };
    struct {
        unsigned PDC0                   :1;
        unsigned PDC1                   :1;
        unsigned PDC2                   :1;
        unsigned PDC3                   :1;
        unsigned PDC4                   :1;
        unsigned PDC5                   :1;
        unsigned PDC6                   :1;
    };
} PWM1CONbits_t;
extern volatile PWM1CONbits_t PWM1CONbits @ 0x09B;
// bitfield macros
#define _PWM1CON_PDC_POSN                                       0x0
#define _PWM1CON_PDC_POSITION                                   0x0
#define _PWM1CON_PDC_SIZE                                       0x7
#define _PWM1CON_PDC_LENGTH                                     0x7
#define _PWM1CON_PDC_MASK                                       0x7F
#define _PWM1CON_PRSEN_POSN                                     0x7
#define _PWM1CON_PRSEN_POSITION                                 0x7
#define _PWM1CON_PRSEN_SIZE                                     0x1
#define _PWM1CON_PRSEN_LENGTH                                   0x1
#define _PWM1CON_PRSEN_MASK                                     0x80
#define _PWM1CON_PDC0_POSN                                      0x0
#define _PWM1CON_PDC0_POSITION                                  0x0
#define _PWM1CON_PDC0_SIZE                                      0x1
#define _PWM1CON_PDC0_LENGTH                                    0x1
#define _PWM1CON_PDC0_MASK                                      0x1
#define _PWM1CON_PDC1_POSN                                      0x1
#define _PWM1CON_PDC1_POSITION                                  0x1
#define _PWM1CON_PDC1_SIZE                                      0x1
#define _PWM1CON_PDC1_LENGTH                                    0x1
#define _PWM1CON_PDC1_MASK                                      0x2
#define _PWM1CON_PDC2_POSN                                      0x2
#define _PWM1CON_PDC2_POSITION                                  0x2
#define _PWM1CON_PDC2_SIZE                                      0x1
#define _PWM1CON_PDC2_LENGTH                                    0x1
#define _PWM1CON_PDC2_MASK                                      0x4
#define _PWM1CON_PDC3_POSN                                      0x3
#define _PWM1CON_PDC3_POSITION                                  0x3
#define _PWM1CON_PDC3_SIZE                                      0x1
#define _PWM1CON_PDC3_LENGTH                                    0x1
#define _PWM1CON_PDC3_MASK                                      0x8
#define _PWM1CON_PDC4_POSN                                      0x4
#define _PWM1CON_PDC4_POSITION                                  0x4
#define _PWM1CON_PDC4_SIZE                                      0x1
#define _PWM1CON_PDC4_LENGTH                                    0x1
#define _PWM1CON_PDC4_MASK                                      0x10
#define _PWM1CON_PDC5_POSN                                      0x5
#define _PWM1CON_PDC5_POSITION                                  0x5
#define _PWM1CON_PDC5_SIZE                                      0x1
#define _PWM1CON_PDC5_LENGTH                                    0x1
#define _PWM1CON_PDC5_MASK                                      0x20
#define _PWM1CON_PDC6_POSN                                      0x6
#define _PWM1CON_PDC6_POSITION                                  0x6
#define _PWM1CON_PDC6_SIZE                                      0x1
#define _PWM1CON_PDC6_LENGTH                                    0x1
#define _PWM1CON_PDC6_MASK                                      0x40
```

```
// Register: ECCPAS
extern volatile unsigned char           ECCPAS              @ 0x09C;
#ifndef _LIB_BUILD
asm("ECCPAS equ 09Ch");
#endif
// bitfield definitions
typedef union {
    struct {
        unsigned PSSBD                  :2;
        unsigned PSSAC                  :2;
        unsigned ECCPAS                 :3;
        unsigned ECCPASE                :1;
    };
    struct {
        unsigned PSSBD0                 :1;
        unsigned PSSBD1                 :1;
        unsigned PSSAC0                 :1;
        unsigned PSSAC1                 :1;
        unsigned ECCPAS0                :1;
        unsigned ECCPAS1                :1;
        unsigned ECCPAS2                :1;
    };
} ECCPASbits_t;
extern volatile ECCPASbits_t ECCPASbits @ 0x09C;
// bitfield macros
#define _ECCPAS_PSSBD_POSN                                  0x0
#define _ECCPAS_PSSBD_POSITION                              0x0
#define _ECCPAS_PSSBD_SIZE                                  0x2
#define _ECCPAS_PSSBD_LENGTH                                0x2
#define _ECCPAS_PSSBD_MASK                                  0x3
#define _ECCPAS_PSSAC_POSN                                  0x2
#define _ECCPAS_PSSAC_POSITION                              0x2
#define _ECCPAS_PSSAC_SIZE                                  0x2
#define _ECCPAS_PSSAC_LENGTH                                0x2
#define _ECCPAS_PSSAC_MASK                                  0xC
#define _ECCPAS_ECCPAS_POSN                                 0x4
#define _ECCPAS_ECCPAS_POSITION                             0x4
#define _ECCPAS_ECCPAS_SIZE                                 0x3
#define _ECCPAS_ECCPAS_LENGTH                               0x3
#define _ECCPAS_ECCPAS_MASK                                 0x70
#define _ECCPAS_ECCPASE_POSN                                0x7
#define _ECCPAS_ECCPASE_POSITION                            0x7
#define _ECCPAS_ECCPASE_SIZE                                0x1
#define _ECCPAS_ECCPASE_LENGTH                              0x1
#define _ECCPAS_ECCPASE_MASK                                0x80
#define _ECCPAS_PSSBD0_POSN                                 0x0
#define _ECCPAS_PSSBD0_POSITION                             0x0
#define _ECCPAS_PSSBD0_SIZE                                 0x1
#define _ECCPAS_PSSBD0_LENGTH                               0x1
#define _ECCPAS_PSSBD0_MASK                                 0x1
#define _ECCPAS_PSSBD1_POSN                                 0x1
#define _ECCPAS_PSSBD1_POSITION                             0x1
#define _ECCPAS_PSSBD1_SIZE                                 0x1
#define _ECCPAS_PSSBD1_LENGTH                               0x1
#define _ECCPAS_PSSBD1_MASK                                 0x2
#define _ECCPAS_PSSAC0_POSN                                 0x2
#define _ECCPAS_PSSAC0_POSITION                             0x2
#define _ECCPAS_PSSAC0_SIZE                                 0x1
#define _ECCPAS_PSSAC0_LENGTH                               0x1
```

```
#define _ECCPAS_PSSAC0_MASK                             0x4
#define _ECCPAS_PSSAC1_POSN                             0x3
#define _ECCPAS_PSSAC1_POSITION                         0x3
#define _ECCPAS_PSSAC1_SIZE                             0x1
#define _ECCPAS_PSSAC1_LENGTH                           0x1
#define _ECCPAS_PSSAC1_MASK                             0x8
#define _ECCPAS_ECCPAS0_POSN                            0x4
#define _ECCPAS_ECCPAS0_POSITION                        0x4
#define _ECCPAS_ECCPAS0_SIZE                            0x1
#define _ECCPAS_ECCPAS0_LENGTH                          0x1
#define _ECCPAS_ECCPAS0_MASK                            0x10
#define _ECCPAS_ECCPAS1_POSN                            0x5
#define _ECCPAS_ECCPAS1_POSITION                        0x5
#define _ECCPAS_ECCPAS1_SIZE                            0x1
#define _ECCPAS_ECCPAS1_LENGTH                          0x1
#define _ECCPAS_ECCPAS1_MASK                            0x20
#define _ECCPAS_ECCPAS2_POSN                            0x6
#define _ECCPAS_ECCPAS2_POSITION                        0x6
#define _ECCPAS_ECCPAS2_SIZE                            0x1
#define _ECCPAS_ECCPAS2_LENGTH                          0x1
#define _ECCPAS_ECCPAS2_MASK                            0x40

// Register: PSTRCON
extern volatile unsigned char           PSTRCON             @ 0x09D;
#ifndef _LIB_BUILD
asm("PSTRCON equ 09Dh");
#endif
// bitfield definitions
typedef union {
    struct {
        unsigned STRA                   :1;
        unsigned STRB                   :1;
        unsigned STRC                   :1;
        unsigned STRD                   :1;
        unsigned STRSYNC                :1;
    };
} PSTRCONbits_t;
extern volatile PSTRCONbits_t PSTRCONbits @ 0x09D;
// bitfield macros
#define _PSTRCON_STRA_POSN                              0x0
#define _PSTRCON_STRA_POSITION                          0x0
#define _PSTRCON_STRA_SIZE                              0x1
#define _PSTRCON_STRA_LENGTH                            0x1
#define _PSTRCON_STRA_MASK                              0x1
#define _PSTRCON_STRB_POSN                              0x1
#define _PSTRCON_STRB_POSITION                          0x1
#define _PSTRCON_STRB_SIZE                              0x1
#define _PSTRCON_STRB_LENGTH                            0x1
#define _PSTRCON_STRB_MASK                              0x2
#define _PSTRCON_STRC_POSN                              0x2
#define _PSTRCON_STRC_POSITION                          0x2
#define _PSTRCON_STRC_SIZE                              0x1
#define _PSTRCON_STRC_LENGTH                            0x1
#define _PSTRCON_STRC_MASK                              0x4
#define _PSTRCON_STRD_POSN                              0x3
#define _PSTRCON_STRD_POSITION                          0x3
#define _PSTRCON_STRD_SIZE                              0x1
#define _PSTRCON_STRD_LENGTH                            0x1
#define _PSTRCON_STRD_MASK                              0x8
#define _PSTRCON_STRSYNC_POSN                           0x4
```

```
#define _PSTRCON_STRSYNC_POSITION                       0x4
#define _PSTRCON_STRSYNC_SIZE                           0x1
#define _PSTRCON_STRSYNC_LENGTH                         0x1
#define _PSTRCON_STRSYNC_MASK                           0x10

// Register: ADRESL
extern volatile unsigned char           ADRESL              @ 0x09E;
#ifndef _LIB_BUILD
asm("ADRESL equ 09Eh");
#endif

// Register: ADCON1
extern volatile unsigned char           ADCON1              @ 0x09F;
#ifndef _LIB_BUILD
asm("ADCON1 equ 09Fh");
#endif
// bitfield definitions
typedef union {
    struct {
        unsigned                        :4;
        unsigned VCFG0                  :1;
        unsigned VCFG1                  :1;
        unsigned                        :1;
        unsigned ADFM                   :1;
    };
} ADCON1bits_t;
extern volatile ADCON1bits_t ADCON1bits @ 0x09F;
// bitfield macros
#define _ADCON1_VCFG0_POSN                              0x4
#define _ADCON1_VCFG0_POSITION                          0x4
#define _ADCON1_VCFG0_SIZE                              0x1
#define _ADCON1_VCFG0_LENGTH                            0x1
#define _ADCON1_VCFG0_MASK                              0x10
#define _ADCON1_VCFG1_POSN                              0x5
#define _ADCON1_VCFG1_POSITION                          0x5
#define _ADCON1_VCFG1_SIZE                              0x1
#define _ADCON1_VCFG1_LENGTH                            0x1
#define _ADCON1_VCFG1_MASK                              0x20
#define _ADCON1_ADFM_POSN                               0x7
#define _ADCON1_ADFM_POSITION                           0x7
#define _ADCON1_ADFM_SIZE                               0x1
#define _ADCON1_ADFM_LENGTH                             0x1
#define _ADCON1_ADFM_MASK                               0x80

// Register: WDTCON
extern volatile unsigned char           WDTCON              @ 0x105;
#ifndef _LIB_BUILD
asm("WDTCON equ 0105h");
#endif
// bitfield definitions
typedef union {
    struct {
        unsigned SWDTEN                 :1;
        unsigned WDTPS                  :4;
    };
    struct {
        unsigned                        :1;
        unsigned WDTPS0                 :1;
        unsigned WDTPS1                 :1;
        unsigned WDTPS2                 :1;
```

```
        unsigned WDTPS3                 :1;
    };
} WDTCONbits_t;
extern volatile WDTCONbits_t WDTCONbits @ 0x105;
// bitfield macros
#define _WDTCON_SWDTEN_POSN                                     0x0
#define _WDTCON_SWDTEN_POSITION                                 0x0
#define _WDTCON_SWDTEN_SIZE                                     0x1
#define _WDTCON_SWDTEN_LENGTH                                   0x1
#define _WDTCON_SWDTEN_MASK                                     0x1
#define _WDTCON_WDTPS_POSN                                      0x1
#define _WDTCON_WDTPS_POSITION                                  0x1
#define _WDTCON_WDTPS_SIZE                                      0x4
#define _WDTCON_WDTPS_LENGTH                                    0x4
#define _WDTCON_WDTPS_MASK                                      0x1E
#define _WDTCON_WDTPS0_POSN                                     0x1
#define _WDTCON_WDTPS0_POSITION                                 0x1
#define _WDTCON_WDTPS0_SIZE                                     0x1
#define _WDTCON_WDTPS0_LENGTH                                   0x1
#define _WDTCON_WDTPS0_MASK                                     0x2
#define _WDTCON_WDTPS1_POSN                                     0x2
#define _WDTCON_WDTPS1_POSITION                                 0x2
#define _WDTCON_WDTPS1_SIZE                                     0x1
#define _WDTCON_WDTPS1_LENGTH                                   0x1
#define _WDTCON_WDTPS1_MASK                                     0x4
#define _WDTCON_WDTPS2_POSN                                     0x3
#define _WDTCON_WDTPS2_POSITION                                 0x3
#define _WDTCON_WDTPS2_SIZE                                     0x1
#define _WDTCON_WDTPS2_LENGTH                                   0x1
#define _WDTCON_WDTPS2_MASK                                     0x8
#define _WDTCON_WDTPS3_POSN                                     0x4
#define _WDTCON_WDTPS3_POSITION                                 0x4
#define _WDTCON_WDTPS3_SIZE                                     0x1
#define _WDTCON_WDTPS3_LENGTH                                   0x1
#define _WDTCON_WDTPS3_MASK                                     0x10

// Register: CM1CON0
extern volatile unsigned char           CM1CON0             @ 0x107;
#ifndef _LIB_BUILD
asm("CM1CON0 equ 0107h");
#endif
// bitfield definitions
typedef union {
    struct {
        unsigned C1CH                   :2;
        unsigned C1R                    :1;
        unsigned                        :1;
        unsigned C1POL                  :1;
        unsigned C1OE                   :1;
        unsigned C1OUT                  :1;
        unsigned C1ON                   :1;
    };
    struct {
        unsigned C1CH0                  :1;
        unsigned C1CH1                  :1;
    };
} CM1CON0bits_t;
extern volatile CM1CON0bits_t CM1CON0bits @ 0x107;
// bitfield macros
#define _CM1CON0_C1CH_POSN                                      0x0
```

```
#define _CM1CON0_C1CH_POSITION                          0x0
#define _CM1CON0_C1CH_SIZE                              0x2
#define _CM1CON0_C1CH_LENGTH                            0x2
#define _CM1CON0_C1CH_MASK                              0x3
#define _CM1CON0_C1R_POSN                               0x2
#define _CM1CON0_C1R_POSITION                           0x2
#define _CM1CON0_C1R_SIZE                               0x1
#define _CM1CON0_C1R_LENGTH                             0x1
#define _CM1CON0_C1R_MASK                               0x4
#define _CM1CON0_C1POL_POSN                             0x4
#define _CM1CON0_C1POL_POSITION                         0x4
#define _CM1CON0_C1POL_SIZE                             0x1
#define _CM1CON0_C1POL_LENGTH                           0x1
#define _CM1CON0_C1POL_MASK                             0x10
#define _CM1CON0_C1OE_POSN                              0x5
#define _CM1CON0_C1OE_POSITION                          0x5
#define _CM1CON0_C1OE_SIZE                              0x1
#define _CM1CON0_C1OE_LENGTH                            0x1
#define _CM1CON0_C1OE_MASK                              0x20
#define _CM1CON0_C1OUT_POSN                             0x6
#define _CM1CON0_C1OUT_POSITION                         0x6
#define _CM1CON0_C1OUT_SIZE                             0x1
#define _CM1CON0_C1OUT_LENGTH                           0x1
#define _CM1CON0_C1OUT_MASK                             0x40
#define _CM1CON0_C1ON_POSN                              0x7
#define _CM1CON0_C1ON_POSITION                          0x7
#define _CM1CON0_C1ON_SIZE                              0x1
#define _CM1CON0_C1ON_LENGTH                            0x1
#define _CM1CON0_C1ON_MASK                              0x80
#define _CM1CON0_C1CH0_POSN                             0x0
#define _CM1CON0_C1CH0_POSITION                         0x0
#define _CM1CON0_C1CH0_SIZE                             0x1
#define _CM1CON0_C1CH0_LENGTH                           0x1
#define _CM1CON0_C1CH0_MASK                             0x1
#define _CM1CON0_C1CH1_POSN                             0x1
#define _CM1CON0_C1CH1_POSITION                         0x1
#define _CM1CON0_C1CH1_SIZE                             0x1
#define _CM1CON0_C1CH1_LENGTH                           0x1
#define _CM1CON0_C1CH1_MASK                             0x2

// Register: CM2CON0
extern volatile unsigned char           CM2CON0             @ 0x108;
#ifndef _LIB_BUILD
asm("CM2CON0 equ 0108h");
#endif
// bitfield definitions
typedef union {
    struct {
        unsigned C2CH                   :2;
        unsigned C2R                    :1;
        unsigned                        :1;
        unsigned C2POL                  :1;
        unsigned C2OE                   :1;
        unsigned C2OUT                  :1;
        unsigned C2ON                   :1;
    };
    struct {
        unsigned C2CH0                  :1;
        unsigned C2CH1                  :1;
    };
```

```
} CM2CON0bits_t;
extern volatile CM2CON0bits_t CM2CON0bits @ 0x108;
// bitfield macros
#define _CM2CON0_C2CH_POSN                      0x0
#define _CM2CON0_C2CH_POSITION                  0x0
#define _CM2CON0_C2CH_SIZE                      0x2
#define _CM2CON0_C2CH_LENGTH                    0x2
#define _CM2CON0_C2CH_MASK                      0x3
#define _CM2CON0_C2R_POSN                       0x2
#define _CM2CON0_C2R_POSITION                   0x2
#define _CM2CON0_C2R_SIZE                       0x1
#define _CM2CON0_C2R_LENGTH                     0x1
#define _CM2CON0_C2R_MASK                       0x4
#define _CM2CON0_C2POL_POSN                     0x4
#define _CM2CON0_C2POL_POSITION                 0x4
#define _CM2CON0_C2POL_SIZE                     0x1
#define _CM2CON0_C2POL_LENGTH                   0x1
#define _CM2CON0_C2POL_MASK                     0x10
#define _CM2CON0_C2OE_POSN                      0x5
#define _CM2CON0_C2OE_POSITION                  0x5
#define _CM2CON0_C2OE_SIZE                      0x1
#define _CM2CON0_C2OE_LENGTH                    0x1
#define _CM2CON0_C2OE_MASK                      0x20
#define _CM2CON0_C2OUT_POSN                     0x6
#define _CM2CON0_C2OUT_POSITION                 0x6
#define _CM2CON0_C2OUT_SIZE                     0x1
#define _CM2CON0_C2OUT_LENGTH                   0x1
#define _CM2CON0_C2OUT_MASK                     0x40
#define _CM2CON0_C2ON_POSN                      0x7
#define _CM2CON0_C2ON_POSITION                  0x7
#define _CM2CON0_C2ON_SIZE                      0x1
#define _CM2CON0_C2ON_LENGTH                    0x1
#define _CM2CON0_C2ON_MASK                      0x80
#define _CM2CON0_C2CH0_POSN                     0x0
#define _CM2CON0_C2CH0_POSITION                 0x0
#define _CM2CON0_C2CH0_SIZE                     0x1
#define _CM2CON0_C2CH0_LENGTH                   0x1
#define _CM2CON0_C2CH0_MASK                     0x1
#define _CM2CON0_C2CH1_POSN                     0x1
#define _CM2CON0_C2CH1_POSITION                 0x1
#define _CM2CON0_C2CH1_SIZE                     0x1
#define _CM2CON0_C2CH1_LENGTH                   0x1
#define _CM2CON0_C2CH1_MASK                     0x2

// Register: CM2CON1
extern volatile unsigned char           CM2CON1             @ 0x109;
#ifndef _LIB_BUILD
asm("CM2CON1 equ 0109h");
#endif
// bitfield definitions
typedef union {
    struct {
        unsigned C2SYNC                 :1;
        unsigned T1GSS                  :1;
        unsigned                        :2;
        unsigned C2RSEL                 :1;
        unsigned C1RSEL                 :1;
        unsigned MC2OUT                 :1;
        unsigned MC1OUT                 :1;
    };
```

```
} CM2CON1bits_t;
extern volatile CM2CON1bits_t CM2CON1bits @ 0x109;
// bitfield macros
#define _CM2CON1_C2SYNC_POSN                    0x0
#define _CM2CON1_C2SYNC_POSITION                0x0
#define _CM2CON1_C2SYNC_SIZE                    0x1
#define _CM2CON1_C2SYNC_LENGTH                  0x1
#define _CM2CON1_C2SYNC_MASK                    0x1
#define _CM2CON1_T1GSS_POSN                     0x1
#define _CM2CON1_T1GSS_POSITION                 0x1
#define _CM2CON1_T1GSS_SIZE                     0x1
#define _CM2CON1_T1GSS_LENGTH                   0x1
#define _CM2CON1_T1GSS_MASK                     0x2
#define _CM2CON1_C2RSEL_POSN                    0x4
#define _CM2CON1_C2RSEL_POSITION                0x4
#define _CM2CON1_C2RSEL_SIZE                    0x1
#define _CM2CON1_C2RSEL_LENGTH                  0x1
#define _CM2CON1_C2RSEL_MASK                    0x10
#define _CM2CON1_C1RSEL_POSN                    0x5
#define _CM2CON1_C1RSEL_POSITION                0x5
#define _CM2CON1_C1RSEL_SIZE                    0x1
#define _CM2CON1_C1RSEL_LENGTH                  0x1
#define _CM2CON1_C1RSEL_MASK                    0x20
#define _CM2CON1_MC2OUT_POSN                    0x6
#define _CM2CON1_MC2OUT_POSITION                0x6
#define _CM2CON1_MC2OUT_SIZE                    0x1
#define _CM2CON1_MC2OUT_LENGTH                  0x1
#define _CM2CON1_MC2OUT_MASK                    0x40
#define _CM2CON1_MC1OUT_POSN                    0x7
#define _CM2CON1_MC1OUT_POSITION                0x7
#define _CM2CON1_MC1OUT_SIZE                    0x1
#define _CM2CON1_MC1OUT_LENGTH                  0x1
#define _CM2CON1_MC1OUT_MASK                    0x80

// Register: EEDATA
extern volatile unsigned char           EEDATA              @ 0x10C;
#ifndef _LIB_BUILD
asm("EEDATA equ 010Ch");
#endif
// aliases
extern volatile unsigned char           EEDAT               @ 0x10C;
#ifndef _LIB_BUILD
asm("EEDAT equ 010Ch");
#endif

// Register: EEADR
extern volatile unsigned char           EEADR               @ 0x10D;
#ifndef _LIB_BUILD
asm("EEADR equ 010Dh");
#endif

// Register: EEDATH
extern volatile unsigned char           EEDATH              @ 0x10E;
#ifndef _LIB_BUILD
asm("EEDATH equ 010Eh");
#endif

// Register: EEADRH
extern volatile unsigned char           EEADRH              @ 0x10F;
#ifndef _LIB_BUILD
```

```
asm("EEADRH equ 010Fh");
#endif

// Register: SRCON
extern volatile unsigned char           SRCON               @ 0x185;
#ifndef _LIB_BUILD
asm("SRCON equ 0185h");
#endif
// bitfield definitions
typedef union {
    struct {
        unsigned FVREN                  :1;
        unsigned                        :1;
        unsigned PULSR                  :1;
        unsigned PULSS                  :1;
        unsigned C2REN                  :1;
        unsigned C1SEN                  :1;
        unsigned SR0                    :1;
        unsigned SR1                    :1;
    };
} SRCONbits_t;
extern volatile SRCONbits_t SRCONbits @ 0x185;
// bitfield macros
#define _SRCON_FVREN_POSN                                       0x0
#define _SRCON_FVREN_POSITION                                   0x0
#define _SRCON_FVREN_SIZE                                       0x1
#define _SRCON_FVREN_LENGTH                                     0x1
#define _SRCON_FVREN_MASK                                       0x1
#define _SRCON_PULSR_POSN                                       0x2
#define _SRCON_PULSR_POSITION                                   0x2
#define _SRCON_PULSR_SIZE                                       0x1
#define _SRCON_PULSR_LENGTH                                     0x1
#define _SRCON_PULSR_MASK                                       0x4
#define _SRCON_PULSS_POSN                                       0x3
#define _SRCON_PULSS_POSITION                                   0x3
#define _SRCON_PULSS_SIZE                                       0x1
#define _SRCON_PULSS_LENGTH                                     0x1
#define _SRCON_PULSS_MASK                                       0x8
#define _SRCON_C2REN_POSN                                       0x4
#define _SRCON_C2REN_POSITION                                   0x4
#define _SRCON_C2REN_SIZE                                       0x1
#define _SRCON_C2REN_LENGTH                                     0x1
#define _SRCON_C2REN_MASK                                       0x10
#define _SRCON_C1SEN_POSN                                       0x5
#define _SRCON_C1SEN_POSITION                                   0x5
#define _SRCON_C1SEN_SIZE                                       0x1
#define _SRCON_C1SEN_LENGTH                                     0x1
#define _SRCON_C1SEN_MASK                                       0x20
#define _SRCON_SR0_POSN                                         0x6
#define _SRCON_SR0_POSITION                                     0x6
#define _SRCON_SR0_SIZE                                         0x1
#define _SRCON_SR0_LENGTH                                       0x1
#define _SRCON_SR0_MASK                                         0x40
#define _SRCON_SR1_POSN                                         0x7
#define _SRCON_SR1_POSITION                                     0x7
#define _SRCON_SR1_SIZE                                         0x1
#define _SRCON_SR1_LENGTH                                       0x1
#define _SRCON_SR1_MASK                                         0x80

// Register: BAUDCTL
```

```
extern volatile unsigned char           BAUDCTL             @ 0x187;
#ifndef _LIB_BUILD
asm("BAUDCTL equ 0187h");
#endif
// bitfield definitions
typedef union {
    struct {
        unsigned ABDEN                  :1;
        unsigned WUE                    :1;
        unsigned                        :1;
        unsigned BRG16                  :1;
        unsigned SCKP                   :1;
        unsigned                        :1;
        unsigned RCIDL                  :1;
        unsigned ABDOVF                 :1;
    };
} BAUDCTLbits_t;
extern volatile BAUDCTLbits_t BAUDCTLbits @ 0x187;
// bitfield macros
#define _BAUDCTL_ABDEN_POSN                                     0x0
#define _BAUDCTL_ABDEN_POSITION                                 0x0
#define _BAUDCTL_ABDEN_SIZE                                     0x1
#define _BAUDCTL_ABDEN_LENGTH                                   0x1
#define _BAUDCTL_ABDEN_MASK                                     0x1
#define _BAUDCTL_WUE_POSN                                       0x1
#define _BAUDCTL_WUE_POSITION                                   0x1
#define _BAUDCTL_WUE_SIZE                                       0x1
#define _BAUDCTL_WUE_LENGTH                                     0x1
#define _BAUDCTL_WUE_MASK                                       0x2
#define _BAUDCTL_BRG16_POSN                                     0x3
#define _BAUDCTL_BRG16_POSITION                                 0x3
#define _BAUDCTL_BRG16_SIZE                                     0x1
#define _BAUDCTL_BRG16_LENGTH                                   0x1
#define _BAUDCTL_BRG16_MASK                                     0x8
#define _BAUDCTL_SCKP_POSN                                      0x4
#define _BAUDCTL_SCKP_POSITION                                  0x4
#define _BAUDCTL_SCKP_SIZE                                      0x1
#define _BAUDCTL_SCKP_LENGTH                                    0x1
#define _BAUDCTL_SCKP_MASK                                      0x10
#define _BAUDCTL_RCIDL_POSN                                     0x6
#define _BAUDCTL_RCIDL_POSITION                                 0x6
#define _BAUDCTL_RCIDL_SIZE                                     0x1
#define _BAUDCTL_RCIDL_LENGTH                                   0x1
#define _BAUDCTL_RCIDL_MASK                                     0x40
#define _BAUDCTL_ABDOVF_POSN                                    0x7
#define _BAUDCTL_ABDOVF_POSITION                                0x7
#define _BAUDCTL_ABDOVF_SIZE                                    0x1
#define _BAUDCTL_ABDOVF_LENGTH                                  0x1
#define _BAUDCTL_ABDOVF_MASK                                    0x80

// Register: ANSEL
extern volatile unsigned char           ANSEL               @ 0x188;
#ifndef _LIB_BUILD
asm("ANSEL equ 0188h");
#endif
// bitfield definitions
typedef union {
    struct {
        unsigned ANS0                   :1;
        unsigned ANS1                   :1;
```

```
        unsigned ANS2                   :1;
        unsigned ANS3                   :1;
        unsigned ANS4                   :1;
    };
} ANSELbits_t;
extern volatile ANSELbits_t ANSELbits @ 0x188;
// bitfield macros
#define _ANSEL_ANS0_POSN                                        0x0
#define _ANSEL_ANS0_POSITION                                    0x0
#define _ANSEL_ANS0_SIZE                                        0x1
#define _ANSEL_ANS0_LENGTH                                      0x1
#define _ANSEL_ANS0_MASK                                        0x1
#define _ANSEL_ANS1_POSN                                        0x1
#define _ANSEL_ANS1_POSITION                                    0x1
#define _ANSEL_ANS1_SIZE                                        0x1
#define _ANSEL_ANS1_LENGTH                                      0x1
#define _ANSEL_ANS1_MASK                                        0x2
#define _ANSEL_ANS2_POSN                                        0x2
#define _ANSEL_ANS2_POSITION                                    0x2
#define _ANSEL_ANS2_SIZE                                        0x1
#define _ANSEL_ANS2_LENGTH                                      0x1
#define _ANSEL_ANS2_MASK                                        0x4
#define _ANSEL_ANS3_POSN                                        0x3
#define _ANSEL_ANS3_POSITION                                    0x3
#define _ANSEL_ANS3_SIZE                                        0x1
#define _ANSEL_ANS3_LENGTH                                      0x1
#define _ANSEL_ANS3_MASK                                        0x8
#define _ANSEL_ANS4_POSN                                        0x4
#define _ANSEL_ANS4_POSITION                                    0x4
#define _ANSEL_ANS4_SIZE                                        0x1
#define _ANSEL_ANS4_LENGTH                                      0x1
#define _ANSEL_ANS4_MASK                                        0x10

// Register: ANSELH
extern volatile unsigned char           ANSELH              @ 0x189;
#ifndef _LIB_BUILD
asm("ANSELH equ 0189h");
#endif
// bitfield definitions
typedef union {
    struct {
        unsigned ANS8                   :1;
        unsigned ANS9                   :1;
        unsigned ANS10                  :1;
        unsigned ANS11                  :1;
        unsigned ANS12                  :1;
        unsigned ANS13                  :1;
    };
} ANSELHbits_t;
extern volatile ANSELHbits_t ANSELHbits @ 0x189;
// bitfield macros
#define _ANSELH_ANS8_POSN                                       0x0
#define _ANSELH_ANS8_POSITION                                   0x0
#define _ANSELH_ANS8_SIZE                                       0x1
#define _ANSELH_ANS8_LENGTH                                     0x1
#define _ANSELH_ANS8_MASK                                       0x1
#define _ANSELH_ANS9_POSN                                       0x1
#define _ANSELH_ANS9_POSITION                                   0x1
#define _ANSELH_ANS9_SIZE                                       0x1
#define _ANSELH_ANS9_LENGTH                                     0x1
```

```
#define _ANSELH_ANS9_MASK                                       0x2
#define _ANSELH_ANS10_POSN                                      0x2
#define _ANSELH_ANS10_POSITION                                  0x2
#define _ANSELH_ANS10_SIZE                                      0x1
#define _ANSELH_ANS10_LENGTH                                    0x1
#define _ANSELH_ANS10_MASK                                      0x4
#define _ANSELH_ANS11_POSN                                      0x3
#define _ANSELH_ANS11_POSITION                                  0x3
#define _ANSELH_ANS11_SIZE                                      0x1
#define _ANSELH_ANS11_LENGTH                                    0x1
#define _ANSELH_ANS11_MASK                                      0x8
#define _ANSELH_ANS12_POSN                                      0x4
#define _ANSELH_ANS12_POSITION                                  0x4
#define _ANSELH_ANS12_SIZE                                      0x1
#define _ANSELH_ANS12_LENGTH                                    0x1
#define _ANSELH_ANS12_MASK                                      0x10
#define _ANSELH_ANS13_POSN                                      0x5
#define _ANSELH_ANS13_POSITION                                  0x5
#define _ANSELH_ANS13_SIZE                                      0x1
#define _ANSELH_ANS13_LENGTH                                    0x1
#define _ANSELH_ANS13_MASK                                      0x20

// Register: EECON1
extern volatile unsigned char           EECON1              @ 0x18C;
#ifndef _LIB_BUILD
asm("EECON1 equ 018Ch");
#endif
// bitfield definitions
typedef union {
    struct {
        unsigned RD                     :1;
        unsigned WR                     :1;
        unsigned WREN                   :1;
        unsigned WRERR                  :1;
        unsigned                        :3;
        unsigned EEPGD                  :1;
    };
} EECON1bits_t;
extern volatile EECON1bits_t EECON1bits @ 0x18C;
// bitfield macros
#define _EECON1_RD_POSN                                         0x0
#define _EECON1_RD_POSITION                                     0x0
#define _EECON1_RD_SIZE                                         0x1
#define _EECON1_RD_LENGTH                                       0x1
#define _EECON1_RD_MASK                                         0x1
#define _EECON1_WR_POSN                                         0x1
#define _EECON1_WR_POSITION                                     0x1
#define _EECON1_WR_SIZE                                         0x1
#define _EECON1_WR_LENGTH                                       0x1
#define _EECON1_WR_MASK                                         0x2
#define _EECON1_WREN_POSN                                       0x2
#define _EECON1_WREN_POSITION                                   0x2
#define _EECON1_WREN_SIZE                                       0x1
#define _EECON1_WREN_LENGTH                                     0x1
#define _EECON1_WREN_MASK                                       0x4
#define _EECON1_WRERR_POSN                                      0x3
#define _EECON1_WRERR_POSITION                                  0x3
#define _EECON1_WRERR_SIZE                                      0x1
#define _EECON1_WRERR_LENGTH                                    0x1
#define _EECON1_WRERR_MASK                                      0x8
```

```
#define _EECON1_EEPGD_POSN                              0x7
#define _EECON1_EEPGD_POSITION                          0x7
#define _EECON1_EEPGD_SIZE                              0x1
#define _EECON1_EEPGD_LENGTH                            0x1
#define _EECON1_EEPGD_MASK                              0x80

// Register: EECON2
extern volatile unsigned char           EECON2          @ 0x18D;
#ifndef _LIB_BUILD
asm("EECON2 equ 018Dh");
#endif

/*
 * Bit Definitions
 */
#define _DEPRECATED __attribute__((__deprecated__))
#ifndef BANKMASK
#define BANKMASK(addr) ((addr)&07Fh)
#endif
extern volatile __bit                   ABDEN           @ (((unsigned) &
    BAUDCTL)*8) + 0;
#define                                 ABDEN_bit       BANKMASK(BAUDCTL),
    0
extern volatile __bit                   ABDOVF          @ (((unsigned) &
    BAUDCTL)*8) + 7;
#define                                 ABDOVF_bit      BANKMASK(BAUDCTL),
    7
extern volatile __bit                   ACKDT           @ (((unsigned) &
    SSPCON2)*8) + 5;
#define                                 ACKDT_bit       BANKMASK(SSPCON2),
    5
extern volatile __bit                   ACKEN           @ (((unsigned) &
    SSPCON2)*8) + 4;
#define                                 ACKEN_bit       BANKMASK(SSPCON2),
    4
extern volatile __bit                   ACKSTAT         @ (((unsigned) &
    SSPCON2)*8) + 6;
#define                                 ACKSTAT_bit     BANKMASK(SSPCON2),
    6
extern volatile __bit                   ADCS0           @ (((unsigned) &
    ADCON0)*8) + 6;
#define                                 ADCS0_bit       BANKMASK(ADCON0),
    6
extern volatile __bit                   ADCS1           @ (((unsigned) &
    ADCON0)*8) + 7;
#define                                 ADCS1_bit       BANKMASK(ADCON0),
    7
extern volatile __bit                   ADDEN           @ (((unsigned) &
    RCSTA)*8) + 3;
#define                                 ADDEN_bit       BANKMASK(RCSTA), 3
extern volatile __bit                   ADFM            @ (((unsigned) &
    ADCON1)*8) + 7;
#define                                 ADFM_bit        BANKMASK(ADCON1),
    7
extern volatile __bit                   ADIE            @ (((unsigned) &
    PIE1)*8) + 6;
#define                                 ADIE_bit        BANKMASK(PIE1), 6
extern volatile __bit                   ADIF            @ (((unsigned) &
    PIR1)*8) + 6;
#define                                 ADIF_bit        BANKMASK(PIR1), 6
```

```
extern volatile __bit ADON @ (((unsigned) &
    ADCON0)*8) + 0;
#define ADON_bit BANKMASK(ADCON0),
    0
extern volatile __bit ANS0 @ (((unsigned) &
    ANSEL)*8) + 0;
#define ANS0_bit BANKMASK(ANSEL), 0
extern volatile __bit ANS1 @ (((unsigned) &
    ANSEL)*8) + 1;
#define ANS1_bit BANKMASK(ANSEL), 1
extern volatile __bit ANS10 @ (((unsigned) &
    ANSELH)*8) + 2;
#define ANS10_bit BANKMASK(ANSELH),
    2
extern volatile __bit ANS11 @ (((unsigned) &
    ANSELH)*8) + 3;
#define ANS11_bit BANKMASK(ANSELH),
    3
extern volatile __bit ANS12 @ (((unsigned) &
    ANSELH)*8) + 4;
#define ANS12_bit BANKMASK(ANSELH),
    4
extern volatile __bit ANS13 @ (((unsigned) &
    ANSELH)*8) + 5;
#define ANS13_bit BANKMASK(ANSELH),
    5
extern volatile __bit ANS2 @ (((unsigned) &
    ANSEL)*8) + 2;
#define ANS2_bit BANKMASK(ANSEL), 2
extern volatile __bit ANS3 @ (((unsigned) &
    ANSEL)*8) + 3;
#define ANS3_bit BANKMASK(ANSEL), 3
extern volatile __bit ANS4 @ (((unsigned) &
    ANSEL)*8) + 4;
#define ANS4_bit BANKMASK(ANSEL), 4
extern volatile __bit ANS8 @ (((unsigned) &
    ANSELH)*8) + 0;
#define ANS8_bit BANKMASK(ANSELH),
    0
extern volatile __bit ANS9 @ (((unsigned) &
    ANSELH)*8) + 1;
#define ANS9_bit BANKMASK(ANSELH),
    1
extern volatile __bit BCLIE @ (((unsigned) &
    PIE2)*8) + 3;
#define BCLIE_bit BANKMASK(PIE2), 3
extern volatile __bit BCLIF @ (((unsigned) &
    PIR2)*8) + 3;
#define BCLIF_bit BANKMASK(PIR2), 3
extern volatile __bit BF @ (((unsigned) &
    SSPSTAT)*8) + 0;
#define BF_bit BANKMASK(SSPSTAT),
    0
extern volatile __bit BRG0 @ (((unsigned) &
    SPBRG)*8) + 0;
#define BRG0_bit BANKMASK(SPBRG), 0
extern volatile __bit BRG1 @ (((unsigned) &
    SPBRG)*8) + 1;
#define BRG1_bit BANKMASK(SPBRG), 1
extern volatile __bit BRG10 @ (((unsigned) &
```

```
    SPBRGH)*8) + 2;
#define                         BRG10_bit           BANKMASK(SPBRGH),
    2
extern volatile __bit           BRG11               @ (((unsigned) &
    SPBRGH)*8) + 3;
#define                         BRG11_bit           BANKMASK(SPBRGH),
    3
extern volatile __bit           BRG12               @ (((unsigned) &
    SPBRGH)*8) + 4;
#define                         BRG12_bit           BANKMASK(SPBRGH),
    4
extern volatile __bit           BRG13               @ (((unsigned) &
    SPBRGH)*8) + 5;
#define                         BRG13_bit           BANKMASK(SPBRGH),
    5
extern volatile __bit           BRG14               @ (((unsigned) &
    SPBRGH)*8) + 6;
#define                         BRG14_bit           BANKMASK(SPBRGH),
    6
extern volatile __bit           BRG15               @ (((unsigned) &
    SPBRGH)*8) + 7;
#define                         BRG15_bit           BANKMASK(SPBRGH),
    7
extern volatile __bit           BRG16               @ (((unsigned) &
    BAUDCTL)*8) + 3;
#define                         BRG16_bit           BANKMASK(BAUDCTL),
    3
extern volatile __bit           BRG2                @ (((unsigned) &
    SPBRG)*8) + 2;
#define                         BRG2_bit            BANKMASK(SPBRG), 2
extern volatile __bit           BRG3                @ (((unsigned) &
    SPBRG)*8) + 3;
#define                         BRG3_bit            BANKMASK(SPBRG), 3
extern volatile __bit           BRG4                @ (((unsigned) &
    SPBRG)*8) + 4;
#define                         BRG4_bit            BANKMASK(SPBRG), 4
extern volatile __bit           BRG5                @ (((unsigned) &
    SPBRG)*8) + 5;
#define                         BRG5_bit            BANKMASK(SPBRG), 5
extern volatile __bit           BRG6                @ (((unsigned) &
    SPBRG)*8) + 6;
#define                         BRG6_bit            BANKMASK(SPBRG), 6
extern volatile __bit           BRG7                @ (((unsigned) &
    SPBRG)*8) + 7;
#define                         BRG7_bit            BANKMASK(SPBRG), 7
extern volatile __bit           BRG8                @ (((unsigned) &
    SPBRGH)*8) + 0;
#define                         BRG8_bit            BANKMASK(SPBRGH),
    0
extern volatile __bit           BRG9                @ (((unsigned) &
    SPBRGH)*8) + 1;
#define                         BRG9_bit            BANKMASK(SPBRGH),
    1
extern volatile __bit           BRGH                @ (((unsigned) &
    TXSTA)*8) + 2;
#define                         BRGH_bit            BANKMASK(TXSTA), 2
extern volatile __bit           C1CH0               @ (((unsigned) &
    CM1CON0)*8) + 0;
#define                         C1CH0_bit           BANKMASK(CM1CON0),
    0
```

```
extern volatile __bit C1CH1 @ (((unsigned) &
    CM1CON0)*8) + 1;
#define C1CH1_bit BANKMASK(CM1CON0),
    1
extern volatile __bit C1IE @ (((unsigned) &
    PIE2)*8) + 5;
#define C1IE_bit BANKMASK(PIE2), 5
extern volatile __bit C1IF @ (((unsigned) &
    PIR2)*8) + 5;
#define C1IF_bit BANKMASK(PIR2), 5
extern volatile __bit C1OE @ (((unsigned) &
    CM1CON0)*8) + 5;
#define C1OE_bit BANKMASK(CM1CON0),
    5
extern volatile __bit C1ON @ (((unsigned) &
    CM1CON0)*8) + 7;
#define C1ON_bit BANKMASK(CM1CON0),
    7
extern volatile __bit C1OUT @ (((unsigned) &
    CM1CON0)*8) + 6;
#define C1OUT_bit BANKMASK(CM1CON0),
    6
extern volatile __bit C1POL @ (((unsigned) &
    CM1CON0)*8) + 4;
#define C1POL_bit BANKMASK(CM1CON0),
    4
extern volatile __bit C1R @ (((unsigned) &
    CM1CON0)*8) + 2;
#define C1R_bit BANKMASK(CM1CON0),
    2
extern volatile __bit C1RSEL @ (((unsigned) &
    CM2CON1)*8) + 5;
#define C1RSEL_bit BANKMASK(CM2CON1),
    5
extern volatile __bit C1SEN @ (((unsigned) &
    SRCON)*8) + 5;
#define C1SEN_bit BANKMASK(SRCON), 5
extern volatile __bit C2CH0 @ (((unsigned) &
    CM2CON0)*8) + 0;
#define C2CH0_bit BANKMASK(CM2CON0),
    0
extern volatile __bit C2CH1 @ (((unsigned) &
    CM2CON0)*8) + 1;
#define C2CH1_bit BANKMASK(CM2CON0),
    1
extern volatile __bit C2IE @ (((unsigned) &
    PIE2)*8) + 6;
#define C2IE_bit BANKMASK(PIE2), 6
extern volatile __bit C2IF @ (((unsigned) &
    PIR2)*8) + 6;
#define C2IF_bit BANKMASK(PIR2), 6
extern volatile __bit C2OE @ (((unsigned) &
    CM2CON0)*8) + 5;
#define C2OE_bit BANKMASK(CM2CON0),
    5
extern volatile __bit C2ON @ (((unsigned) &
    CM2CON0)*8) + 7;
#define C2ON_bit BANKMASK(CM2CON0),
    7
extern volatile __bit C2OUT @ (((unsigned) &
```

```
    CM2CON0)*8) + 6;
#define                 C2OUT_bit           BANKMASK(CM2CON0),
    6
extern volatile __bit   C2POL               @ (((unsigned) &
    CM2CON0)*8) + 4;
#define                 C2POL_bit           BANKMASK(CM2CON0),
    4
extern volatile __bit   C2R                 @ (((unsigned) &
    CM2CON0)*8) + 2;
#define                 C2R_bit             BANKMASK(CM2CON0),
    2
extern volatile __bit   C2REN               @ (((unsigned) &
    SRCON)*8) + 4;
#define                 C2REN_bit           BANKMASK(SRCON), 4
extern volatile __bit   C2RSEL              @ (((unsigned) &
    CM2CON1)*8) + 4;
#define                 C2RSEL_bit          BANKMASK(CM2CON1),
    4
extern volatile __bit   C2SYNC              @ (((unsigned) &
    CM2CON1)*8) + 0;
#define                 C2SYNC_bit          BANKMASK(CM2CON1),
    0
extern volatile __bit   CARRY               @ (((unsigned) &
    STATUS)*8) + 0;
#define                 CARRY_bit           BANKMASK(STATUS),
    0
extern volatile __bit   CCP1IE              @ (((unsigned) &
    PIE1)*8) + 2;
#define                 CCP1IE_bit          BANKMASK(PIE1), 2
extern volatile __bit   CCP1IF              @ (((unsigned) &
    PIR1)*8) + 2;
#define                 CCP1IF_bit          BANKMASK(PIR1), 2
extern volatile __bit   CCP1M0              @ (((unsigned) &
    CCP1CON)*8) + 0;
#define                 CCP1M0_bit          BANKMASK(CCP1CON),
    0
extern volatile __bit   CCP1M1              @ (((unsigned) &
    CCP1CON)*8) + 1;
#define                 CCP1M1_bit          BANKMASK(CCP1CON),
    1
extern volatile __bit   CCP1M2              @ (((unsigned) &
    CCP1CON)*8) + 2;
#define                 CCP1M2_bit          BANKMASK(CCP1CON),
    2
extern volatile __bit   CCP1M3              @ (((unsigned) &
    CCP1CON)*8) + 3;
#define                 CCP1M3_bit          BANKMASK(CCP1CON),
    3
extern volatile __bit   CCP1X               @ (((unsigned) &
    CCP1CON)*8) + 5;
#define                 CCP1X_bit           BANKMASK(CCP1CON),
    5
extern volatile __bit   CCP1Y               @ (((unsigned) &
    CCP1CON)*8) + 4;
#define                 CCP1Y_bit           BANKMASK(CCP1CON),
    4
extern volatile __bit   CCP2IE              @ (((unsigned) &
    PIE2)*8) + 0;
#define                 CCP2IE_bit          BANKMASK(PIE2), 0
extern volatile __bit   CCP2IF              @ (((unsigned) &
```

```
    PIR2)*8) + 0;
#define                         CCP2IF_bit          BANKMASK(PIR2), 0
extern volatile __bit           CCP2M0              @ (((unsigned) &
    CCP2CON)*8) + 0;
#define                         CCP2M0_bit          BANKMASK(CCP2CON),
    0
extern volatile __bit           CCP2M1              @ (((unsigned) &
    CCP2CON)*8) + 1;
#define                         CCP2M1_bit          BANKMASK(CCP2CON),
    1
extern volatile __bit           CCP2M2              @ (((unsigned) &
    CCP2CON)*8) + 2;
#define                         CCP2M2_bit          BANKMASK(CCP2CON),
    2
extern volatile __bit           CCP2M3              @ (((unsigned) &
    CCP2CON)*8) + 3;
#define                         CCP2M3_bit          BANKMASK(CCP2CON),
    3
extern volatile __bit           CCP2X               @ (((unsigned) &
    CCP2CON)*8) + 5;
#define                         CCP2X_bit           BANKMASK(CCP2CON),
    5
extern volatile __bit           CCP2Y               @ (((unsigned) &
    CCP2CON)*8) + 4;
#define                         CCP2Y_bit           BANKMASK(CCP2CON),
    4
extern volatile __bit           CHS0                @ (((unsigned) &
    ADCON0)*8) + 2;
#define                         CHS0_bit            BANKMASK(ADCON0),
    2
extern volatile __bit           CHS1                @ (((unsigned) &
    ADCON0)*8) + 3;
#define                         CHS1_bit            BANKMASK(ADCON0),
    3
extern volatile __bit           CHS2                @ (((unsigned) &
    ADCON0)*8) + 4;
#define                         CHS2_bit            BANKMASK(ADCON0),
    4
extern volatile __bit           CHS3                @ (((unsigned) &
    ADCON0)*8) + 5;
#define                         CHS3_bit            BANKMASK(ADCON0),
    5
extern volatile __bit           CKE                 @ (((unsigned) &
    SSPSTAT)*8) + 6;
#define                         CKE_bit             BANKMASK(SSPSTAT),
    6
extern volatile __bit           CKP                 @ (((unsigned) &
    SSPCON)*8) + 4;
#define                         CKP_bit             BANKMASK(SSPCON),
    4
extern volatile __bit           CREN                @ (((unsigned) &
    RCSTA)*8) + 4;
#define                         CREN_bit            BANKMASK(RCSTA), 4
extern volatile __bit           CSRC                @ (((unsigned) &
    TXSTA)*8) + 7;
#define                         CSRC_bit            BANKMASK(TXSTA), 7
extern volatile __bit           DATA_ADDRESS        @ (((unsigned) &
    SSPSTAT)*8) + 5;
#define                         DATA_ADDRESS_bit    BANKMASK(SSPSTAT),
    5
```

```
extern volatile __bit DC @ (((unsigned) &STATUS)*8) + 1;
#define DC_bit BANKMASK(STATUS), 1
extern volatile __bit DC1B0 @ (((unsigned) &CCP1CON)*8) + 4;
#define DC1B0_bit BANKMASK(CCP1CON), 4
extern volatile __bit DC1B1 @ (((unsigned) &CCP1CON)*8) + 5;
#define DC1B1_bit BANKMASK(CCP1CON), 5
extern volatile __bit DC2B0 @ (((unsigned) &CCP2CON)*8) + 4;
#define DC2B0_bit BANKMASK(CCP2CON), 4
extern volatile __bit DC2B1 @ (((unsigned) &CCP2CON)*8) + 5;
#define DC2B1_bit BANKMASK(CCP2CON), 5
extern volatile __bit D_A @ (((unsigned) &SSPSTAT)*8) + 5;
#define D_A_bit BANKMASK(SSPSTAT), 5
extern volatile __bit D_nA @ (((unsigned) &SSPSTAT)*8) + 5;
#define D_nA_bit BANKMASK(SSPSTAT), 5
extern volatile __bit ECCPAS0 @ (((unsigned) &ECCPAS)*8) + 4;
#define ECCPAS0_bit BANKMASK(ECCPAS), 4
extern volatile __bit ECCPAS1 @ (((unsigned) &ECCPAS)*8) + 5;
#define ECCPAS1_bit BANKMASK(ECCPAS), 5
extern volatile __bit ECCPAS2 @ (((unsigned) &ECCPAS)*8) + 6;
#define ECCPAS2_bit BANKMASK(ECCPAS), 6
extern volatile __bit ECCPASE @ (((unsigned) &ECCPAS)*8) + 7;
#define ECCPASE_bit BANKMASK(ECCPAS), 7
extern volatile __bit EEIE @ (((unsigned) &PIE2)*8) + 4;
#define EEIE_bit BANKMASK(PIE2), 4
extern volatile __bit EEIF @ (((unsigned) &PIR2)*8) + 4;
#define EEIF_bit BANKMASK(PIR2), 4
extern volatile __bit EEPGD @ (((unsigned) &EECON1)*8) + 7;
#define EEPGD_bit BANKMASK(EECON1), 7
extern volatile __bit FERR @ (((unsigned) &RCSTA)*8) + 2;
#define FERR_bit BANKMASK(RCSTA), 2
extern volatile __bit FVREN @ (((unsigned) &SRCON)*8) + 0;
#define FVREN_bit BANKMASK(SRCON), 0
```

```
extern volatile __bit GCEN @ (((unsigned) &
    SSPCON2)*8) + 7;
#define GCEN_bit BANKMASK(SSPCON2),
    7
extern volatile __bit GIE @ (((unsigned) &
    INTCON)*8) + 7;
#define GIE_bit BANKMASK(INTCON),
    7
extern volatile __bit GO @ (((unsigned) &
    ADCON0)*8) + 1;
#define GO_bit BANKMASK(ADCON0),
    1
extern volatile __bit GO_DONE @ (((unsigned) &
    ADCON0)*8) + 1;
#define GO_DONE_bit BANKMASK(ADCON0),
    1
extern volatile __bit GO_nDONE @ (((unsigned) &
    ADCON0)*8) + 1;
#define GO_nDONE_bit BANKMASK(ADCON0),
    1
extern volatile __bit HTS @ (((unsigned) &
    OSCCON)*8) + 2;
#define HTS_bit BANKMASK(OSCCON),
    2
extern volatile __bit I2C_DATA @ (((unsigned) &
    SSPSTAT)*8) + 5;
#define I2C_DATA_bit BANKMASK(SSPSTAT),
    5
extern volatile __bit I2C_READ @ (((unsigned) &
    SSPSTAT)*8) + 2;
#define I2C_READ_bit BANKMASK(SSPSTAT),
    2
extern volatile __bit I2C_START @ (((unsigned) &
    SSPSTAT)*8) + 3;
#define I2C_START_bit BANKMASK(SSPSTAT),
    3
extern volatile __bit I2C_STOP @ (((unsigned) &
    SSPSTAT)*8) + 4;
#define I2C_STOP_bit BANKMASK(SSPSTAT),
    4
extern volatile __bit INTE @ (((unsigned) &
    INTCON)*8) + 4;
#define INTE_bit BANKMASK(INTCON),
    4
extern volatile __bit INTEDG @ (((unsigned) &
    OPTION_REG)*8) + 6;
#define INTEDG_bit BANKMASK
    (OPTION_REG), 6
extern volatile __bit INTF @ (((unsigned) &
    INTCON)*8) + 1;
#define INTF_bit BANKMASK(INTCON),
    1
extern volatile __bit IOCB0 @ (((unsigned) &
    IOCB)*8) + 0;
#define IOCB0_bit BANKMASK(IOCB), 0
extern volatile __bit IOCB1 @ (((unsigned) &
    IOCB)*8) + 1;
#define IOCB1_bit BANKMASK(IOCB), 1
extern volatile __bit IOCB2 @ (((unsigned) &
    IOCB)*8) + 2;
```

```
#define IOCB2_bit BANKMASK(IOCB), 2
extern volatile __bit IOCB3 @ (((unsigned) &
    IOCB)*8) + 3;
#define IOCB3_bit BANKMASK(IOCB), 3
extern volatile __bit IOCB4 @ (((unsigned) &
    IOCB)*8) + 4;
#define IOCB4_bit BANKMASK(IOCB), 4
extern volatile __bit IOCB5 @ (((unsigned) &
    IOCB)*8) + 5;
#define IOCB5_bit BANKMASK(IOCB), 5
extern volatile __bit IOCB6 @ (((unsigned) &
    IOCB)*8) + 6;
#define IOCB6_bit BANKMASK(IOCB), 6
extern volatile __bit IOCB7 @ (((unsigned) &
    IOCB)*8) + 7;
#define IOCB7_bit BANKMASK(IOCB), 7
extern volatile __bit IRCF0 @ (((unsigned) &
    OSCCON)*8) + 4;
#define IRCF0_bit BANKMASK(OSCCON),
    4
extern volatile __bit IRCF1 @ (((unsigned) &
    OSCCON)*8) + 5;
#define IRCF1_bit BANKMASK(OSCCON),
    5
extern volatile __bit IRCF2 @ (((unsigned) &
    OSCCON)*8) + 6;
#define IRCF2_bit BANKMASK(OSCCON),
    6
extern volatile __bit IRP @ (((unsigned) &
    STATUS)*8) + 7;
#define IRP_bit BANKMASK(STATUS),
    7
extern volatile __bit LTS @ (((unsigned) &
    OSCCON)*8) + 1;
#define LTS_bit BANKMASK(OSCCON),
    1
extern volatile __bit MC1OUT @ (((unsigned) &
    CM2CON1)*8) + 7;
#define MC1OUT_bit BANKMASK(CM2CON1),
    7
extern volatile __bit MC2OUT @ (((unsigned) &
    CM2CON1)*8) + 6;
#define MC2OUT_bit BANKMASK(CM2CON1),
    6
extern volatile __bit MSK0 @ (((unsigned) &
    SSPMSK)*8) + 0;
#define MSK0_bit BANKMASK(SSPMSK),
    0
extern volatile __bit MSK1 @ (((unsigned) &
    SSPMSK)*8) + 1;
#define MSK1_bit BANKMASK(SSPMSK),
    1
extern volatile __bit MSK2 @ (((unsigned) &
    SSPMSK)*8) + 2;
#define MSK2_bit BANKMASK(SSPMSK),
    2
extern volatile __bit MSK3 @ (((unsigned) &
    SSPMSK)*8) + 3;
#define MSK3_bit BANKMASK(SSPMSK),
    3
```

```
extern volatile __bit MSK4 @ (((unsigned) &SSPMSK)*8) + 4;
#define MSK4_bit BANKMASK(SSPMSK), 4
extern volatile __bit MSK5 @ (((unsigned) &SSPMSK)*8) + 5;
#define MSK5_bit BANKMASK(SSPMSK), 5
extern volatile __bit MSK6 @ (((unsigned) &SSPMSK)*8) + 6;
#define MSK6_bit BANKMASK(SSPMSK), 6
extern volatile __bit MSK7 @ (((unsigned) &SSPMSK)*8) + 7;
#define MSK7_bit BANKMASK(SSPMSK), 7
extern volatile __bit OERR @ (((unsigned) &RCSTA)*8) + 1;
#define OERR_bit BANKMASK(RCSTA), 1
extern volatile __bit OSFIE @ (((unsigned) &PIE2)*8) + 7;
#define OSFIE_bit BANKMASK(PIE2), 7
extern volatile __bit OSFIF @ (((unsigned) &PIR2)*8) + 7;
#define OSFIF_bit BANKMASK(PIR2), 7
extern volatile __bit OSTS @ (((unsigned) &OSCCON)*8) + 3;
#define OSTS_bit BANKMASK(OSCCON), 3
extern volatile __bit P1M0 @ (((unsigned) &CCP1CON)*8) + 6;
#define P1M0_bit BANKMASK(CCP1CON), 6
extern volatile __bit P1M1 @ (((unsigned) &CCP1CON)*8) + 7;
#define P1M1_bit BANKMASK(CCP1CON), 7
extern volatile __bit PDC0 @ (((unsigned) &PWM1CON)*8) + 0;
#define PDC0_bit BANKMASK(PWM1CON), 0
extern volatile __bit PDC1 @ (((unsigned) &PWM1CON)*8) + 1;
#define PDC1_bit BANKMASK(PWM1CON), 1
extern volatile __bit PDC2 @ (((unsigned) &PWM1CON)*8) + 2;
#define PDC2_bit BANKMASK(PWM1CON), 2
extern volatile __bit PDC3 @ (((unsigned) &PWM1CON)*8) + 3;
#define PDC3_bit BANKMASK(PWM1CON), 3
extern volatile __bit PDC4 @ (((unsigned) &PWM1CON)*8) + 4;
#define PDC4_bit BANKMASK(PWM1CON), 4
extern volatile __bit PDC5 @ (((unsigned) &PWM1CON)*8) + 5;
#define PDC5_bit BANKMASK(PWM1CON),
```

```
    5
extern volatile __bit PDC6 @ (((unsigned) &
    PWM1CON)*8) + 6;
#define PDC6_bit BANKMASK(PWM1CON),
    6
extern volatile __bit PEIE @ (((unsigned) &
    INTCON)*8) + 6;
#define PEIE_bit BANKMASK(INTCON),
    6
extern volatile __bit PEN @ (((unsigned) &
    SSPCON2)*8) + 2;
#define PEN_bit BANKMASK(SSPCON2),
    2
extern volatile __bit PRSEN @ (((unsigned) &
    PWM1CON)*8) + 7;
#define PRSEN_bit BANKMASK(PWM1CON),
    7
extern volatile __bit PS0 @ (((unsigned) &
    OPTION_REG)*8) + 0;
#define PS0_bit BANKMASK
    (OPTION_REG), 0
extern volatile __bit PS1 @ (((unsigned) &
    OPTION_REG)*8) + 1;
#define PS1_bit BANKMASK
    (OPTION_REG), 1
extern volatile __bit PS2 @ (((unsigned) &
    OPTION_REG)*8) + 2;
#define PS2_bit BANKMASK
    (OPTION_REG), 2
extern volatile __bit PSA @ (((unsigned) &
    OPTION_REG)*8) + 3;
#define PSA_bit BANKMASK
    (OPTION_REG), 3
extern volatile __bit PSSAC0 @ (((unsigned) &
    ECCPAS)*8) + 2;
#define PSSAC0_bit BANKMASK(ECCPAS),
    2
extern volatile __bit PSSAC1 @ (((unsigned) &
    ECCPAS)*8) + 3;
#define PSSAC1_bit BANKMASK(ECCPAS),
    3
extern volatile __bit PSSBD0 @ (((unsigned) &
    ECCPAS)*8) + 0;
#define PSSBD0_bit BANKMASK(ECCPAS),
    0
extern volatile __bit PSSBD1 @ (((unsigned) &
    ECCPAS)*8) + 1;
#define PSSBD1_bit BANKMASK(ECCPAS),
    1
extern volatile __bit PULSR @ (((unsigned) &
    SRCON)*8) + 2;
#define PULSR_bit BANKMASK(SRCON), 2
extern volatile __bit PULSS @ (((unsigned) &
    SRCON)*8) + 3;
#define PULSS_bit BANKMASK(SRCON), 3
extern volatile __bit RA0 @ (((unsigned) &
    PORTA)*8) + 0;
#define RA0_bit BANKMASK(PORTA), 0
extern volatile __bit RA1 @ (((unsigned) &
    PORTA)*8) + 1;
```

```
#define                         RA1_bit         BANKMASK(PORTA), 1
extern volatile __bit           RA2             @ (((unsigned) &
    PORTA)*8) + 2;
#define                         RA2_bit         BANKMASK(PORTA), 2
extern volatile __bit           RA3             @ (((unsigned) &
    PORTA)*8) + 3;
#define                         RA3_bit         BANKMASK(PORTA), 3
extern volatile __bit           RA4             @ (((unsigned) &
    PORTA)*8) + 4;
#define                         RA4_bit         BANKMASK(PORTA), 4
extern volatile __bit           RA5             @ (((unsigned) &
    PORTA)*8) + 5;
#define                         RA5_bit         BANKMASK(PORTA), 5
extern volatile __bit           RA6             @ (((unsigned) &
    PORTA)*8) + 6;
#define                         RA6_bit         BANKMASK(PORTA), 6
extern volatile __bit           RA7             @ (((unsigned) &
    PORTA)*8) + 7;
#define                         RA7_bit         BANKMASK(PORTA), 7
extern volatile __bit           RB0             @ (((unsigned) &
    PORTB)*8) + 0;
#define                         RB0_bit         BANKMASK(PORTB), 0
extern volatile __bit           RB1             @ (((unsigned) &
    PORTB)*8) + 1;
#define                         RB1_bit         BANKMASK(PORTB), 1
extern volatile __bit           RB2             @ (((unsigned) &
    PORTB)*8) + 2;
#define                         RB2_bit         BANKMASK(PORTB), 2
extern volatile __bit           RB3             @ (((unsigned) &
    PORTB)*8) + 3;
#define                         RB3_bit         BANKMASK(PORTB), 3
extern volatile __bit           RB4             @ (((unsigned) &
    PORTB)*8) + 4;
#define                         RB4_bit         BANKMASK(PORTB), 4
extern volatile __bit           RB5             @ (((unsigned) &
    PORTB)*8) + 5;
#define                         RB5_bit         BANKMASK(PORTB), 5
extern volatile __bit           RB6             @ (((unsigned) &
    PORTB)*8) + 6;
#define                         RB6_bit         BANKMASK(PORTB), 6
extern volatile __bit           RB7             @ (((unsigned) &
    PORTB)*8) + 7;
#define                         RB7_bit         BANKMASK(PORTB), 7
extern volatile __bit           RBIE            @ (((unsigned) &
    INTCON)*8) + 3;
#define                         RBIE_bit        BANKMASK(INTCON),
    3
extern volatile __bit           RBIF            @ (((unsigned) &
    INTCON)*8) + 0;
#define                         RBIF_bit        BANKMASK(INTCON),
    0
extern volatile __bit           RC0             @ (((unsigned) &
    PORTC)*8) + 0;
#define                         RC0_bit         BANKMASK(PORTC), 0
extern volatile __bit           RC1             @ (((unsigned) &
    PORTC)*8) + 1;
#define                         RC1_bit         BANKMASK(PORTC), 1
extern volatile __bit           RC2             @ (((unsigned) &
    PORTC)*8) + 2;
#define                         RC2_bit         BANKMASK(PORTC), 2
```

```
extern volatile __bit RC3 @ (((unsigned) &
    PORTC)*8) + 3;
#define RC3_bit BANKMASK(PORTC), 3
extern volatile __bit RC4 @ (((unsigned) &
    PORTC)*8) + 4;
#define RC4_bit BANKMASK(PORTC), 4
extern volatile __bit RC5 @ (((unsigned) &
    PORTC)*8) + 5;
#define RC5_bit BANKMASK(PORTC), 5
extern volatile __bit RC6 @ (((unsigned) &
    PORTC)*8) + 6;
#define RC6_bit BANKMASK(PORTC), 6
extern volatile __bit RC7 @ (((unsigned) &
    PORTC)*8) + 7;
#define RC7_bit BANKMASK(PORTC), 7
extern volatile __bit RC8_9 @ (((unsigned) &
    RCSTA)*8) + 6;
#define RC8_9_bit BANKMASK(RCSTA), 6
extern volatile __bit RC9 @ (((unsigned) &
    RCSTA)*8) + 6;
#define RC9_bit BANKMASK(RCSTA), 6
extern volatile __bit RCD8 @ (((unsigned) &
    RCSTA)*8) + 0;
#define RCD8_bit BANKMASK(RCSTA), 0
extern volatile __bit RCEN @ (((unsigned) &
    SSPCON2)*8) + 3;
#define RCEN_bit BANKMASK(SSPCON2),
    3
extern volatile __bit RCIDL @ (((unsigned) &
    BAUDCTL)*8) + 6;
#define RCIDL_bit BANKMASK(BAUDCTL),
    6
extern volatile __bit RCIE @ (((unsigned) &
    PIE1)*8) + 5;
#define RCIE_bit BANKMASK(PIE1), 5
extern volatile __bit RCIF @ (((unsigned) &
    PIR1)*8) + 5;
#define RCIF_bit BANKMASK(PIR1), 5
extern volatile __bit RD @ (((unsigned) &
    EECON1)*8) + 0;
#define RD_bit BANKMASK(EECON1),
    0
extern volatile __bit RE3 @ (((unsigned) &
    PORTE)*8) + 3;
#define RE3_bit BANKMASK(PORTE), 3
extern volatile __bit READ_WRITE @ (((unsigned) &
    SSPSTAT)*8) + 2;
#define READ_WRITE_bit BANKMASK(SSPSTAT),
    2
extern volatile __bit RP0 @ (((unsigned) &
    STATUS)*8) + 5;
#define RP0_bit BANKMASK(STATUS),
    5
extern volatile __bit RP1 @ (((unsigned) &
    STATUS)*8) + 6;
#define RP1_bit BANKMASK(STATUS),
    6
extern volatile __bit RSEN @ (((unsigned) &
    SSPCON2)*8) + 1;
#define RSEN_bit BANKMASK(SSPCON2),
```

```
    1
extern volatile __bit                   RX9                 @ (((unsigned) &
    RCSTA)*8) + 6;
#define                                 RX9_bit             BANKMASK(RCSTA), 6
extern volatile __bit                   RX9D                @ (((unsigned) &
    RCSTA)*8) + 0;
#define                                 RX9D_bit            BANKMASK(RCSTA), 0
extern volatile __bit                   R_W                 @ (((unsigned) &
    SSPSTAT)*8) + 2;
#define                                 R_W_bit             BANKMASK(SSPSTAT),
    2
extern volatile __bit                   R_nW                @ (((unsigned) &
    SSPSTAT)*8) + 2;
#define                                 R_nW_bit            BANKMASK(SSPSTAT),
    2
extern volatile __bit                   SBOREN              @ (((unsigned) &
    PCON)*8) + 4;
#define                                 SBOREN_bit          BANKMASK(PCON), 4
extern volatile __bit                   SCKP                @ (((unsigned) &
    BAUDCTL)*8) + 4;
#define                                 SCKP_bit            BANKMASK(BAUDCTL),
    4
extern volatile __bit                   SCS                 @ (((unsigned) &
    OSCCON)*8) + 0;
#define                                 SCS_bit             BANKMASK(OSCCON),
    0
extern volatile __bit                   SEN                 @ (((unsigned) &
    SSPCON2)*8) + 0;
#define                                 SEN_bit             BANKMASK(SSPCON2),
    0
extern volatile __bit                   SENDB               @ (((unsigned) &
    TXSTA)*8) + 3;
#define                                 SENDB_bit           BANKMASK(TXSTA), 3
extern volatile __bit                   SMP                 @ (((unsigned) &
    SSPSTAT)*8) + 7;
#define                                 SMP_bit             BANKMASK(SSPSTAT),
    7
extern volatile __bit                   SPEN                @ (((unsigned) &
    RCSTA)*8) + 7;
#define                                 SPEN_bit            BANKMASK(RCSTA), 7
extern volatile __bit                   SR0                 @ (((unsigned) &
    SRCON)*8) + 6;
#define                                 SR0_bit             BANKMASK(SRCON), 6
extern volatile __bit                   SR1                 @ (((unsigned) &
    SRCON)*8) + 7;
#define                                 SR1_bit             BANKMASK(SRCON), 7
extern volatile __bit                   SREN                @ (((unsigned) &
    RCSTA)*8) + 5;
#define                                 SREN_bit            BANKMASK(RCSTA), 5
extern volatile __bit                   SSPEN               @ (((unsigned) &
    SSPCON)*8) + 5;
#define                                 SSPEN_bit           BANKMASK(SSPCON),
    5
extern volatile __bit                   SSPIE               @ (((unsigned) &
    PIE1)*8) + 3;
#define                                 SSPIE_bit           BANKMASK(PIE1), 3
extern volatile __bit                   SSPIF               @ (((unsigned) &
    PIR1)*8) + 3;
#define                                 SSPIF_bit           BANKMASK(PIR1), 3
extern volatile __bit                   SSPM0               @ (((unsigned) &
```

```
    SSPCON)*8) + 0;
#define                         SSPM0_bit           BANKMASK(SSPCON),
    0
extern volatile __bit           SSPM1               @ (((unsigned) &
    SSPCON)*8) + 1;
#define                         SSPM1_bit           BANKMASK(SSPCON),
    1
extern volatile __bit           SSPM2               @ (((unsigned) &
    SSPCON)*8) + 2;
#define                         SSPM2_bit           BANKMASK(SSPCON),
    2
extern volatile __bit           SSPM3               @ (((unsigned) &
    SSPCON)*8) + 3;
#define                         SSPM3_bit           BANKMASK(SSPCON),
    3
extern volatile __bit           SSPOV               @ (((unsigned) &
    SSPCON)*8) + 6;
#define                         SSPOV_bit           BANKMASK(SSPCON),
    6
extern volatile __bit           STRA                @ (((unsigned) &
    PSTRCON)*8) + 0;
#define                         STRA_bit            BANKMASK(PSTRCON),
    0
extern volatile __bit           STRB                @ (((unsigned) &
    PSTRCON)*8) + 1;
#define                         STRB_bit            BANKMASK(PSTRCON),
    1
extern volatile __bit           STRC                @ (((unsigned) &
    PSTRCON)*8) + 2;
#define                         STRC_bit            BANKMASK(PSTRCON),
    2
extern volatile __bit           STRD                @ (((unsigned) &
    PSTRCON)*8) + 3;
#define                         STRD_bit            BANKMASK(PSTRCON),
    3
extern volatile __bit           STRSYNC             @ (((unsigned) &
    PSTRCON)*8) + 4;
#define                         STRSYNC_bit         BANKMASK(PSTRCON),
    4
extern volatile __bit           SWDTEN              @ (((unsigned) &
    WDTCON)*8) + 0;
#define                         SWDTEN_bit          BANKMASK(WDTCON),
    0
extern volatile __bit           SYNC                @ (((unsigned) &
    TXSTA)*8) + 4;
#define                         SYNC_bit            BANKMASK(TXSTA), 4
extern volatile __bit           T0CS                @ (((unsigned) &
    OPTION_REG)*8) + 5;
#define                         T0CS_bit            BANKMASK
    (OPTION_REG), 5
extern volatile __bit           T0IE                @ (((unsigned) &
    INTCON)*8) + 5;
#define                         T0IE_bit            BANKMASK(INTCON),
    5
extern volatile __bit           T0IF                @ (((unsigned) &
    INTCON)*8) + 2;
#define                         T0IF_bit            BANKMASK(INTCON),
    2
extern volatile __bit           T0SE                @ (((unsigned) &
    OPTION_REG)*8) + 4;
```

```
#define T0SE_bit BANKMASK
    (OPTION_REG), 4
extern volatile __bit T1CKPS0 @ (((unsigned) &
    T1CON)*8) + 4;
#define T1CKPS0_bit BANKMASK(T1CON), 4
extern volatile __bit T1CKPS1 @ (((unsigned) &
    T1CON)*8) + 5;
#define T1CKPS1_bit BANKMASK(T1CON), 5
extern volatile __bit T1GINV @ (((unsigned) &
    T1CON)*8) + 7;
#define T1GINV_bit BANKMASK(T1CON), 7
extern volatile __bit T1GIV @ (((unsigned) &
    T1CON)*8) + 7;
#define T1GIV_bit BANKMASK(T1CON), 7
extern volatile __bit T1GSS @ (((unsigned) &
    CM2CON1)*8) + 1;
#define T1GSS_bit BANKMASK(CM2CON1),
    1
extern volatile __bit T1INSYNC @ (((unsigned) &
    T1CON)*8) + 2;
#define T1INSYNC_bit BANKMASK(T1CON), 2
extern volatile __bit T1OSCEN @ (((unsigned) &
    T1CON)*8) + 3;
#define T1OSCEN_bit BANKMASK(T1CON), 3
extern volatile __bit T1SYNC @ (((unsigned) &
    T1CON)*8) + 2;
#define T1SYNC_bit BANKMASK(T1CON), 2
extern volatile __bit T2CKPS0 @ (((unsigned) &
    T2CON)*8) + 0;
#define T2CKPS0_bit BANKMASK(T2CON), 0
extern volatile __bit T2CKPS1 @ (((unsigned) &
    T2CON)*8) + 1;
#define T2CKPS1_bit BANKMASK(T2CON), 1
extern volatile __bit TMR0IE @ (((unsigned) &
    INTCON)*8) + 5;
#define TMR0IE_bit BANKMASK(INTCON),
    5
extern volatile __bit TMR0IF @ (((unsigned) &
    INTCON)*8) + 2;
#define TMR0IF_bit BANKMASK(INTCON),
    2
extern volatile __bit TMR1CS @ (((unsigned) &
    T1CON)*8) + 1;
#define TMR1CS_bit BANKMASK(T1CON), 1
extern volatile __bit TMR1GE @ (((unsigned) &
    T1CON)*8) + 6;
#define TMR1GE_bit BANKMASK(T1CON), 6
extern volatile __bit TMR1IE @ (((unsigned) &
    PIE1)*8) + 0;
#define TMR1IE_bit BANKMASK(PIE1), 0
extern volatile __bit TMR1IF @ (((unsigned) &
    PIR1)*8) + 0;
#define TMR1IF_bit BANKMASK(PIR1), 0
extern volatile __bit TMR1ON @ (((unsigned) &
    T1CON)*8) + 0;
#define TMR1ON_bit BANKMASK(T1CON), 0
extern volatile __bit TMR2IE @ (((unsigned) &
    PIE1)*8) + 1;
#define TMR2IE_bit BANKMASK(PIE1), 1
extern volatile __bit TMR2IF @ (((unsigned) &
```

```
    PIR1)*8) + 1;
#define                         TMR2IF_bit          BANKMASK(PIR1), 1
extern volatile __bit           TMR2ON              @ (((unsigned) &
    T2CON)*8) + 2;
#define                         TMR2ON_bit          BANKMASK(T2CON), 2
extern volatile __bit           T0UTPS0             @ (((unsigned) &
    T2CON)*8) + 3;
#define                         T0UTPS0_bit         BANKMASK(T2CON), 3
extern volatile __bit           T0UTPS1             @ (((unsigned) &
    T2CON)*8) + 4;
#define                         T0UTPS1_bit         BANKMASK(T2CON), 4
extern volatile __bit           T0UTPS2             @ (((unsigned) &
    T2CON)*8) + 5;
#define                         T0UTPS2_bit         BANKMASK(T2CON), 5
extern volatile __bit           T0UTPS3             @ (((unsigned) &
    T2CON)*8) + 6;
#define                         T0UTPS3_bit         BANKMASK(T2CON), 6
extern volatile __bit           TRISA0              @ (((unsigned) &
    TRISA)*8) + 0;
#define                         TRISA0_bit          BANKMASK(TRISA), 0
extern volatile __bit           TRISA1              @ (((unsigned) &
    TRISA)*8) + 1;
#define                         TRISA1_bit          BANKMASK(TRISA), 1
extern volatile __bit           TRISA2              @ (((unsigned) &
    TRISA)*8) + 2;
#define                         TRISA2_bit          BANKMASK(TRISA), 2
extern volatile __bit           TRISA3              @ (((unsigned) &
    TRISA)*8) + 3;
#define                         TRISA3_bit          BANKMASK(TRISA), 3
extern volatile __bit           TRISA4              @ (((unsigned) &
    TRISA)*8) + 4;
#define                         TRISA4_bit          BANKMASK(TRISA), 4
extern volatile __bit           TRISA5              @ (((unsigned) &
    TRISA)*8) + 5;
#define                         TRISA5_bit          BANKMASK(TRISA), 5
extern volatile __bit           TRISA6              @ (((unsigned) &
    TRISA)*8) + 6;
#define                         TRISA6_bit          BANKMASK(TRISA), 6
extern volatile __bit           TRISA7              @ (((unsigned) &
    TRISA)*8) + 7;
#define                         TRISA7_bit          BANKMASK(TRISA), 7
extern volatile __bit           TRISB0              @ (((unsigned) &
    TRISB)*8) + 0;
#define                         TRISB0_bit          BANKMASK(TRISB), 0
extern volatile __bit           TRISB1              @ (((unsigned) &
    TRISB)*8) + 1;
#define                         TRISB1_bit          BANKMASK(TRISB), 1
extern volatile __bit           TRISB2              @ (((unsigned) &
    TRISB)*8) + 2;
#define                         TRISB2_bit          BANKMASK(TRISB), 2
extern volatile __bit           TRISB3              @ (((unsigned) &
    TRISB)*8) + 3;
#define                         TRISB3_bit          BANKMASK(TRISB), 3
extern volatile __bit           TRISB4              @ (((unsigned) &
    TRISB)*8) + 4;
#define                         TRISB4_bit          BANKMASK(TRISB), 4
extern volatile __bit           TRISB5              @ (((unsigned) &
    TRISB)*8) + 5;
#define                         TRISB5_bit          BANKMASK(TRISB), 5
extern volatile __bit           TRISB6              @ (((unsigned) &
```

```
    TRISB)*8) + 6;
#define                         TRISB6_bit          BANKMASK(TRISB), 6
extern volatile __bit           TRISB7              @ (((unsigned) &
    TRISB)*8) + 7;
#define                         TRISB7_bit          BANKMASK(TRISB), 7
extern volatile __bit           TRISC0              @ (((unsigned) &
    TRISC)*8) + 0;
#define                         TRISC0_bit          BANKMASK(TRISC), 0
extern volatile __bit           TRISC1              @ (((unsigned) &
    TRISC)*8) + 1;
#define                         TRISC1_bit          BANKMASK(TRISC), 1
extern volatile __bit           TRISC2              @ (((unsigned) &
    TRISC)*8) + 2;
#define                         TRISC2_bit          BANKMASK(TRISC), 2
extern volatile __bit           TRISC3              @ (((unsigned) &
    TRISC)*8) + 3;
#define                         TRISC3_bit          BANKMASK(TRISC), 3
extern volatile __bit           TRISC4              @ (((unsigned) &
    TRISC)*8) + 4;
#define                         TRISC4_bit          BANKMASK(TRISC), 4
extern volatile __bit           TRISC5              @ (((unsigned) &
    TRISC)*8) + 5;
#define                         TRISC5_bit          BANKMASK(TRISC), 5
extern volatile __bit           TRISC6              @ (((unsigned) &
    TRISC)*8) + 6;
#define                         TRISC6_bit          BANKMASK(TRISC), 6
extern volatile __bit           TRISC7              @ (((unsigned) &
    TRISC)*8) + 7;
#define                         TRISC7_bit          BANKMASK(TRISC), 7
extern volatile __bit           TRISE3              @ (((unsigned) &
    TRISE)*8) + 3;
#define                         TRISE3_bit          BANKMASK(TRISE), 3
extern volatile __bit           TRMT                @ (((unsigned) &
    TXSTA)*8) + 1;
#define                         TRMT_bit            BANKMASK(TXSTA), 1
extern volatile __bit           TUN0                @ (((unsigned) &
    OSCTUNE)*8) + 0;
#define                         TUN0_bit            BANKMASK(OSCTUNE),
    0
extern volatile __bit           TUN1                @ (((unsigned) &
    OSCTUNE)*8) + 1;
#define                         TUN1_bit            BANKMASK(OSCTUNE),
    1
extern volatile __bit           TUN2                @ (((unsigned) &
    OSCTUNE)*8) + 2;
#define                         TUN2_bit            BANKMASK(OSCTUNE),
    2
extern volatile __bit           TUN3                @ (((unsigned) &
    OSCTUNE)*8) + 3;
#define                         TUN3_bit            BANKMASK(OSCTUNE),
    3
extern volatile __bit           TUN4                @ (((unsigned) &
    OSCTUNE)*8) + 4;
#define                         TUN4_bit            BANKMASK(OSCTUNE),
    4
extern volatile __bit           TX8_9               @ (((unsigned) &
    TXSTA)*8) + 6;
#define                         TX8_9_bit           BANKMASK(TXSTA), 6
extern volatile __bit           TX9                 @ (((unsigned) &
    TXSTA)*8) + 6;
```

```
#define                         TX9_bit             BANKMASK(TXSTA), 6
extern volatile __bit           TX9D                @ (((unsigned) &
    TXSTA)*8) + 0;
#define                         TX9D_bit            BANKMASK(TXSTA), 0
extern volatile __bit           TXD8                @ (((unsigned) &
    TXSTA)*8) + 0;
#define                         TXD8_bit            BANKMASK(TXSTA), 0
extern volatile __bit           TXEN                @ (((unsigned) &
    TXSTA)*8) + 5;
#define                         TXEN_bit            BANKMASK(TXSTA), 5
extern volatile __bit           TXIE                @ (((unsigned) &
    PIE1)*8) + 4;
#define                         TXIE_bit            BANKMASK(PIE1), 4
extern volatile __bit           TXIF                @ (((unsigned) &
    PIR1)*8) + 4;
#define                         TXIF_bit            BANKMASK(PIR1), 4
extern volatile __bit           UA                  @ (((unsigned) &
    SSPSTAT)*8) + 1;
#define                         UA_bit              BANKMASK(SSPSTAT),
    1
extern volatile __bit           ULPWUE              @ (((unsigned) &
    PCON)*8) + 5;
#define                         ULPWUE_bit          BANKMASK(PCON), 5
extern volatile __bit           ULPWUIE             @ (((unsigned) &
    PIE2)*8) + 2;
#define                         ULPWUIE_bit         BANKMASK(PIE2), 2
extern volatile __bit           ULPWUIF             @ (((unsigned) &
    PIR2)*8) + 2;
#define                         ULPWUIF_bit         BANKMASK(PIR2), 2
extern volatile __bit           VCFG0               @ (((unsigned) &
    ADCON1)*8) + 4;
#define                         VCFG0_bit           BANKMASK(ADCON1),
    4
extern volatile __bit           VCFG1               @ (((unsigned) &
    ADCON1)*8) + 5;
#define                         VCFG1_bit           BANKMASK(ADCON1),
    5
extern volatile __bit           VR0                 @ (((unsigned) &
    VRCON)*8) + 0;
#define                         VR0_bit             BANKMASK(VRCON), 0
extern volatile __bit           VR1                 @ (((unsigned) &
    VRCON)*8) + 1;
#define                         VR1_bit             BANKMASK(VRCON), 1
extern volatile __bit           VR2                 @ (((unsigned) &
    VRCON)*8) + 2;
#define                         VR2_bit             BANKMASK(VRCON), 2
extern volatile __bit           VR3                 @ (((unsigned) &
    VRCON)*8) + 3;
#define                         VR3_bit             BANKMASK(VRCON), 3
extern volatile __bit           VREN                @ (((unsigned) &
    VRCON)*8) + 7;
#define                         VREN_bit            BANKMASK(VRCON), 7
extern volatile __bit           VROE                @ (((unsigned) &
    VRCON)*8) + 6;
#define                         VROE_bit            BANKMASK(VRCON), 6
extern volatile __bit           VRR                 @ (((unsigned) &
    VRCON)*8) + 5;
#define                         VRR_bit             BANKMASK(VRCON), 5
extern volatile __bit           VRSS                @ (((unsigned) &
    VRCON)*8) + 4;
```

```
#define VRSS_bit BANKMASK(VRCON), 4
extern volatile __bit WCOL @ (((unsigned) &
    SSPCON)*8) + 7;
#define WCOL_bit BANKMASK(SSPCON),
    7
extern volatile __bit WDTPS0 @ (((unsigned) &
    WDTCON)*8) + 1;
#define WDTPS0_bit BANKMASK(WDTCON),
    1
extern volatile __bit WDTPS1 @ (((unsigned) &
    WDTCON)*8) + 2;
#define WDTPS1_bit BANKMASK(WDTCON),
    2
extern volatile __bit WDTPS2 @ (((unsigned) &
    WDTCON)*8) + 3;
#define WDTPS2_bit BANKMASK(WDTCON),
    3
extern volatile __bit WDTPS3 @ (((unsigned) &
    WDTCON)*8) + 4;
#define WDTPS3_bit BANKMASK(WDTCON),
    4
extern volatile __bit WPUB0 @ (((unsigned) &
    WPUB)*8) + 0;
#define WPUB0_bit BANKMASK(WPUB), 0
extern volatile __bit WPUB1 @ (((unsigned) &
    WPUB)*8) + 1;
#define WPUB1_bit BANKMASK(WPUB), 1
extern volatile __bit WPUB2 @ (((unsigned) &
    WPUB)*8) + 2;
#define WPUB2_bit BANKMASK(WPUB), 2
extern volatile __bit WPUB3 @ (((unsigned) &
    WPUB)*8) + 3;
#define WPUB3_bit BANKMASK(WPUB), 3
extern volatile __bit WPUB4 @ (((unsigned) &
    WPUB)*8) + 4;
#define WPUB4_bit BANKMASK(WPUB), 4
extern volatile __bit WPUB5 @ (((unsigned) &
    WPUB)*8) + 5;
#define WPUB5_bit BANKMASK(WPUB), 5
extern volatile __bit WPUB6 @ (((unsigned) &
    WPUB)*8) + 6;
#define WPUB6_bit BANKMASK(WPUB), 6
extern volatile __bit WPUB7 @ (((unsigned) &
    WPUB)*8) + 7;
#define WPUB7_bit BANKMASK(WPUB), 7
extern volatile __bit WR @ (((unsigned) &
    EECON1)*8) + 1;
#define WR_bit BANKMASK(EECON1),
    1
extern volatile __bit WREN @ (((unsigned) &
    EECON1)*8) + 2;
#define WREN_bit BANKMASK(EECON1),
    2
extern volatile __bit WRERR @ (((unsigned) &
    EECON1)*8) + 3;
#define WRERR_bit BANKMASK(EECON1),
    3
extern volatile __bit WUE @ (((unsigned) &
    BAUDCTL)*8) + 1;
#define WUE_bit BANKMASK(BAUDCTL),
```

```
    1
extern volatile __bit                   ZERO                @ (((unsigned) &
    STATUS)*8) + 2;
#define                                 ZERO_bit            BANKMASK(STATUS),
    2
extern volatile __bit                   nA                  @ (((unsigned) &
    SSPSTAT)*8) + 5;
#define                                 nA_bit              BANKMASK(SSPSTAT),
    5
extern volatile __bit                   nADDRESS            @ (((unsigned) &
    SSPSTAT)*8) + 5;
#define                                 nADDRESS_bit        BANKMASK(SSPSTAT),
    5
extern volatile __bit                   nBO                 @ (((unsigned) &
    PCON)*8) + 0;
#define                                 nBO_bit             BANKMASK(PCON), 0
extern volatile __bit                   nBOR                @ (((unsigned) &
    PCON)*8) + 0;
#define                                 nBOR_bit            BANKMASK(PCON), 0
extern volatile __bit                   nDONE               @ (((unsigned) &
    ADCON0)*8) + 1;
#define                                 nDONE_bit           BANKMASK(ADCON0),
    1
extern volatile __bit                   nPD                 @ (((unsigned) &
    STATUS)*8) + 3;
#define                                 nPD_bit             BANKMASK(STATUS),
    3
extern volatile __bit                   nPOR                @ (((unsigned) &
    PCON)*8) + 1;
#define                                 nPOR_bit            BANKMASK(PCON), 1
extern volatile __bit                   nRBPU               @ (((unsigned) &
    OPTION_REG)*8) + 7;
#define                                 nRBPU_bit           BANKMASK
    (OPTION_REG), 7
extern volatile __bit                   nRC8                @ (((unsigned) &
    RCSTA)*8) + 6;
#define                                 nRC8_bit            BANKMASK(RCSTA), 6
extern volatile __bit                   nT1SYNC             @ (((unsigned) &
    T1CON)*8) + 2;
#define                                 nT1SYNC_bit         BANKMASK(T1CON), 2
extern volatile __bit                   nTO                 @ (((unsigned) &
    STATUS)*8) + 4;
#define                                 nTO_bit             BANKMASK(STATUS),
    4
extern volatile __bit                   nTX8                @ (((unsigned) &
    TXSTA)*8) + 6;
#define                                 nTX8_bit            BANKMASK(TXSTA), 6
extern volatile __bit                   nW                  @ (((unsigned) &
    SSPSTAT)*8) + 2;
#define                                 nW_bit              BANKMASK(SSPSTAT),
    2
extern volatile __bit                   nWRITE              @ (((unsigned) &
    SSPSTAT)*8) + 2;
#define                                 nWRITE_bit          BANKMASK(SSPSTAT),
    2

#endif // _PIC16F886_H_
```