DYNAMIC VOLTAGE RESTORER DEVELOPMENT AND TESTING

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Abstract – **The growing use of sensitive loads in the electric power system, especially in industrial applications, increases considerably production losses related to voltage sags, stimulating a demand for power electronics' based solutions to mitigate the effects of such problems. This paper shows the implementation and certification tests of a power equipment prototype designed to correct sags and swells, a dynamic voltage restorer, which is one of the many possible solutions for voltage sags and swells problems. The objectives are to show the relevance of proper design criteria and to propose an equipment tests procedure, including industrial certification. Experimental results of a 75kVA prototype are shown both in laboratory and full load conditions, in a certification institution (IEE-USP).**

Keywords **– PWM Converter, Power Quality, Dynamic Voltage Restorer, Voltage Sags, Voltage Swells.**

I. INTRODUCTION

Power system disturbances may affect sensitive loads on most industrial processes [1]. According to [2], momentary voltage sag is defined by a 0.1 to 0.9 RMS supply voltage amplitude decrease, with 1 cycle to 3 seconds duration. Voltage sags are generally caused by adjacent power line failures, climatic factors or a large motor starting, and may cause failures or incorrect operation in electric devices and machines.

One possible power quality solution, the dynamic voltage restorer (DVR) is an equipment series connected to the load, through a power transformer, and it restores the load voltage when voltage sags occur. It uses a power inverter to add a real time calculated voltage to the remaining supply voltage, so that the load voltage remains immune to the power system disturbance, and between acceptable boundaries.

This paper describes a 75kVA DVR prototype and its characteristics, which include voltage and current active filtering, and reactive power compensation. Limited power tests were performed in a development laboratory environment in order to assure hardware and software correct operation, and full power tests were accomplished in a certification institution (IEE-USP) for industrial certification purposes. After obtaining satisfactory operation in laboratory condition, new power equipment still require extensive testing before being installed in industrial environment. Some characteristics need to be verified, such as: reliability, stable long term operation, protections, immunity to power network oscillations and peripheral equipment failures. Only after these extensive testing, a new equipment should be considerate for installation.´

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II. DVR TOPOLOGY

A. Overview

The proposed DVR topology is presented in Figure 1. It shows a series branch composed with three H-bridge inverters connected to the mains using single-phase series transformers. Besides sag and swell correction purposes, series branch also filters mains side voltage harmonics. A parallel branch, composed by a three-phase PWM rectifier, keeps DC-link voltage within design limits for sags and swells events. The parallel branch also works as load harmonic currents active filter.

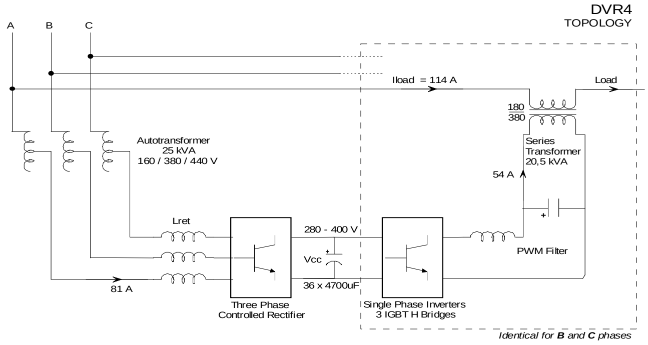

Figure 1: DVR's simplified electric diagram.

The development of the DVR project was accomplished with two distinctive stages. Initially, the basic technology was established with the construction of three prototypes:

• DVR01/03 [3], [4], [5]: A DVR with active current and voltage filters, besides sags and swells compensation. Nominal load and rated voltage: 10kVA/220V (for three phase systems);

• DVR02 [6]: Also a DVR with active current and voltage filters, sags and swells compensation. Nominal load and rated voltage: 75kVA/380-440V (for three phase systems).

For the following stage, improvement and optimization of the earlier developed technology was sought, aiming increased reliability and cost reduction. Prototypes developed at this stage used the consolidated topology and the same rated power as DVR2: 75kVA/380V. Therefore, DVR4 prototype is similar to DVR2, apart from different DSP platforms (migration from Analog Devices 21992 family to Texas Instruments 2812 family), an optimized design of some hardware items, full software upgrade as well as safety and protection procedures revision.

The DVR4 software was implemented on Texas Instruments 2812 fixed point DSP platform, written in the C programming language.

B. Performance criteria

Performance criteria for the DVR's prototypes were established after power distribution network studies inside

CPFL (Companhia Paulista de Força e Luz) concession area.

The DVRs are designed to compensate:

- Single phase voltage sags up to 50% remaining voltage.
- Three phase voltage sags up to 500ms (thirty 60Hz cycles) and 65% remaining voltage.
- Three phase voltage swells up to 500 ms and 20% overvoltage.

III. Tests Results

After their assembly, the DVR prototypes are calibrated and tested in a development laboratory environment, with limited available power. During this stage building errors are detected, sensors are calibrated and controller constants are set to their initial values, for warm-up tests up to 40% of nominal power.

The equipment is tested at rated power at the University of São Paulo's Electrotechnical and Energy Institute (IEE-USP), for design validation and industrial certification purposes. The results for DVR4 prototype are shown next.

A. Development laboratory tests

Development laboratory tests were performed using an experimental setup with:

- Three phase resistive load of 15Ω, 10Ω and 5Ω taps.
- Induction motor, 2 HP rated power, connected to a mechanical load.
- Non-linear load (three phase bridge rectifier connected to a DC-side capacitive filter and variable resistive load).
- Power supply: Porto-sag equipment [7], developed by EPRI (Electric Power Research Institute), generating voltage sags down to 0% and voltage swells up to 25% nominal voltage[1], with 1-60 cycles duration.

Some of the development laboratory experimental results are shown in Figures 2 to 5. Figure 2 shows in detail input and output voltages at the end of voltage sag in no load condition. One can observe that output voltages are undisturbed during the whole period. The voltage overshoot at the end of the event has duration of less than a quarter of a cycle.

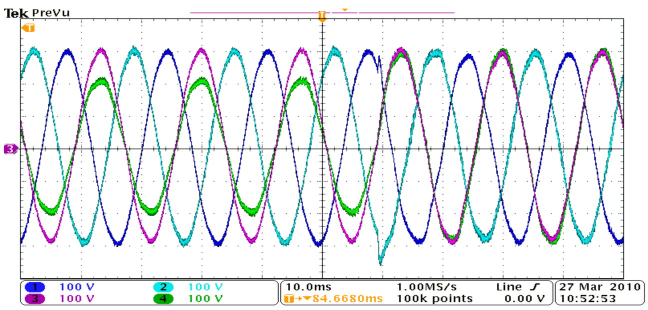

Figure 2: End of sag event in detail - 30 cycle three phase voltage sag, at 60% remaining voltage. Mains voltage waveform is seen in green (channel 4). Output voltage waveforms are seen in the remaining channels.

Figure 3 shows the dynamic behavior of the output voltages and currents after 30 cycle 60% voltage sag, with the 10kW three-phase resistive load. Output voltages and currents remain within nominal values during the voltage sag.

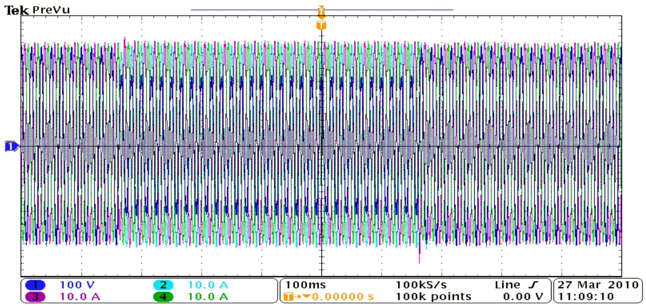

Figure 3: 30 cycle three phase voltage sag, at 60% remaining voltage. Mains voltage waveform is seen in blue (channel 1). Output currents waveforms are seen in the remaining channels.

Figures 4 and 5 show the DVR's performance as active parallel filter, in steady state conditions, with the non-linear load. Figure 4 shows the voltage and current waveforms in the uncompensated case.

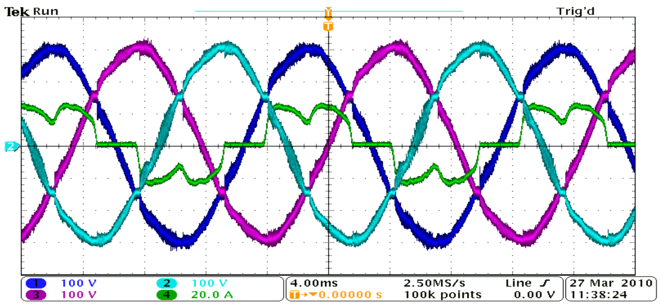

Figure 4: Non-linear load, with active filter turned off. Mains current waveform is seen in green (channel 4). Output voltage waveforms are seen in the remaining channels.

Figure 5 shows the same voltage and current waveforms during the compensated case (current active filter operating).

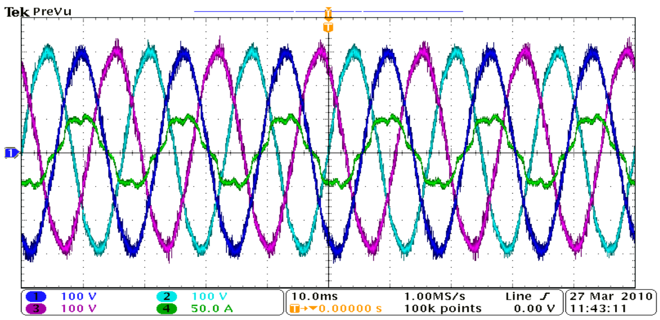

Figure 5: Non-linear load, with active filter turned on. Mains current waveform is seen in green (channel 4). Output voltage waveforms are seen in the remaining channels.

The current total harmonic distortion (THDi) is 32,7% in the uncompensated case, and is reduced to 14,2% as the active filter function is turned on.

B. IEE-USP tests

The development laboratory tests were useful to assure the correct functioning of the DVR prototype, in a power limited environment. The DVR prototype was further tested in more realistic conditions at the IEE-USP, which included voltage regulation, efficiency, harmonic distortion, among other tests, at no load, half load and nominal load conditions, aiming for certification tests approval [8].

[1] A voltage swell up to 25% means 125% load rated voltage is applied. A voltage sag to 65% means that load voltage during the sag is 65% of its rated value.

Figure 6: DVR transport and installation at IEE-USP.

Figure 7: DVR test preparations at IEE-USP.

Figure 8 shows three phase nominal load rejection test, for AC mains and load sides transient behavior records.

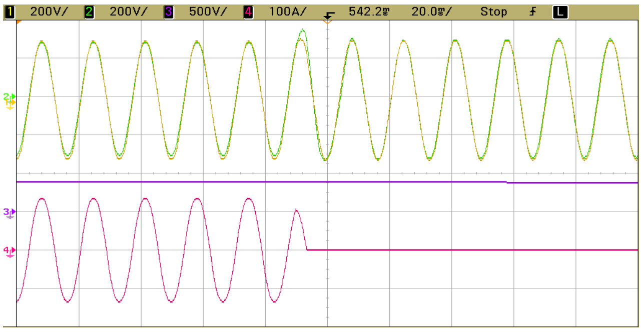

Figure 8: Turning off of three phase resistive nominal load. Mains voltage (yellow), load voltage (green), DC link voltage (purple) and load current (pink).

Figure 9 shows insertion of rated power three phase resistive load.

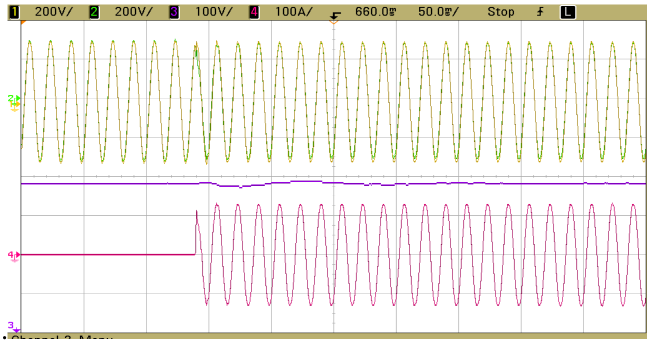

Figure 9: Energization of the DVR with three phase resistive nominal load. Mains voltage (yellow), load voltage (green), DC link voltage (purple) and load current (pink).

Response of three phase voltage sag to 75% is shown in Figure 10. One can observe that the output voltages and currents remain at nominal value during the disturbance. The DC link voltage varies within acceptable limits.

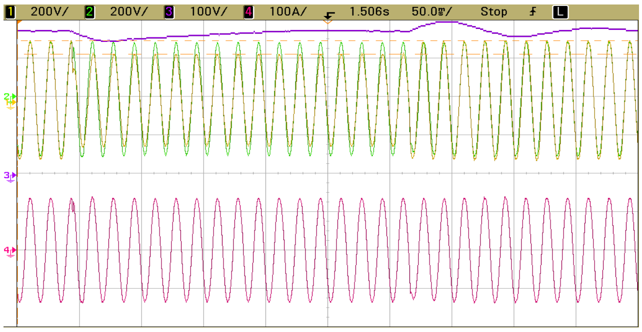

Figure 10: 0,75PU remaining voltage sag, 16 cycles, with three phase resistive nominal load. Mains voltage (yellow), load voltage (green), DC link voltage (purple) and load current (pink).

The parallel harmonic filter was tested with a non linear load, shown in Figure 11. It is composed by three single phase full bridge rectifiers. In each DC side load there is a pre-charge circuit in order to avoid DC capacitors charge surge currents. An autotransformer was used to reduce voltage on the load side, keeping DC capacitors voltage within rated limits. A Y connection was chosen to make line currents more distorted. The three phase power for this test is 30kVA.

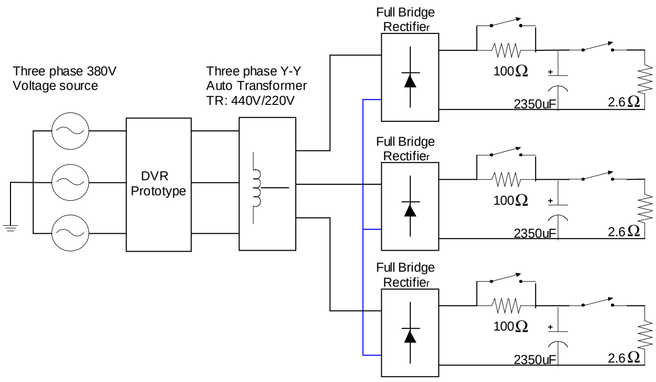

Figure 11: Non linear load experimental setup.

Figure 12 shows the voltages and currents waveforms generated by this setup, with active filter turned off. Load currents are highly distorted as expected. In this case, the mains current total harmonic distortion (THDi) is 57.3%.

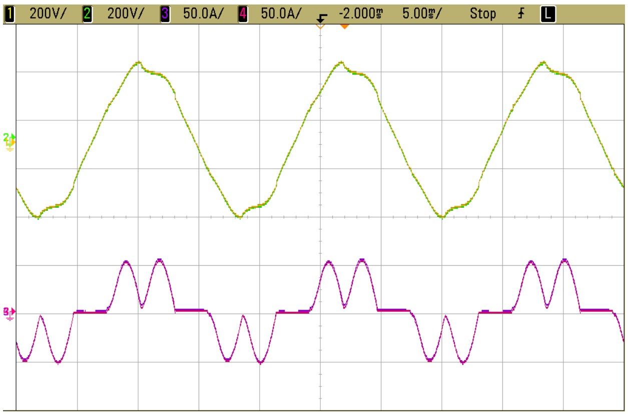

Figure 12: Non-linear load, with active filter turned off. Mains voltage (yellow), load voltage (green), mains current (purple), load current (pink).

Once the active parallel filter is turned on, the current and, therefore also the voltage, distortion is significantly reduced. THDi is reduced to 12.6%. There is still significant distortion, due to limited band pass and control gains values, but improvement is noticeable.

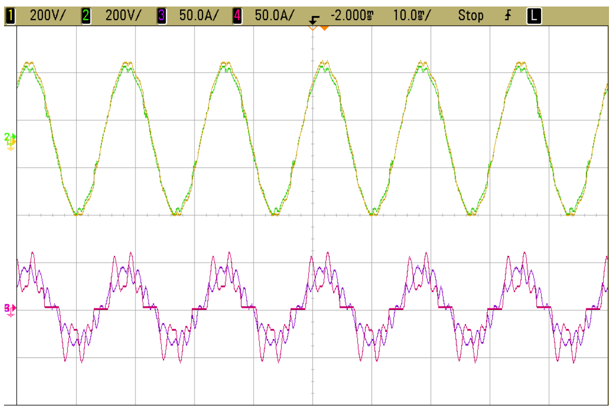

Figure 13: Non-linear load, with active filter turned on. Mains voltage (yellow), load voltage (green), mains current (purple), load current (pink).

Figure 14 shows the active filter's behavior if voltage sag would occur. As the control system detects the voltage sag, it automatically turns off the active filtering, so that the parallel branch can be used only to recharge the DC link capacitors and supply enough energy to compensate nominal voltage. This characteristic can be observed in Figure 14, as the mains and load currents get distorted after the beginning of the voltage sag [9].

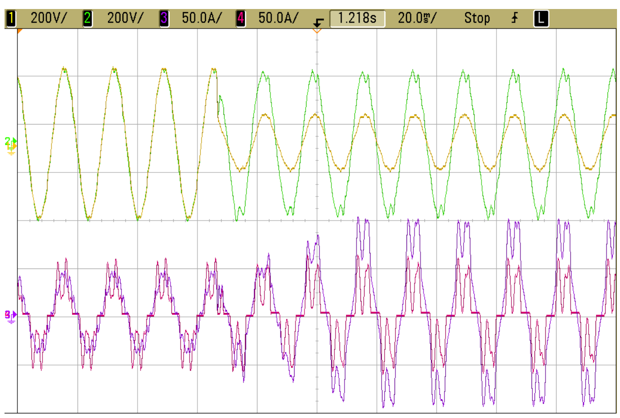

Figure 14: Non-linear load, with active filter turned during steady state behavior, turns off during voltage sag. Mains voltage (yellow), load voltage (green), mains current (purple), load current (pink).

IV. Conclusions

In this paper a DVR prototype topology was described and its constructive characteristics and performance criteria were discussed. Laboratory tests, which demonstrated hardware and software reliability, were discussed and shown. Also, certification tests results at IEE-USP were displayed.

The discussion and establishment of the details in this process is very important in the development of a equipment such as the DVR.

The R&D project's results fulfill the proposed goals and a new prototype, to be called DVR6, should become the first unit past the prototypes phase, aiming for a of a future industrialization process.

Final version of the paper will include more details on the DVR development and its tests.

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V. References

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