1 General technical information

1.1 Introduction

Despite its many benefits, one of the few drawbacks of semiconductor technology is the vulnerability of solid-state devices to overvoltages. Even voltage pulses of very low energy can produce interference and damage, sometimes with far-reaching consequences. So, as electronics makes its way into more and more applications, optimum overvoltage or transient suppression becomes a design factor of decisive importance.

SIOV® varistors have proven to be excellent protective devices because of their application flexibility and high reliability. The metal oxide varistor, with its extremely attractive price/performance ratio, is an ideal component for limiting surge voltage and current as well as for absorbing energy.

The EPCOS product range includes SMDs for surface mounting, radial-lead disks, block varistors, strap-lead varistors and arrester blocks for power distribution applications. Special types for automotive electrical systems and for telecom applications round off the product range.

Overvoltage protection devices like SIOV varistors are in international publications often referred to as TVSS (Transient Voltage Surge Suppressors).

1.2 Definition

Varistors (**Var**iable Res**istors**) are voltage-dependent resistors with a symmetrical *V*/*I* characteristic curve (figure 1b) whose resistance decreases with increasing voltage. Connected in parallel with the electronic device or circuit that is to be guarded, they form a low-resistance shunt when voltage increases and thus prevent any further rise in the overvoltage.

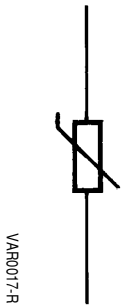


Figure 1a Circuit diagram symbol for a varistor

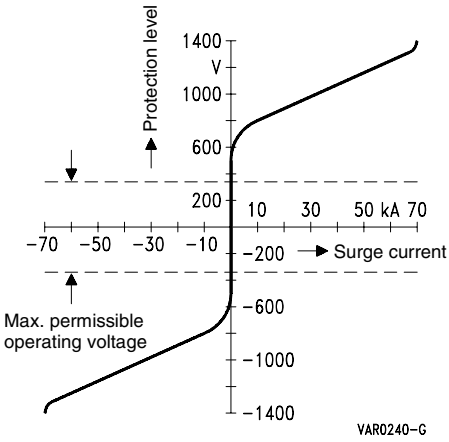


Figure 1b Typical *V*/*I* characteristic curve of a metal oxide varistor on a linear scale, using the SIOV-B60K250 as an example

® Registered trademark for EPCOS metal oxide varistors

The voltage dependence of varistors or VDRs (**V**oltage **D**ependent **R**esistors) may be approximately characterized by the formula $I = K \cdot V^{\alpha}$, where α denotes the "nonlinearity" exponent and in this way may be interpreted as a measure for the "steepness" of the *V*/*I* characteristic (more details will follow in section 1.6). In metal oxide varistors it has been possible to produce α figures of more than 30. This puts their protection levels in the same region as those of zener diodes and suppressor diodes. Exceptional current handling capability combined with response times of < 25 ns (SMD < 0,5 ns) make them an almost perfect protective device. The principle of overvoltage protection by varistors is explained in section 2.2.

1.3 Microstructure and conduction mechanism

Sintering zinc oxide together with other metal oxide additives under specific conditions produces a polycrystalline ceramic whose resistance exhibits a pronounced dependence on voltage. This phenomenon is called the varistor effect.

Figure 2 shows the conduction mechanism in a varistor element in simplified form. The zinc oxide grains themselves are highly conductive, while the intergranular boundary formed of other oxides is highly resistive. Only at those points where zinc oxide grains meet does sintering produce "microvaristors", comparable to symmetrical zener diodes (protection level approx. 3,5 V). The electrical behavior of the metal oxide varistor, as indicated by figure 2, results from the number of microvaristors connected in series or in parallel.

This implies that the electrical properties are controlled by the physical dimensions of the varistor:

- Twice the ceramic thickness produces twice the protection level because then twice as many microvaristors are arranged in series.
- Twice the area produces twice the current handling capability because then twice the number of current paths are arranged in parallel.
- Twice the volume produces almost twice the energy absorption capability because then there are twice as many absorbers in the form of zinc oxide grains.

The series and parallel connection of the individual microvaristors in the sintered body of a SIOV also explains its high electrical load capacity compared to semiconductors. While the power in semiconductors is dissipated almost entirely in the thin p-n junction area, in a SIOV it is distributed over all the microvaristors, i. e. uniformly throughout the component's volume. Each microvaristor is provided with energy absorbers in the form of zinc oxide grains with optimum thermal contact. This permits high absorption of energy and thus exceptionally high surge current handling capability.

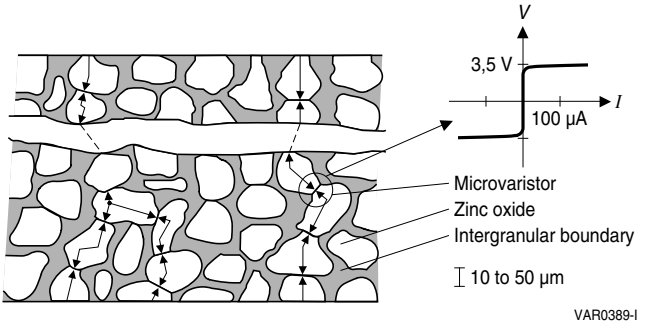


Figure 2 Conduction mechanism in a varistor element

Grain size

For matching very different levels of protection to ceramic thicknesses that are suitable for fabrication, SIOV varistors have to be produced from ceramics with different voltage gradients. The variation of raw materials and sintering control influence the growth of grain size (grain diameter approx. 10 to 100 μm) and thus produce the required specific ceramic voltage (approx. 30 to 250 V/mm). The *V*/*I* characteristic of the individual microvaristors is not affected by this.

Ceramics with a small specific voltage (low-voltage types) cannot handle the same current density as high-voltage types. That explains the differences in surge current, energy absorption and mechanical dimensions within the various type series. The effect of the different grain sizes is most apparent between the voltage classes K40 and K50. For example, the maximum permissible surge current is:

SIOV-S07K40 i_{max} = 250 A
SIOV-S07K50 i_{max} = 1200 A

Multilayer technology overcomes this obstacle by using high-load-capacity fine-grain ceramics even for operating voltages of < 50 V. This permits decidedly higher surge currents with higher non-linearity, i. e. lower protection levels.

1.4 Construction

Sintered metal oxide ceramics are processed on different production lines:

SMD type series CT/CN
The rectangular multilayer ceramics are electroded on their narrow faces (cross section figure 33).

SMD type series CA
These are multilayer chip arrays incorporating multiple varistor systems.

SMD type series CU
The disk-shaped varistor ceramics are fitted with flat metal electrodes (tinned copper alloy) and encapsulated in thermoplast by injection molding.

Disk types
Here the varistor disk is fitted with leads of tinned copper wire and then the ceramic body is coated with epoxy resin in a fluidized bed.

Block types
The large electromagnetic forces involved in handling currents between 10 and 100 kA call for solid contacting with special electrodes and potting in a plastic housing. Block varistors are electrically and mechanically connected by screw terminals.

Strap types
After contacting of the varistor ceramics with special bolt-holed electrodes, these components are coated with epoxy resin in a fluidized bed.

Arrester blocks
Cylindrical varistor ceramics, glass-passivated collar, flame-sprayed electrodes for pressure contacting.

For photos of all constructions see *"Type Series Overview"*, page 8 ff.

1.5 Equivalent circuits

Figure 3a shows the simplified equivalent circuit of a metal oxide varistor. From this the behavior of the varistor can be interpreted for different current ranges.

Leakage current region (< 10^{-4} A)
In the leakage current region the resistance of an ideal varistor goes towards ∞, so it can be ignored as the resistance of the intergranular boundary will predominate. Therefore $R_B << R_{IG}$. This produces the equivalent circuit in figure 3b:

The ohmic resistance R_{IG} determines behavior at small currents, the *V*/*I* curve goes from exponential to linear (downturn region).
R_{IG} shows a distinct temperature dependence, so a marked increase in leakage current must be expected as temperature increases.

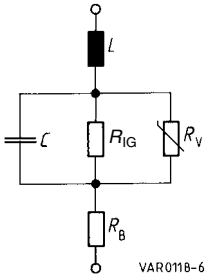
Normal operating region (10^{-5} to 10^3 A)
With $R_V << R_{IG}$ and $R_B << R_V$, R_V determines the electrical behavior (figure 3c). The *V*/*I* curve (figure 5) follows to a good approximation the simple mathematical description by an exponential function (equation 3 in 1.6.1) where $\alpha > 30$, i. e. the curve appears more or less as a straight line on a log-log scale.

High-current region (> 10^3 A)
Here the resistance of the ideal varistor approaches zero. This means that $R_V << R_{IG}$ and $R_V < R_B$ (figure 3d). The ohmic bulk resistance of ZnO causes the *V*/*I* curve to resume a linear characteristic (upturn region).

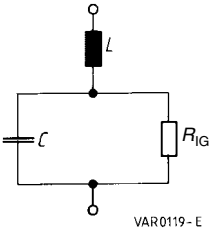
Capacitance
Equivalent circuits 3b and 3c indicate the capacitance of metal oxide varistors (see product tables for typical values).
In terms of overvoltage suppression, a high capacitance is desirable because, with its lowpass characteristic, it smooths steep surge voltage edges and consequently improves the protection level.

Lead inductance
The response time of the actual varistor ceramics is in the picosecond region. In the case of leaded varistors, the inductance of the connecting leads causes the response time to increase to values of several nanoseconds. For this reason, all attempts must be made to achieve a mounting method with the lowest possible inductance i. e. shortest possible leads.
Multilayer varistors have considerably shorter response times due to their low-inductance design.

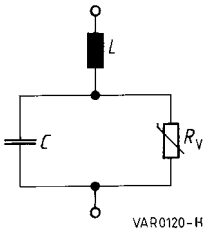
3a



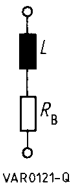
3b



3c



3d



L	Lead inductance (≈ 1 nH/mm)
C	Capacitance
R_{IG}	Resistance of intergranular boundary ($\rho \approx 10^{12}$ to 10^{13} Ωcm)
R_V	Ideal varistor (0 to ∞ Ω)
R_B	Bulk resistance of ZnO ($\rho \approx 1$ to 10 Ωcm)

Figures 3a – d Equivalent circuits

1.6 *V/I* characteristics

1.6.1 Forms of presentation

The *V/I* characteristics of metal oxide varistors are similar to those of power functions (odd exponents), so it is fairly obvious that the latter should be used to describe them. As the curves are symmetrical, only one quadrant is generally shown for reasons of simplification (figure 4a):

$$I = K V^{\alpha} \qquad \alpha > 1 \qquad \text{(equ. 1)}$$

I	Current through varistor
V	Voltage across varistor
K	Ceramic constant (depending on varistor type)
α	Nonlinearity exponent (measure of nonlinearity of curve)

Another possible interpretation of the physical principle underlying these curves is that of a voltage-dependent resistance value, and particularly its rapid change at a predetermined voltage. This phenomenon is the basis of the varistor protection principle (figure 4b):

$$R = \frac{V}{I} = \frac{V}{K\ V^{\alpha}} = \frac{1}{K} V^{1-\alpha} \qquad \text{(equ. 2)}$$

Equations 1 and 2 can be shown particularly clearly on a log-log scale, because power functions then appear as straight lines:

$$\log I = \log K + \alpha\ \log V \qquad \text{(equ. 3)}$$

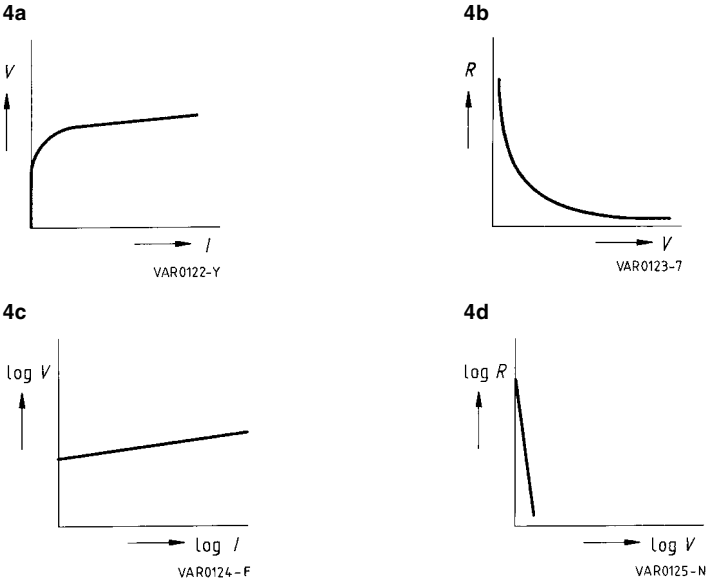
$$\log R = \log\left(\frac{1}{K}\right) + (1-\alpha)\log V \qquad \text{(equ. 4)}$$

This is virtually the only form of presentation used for varistor characteristics (figures 4c and d). A further advantage of the log-log format is the possibility of showing the wide range of the *V/I* curve (more than ten powers of 10).

It is evident that the simplified equations 1 to 4 cannot cover the downturn and upturn regions as described in section 1.5. Here, a mathematical description as shown in equation 21 on page 86 is required.

Determining nonlinearity exponent α
Two pairs of voltage/current values (V_1/I_1 and V_2/I_2) are read from the *V/I* characteristic of the varistor and inserted into equation 3, solved for α:

$$\alpha = \frac{\log I_2 - \log I_1}{\log V_2 - \log V_1} \qquad \text{(equ. 5)}$$



Figures 4a – d Presentation of the *V*/*I* characteristics

1.6.2 Real *V*/*I* characteristic and ohmic resistance

Figure 5 shows a typical *V*/*I* characteristic with SIOV-B60K250 taken as example.

The downturn and upturn regions according to equivalent circuits 3b and 3d are easy to make out.

Calculating nonlinearity exponent α
Normally α is determined according to equation 5 from the pairs of values for 1 A and 1 mA of the *V*/*I* characteristic. For figure 5 this means:

$$\alpha = \frac{\log I_2 - \log I_1}{\log V_2 - \log V_1} = \frac{\log 1 - \log 10^{-3}}{\log 470 - \log 390} = \frac{0 - (-3)}{2{,}67 - 2{,}59} = \frac{3}{0{,}08} \approx 38$$

The *V*/*I* curve of figure 5 is virtually a straight line between 10^{-4} and 10^{3} A, so it is described over a wide range to a good approximation by equation 3. The downturn and upturn regions may be adapted by inserting correction components in equation 3.

Another type of characteristic curve approximation is described in section 3.10.1

Deriving from figure 5, figure 6 shows the change in static resistance $R = V/I$ for SIOV-B60K250. The resistance is > 1 MΩ in the range of the permissible operating voltage, whereas it can drop by as many as ten powers of 10 in case of overvoltage.

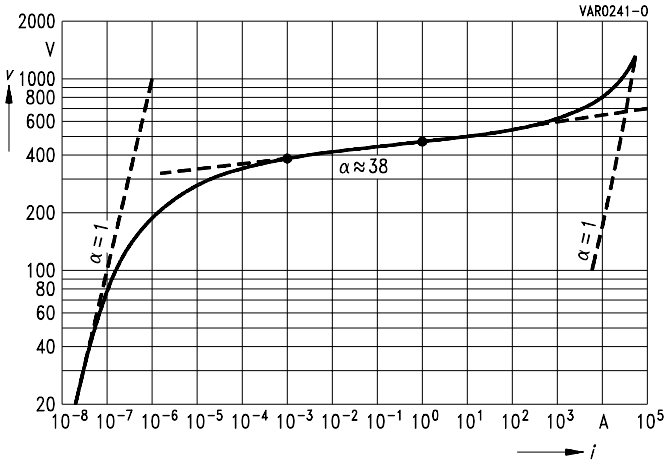


Figure 5 Real *V*/*I* characteristic of a metal oxide varistor with SIOV-B60K250 taken as example

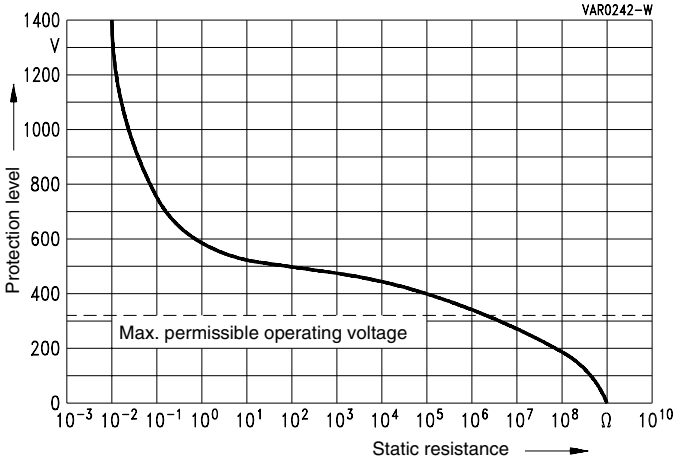


Figure 6 Static resistance of a metal oxide varistor versus protection level with SIOV-B60K250 taken as example

1.6.3 Presentation of tolerance band

The real *V*/*I* characteristic of individual varistors is subject to a certain deviation, which is primarily due to minor fluctuations in manufacturing and assembly process parameters. For varistors belonging to a certain type, their *V*/*I* curves are required to lie entirely within a well defined tolerance band. The tolerance band shown in figure 7a illustrates this in the case of SIOV-S14K14.

Varistors are operated at either one out of two conditions: If the circuit is operated at normal operating voltage, the varistor shall be highly resistive. In an overvoltage event, it shall be highly conductive.

These conditions are concerning two different segments of the *V*/*I* curve:

Lefthand part of curve (< 1 mA): This part of the curve refers to the “high-resistance” mode, where circuit designers may generally want to know about the largest possible leakage current at given operating voltage. Therefore the lower limit of the tolerance band is shown.

Righthand part of the curve (> 1 mA): This segment covers the “low-resistance” mode in an overvoltage event, where circuit designer’s primary concern is about the worst-case voltage drop across the varistor. The upper limit of the tolerance band is shown.

The 1 mA “deviding line” in between those two segments does not really have an electrophysical significance but is generally used as a standard reference (varistor voltage – please refer to section 1.7.5 for explanations).

Related branches are identified by the same maximum AC operating voltage (here “14”).

V/*I* characteristic 1 in figure 7a shows the mean value of the tolerance band between the limits indicated by dashed lines. The mean at 1 mA represents the varistor voltage, in this case 22 V. The tolerance K $\triangleq \pm$ 10 % refers to this value, so at this point the tolerance band ranges from 19,8 to 24,2 V.

Leakage current at operating voltage:
A maximum permissibe operating voltage of 18 V_{DC} is specified for SIOV-S14K14. For this, depending on where the varistor is in the tolerance band (figure 7a), you can derive a leakage current between $6 \cdot 10^{-6}$ A and $2 \cdot 10^{-4}$ A (region 2). If the varistor is operated at a lower voltage, the figure for the maximum possible leakage current also drops (e. g. to max. $2 \cdot 10^{-6}$ A at 10 V_{DC}).

In the worst case, the peak value of the maximum permissible AC operating voltage ($v = \sqrt{2} \cdot 14 =$ 19,8 V) will result in an ohmic peak leakage current of 1 mA (point 3).

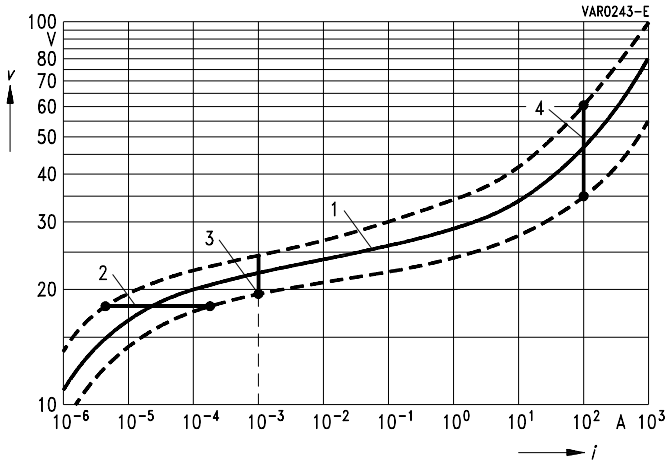
Protection level:
Assuming a surge current of 100 A, the voltage across SIOV-S14K14 will increase to between 35 V and 60 V (region 4), depending on where the varistor is in the tolerance band.

1.6.4 Overlapping *V*/*I* characteristics

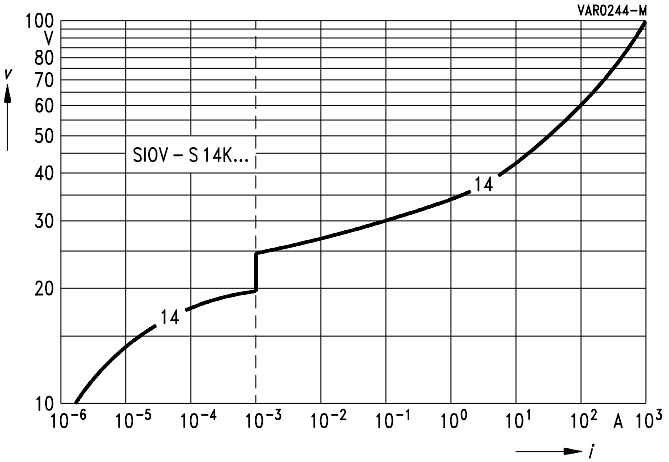
As explained earlier (section 1.3) the differences in non-linearity between voltage classes up to K40 and K50 and above lead to overlapping *V*/*I* curves.

In particular with SIOV-S and SIOV-CU, before selecting voltage rating K40, one should always check whether K50 is not a more favorable solution. Firstly, the protection level is lower for higher surge currents, and secondly, the load capability of K50 is considerably higher for varistors of the same diameter. This consideration does not apply for multilayer varistors since the same ceramic material is used for all voltage ratings in these components.

7a



7b



Figures 7a and b Tolerance limits of a metal oxide varistor with SIOV-S14K14 taken as example

1.7 Terms and descriptions

1.7.1 Operating voltage

The product tables specify maximum AC and DC operating voltages. These figures should only be exceeded by transients. Automotive types, however, are rated to withstand excessive voltage (jump start) for up to 5 minutes.

The leakage current at specified operating voltage is negligible.

The maximum permissible AC operating voltage is used to classify the individual voltage ratings within the type series.

In most applications the operating voltage is a given parameter, so the varistors in the product tables are arranged according to maximum permissible operating voltage to facilitate comparison between the individual varistor sizes.

1.7.2 Surge current, transient

Short-term current flow – especially when caused by overvoltage – is referred to as surge current or transient.

The maximum surge current that can be handled by a metal oxide varistor depends on amplitude, pulse duration and number of pulses applied over device lifetime. The ability of a varistor to withstand a single pulse of defined shape is characterized by the maximum non-repetitive surge current specified in the product tables (single pulse, $t_r \leq 20$ µs).

If pulses of longer duration or multiple pulses are applied, the surge current must be derated as described in section 1.8.

Maximum surge current

The maximum non-repetitive surge current is defined by an 8/20 µs waveform (rise time 8 µs/decay time to half value 20 µs) according to IEC 60060 as shown in figure 8a. This waveform approximates a rectangular wave of 20 µs. The derating curves of the surge current, defined for rectangular waveforms, consequently show a knee between horizontal branch and slope at 20 µs.

1.7.3 Energy absorption

The energy absorption of a varistor is correlated with the surge current by

$$W = \int_{t_0}^{t_1} v(t)\,i(t)\,\mathrm{d}t \qquad \text{(equ. 6)}$$

where $v(t)$ is the voltage drop across the varistor during current flow.

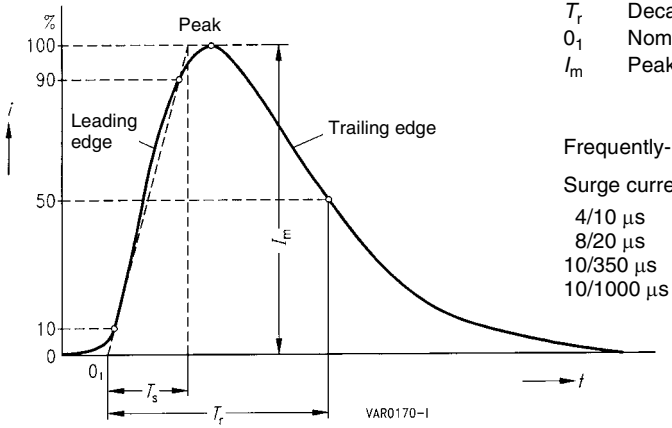
Figure 42 on page 82 illustrates the electrical performance for the absorption of 100 J in the case of SIOV-S20K14AUTO.

Maximum energy absorption

Surge currents of relatively long duration are required for testing maximum energy absorption capability. A rectangular wave of 2 ms according to IEC 60060 (figure 8b) is commonly used for this test.

In the product tables the maximum energy absorption is consequently defined for a surge current of 2 ms.

8a

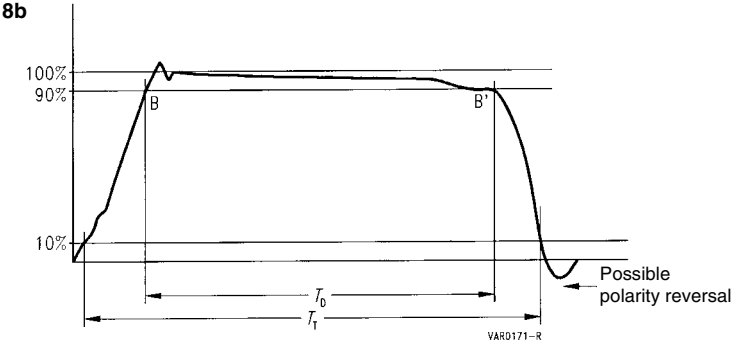


T_s Rise time in µs
T_r Decay time to half value in µs
0_1 Nominal start
I_m Peak value

Frequently-used T_s/T_r ratios:

Surge currents	Surge voltages
4/10 µs	1,2/50 µs
8/20 µs	10/700 µs
10/350 µs	
10/1000 µs	

8b



T_D Duration of peak value (≈ 2 ms)
T_T Total duration

Figures 8a and b Waveforms to IEC 60060 standard

1.7.4 Average power dissipation

If metal oxide varistors are selected in terms of maximum permissible operating voltage, the resulting power dissipation will be negligible.

However, the rated maximum power dissipation must be taken into account if the varistor has not enough time to cool down between a number of pulses occurring within a specified isolated time period.

The examples in section 4 show the calculation of the minimum time interval in periodic application of energy.

1.7.5 Varistor voltage

The varistor voltage is the voltage drop across the varistor when a current of 1 mA is applied to the device. It has no particular electrophysical significance but is often used as a practical standard reference in specifying varistors.

1.7.6 Tolerance

Tolerance figures refer to the varistor voltage at 25 °C. As shown by figure 7a the tolerance band for other current values can be larger.

Note:
When the tolerance is examined, the current of 1 mA must only be applied briefly so that the results are not corrupted by warming of the varistor (see temperature coefficient). The current should only flow for 0,2 up to 2,0 s, typical is a duration of 1 s.

1.7.7 Protection level (clamping voltage)

The protection level is the voltage drop across the varistor for surge currents > 1 mA.

The *V/I* characteristics show the maximum protection level as a function of surge current (8/20 µs waveform).

In the product tables the protection level for surge currents according to the R10 series (ISO 497) is additionally specified. This is also referred to as clamping voltage.

1.7.8 Capacitance

The product tables specify typical capacitance figures for 1 kHz resp. 1 MHz.

The tabulated values show that metal oxide varistors behave like capacitors with ZnO dielectric. The capacitance rises in proportion to disk area (and thus to current handling capability) and drops in proportion to the distance of the electrodes, i. e. it decreases with increasing protection level.

Capacitance values are not subject to outgoing inspection (except for SHCV and the LC, CC and HC versions of the MLV series).

1.7.9 Response behavior, response time

The response time of metal oxide varistor ceramics to transients is in the subnanosecond region, i. e. varistors are fast enough to handle even ESD transients with the extreme steep current rise of up to 50 A/ns.

You can find similar results for the die of the silicon used in semiconductor protective devices like suppressor diodes.

However, when the die is mounted in its package, the response time increases due to the series inductance of its package to values > 1 ns.

The varistors specified in this data book have the following response times:

Leaded parts, block and strap versions	< 25 ns
SMD molded (CU series)	< 10 ns
SMD multilayer	< 0,5 ns

Reason for the different response time figures is the different series inductance of the package styles.

The product tables shows typical inductance figures of only 1 to 3 nH for the multilayer chip varistors (MLV). These extremely low figures make the MLV series ideal for ESD protection requirements.

Comparing the protection behavior of varistors with semiconductors, higher figures of protection levels may be found for varistors. This cannot be explained by a higher response time of varistors – which definitely is not true – but rather it is due to a slightly less non-linearity of the *V*/*I* characteristics.

The *V*/*I* characteristics in this data book have been measured at currents > 1 mA with the standard 8/20 µs waveform (figure 8a). So they allow for the inductive voltage drop across the varistor for the particular d*i*/d*t*.

If surge currents with steep edges are to be handled, one should always design the circuit layout for as low an inductance as possible.

1.7.10 Temperature coefficient

Metal oxide varistors show a negative *TC* of voltage. Figure 9 shows the typical varistor behavior.

The *TC* value drops decidedly with rising currents and is completely negligible from roughly 1 mA upwards.

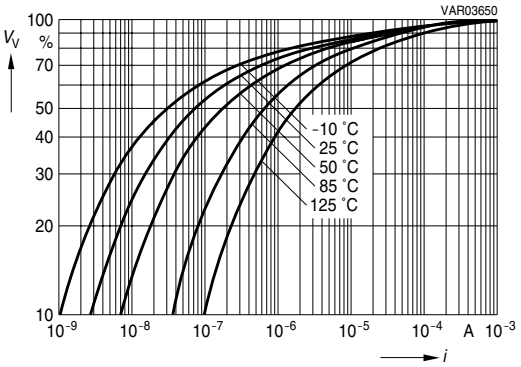


Figure 9 Typical temperature dependance of the *V*/*I* characteristic taking SIOV-S20K275 as an example.
(V_V = applied DC voltage in percentage of varistor voltage at + 25 °C)

An increase in leakage current is consequently noticeable at higher temperatures, especially in the μA region.

Equation 7 describes the *TC* of varistor voltage (at 1 mA):

$|TC| < 0{,}5 \cdot 10^{-3}/K = \ 0{,}05\%/K = 1\%/\Delta 20\,K$ (equ. 7)

Figure 10 shows results for SIOV-S20K275 as an example.

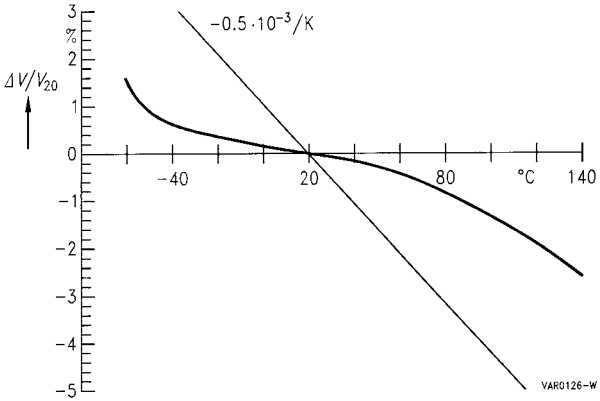


Figure 10 Temperature coefficient of voltage at 1 mA for SIOV-S20K275

1.8 Derating

Derating is the intentional reduction of maximum ratings in the application of a device. With metal oxide varistors derating is of particular interest under the following conditions:

- derating for repetitive surge current and energy absorption,
- derating at increased operating temperatures.

1.8.1 Derating for repetitive surge current

A typical feature of metal oxide varistors is the dependence of the maximum permissible ratings for surge current, and thus for energy absorption, on the pulse shape, pulse duration, an the number of times this load is repeated during the overall lifetime of the varistor.

The derating for a particular maximum permissible surge current can be derived from the curves for a type series in repetition figures graded 10^x. The surge derating curve is mainly dependent on the varistor size but also voltage rating. Such derating curves can be found for all individual varistors in this data book.

The maximum permissible energy absorption can also be calculated from the derating curves by

$W_{max} = v_{max}\, i_{max}\, t_{r\,max}$

1.8.2 Derating at increased operating temperatures

For operating temperatures exceeding 85 °C or 125 °C the following operating conditions of varistors

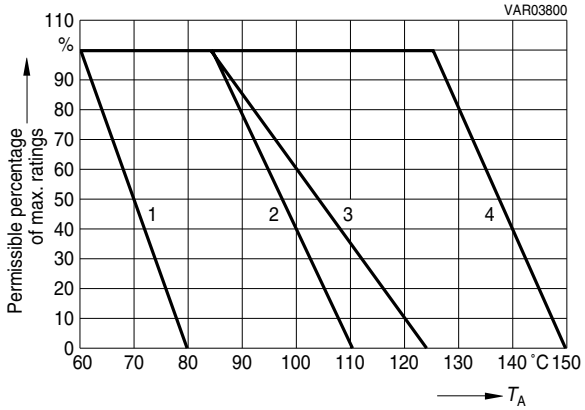
- voltage
- surge current
- energy absorption
- average power dissipation have to be derated according to figure 11.

1.9 Operating and storage temperature

The upper limits of the operating and storage temperature ranges for the individual type series can be deduced from the 100 % and 0 % values in figure 11, respectively. For lower ratings, please refer to the product tables.

1.10 Climatic categories

The limit temperatures according to IEC 60068 are stated in the product tables as LCT (**L**ower **C**ategory **T**emperature) and UCT (**U**pper **C**ategory **T**emperature).



Derating curve 1	Derating curve 2	Derating curve 3	Derating curve 4
SIOV- E	SIOV- B LS	SIOV- CT/CN0402…0603 CA CT/CN1812TELE CT/CN1812S60…95A CU…AUTO S…(AUTO)(E2)(E3) SR Q	SIOV- CT/CN0603AUTO CT/CN0805…2220(AUTO) CT/CN0805…2220AUTO S…AUTOD1

Figure 11 Temperature derating for operating voltage, surge current, energy absorption and average power dissipation

1.11 Overload response

1.11.1 Moderate overload

Surge currents or continuous overload of up to approx. one and a half times the specified figures can lead to a change in varistor voltage by more than ± 10%. In most cases the varistor will not be destroyed, but there may be an irreversible change in its electrical properties.

1.11.2 Heavy overload

Surge currents far beyond the specified ratings will puncture the varistor element. In extreme cases the varistor will burst.

Excessive steady-state overload fuses the ZnO grains and conducting paths are formed with the bulk resistance of ZnO, which is considerably lower than the resistance of the original varistor. The overload can overheat the varistor ceramic to the effect that it becomes unsoldered from the electrodes.

1.12 Design notes

If steep surge current edges are to be expected, you must make sure that your design is as low-inductive as possible (cf 1.7.9).

1.12.1 Physical protection, fuses

Due to the unpredictable nature of transients a varistor may be overloaded although it was carefully selected. Overload may result in package rupture and expulsion of hot material. For this reason the varistor should be physically shielded from adjacent components, e. g. by a suitable metal case.

Fuse protection of varistors against excessive surge current is usually not possible because standard fuses are unable to quench surge currents. But fuses can offer protection against damage caused by follow-on currents. Such follow-on currents flow when a damaged varistor is in low-resistance mode and still connected to power.

When varistors are operated on standard line impedances, nominal fuse currents and varistor type series should be matched as follows:

Type	S05 CU3225	S07 CU4032	S10	S14	S20 Q14	Q20
Nominal fuse current [A]	≤ 1	≤ 3	≤ 6	≤ 10	≤ 16	≤ 25

Type	B32	B40/LS40	B60/LS50	B80
Nominal fuse current [A]	≤ 50	≤ 80	≤ 125	≤ 160

In applications where the conditions deviate from standard power line impedances, better fuse protection of the varistor can be obtained using thermo-fuses. These thermo-fuses should be in direct thermal contact with the varistor.

1.12.2 Potting and sealing, adhesion

Potting, sealing or adhesive compounds can produce chemical reactions in the varistor ceramic that will degrade its electrical characteristics. Information about this is available on inquiry.

1.12.3 Soldering

Varistors with wire leads and versions with strap terminals as well as encapsulated varistors can be soldered using all conventional methods.

Multilayer varistors can be provided with a nickel barrier termination or with silver-palladium termination.

The usage of mild, non-activated fluxes for soldering is recommended as well as a proper cleaning of the PCB.

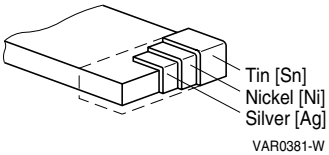


Figure 12a Multilayer varistor: Structure of nickel barrier termination

- Nickel barrier termination (SIOV-CT …)

  The nickel barrier layer of the silver/nickel/tin termination (figure 12a) prevents leaching of the silver base metalization layer. This allows great flexibility in the selection of soldering parameters. The tin prevents the nickel layer from oxidizing and thus ensures better wetting by the solder. The nickel barrier termination is suitable for all commonly-used soldering methods. Figures 13a and 13b show recommended temperature profiles.

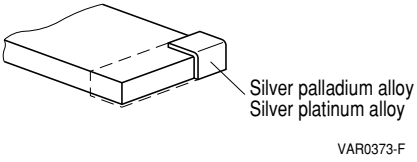


Figure 12b Multilayer varistor: Structure of silver palladium and silver platinum termination

- Silver palladium termination (SIOV-CN …)

  AgPd metallization (figure 12b) is suitable for all common soldering methods. Figures 13a and 13b show recommended temperature profiles.

- Silver platinum termination (SIOV-CN/CA … K2)

  Silver-platinum termination is particularly suitable for soldering delicate structures. For this reason AgPt alloys of this kind (figure 12b) are used in our smallest type series 0402 and in varistor arrays, these being identified by a “K2” suffix to the type designation.

  AgPt termination has been especially developed for reflow soldering methods with reduced temperature profiles. It achieves excellent solder wetting at these reduced soldering temperatures (cf. figure 13c for recommended temperature profile).

  Please note: Do not use wave soldering nor vapor-phase soldering techniques.

Recommended soldering profiles

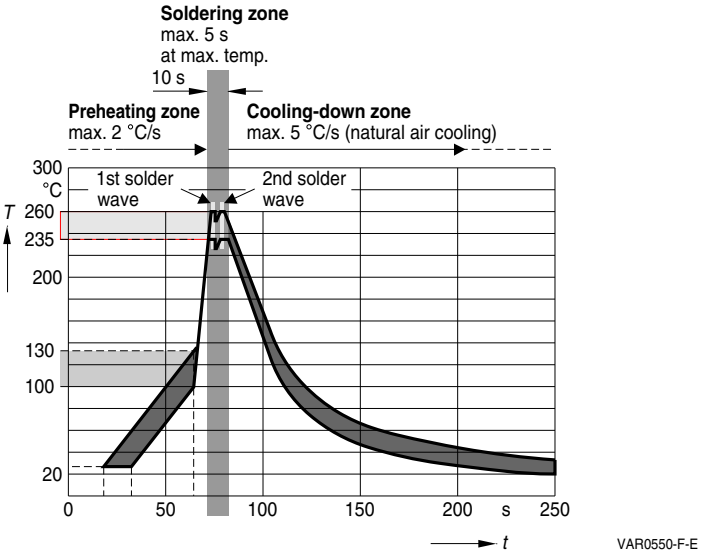


Figure 13a Recommended temperature profile for wave soldering

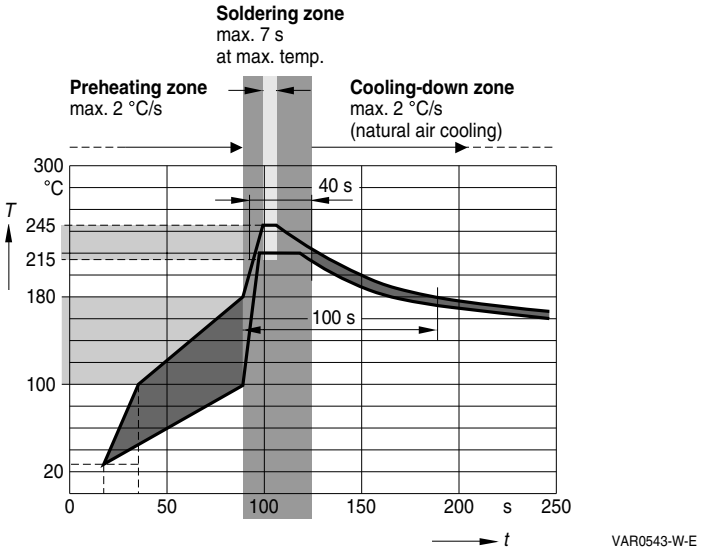


Figure 13b Recommended temperature profile for reflow soldering (except AgPt termination)

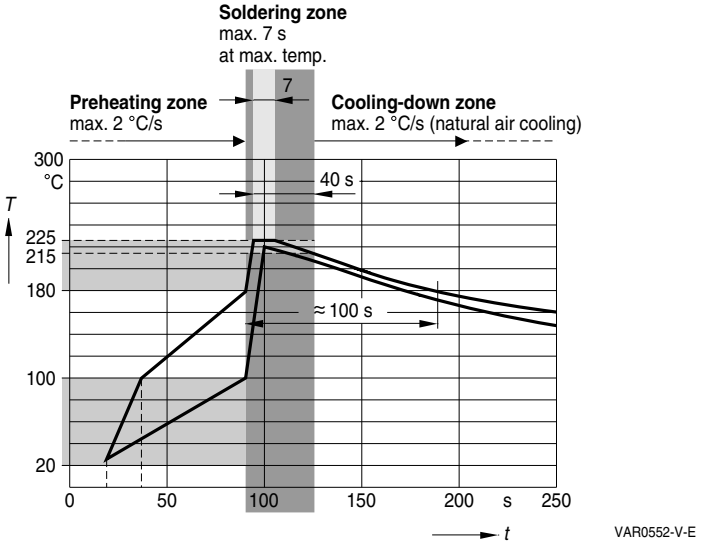


Figure 13c Recommended temperature profile for reflow soldering at reduced temperature (AgPt termination)

1.12.4 Storage

The SIOV type series should be soldered after shipment from EPCOS within the time specified:

SIOV-	S, SR, Q, LS, CU	24 months
	CT	12 months
	CN, CN … K2, CA … K2	6 months

The parts are to be left in the original packing in order to avoid any soldering problems caused by oxidized terminals. Storage temperature – 25 to 45 °C.

Max. relative humidity (without condensation): < 75 % annual average,
< 95 % on max. 30 days per annum.

1.12.5 Prior damage

The values specified only apply to varistors which have not been subjected to prior electrical, mechanical or thermal damage.

1.12.6 Environmental conditions

SIOV varistors are designed for indoor applications. On all accounts, prevent exposure to:

- direct sunlight,
- rain or condensation,
- steam, saline spray,
- corrosive gases,
- atmospheres with reduced oxygen content.

1.12.7 Mechanical strength of wire leads of disk-type varistors

The wire leads comply with the requirements of IEC 60068-2-2. They may only be bent at a minimum distance of 4 mm from the enamel coating end. When bending leads to shape, the lead-component junction must be supported. The minimum bend radius should be 0,75 mm.

1.13 Designation system

Varistor = **Var**iable Res**istor**
SIOV ® = Registered tradename for EPCOS varistors
SHCV = **S**uper **H**igh **C**apacitive **V**aristor (“Hicap varistor”)

Table 1

SIOV SHCV	Design	Area	Tolerance	Max. AC Oper. Volt.	Additional	Specifications

Design	**B**	Block type (HighE series)
	CA … K2	Chip array, multilayer
	CM	Chip, monolithic, not molded
	CN	Chip, multilayer with AgPd termination
	CN … K2	Chip, multilayer with AgPt termination
	CT	Chip, multilayer, with nickel barrier termination
	CU	Chip, monolithic, molded
	E	Arrester block
	LS … QP	Strap type, square, epoxy coating, bent straps (HighE series)
	LS … PK2	Strap type, square, epoxy coating, straight straps (HighE series)
	Q	Disk type, square, leaded (EnergetiQ series)
	S	Disk type, round, leaded
	SR	Disk type, multilayer, rectangular, leaded

Area of varistor element Length × width in 1/100 inch (EIA Standard)	0402 = 4”/100 × 2”/100 = 1,0 mm × 0,5 mm . . . 2220 = 22”/100 × 20”/100 = 5,7 mm × 5,0 mm
Area of varistor encapsulation	3225 = 32”/100 × 25”/100 = 8,0 mm × 6,3 mm 4032 = 40”/100 × 32”/100 = 10,0 mm × 8,0 mm
Abbreviation for SHCV area	1 = 1812 2 = 2220
Rated diameter of varistor disk in mm	05 to 80

Tolerance of varistor voltage (1 mA)	K ± 10 % L ± 15 % M ± 20 % S…A/B/C Special tolerance A, resp. B, resp. C Note: not valid for arrester blocks.

Table 1 (continued)

Max. permissible ac operating voltage	4 to 1100	$V_{RMS\ max.}$
Rated voltage (arrester blocks)	VR302	$30 \cdot 10^2$ V = 3 kV
Capacitance tolerance (SHCVs only)	M	± 20 %
Capacitance (SHCVs only)	474	$47 \cdot 10^4$ pF = 0,47 µF
Code letter for capacitor ceramic material (SHCVs only)	X Z	X7R Z5U

Taping	G	Tape / reel
	GA	Tape / Ammopack
	G.S.	Tape / reel, crimp style S, S2, S3, S4, S5 (see page 212)
Appendix	AUTO	Additional load dump and jump start specification
	AUTO … D1	Additional load dump, jump start and high-temperature specification
	CC	Controlled capacitance (defined tolerance range)
	HC	High capacitance (defined minimum rating)
	LC	Low capacitance (defined maximum rating)
	E2	AdvanceD series
	E3	SuperioR series
	K2	Suffix to define modifications
	M	Customer specific trimmed lead length (in mm)
	P	Standard coating (Epoxy)
	Q	Square shape
	TELE	Additional telecom specification
	R5	= 5,0 Lead spacing differs from standard
	R7	= 7,5 Lead spacing differs from standard

Production code: all coated varistors are marked with year/week code.
Example: 0009 = 9th week of year 2000

Abbreviations for Metal Oxide Varistors:

MOV metal oxide varistor
ZnO zinc oxide varistor
VDR voltage-dependent resistor
MLV multilayer varistor

Abbreviation for overvoltage protection elements in general:
TVSS transient voltage surge suppressor

1.14 Marking of disk varistors

Disk-type varistors have printed markings as shown in figure 14. They are distinguished as follows: no underline under the “S” (Standard), an additional underline under the S… (for type series AdvanceD) or a line above the S… (for type series SuperioR).

The lower section of the marking area contains the date code yyww.

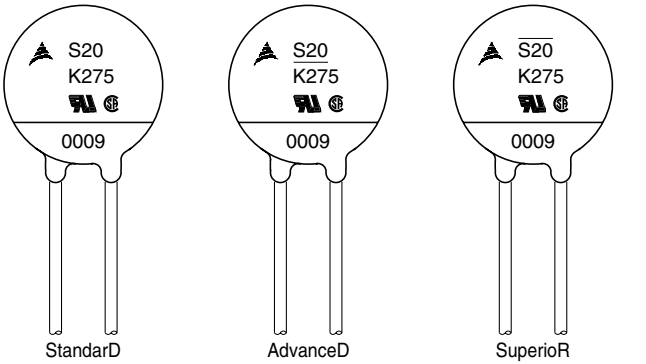


Figure 14 Various forms of printed markings of disk-type varistor series StandarD, AdvanceD and SuperioR, using the S20K275 as an example.
Date code 0009 ≙ yyww ≙ 9th week of year 2000

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